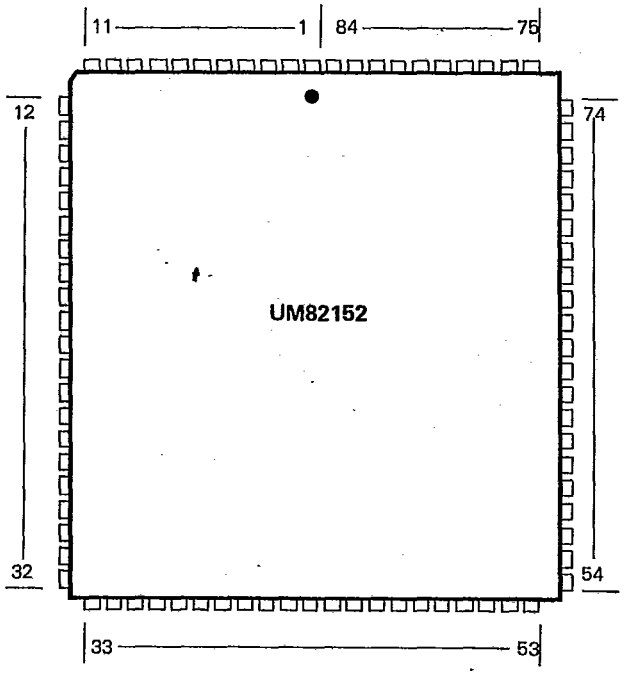
UM82152 Cache Controller

Features

- Controls 32-kB, 4-way, set-associative cache
- Available in 16-MHz, 20-MHz, and 25-MHz speeds
- Direct interface to the 80386
- Direct interface to industry-standard 8K x 8 SRAMs:
  45 ns for 16-MHz systems
  35 ns for 20-MHz systems
  25 ns for 25-MHz systems
- Full 32-bit addressability for 4-GB memory support
- Cache coherency support
- Software cache invalidation
- On-chip programmable noncached regions
- Write buffer support
- Gate A20 support
- 1.5 micron CMOS technology
- 84-lead PLCC, JEDEC standard package
- Pin and functionally identical to A38152*

Pin Configuration



Pin No	Signal	Pin No	Signal	Pin No	Signal
1	GND	29	CACHE-ADDR10	57	ADDR16
2	ADDR2	30	CACHE-ADDR9	58	ADDR17
3	BE0#	31	CACHE-ADDR8	59	ADDR18
4	BE1#	32	CACHE-ADDR7	60	ADDR19
5	BE2#	33	GND	61	ADDR20
6	BE3#	34	ADDR12	62	ADDR21
7	W/R#	35	ADDR11	63	ADDR22
8	CACHE-ADDR6	36	ADDR10	64	GND
9	CACHE-ADDR5	37	ADDR9	65	ADDR23
10	CACHE-ADDR4	38	ADDR8	66	ADDR24
11	CACHE-ADDR3	39	ADDR7	67	ADDR25
12	CACHE-ADDR2	40	ADS#	68	ADDR26
13	GND	41	V_{CC}	69	ADDR27
14	SYS-WR#	42	CLK2	70	ADDR28
15	SYS-RD#	43	GND	71	ADDR29
16	V_{CC}	44	V_{CC}	72	ADDR30
17	SYS-ACK#	45	RESET	73	ADDR31
18	OE#	46	SAMPLE	74	IO-ADDR3
19	W3#	47	NON-CACHE#	75	V_{CC}
20	W2#	48	NA#	76	IO-ADDR2
21	W1#	49	LOCK#	77	IO-ADDR1
22	W0#	50	DMA#	78	IO-ADDR0
23	CACHE-ADDR1	51	READY#	79	D/C#
24	CACHE-ADDR0	52	CACHE-FAULT	80	M/IO#
25	GND	53	ADDR13	81	ADDR6
26	CACHE-ADDR12	54	V_{CC}	82	ADDR5
27	V_{CC}	55	ADDR14	83	ADDR4
28	CACHE-ADDR11	56	ADDR15	84	ADDR3

***A38152 is AUSTEK's cache controller for 25 MHz 386 AT system.**