TVP3026
Data Manual

Video Interface Palette

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1 Introduction

The TVP3026 is an advanced video interface palette (VIP) from Texas Instruments implemented in EPIC™ 0.2-micron CMOS process. The TVP3026 is a 64-bit VIP that supports packed-24 modes enabling 24-bit true color and high resolution at the same time without excessive amounts of frame buffer memory. For example, a 24-bit true color display with 1280 x 1024 resolution may be packed into 4M of VRAM. A PLL-generated, 50 % duty cycle reference clock is output in the packed-24 modes, maximizing VRAM cycle time and the screen refresh rate.

The TVP3026 supports all of the pixel formats of the TVP3020 VIP. Data can be split into 4 or 8 bit planes for pseudo-color mode or split into 12-, 16- or 24-bit true-color and direct-color modes. For the 24-bit direct color modes, an 8-bit overlay plane is available. The 16-bit direct- and true-color modes can be configured to IBM XGA® (5, 6, 5), TARGA® (1, 5, 5, 5), or 16-bit/pixel (6, 6, 4) configuration as another existing format. An additional 12-bit mode with 4-bit overlay (4, 4, 4, 4) is supported with 4 bits for each color and overlay. All color modes support selection of little or big endian data format for the pixel bus. Additionally, the device is also software compatible with the INMOS™ IMSG176/8 and Brooktree™ Bt476/8 color palettes.

Two fully programmable phase-locked loops (PLLs) for pixel clock and memory clock functions are provided, as well as a simple frequency doubler for dramatic improvements in graphics system cost and integration. A third loop clock PLL is incorporated making pixel data latch timing much simpler than with other existing color palettes. In addition, four digital clock inputs (2 TTL- and 2 ECL/TTL-compatible) may be utilized and are software selectable. The video clock provides a software selected divide ratio of the chosen pixel clock. The shift clock output may be used directly as the VRAM shift clock. The reference clock output is driven by the loop clock PLL and provides a timing reference to the graphics accelerator.

Like the TVP3020, the TVP3026 also integrates a complete IBM XGA-compatible hardware cursor on chip, making significant graphics performance enhancements possible. Additionally, hardware port select and color-keyed switching functions are provided, giving the user several efficient means of producing graphical overlays on direct-color backgrounds.

The TVP3026 has three 256-by-8 color lookup tables with triple 8-bit video digital-to-analog converters (DACs) capable of directly driving a doubly terminated 75-Ω line. The lookup tables are designed with a dual-ported RAM architecture that enables ultra-high speed operation. Sync generation is incorporated on the green output channel. Horizontal sync (HSYNC) and vertical sync (VSYNC) are pipeline delayed through the device and optionally inverted to indicate screen resolution to the monitor. A palette-page register is available to select from multiple color maps in RAM when 4 bit planes are used. This allows the screen colors to be changed with only one microprocessor write cycle.

The device features a separate VGA bus which supports the integrated VGA modes in graphics accelerator applications, allowing efficient support for VGA graphics and text modes. The separate bus also is useful for accepting data from the feature connector of most VGA-supported personal computers, without the need for external data multiplexing.

The TVP3026 is highly system integrated. It can be connected to the serial port of VRAM devices without external buffer logic and connected to many graphics engines directly. It also supports the split shift-register transfer function, which is common to many industry standard VRAM devices.

The system-integration concept is even carried further to manufacturing test and field diagnosis. To support these, several highly integrated test functions have been designed to enable simplified testing of the palette and the entire graphics system.

1.1 Features

There are many features that the TVP3026 video interface palette possesses; and, the itemized list of them are:

- Supports system resolutions up to 1600 × 1280 @ 76-Hz refresh rate
- Supports color depths of 4, 8, 16, 24 and 32 bit/pixel
- 64-bit-wide pixel bus
- Versatile direct-color modes:
  - 24-bit/pixel with 8-bit overlay (O, R, G, B)
  - 24-bit/pixel (R, G, B)
  - 16-bit/pixel (5, 6, 5) XGA configuration
  - 16-bit/pixel (6, 6, 4) configuration
  - 15-bit/pixel with 1 bit overlay (1, 5, 5, 5) TARGA configuration
  - 12-bit/pixel with 4 bit overlay (4, 4, 4, 4)
- True-color gamma correction
- Supports packed pixel formats for 24 bit/pixel using a 32-or 64-bit/pixel bus
- 50% duty cycle reference clock for higher screen refresh rates in packed-24 modes
- Programmable frequency synthesis phase-locked loops (PLLs) for dot clock and memory clock
- Loop clock PLL compensates for system delay and ensures reliable data latching
- Versatile pixel bus interface supports little- and big-endian data formats
- 135-, 175-, and 220-MHz versions
- On-chip hardware cursor, 64 × 64 × 2 cursor (XGA and X-windows functionally compatible)
- Direct interfacing to video RAM
- Supports overscan for creation of custom screen borders
- Color-keyed switching of direct color and true color or overlay
- Hardware port select switching between direct color and true color or overlay
- Triple 8-Bit D/A converters
- Analog output comparators for monitor detection
- RS-343A compatible outputs
- Direct VGA pass-through capability
- Palette page register
- Horizontal zooming capability

1.2 Functional Block Diagram

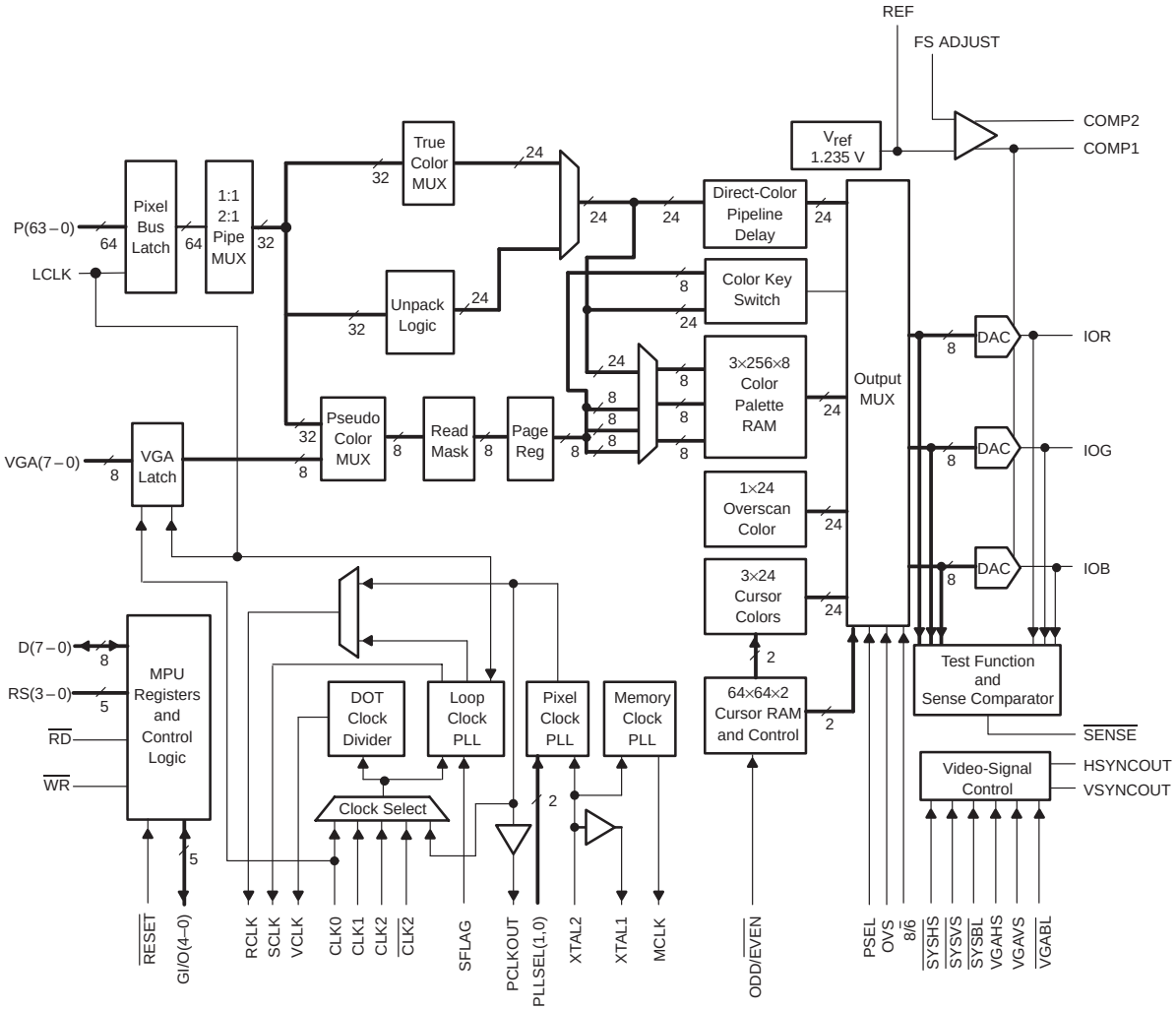
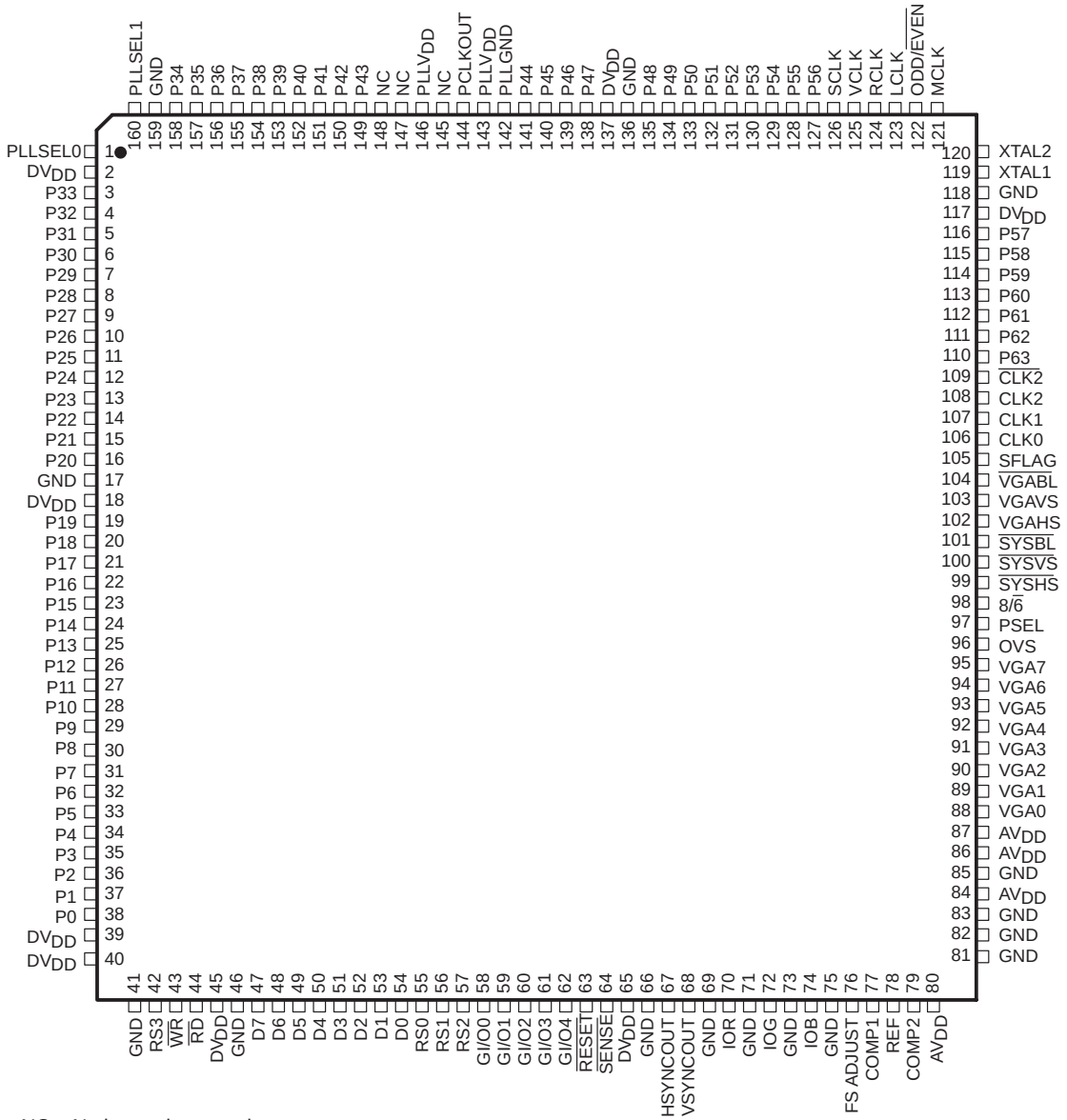


Figure 1–1. Functional Block Diagram

1.3 Terminal Assignments



NC – No internal connection

Figure 1–2. Terminal Assignments

1.4 Ordering Information

TVP3026 – XXX XXXX

Pixel Clock Frequency Indicator

MUST CONTAIN THREE CHARACTERS:

- –135: 135-MHz pixel clock (revision A only)
- –175: 175-MHz pixel clock
- –220: 220-MHz pixel clock
- –250: 250-MHz pixel clock

Device Revision

MUST CONTAIN ONE LETTER:

- A
- B

Package

MUST CONTAIN THREE LETTERS:

- PCE: Plastic, Quad Flat Pack
- MDN: Metal, Quad Flat Pack

1.5 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{DD}	80, 84, 86, 87		Analog power. All AV_{DD} terminals must be connected. A separate cutout in the DV_{DD} plane should be made for AV_{DD}. The DV_{DD} and AV_{DD} planes should be connected only at a single point through a ferrite bead close to where power enters the board.
CLK0	106	I	Dot clock 0 TTL input. CLK0 can be selected to drive the dot clock at frequencies up to 140 MHz. When using the VGA port, the maximum frequency is 85 MHz. CLK0 can be selected as the latch clock for VGA data and video controls. (power-up default).
CLK1	107	I	Dot clock 1 TTL input. CLK1 can be selected to drive the dot clock at frequencies up to 140 MHz.
CLK2, $\overline{CLK2}$	108, 109	I	Dual-mode dot clock input. These inputs are emitter-coupled logic (ECL)-compatible inputs. Alternatively, CLK2 and $\overline{CLK2}$ may be used as individual TTL clock inputs. Programming the clock selection register selects the chosen configuration. These inputs may be selected as the dot clock up to the device limit while in the ECL mode or up to 140 MHz in the TTL mode.
COMP1, COMP2	77, 79	I	Compensation. COMP1 and COMP2 provide compensation for the internal reference amplifier. A 0.1-µF ceramic capacitor is required between COMP1 and COMP2. This capacitor must be as close to the device as possible to avoid noise pick up.
DV_{DD}	2, 18, 39, 40, 45, 65, 117, 137		Digital power. All DV_{DD} terminals must be connected to the digital power plane with sufficient decoupling capacitors near the TVP3026.
D7–D0	47–54	I/O	MPU interface data bus. Data is transferred in and out of the register map, palette RAM, and cursor RAM on D7–D0.

NOTE 1: All unused inputs should be tied to a logic level and not allowed to float.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
FS ADJUST	76	I	Full-scale adjustment. A resistor connected between FS ADJUST and GND controls the full-scale range of the DACs.
GND	17, 41, 46, 66, 69, 71, 73, 75, 81–83, 85, 118, 136, 159		Ground. All GND terminals must be connected. A common ground plane should be used.
HSYNCOUT, VSYNCOUT	67, 68	O	Horizontal and vertical sync outputs. These outputs are pipeline delayed versions of the selected sync inputs. Output polarity inversion may be independently selected using general control register bits GCR(1,0).
IOR, IOG, IOB	70, 72, 74	O	Analog current outputs. These outputs can drive a 37.5-Ω load directly (doubly terminated 75-Ω line), thus eliminating the requirement for any external buffering.
GI/O4 – GI/O0	58 – 62	I/O	Software programmable general I/O terminals that can be used to control external devices.
LCLK	123	I	Latch clock input. LCLK latches pixel-bus-input data and system video controls. VGA data may also be latched with LCLK when selected. LCLK may be a delayed version of RCLK provided that linear phase changes in RCLK cause corresponding linear phase changes in LCLK.
MCLK	121	O	Memory clock output. MCLK is the output of an independently programmable PLL frequency synthesizer. The frequency range is 14 – 100 MHz. The dot clock may be output on this terminal while the MCLK frequency is reprogrammed. See subsection 2.4.2.1, *Changing the MCLK Frequency.*
PCLKOUT	144	O	Pixel clock PLL output. PCLKOUT is a buffered version of the pixel clock PLL output and is mainly for test purposes. This output is independent of the dot clock source selected by the clock selection register.
PLLGND	142		Ground for PLL supplies. Decoupling capacitors should be connected between $PLLV_{DD}$ and PLLGND. PLLGND should be connected to the system ground through a ferrite bead.
$PLLV_{DD}$	143, 146		PLL power supply. $PLLV_{DD}$ must be a well regulated 5-V power supply voltage. Decoupling capacitors should be connected between $PLLV_{DD}$ and PLLGND. Terminal 143 supplies power to the pixel clock PLL. Terminal 146 supplies power to the MCLK PLL and the loop clock PLL.
OVS	96	I	Overscan input. OVS controls the display of custom screen borders. When OVS is not used, it should be connected to GND.
ODD/$\overline{\text{EVEN}}$	122	I	Odd or even field display. ODD/$\overline{\text{EVEN}}$ indicates odd or even field during interlaced display for cursor operation. A low signal indicates the even field and a high signal indicates the odd field. See subsection 2.7.4, *Interlaced Cursor Operation*, for cursor operation in interlace mode.
PLLSEL0, PLLSEL1	1, 160	I	Pixel clock PLL frequency selection. PLLSELx selects among two fixed frequencies and the programmed frequency of the pixel clock PLL.

NOTE 1: All unused inputs should be tied to a logic level and not allowed to float.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PSEL	97	I	Port select. PSEL provides the capability of switching between direct color and true color or overlay. Multiple true color or overlay windows may be displayed using the PSEL control. Since PSEL is sampled with LCLK, the granularity for switching depends on the number of pixels loaded per LCLK. When PSEL is not used, it should be connected to GND.
P63–P0	3–16, 19–38, 110–116, 127–135, 138–141, 149–158	I	Pixel input port. The port can be used in various modes as described in Section 2.6, Multplexing Modes of Operation. Unused terminals should not be allowed to float.
RCLK	124	O	Reference clock output. RCLK can be programmed to output either the pixel clock PLL (power up default) or the loop clock PLL. The pixel clock PLL is selected to provide a reference clock to the VGA controller. In this configuration, the VGA controller returns VGA data and video controls along with a synchronous clock which becomes the TVP3026 dot clock source using CLK0. For all other modes, the loop clock PLL is selected to provide the reference clock. In this configuration, the pixel clock PLL (or external clock) becomes the TVP3026 dot clock source. The reference clock is used to generate VRAM shift clocks (or clocks a VGA controller) and generate video controls. The pixel port (or VGA port) and video controls are latched by LCLK. The loop clock PLL controls the phase of RCLK to phase-lock the received LCLK with the internal dot clock. For systems that use SCLK as the VRAM shift clock, RCLK should be connected to LCLK. An external buffer may be used between RCLK and LCLK when SCLK is also buffered, within the timing constraints of the TVP3026. RCLK is not gated off during blanking.
REF	78	I/O	Voltage reference for DACs. An internal voltage reference of nominally 1.235 V is provided that requires an external 0.1-µF ceramic capacitor between REF and analog GND. However, the internal reference voltage can be overdriven by an externally-supplied reference voltage.
$\overline{\text{RESET}}$	63	I	Master reset. All the registers assume their default state after reset. The default state is VGA mode 2 (CLK0 latching of VGA data and video controls).
$\overline{\text{RD}}$	44	I	Read strobe input. A low signal on $\overline{\text{RD}}$ initiates a read from the register map. Read transfer data is enabled onto the D(7–0) bus when $\overline{\text{RD}}$ is low (see Figure 3–1).
RS3–RS0	42, 55–57	I	Register select inputs. These terminals specify the location in the direct register map that is to be accessed as shown in Table 2–1.
SCLK	126	O	Shift clock output. SCLK is a gated version of the loop clock PLL output and is gated off during blanking. SCLK may drive the VRAM shift clock directly. This is intended for designs in which the graphics controller does not supply the VRAM shift clock.
$\overline{\text{SENSE}}$	64	O	Test mode DAC comparator output signal. $\overline{\text{SENSE}}$ is low when one or more of the DAC output analog levels is above the internal comparator reference of 350 mV ±50 mV.

NOTE 1: All unused inputs should be tied to a logic level and not allowed to float.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
SFLAG	105	I	Split shift register transfer flag. A high pulse on SFLAG during blanking is passed directly to the SCLK terminal. This operation is available to meet the special serial clocking requirements of some VRAM devices. When SFLAG is not used, SFLAG should be connected to GND.
$\overline{\text{SYSBL}}$	101	I	System blank input. $\overline{\text{SYSBL}}$ is active low. This should be selected for all modes other than VGA mode 2. This signal is pipeline delayed before being passed to the DACs.
$\overline{\text{SYSHS}}$, $\overline{\text{SYSVS}}$	99, 100	I	System horizontal and vertical sync inputs. These signals should be selected for all modes other than VGA mode 2. These signals are pipeline delayed and each may be inverted before being passed to the HSYNCOUT and VSYNCOUT terminals. General control register bits GCR(1,0) control the polarity inversion. When used to generate the sync level on the green current output, $\overline{\text{SYSHS}}$ and $\overline{\text{SYSVS}}$ must be active low at the input to the TVP3026.
VCLK	125	O	Programmable auxiliary clock output. VCLK is derived from the internal dot clock using a programmable divide ratio and does not utilize the loop clock PLL for synchronization. Since pixel data and video controls are always referenced to RCLK and LCLK (or CLK0), use of VCLK for the frame buffer interface or video timing is not recommended.
$\overline{\text{VGABL}}$	104	I	VGA blank input. $\overline{\text{VGABL}}$ is active low. This should be selected when in VGA mode 2 (CLK0 latching of VGA data and video controls). $\overline{\text{VGABL}}$ is pipeline delayed before being passed to the DACs.
VGAHS, VGAVS	102, 103	I	VGA horizontal and vertical sync inputs. These signals should be used when in VGA mode 2 (CLK0 latching of VGA data and video controls). These signals are pipeline delayed and each may be inverted before being passed to the HSYNCOUT and VSYNCOUT terminals. General control register bits GCR(1,0) control the polarity inversion. When used to generate the sync level on the green current output, VGAHS and VGAVS must be active low at the input to the TVP3026.
VGA7–VGA0	88–95	I	VGA port. This bus can be selected as the pixel input bus for VGA modes, but it does not allow for any multiplexing.
$\overline{\text{WR}}$	43	I	Write strobe input. A low signal on $\overline{\text{WR}}$ initiates a write to the register map. Write transfer data is latched from the D(7–0) bus with the rising edge of $\overline{\text{WR}}$.
XTAL1, XTAL2	119, 120	I/O	Connections for quartz crystal resonator. XTALx is a reference for the frequency synthesis PLLs. XTAL2 may be used as a TTL reference clock input, in which case XTAL1 is left unconnected.
8/$\overline{6}$	98	I	DAC resolution selection. This terminal is used to select the data bus width (8 or 6 bits) for the DACs and is provided for VGA downward compatibility. When the 8/$\overline{6}$ signal is high, 8-bit bus transfers are used with D7 the MSB and D0 the LSB. For 6-bit bus operation, while the color palette RAM still has the 8-bit information, the data is shifted to the upper six bits and the two LSBs are filled with zeros at the output multiplexer to the DACs. The palette RAM data register zeroes the two MSBs when the palette RAM is read in the 6-bit mode. The function of this terminal may be overridden in software. When not used, the 8/$\overline{6}$ terminal should be connected to GND so that 6-bit VGA operation begins at power up.

NOTE 1: All unused inputs should be tied to a logic level and not allowed to float.

2 Detailed Description

2.1 Microprocessor Unit Interface

The standard microprocessor unit (MPU) interface is supported, giving the MPU direct access to the registers and memories of the TVP3026. The processor interface is controlled using read and write strobes ($\overline{RD}$, $\overline{WR}$), four register select terminals (RS3–RS0), the D7–D0 data terminals, and the 8/$\overline{6}$-select terminal. The 8/$\overline{6}$ terminal is used to select between an 8- or 6-bit-wide data path to the color palette RAM and is provided to maintain compatibility with the IMSG176. See subsection 2.1.1, *8/$\overline{6}$ Operation*.

Table 2–1 lists the direct register map. These registers are addressed directly by the register select lines RS0–RS3. Table 2–2 lists the indirect register map. The index for the indirect register map is loaded into the index register (direct register: 0000). This register also stores the palette RAM write address and cursor RAM write address. The indexed data register (direct register: 1010) is then used to read or write the register pointed to in the indirect register map. The index does not post-increment following accesses to the indirect map.

Table 2–1. Direct Register Map

RS3	RS2	RS1	RS0	REGISTER ADDRESSED BY MPU	R/W	DEFAULT (HEX)
0	0	0	0	Palette/Cursor RAM Write Address/ Index Register	R/W	XX
0	0	0	1	Palette RAM Data	R/W	XX
0	0	1	0	Pixel Read-Mask	R/W	FF
0	0	1	1	Palette/Cursor RAM Read Address	R/W	XX
0	1	0	0	Cursor/Overscan Color Write Address	R/W	XX
0	1	0	1	Cursor/Overscan Color Data	R/W	XX
0	1	1	0	Reserved		
0	1	1	1	Cursor/Overscan Color Read Address	R/W	XX
1	0	0	0	Reserved		
1	0	0	1	Direct Cursor Control	R/W	00
1	0	1	0	Indexed Data	R/W	XX
1	0	1	1	Cursor RAM Data	R/W	XX
1	1	0	0	Cursor-Position X LSB	R/W	XX
1	1	0	1	Cursor-Position X MSB	R/W	XX
1	1	1	0	Cursor-Position Y LSB	R/W	XX
1	1	1	1	Cursor-Position Y MSB	R/W	XX

Table 2–2. Indirect Register Map (Extended Registers)

INDEX	R/W	DEFAULT	REGISTER ADDRESSED BY INDEX REGISTER
0x00			Reserved
0x01	R	0x00†	Silicon Revision
0x02–0x05			Reserved
0x06	R/W	0x00	Indirect Cursor Control
0x07–0x0E			Reserved
0x0F	R/W	0x06	Latch Control
0x10–0x17			Reserved
0x18	R/W	0x80	True Color Control
0x19	R/W	0x98	Multiplex Control
0x1A	R/W	0x07	Clock Selection
0x1B			Reserved
0x1C	R/W	0x00	Palette Page
0x1D	R/W	0x00	General Control
0x1E	R/W	0x00	Miscellaneous Control
0x1F–0x29			Reserved
0x2A	R/W	0x00	General-Purpose I/O Control
0x2B	R/W	XX	General-Purpose I/O Data
0x2C	R/W	XX	PLL Address
0x2D	R/W	XX	Pixel Clock PLL Data
0x2E	R/W	XX	Memory Clock PLL Data
0x2F	R/W	XX	Loop Clock PLL Data
0x30	R/W	XX	Color-Key Overlay Low
0x31	R/W	XX	Color-Key Overlay High
0x32	R/W	XX	Color-Key Red Low
0x33	R/W	XX	Color-Key Red High
0x34	R/W	XX	Color-Key Green Low
0x35	R/W	XX	Color-Key Green High
0x36	R/W	XX	Color-Key Blue Low
0x37	R/W	XX	Color-Key Blue High
0x38	R/W	0x00	Color-Key Control
0x39	R/W	0x18	MCLK/Loop Clock Control
0x3A	R/W	0x00	Sense Test
0x3B	R	XX	Test Mode Data
0x3C	R	XX	CRC Remainder LSB

† Silicon revision register is 0x00 for the first pass silicon (see subsection 2.11.4, *Silicon Revision*).

NOTE 1: Reserved registers should be avoided; otherwise, circuit behavior could deviate from that specified.

Table 2–2. Indirect Register Map (Extended Registers) (Continued)

INDEX	R/W	DEFAULT	REGISTER ADDRESSED BY INDEX REGISTER
0x3D	R	XX	CRC Remainder MSB
0x3E	W	XX	CRC Bit Select
0x3F	R	0x26	ID
0xFF	W	XX	Software Reset

NOTE 1: Reserved registers should be avoided; otherwise, circuit behavior could deviate from that specified.

2.1.1 8/$\overline{6}$ Operation

The 8/$\overline{6}$ terminal is used to select between an 8-bit (set to 1) or 6-bit (reset to 0) data path to the color palette RAM and it is provided in order to maintain compatibility with the INMOS IMSG176. When miscellaneous-control register bit 2 (MSC2) is set to 1, the 8/$\overline{6}$ terminal is disabled and 8/$\overline{6}$ operation is controlled by bit 3 of the miscellaneous-control register (MSC3). The reset default is for the 8/$\overline{6}$ terminal to be enabled (miscellaneous-control register bit 2 = 0, see Section 2.2, *Color Palette RAM*).

2.1.2 Pixel Read-Mask Register

The pixel read-mask register (direct register: 0010) is an 8-bit register used to enable or disable a bit plane from addressing the color-palette RAM in the pseudo-color and VGA modes. Each palette address bit is logically ANDed with the corresponding bit from the read-mask register before going to the palette-page register and addressing the palette RAM.

2.1.3 Palette-Page Register

The palette page register (index: 0x1C) allows selection of multiple color look-up tables stored in the palette RAM when using a mode that addresses the palette RAM with less than 8 bits. When using 1, 2, or 4 bit planes in the pseudo-color or direct-color + overlay modes, the additional planes are provided from the page register before the data addresses the color palette. This is illustrated in Table 2–3.

NOTE

The additional bits from the page register are inserted after the read mask.

The palette-page register specifies the additional bit planes for the overlay field in direct-color modes with less than 8 bits per pixel overlay.

Table 2–3. Allocation of Palette-Page Register Bits

NUMBER OF BIT PLANES	MSB	PALETTE ADDRESS BITS						LSB
8	M	M	M	M	M	M	M	M
4	P7	P6	P5	P4	M	M	M	M
2	P7	P6	P5	P4	P3	P2	M	M
1	P7	P6	P5	P4	P3	P2	P1	M

M = bit from pixel port and Pn = n bit from page register.

2.1.4 Cursor and Overscan Color Registers

The registers for the three cursor colors and the overscan border color are accessed through the direct register map. See Section 2.9, *Overscan Border* description and subsection 2.7.3, *Three-Color 64 X 64 Cursor*, for use of the cursor colors.

The color write address register (direct register: 0100) must be initialized before writing to the color registers. The lower two bits of this register select one of the four color registers according to Table 2–4. The selected 24-bit color register is loaded a byte at a time by writing a sequence of three bytes (red, green, and blue) to the color data register (direct register: 0101). After the blue byte is written, the color address register increments to the next color. All four colors may be loaded with a single write to the color write address register followed by 12 consecutive writes to the color data register.

The color read address register (direct register: 0111) must be initialized before reading from the color registers. The lower two bits of this register select one of the four color registers according to Table 2–4. Next, the color data register (direct register: 0101) is read three times, producing red, green, and blue bytes from the selected register. After the blue byte is read, the color address register is incremented to the next color. All four colors may be read with a single write to the color read address register followed by 12 consecutive reads of the color data register.

The sequence followed by the color address register is overscan color, cursor color 0, cursor color 1, cursor color 2, . . ., etc. The starting point depends on what was written to the color write address or color read address register.

Table 2–4. Color Register Address Format

BIT 1	BIT 0	REGISTER
0	0	Overscan color
0	1	Cursor color 0
1	0	Cursor color 1
1	1	Cursor color 2

2.2 Color-Palette RAM

The color-palette RAM is addressed by an internal 8-bit address register for reading/writing data from/to the RAM. This register is automatically incremented following a RAM transfer, allowing the entire palette to be read/written with only one access of the address register. When the address register increments beyond the last location in RAM, it is reset to the first location (address 0). All read and write accesses to the RAM are asynchronous to the internal clocks but are performed within one dot clock. Therefore, read/write accesses do not cause any noticeable disturbance on the display.

The color palette RAM is 24 bits wide for each location and 8 bits wide for each color. Since a MPU access is 8 bits wide, the color data stored in the palette is eight bits when the 6-bit mode is chosen. When the 6-bit mode is chosen, the two MSBs of color data in the palette have the values previously written. However, when they are read back in the 6-bit mode, the two MSBs are zeros to be compatible with INMOS IMSG176 and Brooktree Bt176. The output multiplexer shifts the six LSB bits to the six MSB positions and fills the two LSBs with 0s after the color palette. The multiplexer then feeds the data to the DAC. The test mode data register and the cyclic redundancy check (CRC) calculation both take data after the output multiplexer, enabling total system verification. The color palette access is described in the following two sections, and it is fully compatible with IMSG176/8 and Bt476/8.

2.2.1 Writing to Color-Palette RAM

To load the color palette, the MPU must first write to the color-palette RAM write address register (direct register: 0000) with the address where the modification is to start. The selected color-palette RAM location is loaded a byte at a time by writing a sequence of three bytes (red, green, and blue) to the palette RAM data register (direct register: 0001). After the blue write cycle, the color-palette RAM address register increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data.

2.2.2 Reading From Color-Palette RAM

Reading from the color-palette RAM is performed by writing to the palette read address register (direct register: 0011) with the location to be read. Three successive MPU reads from the palette RAM data register produce red, green, and blue color data (6 or 8 bits depending on the 8/$\overline{6}$ mode) for the specified location. Following the blue read cycle, the address register is incremented. Since the color-palette RAM is dual ported, the RAM may be read during active display without disturbing the video.

2.3 Clock Selection

The TVP3026 VIP provides a maximum of four clock inputs (CLK0, CLK1, and CLK2/$\overline{\text{CLK2}}$) which can be selected as two TTL inputs and a differential ECL input or as four TTL inputs. The TTL inputs can be used for video rates up to 140 MHz while the differential ECL can be utilized up to the device limit. At reset, CLK0 is selected as the clock source for VGA mode 2. This power-up state supports VGA pass through operation without requiring software intervention.

An alternative clock source can be selected in the clock-selection register (index: 0x1A) during normal operation. This chosen clock input is then used as the dot clock (representing pixel rate to the monitor, see Table 2–5).

There are two ways of using CLK0 as a clock source. When CSR(2–0) = 111, CLK0 is selected as the clock source to generate the internal dot clock (see Table 2–6). In this mode, multiplex control register bit MCR6 must be set to 1 and only the VGA port can be used. This selects latching of VGA(7–0) and $\overline{\text{VGABL}}$ with CLK0. When CSR(2–0) = 000, CLK0 is also selected as the clock source to generate the internal dot clock. However, in this mode, MCR6 must be logic 0, which selects latching of VGA(7–0) and $\overline{\text{SYSBL}}$ with LCLK. In this mode, the pixel port or the VGA port can be used.

Additionally, two crystal oscillator terminals (XTAL1, XTAL2) are provided for the integrated pixel clock and memory clock frequency synthesis PLLs. These terminals are intended for use with a quartz crystal resonator, but a discrete oscillator can also be utilized and input on the XTAL2 terminal (XTAL1 terminal should be left floating in this case).

Selection of the pixel clock PLL as the pixel clock source is performed by programming the clock selection register. In general, when the pixel clock PLL is to be selected, it should be selected after the PLL has been programmed and allowed to achieve lock.

Table 2–5. Clock-Selection Register Bits CSR(6–4) (Index: 0x1A, Access: R/W, Default: 0x07)

CLOCK-SELECT REGISTER BITS			VCLK FREQUENCY
6	5	4	
0	0	0	Dot clock
0	0	1	Dot clock/2
0	1	0	Dot clock/4
0	1	1	Dot clock/8
1	0	0	Dot clock/16
1	0	1	Dot clock/32
1	1	0	Dot clock/64
1	1	1	Reset to 0

NOTE 2: Bit CSR7 enables the SCLK output when set to 1.

Table 2–6. Clock-Selection Register Bits CSR(3–0) (Index: 0x1A, Access: R/W, Default: 0x07)

CLOCK SELECT REGISTER BITS				FUNCTION
3	2	1	0	
0	0	0	0	Select CLK0 as clock source (for use with LCLK latching of VGA port). See subsection 2.6.2, *VGA Modes*.
0	0	0	1	Select CLK1 as clock source
0	0	1	0	Select CLK2 as TTL clock source
0	0	1	1	Select $\overline{\text{CLK2}}$ as TTL clock source
0	1	0	0	Select CLK2 and $\overline{\text{CLK2}}$ as ECL clock source
0	1	0	1	Select pixel clock PLL as clock source
0	1	1	0	Disable internal dot clock for reduced power consumption.
0	1	1	1	Select CLK0 as clock source (for use with CLK0 latching of VGA port). See subsection 2.6.2, *VGA Modes*.
1	X	X	X	Reserved

x = do not care

2.4 PLL Clock Generators

In addition to externally supplied clock sources, the TVP3026 has three on-chip, fully programmable, frequency-synthesis phase-locked loops (PLLs). The first PLL ,pixel clock, is intended for pixel clock generation for frequencies up to the device limit. The second PLL ,MCLK, is provided for general system clocking such as the system clock or memory clock, and the third PLL ,called the loop clock PLL, is useful for synchronizing pixel data and latch timing by compensating for system loop delay.

The clock generators use a modified M over ($N \times 2^P$) scheme to enable a wide range of precise frequencies. (Appendix A provides a listing of all frequencies that can be synthesized and the register values for each.) The advanced PLLs utilize an internal loop filter to provide maximum noise immunity and minimum jitter. Except for the reference crystal or oscillator, no external components or adjustments are necessary. Each PLL can be independently enabled or disabled for maximum system flexibility. Figure 2–1 illustrates the TVP3026 PLL clocking scheme. The PLLs are programmed through a group of four registers in the TVP3026 indirect register map. The registers are listed in Table 2–7.

Table 2–7. PLL Top Level Registers

INDEX	REGISTER
0x2C	PLL address register (PAR)
0x2D	Pixel clock PLL data register (PPD)
0x2E	MCLK PLL data register (MPD)
0x2F	Loop clock PLL data register (LPD)

The PLL address register (PAR) points to the M, N, P, and status registers of each PLL. This register allows read and write access and contains three 2-bit pointers, one for each PLL, according to the Table 2–8. Each pointer may be programmed independently.

Table 2–8. PLL Address Register (Index: 0x2C, Access: R/W, Default: Uninitialized)

PAR BITS	POINTER
1–0	Pixel clock PLL data register pointer
3–2	MCLK PLL data register pointer
5–4	Loop clock PLL data register pointer

Each PLL data register pointer directs its associated PLL to one of its four PLL registers according to Table 2–9.

Table 2–9. PLL Data Register Pointer Format

BIT 1	BIT 0	REGISTER
0	0	N-value register
0	1	M-value register
1	0	P-value register
1	1	Status register (read-only)

Once the PLL data register pointers are set, the selected register is accessed through the pixel clock PLL data register (index: 0x2D), MCLK PLL data register (index: 0x2E) or the loop clock PLL data register (index: 0x2F). The PLL data register pointer bits are independently autoincremented following a write cycle to the corresponding PLL data register. The current state of each pointer can be identified by reading the PLL address register (index: 0x2C). The PLL data register pointer bits do not autoincrement following a read cycle of the PLL data registers.

The most efficient way to program the pixel clock PLL is to first write zeros to PLL address register bits PAR(1,0) followed by three consecutive writes to the pixel clock PLL data register to program the N, M, and P-value registers. Following the third write, the pixel clock PLL pointer will point to the read-only status register. The status register can then be polled until the LOCK bit is set (the pointer does not autoincrement on reads). For test purposes, the pixel clock PLL can be output on the PCLKOUT terminal by setting the pixel clock PLL P-value register bit 6 to 1.

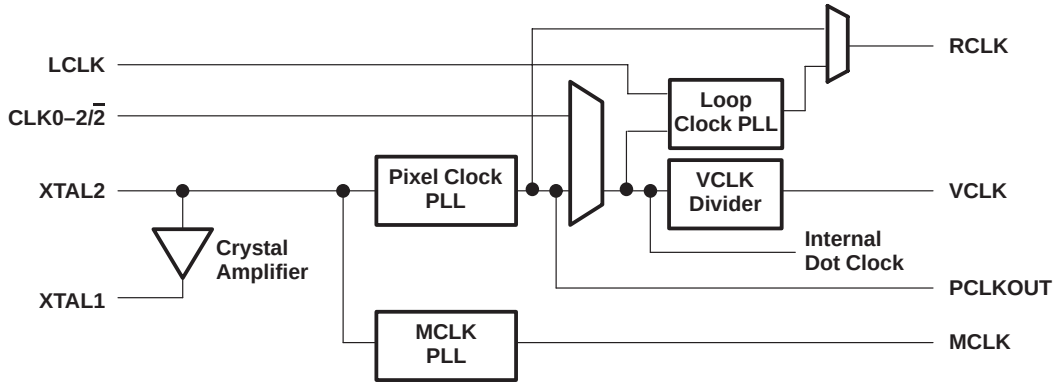


Figure 2–1. TVP3026 Clocking Scheme

2.4.1 Pixel Clock PLL

The pixel clock PLL may be used at frequencies up to the device limit. Appendix A provides optimal register values for all frequencies that can be synthesized using the common 14.31818 MHz reference. The following equations describe the voltage controlled oscillator frequency and the PLL output frequency for the pixel clock PLL as a function of the N, M, and P values and the reference frequency F_{REF}.

The frequency of the voltage controlled oscillator (VCO) is given by:

$$F_{VCO} = 8 \times F_{REF} \times \frac{65 - M}{65 - N} \quad (1)$$

Provided:

$$\text{Minimum VCO Frequency} \leq F_{VCO} \leq \text{Maximum VCO Frequency}$$

Then the PLL output frequency is :

$$F_{PLL} = \frac{F_{VCO}}{2^P} \quad (2)$$

The N-, M-, and P-value registers may be programmed to any value within the following limits:

$40 \leq N(5–0) \leq 62$

$1 \leq M(5–0) \leq 62$

$0 \leq P(1, 0) \leq 3$

The bit assignments of the N-, M-, and P-value and the status register for the pixel clock PLL are given in Table 2–10. The bits shown as set to 0 or 1 must be written with these fixed values. PCLKEN enables the pixel clock PLL output onto the PCLKOUT output terminal when set to 1. When PCLKEN is reset to 0, the PCLKOUT terminal is held at 0. PLLEN resets the PLL to 0 and enables the PLL to oscillate when set to 1. When PFORCE is set to 1, the pixel clock PLL uses its programmed N, M, and P registers and ignores PLLSEL(1,0). When LFORCE is set to 1, the loop clock PLL uses its programmed N, M, and P registers and ignores PLLSEL(1,0). The LOCK status bit indicates that the PLL has locked to the selected frequency when set to 1. The remaining status register bits are for test purposes.

Table 2–10. Pixel Clock PLL Registers

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
N value	1	1	N5	N4	N3	N2	N1	N0
M value	0	0	M5	M4	M3	M2	M1	M0
P value	PLLEN	PCLKEN	1	1	LFORCE	PFORCE	P1	P0
Status	X	LOCK	X	X	X	X	X	X

X = do not care

2.4.1.1 Pixel Clock PLL Frequency Selection

The pixel clock PLL frequency may be selected using the PLL select inputs PLLSEL(1,0) as shown in Table 2–11. The first two selections are fixed frequency settings for standard VGA operation. Use of a standard 14.31818 MHz crystal is assumed. When PLLSEL1 is set to 1, the frequency specified by the pixel clock PLL N-, M-, and P-value registers is selected. When PLLSEL1 is set to 1 at power up or during a software reset, the pixel clock PLL N-, M-, and P-value registers default to settings for 25.057 MHz, but with the PLL disabled. Therefore, the system must reset PLLSEL(1,0) to 0x when a software reset occurs or the pixel clock PLL and RCLK stops oscillating.

The frequency select inputs also apply to the loop clock PLL. When a fixed frequency is selected (PLLSEL(1,0) = 0x), the loop clock PLL passes the dot clock frequency to the RCLK multiplexer. Internal feedback is used, no external signal path from RCLK to LCLK is required. When PLLSEL1 is 1, the frequency specified by the loop clock PLL N-, M-, and P-value registers is selected.

For VGA Mode 1, the pixel clock PLL is normally selected as the dot clock source (CSR = 0x05) and the RCLK terminal passes the loop clock PLL output (MCK5 = 1). Then, when PLLSEL(1,0) changes between a programmed frequency and a fixed frequency, the loop clock PLL automatically changes with it. The loop clock PLL does not require reprogramming.

For VGA Mode 2, CLK0 should be selected as the dot clock source (CSR = 0x07) and the RCLK terminal should pass the pixel clock PLL output (MCK5 = 0). In this case, the loop clock PLL should be disabled (bit P7 = 0) since its output is not used.

Table 2–11. Pixel Clock PLL Frequency Selection

PLLSEL1	PLLSEL0	PIXEL CLOCK PLL FREQUENCY	LOOP CLOCK PLL FREQUENCY
0	0	25.057 MHz	Pass DOT CLOCK, internal feedback
0	1	28.636 MHz	Pass DOT CLOCK, internal feedback
1	X	Programmed by pixel clock PLL registers	Programmed by loop clock PLL registers

X = do not care

2.4.2 Memory Clock PLL

The memory clock (MCLK) PLL may be used at frequencies up to 100 MHz. Appendix A provides optimal register values for all frequencies that can be synthesized using the common 14.31818 MHz reference. The MCLK PLL maximum output frequency of 100 MHz may not be exceeded. The equations for the VCO frequency and for the PLL output frequency are the same as for the pixel clock PLL.

$$F_{VCO} = 8 \times F_{REF} \times \frac{65 - M}{65 - N} \quad (3)$$

Provided:

$$\text{Minimum VCO Frequency} \leq F_{VCO} \leq \text{Maximum VCO Frequency}$$

Then the PLL output frequency is :

$$F_{PLL} = \frac{F_{VCO}}{2^P} \quad (4)$$

The N-, M-, and P-value registers may be programmed to any value within the following limits:

$40 \leq N(5–0) \leq 62$

$1 \leq M(5–0) \leq 62$

$0 \leq P(1, 0) \leq 3$

The bit assignments of the N-, M-, and P-value and the status register for the MCLK PLL are given in Table 2–12. The bits shown as 0 or 1 must be written with these fixed values. PLLEN resets the PLL with 0 and enables the PLL to oscillate when set to 1. When set to 1, the LOCK status bit indicates that the PLL has locked to the selected frequency. The remaining status register bits are for test purposes. The MCLK PLL and loop clock PLL are further controlled by the MCLK/loop clock control register shown in Table 2–13.

Table 2–12. MCLK PLL Registers

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
N value	1	1	N5	N4	N3	N2	N1	N0
M value	0	0	M5	M4	M3	M2	M1	M0
P value	PLLEN	0	1	1	0	0	P1	P0
Status	X	LOCK	X	X	X	X	X	X

X = do not care

Table 2–13. MCLK/Loop Clock Control Register (Index: 0x39 hex, Access: R/W, Default: 0x18)

BIT NAME	VALUES	DESCRIPTION
MKC7	0	Reserved
MKC6, MKC5	00: Pixel clock PLL (default) 01: Loop clock PLL 10: Dot clock /N 11: Reserved	Selects signal to output on RCLK terminal. Pixel clock PLL is selected as default to support VGA mode 2. In VGA mode 2, the graphics accelerator receives RCLK and returns its VGA output clock to the CLK0 terminal along with synchronous VGA data. Select loop clock PLL for all modes using LCLK data latching. The dot clock /N option provides the output of the loop clock PLL N prescaler. This signal is a low pulse, one dot clock wide, with a repetition rate of F_{REF} / (65–N).
MKC4	0: Dot clock 1: MCLK PLL (default)	MKC4 selects the signal to output on MCLK terminal. MCLK PLL is selected as default. Select dot clock to ensure a stable output on MCLK while MCLK PLL frequency is reprogrammed. See subsection 2.4.2.1, *Changing the MCLK Frequency.* A change of this bit does not take effect until MKC3 bit transitions from 0 to 1. During this transistion, the MKC4 bit should not be changed.
MKC3	0: 1: (default)	Strobe for MCLK terminal output multiplexer control (MKC4). A 0 to 1 transition of this bit strobes in bit MKC4, causing bit MKC4 to take effect. While MKC3 is transitioning from 0 to 1, MKC4 should not be changed.
MKC2, MKC1, MKC0	000: Divide by 2 (default) 001: Divide by 4 010: Divide by 6 011: Divide by 8 100: Divide by 10 101: Divide by 12 110: Divide by 14 111: Divide by 16	Loop clock PLL post scalar Q divider. This additional frequency division is applied after the 2^P division of the loop clock PLL P-value register. For a binary value of Q in MKC2 – MKC0, the resulting frequency division is 2*(Q+1).

After the device resets, the MCLK PLL outputs a 50.11 MHz clock frequency and the pixel clock PLL output depends on the PLLSEL1 and PLLSEL0 inputs according to Table 2–11. These frequencies assume a standard 14.31818 MHz crystal reference. The actual output frequencies are proportional to the reference frequency used.

2.4.2.1 Changing the MCLK Frequency

The MCLK is normally used as the graphics controller system clock and memory clock. During reprogramming of the PLLs, a wide range of unpredictable frequencies are generated as the PLL transitions to the new programmed frequency. These transition effects can produce unwanted results in some systems. The TVP3026 provides a mechanism for smooth transitioning of the MCLK PLL. The following programming steps are recommended.

1. Disable the pixel clock PLL (PLLEN bit = 0). Program the pixel clock PLL N, M, and P registers (with PLLEN bit = 1) to the same frequency to which MCLK is to be changed. Poll the pixel clock PLL status until the LOCK bit is set to 1.
2. Select the pixel clock PLL as the dot clock source if it is not already selected.
3. Switch to output dot clock on the MCLK terminal by writing bits MKC4 and MKC3 to 0,0 followed by 0,1 in the MCLK/loop clock control register.
4. Disable the MCLK PLL (PLLEN bit = 0). program the MCLK PLL N, M, and P registers (with PLLEN bit = 1) for the new frequency. Poll the MCLK PLL status until the LOCK bit is set to 1.
5. Switch to output MCLK on the MCLK terminal by writing bits MKC4 MKC3 to 1,0 respectively, followed by 1,1 respectively in the MCLK/loop clock control register.

6. Disable the pixel clock PLL (PLLEN bit = 0). Program the pixel clock PLL N, M, and P registers (with PLLEN bit = 1) for the original operating pixel frequency. Poll the pixel clock PLL status until the LOCK bit is set to 1.

2.4.3 Loop Clock PLL

Many of the current high performance graphics accelerators with built in VGA support prefer to generate their own VRAM shift clock and pixel data latching clock (LCLK) as discussed in subsection 2.5.2, *Frame-Buffer Timing Without Using SCLK*. As stated before, the TVP3026 provides an RCLK timing reference output to be used by the graphics controller to generate these signals. A common industry problem exists, however, in that the delay through the loop (i.e., from RCLK through the controller to produce LCLK and pixel data) may be greater than the RCLK cycle time minus setup time. It then becomes very difficult to resynchronize the rising edges of the LCLK signal to the internal dot clock within the specified timing requirements. Variations in graphics accelerator propagation delays from device to device can cause severe production problems at the board level. The TVP3026 incorporates a unique loop clock PLL circuit to maintain a valid LCLK/dot clock phase relationship and ensure that proper LCLK and pixel data setup timing is met, regardless of the amount of system loop delay.

After device reset, the loop clock PLL provides the dot clock frequency to the RCLK output multiplexer. However, the RCLK output multiplexer will ignore the loop clock PLL output and instead pass the pixel clock PLL output to the RCLK terminal, which provides a reference clock to the VGA controller. In this configuration (VGA mode 2), the VGA controller returns VGA data and video controls along with a synchronous clock that becomes the TVP3026 dot clock source using CLK0. The PLLSEL(1,0) lines select either the 25.057 MHz or 28.636 MHz VGA frequencies.

Figure 2–2 illustrates the pixel data latching structure and the operation of the loop clock PLL. The selected clock source generates the dot clock which drives most of the digital logic of the TVP3026. The dot clock is used as a reference frequency by the loop clock PLL and is subdivided as specified by the N value register. The incoming LCLK is used as the other input of the PLL and is subdivided as specified by the M value register. The PLL generates RCLK with the proper frequency and phase shift to phase align the divided dot clock and divided LCLK. The pixel bus is latched on the rising edge of LCLK and then aligned with the internal dot clock to synchronize with internal logic.

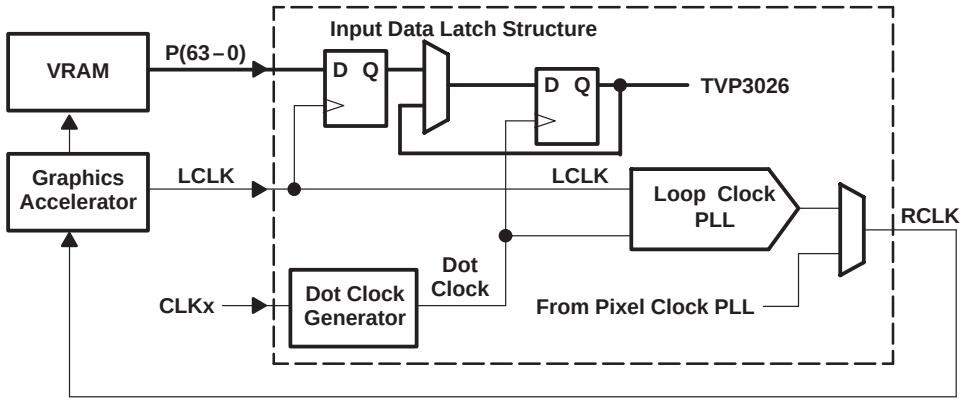


Figure 2–2. Loop Clock PLL Operation

The bit assignments of the N-, M-, and P-value and the status register for the loop clock PLL are shown in Table 2–14. The bits shown as 0 or set to 1 must be written with these fixed values. When cleared to 0, PLLEN disables the PLL and when set to 1, enables the PLL to oscillate. When reset to 1,the LOCK status bit indicates that the PLL has locked to the selected frequency. The remaining status register bits are for test purposes.

The N-, M-, and P-value registers may be programmed to any value within the following limits.

$1 \leq N(5–0) \leq 62$

$1 \leq M(5–0) \leq 62$

$0 \leq P(1, 0) \leq 3$

LESEN enables the LCLK edge synchronizer function and should be set to 1 whenever a packed-24 mode is used. In the packed-24 modes, only one LCLK rising edge per pixel group is aligned with the internal dot clock. For example, in 8:3 packed-24 mode, only one of the three LCLKs is aligned to the internal dot clock. The LCLK edge synchronizer function allows selection of which LCLK edge in the sequence of pixel bus words is aligned with the internal dot clock. For each packed-24 mode there is an optimum setting for the LCLK edge synchonizer delay LES1 and LES0. See Table 2–15 and subsection 2.6.6, *Packed-24 Mode*, for more details.

Table 2–14. Loop Clock PLL Registers

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
N value	1	1	N5	N4	N3	N2	N1	N0
M value	LES1	LES0	M5	M4	M3	M2	M1	M0
P value	PLLEN	1	1	1	LESEN	0	P1	P0
Status	X	LOCK	X	X	X	X	X	X

X = do not care

2.4.3.1 Programming for All Modes Except Packed-24

For all modes except packed-24, programming of the loop clock PLL registers depends on the system configuration, pixel rate, color depth and pixel bus width. In addition, the internal VCO must be within its operating range of 110 MHz to 220 MHz for the required RCLK output frequency. To determine the proper M, N, P, and Q register values one should know the following:

- Dot clock frequency (MHz) (F_D) – pixel rate
- Bits/pixel (B) – bits/pixel including overlay fields
- Pixel bus width (W) – total pixel bus width used for this mode
- External division factor (K) – external frequency division between RCLK output and LCLK input

The dot clock frequency can either be generated by the on-chip pixel clock PLL or by an external clock source. The following two parameters can be easily calculated from the above parameters.

- LCLK frequency (MHz) (F_L) – frequency at which the pixel bus is loaded by the TVP3026
- RCLK frequency (MHz) (F_R) – frequency at RCLK output terminal of TVP3026

The LCLK frequency is given by

$$F_L = F_D \times \frac{B}{W} \tag{5}$$

The RCLK frequency is F_L times the external divide factor. When no external divide factor, K = 1.

$$F_R = K \times F_L = K \times F_D \times \frac{B}{W} \tag{6}$$

The N and M values are set as follows:

$$N = 65 - 4 \times \frac{W}{B}$$

$$M = 61$$

The P and Q frequency dividers must be programmed so that the VCO is within its operating range. The VCO frequency is post-scaled by the P-divider followed by the Q-divider. The P-divider register (P) can take

on values of 0, 1, 2, or 3 which correspond to division factors of 1, 2, 4, or 8. The Q-divider register (Q) is stored in bits 2 – 0 of the MCLK/loop clock control register (index: 0x39) and can take on values of 0, 1, 2, . . ., 7 which correspond to division factors of 2, 4, 6, . . ., 16. The total post-scalar frequency division factor is:

$$Z = 2^{P+1} \times (Q + 1) = \frac{F_{VCO} \times (65 - N)}{4 \times F_D \times K} \quad (7)$$

Next, set F_{VCO} to the lower limit of 110 MHz and solve for Z:

$$Z = \frac{27.5 \times (65 - N)}{F_D \times K} \quad (8)$$

Finally, determine the P and Q values:

$$\text{IF } Z \leq 16 \text{ then } P = \text{TRUNC } (\log_2 Z),\ Q = 0$$

$$\text{IF } Z > 16 \text{ then } P = 3,\ Q = \text{INT } \left(\frac{Z - 16}{16}\right) + 1$$

Set bits 7,6 of the N-value register to 1,1 (default). Set LES1 and LES0 in the M-value register (bits 7,6) to 0,0 (default). Set bits 7–2 of the P-value register to 1111 00. This enables the PLL to oscillate and disables the LCLK edge synchronizer function, which is only used for packed-24 modes. To reset the PLL by resetting bit 7 of the P-value register to 0.

2.4.3.2 Programming for Packed-24 Modes

For packed-24 modes, the loop clock PLL is programmed according to Table 2–15. The LCLK edge synchronizer delay (M-value register bits 7 and 6) depends on whether the graphics accelerator is driving the VRAM shift clock (true color control register bit TCR5 is cleared to 0) or the TVP3026 is driving the VRAM shift clock (TCR5 = 1). See subsection 2.6.6, *Packed-24 Mode*, for a typical setup procedure for packed-24 modes. As shown in Table 2–15, a different setting is required for the M-value register in the 4:3 multiplex mode depending on the silicon revision. Software can determine the silicon revision by reading the silicon revision register at index 0x01 (a value ≤ 0x20 indicates revision A and ≥ 0x21 indicates revision B).

Table 2–15. Loop Clock PLL Settings for Packed-24 Mode

PACKED-24 MODE	BIT TCR5 (Index 0x18)	N-VALUE REGISTER	M-VALUE REGISTER TVP3026A	M-VALUE REGISTER TVP3026B
4:3	0	0xFD	0×BE	0x3E
8:3	0	0×F9	0×BE	0×BE
5:4	0	0×FC	0×3D	0×3D
5:2	0	0×FC	0×7F	0×7F
4:3	1	0×FD	0×3E	0×BE
8:3	1	0×F9	0×3E	0×3E
5:4	1	0×FC	0×BD	0×BD
5:2	1	0×FC	0×FF	0×FF

The latch-control register definition is listed in Table 2–16.

Table 2–16. Latch-Control Register (Index: 0x0F, Access: R/W, Default: 0x06)

BIT NAME	VALUES	DESCRIPTION
LCR7, LCR6	00	Reserved
LCR5–LCR0	0×06	All 1:1, 4:1, 8:1, and 16:1 multiplex modes.
	0×07	All 2:1 multiplex modes. 8:3 packed-24 or 4:3 packed-24 (revision A)
	0×08	4:3 packed-24 (revision B)
	0×20	5:2 packed-24
	0×1F	5:4 packed-24, ×1 horizontal zoom
	0×1E	5:4 packed-24, ×2 horizontal zoom
	0×1C	5:4 packed-24, ×4 horizontal zoom
	0×18	5:4 packed-24, ×8 horizontal zoom

The P and Q frequency dividers must be programmed so that the VCO is within its operating range of 110 MHz to 220 MHz. The VCO frequency is post scaled by the P-divider followed by the Q-divider. The P-divider register (P) can take on values of 0, 1, 2, or 3 which correspond to division factors of 1, 2, 4, or 8. The Q-divider register (Q) is stored in bits 2 – 0 of the MCLK/loop clock control register (index: 0x39) and can take on values of 0, 1, 2, . . ., 7 which correspond to division factors of 2, 4, 6, . . ., 16. The total post-scalar frequency division factor is:

$$Z = 2^{P+1} \times (Q + 1) = \frac{F_{VCO}}{F_D \times K} \times \frac{65 - N}{65 - M} \tag{9}$$

Next, set F_{VCO} to the lower limit of 110 MHz and solve for Z:

$$Z = \frac{110}{F_D \times K} \times \frac{65 - N}{65 - M} \tag{10}$$

Finally, determine the P and Q values:

$$\text{IF } Z \leq 16 \text{ then } P = \text{TRUNC}\left(\log_2 Z\right),\ Q = 0$$

$$\text{IF } Z > 16 \text{ then } P = 3,\ Q = \text{INT}\left(\frac{Z - 16}{16}\right) + 1$$

Set bits 7–2 of the P-value register to 1111 10. This enables the PLL to oscillate and enables the LCLK edge synchronizer function. To reset the PLL, clear bit 7 of the P-value register to 0.

2.4.3.3 Typical Device Connection

After reset, the TVP3026 defaults to VGA mode 2 (VGA pass through mode, see subsection 2.6.2, *VGA Modes*) as do other devices in the TVP302x family. The RCLK terminal outputs the pixel clock PLL frequency which is selected by PLLSEL1 and PLLSEL0. CLK0 is selected as the clock source and the VGA port is selected as well as $\overline{\text{VGABL}}$, VGAHS, and VGAVS and these are latched with CLK0. The MCLK PLL outputs the default 50.11 MHz clock frequency.

Figure 2–3 shows the typical device connection for a system with VRAM clocked by the graphics accelerator. After power up, the pixel clock PLL is output on RCLK and this clock drives the graphics accelerator's VGA controller and video timing logic. The accelerator's output clock is output synchronous to the VGA data and is input to the TVP3026 CLK0 input as the dot clock source.

Figure 2–4 shows the typical device connection for a system with VRAM clocked by the TVP3026. In this case, the RCLK is tied back to the LCLK and this same clock drives the graphics-accelerator VGA controller and video timing logic. If necessary, the RCLK and SCLK signals may be externally buffered within the timing constraints (RCLK to LCLK delay) of the TVP3026. The pixel clock PLL is output on RCLK after power up.

For high resolution modes in both configurations, the pixel data is received from VRAM and the loop clock PLL is used to adjust RCLK so that the received LCLK is aligned with the internal dot clock. The loop clock PLL must be selected for output on the RCLK terminal. The pixel clock PLL (or an external clock source) should be selected as the dot clock source.

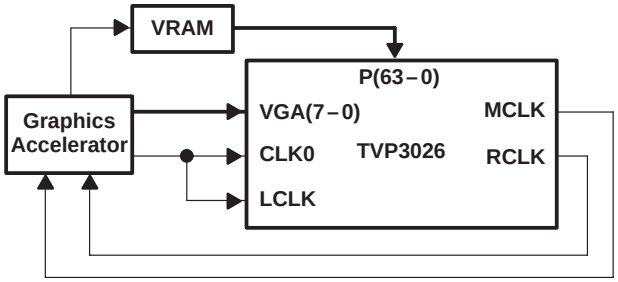


Figure 2–3. Typical Configuration – VRAM Clocked by Accelerator

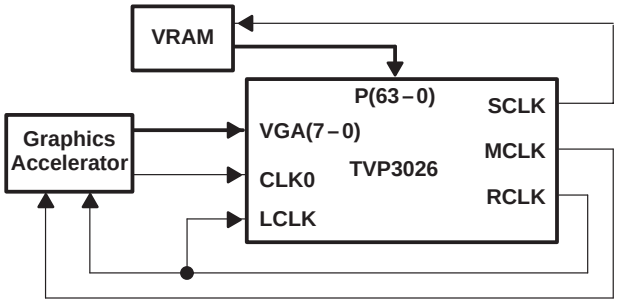


Figure 2–4. Typical Configuration – VRAM Clocked by TVP3026

2.5 Frame-Buffer Interface

The TVP3026 provides two output clock signals and one input clock signal for controlling the frame-buffer interface — SCLK, RCLK, and LCLK. The VCLK output is a division of the internal dot clock and has no guaranteed phase relationship with RCLK. Therefore, VCLK should not be used for frame buffer interface timing (pixel data and video controls). VCLK can drive general purpose external logic. Clocking of the frame buffer interface is discussed in subsection 2.5.1, *Frame-Buffer Clocking*. The 64-bit pixel bus allows many operational display modes as defined in Section 2.6, *Multiplexing Modes of Operation*, and Table 2–17. The pixel latching sequence is initiated by a rising edge on LCLK. For those multiplexed modes in which multiple pixels are latched on one LCLK rising edge, the pixel clock shifts the pixels out starting with the pixels that reside on the low numbered pixel port terminals. For example, in an 8-bit-per-pixel pseudo-color mode with an 8:1 multiplex ratio, the pixel display sequence is P(7–0), P(15–8), P(23–16), P(31–24), P(39–32), P(47–40), P(55–48), and P(63–56).

The TVP3026 frame-buffer interface also supports little- and big-endian data formats on the pixel bus. This can be controlled by general-control register (GCR) bit 3. See subsection 2.6.1, *Little-Endian and Big-Endian Data Format*, for details of operation.

2.5.1 Frame-Buffer Clocking

The TVP3026 provides SCLK and RCLK signals, allowing for flexibility in the frame buffer interface timing. For the pixel port (P63–P0), data is always latched on the rising edge of LCLK. If TCR5 in the true-color control register is set to 1, use of SCLK is assumed and internal pipeline delay is added to Sync and Blank to account for the delay in the generation of SCLK. When TCR5 bit clears to 0 (default), then this pipeline delay is not added, and SCLK should not be used.

2.5.2 Frame-Buffer Timing Without Using SCLK

For those systems where the color palette data latch clock (LCLK) and VRAM shift clock are generated by the graphics controller, the TVP3026 SCLK output is not utilized. In these systems, RCLK should be connected to the graphics controller to provide the timing reference for pixel data and video control signals. LCLK should be a delayed version of RCLK such that the pixel data and video control signals meet the setup and hold requirements relative to the rising edge of LCLK. LCLK may be a frequency-divided and delayed version of RCLK as long as linear phase changes in RCLK produce linear phase changes in LCLK (and the pixel data). Bit TCR5 in the true-color control register must be reset to 0 when SCLK is not being used, so that additional pipeline delay in the video controls is not inserted.

The first LCLK rising edge out of blank latches the first pixel group. The last LCLK rising edge during blanking latches the last pixel group. Figure 2–5 shows typical frame-buffer timing for this case. In Figure 2–5, the delay from RCLK to SYSBL and P63–P0 depends on the total system loop delay through the graphics accelerator and the VRAM. This delay may be as long as is required. It need not be less than the RCLK cycle time.

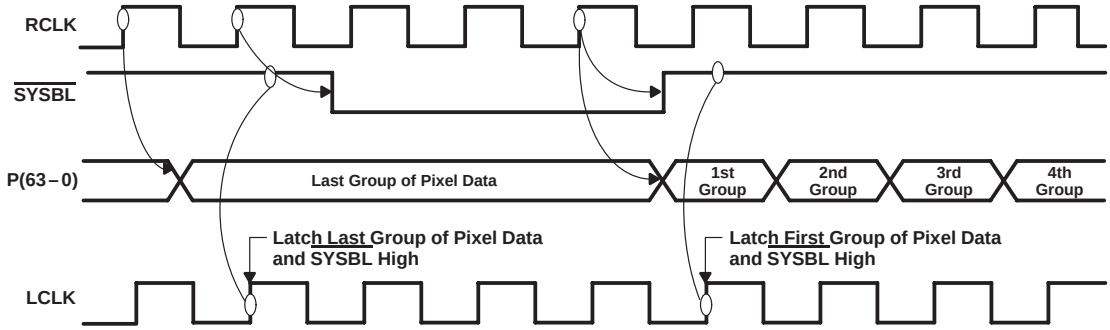


Figure 2–5. Frame-Buffer Timing Without Using SCLK

2.5.3 Frame-Buffer Timing Using SCLK

The SCLK signal which is generated in the TVP3026 may be directly connected to VRAM, providing the shift clock-to-clock data from VRAM into the TVP3026 pixel input port. The RCLK signal must be used as the timing reference to clock pixel data into this port. Therefore, when SCLK is used, RCLK is typically directly tied back to LCLK, or LCLK can be a delayed version (buffered) of RCLK within the timing requirements of the TVP3026.

Operation using the SCLK timing mode must limit the RCLK-to-LCLK loop delay to the specified maximum delay. This ensures that the relationship between the end of blanking (SYSBL active) and the first SCLK pulse is not disturbed. When SCLK is not used, the RCLK to SCLK delay may be as long as is needed by system logic. Figure 2–6 illustrates the frame-buffer timing using SCLK.

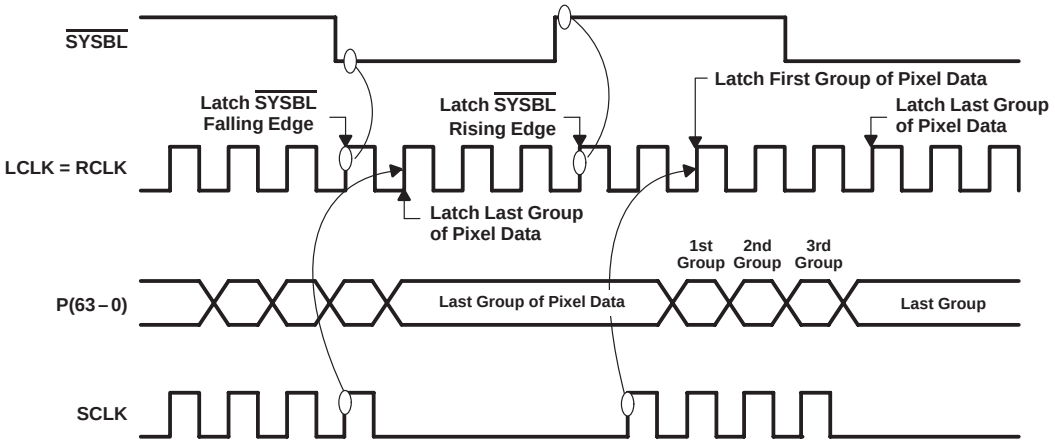


Figure 2–6. Frame-Buffer Timing Using SCLK

2.5.4 Split Shift-Register-Transfer Support

When SCLK is used, the TVP3026 supports the special clocking requirements of some VRAM devices. For example, some VRAM devices require the first SCLK pulse to occur during blanking ($\overline{\text{SYSBL}}$ active) between the split shift register transfer (SSRT) and the full shift register transfer VRAM operations. When SCLK mode is enabled (TCR5 = 1) and $\overline{\text{SYSBL}}$ is active, a high pulse on the SFLAG input is passed directly to the SCLK output. When the high pulse on SFLAG is detected at any time during blanking, the first SCLK pulse normally generated after coming out of blanking is suppressed. This is because the SSRT operation leaves the first pixel group of the new line on the pixel bus as opposed to the last pixel group of the previous line. Figure 2–7 shows the SCLK timing mode with the first SCLK pulse relocated. When this function is not used, the SFLAG terminal should be connected to GND.

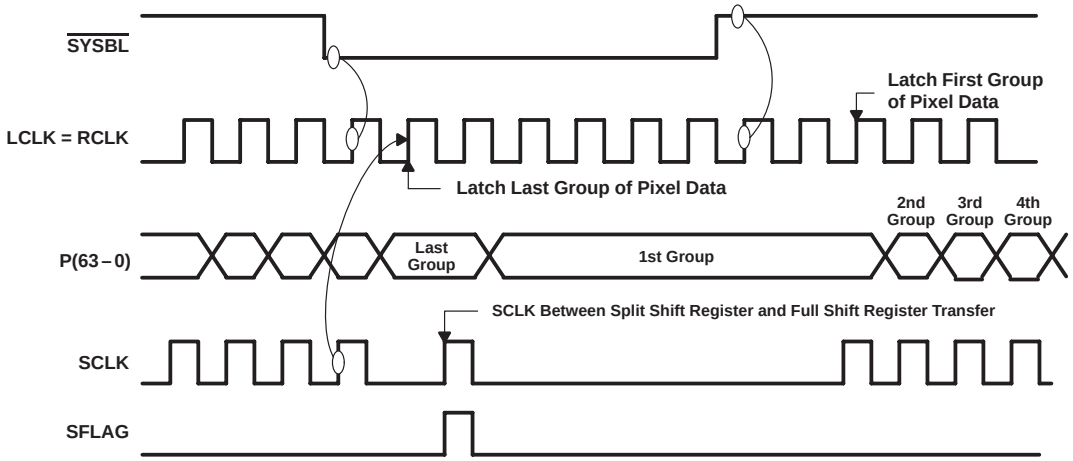


Figure 2–7. Frame-Buffer Timing Using SCLK (With First SCLK Pulse Relocated)

2.6 Multiplexing Modes of Operation

The TVP3026 offers a highly versatile multiplexing scheme as illustrated in Tables 2–17 through 2–21. The multiplexing modes allow the pixel bus (P63–P0) to be programmed to 4, 8, 16, 24, or 32 bits/pixel with pixel bus widths ranging from 8 to 64 bits. The use of on-chip multiplexing allows graphics systems to be designed that can support multiple pixel depths and resolutions with no hardware modification. The TVP3026 can also be configured for pseudo-color or true-color operation.

Multiplexing of the pixel bus is controlled by and programmed through the multiplex-control register and the true-color control register. Table 2–17 details the register settings for each mode of operation.

2.6.1 Little-Endian and Big-Endian Data Format

The TVP3026 pixel bus supports both little- and big-endian data formats for all pseudo-color, direct-color, and true-color modes of operation. The data-format select is controlled by GCR3 of the general-control register (see subsection 2.15.1, *General Control Registers*). When GCR3 is reset 0 (default), the format is set to little endian. When GCR3 is set to 1, the format is set to big endian.

In a big-endian design, the external VRAM data bus bits must be connected in reverse order to the TVP3026 pixel bus; i.e., D63 connected to P0, D0 connected to P63, etc. This configuration connects the pixels to the P63–P0 bus in the correct order with the first pixel to be displayed on the LSBs of the P63–P0 bus. However, the individual bits within each pixel are now connected in bit-reversed order. When big-endian format is selected, this bit-reversed order of each pixel is compensated for internally. The bit-reversal of pixels takes place in groups of 4, 8, 16, or 32 bits depending on the multiplexing mode selected. This scheme enables big-endian systems to operate in all of the available color-depths excluding the packed-24 modes.

2.6.2 VGA Modes

The VGA modes emulate the VGA modes of most personal computers. The TVP3026 has a single configuration called VGA mode 2 to support VGA modes. VGA mode 1, which was formerly specified to utilize the loop clock PLL with the VGA pixel port is not recommended.

VGA mode 2 supports most graphics accelerators with integrated VGA and also supports add-on graphics boards that receive the VGA pseudo-color data from a separate VGA controller using a feature connector. VGA mode 2 is active at power up and after reset and is fully functional without any software intervention. VGA data and video controls are received with a synchronous VGA clock.

The feature connector configuration is emulated by many graphics accelerators with integrated VGA. In this configuration, the pixel clock PLL is output on the RCLK terminal (bit MKC5 = 0) and sent to the accelerator's clock input. The clock output from the accelerator is connected to the CLK0 input of the TVP3026. The loop clock PLL is not used. The accelerator outputs the VGA video controls and VGA7–VGA0 data synchronous with CLK0 and, thereby, emulates the feature connector configuration. In VGA mode 2, the TVP3026 derives the dot clock from CLK0 and latches the VGA7–VGA0 data and VGA video controls using CLK0.

To program for VGA mode 2, bit MCR7 in the multiplex control register must be set to 1 to select VGA mode, and bit MCR6 must be reset to 0 to latch VGA7–VGA0 and the VGA video controls with CLK0. The clock selection register bits CSR3–CSR0 must be set as 0111 for CLK0 data latching.

2.6.3 Pseudo-Color Mode

In pseudo-color mode (sometimes called color indexing), the pixel-bus inputs address the palette RAM. The pallete RAM functions as a color look-up table. The data in each RAM location is comprised of 24 bits, 8 bits for each of the red, green, and blue color DACs. The pseudo-color mode is further grouped into 3 submodes, depending on the data bits per pixel. In each submode, a pixel bus width of 8, 16, 32 or 64 bits may be used. Data should always be presented on the least significant bits of the pixel bus. For example, when a 16-bit pixel bus width is used, the pixel data must be presented on P15–P0. See Tables 2–17 and 2–18 for more details.

Submode 1 uses four bit planes to address the color palette. The four bits are fed into the low-order address bits of the palette with the four high-order address bits being defined by the palette-page register. This mode provides 16 pages of 16 colors and can be used at multiplex ratios of 2:1 to 16:1.

Submode 2 uses four bit planes to address the color palette. Each byte of the pixel bus contains two pixels which are in reverse order (nibble swapped). The first pixel is latched in on the upper four bits and the second pixel is latched in on the lower four bits of each byte. The 4-bit pixels are fed into the low-order address bits of the palette with the four high-order address bits being defined by the palette-page register. This mode provides 16 pages of 16 colors and can be used at multiplex ratios from 2:1 to 16:1.

Submode 3 uses eight bit planes to address the color palette. Since all eight bits of palette address are specified from the pixel port, the palette-page register is not used. This mode provides 256 colors and can be used at mulitplex ratios from 1:1 to 8:1.

NOTE

The port select and color-key switching functions must be disabled and set for palette graphics when in the pseudo-color mode. This is the default condition at reset. See Section 2.8, *Port Select and Color-Key Switching*.

2.6.4 Direct-Color Mode

In direct-color mode, 24, 16, 15, or 12 bits of data can be transferred directly to the RGB DACs but with the same amount of pipeline delay as the overlay data and the control signals. Depending on which direct-color mode is selected, overlay is provided by utilizing the remaining bits of the pixel bus to address the palette RAM. This results in a 24-bit RAM output that is then used as overlay information to the DACs. The overlay capability is designed to work with the port select and color-key switching functions to provide overlay in specific windows or on a pixel-by-pixel basis on the direct-color display as discussed in Section 2.8, *Port Select and Color-Key Switching*. See Table 2–17 for more details on selecting the direct-color modes. See NOTES in the following section.

Submodes 1 and 2 are packed-24 modes. See subsection 2.6.6, *Packed-24 Modes*, for a description of the packed-24 modes.

Submodes 3 and 4 are the 32-bit direct-color modes that use eight bits to represent each color and eight bits for overlay. The 64-bit-wide pixel bus of the TVP3026 allows multiplex ratios of 1:1 or 2:1. Submode 3 is organized as overlay, red, green, and blue, while submode 4 is organized as blue, green, red, and overlay.

Submode 5 is the XGA-compatible 5–6–5 (16-bit-color) mode supporting five bits of red, six bits of green, and five bits of blue data. The TVP3026 supports multiplex ratios for this mode of 1:1, 2:1, and 4:1. Overlay is not available in this mode.

Submode 6 is the TARGA-compatible 1–5–5–5 mode that uses 15 bits for color and 1 bit for overlay. It allows 5 bits for each of red, green, and blue data and one bit for overlay. The TVP3026 supports 1:1, 2:1, and 4:1 multiplex ratios in this mode.

Submode 7 is the 6–6–4 configuration. It provides six bits of red, six bits of green, and four bits of blue. The TVP3026 supports 1:1, 2:1, and 4:1 multiplexing in this mode. Overlay is not available in this mode.

Submode 8 is the 4–4–4–4 configuration. It provides 12 bits of direct color and 4 bits of overlay. It allows four bits for each of red, green, and blue data. The TVP3026 supports 1:1, 2:1, and 4:1 multiplexing ratios in this mode.

2.6.5 True-Color Mode

In true-color mode, the palette RAM is partitioned into three independent 256-word x 8-bit memory blocks that can be individually addressed by each color field of the true-color data. The independent memory blocks provide data for a single DAC output. With this architecture, gamma correction for each color is possible. Since the palette is used in true-color mode, there is no memory space to be used for the overlay function. All of the true-color submodes are the same as direct color except that overlay is not available. See Table 2–17 for more details on mode selection, and see NOTES below.

NOTES

Since less than 8 bits are defined for each color in the various 12- or 16-bit direct- or true-color modes, the data bits for the individual colors are internally shifted to the MSB locations and the remaining LSB locations for each color are set to 0 before 8-bit data is sent to the DACs.

Since the overlay information goes through the pseudo-color data path, it is subject to read masking and the palette-page register. This is especially important for those direct-color modes that have less than eight bits of overlay information. The overlay information in these modes justifies to the LSB positions, and the remaining MSB positions are filled with the corresponding palette-page data before addressing the palette RAM.

In order to display true color (gamma corrected through the palette), the port select function or the color-key switching function must be set for palette graphics. For direct color, both functions must be set for direct color.

When in the 24-bit direct-color or true-color modes, the data input works only in the 8-bit mode. In other words, when only six bits are used, the two LSB inputs for each color need to be tied to GND. However, the palette, which is used by the overlay input, is still governed by the 8/$\overline{6}$ function, and the output multiplexer selects 8 bits or 6 bits of data accordingly. The 8/$\overline{6}$ function is also valid in the other 16-bit modes.

The default condition after reset is for the port select function to be disabled and selecting palette graphics (MSC4 = MSC5 = 0) The default condition for the color key function is to be disabled and selecting direct-color graphics (CKC4 = CKC3 = CKC2 = CKC1 = CKC0 = 0). The overall effect is to default to palette graphics since the two are combined by a logical OR function. Also since MCR7 = 1 at reset, the VGA port is selected.

2.6.6 Packed-24 Mode

The packed-24 mode provides for more efficient use of the frame buffer. For example, a 1280 x 1024 x 24 bpp display may be implemented using 4 Mbytes of VRAM. Without packed-24, this can require 6 or 8 Mbytes of VRAM. Packed-24 modes can be used with direct-color (color palette bypass) or with true-color (gamma correction). The color depth is 24 bit/pixel and data may be arranged as R-G-B or B-G-R. Overlay fields are not available. Either a 64-bit pixel bus or a 32-bit pixel bus may be used. The 64-bit pixel bus supports 8:3 packed-24 (8 pixels per 3 LCLKs) and 5:2 packed-24 (5 pixels per 2 LCLKs). The 32-bit pixel bus supports 4:3 packed-24 (4 pixels per 3 LCLKs) and 5:4 packed-24 (5 pixels per 4 LCLKs). See Tables 2–19 and 2–20 for data formats.

The loop clock PLL must be set up to generate RCLK at the proper frequency which can be 3/8, 2/5, 3/4, or 4/5 of the dot clock frequency for the multiplexing ratios given above. Since the RCLK is PLL-synthesized, a 50% duty cycle RCLK is generated. As compared to other packed-pixel palette DACs, which generate the RCLK waveform using a digital state machine, the TVP3026 provides a longer RCLK period for a given dot clock frequency. This means a higher screen refresh rate is possible using VRAM of the same speed grade. For example, for the 8:3 packed-24 mode, the RCLK PLL must be set to output a clock that is 3/8 the frequency of the pixel clock. For a 1280 x 1024 display at 135 MHz pixel rate, a 50.6 MHz VRAM serial clock rate can be used. See subsection 2.4.3, *Loop Clock PLL*, for a description of the loop clock PLL.

Packed-24 operation using the SCLK timing mode must limit the RCLK-to-LCLK loop delay to the specified maximum delay. The following constraints apply to packed-24 mode:

- The number of LCLKs (pixel bus loads) during the active portion of the horizontal line must be a multiple of the number of LCLKs for each pixel group, i.e., a multiple of 3 for 8:3 packed-24 mode.
- The number of LCLKs during the total horizontal line (active + blanked) must be a multiple of the number of LCLKs for each pixel group.

- The first active pixel bus load (LCLK rising edge) of the horizontal line must load the first word of the M-word sequence comprising the pixel group. For designs not using SCLK (bit TCR5 = 0), the first active pixel bus load coincides with the first time SYSBL is sampled high. For designs using SCLK (bit TCR5 = 1), the first active pixel bus load occurs two LCLKs after the first time SYSBL is sampled high. See Figures 2–5 and 2–6.

Synchronization of the packed-24 operation is performed by the loop clock PLL. Consider an N:M packed-24 mode which packs N pixels into M pixel bus words. Internally, the TVP3026 must run through a sequence of N dot clocks for each pixel group. The loop clock PLL supplies a clock (RCLK) which is M/N times the dot clock frequency. The graphics accelerator uses RCLK to generate SYSBL. Initially, SYSBL could change on any of the M LCLKs of the sequence. Once SYSBL is sampled, the TVP3026 declares the proper LCLK as the first in the M-word sequence. However, the relationship between LCLK and the internal dot clock has not been established. Only one LCLK rising edge in the M-word pixel group is aligned with the internal dot clock, but which one of the M LCLKs is aligned has not been specified. This selection is important for operation of the unpacking logic and is programmable using the LCLK edge synchronizer delay. The LCLK edge synchronizer function allows selection of which LCLK edge of the pixel group is aligned with the internal dot clock. For each packed-24 mode, there is an optimum setting for LES1 and LES0 (see Tables 2–14 and 2–15).

The following steps outline a typical setup procedure for packed-24 mode:

1. Program the pixel clock PLL for the desired dot clock frequency and poll status until locked.
2. Select pixel clock PLL as clock source in clock selection register.
3. Program true-color control register and multiplex control register as given in Table 2–17.
4. Download palette RAM when gamma correction is being used (true-color mode).
5. Program latch control register as given in Table 2–27.
6. Set port select and color-key switching functions appropriately. For true-color mode, select the palette RAM. This is the power-up default. For direct-color mode, select palette bypass. From defaults, this can be done by setting bit MSC5 = 1 in the miscellaneous control register.
7. Select loop clock PLL for output on RCLK terminal by setting MCLK/loop clock control register bit MKC5 to 1.
8. Program the loop clock PLL as described in subsection 2.4.3.2, *Programming for Packed-24 Modes*, and poll status until locked.

2.6.7 Multiplex-Control Registers

The pixel port multiplexer is controlled by two 8-bit registers in the indirect register map (see Table 2–2). The various multiplexing modes can be selected according to Table 2–17.

NOTES

For all modes utilizing VGA7–VGA0, MCR6 should be set to 0, When MCR6 is reset to 0, $\overline{\text{VGABL}}$, $\overline{\text{VGAVS}}$, $\overline{\text{VGAHS}}$ are used and these video controls and VGA7–VGA0 are latched by CLK0. This is referred to as VGA mode 2. VGA mode 2 supports most graphics accelerators with integrated VGA and also supports add-on graphics boards that receive the VGA pseudo-color data from a separate VGA controller using a feature connector. VGA mode 2 is active at power up and after reset, and is fully functional without any software intervention. VGA data and video controls are received with a synchronous VGA clock.

For all modes, true-color control register bit TCR5 selects one of two timing modes for the blanking pipelining and pixel bus timing. See Figures 2–5 and 2–6.

When bit TCR5 is set to 0 (default) it is assumed that the VRAM shift clock is sourced by the graphics accelerator, and that SCLK from the TVP3026 is not being used. In this case, the first sample of blanking ($\overline{\text{SYSBL}}$ or $\overline{\text{VGABL}}$) inactive and the first pixel group latched into P63–P0 are assumed to coincide on the same rising edge of LCLK.

When bit TCR5 is set to 1, it is assumed that SCLK is used as the VRAM shift clock. In this case, the TVP3026 must first sample blanking in order to start toggling SCLK and then latch the first pixel group into P63 – P0. Therefore, the TVP3026 assumes there will be a 2-LCLK delay between the first sample of blanking inactive and the latching of the first pixel group by LCLK. In this case, the TVP3026 inserts additional pipeline delays to align the internal blanking signal with the pixel data at the DACs.

It is recommended that all unused input terminals be connected to ground to conserve power.

Table 2–17. Multiplex Mode and Bus-Width Selection

MODE	SUB-MODE	TRUE-COLOR-CONTROL REGISTER (INDEX 0x18)	MULTIPLEX-CONTROL REGISTER (INDEX 0x19)	DATA BITS PER PIXEL (see Note 3)	PIXEL BUS WIDTH	MULTI-PLEX RATIO (see Note 4)	OVERLAY BITS PER PIXEL	TABLE REFERENCE (see Note 5)
VGA		0x80	0x98	8	8	1	NA	v1
Pseudo-Color	1 4-Bit, Normal	0x80	0x41	4	8	2	NA	s1
		0x80	0x42	4	16	4	NA	s2
		0x80	0x43	4	32	8	NA	s3
		0x80	0x44	4	64	16	NA	s4
	2 4-Bit, Nibble Swapped	0x80	0x61	4	8	2	NA	s5
		0x80	0x62	4	16	4	NA	s6
		0x80	0x63	4	32	8	NA	s7
		0x80	0x64	4	64	16	NA	s8
	3 8-Bit	0x80	0x49	8	8	1	NA	s9
		0x80	0x4A	8	16	2	NA	s10
		0x80	0x4B	8	32	4	NA	s11
		0x80	0x4C	8	64	8	NA	s12
Direct-Color	1 Packed-24 R-G-B 8–8–8	0x16	0x5B	24	32	4:3	NA	d1
		0x16	0x5C	24	64	8:3	NA	d2
		0x1E	0x5B	24	32	5:4	NA	d3
		0x1E	0x5C	24	64	5:2	NA	d4
	2 Packed-24 B-G-R 8–8–8	0x17	0x5B	24	32	4:3	NA	d5
		0x17	0x5C	24	64	8:3	NA	d6
		0x1F	0x5B	24	32	5:4	NA	d7
		0x1F	0x5C	24	64	5:2	NA	d8
	3 32-Bit O-R-G-B	0x06	0x5B	24	32	1	8	d9
		0x06	0x5C	24	64	2	8	d10
	4 32-bit B-G-R-O	0x07	0x5B	24	32	1	8	d11
		0x07	0x5C	24	64	2	8	d12

NOTES: 3. Data bits per pixel is the number of bits of pixel information used as color data for each displayed pixel, often referred to as the number of bit planes.

4. Multiplex ratio indicates the number of pixels per bus load or the number of pixels associated with each LCLK (load clock) pulse. For example, with a 64-bit pixel bus width and 8 bit planes, each bus load is comprised of 8 pixels. The RCLK frequency must be chosen as a function of the multiplex mode selected. The RCLK frequency is not automatically set by mode selection; it must be set by programming the loop clock PLL registers.

5. This column is a reference to Tables 2–18 through 2–21, where the actual manipulation of pixel information and pixel latching sequences are illustrated for each of the multiplexing modes. For the pseudo-color pixel latching sequence (V1 and S1 through S12) refer to Table 2–18. For the packed-24 mode pixel latching sequence associated with the direct-color and true-color modes, refer to Table 2–19. For the direct-color mode pixel latching sequence, refer to Table 2–20 for little-endian format and to Table 2–21 for big-endian format.

Table 2–17. Multiplex Mode and Bus-Width Selection (Continued)

MODE	SUB-MODE	TRUE-COLOR-CONTROL REGISTER (INDEX 0x18)	MULTIPLEX-CONTROL REGISTER (INDEX 0x19)	DATA BITS PER PIXEL (see Note 3)	PIXEL BUS WIDTH	MULTI-PLEX RATIO (see Note 4)	OVERLAY BITS PER PIXEL	TABLE REFERENCE (see Note 5)
Direct-Color	5 16-bit XGA R-G-B 5–6–5	0x05	0x52	16	16	1	NA	d13
		0x05	0x53	16	32	2	NA	d14
		0x05	0x54	16	64	4	NA	d15
	6 16-bit TARGA O-R-G-B 1–5–5–5	0x04	0x52	15	16	1	1	d16
		0x04	0x53	15	32	2	1	d17
		0x04	0x54	15	64	4	1	d18
	7 16-bit R-G-B 6–6–4	0x03	0x52	16	16	1	NA	d19
		0x03	0x53	16	32	2	NA	d20
		0x03	0x54	16	64	4	NA	d21
	8 16-bit R-G-B-O 4–4–4–4	0x01	0x52	12	16	1	4	d22
		0x01	0x53	12	32	2	4	d23
		0x01	0x54	12	64	4	4	d24
True-Color	1 Packed-24 R-G-B 8–8–8	0x56	0x5B	24	32	4:3	NA	d1
		0x56	0x5C	24	64	8:3	NA	d2
		0x5E	0x5B	24	32	5:4	NA	d3
		0x5E	0x5C	24	64	5:2	NA	d4
	2 Packed-24 B-G-R 8–8–8	0x57	0x5B	24	32	4:3	NA	d5
		0x57	0x5C	24	64	8:3	NA	d6
		0x5F	0x5B	24	32	5:4	NA	d7
		0x5F	0x5C	24	64	5:2	NA	d8
	3 32-Bit X-R-G-B	0x46	0x5B	24	32	1	NA	d9
		0x46	0x5C	24	64	2	NA	d10
	4 32-bit B-G-R-X	0x47	0x5B	24	32	1	NA	d11
		0x47	0x5C	24	64	2	NA	d12

NOTES: 3. Data bits per pixel is the number of bits of pixel information used as color data for each displayed pixel, often referred to as the number of bit planes.

4. Multiplex ratio indicates the number of pixels per bus load or the number of pixels associated with each LCLK (load clock) pulse. For example, with a 64-bit pixel bus width and 8 bit planes, each bus load is comprised of 8 pixels. The RCLK frequency must be chosen as a function of the multiplex mode selected. The RCLK frequency is not automatically set by mode selection; it must be set by programming the loop clock PLL registers.

5. This column is a reference to Tables 2–18 through 2–21, where the actual manipulation of pixel information and pixel latching sequences are illustrated for each of the multiplexing modes. For the pseudo-color pixel latching sequence (V1 and S1 through S12) refer to Table 2–18. For the packed-24 mode pixel latching sequence associated with the direct-color and true-color modes, refer to Table 2–19. For the direct-color mode pixel latching sequence, refer to Table 2–20 for little-endian format and to Table 2–21 for big-endian format.

Table 2–17. Multiplex Mode and Bus-Width Selection (Continued)

MODE	SUB-MODE	TRUE-COLOR-CONTROL REGISTER (INDEX 0x18)	MULTIPLEX-CONTROL REGISTER (INDEX 0x19)	DATA BITS PER PIXEL (see Note 3)	PIXEL BUS WIDTH	MULTI-PLEX RATIO (see Note 4)	OVERLAY BITS PER PIXEL	TABLE REFERENCE (see Note 5)
True-Color	5 16-bit XGA R-G-B 5–6–5	0x45	0x52	16	16	1	NA	d13
		0x45	0x53	16	32	2	NA	d14
		0x45	0x54	16	64	4	NA	d15
	6 16-bit TARGA X-R-G-B 1–5–5–5	0x44	0x52	15	16	1	NA	d16
		0x44	0x53	15	32	2	NA	d17
		0x44	0x54	15	64	4	NA	d18
	7 16-bit R-G-B 6–6–4	0x43	0x52	16	16	1	NA	d19
		0x43	0x53	16	32	2	NA	d20
		0x43	0x54	16	64	4	NA	d21
	8 16-bit R-G-B-X 4–4–4–4	0x41	0x52	12	16	1	NA	d22
		0x41	0x53	12	32	2	NA	d23
		0x41	0x54	12	64	4	NA	d24

NOTES: 3. Data bits per pixel is the number of bits of pixel information used as color data for each displayed pixel, often referred to as the number of bit planes

4. Multiplex ratio indicates the number of pixels per bus load, or the number of pixels associated with each LCLK (load clock) pulse. For example, with a 64-bit pixel bus width and 8 bit planes, each bus load is comprised of 8 pixels. The RCLK frequency must be chosen as a function of the multiplex mode selected. The RCLK frequency is not automatically set by mode selection; it must be set by programming the loop clock PLL registers.

5. This column is a reference to Tables 2–18 through 2–21, where the actual manipulation of pixel information and pixel latching sequences are illustrated for each of the multiplexing modes. For the pseudo-color pixel latching sequence (V1 and S1 through S12) refer to Table 2–18. For the packed-24 mode pixel latching sequence associated with the direct-color and true-color modes, refer to Table 2–19. For the direct-color mode pixel latching sequence, refer to Table 2–20 for little-endian format and to Table 2–21 for big-endian format.

Table 2–18. Pseudo-Color Mode Pixel-Latching Sequence (see Note 6)

v1	s1	s2	s3	s4	s5	s6
VGA7–VGA0	P3–P0 P7–P4	P3–P0 P7–P4 P11–P8 P15–P12	P3–P0 P7–P4 P11–P8 • • P31–P28	P3–P0 P7–P4 P11–P8 • • P63–P60	P7–P4 P3–P0	P7–P4 P3–P0 P15–P12 P11–P8

s7	s8	s9	s10	s11	s12
P7–P4 P3–P0 P15–P12 P11–P8 • P31–P28 P27–P24	P7–P4 P3–P0 P15–P12 P11–P8 • P63–P60 P59–P56	P7–P0	P7–P0 P15–P8	P7–P0 P15–P8 P23–P16 P31–P24	P7–P0 P15–P8 P23–P16 • • P55–P48 P63–P56

NOTE 6: The latching sequence is initiated by a rising edge on LCLK. For modes in which multiple pixels are latched, the LCLK rising edge latches all the pixels and the pixel clock shifts them out starting with the lowest-numbered pixel. For example, in pseudo-color submode 1 with a 16-bit pixel bus width, the rising edge of LCLK latches four pixels and the pixel clock shifts them out in the order P(3–0), P(7–4), P(11–8), and P(15–12). Note that each line in each entry above represents one pixel.

Table 2–19. Packed-24 Formats

d1								
LCLK					**P31–P24**	**P23–P16**	**P15–P8**	**P7–P0**
First					B1(7–0)	R0(7–0)	G0(7–0)	B0(7–0)
Second					G2(7–0)	B2(7–0)	R1(7–0)	G1(7–0)
Third					R3(7–0)	G3(7–0)	B3(7–0)	R2(7–0)
d2								
LCLK	**P63–P56**	**P55–P48**	**P47–P40**	**P39–P32**	**P31–P24**	**P23–P16**	**P15–P8**	**P7–P0**
First	G2(7–0)	B2(7–0)	R1(7–0)	G1(7–0)	B1(7–0)	R0(7–0)	G0(7–0)	B0(7–0)
Second	B5(7–0)	R4(7–0)	G4(7–0)	B4(7–0)	R3(7–0)	G3(7–0)	B3(7–0)	R2(7–0)
Third	R7(7–0)	G7(7–0)	B7(7–0)	R6(7–0)	G6(7–0)	B6(7–0)	R5(7–0)	G5(7–0)
d3								
LCLK					**P31–P24**	**P23–P16**	**P15–P8**	**P7–P0**
First					B1(7–0)	R0(7–0)	G0(7–0)	B0(7–0)
Second					G2(7–0)	B2(7–0)	R1(7–0)	G1(7–0)
Third					R3(7–0)	G3(7–0)	B3(7–0)	R2(7–0)
Fourth						R4(7–0)	G4(7–0)	B4(7–0)
d4								
LCLK	**P63–P56**	**P55–P48**	**P47–P40**	**P39–P32**	**P31–P24**	**P23–P16**	**P15–P8**	**P7–P0**
First	G2(7–0)	B2(7–0)	R1(7–0)	G1(7–0)	B1(7–0)	R0(7–0)	G0(7–0)	B0(7–0)
Second		R4(7–0)	G4(7–0)	B4(7–0)	R3(7–0)	G3(7–0)	B3(7–0)	R2(7–0)
d5								
LCLK					**P31–P24**	**P23–P16**	**P15–P8**	**P7–P0**
First					R1(7–0)	B0(7–0)	G0(7–0)	R0(7–0)
Second					G2(7–0)	R2(7–0)	B1(7–0)	G1(7–0)
Third					B3(7–0)	G3(7–0)	R3(7–0)	B2(7–0)
d6								
LCLK	**P63–P56**	**P55–P48**	**P47–P40**	**P39–P32**	**P31–P24**	**P23–P16**	**P15–P8**	**P7–P0**
First	G2(7–0)	R2(7–0)	B1(7–0)	G1(7–0)	R1(7–0)	B0(7–0)	G0(7–0)	R0(7–0)
Second	R5(7–0)	B4(7–0)	G4(7–0)	R4(7–0)	B3(7–0)	G3(7–0)	R3(7–0)	B2(7–0)
Third	B7(7–0)	G7(7–0)	R7(7–0)	B6(7–0)	G6(7–0)	R6(7–0)	B5(7–0)	G5(7–0)
d7								
LCLK					**P31–P24**	**P23–P16**	**P15–P8**	**P7–P0**
First					R1(7–0)	B0(7–0)	G0(7–0)	R0(7–0)
Second					G2(7–0)	R2(7–0)	B1(7–0)	G1(7–0)
Third					B3(7–0)	G3(7–0)	R3(7–0)	B2(7–0)
Fourth						B4(7–0)	G4(7–0)	R4(7–0)
d8								
LCLK	**P63–P56**	**P55–P48**	**P47–P40**	**P39–P32**	**P31–P24**	**P23–P16**	**P15–P8**	**P7–P0**
First	G2(7–0)	R2(7–0)	B1(7–0)	G1(7–0)	R1(7–0)	B0(7–0)	G0(7–0)	R0(7–0)
Second		B4(7–0)	G4(7–0)	R4(7–0)	B3(7–0)	G3(7–0)	R3(7–0)	B2(7–0)

Table 2–20. Direct-Color Mode Pixel-Latching Sequence (Little-Endian) (see Note 7)

d9	d10
P31–P24(O), P23–P16(R), P15–P8(G), P7–P0(B) MSB LSB	P31–P24(O), P23–P16(R), P15–P8(G), P7–P0(B) P63–P56(O), P55–P48(R), P47–P40(G), P39–P32(B) MSB LSB
d11	**d12**
P31–P24(B), P23–P16(G), P15–P8(R), P7–P0(O) MSB LSB	P31–P24(B), P23–P16(G), P15–P8(R), P7–P0(O) P63–P56(B), P55–P48(G), P47–P40(R), P39–P32(O) MSB LSB
d13	**d14**
P15–P11(R), P10–P5(G), P4–P0(B) MSB LSB	P15–P11(R), P10–P5(G), P4–P0(B) P31–P27(R), P26–P21(G), P20–P16(B) MSB LSB
d15	**d16**
P15–P11(R), P10–P5(G), P4–P0(B) P31–P27(R), P26–P21(G), P20–P16(B) P47–P43(R), P42–P37(G), P36–P32(B) P63–P59(R), P58–P53(G), P52–P48(B) MSB LSB	P15(O), P14–P10(R), P9–P5(G), P4–P0(B) MSB LSB
d17	**d18**
P15(O), P14–P10(R), P9–P5(G), P4–P0(B) P31(O), P30–P26(R), P25–P21(G), P20–P16(B) MSB LSB	P15(O), P14–P10(R), P9–P5(G), P4–P0(B) P31(O), P30–P26(R), P25–P21(G), P20–P16(B) P47(O), P46–P42(R), P41–P37(G), P36–P32(B) P63(O), P62–P58(R), P57–P53(G), P52–P48(B) MSB LSB
d19	**d20**
P15–P10(R), P9–P4(G), P3–P0(B) MSB LSB	P15–P10(R), P9–P4(G), P3–P0(B) P31–P26(R), P25–P20(G), P19–P16(B) MSB LSB
d21	**d22**
P15–P10(R), P9–P4(G), P3–P0(B) P31–P26(R), P25–P20(G), P19–P16(B) P47–P42(R), P41–P36(G), P35–P32(B) P63–P58(R), P57–P52(G), P12–P48(B) MSB LSB	P15–P12(R), P11–P8(G), P7–P4(B), P3–P0(O) MSB LSB
d23	**d24**
P15–P12(R), P11–P8(G), P7–P4(B), P3–P0(O) P31–P28(R), P27–P24(G), P23–P20(B), P19–P16(O) MSB LSB	P15–P12(R), P11–P8(G), P7–P4(B), P3–P0(O) P31–P28(R), P27–P24(G), P23–P20(B), P19–P16(O) P47–P44(R), P43–P40(G), P39–P36(B), P35–P32(O) P63–P60(R), P59–P56(G), P55–P52(B), P51–P48(O) MSB LSB

NOTE 7: The latching sequence is initiated by a rising edge on LCLK. For modes in which multiple pixels are latched on one LCLK rising edge, the pixel clock shifts them out starting with the low-numbered pixel. Note that each line of each table entry above represents one pixel. In the table, P31–P24(B) means P31 = BLUE7 (MSB), P30 = BLUE6, . . ., P24 = BLUE0 (LSB). True-color modes are similar, but the overlay fields are not supported.

Table 2–21. Direct-Color Mode Pixel-Latching Sequence (Big-Endian) (see Note 8)

d9	d10
P31–P24(B), P23–P16(G), P15–P8(R), P7–P0(O) LSB MSB	P31–P24(B), P23–P16(G), P15–P8(R), P7–P0(O) P63–P56(B), P55–P48(G), P47–P40(R), P39–P32(O) LSB MSB
d11	**d12**
P31–P24(O), P23–P16(R), P15–P8(G), P7–P0(B) LSB MSB	P31–P24(O), P23–P16(R), P15–P8(G), P7–P0(B) P63–P56(O), P55–P48(R), P47–P40(G), P39–P32(B) LSB MSB
d13	**d14**
P15–P11(B), P10–P5(G), P4–P0(R) LSB MSB	P15 – P11(B), P10 – P5(G), P4 – P0(R) P31 – P27(B), P26 – P21(G), P20 – P16(R) LSB MSB
d15	**d16**
P15 – P11(B), P10 – P5(G), P4 – P0(R) P31 – P27(B), P26 – P21(G), P20 – P16(R) P47 – P43(B), P42 – P37(G), P36 – P32(R) P63 – P59(B), P58 – P53(G), P52 – P48(R) LSB MSB	P15 – P11(B),P10 – P6(G),P5 – P1(R),P0(O) LSB MSB
d17	**d18**
P15 – P11(B), P10 – P6(G), P5 – P1(R), P0(O) P31 – P27(B), P26 – P22(G), P21 – P17(R), P16(O) LSB MSB	P15 – 11(B), P10 – P6(G), P5 – P1(R), P0(O) P31 – P27(B), P26 – P22(G), P21 – P17(R), P16(O) P47 – P43(B), P42 – P38(G), P37 – P33(R), P32(O) P63 – P59(B), P58 – P54(G), P53 – P49(R), P48(O) LSB MSB
d19	**d20**
P15 – P12(B), P11 – P6(G), P5 – P0(R) LSB MSB	P15 – P12(B), P11 – P6(G), P5 – P0(R) P31 – P28(B), P27 – P22(G), P21 – P16(R) LSB MSB
d21	**d22**
P15 – P12(B), P11 – P6(G), P5 – P0(R) P31 – P28(B), P27 – P22(G), P21 – P16(R) P47 – P44(B), P43 – P38(G), P37 – P32(R) P63 – P60(B), P59 – P54(G), P53 – P48(R) LSB MSB	P15 – P12(O), P11 – P8(B), P7 – P4(G), P3 – P0(R) LSB MSB
d23	**d24**
P15 – P12(O), P11 – P8(B), P7 – P4(G), P3 – P0(R) P31–P28(O),P27– P24(B),P23 – P20(G),P19 – P16(R) LSB MSB	P15 – P12(O), P11 – P8(B), P7 – P4(G), P3 – P0(R) P31–P28(O), P27–P24(B), P23–P20(G), P19–P16(R) P47–P44(O), P43–P40(B), P39–P36(G), P35–P32(R) P63–P60(O), P59–P56(B), P55–P52(G), P51–P48(R) LSB MSB

NOTE 8: The latching sequence is the same as little-endian. Each line represents one pixel. The table assumes that the pixel bus has been externally reverse wired. Therefore, P31–P24(B) in the table means P31 = BLUE0 (LSB), P30 = BLUE1, ..., P24 = BLUE7 (MSB). True-color modes are similar, but overlay fields are not supported.

2.7 On-Chip Cursor

The TVP3026 has an on-chip three-color 64x64 pixel user-definable cursor. The cursor operation defaults to the XGA standard, but X-windows and three-color modes are also available (see subsection 2.7.3, *Three-Color 64 X 64 Cursor*). The cursor operates in both noninterlaced and interlaced modes.

The pattern for the 64 x 64 cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. Cursor positioning is performed using the cursor-position (x,y) registers (see register bit definitions in subsection 2.15.5, *Cursor Position-(x,y) Registers*). Positions x and y are defined in the TVP3026 increasing from left to right and from top to bottom, respectively, as seen on the display screen.

On-chip cursor control is performed by the indirect cursor-control register (index: 0x06). The direct cursor control register provides an alternate means of enabling and disabling the cursor and selecting the cursor mode. See the cursor-control register bit definitions in subsection 2.15.3, *Indirect Cursor Control Register*, and subsection 2.15.4, *Direct Cursor-Control Register*, for more details.

2.7.1 Cursor RAM

The 64 x 64 x 2 cursor RAM defines the pixel pattern within the 64x64 pixel cursor window. It is not initialized and may be written to or read by the MPU at any time, even when the cursor is enabled.

The cursor RAM address zero is at the top left corner of the RAM as shown in Figure 2–8. The 0 bits for the entire cursor array (associated with the cursor plane) cursor plane are stored in the first 512 bytes of the RAM, and the 1 bits for the entire cursor array are stored in the last 512 bytes of the RAM. Information for eight cursor pixels is stored in each byte. The MSB (D7) corresponds with the first or leftmost pixel displayed on the screen.

The 64 x 64 x 2 cursor RAM stores a total of 8192 bits and is accessed through the 8-bit MPU data bus. There are, therefore, 1024 bytes stored in the RAM and a 10-bit address is used. The upper two bits of the cursor RAM address (A9, A8) are written to cursor control register (index: 0x06) bits CCR3 and CCR2. The MSB of the address (CCR3) selects cursor plane 0 or cursor plane 1. The lower eight bits of the cursor RAM address (A7–A0) are written to the cursor RAM write address register (direct register: 0000) for writing to the RAM and to the cursor RAM read address register (direct register: 0011) for reading the RAM. Then the plane 0 or 1 data for the first eight pixels is written to the cursor RAM data register (direct register: 1011). This stores the cursor pixel data in the cursor RAM and automatically increments the cursor RAM address register. The upper two bits of the cursor RAM address also increment when the lower eight bits roll over from 0xFF to 0x00. A second write to the cursor RAM data register loads the plane 0 or 1 data for the next eight cursor pixels, and so on. Update of the entire cursor RAM requires 1024 writes to the cursor RAM data register.

To read from the cursor RAM, the address of the first cursor-RAM location to be read is loaded using CCR3 and CCR2 and the cursor-RAM read address register. Then a read is performed on the cursor-RAM data register (direct register: 1011) which reads the plane 0 or 1 data for eight consecutive pixels. Similar to the cursor RAM write operation, when the read is completed, CCR3 and CCR2 and the cursor-RAM address register are automatically incremented and further reads are made to successive cursor RAM locations. Upload of the entire cursor RAM requires 1024 reads of the cursor RAM data register.

NOTES

The cursor RAM upper address bits CCR3 and CCR2 in the cursor control register default to zeros after reset. Since software normally sets these bits to 0s before accessing the cursor RAM, it may not be necessary to write to CCR3 and CCR2

Internally, the entire 10-bit address is loaded into the address counter after a write to the cursor RAM address register (direct register, 0000 or 0011), so CCR3 and CCR2 should be written first if they are to be changed.

Vertical retrace is determined by detecting 2048 or 4096 pixel clocks between rising edges of the internal $\overline{\text{BLANK}}$ signal. CCR4 selects 2048 when reset to 0 and 4096 when set to 1.

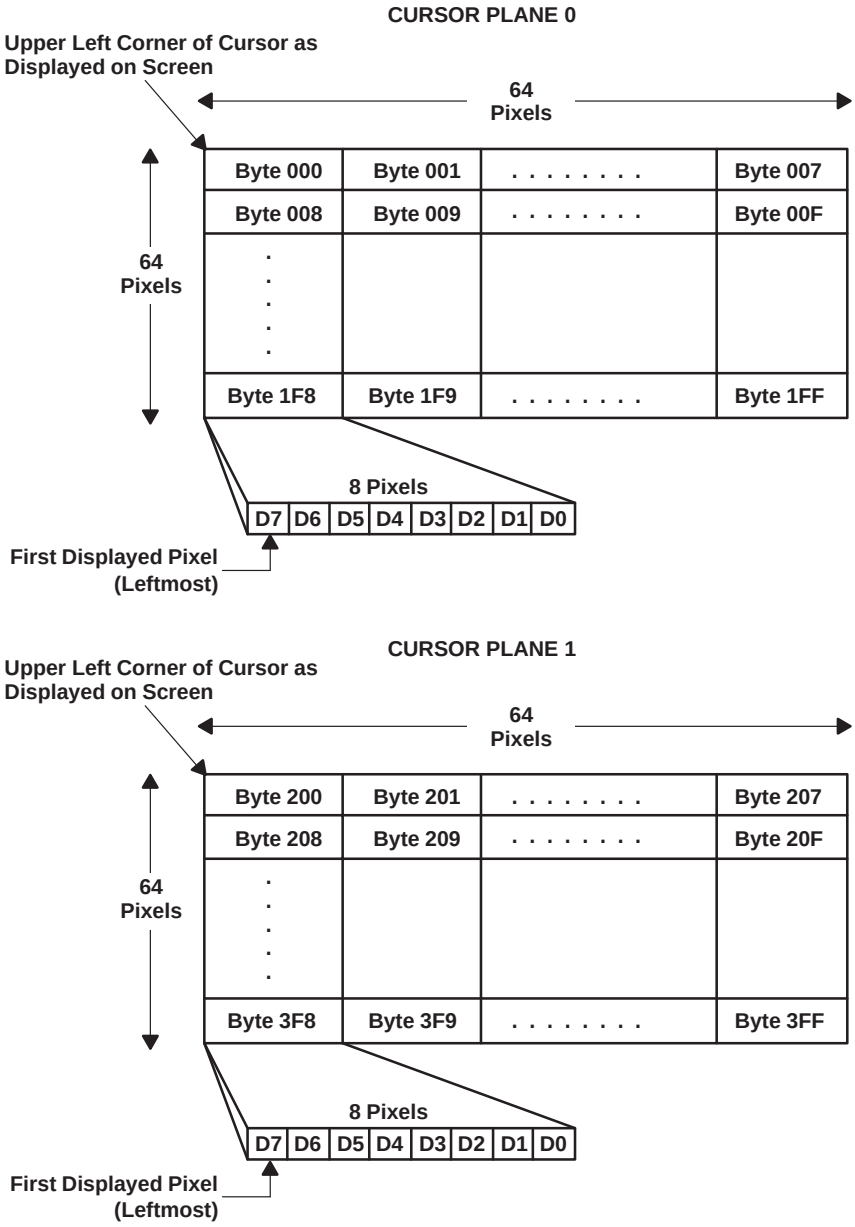


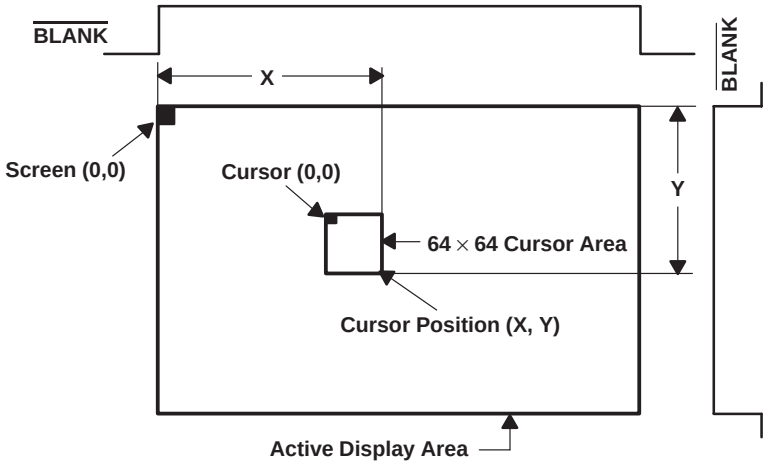
Figure 2–8. Cursor-RAM Organization

2.7.2 Cursor Positioning

The cursor-position (x,y) registers position the 64 x 64 cursor on the display screen. The cursor-position (x,y) registers specify the location of the cursor bottom right corner on the display screen relative to the end of the internal $\overline{\text{BLANK}}$ signal. Figure 2–9 shows the orientation of the x,y coordinates for positioning the cursor.

The values written to the cursor position registers represent the position of the bottom right corner of the cursor. When zero is written to the cursor position x or cursor position y registers, the cursor is off the screen. When the cursor position (x,y) is (1,1), only a single pixel of the cursor (cursor 63,63)is displayed and it appears at the upper left corner of the screen.

When the upper left corner of the cursor is preferred as a reference, determine the screen (x,y) coordinate where cursor (0,0) is to be positioned. Then add 64 (0x40) to the x coordinate and add 64 (0x40) to the y coordinate and write these values to the cursor position (x,y) registers. For example, when the upper left corner of the cursor is to be positioned at screen (0,0), write (0x40, 0x40) to the cursor (x, y) registers.



Cursor Position (X,Y) = Screen (X,Y) Where Cursor (0,0) is Located + (64,64)

Figure 2–9. Cursor Positioning

2.7.3 Three-Color 64 x 64 Cursor

The 64 x 64 x 2 cursor RAM provides two bits of cursor information on every dot clock cycle during the 64 x 64 cursor window. CCR1 and CCR0 specifiy whether the XGA mode (10) or X-window mode (11) or 3-color mode (01) interprets the cursor information. When CCR1 and CCR0 are 00, the cursor is disabled. The cursor enable/disable and mode select may also be programmed using the direct cursor control register. The two bits of cursor pixel data determine the cursor appearance as shown in Table 2-22.

Table 2–22. Cursor RAM Vs. Color Selection

RAM		COLOR SELECTION		
PLANE 1	PLANE 0	THREE-COLOR MODE	XGA MODE	X-WINDOW MODE
0	0	Transparent	Cursor color 0	Transparent
0	1	Cursor color 0	Cursor color 1	Transparent
1	0	Cursor color 1	Transparent	Cursor color 0
1	1	Cursor color 2	Complement	Cursor color 1

Cursor color 0, 1, and 3: These colors are set by writing to the cursor-color registers.

Transparent: The underlying pixel color is displayed.

Complement: The 1s complement of the underlying pixel color is displayed.

2.7.4 Interlaced Cursor Operation

The cursor supports an interlaced display when bit CCR5 in the cursor control register is set to 1. For the purposes of this discussion assume that the interlaced display consists of an even field of scan lines numbered 0, 2, 4, . . ., etc., and an odd field of scan lines numbered 1, 3, 5, . . ., etc. Scan line 0 is the first scan line at the top of the display. When interlaced mode is enabled and cursor position y (CPy) is greater than 64 (0x40) and less than or equal to 4095 (0xFFF), the first cursor line displayed depends on the state of the ODD/EVEN terminal and value of CPy.

When CPy is an even number, the data in row 0 of the cursor RAM array is displayed during the even field (ODD/EVEN = 0), followed by rows 2, 4, . . ., 62 on successive scan lines. The data in row 1 of the cursor RAM array is displayed during the odd field (ODD/EVEN = 1), followed by rows 3, 5, . . ., 63 on successive scan lines.

When CPy is an odd number, the data in row 0 of the cursor RAM array is displayed during the odd field (ODD/EVEN = 1), followed by rows 2, 4, . . ., 62 on successive scan lines. The data in row 1 of the cursor RAM array is displayed during the even field (ODD/EVEN = 0), followed by rows 3, 5, . . ., 63 on successive scan lines.

When CPy is between 0 and 64 (0x40), the cursor is partially off the top of the screen. In this case, the data in the first displayed row of the cursor RAM (row N) is always displayed on scan line 0, which is the first scan line of the even field, followed by rows N + 2, N + 4, . . ., etc. on successive scan lines. The data in row N + 1 is displayed on scan line 1, which is the first scan line of the odd field, followed by cursor rows N + 3, N + 5, . . ., etc. on successive scan lines.

The CCR6 bit of the cursor control register allows the polarity of the received ODD/EVEN signal to be inverted when set to 1.

2.8 Port-Select and Color-Key Switching

The TVP3026 provides two integrated mechanisms for switching between direct-color images and overlay graphics or between direct-color images and gamma-corrected true-color images midscreen. The port-select function utilizes the external PSEL terminal to enable the display of multiple true-color or overlay and direct-color on screen. The color-key switching function combines images on screen based on color comparison with stored color range registers.

The port-select function is controlled by the miscellaneous-control register (index: 0x1E, see subsection 2.15.2, *Miscellaneous-Control Register*, for register bit definitions). For switching between direct-color and true-color, a true-color mode must be selected from Table 2–17. For switching between direct-color and overlay, a direct-color mode must be selected from Table 2–17 and the VGA port must be disabled (MCR7 = 0). Overlay switching is not supported for those direct-color modes that do not have overlay capability. In all cases, the color-key switching function should be disabled and direct-color (CKC4 = CKC3 = CKC2 = CKC1 = CKC0 = 0) selected. The miscellaneous-control register enables the port-select function and defines the polarity of PSEL. Since PSEL is sampled with LCLK, the granularity for port-select switching depends on the number of pixels loaded for each LCLK.

The color-key switching function is controlled by the color-key-control register (index: 0x38, see subsection 2.15.7, *Color-Key Control Register*, for register definition). For switching between direct-color and true-color, a true-color mode must be selected from Table 2–17. The incoming red, green, and blue color fields are compared with their respective color range registers before gamma correction occurs. The overlay terminals could also be used for the color comparison, although the overlay information is not displayable in true-color mode. For switching between direct-color and overlay, a direct color mode must be selected from Table 2–17 and the VGA port must be disabled (MCR7 = 0). In all cases, the port-select function should be disabled and direct-color(MSC5 = 1, MSC4 = 0) selected. The color-key control register enables/disables the red, green, blue, and/or overlay range comparators and defines the polarity of the color-key switching function. The comparison values are then written to the eight 8-bit color-key-range registers; color key overlay (low, high), color key red (low, high), color key green (low, high), and color key blue (low, high). These registers are accessed through index 0x30 through index 0x37. The granularity for color-key switching is on a pixel-by-pixel basis.

The port-select and color-key functions are integrated like a logical OR function. When either of the functions switches to palette graphics (true-color or overlay through the palette RAM), palette graphics are displayed instead of direct color. Therefore, when programming the device for any direct color mode, both the color-key-control and miscellaneous-control registers must be set so that direct color graphics is displayed. For true color, gamma corrected through the palette, one of the functions must be set to palette graphics.

2.8.1 Port-Select Switching

The port-select switching function is governed by the following equation:

$$SWITCH = (PSEL \times MSC4) \oplus \overline{MSC5} \quad (11)$$

where:

MSCn is the nth bit of the miscellaneous control register.

Table 2-23 then applies:

Table 2–23. Port-Select Switching

MULTIPLEX MODE SELECTED	DISPLAY RESULT	
	SWITCH = 0	SWITCH = 1
Direct-color with overlay	Direct-color	Overlay
Direct-color with true-color	Direct-color	True-color

NOTES

The DAC output is undefined if SWITCH = 1 when doing overlay switching in a direct-color mode that does not have overlay capability.

Miscellaneous-control register bits MSC5 and MSC4 enable or disable the port select function and select the polarity, as shown in the equation above. When port-select switching is disabled (MSC4 = 0), MSC5 sets the port-select function to either palette graphics (MSC5 = 0, default) or direct-color graphics (MSC5 = 1).

The device supports port-select switching when using multiplexing modes. However, caution must be observed when using the port-select function with the multiplexing modes other than 1:1, since the PSEL signal is latched on LCLK (same as the pixel port). Port-select switching on a pixel basis with multiplexing modes other than 1:1 can be accomplished using the color-key switching function by supplying multiple PSEL signals, one per pixel, into the available overlay terminals.

2.8.2 Color-Key Switching

The TVP3026 supports color-key-switching modes in which color data from the direct-color and overlay ports is compared to a set of user-definable color-key registers. Based on the outcome of the comparison, either direct color, true-color, or overlay, is displayed. High and low color-key registers are provided for each color and overlay so that ranges of colors can be compared as opposed to a single color value. The color-key function is controlled by the color-key-control register bits CKC0–CKC4 according to the following equation:

$$COLOR\text{–}KEY = [(OL + \overline{CKC0}) \times (R + \overline{CKC1}) \times (G + \overline{CKC2}) \times (B + \overline{CKC3})] \oplus \overline{CKC4} \quad (12)$$

where:	OL = 1	if	color-key OL low	≤ overlay (Note 17)	≤ color-key OL high
	R = 1	if	color-key red low	≤ direct color (RED)	≤ color-key red high
	G = 1	if	color-key green low	≤ direct color (GREEN)	≤ color-key green high
	B = 1	if	color-key blue low	≤ direct color (BLUE)	≤ color-key blue high

then if COLOR–KEY = 1, overlay or true-color is displayed.
if COLOR–KEY = 0, direct-color is displayed.

NOTES

CKC0–CKC3 can be used to individually enable or disable certain colors in the comparison for maximum flexibility. When color-key switching is not desired, CKC0–CKC3 should be set to 0. CKC4 then sets the default for either direct color or palette graphics. The default condition at reset is CKC0 = CKC1 = CKC2 = CKC3 = CKC4 = 0. This causes the color-key function to default to direct-color graphics.

The color-key comparison for the overlay data is performed after the read mask and palette page registers so that an 8-bit comparison can be performed. This also gives the maximum flexibility to the user in performing the color comparisons. If the overlay defined for a given mode is less than 8 bits per pixel, the data is shifted to the LSB locations and the palette-page register (index: 0x1C) fills the remaining MSB positions.

For those direct-color modes that have less than 8 bits for each pixel of red, green, and blue direct-color data, the data is internally shifted to the MSB positions for each color and the remaining LSB bits are filled with zeros before the 8-bit comparisons are performed.

2.9 Overscan Border

The TVP3026 provides the capability to produce a custom screen border using the overscan function. The overscan function is enabled by the general-control register bit GCR6. The overscan color is user-programmable by loading the overscan color red, green, and blue registers (see subsection 2.1.4, *Cursor and Overscan Color Registers*).

When the overscan function is enabled (GCR6 = 1), then the overscan color is displayed any time that OVS is high and $\overline{\text{BLANK}}$ is low (active). The blanking pedestal is imposed on the analog outputs when both OVS and $\overline{\text{BLANK}}$ are low. When overscan is disabled, then the blanking pedestal occurs whenever $\overline{\text{BLANK}}$ is low.

The OVS terminal is always sampled on LCLK. Therefore, overscan can only be used with the VGA port in VGA mode 1 (MSC6 = 1 in the multiplex control register). This selects $\overline{\text{SYSBL}}$, $\overline{\text{SYSHS}}$, $\overline{\text{SYSVS}}$, and LCLK latching of the VGA port.

Figure 2–10 demonstrates the use of OVS to produce a custom overscan screen border.

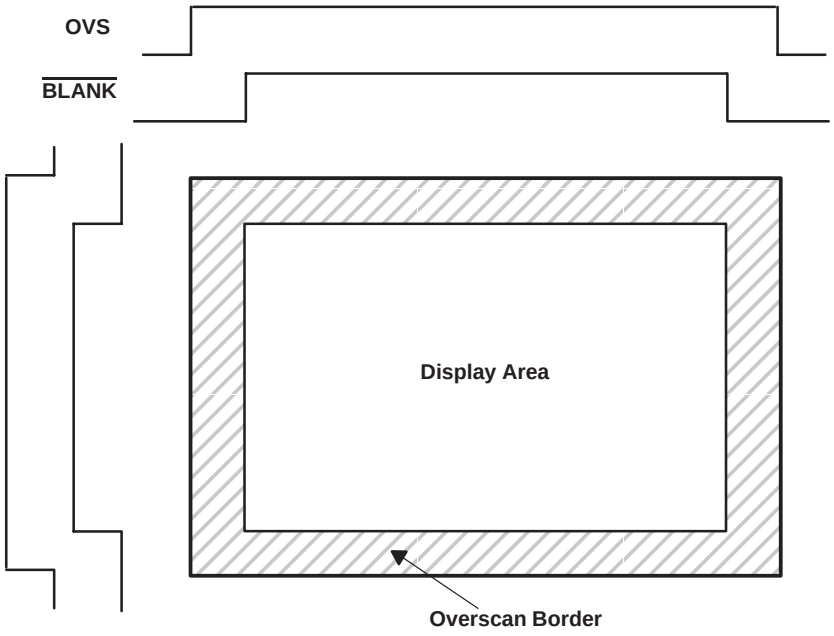


Figure 2–10. Overscan

2.10 Horizontal Zooming

The TVP3026 supports a user-programmable horizontal zooming function of 2, 4, 8, 16, or 32×. Zooming is controlled through the CKC5–CKC7 bits of the color-key control register (index: 0x38, see subsection 2.15.7, *Color-Key Control Register*, for the color-key control register definition).

When one of the horizontal zoom factors (other than 1×) is chosen, the internal pixel multiplexer is configured so that it replicates the pixel data on successive dot clocks by the number of times specified by CKC5–CKC7. Also, the RCLK frequency must be modified by changing the loop clock PLL registers to load pixel data at the new reduced rate. The new RCLK frequency should be chosen as the old RCLK frequency divided by the zoom factor.

The horizontal zoom function applies only to the pixel port (P63–P0) data. VGA data cannot be zoomed. The maximum zoom factor for all packed-24 modes is 8×. When zooming in 5:4 packed-24 mode, the latch control register setting depends on the zoom factor as described in subsection 2.15.6, *Latch-Control Register*.

2.11 Test Functions

The TVP3026 provides several functions that enable system testing and verification. These are detailed in subsection 2.11.1, *16-Bit CRC*, through subsection 2.11.4, *Silicon Revision*.

2.11.1 16-Bit CRC

A 16-bit cyclic redundancy check (CRC) is provided so that video data integrity can be verified at the input to the DACs. The CRC is updated when two consecutive horizontal sync (HSYNC) pulses are detected while blanking is active (vertical retrace). For the use of the CRC function, HSYNC must be active low at the input to the TVP3026. The CRC is only calculated on the active screen area, i.e., active blanking stops the calculation. One complete vertical screen must be completed to generate a valid CRC.

The CRC can be performed on any of the 24 data lines that enter the DACs and is controlled by the CRC bit select register (index: 0x3E). Values from 0 to 23 (0x17) may be written to this register to select between

the 24 different DAC data inputs. The 16-bit remainder that is calculated on the individual DAC data line can be read from the CRC remainder LSB and CRC remainder MSB registers. See subsection 2.15.9, *CRC Remainder LSB and MSB Registers*, and subsection 2.15.10, *CRC Bit-Select Register*, for the CRC register bit definitions.

As long as the display pattern for each screen remains fixed, the CRC result should remain constant. When the CRC result changes, an error condition should be assumed. The CRC is calculated using the algorithm depicted by the circuit in Figure 2–11. The user can calculate and store the CRC remainder for a test screen in software and compare this to the TVP3026 calculated CRC remainder to verify data integrity.

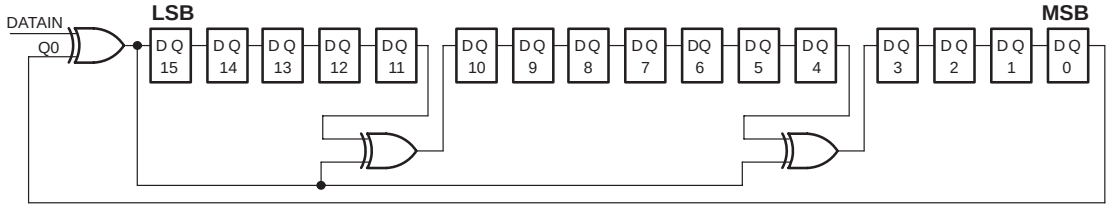


Figure 2–11. CRC Algorithm

2.11.2 Sense Comparator Output and Test Register

The TVP3026 provides a $\overline{\text{SENSE}}$ output to support system diagnostics. $\overline{\text{SENSE}}$ can determine the presence of the CRT monitor or verify that the RGB termination is correct. $\overline{\text{SENSE}}$ is reset to 0 when one or more of the DAC outputs exceeds the internal comparator voltage of 350 mV. The internal 350-mV reference has a tolerance of ±50 mV when using an external 1.235-V reference. When the internal voltage reference is used, the tolerance is higher.

The sense comparators are also integrated with the sense test register (index: 0x3A) so that the comparison results for the red, green, and blue comparators can be read independently through the 8-bit microinterface. When the sense test register (STR) is read, the results are indicated in the bit positions of Table 2-24.

Table 2–24. Sense Test Register Results

INDEX: 0x3A, ACCESS: R/W, DEFAULT: UNINITIALIZED								
STR BITS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Data	DIS	0	0	0	0	R	G	B

where: R = set to 1 if IOR > 350 mV
G = set to 1 if IOG > 350 mV
B = set to 1 if IOB > 350 mV
D6 – D3 are reserved
D7 is disable (set to 1) bit

NOTE

D7 can be set to 1 to disable the sense comparison function. At reset, the sense comparison is enabled (D7 = 0). D6–D3 are reserved. When this register is written to, to disable the sense comparator function, bits D6–D0 need to be reset 0.

Both the SENSE output and the sense test register are latched by the falling edge of the internally sampled blank signal ($\overline{\text{SYSBL}}$ or $\overline{\text{VGABL}}$ depending on bit MCR6). In order to have stable voltage inputs to the comparators, the frame-buffer inputs should be set such that data entering the DACs remains unchanged for a sufficient period of time prior to and after the BLANK signal falling edge.

2.11.3 Identification Code

An ID register with a hardwired code is provided that can be used as a software identification of the device for different versions of the system design. The ID register is read only through index 0x3F. The value defined for the TVP3026 is 0x26.

2.11.4 Silicon Revision

The silicon revision register (index: 0x01) is a read-only register that enables software to identify the silicon revision of the TVP3026. On the first pass silicon, this register reads back 0x00. A major revision number is stored in bits 7–4 and a minor revision number is stored in bits 3–0.

2.12 General-Purpose I/O Register and Terminals

The general-purpose I/O register and output terminals provide a means of controlling external functions through the TVP3026 microinterface. The 8-bit general-purpose I/O data register has five bit locations (D0–D4) tied to external I/O terminals (GI/O0–GI/O4). The other three bits (D5–D7) can be used for general data storage and do not affect any other circuitry. The general-purpose I/O data register is controlled by the general-purpose I/O control register. GP I/O control register bits IOC0–IOC4 control whether the corresponding general-purpose I/O terminals are configured as inputs or outputs. The reset default condition is for GP I/O control register bits IOC0–IOC4 = 0, which configures terminals GI/O0–GI/O4 as inputs. When any of the GP I/O control register bits are set to 1, the corresponding GI/O terminals are configured as outputs.

The general-purpose I/O control register, data register, and terminal relationships are shown in Table 2–25.

Table 2–25. General Purpose I/O Registers

	DATA BIT							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
General-Purpose I/O Control Register Index: 0x2A Access: R/W Default: 0x00	X	X	X	IOC4	IOC3	IOC2	IOC1	IOC0
General-Purpose I/O Data Register Index: 0x2B Access: R/W Default: Uninitialized	X	X	X	D4	D3	D2	D1	D0
General-Purpose I/O Terminal Locations				GI/O4	GI/O3	GI/O2	GI/O1	GI/O0

X = do not care

2.13 Reset

There are two ways to reset the TVP3026. The $\overline{\text{RESET}}$ input terminal can perform a hardware reset. Alternatively, the device has an integrated software reset function.

A hardware reset is initiated by pulling the $\overline{\text{RESET}}$ input terminal low. When $\overline{\text{RESET}}$ is pulled low all TVP3026 registers go to default states. This reset is asynchronous, and any glitch on this terminal could change the intended register setup. The default state at reset is VGA mode, and all default register settings are given in Table 2–2. When a reset is desired at power up, an external resistor, capacitor, and diode network can be connected to the $\overline{\text{RESET}}$ terminal. When TTL logic is employed to provide the signal to the $\overline{\text{RESET}}$ terminal, a pullup resistor should be used to make sure that CMOS levels are achieved.

For a software reset, anytime the reset register (index: 0xFF) is written to, all registers are initialized to TVP3026 default settings. The data written into the reset register is ignored.

2.14 Analog Output Specifications

The DAC outputs are controlled by three current sources (only two for IOR and IOB) as shown in Figure 2–12. The default condition is to have 0 IRE difference between blank and black levels, which is shown in Figure 2–13. When a 7.5-IRE (Institute of Radio Engineers, predecessor to the IEEE) pedestal is desired, it can be selected by setting bit 4 of the general-control register. This video output is shown in Figure 2–14.

A resistor (R_{SET}) is needed between the FS ADJUST terminal and GND to control the magnitude of the full-scale video signal. The IRE relationships in Figures 2–13 and 2–14 are maintained regardless of the full-scale output current.

The relationship between R_{SET} and the full-scale output current IOG is:

$$R_{SET}\ (\Omega) = K1 \times V_{ref}\ (V) / IOG\ (mA) \quad (13)$$

The full-scale output current on IOR and IOB for a given R_{SET} is:

$$IOR,\ IOB\ (mA) = K2 \times V_{ref}\ (V) / R_{SET}\ (\Omega) \quad (14)$$

where K1 and K2 are defined as:

PEDESTAL	IOG		IOR, IOB	
	8-BIT OUTPUT	6-BIT OUTPUT	8-BIT OUTPUT	6-BIT OUTPUT
7.5 IRE	K1 = 11,294	K1 = 11,206	K2 = 8,067	K2 = 7,979
0 IRE	K1 = 10,684	K1 =10,600	K2 = 7,462	K2 = 7,374

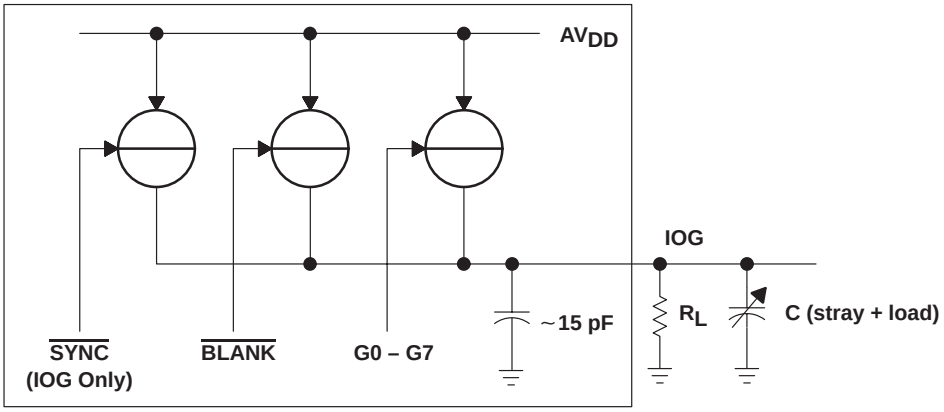
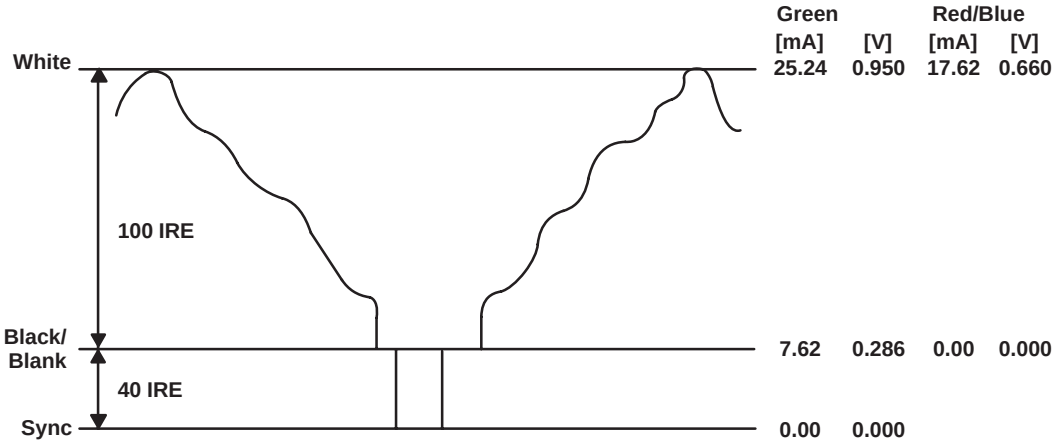
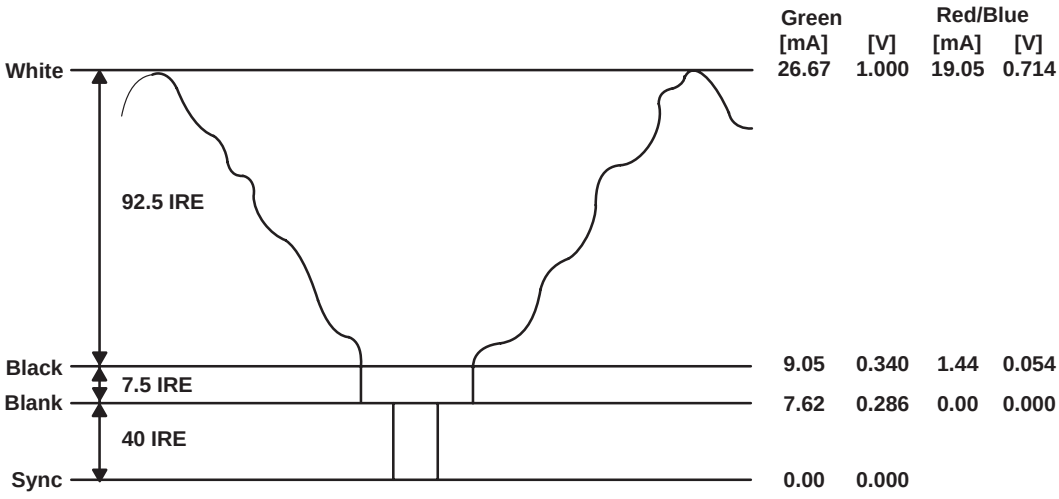


Figure 2–12. Equivalent Circuit of the Current Output (IOG)



NOTE A: 75-Ω doubly terminated load, V_{ref} = 1.235 V, R_{SET} = 523 Ω. RS343A-levels and tolerances are assumed on all levels.

Figure 2–13. Composite Video Output (With 0 IRE, 8-Bit Output)



NOTE A: 75-Ω doubly terminated load, V_{ref} = 1.235 V, R_{SET} = 523 Ω. RS343A-levels and tolerances are assumed on all levels.

Figure 2–14. Composite Video Output (With 7.5 IRE, 8-Bit Output)

2.15 Register Definitions

2.15.1 General-Control Register (Index: 0x1D, Access: R/W, Default: 0x00)

The general-control register definition is listed in Table 2–26.

Table 2–26. General-Control Register

BIT NAME	VALUES	DESCRIPTION
GCR7	0	Reserved
GCR6	0: Disable (default) 1: Enable	Overscan enable. GCR6 specifies whether to enable the user-defined overscan screen border.
GCR5	0: Disable (default) 1: Enable	Sync enable. Bit GCR5 specifies whether sync information is to be output onto IOG.
GCR4	0: 0 IRE (default) 1: 7.5 IRE	Pedestal control. GCR4 specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs.
GCR3	0: Little-endian (default) 1: Big-endian	Little-endian/big-endian select. GCR3 selects either little- or big-endian format for the pixel-bus interface.
GCR2	0	Reserved
GCR1	0: Do not invert (default) 1: Invert	VSYNCOUT output polarity. GCR1 specifies whether vertical sync output is positive or negative.
GCR0	0: Do not invert (default) 1: Invert (high)	HSYNCOUT output polarity. GCR0 specifies whether horizontal sync output is positive or negative.

2.15.2 Miscellaneous-Control Register (Index: 0x1E, Access: R/W, Default: 0x00)

The miscellaneous-control register definition is listed in Table 2–27.

Table 2–27. Miscellaneous-Control Register

BIT NAME	VALUES	DESCRIPTION (SEE NOTE 9)
MSC7	0	Reserved
MSC6	0	Reserved
MSC5	0: True function (default) 1: Complementary	PSEL polarity select. When MSC5 is reset to 0 and setting PSEL to active high selects direct-color (provided that the color-key function is set to select direct-color). When MSC5 is set to 1, and then PSEL high selects pseudo-color or true-color.
MSC4	0: Disable (default) 1: Enable	Port select switching enable. When MSC4 is set to 1, direct-color/true-color or direct-color/overlay switching is controlled by the PSEL input. MSC5 controls the polarity of the PSEL input.
MSC3	0: 6-bit (default) 1: 8-bit	8- or 6-bit operation bit. When MSC2 is set to 1, MSCR3 determines 8- or 6-bit operation.
MSC2	0: Enable (default) 1: Disable	8/$\overline{6}$ terminal disable. When MSC2 is set to 1, the 8/$\overline{6}$ terminal is ignored and the 8/$\overline{6}$ function is controlled by bit 3 of this register.
MSC1	0	Reserved
MSC0	0: Disable (default) 1: Enable	DAC power down. When MSC0 is set to 1, the DACs power down.

NOTE 9: Additional power reduction can be achieved by disabling the internal dot clock by writing the binary value 110 to clock selection register (index: 0x1A) bits 2–0.

2.15.3 Indirect Cursor-Control Register (Index: 0x06, Access: R/W, Default: 0x00)

The indirect cursor-control register is accessed using the indirect register map. This register provides for enabling and disabling the cursor and other cursor controls. The cursor mode-select may also be controlled using the direct cursor-control register. The indirect cursor-control register definition is listed in Table 2–28.

Table 2–28. Indirect Cursor-Control Register

BIT NAME	VALUES	DESCRIPTION
CCR7	0: Use indirect CCR (default)	Cursor control register select. CCR7 selects which cursor control register is used (direct or indirect). The video BIOS must initialize this bit to 1 for driver software that uses the direct cursor control register.
	1: Use direct CCR	
CCR6	0: Normal (default)	ODD/$\overline{\text{EVEN}}$ sense invert. When CCR6 is reset to 0, the field indicator ODD/$\overline{\text{EVEN}}$ used by the hardware cursor in interlaced display mode, is set to 1 for the odd field and is reset to 0 for the even field. When CCR6 is set to 1, the polarity of ODD/$\overline{\text{EVEN}}$ is the opposite.
	1: Invert	
CCR5	0: Disable (default)	Enable interlaced cursor. When CCR5 is set to 1, interlaced cursor operation is enabled. During interlaced cursor operation, the ODD/$\overline{\text{EVEN}}$ terminal indicates the odd or even field, as determined by value in CCR6.
	1: Enable	
CCR4	0: 2048 pixels (default)	Vertical blank detection method. Vertical blank is detected using only the blank signal. The logic detects when there has been either 2048 or 4096 consecutive dot clocks between rising edges of $\overline{\text{BLANK}}$.
	1: 4096 pixels	
CCR3, CCR2	00: (default)	Cursor RAM address bits 9 and 8. CCR3 is bit 9 and CCR2 is bit 8. These bits are used with the lower 8 bits of the cursor RAM address supplied by the cursor RAM address register in the direct register map.
CCR1, CCR0	00: Cursor off (default)	Cursor mode select. CCR1 and CCR0 disable the cursor and select the format used to interpret the information stored in the cursor RAM when displaying the cursor. See Table 2–27.
	01: Three-color cursor	
	10: XGA cursor	
	11: X-windows cursor	

2.15.4 Direct Cursor-Control Register (Direct Register: 1001, Access: R/W, Default: 0x00)

The direct cursor control register is accessed using the direct register map. This register provides an alternate means of enabling and disabling the cursor and selecting the cursor mode. This register is provided for compatibility with commonly used software drivers. The direct cursor-control register definition is listed in Table 2–29.

Table 2–29. Direct Cursor-Control Register

BIT NAME	VALUES	DESCRIPTION
DCC7–DCC2	000000	Reserved
DCC1, DCC0	00: Cursor off (default)	Cursor mode select. DCC1 and DCC0 disable the cursor and select the format used to interpret the information stored in the cursor RAM when displaying the cursor. See Table 2–27.
	01: Three color cursor	
	10: XGA cursor	
	11: X-windows cursor	

2.15.5 Cursor-Position (x, y) Registers (Direct Register: 1100 – 1111, Access: R/W, Default: Uninitialized)

These registers specify the (x,y) coordinate of the lower right corner of the cursor, see Table 2-30. All registers are uninitialized and may be written to or read from by the MPU at any time.

Table 2–30. Cursor-Position (x, y) Registers

	CURSOR-POSITION X MSB								**CURSOR-POSITION X LSB**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Position	0	0	0	0	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	Direct register 1101								Direct register 1100							
	CURSOR-POSITION Y MSB								**CURSOR-POSITION Y LSB**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Position	0	0	0	0	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	Direct register 1111								Direct register 1110							

The cursor-position X and Y values to be written are calculated as follows:

CPx = desired display screen x position for upper left corner of cursor + 0x40

CPy = desired display screen y position for upper left corner of cursor + 0x40

Values from 0 to 4095 (0xFFF) can be written into the cursor-position X and Y registers. The values written into the cursor-position X and Y registers are the screen coordinates for the lower right corner of the cursor. When zero is written to either the CPx or CPy registers, the cursor is positioned off screen. See subsection 2.7.2, *Cursor Positoning*.

2.15.6 Color-Key Control Register (Index 0x38, Access R/W, Default 0x00)

The color-key control register definition is listed in Table 2–31.

Table 2–31. Color-Key Control Register

BIT NAME	VALUES	DESCRIPTION
CKC7–CKC5	000: 1× zoom	Horizontal zoom factor. When other than 1× zoom is selected, the internal pixel multiplier is configured so that it loads pixel data at a reduced rate. Also, the RCLK frequency must be modified to facilitate the new reduced rate. The new RCLK frequency should be chosen as the old RCLK frequency divided by the zoom factor. The horizontal zoom function applies only to the pixel port (P63–P0) data. VGA data cannot be zoomed.
	001: 2× zoom	
	010: 4× zoom	
	011: 8× zoom	
	100: 16× zoom	
	101: 32× zoom	
CKC4	0: True function	Color-key-function select. CKC4 controls the polarity of the color-key function. See equation (12) in subsection 2.8.2, *Color-Key Switching*.
	1: Complementary (default)	
CKC3	0: Disable compare (default)	Blue-compare enable. CKC3 enables or disables the direct-color blue field comparison. See equation (12) in subsection 2.8.2, *Color-Key Switching*.
	1: Enable compare	
CKC2	0: Disable compare (default)	Green-compare enable. This is used to enable or disable the direct-color green field comparison. See equation (12) in subsection 2.8.2, *Color-Key Switching*.
	1: Enable compare	
CKC1	0: Disable compare (default)	Red-compare enable. This is used to enable or disable the direct-color red field comparison. See equation (12) in subsection 2.8.2, *Color-Key Switching*.
	1: Enable compare	
CKC0	0: Disable compare (default)	Overlay compare enable. This is used to enable or disable the overlay field comparison. See equation (12) in subsection 2.8.2, *Color-Key Switching*.
	1: Enable compare	

2.15.7 Color-Key (Overlay, Red, Green, Blue) Registers (Index: 0x30–0x37, Access: R/W, Default: Uninitialized)

These registers specify the color comparison ranges for the four direct-color data fields when performing color-key switching. A low and a high register are provided for each of the four data fields to facilitate the range comparison. See subsection 2.8.2, *Color-Key Switching*, for more details on their usage. There are eight registers total, two for each color and associated overlay. The formats for both low and high registers are shown in Table 2-32. Values 0 to 0xFF may be written into the four color-key-low and four color-key-high registers.

Table 2–32. Color-Key Low and High Registers

	COLOR-KEY LOW							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Low Value	L7	L6	L5	L4	L3	L2	L1	L0
	Index = 0x30, 0x32, 0x34, and 0x36							
	COLOR-KEY HIGH							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
High Value	H7	H6	H5	H4	H3	H2	H1	H0
	Index = 0x31, 0x33, 0x35, and 0x37							

2.15.8 CRC Remainder LSB and MSB Registers (Index: 0x3C–0x3D, Access: Read Only, Default: Uninitialized)

These registers read the result of the 16-bit CRC calculation (see subsection 2.11.1, *16-Bit CRC*). They are not initialized and can be read by the MPU at any time. The CRC is updated when two consecutive HSYNC pulses are detected while BLANK is active (vertical retrace). The CRC is only calculated on the active screen area, i.e., active blanking stops the calculation, see Table 2-33. One complete vertical screen must be completed to generate a valid CRC.

Table 2–33. CRC Remainder LSB and MSB Registers

	CRC MSB								CRC LSB							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
CRC Remainder	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
	Index = 0x3D								Index = 0x3C							

2.15.9 CRC Bit Select Register (Index: 0x3E, Access: Write Only, Default: Uninitialized)

This write-only register specifies which of the 24 DAC data lines the 16-bit CRC should be calculated on (see subsection 2.11.1, *16-Bit CRC*). The register is not initialized and can be written to by the MPU at any time. The CRC bit select register data format is shown in Table 2-34. Values from 0 to 23 (0x17) may be written into the register to select the appropriate data line.

Table 2–34. CRC Bit Select Register

BIT NAME	VALUES	DESCRIPTION
BSR7–BSR5	000	Reserved
BSR4–BSR0	0x00–0x07: red0–red7	CRC control code. BSR4–BSR0 selects one of the 24 DAC input lines as the input to the CRC calculation.
	0x08–0x0F: green0–green7	
	0x10–0x17: blue0–blue7	

3 Electrical Characteristics

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Input voltage range, V_I . . . . . −0.5 V to V_{DD} + 0.5 V
Analog output short-circuit duration to any power supply or common . . . . . unlimited
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Junction temperature, T_J . . . . . 175°C
Case temperature for 10 seconds, T_C . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltages, AV_{DD}, DV_{DD}	4.75	5	5.25	V
Reference voltage, V_{ref}	1.15	1.235	1.26	V
High-level input voltage, V_{IH}	2.4		V_{DD}+0.5	V
Low-level input voltage, V_{IL}			0.8	V
Output load resistance, R_L		37.5		Ω
FS ADJUST resistor, R_{SET}		523		Ω
XTAL1/XTAL2 crystal frequency		14.31818		MHz
Operating free-air temperature, T_A	0		70	°C

3.3 Electrical Characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = –800 µA	2.4			V
V_{OL}	Low-level output voltage	D(7–0), GI/O (4–0), VCLK, RCLK, SENSE, PCLKOUT, MCLK	I_{OL} = 3.2 mA			0.4	V
		HSYNCOUT, VSYNCOUT	I_{OL} = 15 mA			0.4	
		SCLK	I_{OL} = 18 mA			0.4	
I_{IH}	High-level input current	TTL inputs	V_I = 2.4 V			1	µA
		ECL inputs	V_I = 4 V			1	
I_{IL}	Low-level input current	TTL inputs	V_I = 0.8 V			–1	µA
		ECL inputs	V_I = 0.4 V			–1	
I_{DD}	Supply current	TVP3026-135A				500	mA
		TVP3026-175A				550	
		TVP3026-175B				350	mA
		TVP3026-220A				650	mA
		TVP3026-220B				450	mA
		TVP3026-250A				650	mA
		TVP3026-250B				530	mA
I_{DD}	Supply current reduction	TVP3026-135	DAC disabled		60		mA
		TVP3026-175			60		
		TVP3026-220			60		
		TVP3026-250			60		
		TVP3026-135A	DAC and DOT CLOCK disabled		300		mA
		TVP3026-175A			350		
		TVP3026-175B			200		mA
		TVP3026-220A			450		mA
		TVP3026-220B			300		mA
		TVP3026-250A			450		mA
		TVP3026-250B			380		mA
I_{OZ}	High-impedance-state output current					10	µA
C_i	Input capacitance	TTL inputs	f = 1 MHz, V_I = 2.4 V		4		pF
		ECL inputs	f = 1 MHz, V_I = 4 V		4		
V_{ID}	Differential input voltage	ECL inputs		0.6		6	V
V_{IC}	Common-mode input voltage	ECL inputs		2.85	3.15	V_{DD}–0.5	V

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

3.4 Operating Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution (each DAC)	8/$\overline{6}$ high		8		bits
		8/$\overline{6}$ low		6		
E_L	End-point linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
E_D	Differential linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
	Gray scale error				5%	
	Output current (see Note 2)	White level relative to blank	17.69	19.05	20.4	mA
		White level relative to black (7.5 IRE only)	16.74	17.62	18.5	mA
		Black level relative to blank (7.5 IRE only)	0.95	1.44	1.9	mA
		Blank level on IOR, IOB	0	5	50	µA
		Blank level on IOG (with SYNC enabled)	6.29	7.6	8.96	mA
		Sync level on IOG (with SYNC enabled)	0	5	50	µA
		One LSB (8/$\overline{6}$ high)		69.1		µA
		One LSB (8/$\overline{6}$ low)		276.4		µA
	DAC-to-DAC matching			2%	5%	
	DAC-to-DAC crosstalk			–20		dB
	Output compliance		–1		1.2	V
	Voltage reference output voltage		1.15	1.235	1.26	V
	Output impedance			50		kΩ
	Output capacitance	f = 1 MHz, I_{OUT} = 0		13		pF
	Sense voltage reference		300	350	400	mV
	Clock and data feedthrough			–20		dB
	Glitch area (see Note 3)			50		pV–s
	Pipeline delay, VGA port			18		DOTCLK periods
	Pipeline delay, pixel port (see Note 4)			18		DOTCLK periods
	Pixel clock PLL, MCLK PLL	Lock time		5		ms
		Jitter		±200		ps

NOTES: 2. Test conditions for RS343-A video signals (unless otherwise specified), see Section 3.2, *Recommended Operating Conditions*, using external voltage reference V_{ref} = 1.235 V, R_{SET} = 523 Ω. When using the internal voltage reference, R_{SET} may need to be adjusted in order to meet these limits.

3. Glitch area does not include clock and data feedthrough. The – 3-dB test bandwidth is twice the clock rate.

4. Pipeline delay from pixel port depends on Latch Control Register setting. Value shown is for LCR = 0x06.

3.5 Timing Requirements (see Note 5 and Figures 3-1 and 3-2)

			TVP3026 -135		TVP3026 -175		TVP3026 -220		TVP3026 -250		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	DOTCLK frequency			135		175		220		250	MHz
	Pixel clock PLL	Internal frequency		135		175		220		250	MHz
		PCLKOUT frequency		110		110		110		110	MHz
	MCLK PLL frequency			100		100		100		100	MHz
	VCO frequency, pixel clock PLL, MCLK PLL, and loop clock PLL		110	220	110	220	110	220	110	250	MHz
	CLK0 frequency for VGA mode 2			85		85		85		85	MHz
t_{cyc}	Clock cycle time	TTL	7.4		7.1		7.1		7.1		ns
		ECL	7.4		5.7		4.5		4		
t_{d4}	Delay time, RCLK to LCLK (see Note 6)			0.5		0.5		0.5	0.5		RCLK periods
t_{su1}	Setup time, RS(3–0) valid before $\overline{RD}$ or $\overline{WR}\downarrow$		10		10		10		10		ns
t_{h1}	Hold time, RS(3–0) valid after $\overline{RD}$ or $\overline{WR}\downarrow$		10		10		10		10		ns
t_{su2}	Setup time, D(7–0) valid before $\overline{WR}\uparrow$		35		35		35		35		ns
t_{h2}	Hold time, D(7–0) valid after $\overline{WR}\uparrow$		0		0		0		0		ns
t_{su3}	Setup time, VGA(7–0) and $\overline{VGAHS}$, $\overline{VGAVS}$, and $\overline{VGABL}$ valid before CLK0$\uparrow$		2		2		2		2		ns
t_{h3}	Hold time, VGA(7–0) and $\overline{VGAHS}$, $\overline{VGAVS}$, and $\overline{VGABL}$ valid after CLK0$\uparrow$		2		2		2		2		ns
t_{su4}	Setup time, P(63–0), and PSEL valid before LCLK$\uparrow$		2		2		2		2		ns
t_{h4}	Hold time, P(63–0), and PSEL valid after LCLK$\uparrow$		1		1		1		1		ns
t_{su5}	Setup time, $\overline{SYSHS}$, $\overline{SYSVS}$, and OVS valid before LCLK$\uparrow$		2		2		2		2		ns
t_{h5}	Hold time, $\overline{SYSHS}$, $\overline{SYSVS}$, and OVS valid after LCLK$\uparrow$		1		1		1		1		ns

NOTES: 5. TTL input signals are 0 to 3 V with less than 3 ns rise/fall time between the 10% and 90% levels unless otherwise specified. ECL input signals are V_{DD}–1.8 V to V_{DD}–0.8 V with less than 2 ns rise/fall time between the 20% and 80% levels. For input and output signals, timing reference points are at the 10% and 90% signal levels. Analog output loads are less than 10 pF. D7–D0 output loads are less than 50 pF. All other output loads are less than 50 pF unless otherwise specified.

6. This parameter only applies when SCLK is used as the VRAM shift clock. When SCLK is not used, the delay may be as much as is required by system logic (assuming the loop clock PLL compensates for the system delay).

3.5 Timing Requirements (see Note 5 and Figures 3-1 and 3-2) (continued)

			TVP3026 -135		TVP3026 -175		TVP3026 -220		TVP3026 -250		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{su6}	Setup time, $\overline{\text{SYSBL}}$ valid before LCLK↑		3		3		3		3		ns
t_{h6}	Hold time, $\overline{\text{SYSBL}}$ valid after LCLK↑		2		2		2		2		ns
t_{w1}	Pulse duration, $\overline{\text{RD}}$ or $\overline{\text{WR}}$ low		50		50		50		50		ns
t_{w2}	Pulse duration, $\overline{\text{RD}}$ or $\overline{\text{WR}}$ high		30		30		30		30		ns
t_{w3}	Pulse duration, clock high	TTL	3		3		2		2		ns
		ECL	3		2.5		2		2		
t_{w4}	Pulse duration, clock low	TTL	3		3		2		2		ns
		ECL	3		2.5		2		2		

NOTE 5. TTL input signals are 0 to 3 V with less than 3 ns rise/fall time between the 10% and 90% levels unless otherwise specified. ECL input signals are V_{DD} – 1.8 V to V_{DD} – 0.8 V with less than 2 ns rise/fall time between the 20% and 80% levels. For input and output signals, timing reference points are at the 10% and 90% signal levels. Analog output loads are less than 10 pF. D7 – D0 output loads are less than 50 pF. All other output loads are less than 50 pF unless otherwise specified.

3.6 Switching Characteristics (See Figures 3-1 and 3-2)

PARAMETER		TVP3026-135			TVP3026-175			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	SCLK/RCLK frequency (see Note 7)			85			85	MHz
	VCLK frequency (see Note 7)			85			85	MHz
t_{en1}	Enable time, $\overline{RD}$ low to D(7–0) valid			40			40	ns
t_{dis1}	Disable time, $\overline{RD}$ high to D(7–0) disabled			17			17	ns
t_{v1}	Valid time, D(7–0) valid after $\overline{RD}$ high	5			5			ns
t_{d1}	Delay time, $\overline{RD}$ low to D(7–0) starting to turn on	5			5			ns
t_{d2}	Delay time, selected input clock high/low to DOTCLK (internal signal) high/low		7			7		ns
t_{d3}	Delay time, SCLK high/low to RCLK high/low (see Notes 8, 9, and 10)	1	2	4	1	2	4	ns
t_{d6}	Analog output settling time (see Note 11)		6			5		ns
t_r	Analog output rise time (see Note 12)		2			2		ns
	Analog output skew	0		2	0		2	ns

NOTES: 7. SCLK can drive an output capacitive load up to 60 pF. The worst-case transition time between the 10% and 90% levels is less than 4 ns (typically 3 ns). RCLK and VCLK can drive output capacitive loads up to 15 pF, with worst-case transition times between 10% and 90% levels less than 4 ns (typically 3 ns).

8. The SCLK delay time to RCLK depends on the load that the signals drive. This parameter is measured with a VCLK = RCLK load of 15 pF and SCLK load of 60 pF.
9. In SCLK mode, RCLK is delayed from SCLK so that when RCLK is connected to LCLK, the timing is essentially the same as the TLC3407x family of parts.
10. This parameter applies when SCLK is used.
11. Measured within ± 1 LSB from 50% point of full-scale transition to output settling, (settling time does not include clock and data feedthrough).
12. Measured between 10% and 90% of full-scale transition.

3.6 Switching Characteristics (See Figures 3-1 and 3-2) (continued)

PARAMETER		TVP3026-220			TVP3026-250			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	SCLK/RCLK frequency (see Note 7)			85			85	MHz
	VCLK frequency (see Note 7)			85			85	MHz
t_{en1}	Enable time, $\overline{RD}$ low to D(7–0) valid			40			40	ns
t_{dis1}	Disable time, $\overline{RD}$ high to D(7–0) disabled			17			17	ns
t_{v1}	Valid time, D(7–0) valid after $\overline{RD}$ high	5			5			ns
t_{d1}	Delay time, $\overline{RD}$ low to D(7–0) starting to turn on	5			5			ns
t_{d2}	Delay time, selected input clock high/low to DOTCLK (internal signal) high/low		7			7		ns
t_{d3}	Delay time, SCLK high/low to RCLK high/low (see Notes 8, 9, and 10)	1	2	4	1	2	4	ns
t_{d6}	Analog output settling time (see Note 11)		5			5		ns
t_r	Analog output rise time (see Note 12)		2			2		ns
	Analog output skew	0		2	0		2	ns

NOTES: 7. SCLK can drive an output capacitive load up to 60 pF. The worst-case transition time between the 10% and 90% levels is less than 4 ns (typically 3 ns). RCLK and VCLK can drive output capacitive loads up to 15 pF, with worst-case transition times between 10% and 90% levels less than 4 ns (typically 3 ns).

8. The SCLK delay time to RCLK depends on the load that the signals drive. This parameter is measured with a VCLK = RCLK load of 15 pF and SCLK load of 60 pF.
9. In SCLK mode, RCLK is delayed from SCLK so that when RCLK is connected to LCLK, the timing is essentially the same as the TLC3407x family of parts.
10. This parameter applies when SCLK is used.
11. Measured within ± 1 LSB from 50% point of full-scale transition to output settling, (settling time does not include clock and data feedthrough).
12. Measured between 10% and 90% of full-scale transition.

3.7 Timing and Switching Diagrams

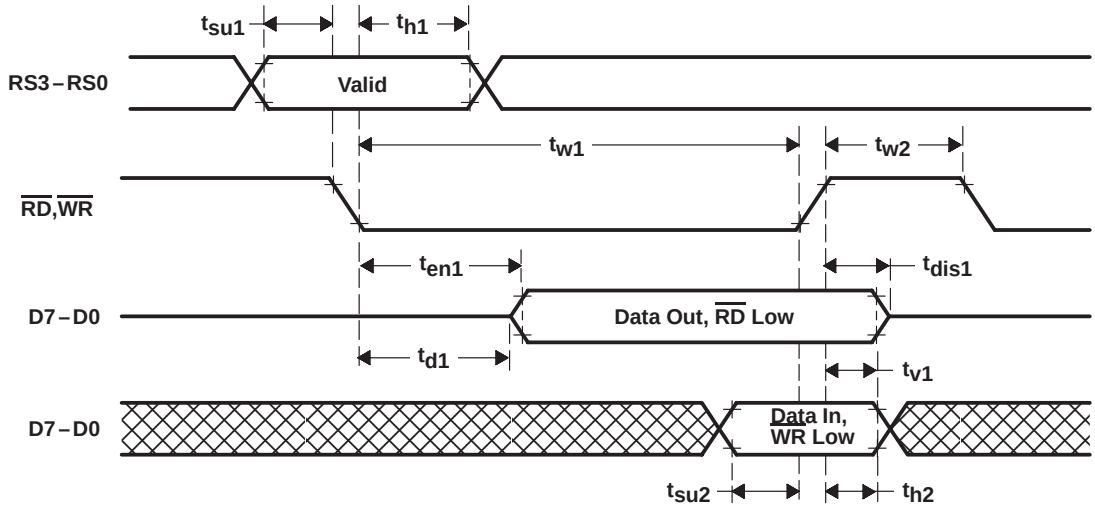


Figure 3–1. MPU Interface Timing and Switching Waveforms

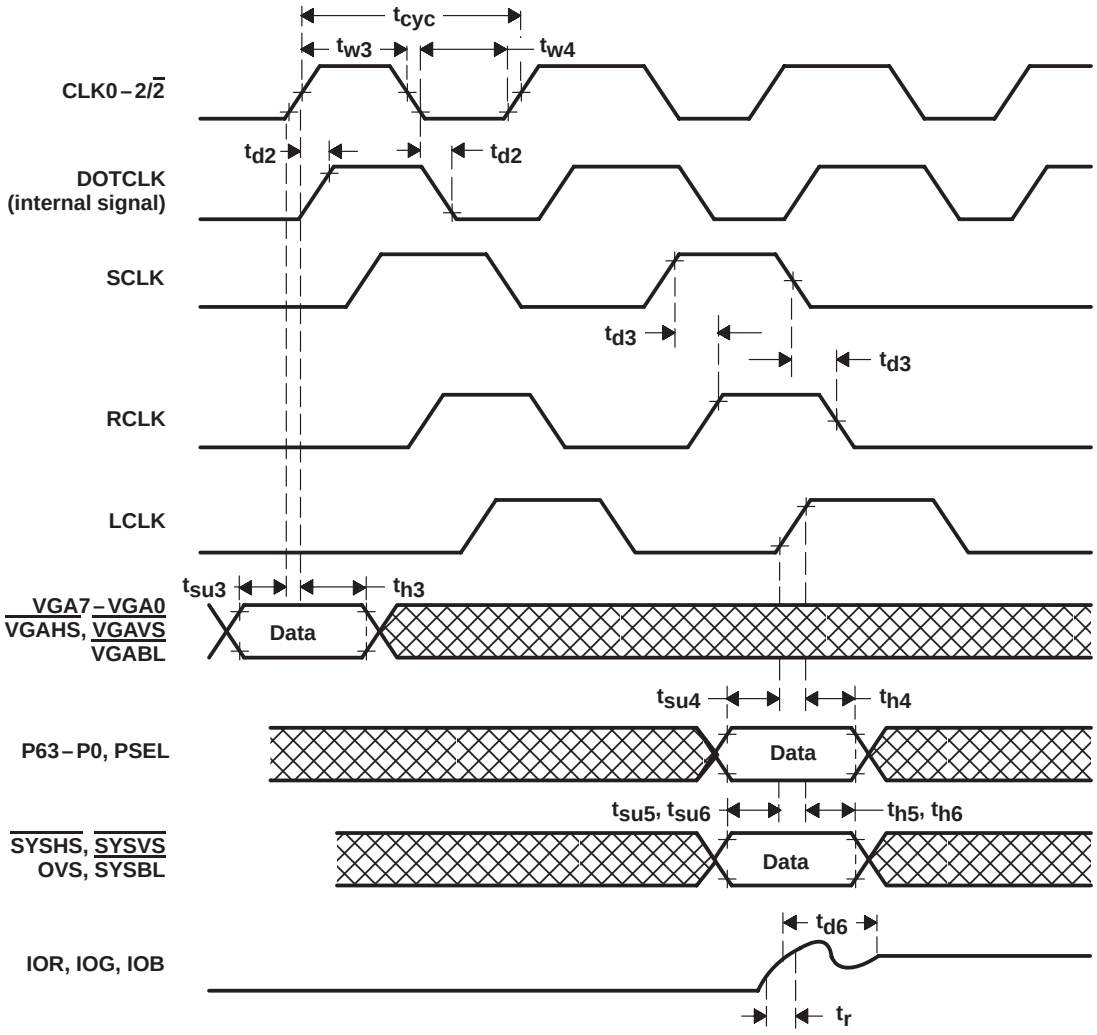


Figure 3–2. Video Input/Output Timing and Switching Waveforms

Appendix A
Frequency Synthesis PLL Register Settings

Table A–1 provides a listing of all possible frequency settings that may be used by the pixel clock PLL for frequency synthesis using the common 14.31818 MHz crystal. The same register settings may be used for the MCLK PLL provided that the MCLK maximum frequency of 100 MHz is not exceeded. The constraints used to generate the table include limits for the VCO frequency and limits for the N-register value.

PLL Architecture — TVP3026
Reference Frequency (MHz) — 14.318180
Minimum VCO Frequency (MHz) — 110.000000
Maximum VCO Frequency (MHz) — 250.000000
Minimum N-Register Value (dec) — 40
Maximum N-Register Value (dec) — 62

Table A–1. PLL Register Settings for 14.31818 MHz Reference

OUTPUT	VCO	NREG	MREG	PREG
14.32	114.55	FE	3E	B3
14.89	119.13	E8	27	B3
14.91	119.32	E9	28	B3
14.94	119.53	EA	29	B3
14.97	119.75	EB	2A	B3
15.00	120.00	EC	2B	B3
15.03	120.27	ED	2C	B3
15.07	120.57	EE	2D	B3
15.11	120.91	EF	2E	B3
15.16	121.28	F0	2F	B3
15.21	121.70	F1	30	B3
15.27	122.18	F2	31	B3
15.34	122.73	F3	32	B3
15.42	123.36	F4	33	B3
15.46	123.71	E8	26	B3
15.51	124.09	F5	34	B3
15.56	124.51	EA	28	B3
15.62	124.96	F6	35	B3
15.68	125.45	EC	2A	B3
15.75	126.00	F7	36	B3
15.83	126.60	EE	2C	B3
15.91	127.27	F8	37	B3
16.00	128.02	F0	2E	B3

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
16.04	128.29	E8	25	B3
16.11	128.86	F9	38	B3
16.19	129.49	EA	27	B3
16.23	129.82	F2	30	B3
16.27	130.17	FB	28	B3
16.36	130.91	FA	39	B3
16.47	131.73	FD	2A	B3
16.52	132.17	F4	32	B3
16.58	132.63	FE	2B	B3
16.61	132.87	E8	24	B3
16.70	133.64	FB	3A	B3
16.81	134.47	EA	26	B3
16.84	134.76	F0	2D	B3
16.92	135.37	F6	34	B3
17.00	136.02	E1	2E	B3
17.05	136.36	FC	28	B3
17.18	137.45	FC	3B	B3
17.30	138.41	E9	24	B3
17.33	138.66	EE	2A	B3
17.39	139.09	F3	30	B3
17.43	139.45	EA	25	B3
17.50	140.00	F8	36	B3
17.57	140.58	EB	26	B3
17.62	140.98	F4	31	B3
17.69	141.50	F0	2C	B3
17.73	141.82	EC	27	B3
17.75	142.04	E8	22	B3
17.90	143.18	FD	3C	B3
18.05	144.43	EA	24	B3
18.09	144.69	EE	29	B3
18.14	145.09	F2	2E	B3
18.22	145.79	F6	33	B3
18.30	146.36	EF	2A	B3
18.33	146.62	E8	21	B3
18.41	147.27	FA	38	B3
18.49	147.95	E9	22	B3
18.53	148.24	F0	2B	B3
18.61	148.91	F7	34	B3

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
18.68	149.41	EA	23	B3
18.72	149.79	F4	30	B3
18.79	150.34	F1	2C	B3
18.84	150.72	EE	28	B3
18.87	150.99	EB	24	B3
18.90	151.20	E8	20	B3
19.09	152.73	FE	3D	B3
19.30	154.39	EA	22	B3
19.33	154.64	ED	26	B3
19.37	154.97	F0	2A	B3
19.43	155.45	F3	2E	B3
19.47	155.78	E8	1F	B3
19.52	156.20	F6	32	B3
19.59	156.75	EE	27	B3
19.69	157.50	F9	36	B3
19.77	158.18	EC	24	B3
19.83	158.60	F4	2F	B3
19.89	159.09	EF	28	B3
19.92	159.37	EA	21	B3
20.05	160.36	FC	3A	B3
20.18	161.40	EB	22	B3
20.21	161.71	F0	29	B3
20.28	162.27	F5	30	B3
20.35	162.78	EE	26	B3
20.45	163.64	FA	37	B3
20.54	164.35	EA	20	B3
20.58	164.66	F1	2A	B3
20.62	164.95	E8	1D	B3
20.68	165.45	F8	34	B3
20.76	166.09	ED	24	B3
20.83	166.61	F6	31	B3
20.88	167.05	E9	1E	B3
20.93	167.41	F4	2E	B3
21.00	168.00	F2	2B	B3
21.06	168.45	F0	28	B3
21.10	168.80	EE	25	B3
21.14	169.09	EC	22	B3
21.17	169.33	EA	1F	B3
21.19	169.53	E8	1C	B3

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
21.48	171.82	BD	3B	B3
21.76	174.11	E8	1B	B3
21.79	174.31	EA	1E	B3
21.82	174.55	EC	21	B3
21.85	174.83	EE	24	B3
21.90	175.19	F0	27	B3
21.95	175.64	F2	2A	B3
22.03	176.22	F4	2D	B3
22.07	176.59	E9	1C	B3
22.13	177.02	F6	30	B3
22.19	177.55	ED	22	B3
22.27	178.18	F8	33	B3
22.34	178.69	E8	1A	B3
22.37	178.98	F1	28	B3
22.41	179.29	EA	1D	B3
22.50	180.00	FA	36	B3
22.61	180.86	EE	23	B3
22.67	181.36	F5	2E	B3
22.74	181.93	F0	26	B3
22.78	182.23	EB	1E	B3
22.91	183.27	FC	39	B3
23.03	184.27	EA	1C	B3
23.07	184.55	EF	24	B3
23.13	185.03	F4	2C	B3
23.18	185.45	EC	1F	B3
23.27	186.14	F9	34	B3
23.36	186.89	EE	22	B3
23.43	187.44	F6	2F	B3
23.48	187.85	E8	18	B3
23.52	188.18	F3	2A	B3
23.58	188.66	B0	25	B3
23.62	189.00	ED	20	B3
23.66	189.25	EA	1B	B3
23.86	190.91	FE	3C	B3
24.05	192.44	E8	17	B3
24.08	192.64	EB	1C	B3
24.11	192.92	EE	21	B3
24.16	193.30	F1	26	B3
24.23	193.85	F4	2B	B3

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
24.28	194.23	EA	1A	B3
24.34	194.73	F7	30	B3
24.43	195.40	F0	24	B3
24.46	195.68	E9	18	B3
24.55	196.36	FA	35	B3
24.63	197.02	E8	16	B3
24.66	197.27	EF	22	B3
24.73	197.85	F6	2E	B3
24.82	198.55	F2	27	B3
24.87	198.95	EE	20	B3
24.90	199.21	EA	19	B3
25.06	200.45	FD	3A	B3
25.20	201.60	E8	15	B3
25.23	201.82	EC	1C	B3
25.27	202.14	F0	23	B3
25.33	202.66	F4	2A	B3
25.38	203.06	EB	1A	B3
25.45	203.64	B8	31	B3
25.52	204.19	EA	18	B3
25.57	204.55	F3	28	B3
25.62	204.98	EE	1F	B3
25.65	205.23	A9	16	B3
25.77	206.18	BC	38	B3
25.91	207.27	EC	1B	B3
25.95	207.61	F1	24	B3
26.03	208.26	F6	2D	B3
26.11	208.88	F0	22	B3
26.15	209.17	EA	17	B3
26.25	210.00	FB	36	B3
26.35	210.76	E8	13	B3
26.38	211.00	EE	1E	B3
26.43	211.47	F4	29	B3
26.49	211.91	ED	1C	B3
26.59	212.73	BA	34	B3
26.68	213.47	EB	18	B3
26.73	213.82	F2	25	B3
26.77	214.15	EA	16	B3
26.85	214.77	F9	32	B3
26.92	215.35	E8	12	B3
26.95	215.61	F0	21	B3

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
27.05	216.36	F8	30	B3
27.13	217.03	EE	1D	B3
27.20	217.64	F7	2E	B3
27.27	218.18	EC	19	B3
27.33	218.68	F6	2C	B3
27.39	219.13	EA	15	B3
27.44	219.55	F5	2A	B3
27.49	219.93	E8	11	B3
28.64	114.55	FE	3E	B2
29.78	119.13	E8	27	B2
29.83	119.32	E9	28	B2
29.88	119.53	EA	29	B2
29.94	119.75	EB	2A	B2
30.00	120.00	EC	2B	B2
30.07	120.27	ED	2C	B2
30.14	120.57	EE	2D	B2
30.23	120.91	EF	2E	B2
30.32	121.28	F0	2F	B2
30.43	121.70	F1	30	B2
30.55	122.18	F2	31	B2
30.68	122.73	F3	32	B2
30.84	123.36	F4	33	B2
30.93	123.71	E8	26	B2
31.02	124.09	F5	34	B2
31.13	124.51	EA	28	B2
31.24	124.96	F6	35	B2
31.36	125.45	EC	2A	B2
31.50	126.00	F7	36	B2
31.65	126.60	EE	2C	B2
31.82	127.27	F8	37	B2
32.01	128.02	F0	2E	B2
32.07	128.29	E8	25	B2
32.22	128.86	F9	38	B2
32.37	129.49	EA	27	B2
32.45	129.82	F2	30	B2
32.54	130.17	EB	28	B2
32.73	130.91	FA	39	B2
32.93	131.73	ED	2A	B2
33.04	132.17	F4	32	B2
33.16	132.63	EE	2B	B2

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
33.22	132.87	E8	24	B2
33.41	133.64	FB	3A	B2
33.62	134.47	EA	26	B2
33.69	134.76	F0	2D	B2
33.84	135.37	F6	34	B2
34.01	136.02	F1	2E	B2
34.09	136.36	EC	28	B2
34.36	137.45	FC	3B	B2
34.60	138.41	E9	24	B2
34.67	138.66	EE	2A	B2
34.77	139.09	F3	30	B2
34.86	139.45	EA	25	B2
35.00	140.00	F8	36	B2
35.14	140.58	EB	26	B2
35.24	140.98	F4	31	B2
35.37	141.50	F0	2C	B2
35.45	141.82	EC	27	B2
35.51	142.04	E8	22	B2
35.80	143.18	FD	3C	B2
36.11	144.43	EA	24	B2
36.17	144.69	EE	29	B2
36.27	145.09	F2	2E	B2
36.45	145.79	F6	33	B2
36.59	146.36	EF	2A	B2
36.65	146.62	E8	21	B2
36.82	147.27	FA	38	B2
36.99	147.95	E9	22	B2
37.06	148.24	F0	2B	B2
37.23	148.91	F7	34	B2
37.35	149.41	EA	23	B2
37.45	149.79	F4	30	B2
37.59	150.34	F1	2C	B2
37.68	150.72	EE	28	B2
37.75	150.99	EB	24	B2
37.80	151.20	E8	20	B2
38.18	152.73	FE	3D	B2
38.60	154.39	EA	22	B2
38.66	154.64	ED	26	B2
38.74	154.97	F0	2A	B2
38.86	155.45	F3	2E	B2

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
38.95	155.78	E8	1F	B2
39.05	156.20	F6	32	B2
39.19	156.75	EE	27	B2
39.37	157.50	F9	36	B2
39.55	158.18	EC	24	B2
39.65	158.60	F4	2F	B2
39.77	159.09	EF	28	B2
39.84	159.37	EA	21	B2
40.09	160.36	FC	3A	B2
40.35	161.40	EB	22	B2
40.43	161.71	F0	29	B2
40.57	162.27	F5	30	B2
40.69	162.78	EE	26	B2
40.91	163.64	FA	37	B2
41.09	164.35	EA	20	B2
41.16	164.66	F1	2A	B2
41.24	164.95	E8	1D	B2
41.36	165.45	F8	34	B2
41.52	166.09	ED	24	B2
41.65	166.61	F6	31	B2
41.76	167.05	E9	1E	B2
41.85	167.41	F4	2E	B2
42.00	168.00	F2	2B	B2
42.11	168.45	F0	28	B2
42.20	168.80	EE	25	B2
42.27	169.09	EC	22	B2
42.33	169.33	EA	1F	B2
42.38	169.53	E8	1C	B2
42.95	171.82	FD	3B	B2
43.53	174.11	E8	1B	B2
43.58	174.31	EA	1E	B2
43.64	174.55	EC	21	B2
43.71	174.83	EE	24	B2
43.80	175.19	F0	27	B2
43.91	175.64	F2	2A	B2
44.06	176.22	F4	2D	B2
44.15	176.59	E9	1C	B2
44.26	177.02	F6	30	B2
44.39	177.55	ED	22	B2
44.55	178.18	F8	33	B2

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
44.67	178.69	E8	1A	B2
44.74	178.98	F1	28	B2
44.82	179.29	EA	1D	B2
45.00	180.00	FA	36	B2
45.22	180.86	EE	23	B2
45.34	181.36	F5	2E	B2
45.48	181.93	F0	26	B2
45.56	182.23	EB	1E	B2
45.82	183.27	FC	39	B2
46.07	184.27	EA	1C	B2
46.14	184.55	EF	24	B2
46.26	185.03	F4	2C	B2
46.36	185.45	EC	1F	B2
46.53	186.14	F9	34	B2
46.72	186.89	EE	22	B2
46.86	187.44	F6	2F	B2
46.96	187.85	E8	18	B2
47.05	188.18	F3	2A	B2
47.17	188.66	F0	25	B2
47.25	189.00	ED	20	B2
47.31	189.25	EA	1B	B2
47.73	190.91	FE	3C	B2
48.11	192.44	E8	17	B2
48.16	192.64	EB	1C	B2
48.23	192.92	EE	21	B2
48.32	193.30	F1	26	B2
48.46	193.85	F4	2B	B2
48.56	194.23	EA	1A	B2
48.68	194.73	F7	30	B2
48.85	195.40	F0	24	B2
48.92	195.68	E9	18	B2
49.09	196.36	FA	35	B2
49.25	197.02	E8	16	B2
49.32	197.27	EF	22	B2
49.46	197.85	F6	2E	B2
49.64	198.55	F2	27	B2
49.74	198.95	EE	20	B2
49.80	199.21	EA	19	B2
50.11	200.45	FD	3A	B2
50.40	201.60	E8	15	B2

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
50.45	201.82	EC	1C	B2
50.53	202.14	F0	23	B2
50.66	202.66	F4	2A	B2
50.76	203.06	EB	1A	B2
50.91	203.64	F8	31	B2
51.05	204.19	EA	18	B2
51.14	204.55	F3	28	B2
51.24	204.98	EE	1F	B2
51.31	205.23	E9	16	B2
51.55	206.18	FC	38	B2
51.82	207.27	EC	1B	B2
51.90	207.61	F1	24	B2
52.07	208.26	F6	2D	B2
52.22	208.88	F0	22	B2
52.29	209.17	EA	17	B2
52.50	210.00	FB	36	B2
52.69	210.76	E8	13	B2
52.75	211.00	EE	1E	B2
52.87	211.47	F4	29	B2
52.98	211.91	ED	1C	B2
53.18	212.73	FA	34	B2
53.37	213.47	EB	18	B2
53.45	213.82	F2	25	B2
53.54	214.15	EA	16	B2
53.69	214.77	F9	32	B2
53.84	215.35	E8	12	B2
53.90	215.61	F0	21	B2
54.09	216.36	F8	30	B2
54.26	217.03	EE	1D	B2
54.41	217.64	F7	2E	B2
54.55	218.18	EC	19	B2
54.67	218.68	F6	2C	B2
54.78	219.13	EA	15	B2
54.89	219.55	F5	2A	B2
54.98	219.93	E8	11	B2
57.27	114.55	FE	3E	B1
59.56	119.13	E8	27	B1
59.66	119.32	E9	28	B1
59.76	119.53	EA	29	B1
59.88	119.75	EB	2A	B1

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
60.00	120.00	EC	2B	B1
60.14	120.27	ED	2C	B1
60.29	120.57	EE	2D	B1
60.45	120.91	EF	2E	B1
60.64	121.28	F0	2F	B1
60.85	121.70	F1	30	B1
61.09	122.18	F2	31	B1
61.36	122.73	F3	32	B1
61.68	123.36	F4	33	B1
61.85	123.71	E8	26	B1
62.05	124.09	F5	34	B1
62.25	124.51	EA	28	B1
62.48	124.96	F6	35	B1
62.73	125.45	EC	2A	B1
63.00	126.00	F7	36	B1
63.30	126.60	EE	2C	B1
63.64	127.27	F8	37	B1
64.01	128.02	F0	2E	B1
64.15	128.29	E8	25	B1
64.43	128.86	F9	38	B1
64.74	129.49	EA	27	B1
64.91	129.82	F2	30	B1
65.08	130.17	EB	28	B1
65.45	130.91	FA	39	B1
65.86	131.73	ED	2A	B1
66.08	132.17	F4	32	B1
66.32	132.63	EE	2B	B1
66.44	132.87	E8	24	B1
66.82	133.64	FB	3A	B1
67.23	134.47	EA	26	B1
67.38	134.76	F0	2D	B1
67.69	135.37	F6	34	B1
68.01	136.02	F1	2E	B1
68.18	136.36	EC	28	B1
68.73	137.45	FC	3B	B1
69.20	138.41	E9	24	B1
69.33	138.66	EE	2A	B1
69.55	139.09	F3	30	B1
69.72	139.45	EA	25	B1
70.00	140.00	F8	36	B1

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
70.29	140.58	EB	26	B1
70.49	140.98	F4	31	B1
70.75	141.50	F0	2C	B1
70.91	141.82	EC	27	B1
71.02	142.04	E8	22	B1
71.59	143.18	FD	3C	B1
72.21	144.43	EA	24	B1
72.34	144.69	EE	29	B1
72.55	145.09	F2	2E	B1
72.89	145.79	F6	33	B1
73.18	146.36	EF	2A	B1
73.31	146.62	E8	21	B1
73.64	147.27	FA	38	B1
73.98	147.95	E9	22	B1
74.12	148.24	F0	2B	B1
74.45	148.91	F7	34	B1
74.70	149.41	EA	23	B1
74.90	149.79	F4	30	B1
75.17	150.34	F1	2C	B1
75.36	150.72	EE	28	B1
75.50	150.99	EB	24	B1
75.60	151.20	E8	20	B1
76.36	152.73	FE	3D	B1
77.19	154.39	EA	22	B1
77.32	154.64	ED	26	B1
77.49	154.97	F0	2A	B1
77.73	155.45	F3	2E	B1
77.89	155.78	E8	1F	B1
78.10	156.20	F6	32	B1
78.37	156.75	EE	27	B1
78.75	157.50	F9	36	B1
79.09	158.18	EC	24	B1
79.30	158.60	F4	2F	B1
79.55	159.09	EF	28	B1
79.68	159.37	EA	21	B1
80.18	160.36	FC	3A	B1
80.70	161.40	EB	22	B1
80.86	161.71	F0	29	B1
81.14	162.27	F5	30	B1
81.39	162.78	EE	26	B1

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
81.82	163.64	FA	37	B1
82.17	164.35	EA	20	B1
82.33	164.66	F1	2A	B1
82.47	164.95	E8	1D	B1
82.73	165.45	F8	34	B1
83.05	166.09	ED	24	B1
83.31	166.61	F6	31	B1
83.52	167.05	E9	1E	B1
83.71	167.41	F4	2E	B1
84.00	168.00	F2	2B	B1
84.22	168.45	F0	28	B1
84.40	168.80	EE	25	B1
84.55	169.09	EC	22	B1
84.66	169.33	EA	1F	B1
84.76	169.53	E8	1C	B1
85.91	171.82	FD	3B	B1
87.05	174.11	E8	1B	B1
87.15	174.31	EA	1E	B1
87.27	174.55	EC	21	B1
87.42	174.83	EE	24	B1
87.59	175.19	F0	27	B1
87.82	175.64	F2	2A	B1
88.11	176.22	F4	2D	B1
88.30	176.59	E9	1C	B1
88.51	177.02	F6	30	B1
88.77	177.55	ED	22	B1
89.09	178.18	F8	33	B1
89.35	178.69	E8	1A	B1
89.49	178.98	F1	28	B1
89.64	179.29	EA	1D	B1
90.00	180.00	FA	36	B1
90.43	180.86	EE	23	B1
90.68	181.36	F5	2E	B1
90.96	181.93	F0	26	B1
91.12	182.23	EB	1E	B1
91.64	183.27	FC	39	B1
92.13	184.27	EA	1C	B1
92.27	184.55	EF	24	B1
92.52	185.03	F4	2C	B1
92.73	185.45	EC	1F	B1

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
93.07	186.14	F9	34	B1
93.44	186.89	EE	22	B1
93.72	187.44	F6	2F	B1
93.93	187.85	E8	18	B1
94.09	188.18	F3	2A	B1
94.33	188.66	F0	25	B1
94.50	189.00	ED	20	B1
94.62	189.25	EA	1B	B1
95.45	190.91	FE	3C	B1
96.22	192.44	E8	17	B1
96.32	192.64	EB	1C	B1
96.46	192.92	EE	21	B1
96.65	193.30	F1	26	B1
96.92	193.85	F4	2B	B1
97.11	194.23	EA	1A	B1
97.36	194.73	F7	30	B1
97.70	195.40	F0	24	B1
97.84	195.68	E9	18	B1
98.18	196.36	FA	35	B1
98.51	197.02	E8	16	B1
98.64	197.27	EF	22	B1
98.93	197.85	F6	2E	B1
99.27	198.55	F2	27	B1
99.47	198.95	EE	20	B1
99.60	199.21	EA	19	B1
100.23	200.45	FD	3A	B1
100.80	201.60	E8	15	B1
100.91	201.82	EC	1C	B1
101.07	202.14	F0	23	B1
101.33	202.66	F4	2A	B1
101.53	203.06	EB	1A	B1
101.82	203.64	F8	31	B1
102.09	204.19	EA	18	B1
102.27	204.55	F3	28	B1
102.49	204.98	EE	1F	B1
102.61	205.23	E9	16	B1
103.09	206.18	FC	38	B1
103.64	207.27	EC	1B	B1
103.81	207.61	F1	24	B1
104.13	208.26	F6	2D	B1

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
104.44	208.88	F0	22	B1
104.58	209.17	EA	17	B1
105.00	210.00	FB	36	B1
105.38	210.76	E8	13	B1
105.50	211.00	EE	1E	B1
105.73	211.47	F4	29	B1
105.95	211.91	ED	1C	B1
106.36	212.73	FA	34	B1
106.74	213.47	EB	18	B1
106.91	213.82	F2	25	B1
107.08	214.15	EA	16	B1
107.39	214.77	F9	32	B1
107.67	215.35	E8	12	B1
107.81	215.61	F0	21	B1
108.18	216.36	F8	30	B1
108.52	217.03	EE	1D	B1
108.82	217.64	F7	2E	B1
109.09	218.18	EC	19	B1
109.34	218.68	F6	2C	B1
109.57	219.13	EA	15	B1
109.77	219.55	F5	2A	B1
109.96	219.93	E8	11	B1
114.55	114.55	FE	3E	B0
119.13	119.13	E8	27	B0
119.32	119.32	E9	28	B0
119.53	119.53	EA	29	B0
119.75	119.75	EB	2A	B0
120.00	120.00	EC	2B	B0
120.27	120.27	ED	2C	B0
120.57	120.57	EE	2D	B0
120.91	120.91	EF	2E	B0
121.28	121.28	F0	2F	B0
121.70	121.70	F1	30	B0
122.18	122.18	F2	31	B0
122.73	122.73	F3	32	B0
123.36	123.36	F4	33	B0
123.71	123.71	E8	26	B0
124.09	124.09	F5	34	B0
124.51	124.51	EA	28	B0
124.96	124.96	F6	35	B0

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
125.45	125.45	EC	2A	B0
126.00	126.00	F7	36	B0
126.60	126.60	EE	2C	B0
127.27	127.27	F8	37	B0
128.02	128.02	F0	2E	B0
128.29	128.29	E8	25	B0
128.86	128.86	F9	38	B0
129.49	129.49	EA	27	B0
129.82	129.82	F2	30	B0
130.17	130.17	EB	28	B0
130.91	130.91	FA	39	B0
131.73	131.73	ED	2A	B0
132.17	132.17	F4	32	B0
132.63	132.63	EE	2B	B0
132.87	132.87	E8	24	B0
133.64	133.64	FB	3A	B0
134.47	134.47	EA	26	B0
134.76	134.76	F0	2D	B0
135.37	135.37	F6	34	B0
136.02	136.02	F1	2E	B0
136.36	136.36	EC	28	B0
137.45	137.45	FC	3B	B0
138.41	138.41	E9	24	B0
138.66	138.66	EE	2A	B0
139.09	139.09	F3	30	B0
139.45	139.45	EA	25	B0
140.00	140.00	F8	36	B0
140.58	140.58	EB	26	B0
140.98	140.98	F4	31	B0
141.50	141.50	F0	2C	B0
141.82	141.82	EC	27	B0
142.04	142.04	E8	22	B0
143.18	143.18	FD	3C	B0
144.43	144.43	EA	24	B0
144.69	144.69	EE	29	B0
145.09	145.09	F2	2E	B0
145.79	145.79	F6	33	B0
146.36	146.36	EF	2A	B0
146.62	146.62	E8	21	B0

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
147.27	147.27	FA	38	B0
147.95	147.95	E9	22	B0
148.24	148.24	F0	2B	B0
148.91	148.91	F7	34	B0
149.41	149.41	EA	23	B0
149.79	149.79	F4	30	B0
150.34	150.34	F1	2C	B0
150.72	150.72	EE	28	B0
150.99	150.99	EB	24	B0
151.20	151.20	E8	20	B0
152.73	152.73	FE	3D	B0
154.39	154.39	EA	22	B0
154.64	154.64	ED	26	B0
154.97	154.97	F0	2A	B0
155.45	155.45	F3	2E	B0
155.78	155.78	E8	1F	B0
156.20	156.20	F6	32	B0
156.75	156.75	EE	27	B0
157.50	157.50	F9	36	B0
158.18	158.18	EC	24	B0
158.60	158.60	F4	2F	B0
159.09	159.09	EF	28	B0
159.37	159.37	EA	21	B0
160.36	160.36	FC	3A	B0
161.40	161.40	EB	22	B0
161.71	161.71	F0	29	B0
162.27	162.27	F5	30	B0
162.78	162.78	EE	26	B0
163.64	163.64	FA	37	B0
164.35	164.35	EA	20	B0
164.66	164.66	F1	2A	B0
164.95	164.95	E8	1D	B0
165.45	165.45	F8	34	B0
166.09	166.09	ED	24	B0
166.61	166.61	F6	31	B0
167.05	167.05	E9	1E	B0
167.41	167.41	F4	2E	B0
168.00	168.00	F2	2B	B0
168.45	168.45	F0	28	B0

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
168.80	168.80	EE	25	B0
169.09	169.09	EC	22	B0
169.33	169.33	EA	1F	B0
169.53	169.53	E8	1C	B0
171.82	171.82	FD	3B	B0
174.11	174.11	E8	1B	B0
174.31	174.31	EA	1E	B0
174.55	174.55	EC	21	B0
174.83	174.83	EE	24	B0
175.19	175.19	F0	27	B0
175.64	175.64	F2	2A	B0
176.22	176.22	F4	2D	B0
176.59	176.59	E9	1C	B0
177.02	177.02	F6	30	B0
177.55	177.55	ED	22	B0
178.18	178.18	F8	33	B0
178.69	178.69	E8	1A	B0
178.98	178.98	F1	28	B0
179.29	179.29	EA	1D	B0
180.00	180.00	FA	36	B0
180.86	180.86	EE	23	B0
181.36	181.36	F5	2E	B0
181.93	181.93	F0	26	B0
182.23	182.23	EB	1E	B0
183.27	183.27	FC	39	B0
184.27	184.27	EA	1C	B0
184.55	184.55	EF	24	B0
185.03	185.03	F4	2C	B0
185.45	185.45	EC	1F	B0
186.14	186.14	F9	34	B0
186.89	186.89	EE	22	B0
187.44	187.44	F6	2F	B0
187.85	187.85	E8	18	B0
188.18	188.18	F3	2A	B0
188.66	188.66	F0	25	B0
189.00	189.00	ED	20	B0
189.25	189.25	EA	1B	B0
190.91	190.91	FE	3C	B0

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
192.44	192.44	E8	17	B0
192.64	192.64	EB	1C	B0
192.92	192.92	EE	21	B0
193.30	193.30	F1	26	B0
193.85	193.85	F4	2B	B0
194.23	194.23	EA	1A	B0
194.73	194.73	F7	30	B0
195.40	195.40	F0	24	B0
195.68	195.68	E9	18	B0
196.36	196.36	FA	35	B0
197.02	197.02	E8	16	B0
197.27	197.27	EF	22	B0
197.85	197.85	F6	2E	B0
198.55	198.55	F2	27	B0
198.95	198.95	EE	20	B0
199.21	199.21	EA	19	B0
200.45	200.45	FD	3A	B0
201.60	201.60	E8	15	B0
201.82	201.82	EC	1C	B0
202.14	202.14	F0	23	B0
202.66	202.66	F4	2A	B0
203.06	203.06	EB	1A	B0
203.64	203.64	F8	31	B0
204.19	204.19	EA	18	B0
204.55	204.55	F3	28	B0
204.98	204.98	EE	1F	B0
205.23	205.23	E9	16	B0
206.18	206.18	FC	38	B0
207.27	207.27	EC	1B	B0
207.61	207.61	F1	24	B0
208.26	208.26	F6	2D	B0
208.88	208.88	F0	22	B0
209.17	209.17	EA	17	B0
210.00	210.00	FB	36	B0
210.76	210.76	E8	13	B0
211.00	211.00	EE	1E	B0
211.47	211.47	F4	29	B0
211.91	211.91	ED	1C	B0
212.73	212.73	FA	34	B0
213.47	213.47	EB	18	B0

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
213.82	213.82	F2	25	B0
214.15	214.15	EA	16	B0
214.77	214.77	F9	32	B0
215.35	215.35	E8	12	B0
215.61	215.61	F0	21	B0
216.36	216.36	F8	30	B0
217.03	217.03	EE	1D	B0
217.64	217.64	F7	2E	B0
218.18	218.18	EC	19	B0
218.68	218.68	F6	2C	B0
219.13	219.13	EA	15	B0
219.55	219.55	F5	2A	B0
219.93	219.93	E8	11	B0
220.28	220.28	F4	28	B0
220.91	220.91	F3	26	B0
221.45	221.45	F2	24	B0
221.93	221.93	F1	22	B0
222.35	222.35	F0	20	B0
222.73	222.73	EF	1E	B0
223.06	223.06	EE	1C	B0
223.36	223.36	ED	1A	B0
223.64	223.64	EC	18	B0
223.88	223.88	EB	16	B0
224.11	224.11	EA	14	B0
224.32	224.32	E9	12	B0
224.51	224.51	E8	10	B0
229.09	229.09	FE	3B	B0
233.67	233.67	E8	0E	B0
233.86	233.86	E9	10	B0
234.07	234.07	EA	12	B0
234.30	234.30	EB	14	B0
234.55	234.55	EC	16	B0
234.82	234.82	ED	18	B0
235.12	235.12	EF	1A	B0
235.45	235.45	EF	1C	B0
235.83	235.83	F0	1E	B0
236.25	236.25	F1	20	B0
236.73	236.73	F2	22	B0
237.27	237.27	F3	24	B0
237.90	237.90	F4	26	B0

Table A–1. PLL Register Settings for 14.31818 MHz Reference (Continued)

OUTPUT	VCO	NREG	MREG	PREG
238.25	238.25	E8	0D	B0
238.64	238.64	F5	28	B0
239.05	239.05	EA	11	B0
239.50	239.50	F6	2A	B0
240.00	240.00	EC	15	B0
240.55	240.55	F7	2C	B0
241.15	241.15	EE	19	B0
241.82	241.82	F8	2E	B0
242.57	242.57	F0	1D	B0
242.84	242.84	E8	0C	B0
243.41	243.41	F9	30	B0
244.03	244.03	EA	10	B0
244.36	244.36	F2	21	B0
244.71	244.71	EB	12	B0
245.45	245.45	FA	32	B0
246.27	246.27	ED	16	B0
246.71	246.71	F4	25	B0
247.18	247.18	EE	18	B0
247.42	247.42	E8	0B	B0
248.18	248.18	FB	34	B0
249.01	249.01	EA	0F	B0
249.30	249.30	F0	1C	B0
249.92	249.92	F6	29	B0

Appendix B
PLL Programming Examples

Loop Clock PLL

The internal structure of the loop clock PLL is shown in Figure B–1. The loop clock PLL phase aligns the received LCLK with the internal dot clock in order to ensure reliable data latching into the TVP3026. The phase detector performs phase comparison at the rising edge of the received clocks after the N and M prescalers. The charge pump and loop filter generate an analog control signal to the voltage controlled oscillator. The VCO frequency is then divided by the P and Q post-scalers. The P post-scaler provides division ratios of 1, 2, 4, or 8. The Q post-scalar provides additional division ratios of 2, 4, 6, 8, 10, 12, 14 and 16. The Q post-scalar provides for the extra low frequencies needed for low-resolution graphics using a high multiplex ratio, such as 640 x 480, 8 bits/pixel, using a 64-bit pixel bus. The output from the loop clock PLL or the pixel clock PLL may be selected for output on the RCLK terminal.

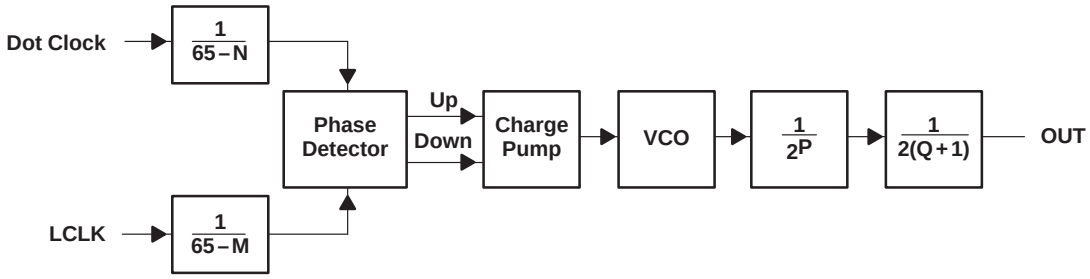


Figure B–1. Loop Clock PLL Structure

As a programming example, we can follow the procedure of subsection 2.4.3.1, *Programming for All Modes Except Packed-24*, for a mode using a 170 MHz pixel clock, 8 bits/pixel, a 64-bit pixel bus, and an external division factor (through the GUI accelerator) of 2.

$$F_D = 170\ \text{MHz}, \quad B = 8, \quad W = 64, \quad K = 2$$

$$F_L = F_D \times \frac{B}{W} = 170 \times \frac{8}{64} = 21.25\ \text{MHz}$$

$$F_R = K \times F_L = 2 \times 21.25 = 42.5\ \text{MHz}$$

$$N = 65 - 4 \times \frac{W}{B} = 65 - 4 \times \frac{64}{8} = 33 = 0\text{x}21$$

$$M = 61 = 0\text{x}3D$$

$$Z = \frac{27.5 \times (65 - N)}{F_D \times K} = \frac{27.5 \times (65 - 33)}{170 \times 2} = 2.59$$

Since $Z < 16$ and $\log_2 (Z)$ is between 1 and 2, then P = 1 and Q = 0

Since bits 7 and 6 of the N-value register must be 1,1 the N-value register is loaded with 0x21 + 0xC0 = 0xE1. The M-value register is loaded with 0x3D. Since bits 7–2 of the P-value register must be 1111 00, the P-value register is loaded with 0x01 + 0xF0 = 0xF1. Bits 2–0 of the MCLK/loop clock control register (index: 0x39) are loaded with the Q value of 000.

The resulting divide ratios and clock frequencies are illustrated in Figure B–2.

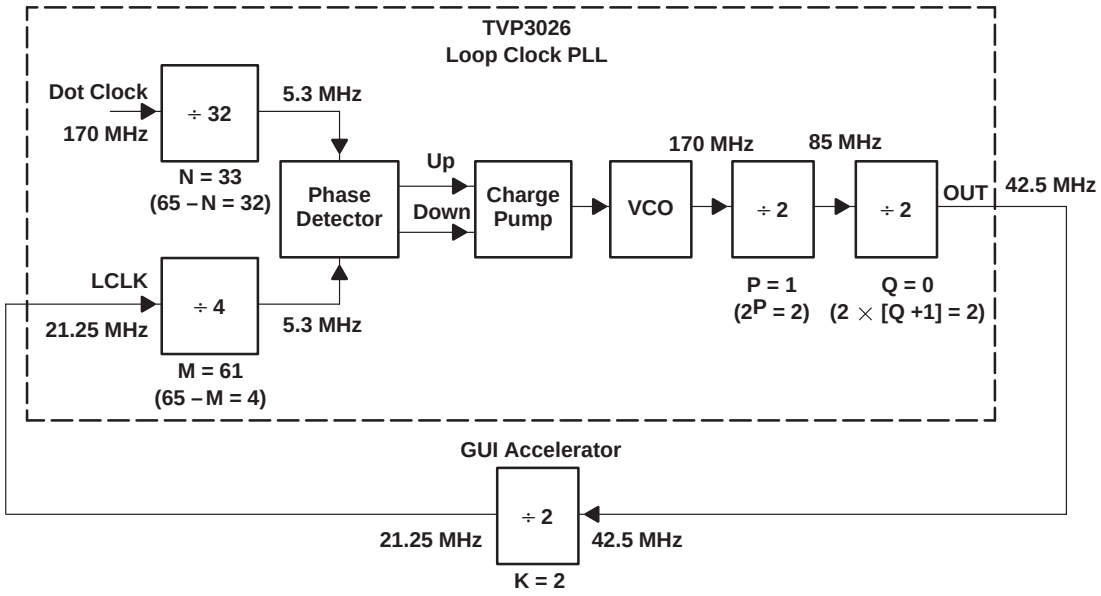


Figure B–2. Loop Clock PLL Example

Pixel Clock and MCLK PLLs

The internal structure used for the pixel clock and MCLK PLLs is shown in Figure B–3. These PLLs synthesize the pixel clock and MCLK frequencies. The reference clock can be either a resonant crystal or can be driven with a TTL level signal. The phase detector performs phase comparison at the rising edge of the received clocks after the N and M prescalers. The charge pump and loop filter generate an analog control signal to the VCO. The VCO frequency is then divided by the P post-scalar. The P post-scalar provides division ratios of 1, 2, 4, or 8. The output from the pixel clock PLL or the loop clock PLL may be selected for output on the RCLK terminal. The output from the MCLK PLL or the internal dot clock (to provide a smooth transition on MCLK) may be selected for output on the MCLK terminal. The same PLL register values may be used for the pixel clock PLL or MCLK PLL as long as the output frequency of the MCLK PLL does not exceed 100 MHz.

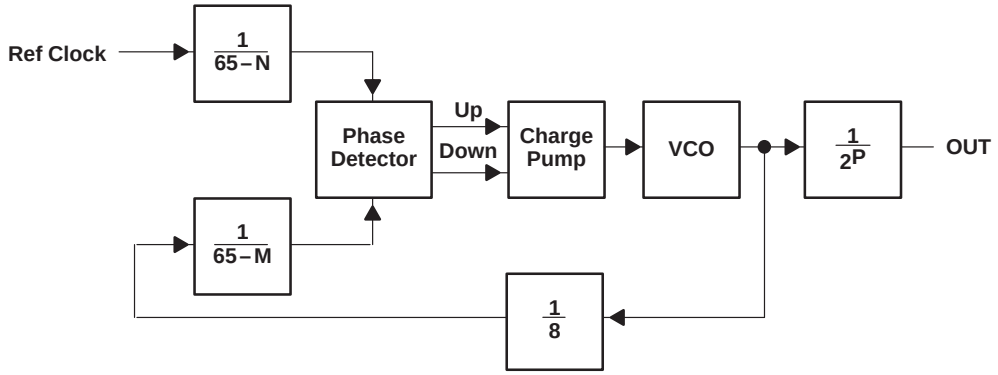


Figure B–3. Pixel Clock and MCLK PLL Structure

As a programming example, we can consider programming the pixel clock PLL for a mode using a 170 MHz pixel clock. Since the reference clock is the common 14.31818 MHz crystal, the register values in

Appendix A may be used directly. The closest frequency in Table A–1 is 169.53 MHz for which the PLL registers are loaded with N-value register = 0xE8, M-value register = 0x1C, and P-value register = 0xB0. The N and M numbers are the lower 6 bits of the N-value register and the M-value register respectively. The P number is the lower two bits of the P-value register. After extracting and converting to decimal, this becomes N = 40, M = 28, and P = 0. The resulting divide ratios for the prescalers and the post-scaler and the resulting clock frequencies are illustrated in Figure B–4.

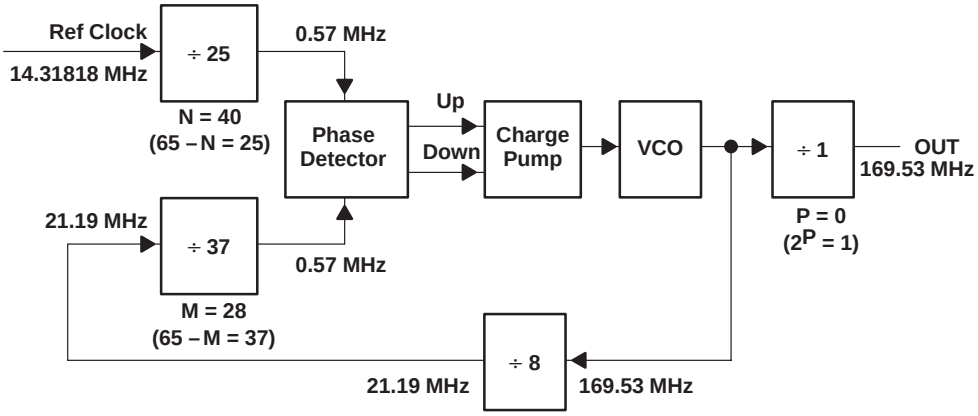


Figure B–4. Pixel Clock PLL Example

The equations given in subsection 2.4.1, *Pixel Clock PLL*, give the same result for the VCO frequency and PLL output frequency. The VCO frequency is within the specified limits.

$$F_{VCO} = 8 \times F_{REF} \times \frac{65 - M}{65 - N} = 8 \times 14.31818 \times \frac{65 - 28}{65 - 40} = 169.53 \text{ MHz}$$

$$110 \text{ MHz} \leq F_{VCO} \leq 220 \text{ MHz}$$

$$F_{PLL} = \frac{F_{VCO}}{2^P} = \frac{169.53}{2^0} = 169.53 \text{ MHz}$$

Appendix C
Recommended Clock Programming Procedures

The following procedures are recommended for programming the TVP3026 PLLs. In a typical system, many combinations of resolution and refresh rates are possible. The PLLs must be able to switch between any two of these frequencies. It is difficult to test all possible combinations. In order to reduce the possibility of error, it is recommended that the PLL is reset prior to programming. This causes the voltage controlled oscillator (VCO) to stop oscillating prior to searching for the new programmed frequency. When this is done, the frequency search always begins at the same point and the possibility for error is greatly reduced.

MCLK PLL

This is the simplified method of programming the MCLK PLL. If the system does not allow MCLK to be stopped or is sensitive to transition effects on MCLK, the procedure described in Section 2.4.2.1 can be used instead.

1. Disable MCLK PLL (PLLEN bit = 0).
2. Program MCLK PLL N, M, and P registers (with PLLEN bit = 1) for new frequency.

VGA Mode Setup

1. Set loop clock PLL PLLEN bit to 0.
2. Set pixel clock PLL PLLEN bit to 0.
3. Set PLLSEL(1, 0) bits to 1x. (This causes programmed PLLEN bits to take effect. VCOs are stopped.)
4. Set PLLSEL(1, 0) bits to 00 (25.057 MHz) or 01 (28.686 MHz).

Table C–1. Programming Procedure – VGA Mode Setup

Index	Data	Comment
1A	77	Select CLK0 as clock source. Set bits 6–4 to disable unused VCLK output.
18, 19	80, 98	VGA mode
2C	2A	Point to P registers
2F	0	Set loop clock PLL PLLEN bit to 0
2D	0	Set pixel clock PLL PLLEN bit to 0
PLLSEL(1, 0)	11	Causes programmed PLLEN bits to take effect. VCOs are stopped.
PLLSEL(1, 0)	00 (for 25.057 MHz) 01 (for 28.636 MHz)	Select one of the hard-wired VGA pixel clock PLL settings.
39	18	Pixel clock PLL routed to RCLK terminal (see Note 2).

NOTES: 1. These procedures show the order of programming that should be used for programming the clocks and related registers. The complete mode setup may require other registers to be programmed also.
2. In standard VGA modes, the PLLSEL(1,0) inputs select the pixel clock PLL fixed frequency settings (25.057 MHz or 28.636 MHz). The loop clock PLL is normally reset and the pixel clock PLL is routed to the RCLK output.

Extended Mode Setup

1. Set loop clock PLL PLLEN bit to 0.
2. Set pixel clock PLL PLLEN bit to 0.
3. Set PLLSEL(1, 0) bits to 1x. (This causes programmed PLLEN bits to take effect. VCOs are stopped.)
4. Program pixel clock PLL N, M, and P registers (with PLLEN bit = 1) for new frequency.
5. Poll pixel clock PLL status register until LOCK bit is set to 1.
6. Program loop clock PLL Q divider (MCLK/loop clock control register bits 2–0).
7. Program loop clock PLL N, M, and P registers (with PLLEN bit = 1) to new setting.
8. Poll loop clock PLL status register until LOCK bit is set to 1.

Table C–2 TVP3026 Clock Programming Procedure – Extended Mode Setup

Index	Data	Comment
1A	75	Select pixel clock PLL as clock source. Set bits 6–4 to disable unused VCLK output (see Note 3).
2C	2A	Point to P registers
2F	0	Set loop clock PLL PLLEN bit to 0.
2D	0	Set pixel clock PLL PLLEN bit to 0.
PLLSEL(1, 0)	11	Causes programmed PLLEN bits to take effect. VCOs are stopped.
2C	0	Point to N registers
2D	N, M, P from table	Program pixel clock PLL (see Note 4)
2C	3F	Point to status registers
2D	(read)	Poll until bit 6 (LOCK bit) is set
39	3X†	Set Q divider for loop clock PLL
2C	0	Point to N registers
2F	E1, 3D, Fx† (8 bpp) F1, 3D, Fx (15/16 bpp) F9, BE, Fx (24 bpp, 8:3 mux) F9, 3D, Fx (32 bpp)	Program loop PLL
2C	3F	Point to status registers
2F	(read)	Poll until bit 6 (LOCK bit) is set to 1.

† Depends on pixel clock frequency so that the loop clock PLL VCO is within its operating range.

NOTES: 3. Setting index 0x1A bits 6–4 to 111 for all modes is optional. This disables the unused VCLK output for the purpose of eliminating unnecessary switching. This changes the value from 0x07 to 0x77 for VGA mode, and from 0x05 to 0x75 for high-resolution VGA and extended modes.

4. The upper two bits of the N register for all PLLs should be set to 11.

Appendix D
PC-Board Layout Considerations

PC-Board Considerations

It is recommended that a 4-layer PC board be used with the TVP3026 video interface palette: one layer for 5-V power, one for GND, and two for signals. The layout should be optimized for the lowest noise on the TVP3026 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of analog V_{DD} and GND terminals (see Figure D–1) should be minimized so as to minimize inductive ringing. The TVP3026 P0–P63 terminal assignments have been selected for minimum interconnect lengths between these inputs and the standard VRAM pixel data outputs. The TVP3026 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

For maximum performance, the analog-video-output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the TVP3026 to minimize reflections. Unused analog outputs should be connected to GND.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length-dependent ghosts. Simple pulse filters can reduce high-frequency energy, thus reducing EMI and noise. The filter impedance must match the line impedance.

Ground Plane

It is also recommended that only one ground plane be used for both the TVP3026 and the rest of the logic. Separate digital and analog ground planes are not needed and can potentially cause system problems.

Power Plane

Split-power planes for the TVP3026 and the rest of the logic are recommended. The TVP3026 VIP analog circuitry should have its own power plane, referred to as AV_{DD}. These two power planes should be connected at a single point through a ferrite bead, as shown in Figures D–1 and D–2.This bead should be located as near as possible to where the power supply connects to the board. To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible. This reduces the lead inductance and is consistent with reliable operation.

For the best performance, a 0.1-µF ceramic capacitor in parallel with a 0.01-µF chip capacitor should be used to decouple each of the groups of power terminals to GND. These capacitors should be placed as close as possible to the device, as shown in Figure D–2.

When a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a 3-terminal voltage regulator for supplying power to AV_{DD}.

COMP and REF Terminals

A 0.1-μF ceramic capacitor should be connected between COMP1 and COMP2 to avoid noise and color-smearing problems. A 0.1-μF ceramic capacitor is also recommended between GND and REF to further stabilize the output image. This 0.1-μF capacitor is needed for either internal or external voltage references. These capacitor values may depend on the board layout; experimentation may be required in order to determine optimum values.

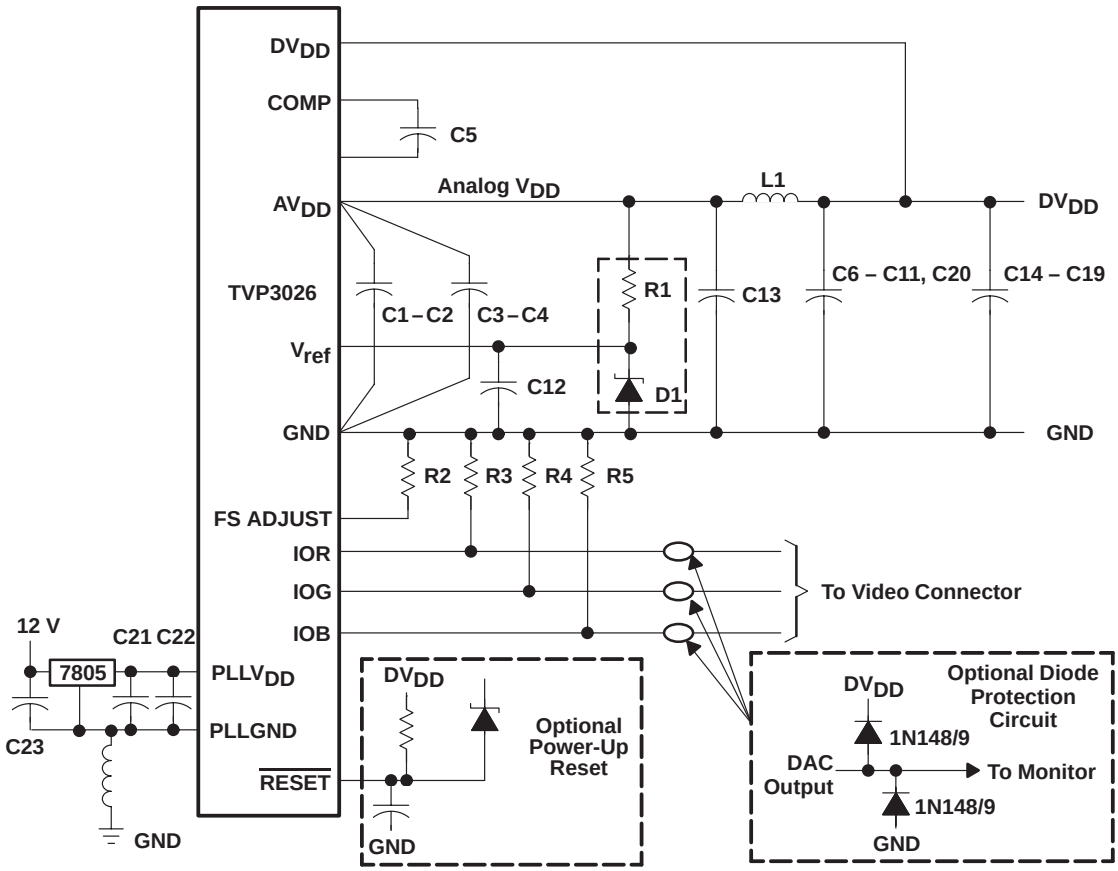
Analog Output Protection

The TVP3026 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching ac-coupled monitors.

The diode protection circuit shown in Figure D–1 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The IN4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PLL Supply

A separate 5-V regulator is recommended for the PLL supply. A typical circuit is shown in Figure D–1.



Location	Description	VENDOR PART NUMBER†
C1, C2, C5 – C12, C20	0.1-µF ceramic capacitor	Erie RPE110Z5U104M50V
C3, C4, C14 – C19, C21, C22	0.01-µF ceramic chip capacitor	AVX 12102T103QA1018
C13	33-µF tantalum capacitor	Mallory CSR13F336KM
C23	10-µF ceramic capacitor	Panasonic ECS–H1ED106R
L1	Ferrite bead	Fair-Rite 2743001111‡
R1	1000-Ω 1% metal-film resistor	Dale CMF-55C
R2	523-Ω 1% metal-film resistor	Dale CMF-55C
R3, R4, R5	75-Ω 1% metal-film resistor	Dale CMF-55C
D1	1.2-V voltage reference	TI LM385-1.2

† The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the TVP3026.

‡ Or equivalent only.

NOTE A: R1, D1, and reset circuit are optional. In general, each pair of device power and GND terminals should be separately decoupled with 0.1-µF and 0.01-µF capacitors

Figure D–1. Typical Connection Diagram and Parts

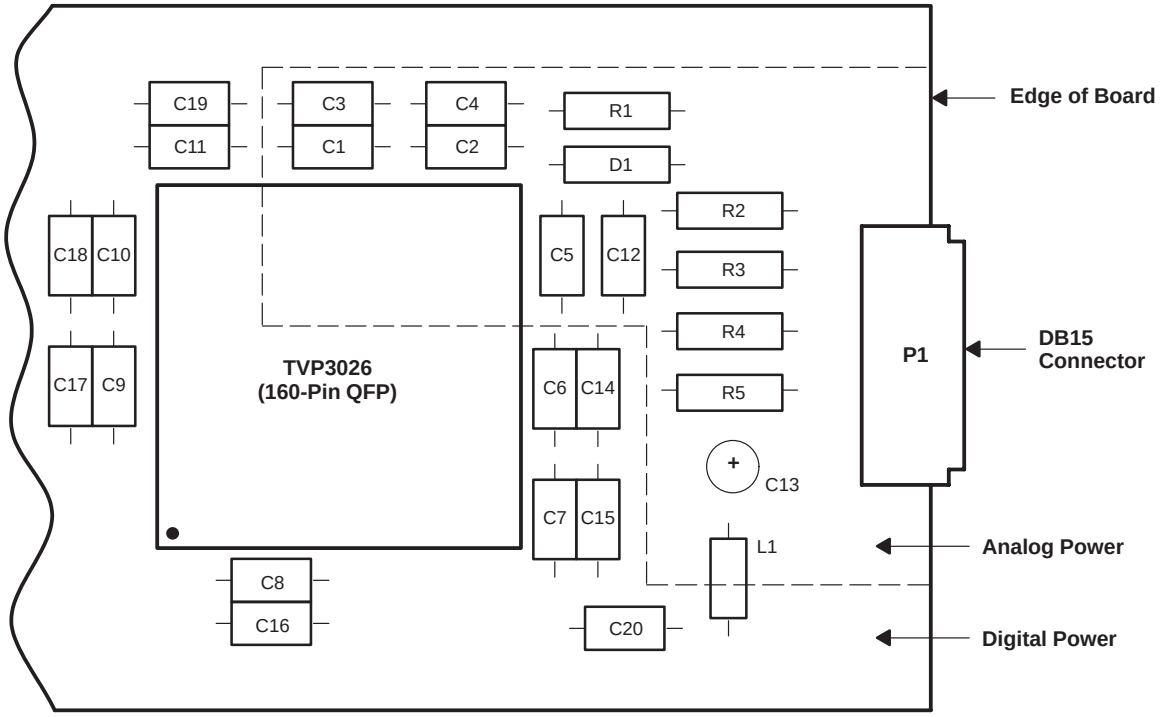


Figure D–2. Typical Component Placement With Split-Power Plane

Appendix E
Crystal Selection

This section provides typical crystal specifications for the reference crystal used with the TVP3026. The recommended reference frequency is the common 14.31818 MHz. The hard-wired VGA frequencies assume this reference frequency. Other reference frequencies can be used as indicated below, but the VGA frequencies will be incorrect.

The specifications below are commonly specified by crystal manufacturers. Frequency calibration tolerance is a measurement of how close the mean output frequency is to the target frequency. The accuracy of this parameter is not critical in video display systems. Small errors in the mean frequency are undetectable on the display, but .produce slight changes in the horizontal and vertical scan rates.

The oscillator circuit in the TVP3026 is of the pierce oscillator type and is therefore designed for a parallel-resonant crystal. For the TVP3026A, a series resonant crystal is also acceptable, but results in a 250–500 ppm increase in mean frequency. For the TVP3026B, use of a series-resonant crystal will not result in an increase in mean frequency.

Frequency stability is a critical factor for video display systems. This is a measurement of frequency deviations about the mean (jitter). Frequency stability determines the degree to which the crystal contributes to on-screen jitter.

Table E–1. Typical Crystal Specifications

PARAMETER	MIN	TYP	MAX	UNITS
Frequency		14.31818		MHz
Frequency calibration tolerance		1%		
Frequency stability		50		ppm
Equivalent series resistance		35		Ω

Appendix F
Changes Made For TVP3026 Revision B

Functional Changes

- Process Change / Die Shrink – The process was changed from 0.8 micron CMOS to 0.72 micron CMOS.
- PLL Loop Filter and Charge Pump – The loop filter parameters and charge pump were modified to further enhance the stability of the PLL.
- Crystal Oscillator Circuit – The crystal oscillator circuit was changed to a dc coupled input. This causes the circuit to oscillate at the crystal frequency as opposed to the slight difference seen in the A revision due to its ac coupled input.
- ESD Structures – The ESD structures were slightly modified to accommodate for changes in process parameters and feature sizes.
- Internal Timing Change – An internal timing change was made to improve pixel port latch timing for the 1:1 multiplex modes.

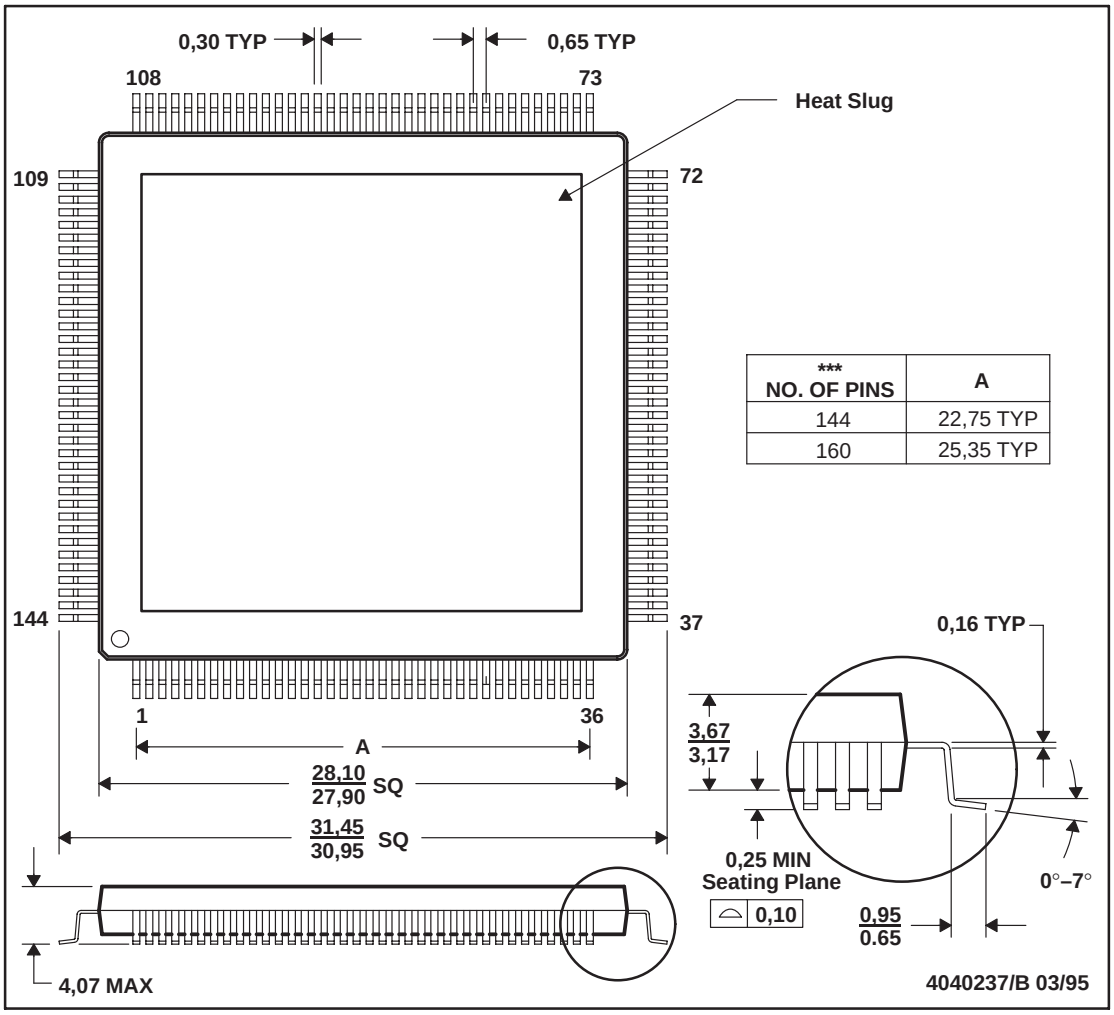
Programming Changes

- PLL N-Value Registers – Bits 7 and 6 of the PLL N-value register for all PLLs are do not cares. It is not necessary to program these bits to 11.
- Loop Clock PLL M-Value Register Programming – Loop clock PLL M-value register programming is changed as shown in Table 2–15. For the 4:3 multiplex mode, the silicon revision register (index: 0x01) must be tested to determine the value for the M-value register.
- Latch Control Register Programming – Latch control register (index: 0x0F) programming is changed as shown in Table 2-16. For the 4:3 multiplex mode, the silicon revision register (index: 0x01) must be tested to determine the value for the latch control register.
- Silicon Revision Register – The silicon revision register (index: 0x01) indicates revision A when $\leq$ 0x20 and indicates revision B when $\geq$ 0x21.

Appendix G
Mechanical Data

PCE (S-PQFP-G*)** **PLASTIC QUAD FLATPACK**

144-PIN SHOWN

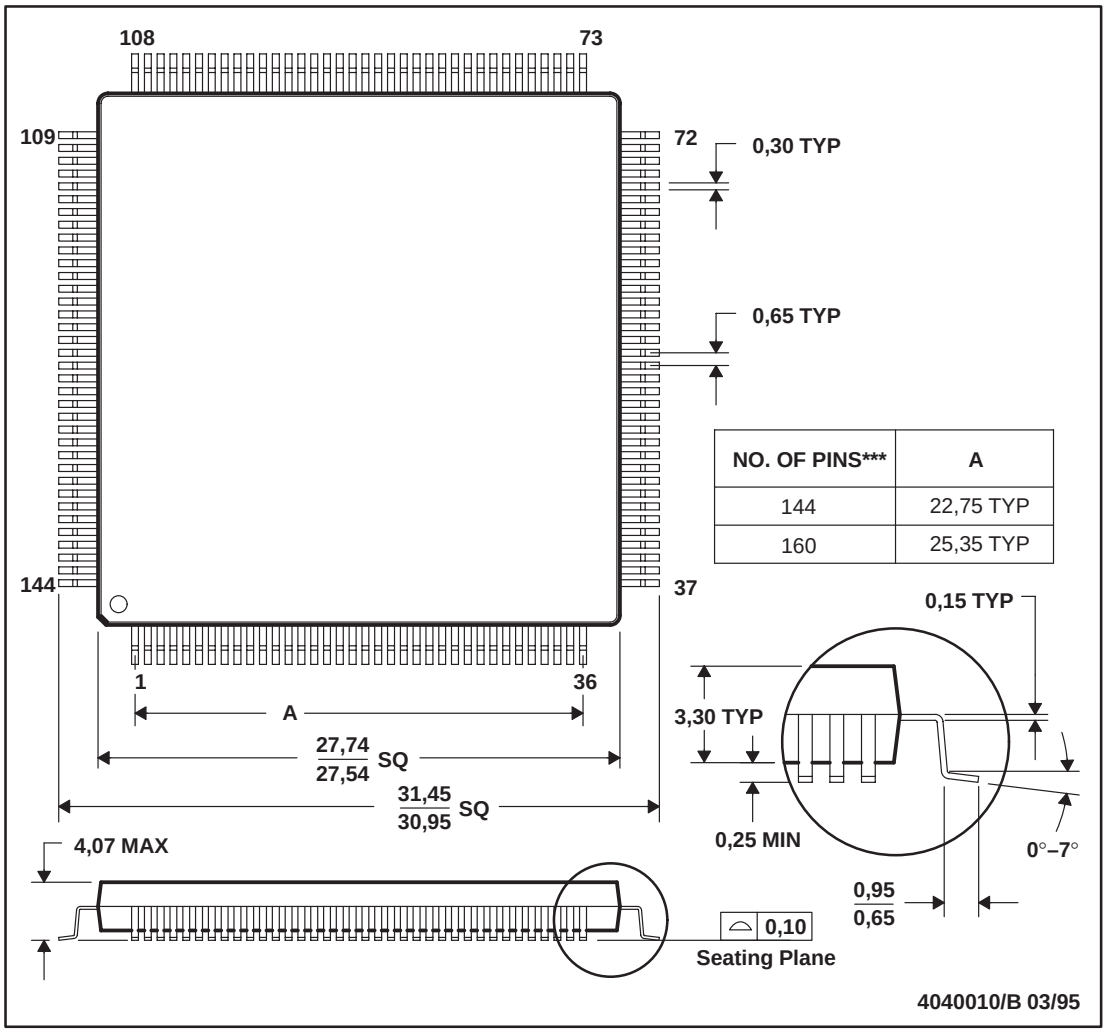


*** NO. OF PINS	A
144	22,75 TYP
160	25,35 TYP

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package (HSL).

MDN (S-MQFP-G***) METAL QUAD (MQUAD®) CAVITY-UP FLAT PACKAGE

144-PIN SHOWN



NO. OF PINS***	A
144	22,75 TYP
160	25,35 TYP

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MQUAD is a registered trademark of Olin Corporation.
D. This quad flat package consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic. Ultrasonic cleaning of this package or boards with this package is not permitted.
E. The 144 MDN is identical to 160 MDN except 4 leads per corner are removed.

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