High-Performance Single-Chip GPIB Talker/Listener ASIC – NI TNT5002

NI TNT5002

- Integrated IEEE 488.1 compliant transceivers
- Single-chip PCI-to-GPIB solution
- PCI or 16-bit generic CPU interface
- 144-pin plastic quad flat pack (QFP), surface-mount package
- Fast data transfers
  - More than 1.5 MB/s (IEEE 488.1)
  - More than 8 MB/s (HS488)
- Compliant with PCI Local Bus Specification, Revision 2.2
- 32-bit/33 MHz PCI bus master
- 3.3 or 5 V PCI signaling; 3.3 V core
- Internal loop-back mode for complete in-system functional testing
- Meets all IEEE 488.2 requirements
- REM, listen addressed, talk addressed indicator pins
- Automatic EOS and/or new line message detection
- Built-in DMA controller in PCI mode, DMA capable in generic mode
- Programmable timer interrupt for general-purpose timing
- Reduces software overhead
  - Does not lose a data byte if ATN asserts during transmission
  - Static interrupt status bits that do not clear when read
  - Automatically transmits END or performs RFD holdoff on last byte of DMA transfer
- Interrupts when handshake is complete on last byte of a DMA transfer
- 32-bit counter for large, uninterrupted data transfers
- 32-byte FIFO buffers data between GPIB and CPU/DMA controller

Overview

The National Instruments TNT5002 is a single-chip IEEE 488.2 Talker/Listener interface to GPIB. The NI TNT5002 contains complete NI TNT4882 and NI NAT9914/TI TMS9914A register sets. Therefore, if you are using any of these ASICs, you can port existing code directly to the TNT5002, significantly reducing software development time. The TNT5002 is ideal for use in all IEEE 488 instrument designs that incorporate the PCI bus because of the compact size of the chip, its surface-mount package, and performance enhancements, which include the HS488 high-speed protocol for GPIB transfers.

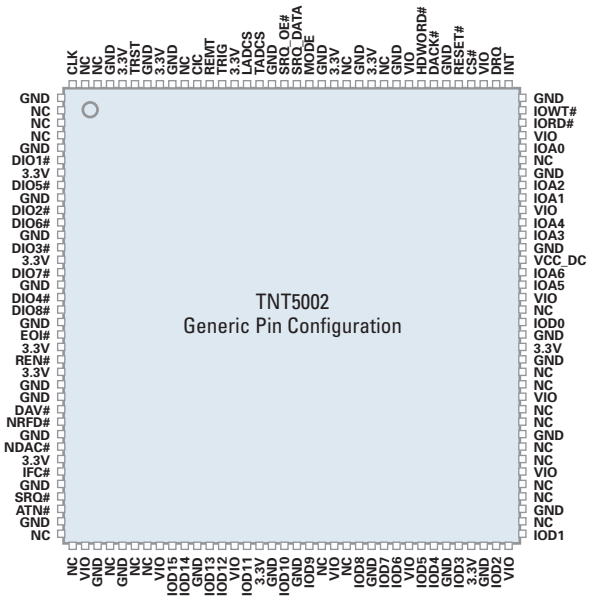

Figure 1. TNT5002 Generic Pin Configuration

HS488

The HS488 protocol for GPIB transfers, adopted as part of ANSI/IEEE Standard 488.1-2003, increases the maximum data transfer rate of IEEE 488.1-1987 devices up to 8 MB/s. Maximum data transfer rates obtainable using HS488 depend on the host architecture and system configuration. The TNT5002 completely and transparently handles the HS488 protocol without additional circuitry. Because HS488 is a superset of the IEEE 488.1 standard, you can mix non-HS488 GPIB devices with devices that are high-speed capable without changing your application programs.

TNT5002 Hardware Architecture and Modes

The National Instruments TNT5002 integrates the circuitry of the TNT4882 with a 3.3 V PCI core (Figure 2). There are four distinct modes of operation for the TNT5002. PCI4882 and GEN4882 modes implement the TNT4882 one-chip register set. PCI9914 and GEN9914 modes implement the NAT9914/TI TMS9914A register set. Each of these two register sets can be accessed through a generic I/O interface or a PCI interface. PCI4882 and PCI9914 modes implement a PCI bus-master

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interface. GEN4882 and GEN9914 modes implement a generic I/O interface. You can change the register set dynamically because the pinout does not change between the two sets. However, the interface must be selected by the MODE pin and must not be changed dynamically becuase the pinout is significantly different between interfaces.

The TNT5002 has two different pin configurations. The generic pin configuration provides a simple interface to any CPU (Figure 1). With the PCI pin configuration, you can connect the TNT5002 directly to a PCI bus (Figure 3).

Software API

The TNT5002 is fully compatible with NI-Device software. NI-Device provides a powerful API with which instrument developers can create bus-independent firmware for their ANSI/IEEE Standard 488.2-1992 devices. The TNT5002 is compatible with the NI-Device DDK (driver development kit) and you can use plug-in boards that incorporate the ASIC with regular NI-Device packages on instruments running Windows OSs.

Developer Kit

To assist in the TNT5002 hardware design and software implementation, NI offers a special developer kit, which contains five TNT5002 samples, a plug-in evaluation board, high-performance NI-Device DDK source code software, and software and hardware reference manuals. This kit is available to all interested developers who want to use the TNT5002 in their designs.

RoHS Compliance

NI currently offers the TNT5002 in both a standard package and a RoHS-compliant chip. You can order the chips using the part numbers shown below. The RoHS-compliant parts are identified through the added "F" at the end of the part number and the chip itself is marked with an e3 inside an ellipse to indicate a pure tin lead finish in accordance with the marking recommendations defined in JEDEC JESD97. The TNT5002 RoHS-compliant ASICs have a matte pure tin finish on their leads.

The RoHS-compliant TNT5002 meets industry requirements for baking and maximum solder reflow temperature. The baking requirements are outlined in JEDEC J-STD-033, and NI recommends using the solder reflow profile as shown in IPC/JEDEC J-STD-020C with a peak temperature of 260 °C, the maximum temperature they can withstand. The Moisture Sensitivity Level (MSL) for the RoHS-compliant surface mount TNT5002 ASIC is 3.

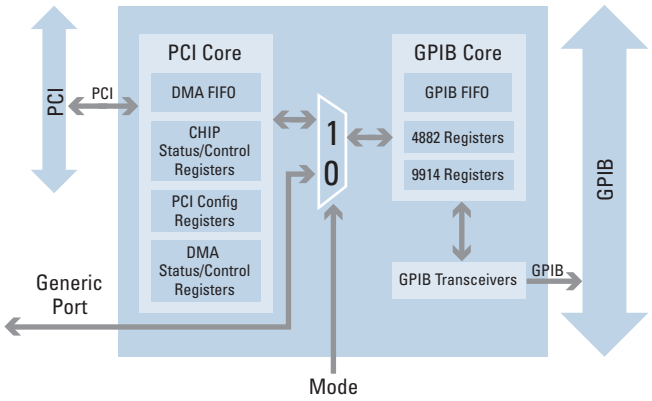

Figure 2. TNT5002 Block Diagram

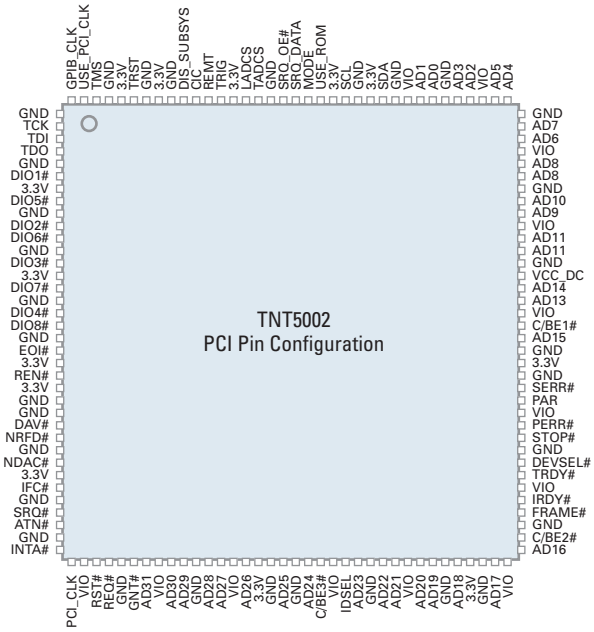

Figure 3. TNT5002 PCI Pin Configuration

Ordering Information

NI TNT5002-AQ

RoHS-compliant TNT5002-AQF24

Standard TNT5002-AQ24

Developer kit (RoHS-compliant) 778582-01

Sample kit (RoHS-compliant, 5 ASICs) 778583-01

Visit ni.com for a more detailed reference manual.

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