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Enhanced Micro Channel Interface Circuit (μCIC)

FEATURES

- Conforms to the IBM® Micro Channel™ Bus Interface Specifications
- Stores POS Option Select Bytes
- Supports Two DMA Channels Simultaneously
  - Full DMA Arbitration Support
  - Single Transfer and Burst DMA Modes
  - Support Programmable Fairness Mode
  - Software-Triggered DMA Supported
  - Register Programmable Priority
- Maps and Merges up to Five Interrupts into Four Micro Channel IRQ Lines
- On-Chip Timer/Frequency Generator
- Provides Shared Memory Arbitration Function for Intelligent Co-Processor Peripherals or Local CPU Applications
- Supports Independent Programmable Wait State Generation for Memory and I/O Cycles
  - Supports No Wait States, Synchronous and Asynchronous Extended Cycles
- Supplies a Combined Strobe Signal for Externally Latching the Contents of POS Registers 3, 6, and 7
- Provides Data Bus Transceiver Direction and Enable Control
- Hardware and Software Controlled Channel Check (CHCK) Interrupt Supported
- Provides Direct, High Current Drive to the Micro Channel Bus
- Low Power CMOS Technology

GENERAL DESCRIPTION

Standard Microsystems Corporation's MCI94C18A Enhanced Micro Channel Interface Circuit (μCIC) is a CMOS device which simplifies the design of adapter boards for IBM PS/2 computers. By integrating the most general functions in a single 68-pin package, the MCI94C18A significantly reduces the number of components required on the adapter board. The MCI94C18A implements all of the mandatory logic functions of the Micro Channel bus. In addition, a number of optional Micro Channel functions plus a flexible peripheral interface are provided.

In support of the Programmable Option Select (POS) function, the μCIC provides the signals required to place the card ID data on the bus. The card ID data is stored externally. Three additional POS registers are also implemented which include the mandatory bits defined by IBM.

The MCI94C18A supports two independent DMA channels from the peripheral. DMA transfers can be initiated via either hardware request signals from the peripheral or software bits set by the CPU. After arbitrating on the Micro Channel bus for the DMA cycle, the MCI94C18A allows for single cycle or multiple (Burst) cycle transfers. A programmable option is provided to select between linear priority or fairness algorithms for DMA accesses.

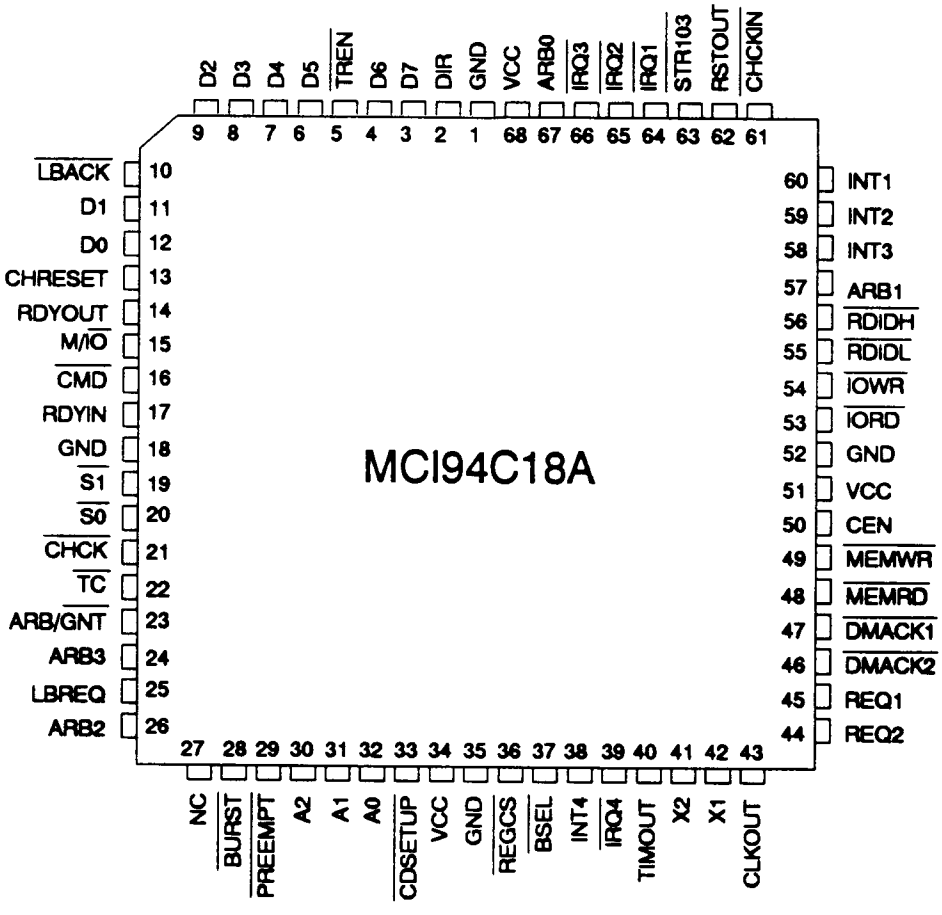
A local bus arbitration circuitry is included in the MCI94C18A device to simplify the implementation of a shared memory function on an adapter board. This feature is most useful for applications with intelligent peripherals.

The MCI94C18A features a flexible interrupt interface whereby four user interrupt signals can be mapped in a one-to-one or many-to-one fashion to four IRQ signals on the Micro Channel. In addition, an on-chip Timer/ Frequency generator can be used as a fifth interrupt source. The Timer generates a programmable general purpose clock to be used on the adapter board.

Both synchronous and asynchronous extended cycles are supported by the MCI94C18A. Additionally, a programmable wait state generator and automatic extension of the cycle are provided to simplify the interface to slow memory or I/O peripherals.

The physical pin placement of the MCI94C18A is assigned to correspond to the positioning of I/O signals on the Micro Channel bus. This simplifies the routing of a printed circuit board.

PIN CONFIGURATION



Package: 68-Pin PLCC

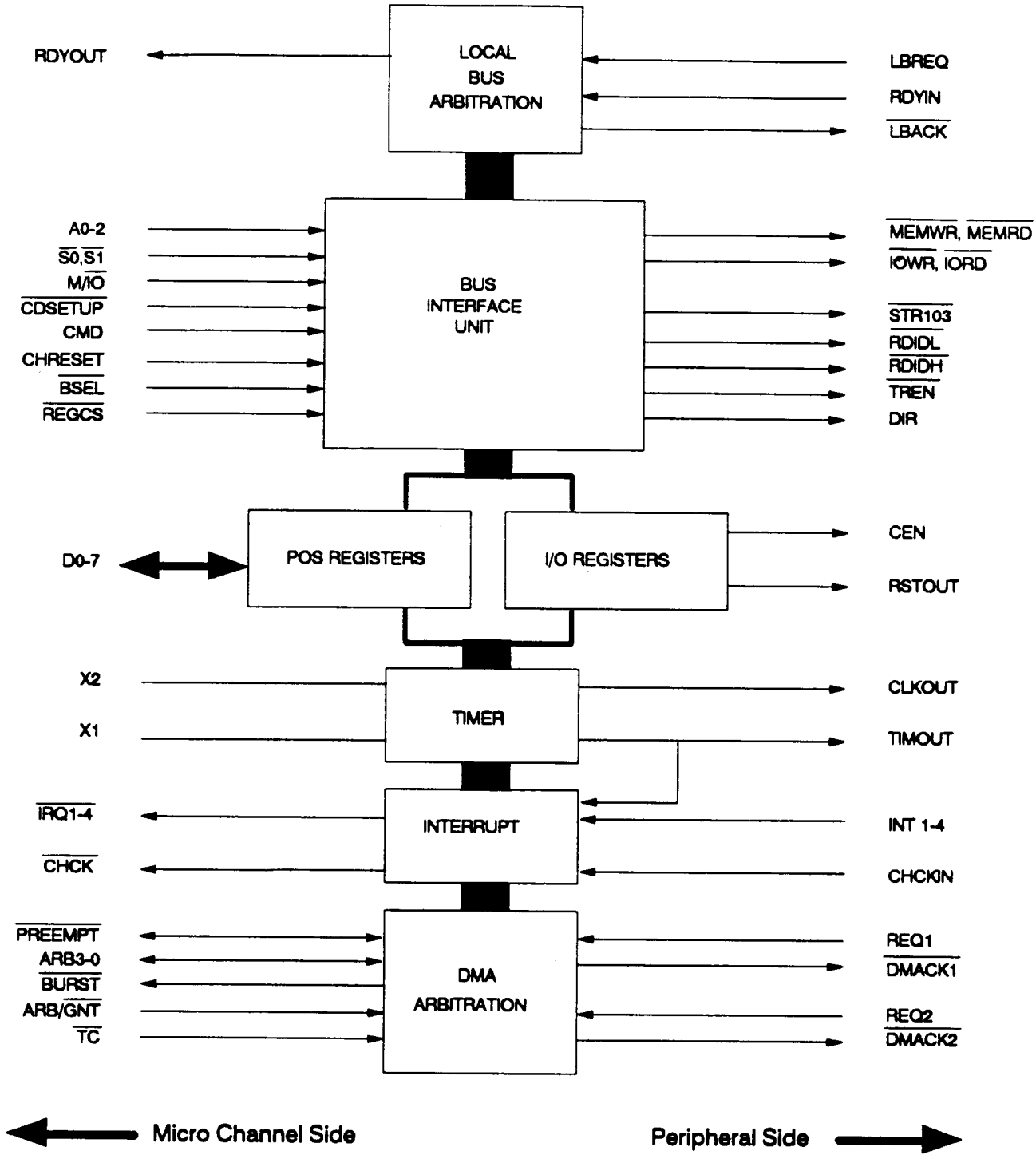


FIGURE 1 - INTERNAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
		MICRO CHANNEL INTERFACE	
19 20	Status 1 Status 2	$\overline{S1}$ $\overline{S2}$	Input. These signals define the type of access cycle (read vs. write) being performed. Directly connected to the corresponding status lines of the Micro Channel bus, they are internally latched on the falling edge of $\overline{CMD}$.
30,31, 32	Address 2-0	A2-A0	Input. Low order bits of the address bus. These lines are used to indicate which of the internal POS or I/O registers are selected for access. Directly connected to the Micro Channel bus, these lines are internally latched on the falling edge of $\overline{CMD}$.
15	Memory/Input Output	M/$\overline{IO}$	Input. This signal distinguishes between a memory and an I/O cycle. Directly connected to the Micro Channel bus, this line is internally latched on the falling edge of $\overline{CMD}$.
33	Card Setup	$\overline{CDSETUP}$	Input. This signal selects the board POS registers for access. Generally used for setup or error recovery, this signal is directly connected to the Micro Channel bus and is internally latched on the falling edge of $\overline{CMD}$.
13	Channel Reset	CHRESET	Input. This signal is generated by the Micro Channel to reset and initialize all adapters. The MCI94C18A is reset to its power-up state upon CHRESET and generates the RSTOUT signal for the board.
16	Command	$\overline{CMD}$	Input. This signal defines a valid cycle on the bus. Directly connected to the Micro Channel bus, its falling edge is used to latch various pipelined inputs.
14	Ready Out	RDYOUT	Output. This signal, when connected to the CD CHRDY line of the Micro Channel bus, is used to extend bus cycles. The programmable wait state generation circuitry of the MCI94C18A controls the generation of no wait, synchronous, or asynchronous extended cycles.
39,66 65,64	Interrupt Request Outputs	$\overline{IRQ4\text{-}1}$	Output. These open drain signals are used as interrupt requests on the Micro Channel bus. They can be connected to any of $\overline{IRQ3\text{-}7}$, $\overline{IRQ9\text{-}12}$ or $\overline{IRQ14\text{-}15}$ lines of the Micro Channel.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
21	Channel Check	$\overline{\text{CHCK}}$	Output. This open drain signal is used to indicate a serious error. Asserted as a function of CHCKIN, this signal is directly connected to the Micro Channel bus.
DMA ARBITRATION INTERFACE			
24,26 57,67	Arbitration Priority	ARB3-0	Input/Output. These four open drain I/O lines are used to drive and sense the arbitration levels on the Micro Channel bus. They connect directly to the ARB3-0 lines of the Micro Channel.
23	Arbitrate/Grant	ARB/$\overline{\text{GNT}}$	Input. This signal is generated by the Micro Channel Central Arbitration Control Point and indicates the beginning and end of a DMA arbitration cycle.
22	Terminal Count	$\overline{\text{TC}}$	Input. Directly connected to the Micro Channel's $\overline{\text{TC}}$ line, this signal indicates the terminal count of a DMA transfer. The MCI94C18A immediately stops burst DMA transfers upon detecting $\overline{\text{TC}}$.
29	Preempt	$\overline{\text{PREEMPT}}$	Input/Output. This open drain I/O signal is driven by the MCI94C18A to request a Micro Channel arbitration cycle. After winning an arbitration cycle, the MCI94C18A senses $\overline{\text{PREEMPT}}$ to cease a burst transfer. This signal is directly connected to the Micro Channel bus.
28	Burst	$\overline{\text{BURST}}$	Output. This open drain signal is driven by the MCI94C18A to indicate a block DMA transfer on the Micro Channel. It is directly connected to the Micro Channel bus.
45 44	DMA Request 1 DMA Request 2	REQ1 REQ2	Input. These active high signals are asserted by the peripheral to request DMA cycles from the corresponding channel of the MCI94C18A.
46,47	DMA Acknowledge	$\overline{\text{DMACK2-1}}$	Output. These active low signals are generated by the MCI94C18A indicating that it has won an arbitration cycle for the corresponding cycle.
PERIPHERAL INTERFACE			
63	Strobe 103	$\overline{\text{STR103}}$	Output. This active low signal is used to signal a write operation into POS registers 103, 106 or 107. It is intended to simplify the implementation of the external POS register.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
50	Card Enable	CEN	Output. This signal reflects the value of POS 102 register bit 0. A low level indicates the board has not been configured and enabled for normal operation. Following CHRESET, CEN is set low.
37	Board Select	$\overline{\text{BSEL}}$	Input. This signal selects the memory or I/O space of the board for access. It is supplied by the external address comparator and is internally latched on the falling edge of $\overline{\text{CMD}}$.
36	Register Chip Select	$\overline{\text{REGCS}}$	Input. This signal selects the I/O registers of the MCI94C18A for access. It is supplied by the external address comparator and is internally latched on the falling edge of $\overline{\text{CMD}}$.
62	Reset Output	RSTOUT	Output. This signal is the reset output for the board. It is asserted during CHRESET or as a function of the software reset bit.
40	Timer Output	TIMOUT	Output. This signal is a general purpose square wave output with a programmable frequency. An internal timer interrupt is generated on the rising edge of TIMOUT.
53	IO Read	$\overline{\text{IORD}}$	Output. This signal is the read strobe for the I/O space of the board. It is tristated when $\overline{\text{LBACK}}$ is low and includes an internal pullup resistor.
54	IO Write	$\overline{\text{IOWR}}$	Output. This signal is the write strobe for the I/O space of the board. It is tristated when $\overline{\text{LBACK}}$ is low and includes an internal pullup resistor.
48	Memory Read	$\overline{\text{MEMRD}}$	Output. This signal is the read strobe for the memory space of the board. It is tristated when $\overline{\text{LBACK}}$ is low and includes an internal pullup resistor.
49	Memory Write	$\overline{\text{MEMWR}}$	Output. This signal is the write strobe for the memory space of the board. It is tristated when $\overline{\text{LBACK}}$ is low and includes an internal pullup resistor.
55	Read ID Low	$\overline{\text{RDIDL}}$	Output. This active low output is used to externally enable the low byte of the card ID onto the Micro Channel data bus.
56	Read ID High	$\overline{\text{RDIDH}}$	Output. This active low output is used to externally enable the high byte of the card ID onto the Micro Channel data bus.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
3,4,6 7,8,9 11,12	Data Bus	D7-D0	Input/Output. An 8-bit data bus used to access the POS and I/O registers of the MCI94C18A device. It is connected to the lower byte of the Micro Channel data bus via a transceiver. These pins have internal pullup resistors.
2	Direction	DIR	Output. This signal is used to control the direction of the data bus transceiver. A low level indicates data flow from the adapter board to the Micro Channel.
5	Transceiver Enable	$\overline{\text{TREN}}$	Output. This active low output is used to enable the data bus transceiver. When in local bus arbitration mode, it is only asserted when the Micro Channel host gains access to the local bus.
25	Local Bus Request	LBREQ	Input. This active high signal is asserted by a peripheral or an on-board processor asking for control over the board local bus.
10	Local Bus Acknowledge	$\overline{\text{LBACK}}$	Output. This active low signal is asserted by the MCI94C18A to acknowledge local bus control to the requestor.
61	Channel Check Input	CHCKIN	Input. This active high signal is asserted by the peripheral to indicate an error. This signal causes $\overline{\text{CHCK}}$ to be asserted on the Micro Channel after the card has been enabled.
38,58 59,60	Interrupt Inputs	INT4-1	Input. These four signals are positive edge triggered interrupt inputs from the peripheral INT4-1 and the internal timer interrupt can be flexibly managed and presented to the $\overline{\text{IRQ4-1}}$ outputs.
17	Ready In	RDYIN	Input. This signal is used to extend wait states beyond the programmed value. A logic "0" on this pin during a waited cycle keeps the RDYOUT output low until a rising edge is detected on RDYIN. This signal is connected to an internal pull-up resistor.
MISCELLANEOUS			
34 51,68	Power Supply	VCC	+5V power supply pins.
1,18 35,52	Ground	GND	Ground pins.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
42 41	Crystal1 Crystal2	X1 X2	An external crystal is connected to these pins. If an external TTL level clock is used, it should be connected to X1 with a 390 Ohm pullup resistor; X2 must be left floating. (See Figures 22 and 23 for connection diagrams.)
43	Clock Output	CLKOUT	Output. This signal is the buffered version of the signal at X1. It is intended for general use on the adapter board.
27	No Connect	NC	Make no connection to this pin.

SYSTEM DESCRIPTION

The MCI94C18A is a general purpose Micro Channel interface circuit that supports various types of adapter board applications. In addition to integrating the basic functions of the Micro Channel interface, the MCI94C18A supports several high-level adapter board architectures. The type of system-level applications best served by the MCI94C18A are:

I/O or Memory Mapped Applications
Slave DMA Applications
Shared (Dual-Ported) Memory Applications
Master Mode DMA Applications

I/O or Memory Mapped Applications

This represents the simplest form of interface to the Micro Channel. The I/O peripheral or memory is simply mapped in the I/O or memory space of the Micro Channel's host. In this application, the MCI94C18A will be used as a Bus Interface Unit which translates the control signals of the Micro Channel into conventional read and write signals. The Programmable Wait State Generator will be used if the peripheral needs extended cycles. The POS registers will be handled by the MCI94C18A.

Besides the MCI94C18A and the peripheral, the only external circuitry required to complete an adapter board design is the POS 103 register, address decoding and latching circuitry, ID logic and a data bus transceiver.

Slave DMA Applications

This type of application will take advantage of the flexible DMA interface capabilities of the MCI94C18A. The entire DMA arbitration function is conducted by the MCI94C18A. The peripheral needs to generate a DMA Request signal when it wishes to transfer data and the MCI94C18A will generate a DMA Acknowledge signal after it gains access to the Micro Channel. The combination of hardware- and software-generated DMA requests and the ability to OR or AND these requests give the user the flexibility needed to interface to various types of DMA-based peripherals.

Shared (Dual-Ported) Memory Applications

This very popular architecture allows for the sharing of a local adapter bus between the Micro Channel and the on-board peripheral.

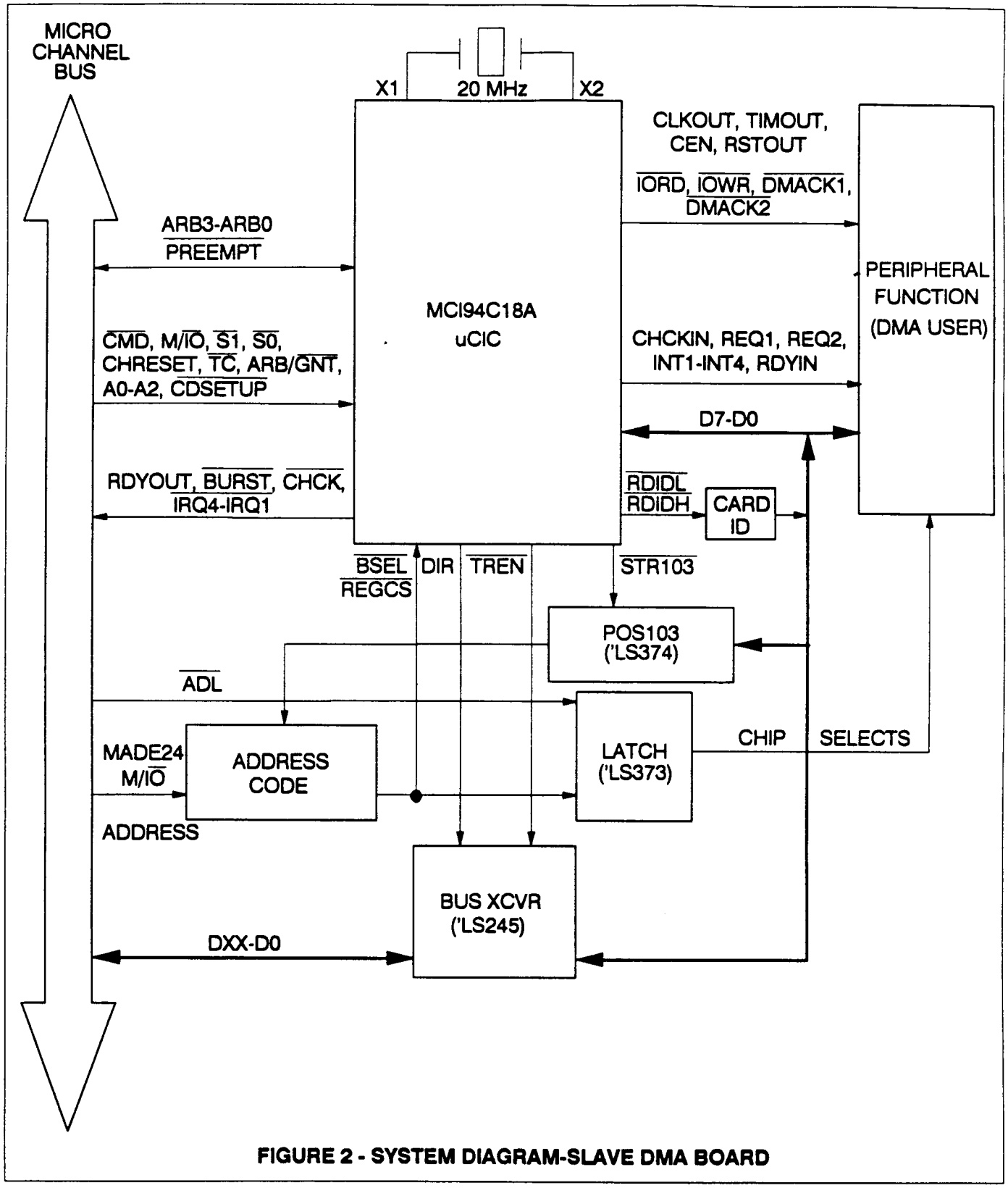


FIGURE 2 - SYSTEM DIAGRAM-SLAVE DMA BOARD

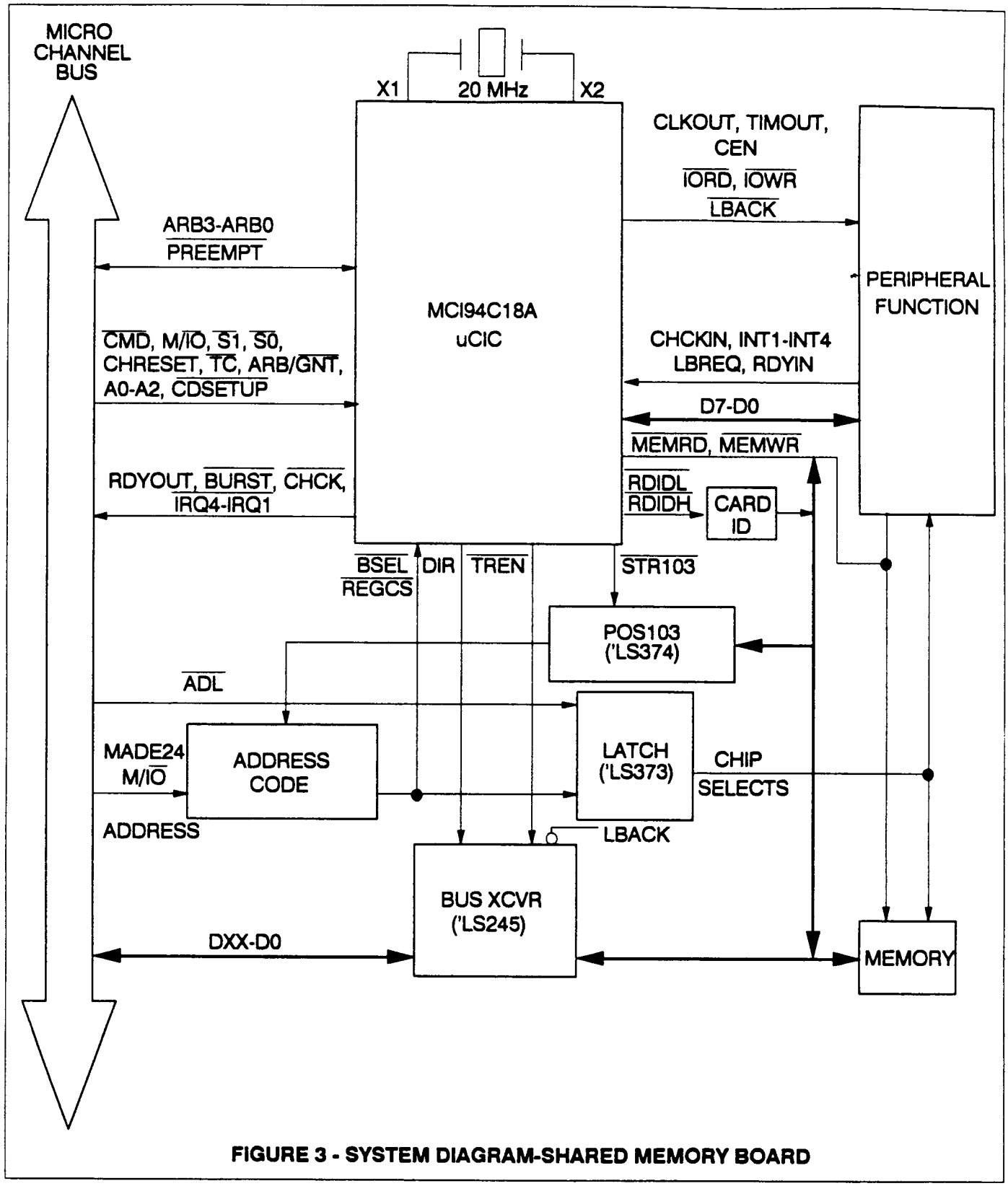


FIGURE 3 - SYSTEM DIAGRAM-SHARED MEMORY BOARD

The MCI94C18A incorporates dual port arbitration circuitry that monitors accesses from the two sides and grants cycles by resolving contentions. This architecture will be best suited for applications with intelligent peripherals such as microprocessors. Typical applications include smart modem boards, micro to mainframe communications adapters and local area network interface boards.

Master Mode DMA Applications

The MCI94C18A provides all the necessary hooks for simplifying the design of adapters using Master Mode DMA. By presenting the peripheral with a DMA Acknowledge signal as a response to DMA Request, the MCI94C18A provides an envelope during which the peripheral can enable its control lines as well as address bus onto the Micro Channel.

FUNCTIONAL DESCRIPTION

ADAPTER ID STORAGE AND RETRIEVAL

Two pins are dedicated for reading the adapter ID which is stored externally to the chip. $\overline{\text{RDIDL}}$ becomes active when $\overline{\text{CDSETUP}}$ is active during a read operation from POS address zero and $\overline{\text{RDIDH}}$ becomes active during a read operation from POS address one.

During a read ID operation, the MCI94C18A generates the DIR and $\overline{\text{TREN}}$ signals and tristates its data bus.

POS REGISTERS

The MCI94C18A provides complete support for all eight POS registers according to the Micro Channel specification. Some of these registers are implemented on the chip while others are most conveniently handled off the chip.

Internal POS Registers

POS registers 102, 104 and 105 are placed inside the MCI94C18A and control the behavior of the chip. According to the Micro Channel specification, the Card Enable bit is placed in bit 0 of the POS 102 register. Bits 7 and 6 of POS register 105 are assigned as the $\overline{\text{CHCK}}$ interrupt status bit and the optional Channel Check status indicator. POS register 102 stores the arbitration priority level of DMA channel one in addition to the synchronous $\overline{\text{BURST}}$ removal enable bit and the Local Bus Arbitration enable bit. A copy of the POS 103 register is stored inside the MCI94C18A to allow for readback. This simplifies the external circuitry. POS register 104 is dedicated for the mapping of the INT interrupts into the IRQ lines. Register 105 stores the arbitration priority level of DMA channel two and the Fairness mode bit.

External POS Registers

POS registers 100 and 101 (Board ID) are placed on the adapter board and the $\overline{\text{RDIDL}}$ and $\overline{\text{RDIDH}}$ signals are provided by the MCI94C18A to enable the reading of the board ID. The $\overline{\text{STR103}}$ signal is generated by the MCI94C18A during a write operation to POS registers 103, 106 or 107. This allows address relocation and sub-address extension to be handled conveniently off the chip.

INTERNAL I/O REGISTERS

In addition to the internal POS registers, the MCI94C18A includes six general purpose input/output registers. These registers control the operational features of the device and present status information to the host processor.

This block of six registers is selected for access when the Register Chip Select ($\overline{REGCS}$) signal is active.

This set of registers controls the number of wait states generated for memory or I/O cycles, the enabling of the two DMA channels and their mode of operation, and the enabling, status and acknowledgement of the interrupt inputs (refer to the operational description for details).

Peripheral Interface

After the card has been enabled, the MCI94C18A monitors the board select ($\overline{BSEL}$) signal which indicates accesses to the board. Upon detecting $\overline{BSEL}$, the MCI94C18A generates the memory and I/O read/write signals ($\overline{MEMRD}$, $\overline{MEMWR}$, $\overline{IORD}$, $\overline{IOWR}$) to the peripheral. Additionally, the DIR and $\overline{TREN}$ signals are generated and the data bus of the μCIC is tristated during read and write cycles to the board.

Programmable Wait State Generation

Accesses to the internal registers (both POS and I/O) of the μCIC follow the synchronous extended cycle timing where the μCIC asserts the RDYOUT signal on the falling edge of $\overline{S0}$ and $\overline{S1}$ and deasserts it on the falling edge of $\overline{CMD}$.

For access cycles to the remainder of the board's I/O and memory space, the μCIC allows for programmable wait states. The number of wait states programmed ranges from 0 to 7.

When programmed for zero wait states, the μCIC will not assert the RDYOUT signal unless the internal registers are being accessed.

When programmed for one wait state, the μCIC will induce a synchronous extended cycle. This cycle is independent of the crystal clock frequency used.

For values larger than one, the μCIC will implement asynchronous extended cycles where a bus cycle will be extended according to the number of not ready clocks programmed (2-7). Asynchronous extended cycles use the crystal clock to extend bus cycles.

Independent I/O and memory wait state programmability is provided by the μCIC. This, for example, allows for the programming of wait states for I/O devices while allowing memory to run with no wait states. In addition, the RDYIN input may be used to extend wait states beyond the programmed value. When the RDYIN input is low during a waited cycle, the RDYOUT output remains low until a rising edge is detected on RDYIN.

Programming the wait states is through I/O register zero and can be altered during normal operation.

Upon reset, the μCIC defaults to the maximum wait states. No wait states are generated prior to card enable.

Interrupt Interface

The MCI94C18A allows a flexible interrupt interface where four user interrupt signals can be mapped into four IRQ lines of the Micro Channel. The INTn signals are treated as positive edge triggered interrupts and are converted into level triggered interrupts by the μCIC. Each interrupt can be enabled or disabled via I/O register 2. Reading I/O register 3 provides interrupt status information while writing to it will acknowledge an interrupt and reset the corresponding interrupt source. The IRQ lines are disabled until the card is enabled (CEN).

The Timer output can also be used as the fifth interrupt source. It can be disabled, read and acknowledged just like the other four external interrupts.

The interrupt mapping circuitry in conjunction with the POS 104 register allows the mapping and merging of any of the INTn lines into any of the IRQn lines. INT4 and the Timer Interrupt are ORed into a common line for mapping purposes. This mapping is done during setup and stored in the POS 104 register.

THE DMA BLOCK

The MCI94C18A supports two independent DMA channels. Each channel has a DMA Request pin and a DMA Acknowledge pin on the peripheral side. As a response to DMA Request, the MCI94C18A performs the Micro Channel arbitration process and grants DMA Acknowledge to the peripheral when it wins a cycle. Therefore, the entire DMA process is handled by the μCIC and the peripheral is presented with classical DMA Request/DMA Acknowledge signals.

Since the μCIC supports two DMA channels simultaneously, the Micro Channel arbitration spirit is preserved when arbitrating between the two on-board DMA requests. In fact, two priority detection circuits (one for each channel) are provided in the μCIC and the arbitration is performed on the Micro Channel bus and not inside the μCIC. When one of the channels requests DMA while the other one is performing a burst cycle, PREEMPT will be generated and a new arbitration cycle will be forced.

Each channel has its own DMA priority level stored in the POS registers. A common fairness bit is provided in POS register 105. In addition, each channel has a DMA enable bit which enables or disables the channel, a BURST mode bit which specifies single cycle or BURST mode transfers, and a software DMA request bit which initiates DMA requests by setting a bit. These bits are stored in the I/O registers and are dynamically accessed during normal operations.

Enabling the DMA Channel

In order to properly initialize for a DMA operation, the user must program the host DMA controller prior to enabling the DMA channel in the μCIC. Note that it is the programmer's responsibility to maintain consistency between the enable bit of a particular request and the programming of the host DMA controller channel (virtual channel) associated with the arbitration level used.

A peripheral requesting the Micro Channel while the virtual DMA channel on the host DMA controller is disabled will still get the channel but no transfers will occur.

The μCIC will assist the programmer in maintaining the consistency between the programming of the host DMA controller and the enabling of a DMA channel. A DMA protection timeout on bus ownership is provided. This timeout will act whenever the bus is granted to a requestor but no transfers occur. This could result from misprogramming of the host DMA controller. The timeout protection is extremely useful for debugging purposes because it lets the system recover from a bus deadlock situation.

Since the Enable DMA bit does not get reset by Terminal Count, it allows for circular DMA operations. The way to disable DMA operations at Terminal Count is by using the AND mode between hardware and software DMA requests (refer to the Protection Timeout section).

Burst Versus Single Cycle

Bits 4 and 5 of I/O register 1 select between burst and single cycle transfer modes. When the channel which is programmed for BURST transfers is active on the Micro Channel it will assert the $\overline{\text{BURST}}$ signal for as long as the

peripheral's REQ is active and there are no preemptions by other requesters. If a preemption occurs, the μCIC will release the $\overline{\text{BURST}}$ signal and determine whether it should participate in the next arbitration cycle depending on the value of the FAIRNESS bit. In any case, the peripheral might hold its REQ active and its DMACK will be reactivated the moment the μCIC secures the channel again.

When a preemption occurs, the removal of the $\overline{\text{BURST}}$ signal may occur synchronous to the leading edge of control or asynchronously. For slave applications, bit 5 of the POS 2 register should be programmed to a logic "1" for synchronous deactivation. For master applications, this bit may be programmed to a logic "0".

If single cycle transfers are used, the μCIC will not assert the $\overline{\text{BURST}}$ signal and the peripheral will enjoy a relaxed timing requirement on withdrawing its REQ signal. The REQ should be removed before the next $\overline{\text{ARB/GNT}}$ rising edge.

Bus Master Operation

The μCIC provides all the hooks to support easy implementation of master mode application. When a bus master requests DMA services, it is responsible for generating the Micro Channel address and control signals. The μCIC will provide the DMACK signal as an envelope for bus mastership. This means that the master will enable its signals as a function of DMACK. The DMACK signal will be valid from the moment the peripheral is granted the channel until the beginning of the next arbitration cycle.

Software DMA Requests

A particularly useful feature provided by the μCIC is the ability to request DMA transfers under software control. This will be useful in various applications such as adapter boards with large RAM buffers.

The μCIC provides the option of internally ORing or ANDing software and hardware DMA requests.

ANDing the requests will protect the system from inconsistencies that may arise at Terminal Count. Regardless of whether the hardware peripheral removes its REQ signal at the end of a DMA transfer session, the fact that the Software DMA Request bit is reset on $\overline{\text{TC}}$ will guarantee that the hardware REQ signal is ignored. This will support applications where the adapter peripheral is not capable of keeping track of byte count.

ORing is useful when the peripheral determines the byte count and this number is not known by the programmer in advance (typical receive applications). The host DMA controller should be programmed for the maximum number of expected transfers or it should be configured to auto-initialize for cyclic buffer applications. ORing is also useful for emulating requests during the debugging.

The user should program the host DMA controller for the required number of transfers and then set the appropriate Software DMA Request bit in the μCIC. This bit will be cleared automatically on $\overline{\text{TC}}$ without any host or hardware intervention.

The DMACK signal will be activated when the bus is granted to the Software Requester. The Software Request bits reside in Register 5 and are read/write bits. Note that only the channel that was active when $\overline{\text{TC}}$ goes active will have its Software Request bit cleared. Upon request the μCIC defaults to the ORed mode. Software DMA supports both BURST and non-BURST applications.

Protection Timeout for BURST Mode

The DMA protection timeout duration is 32 clocks long. When a device holds the channel

without transfers taking place, the protection timer will count. If a preemption occurs and the timer has expired, the μCIC will remove the $\overline{\text{BURST}}$ signal. Note that a preemption will occur eventually due to REFRESH. When the μCIC recovers by timing out, it will clear the appropriate software DMA Request bit. Clearing this bit serves the purpose of disabling the offender provided that it was set in the AND mode. This informs the programmer of the timeout. Protection timeout does not apply for non-BURST transfers.

The value of the timeout was designed to function well for frequencies in the range of 5-20 MHz. The timeout is long enough not to expire during normal operations and short enough to prevent the host from generating an error NMI.

Local Bus Arbitration

A local bus arbitration function is included in the μCIC in order to support another popular architecture - Shared Memory.

This mode is useful for adapter boards with intelligent peripherals such as microprocessors. The local adapter bus can be shared by the adapter peripheral and the Micro Channel on an equal priority basis. The arbitration circuitry of the μCIC monitors requests for the local bus from the two sides - the Micro Channel (side A) and the on-board peripheral (side B). If the side A request is sampled first, side B is waited until side A completes its access to the local bus.

When the peripheral requests access to the local bus, it asserts LBREQ. It is granted access to the bus by asserting $\overline{\text{LBACK}}$. The $\overline{\text{MEMRD}}$, $\overline{\text{MEMWR}}$, $\overline{\text{IORD}}$, and $\overline{\text{IOWR}}$ lines are floated while $\overline{\text{LBACK}}$ is active. The Micro Channel is considered to request access to the local bus whenever it addresses the POS Registers, or after enabling the card, either the I/O Registers ($\overline{\text{REGCS}}$) or the board Memory/IO space ($\overline{\text{BSEL}}$).

The arbitration function can be described as follows:

1. Micro Channel cycle first.
   LBREQ is asserted next.
   An asynchronous extended Micro Channel cycle takes place.
   RDYOUT is negated.
   $\overline{\text{LBACK}}$ is asserted after the Micro Channel cycle is completed.
   $\overline{\text{LBACK}}$ is de-asserted after LBREQ goes inactive.

2. Peripheral cycle first.
   LBREQ is asserted.
   A Micro Channel cycle starts but it is waited (by negating RDYOUT).
   DIR and $\overline{\text{TREN}}$ remain inactive.
   $\overline{\text{LBACK}}$ is de-asserted after LBREQ goes inactive.
   $\overline{\text{TREN}}$ is activated, DIR is enabled and the control lines are driven. (Note that RDYOUT stays active for the programmed number of clocks starting from this moment.)

Upon reset, the MCI94C18A defaults to the non-arbiter mode. It can be programmed to the local bus arbitration mode by setting the LBARB bit in the POS 102 register.

Simultaneous accesses to the local bus are resolved by the arbitration circuitry.

The Programmable Timer

A programmable timer is provided that is able to generate baud rates as well as interrupts. The timer is made up of an eight-bit upcounter starting at the value programmed in the I/O register 4 and wrapping around at the count of 255. On wrap-around, the counter is reloaded with a new count value if it was reprogrammed, and generates an interrupt if enabled to do so. The TIMOUT pin will toggle every time the count reaches 255.

The counter runs at the rate of the crystal clock divided by 64. The lowest square wave frequency that can be achieved at TIMOUT is the clock divided by (64 * 256 * 2) by programming register 4 to 00h. The highest frequency is clock divided by (64 * 2) when I/O register 4 is programmed with FF hex.

The counter can be enabled or disabled via bit 6 of I/O register zero. The value of the counter can be read. Upon reset, the count value defaults to zero (maximum count) and the counter is disabled.

Writing a 1 into the most significant bit of I/O register 3 allows to bypass part of the counter for testability purposes. The counter will then be using its four MSBs only. This mode can be used in order to achieve TIMOUT frequencies of up to one sixteenth of the clock rate by programming register 4 to EFh.

It is recommended to disable the counter prior to accessing its register.

Clock Generation

The MCI94C18A incorporates an on-chip crystal oscillator. A parallel resonant crystal is connected to the X1 and X2 pins along with a 1.0 MOhm resistor across the crystal and two 22 pF capacitors from each node of the crystal to ground.

A TTL clock can also be used to supply the clock signal of the MCI94C18A. This is done by connecting the TTL clock to the X1 pin along with a 390 Ohm pullup resistor and leaving X2 unconnected (see Figures 22 and 23).

X1 is buffered to provide a MOS clock (CLCKOUT) that can be used by the rest of the board.

Scaling down the value of the clock will scale down the Wait State Generation circuitry if it was programmed for two clocks or more. The DMA protection timeout and the timer interrupt period are also affected by the scaling of the clock. Using a frequency of less than 20 MHz can be useful in cases where a large number of wait states are required, or in cases where the timer interrupt and timer output have very specific requirements.

Decoding Consideration

Three decoding signals are connected to the MCI94C18A, namely $\overline{\text{CDSETUP}}$, $\overline{\text{REGCS}}$, and $\overline{\text{BSEL}}$.

$\overline{\text{CDSETUP}}$ - Card Setup is connected to the $\overline{\text{CDSETUP}}$ line of the Micro Channel and serves as the chip select signal for the POS registers. It also governs the generation of the $\overline{\text{RDIDL}}$, $\overline{\text{RDIDH}}$, and $\overline{\text{STR103}}$ signals. Bus cycles to the POS registers follow the synchronous extended cycle timing.

$\overline{\text{REGCS}}$ - Is the chip select signal for the internal I/O registers of the MCI94C18A. Bus cycles to the I/O registers follow the synchronous extended cycle timing.

$\overline{\text{BSEL}}$ - This signal must be active for accesses to the memory or I/O space of the board. It is not necessary to activate $\overline{\text{BSEL}}$ for accesses to the internal I/O registers of the MCI94C18A. If included, however, accesses to the internal I/O register will be extended according to the number of wait states programmed.

These signals are internally latched on the falling edge of $\overline{\text{CMD}}$ and do not require external latching. Speedy decoding of $\overline{\text{REGCS}}$ and $\overline{\text{BSEL}}$ is recommended in order to meet the bus timing specifications.

All functions related to $\overline{\text{BSEL}}$ and $\overline{\text{REGCS}}$ are disabled until Card Enable (CEN) is set.

POS REGISTERS DESCRIPTION

POS 102 - bit 7 - LOCAL BUS ARBITRATION ENABLE
A 1 in this bit enables the local bus arbiter. When enabled, the memory and I/O wait state generation has to be set to two clocks or more. This bit defaults to 0 upon reset.

POS 102 - bit 6 - POS1026
When set, this bit changes the meaning of two control lines. $\overline{IORD}$ becomes a data strobe signal $\overline{DS}$, while $\overline{IOWR}$ becomes a R/$\overline{W}$ (direction) signal. These signals are independent of M/$\overline{IO}$ and are tristated when $\overline{LBACK}$ is low. This bit defaults to 0 upon request.

POS 102 - bit 5 - SYNCH $\overline{BURST}$
A logic "1" in this bit enables the $\overline{BURST}$ signal to be removed synchronous to the leading edge of the control signal. A logic "0" allows $\overline{BURST}$ to be removed asynchronously on $\overline{PREEMPT}$.

POS 102 - bits 4-1 - DMA CHANNEL 1 ARBITRATION LEVEL (4 bits)
This field defines the DMA arbitration level to be associated with the DMA request line REQ1. It defaults to zero upon reset.

POS 102 - bit 0 - CARD ENABLE
This bit has to be set after all other POS registers are configured. Interrupt, DMA, and wait state generation logic are disabled until the CARD ENABLE bit is set. This bit is also available at the CEN pin to allow for the disabling of external logic. Upon reset this bit is cleared.

POS 103 - EXTERNALLY IMPLEMENTED REGISTER
A typical external assignment for register 103 is the memory and I/O address relocation options. As this option is required for most applications, the $\overline{STR103}$ pin is dedicated to latch the POS byte 103 into an external latch.

The MCI94C18A stores a replica of this register for readback purposes.

POS 104 - INTERRUPT MAPPING REGISTER
The mapping bits specify the $\overline{IRQn}$ pin to be associated with each INTn interrupt input. Interrupts can be merged into a pin by assigning them the same mapping. All bits default to 0 (all interrupts merged into $\overline{IRQ1}$) upon reset.

INTxMAP	MAPPED TO PIN
00	$\overline{IRQ1}$
01	$\overline{IRQ2}$
10	$\overline{IRQ3}$
11	$\overline{IRQ4}$

POS 105 - bit 7 - CHANNEL CHECK BIT ($\overline{CHCK}$)
This bit is asserted low when the CHCKIN pin is high. The $\overline{CHCK}$ output pin reflects the value of the $\overline{CHCK}$ bit.

The $\overline{CHCK}$ bit is polled and cleared by the error handler routine. It defaults to high on reset. This bit must be written high during normal setup. Writing a low will generate a channel check interrupt. In order to reset the $\overline{CHCK}$ interrupt, a one must be written to this bit after the CHCKIN pin has been reset.

POS 105- bit 6 - OPTIONAL CHANNEL CHECK STATUS
This is a one-bit memory used as the channel check status indicator. It is typically written during setup to indicate the presence of a channel check status word on the adapter. This information is used by the error handling routines in case of $\overline{CHCK}$ activation.

POS 105 - bit 5 - ZERO
This bit is not used and must be 0.

POS 105 - bit 4 - FAIRNESS BIT
A 0 in this bit position informs the DMA channel being preempted to participate in the following arbitration cycle. A one, on the other hand, instructs the DMA controller to wait until after all other bus requesters gain the bus. This bit defaults to 1 on reset.

POS 105 - bits 3-0 - DMA CHANNEL 2 ARBITRATION LEVEL (4 bits)
This field defines the DMA arbitration level to be associated with the DMA request line REQ2. Upon reset, it defaults to 0.

I/O REGISTERS DESCRIPTION

REGISTER 0 - bit 7 - SOFTWARE RESET
This is a one-bit output port. It is typically used as a software reset. A 1 in this bit activates the RSTOUT pin. It does not reset the MCI94C18A internal circuitry. This bit defaults to 0 upon reset.

REGISTER 0 - bit 6 - ENABLE TIMER
A 1 enables the programmable TIMER used to produce a square wave on the TIMOUT pin and to generate internal interrupts. This bit defaults to 0 upon reset.

REGISTER 0 - bits 5-3 - NUMBER OF I/O WAIT STATES (3 bits)
Defines the behavior of the RDYOUT pin for I/O accesses (pin $\overline{BSEL}$ = 0 and pin M/$\overline{IO}$ =0) according to the table below.

REGISTER 0 - bits 2-0 - NUMBER OF MEMORY WAIT STATES (3 bits)
Defines the behavior of the RDYOUT pin for memory accesses (pin $\overline{BSEL}$ = 0 and pin M/$\overline{IO}$ = 1 according to the table below.

PROGRAMMED VALUE	BEHAVIOR
7	no wait state - basic cycle
6	1 wait state - synchronous extended cycle
5	asynchronous not ready - 2 clocks
4	asynchronous not ready - 3 clocks
3	asynchronous not ready - 4 clocks
2	asynchronous not ready - 5 clocks
1	asynchronous not ready - 6 clocks
0	asynchronous not ready - 7 clocks

REGISTER 1 - bits 7,6 - ZERO
These bits are not used and must be 0.

REGISTER 1 - bits 5,4 - ENABLE BURST 1, ENABLE BURST 2 (2 bits)
Each enable burst bit is programmed to determine whether the associated DMA channel will perform burst transfers (bit set to 1) or it will relinquish the bus and re-arbitrate before each transfer (bit set to 0). Default to 0.

REGISTER 1 - bits 3,2 - ZERO
These bits are not used and must be 0.

REGISTER 1 - bits 1,0 - ENABLE DMA 1, ENABLE DMA 2 (2 bits)
Each of these bits is used to enable the corresponding DMA channel. They default to 0 (channel disabled) upon reset.

REGISTER 2 - bit 7 - ZERO
This bit is not used and must be 0.

REGISTER 2 - bits 6-2 - INTERRUPT ENABLE BITS (5 bits)
These bits are used to individually enable/disable each of the five interrupt sources. When the enable bit is set to 0 the corresponding interrupt input is prevented from causing an IRQ on the Micro Channel. A rising edge on the INT pin will still be stored, and its value can be polled using the interrupt status register. A 1 in the enable bit allows the stored interrupt onto the IRQ line determined by the mapping bits. These five bits default to 0 upon reset.

REGISTER 2 - bits 1,0 - ZERO
These bits are not used and must be 0.

REGISTER 3 (WRITE) - bit 7 - TIMER TEST BIT
This bit, when 1, scales down the timer to be a four-bit counter. The most significant four bits may be used to achieve fast frequencies on the TIMOUT pin.

REGISTER 3 (WRITE) - bits 6-2 - INTERRUPT ACKNOWLEDGE BITS (5 bits)
These bits are used to acknowledge each of the stored interrupt sources. Writing a 1 in any of the acknowledge bits clears the corresponding stored interrupt. Following interrupts will be normally stored.

REGISTER 3 (WRITE) - bits 1,0 - ZERO
These bits are not used and must be 0.

REGISTER 3 (READ) - bit 7 - ANY INTERRUPT
This bit represents the OR function between the five interrupt sources. It is typically used for fast software polling loops.

REGISTER 3 (READ) - bits 6-2 - INTERRUPT STATUS BITS (5 bits)
This register reflects the value of each stored interrupt. It can be used for polling purposes or to identify the source when the interrupts are merged.

REGISTER 3 (READ) - bits 1,0 - ZERO
These bits are read as 0s.

REGISTER 4 (WRITE) - TIMER COUNT (8 bits)
This register is written with the starting value of the up counter. Loading occurs when the count reaches the count of 255. The count is programmed as (255 minus the desired value).

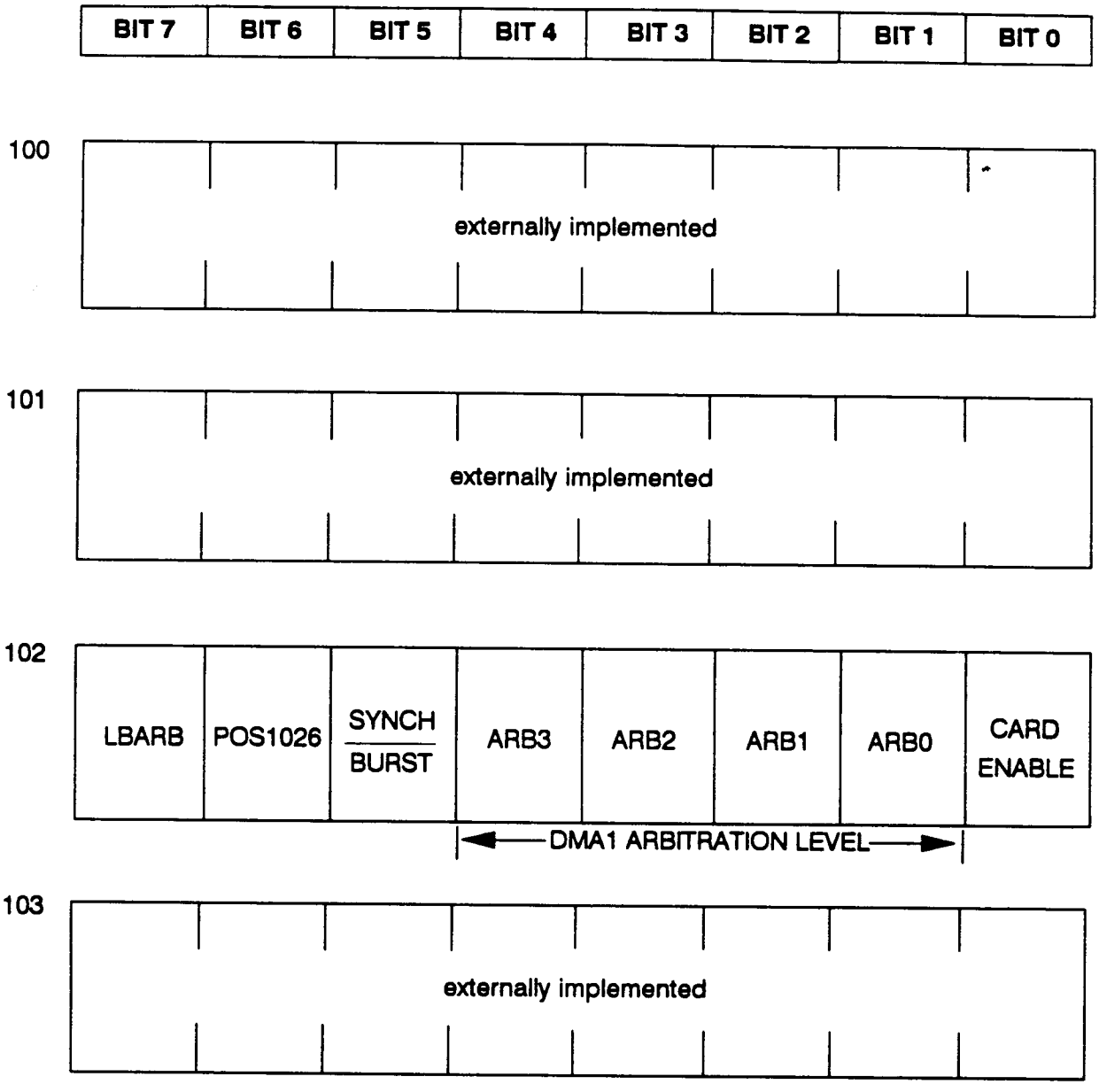
REGISTER 4 (READ) - TIMER COUNT (8 bits)
Reading this register provides the present count.

REGISTER 5 - bits 7,6 - AND/OR2, AND/OR1 (2 bits)
Each bit specifies whether the software and hardware DMA requests of the corresponding channel are ANDed or ORed. The requests are ANDed when the bit is set to 1. These bits default to 0 upon reset or card disable.

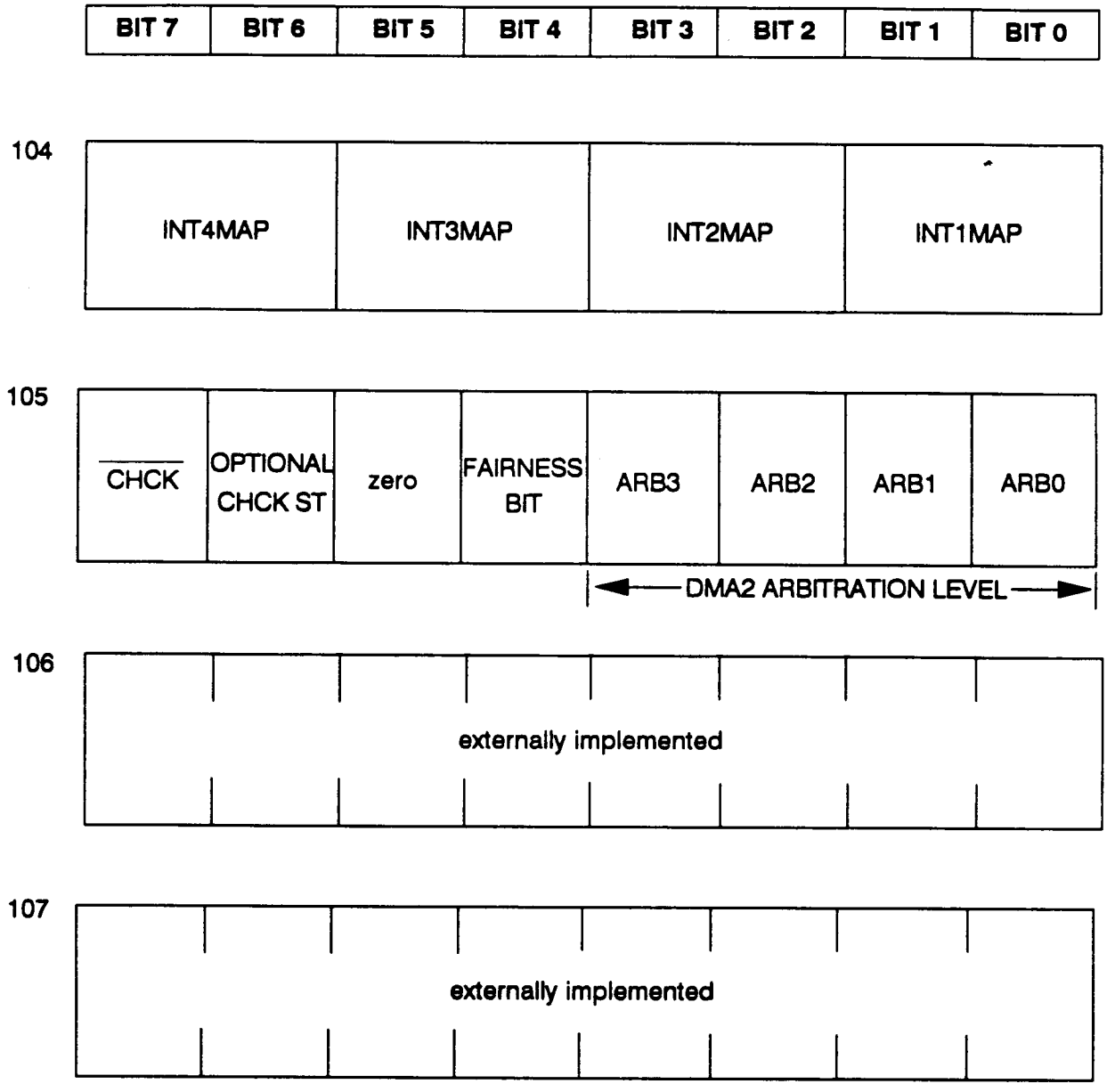
REGISTER 5 - bits 5-2 - ZERO
These bits are not used and must be 0.

REGISTER 5 - bits 1,0 - S/W REQ2, S/W REQ1 (2 bits)
Each software request is associated with a DMA channel. Writing a 1 initiates a software DMA request on the corresponding channel. Each bit will be automatically reset by a terminal count ($\overline{TC}$ pin going low) while its channel has the bus. A software DMA request can be withdrawn by writing a 0 into these bits. These bits default to 0 upon reset.

POS REGISTERS



POS REGISTERS (continued)



I/O REGISTERS

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

0 - Read/Write*

Software Reset	Enable Timer	IOW2	IOW1	IOW0	MW2	MW1	MW0

I/O wait states | Memory wait states

1 - Read/Write

zero	zero	Enable Burst 2	Enable Burst 1	zero	zero	Enable DMA 2	Enable DMA 1

2 - Read/Write

zero	TIMER INTERRUPT	INT4	INT3	INT2	INT1	zero	zero

interrupt enable bits

3 - Write

Timer Test Bit	TIMER INTERRUPT	INT4	INT3	INT2	INT1	zero	zero

interrupt acknowledge bits

I/O REGISTERS (continued)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

3 - Read

Any Interrupt	TIMER INTERRUPT	INT4	INT3	INT2	INT1	zero	zero

interrupt status bits

4 - Read/Write

T7	T6	T5	T4	T3	T2	T1	T0

timer count bits

5 - Read/Write

AND/OR DMA2	AND/OR DMA1	zero	zero	zero	zero	S/W REQ2	S/W REQ1

*The number of wait states is programmed as (7-desired number of wait states).
The zero bits are reserved for future enhancements. Must be written zero.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -55°C to +150°C
Leading Temperature (Soldering, 10 sec) . . . . . +300°C
Positive voltage on any pin WRT (with respect to ground) . . . . . V_{CC} + 0.3V
Negative voltage on any pin WRT (with respect to ground) . . . . . -0.3V
Maximum V_{CC} . . . . . +7.0V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

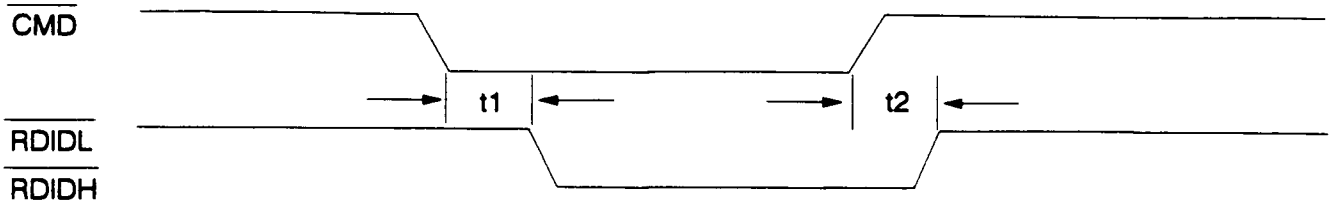
CAPACITANCE T_A = 25°C; f_c = 1 MHz; V_{CC} = 0V
Output and I/O pins capacitive load specified as follows:

PARAMETER	SYMBOL	LIMITS			UNIT	CONDITIONS
		MIN	TYP	MAX		
Group 1: $\overline{\text{TREN}}$, $\overline{\text{LBACK}}$, $\overline{\text{RDIDH}}$, $\overline{\text{RDIDL}}$, D[7-0], $\overline{\text{STR103}}$, CEN, CLKOUT, RSTOUT, $\overline{\text{IORD}}$, $\overline{\text{MEMRD}}$, $\overline{\text{IOWR}}$, $\overline{\text{MEMWR}}$, $\overline{\text{DMACK1}}$, $\overline{\text{DMACK2}}$, TIMEOUT, DIR	C_{OUT1}			100	pF	
Group 2: $\overline{\text{PREEMPT}}$, ARB3-0, $\overline{\text{BURST}}$	C_{OUT2}			200	pF	
Group 3: RDYOUT, $\overline{\text{IRQ[4-0]}}$, $\overline{\text{CHCK}}$	C_{OUT3}			240	pF	

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

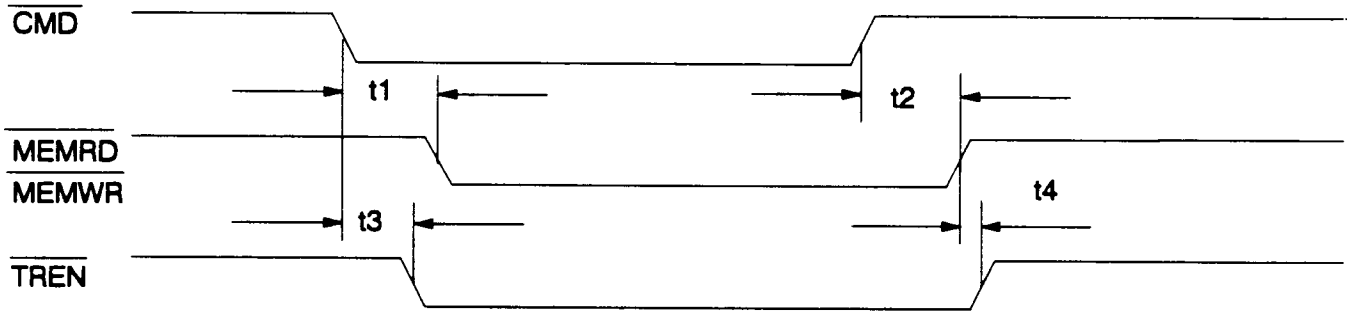
PARAMETER	SYMBOL	LIMITS			UNIT	CONDITIONS
		MIN	TYP	MAX		
Low Input Voltage	V_{IL}			0.8	V	
High Input Voltage	V_{IH}	2.0			V	
Low Output Voltage	V_{OL}			0.4	V	Note 1
High Output Voltage	V_{OH}	2.4			V	
Leakage	I			±10	μA	
Input Capacitance	C_{IN}			5	pf	
V_{CC} Supply Current	I_{CC}		25		mA	@20 MHz

NOTE 1: Pin current drive capabilities
Group 1 = 24 mA (ARB0-3, $\overline{\text{PREEMPT}}$, $\overline{\text{BURST}}$, $\overline{\text{IRQ[4-1]}}$)
Group 2 = 12 mA (D[7-0], RDYOUT, $\overline{\text{CHCK}}$)
Group 3 = 4 mA all other output or bidirectional pins



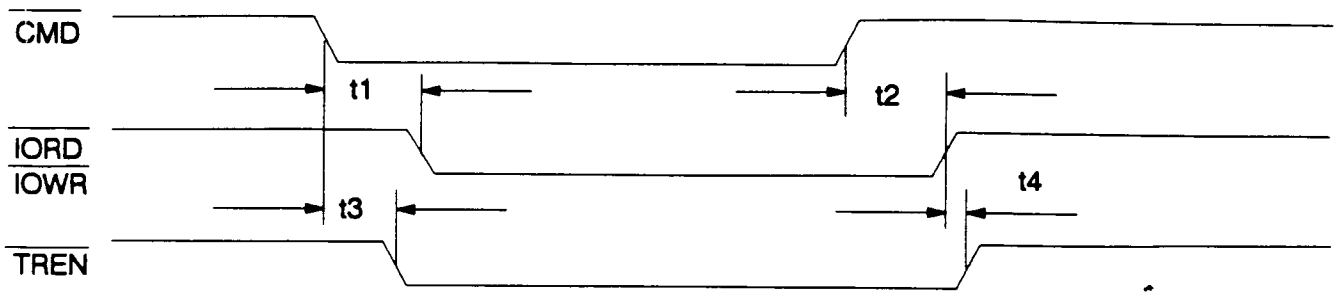
	MIN	TYP	MAX
t1			40 ns
t2			30 ns

FIGURE 4 - READ ID TIMING



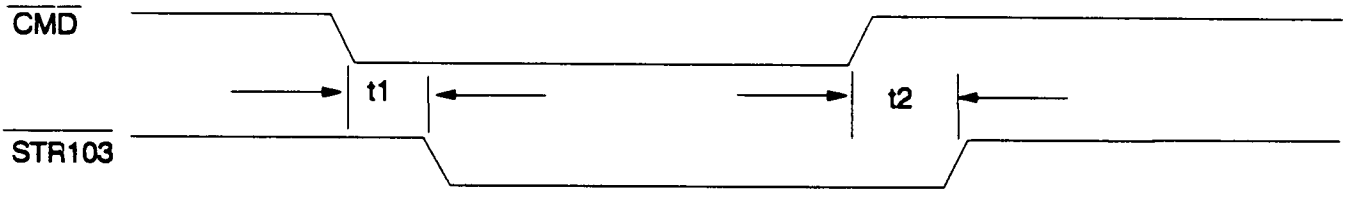
	MIN	TYP	MAX
t1		35 ns	
t2		18 ns	
t3		25 ns	
t4	10 ns		

FIGURE 5 - MEMORY READ, MEMORY WRITE TIMING



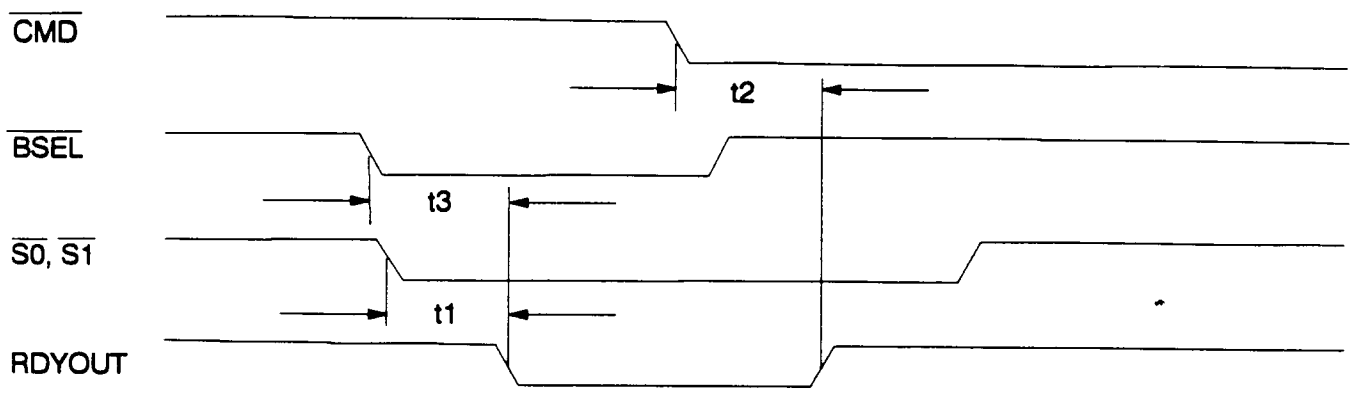
	MIN	TYP	MAX
t1		35 ns	
t2		18 ns	
t3		25 ns	
t4	10 ns		

FIGURE 6 - IO READ, IO WRITE TIMING



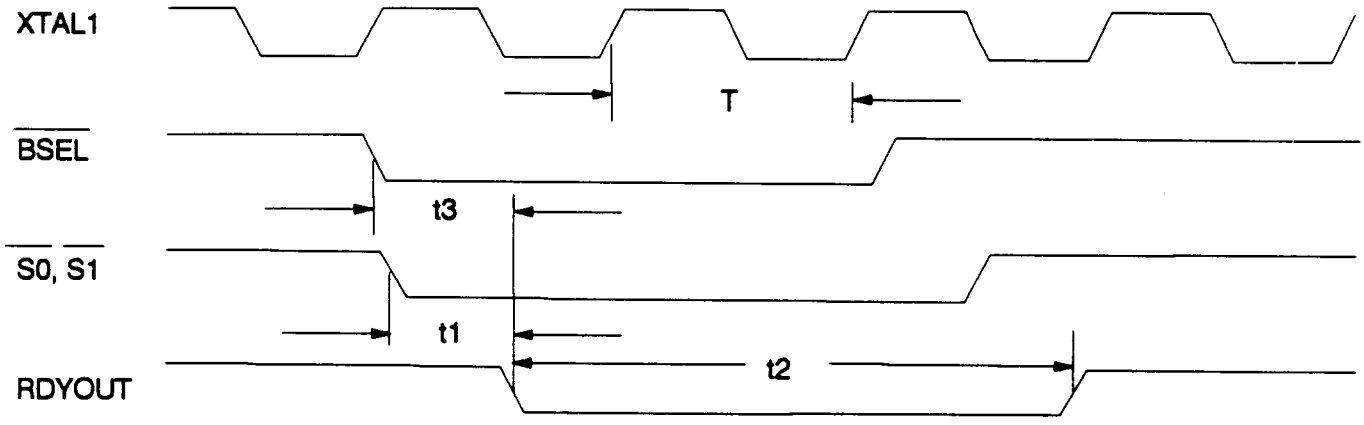
	MIN	TYP	MAX
t1			30 ns
t2			18 ns

FIGURE 7 - STROBE 103 TIMING



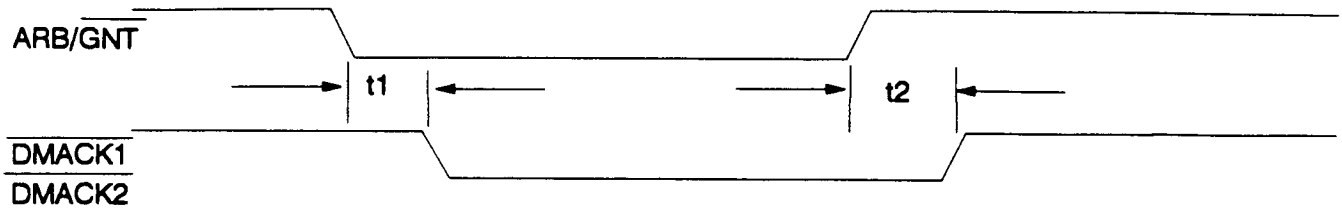
	MIN	TYP	MAX
t1			28 ns
t2			20 ns
t3			30 ns

FIGURE 8 - SYNCHRONOUS READY TIMING



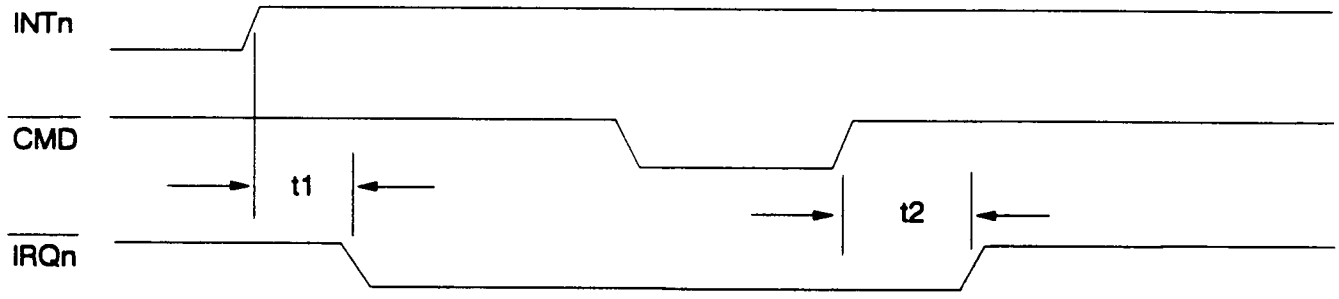
	MIN	TYP	MAX
t1			28 ns
t2	nT		(n + 1)T + 50 ns
t3			30 ns

FIGURE 9 - ASYNCHRONOUS READY TIMING



	MIN	TYP	MAX
t1			40 ns
t2			30 ns

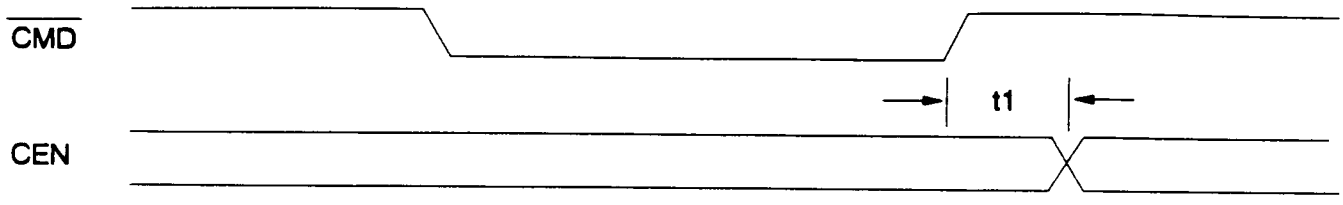
FIGURE 10 - DMA ACKNOWLEDGE TIMING



NOTE - WRITE INTERRUPT ACKNOWLEDGE CYCLE

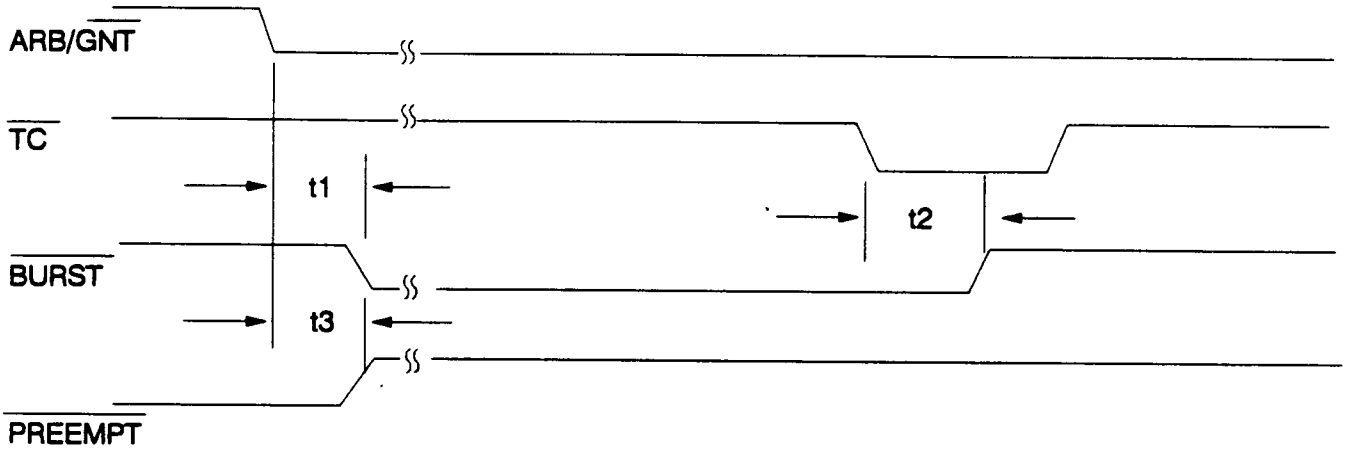
	MIN	TYP	MAX
t1			100 ns
t2			100 ns

FIGURE 11 - INTERRUPT TIMING



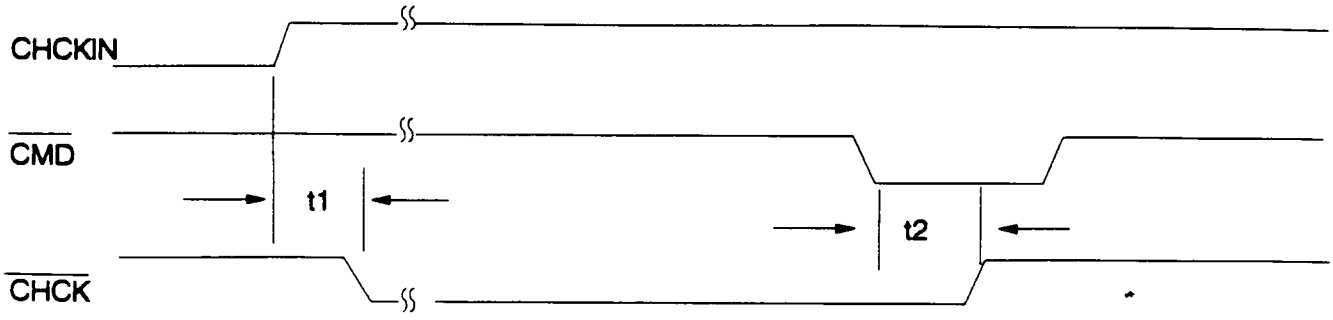
	MIN	TYP	MAX
t1			100 ns

FIGURE 12 - CARD ENABLE TIMING



	MIN	TYP	MAX
t1			40 ns
t2			25 ns
t3			40 ns

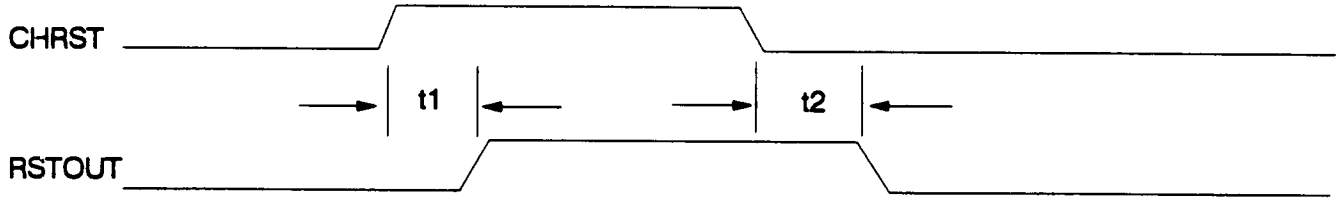
FIGURE 13 - DMA GRANT TIMING



NOTE: WRITE TO CHANNEL CHECK LATCH

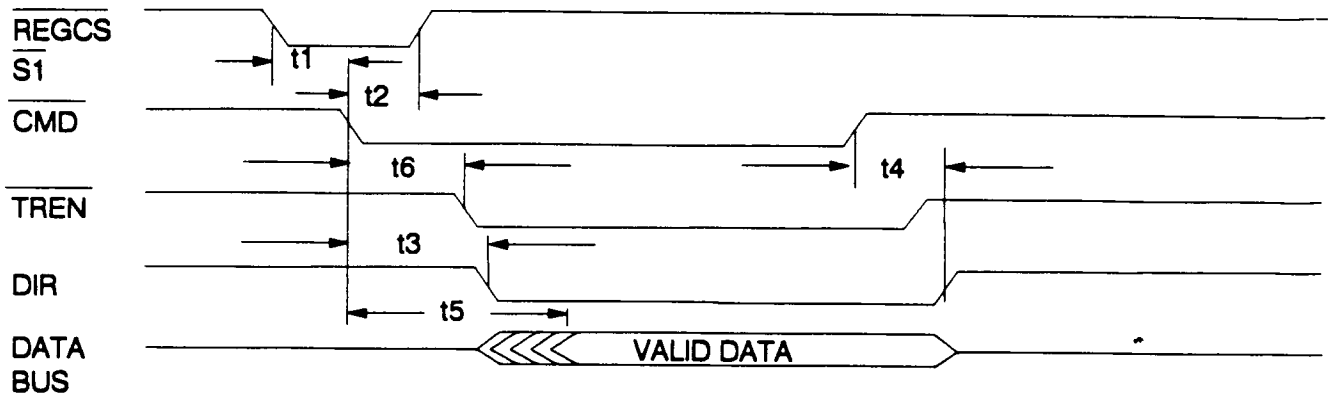
	MIN	TYP	MAX
t1			100 ns
t2			100 ns

FIGURE 14 - CHANNEL CHECK TIMING



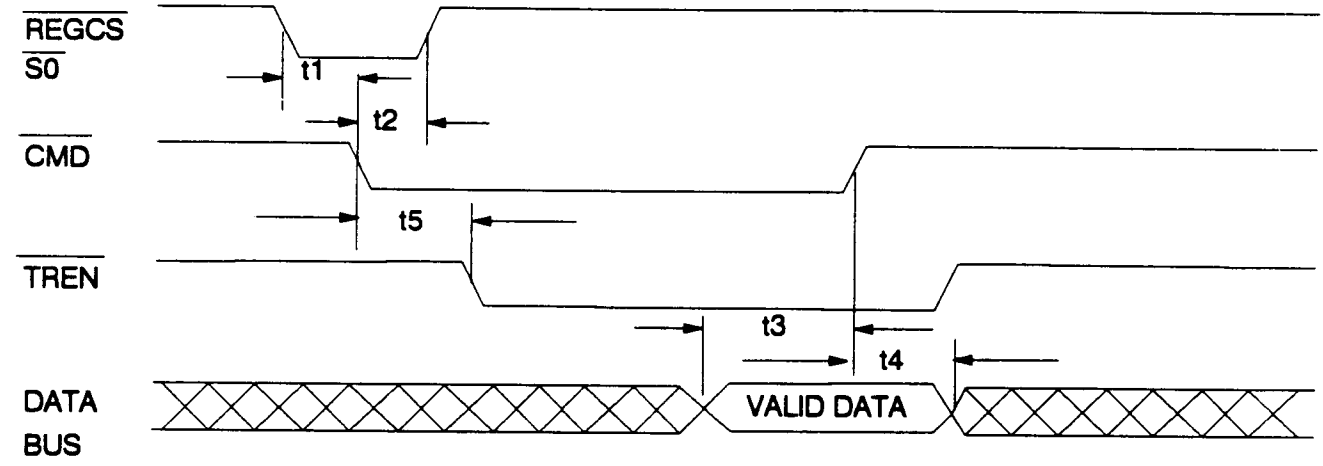
	MIN	TYP	MAX
t1			100 ns
t2			100 ns

FIGURE 15 - RESET OUT TIMING



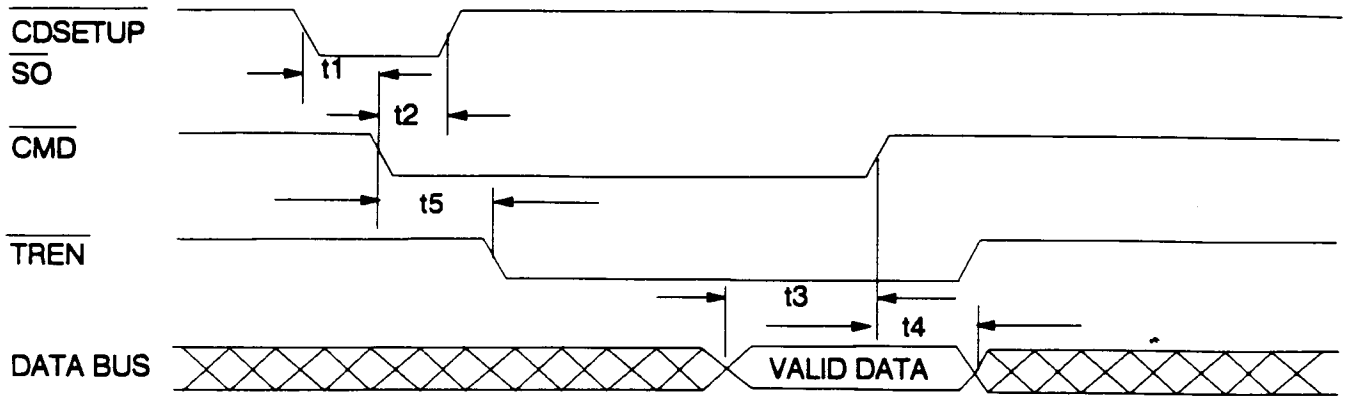
	MIN	TYP	MAX
t1	20 ns		
t2	20 ns		
t3		30 ns	
t4		30 ns	
t5		60 ns	
t6		25 ns	

FIGURE 16 - READ REGISTER TIMING



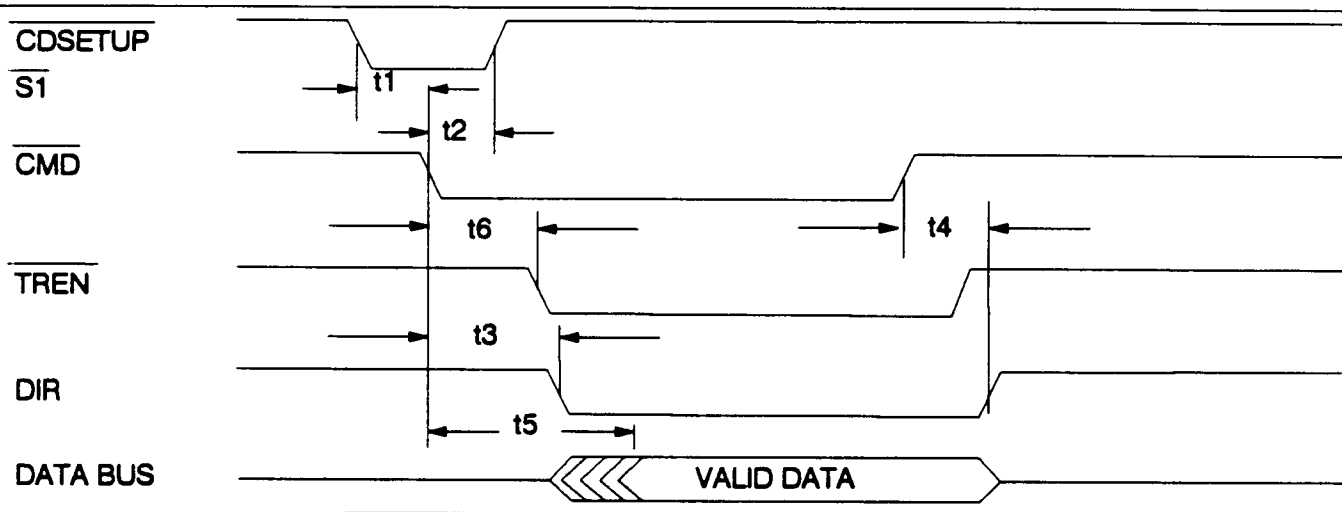
	MIN	TYP	MAX
t1	20 ns		
t2	20 ns		
t3	30 ns		
t4	0 ns		
t5		25 ns	

FIGURE 17 - WRITE REGISTER TIMING



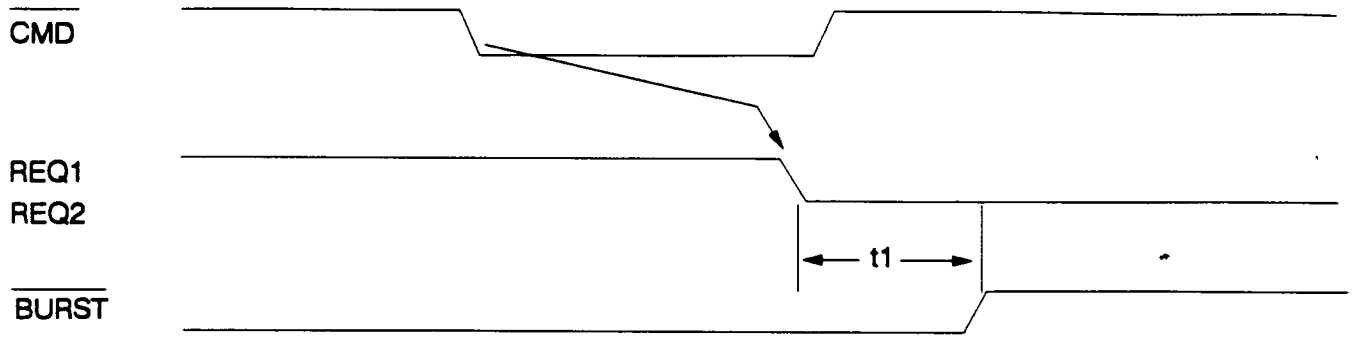
	MIN	TYP	MAX
t1	20 ns		
t2	20 ns		
t3	30 ns		
t4	0 ns		
t5		25 ns	

FIGURE 18 - WRITE POS TIMING



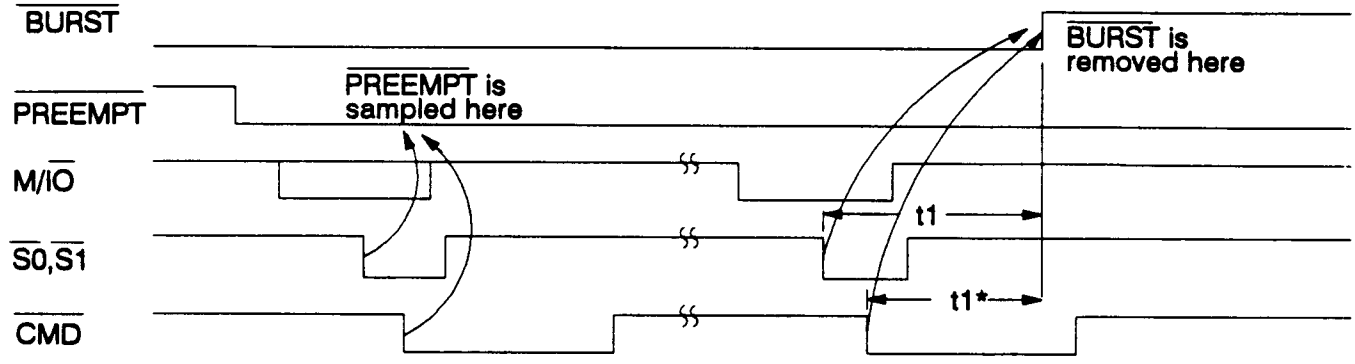
	MIN	TYP	MAX
t1	20 ns		
t2	20 ns		
t3			30 ns
t4			30 ns
t5			60 ns
t6			25 ns

FIGURE 19 - READ POS TIMING



	MIN	TYP	MAX
t1			35 ns

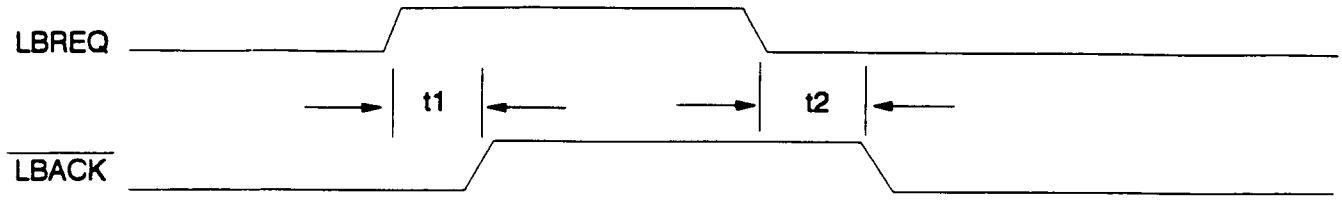
FIGURE 20 - BURST DMA TIMING



	MIN	TYP	MAX	COMMENTS
t1			40 ns	When using default cycles, PREEMPT is first internally sampled by the leading edge of S0, S1 before BURST removal.
t1*			40 ns	When using extended cycles, PREEMPT is first internally sampled by the leading edge of CMD before BURST removal.

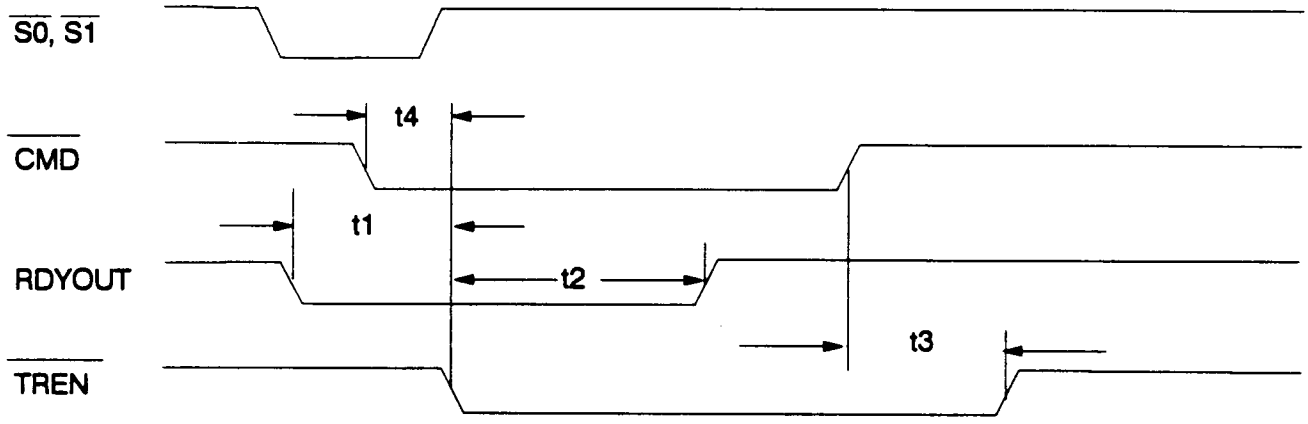
Note 1: This timing diagram only applies when POS 102 bit 5 is set to logic "1".
Note 2: t1 applies only when using default cycles.
t1* applies only when using extended cycles.

FIGURE 20A - SYNCHRONOUS REMOVAL OF BURST



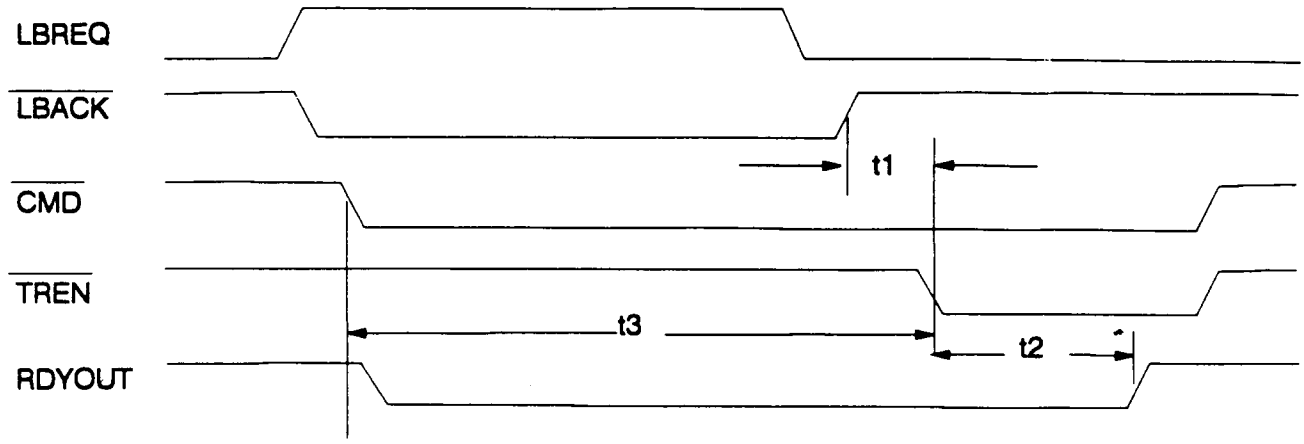
	MIN	TYP	MAX
t1	(1/2) CLK		(3/2) CLK + 30 ns
t2	(1/2) CLK		(3/2) CLK + 30 ns

FIGURE 21 - LOCAL BUS ARBITRATION PERIPHERAL HIT CYCLE



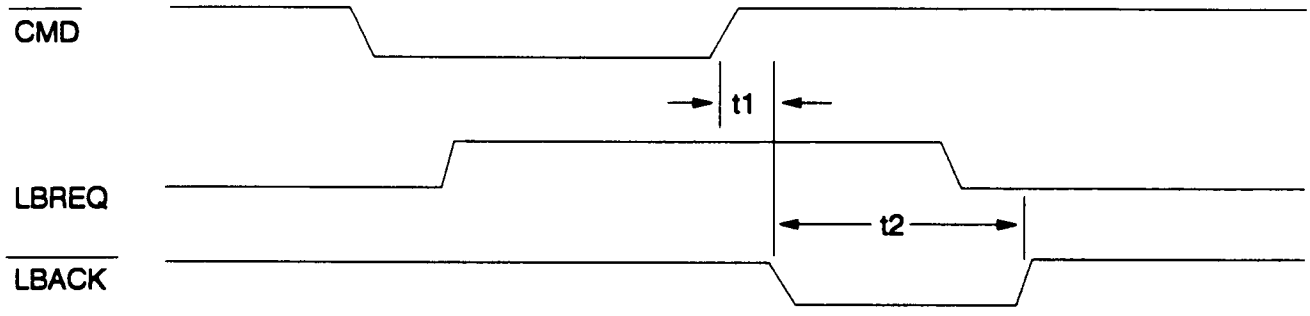
	MIN	TYP	MAX
t1	CLK/2		3CLK/2 + 30 ns
t2		n + 1 CLK	
t3			25 ns
t4			25 ns

FIGURE 22 - LOCAL BUS ARBITRATION HOST ONLY CYCLE



	MIN	TYP	MAX
t1	CLK/2		1 CLK
t2		n + 1 CLK	
t3			25 ns

FIGURE 23 - LOCAL BUS ARBITRATION HOST MISS CYCLE



	MIN	TYP	MAX
t1	1 CLK		2 CLK
t2	1/2 CLK		3/2 CLK + 30 ns

FIGURE 24 - LOCAL BUS ARBITRATION PERIPHERAL MISS CYCLE

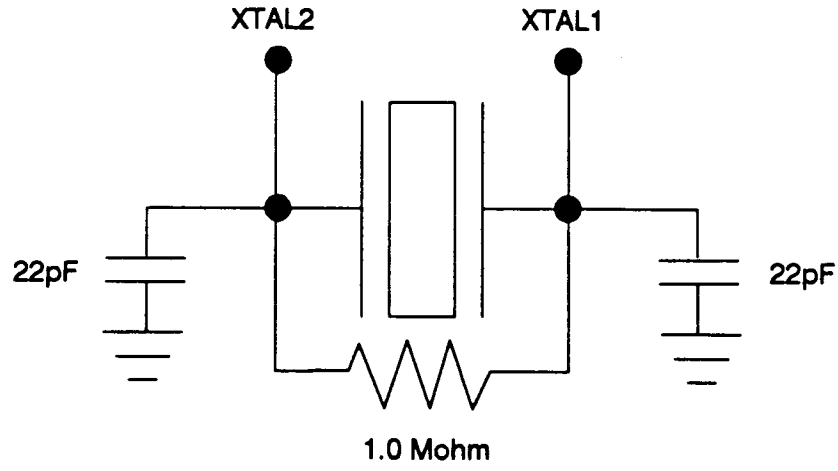


FIGURE 25 - CONNECTION DIAGRAM FOR PARALLEL RESONANT CRYSTAL

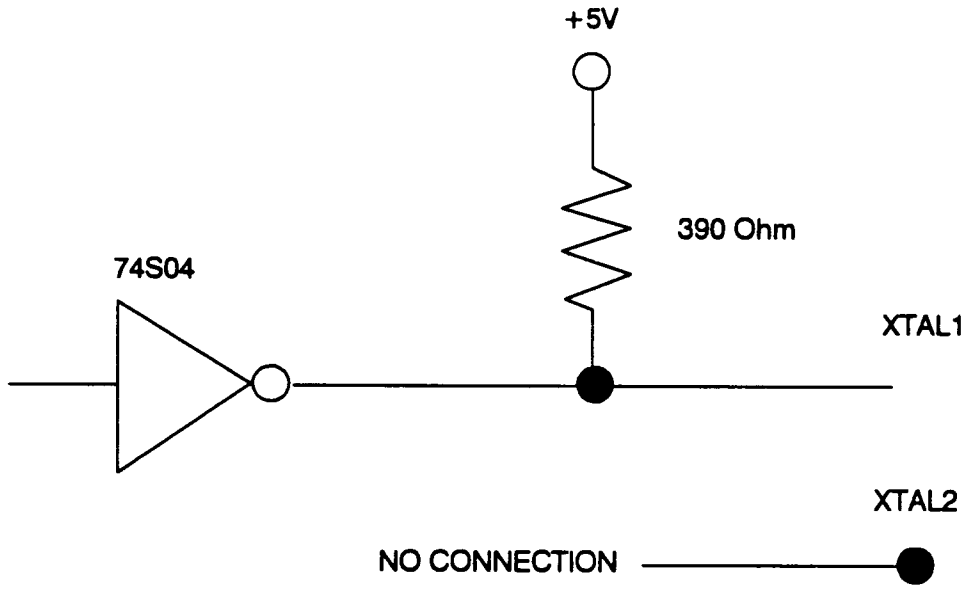


FIGURE 26 - RECOMMENDED EXTERNAL TTL CLOCK CONNECTION

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