National Semiconductor

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SCX microCMOS Gate Array Family Application Guide

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1.0 General Description

National Semiconductor's CMOS gate array Family utilizes a dual layer metal technology (microCMOS) to achieve operating speeds similar to Schottky-TTL with the inherent lower power consumption of standard CMOS integrated circuits. The SCX6200-Series Family is available in 2-micron drawn geometry with a 1.4 micron effective channel length. The range of complexity is currently from 600 to 6000 gates. The gates are arranged in cells. Each cell has the equivalent of three 2-input NAND or NOR gates. All outputs have the ability to drive 10 LSTTL loads. All inputs have high noise immunity and are protected from static discharge.

National Semiconductor supports gate array designs with a variety of user/vendor interfaces. This ranges from producing arrays from the user's schematic to accepting databases for mask generation. A large dedicated staff of gate array professionals is available to help the user determine the most efficient and cost effective way to interface on any given design.

The design automation tools include workstation or text file entry (for schematic capture), logic and timing verifiers to substantiate the actual design, fault grading analysis to gauge testability and a large selection of macros (hardware and software) to speed and simplify the design.

2.0 Product Features

- Latch-up proof, state-of-the-art 2-micron (drawn) dual-metal silicon-gate microCMOS technology
- Ultra-high performance—1 ns typical gate delays
- Available from 600 gates to 6000 gates
- CMOS power dissipation
- All inputs and I/Os protected from over-voltage and latch-up
- Full design automation support
  - — Schematic capture
  - — Logic simulator with timing information
  - — Fault grading
- Multiple power rail pin connections
- Multiple packaging options in ceramic, plastic, leaded and leadless
- Pin counts to 172
- Military performance
- Alternately sourced
- Complete hardware/software macrocell libraries
- On-chip self-test capability (6.0K only)
- 100% auto-place-and-route at 90% utilization
- Design automation system supported on mainframe and workstations

2.0.1 Enhanced Product Features

The SCX6200-series gate array family is available in seven device increments from 600 to 6000 gates. The initial members of the 2-micron family consist of SCX6212, 6225 and 6260. Today it has been enhanced and expanded to include the 6244, 6232, 6218 and 6206. These enhanced devices contain several new features as follows:

- **Flexible I/O Structure** - The I/O buffer has been enhanced to handle multiple functions including:
  - — Low-drive inputs compatible with TTL, CMOS or Schmitt Trigger
  - — High-drive (Clock Driver) inputs compatible with TTL, CMOS or Schmitt Trigger
  - — Output compatible with TTL and CMOS and configurable as TRI-STATE®, non TRI-STATE or Open Drain
  - — Outputs selectable for 1, 2 or 4 mA drive
  - — Bidirectional inputs/outputs
  - — Oscillator macros to drive 1, 2 or 4 mA
  - — Separate power supply traces for output drivers improve noise immunity

The input capacitance loading of the output drivers has also been reduced to enhance the overall circuit performance.

- **Selectable Output Drive Capability** - The enhanced I/O structure now makes it possible to offer a variety of output drives for any given I/O location. Through implementation of I/O macro options, users can select their output drives in 1, 2 or 4 mA for each output buffer.
- **Parallel I/O Buffers for High Drives** - By means of special I/O macros, output drive current in excess of 4 mA can be achieved by paralleling I/O buffers without losing the input functions. For example, to achieve 24 mA, six 4 mA I/O buffers need to be paralleled up; through use of the special macros, one pin is needed to implement the output which can be bidirectional while 5 pins can still be used as inputs.
- **Dedicated Multiplexed D-Flip/Flops** - Incorporated into the internal array core is a number of dedicated multiplexed D-flip/flops. These flip/flops have been designed to achieve significant system speed improvement over a logically eqivalent macro function while minimizing silicon space to implement. They are ideal for scan path design techniques as well as registers and counters.

Array Name	Equivalent 2-Input Gates (Note 1)	Input Cells	I/O Cells	Signal Pins	Test Pin	V_{DD} Pins	V_{SS} Pins
SCX6206	600	8	40	48	1	4	4
SCX6212	1260	17	42	59	1	4	4
SCX6218	1806	3	70	73	1	8	8
SCX6225	2430	12	76	88	1	6	6
SCX6232	3162	3	101	104	1	8	8
SCX6244	4380	3	110	113	1	8	8
SCX6260 (Note 2)	6090	66	88	154	6	8	8

Note 1: Input and I/O cells are not considered part of the internal cell count.

Note 2: Advanced Architecture with additional 2500 gates for on-chip self-test capability.

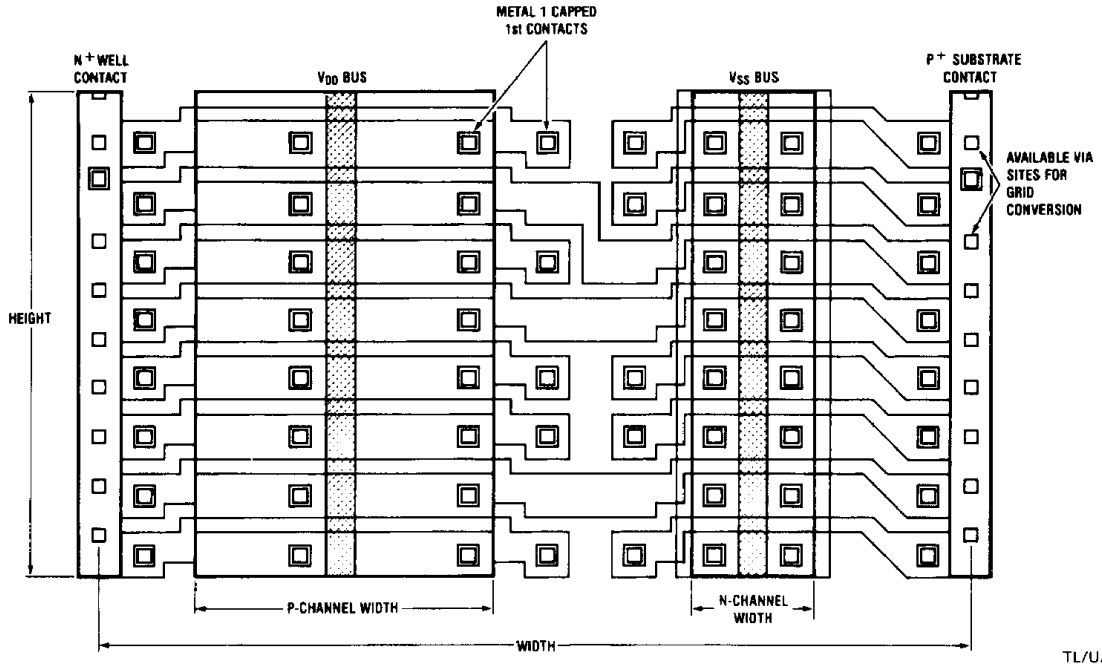

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FIGURE 1. Cell

2.1 microCMOS PROCESS AND CIRCUIT PERSONALIZATION

The microCMOS process developed by National is based on P-type starting material, N-well technology and oxide isolation. After the basic transistors are formed (in their respective cells), two separate layers of metalization (M1 and M2) are placed on the wafers.

The processing steps and tooling requirements for all the wafers up to the metal layers are common and fixed. Circuit patterns—called "options"—are defined by the two metal layers and the VIAs. In this way, the user's design (or circuit personality) is imposed on the wafer.

All SCX gate arrays in the family use the same basic internal cell. There are eight pairs of N and P-type MOS transistors in each cell (see *Figure 1*). The power and ground lines (V_{DD} and V_{SS} buses, respectively) run up and down the cell. This cell is repeated in all four directions to form columns and rows in the core of the array. The structure of the internal core is optimized to the size of each family member.

National Semiconductor maintains an inventory of gate array wafers fabricated up to but before metalization. As the customer's options are designed and the last three patterns finalized, wafers are taken out of inventory and the fabrication process completed for the metal layers.

In this way, National Semiconductor can provide gate array users with quick turn-around cost effective designs while maintaining the quality, reliability and production control of an in-house (4 and 6-inch) wafer fab line.

2.2 GATE ARRAY BASIC CELL

Figure 1 shows the basic internal cell. The geometries are not drawn to scale and the exact topology has been modified for illustration purposes.

2.3 POWER DISSIPATION

An outstanding feature of microCMOS circuits is their low power dissipation. CMOS circuits draw electrical current for basically two reasons:

(1) During transition from a logic "0" to a logic "1" or vice versa, there exists a finite time when the P-channel and N-channel devices associated with the logic element are both conducting. The CMOS circuit consumes power during this transition.

(2) When signals change state, the distributed capacitance in the circuit (and its load) need to be either charged or discharged. The electrical current required for this purpose increases power consumption.

Thus, power dissipation is dependent on operating voltage, nodal capacitance and the frequency of circuit operation. Mathematically speaking:

$$P_D = CV^2F$$

For estimation purposes, the value of:

25 μW/gate/MHz per gate equivalent can be used for elements within the array.

700 μW/MHz/output buffer at 15 pF load or 1500 μW/MHz/output at 50 pF load, can be used for the output buffers.

Power dissipation in a CMOS array is typically dominated by output buffers driving large capacitive loads.

Figure 2 will help in estimating power consumption in a particular design.

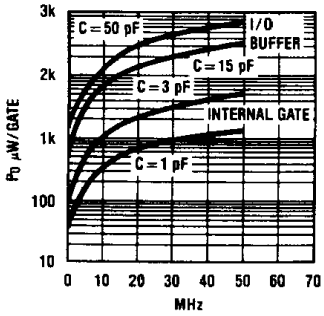

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FIGURE 2. Power Consumption vs Frequency

2.4 ABSOLUTE MAXIMUM RATINGS

Exceeding the following absolute maximum ratings may result in permanent damage to the device.

Supply Voltage	−0.5V to 7V
Input or Output Voltage	−0.5V to V_{DD} +0.5V
Storage Temperature	−65°C to 150°C
Power Dissipation (Package Dependent)	1W
Lead Temp. (Soldering, 10 seconds)	300°C

2.5 RECOMMENDED OPERATING CONDITIONS

	Min	Max	Units
V_{DD}, Supply Voltage	2	6	V
V_I, V_O, Input or Output Voltage	V_{SS}	V_{DD}	V
I_O, High or Low Level Output Current	0	±25	mA
I_{DD}, V_{DD} or V_{SS} Current per Pad	0	±50	mA
T_A, Ambient Operating Temperature	−40	+85	°C

2.6 DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ± 10%, min/max limits apply over recommended operating temperature range unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage	V_O = 0.5V or V_{DD} − 1V, I_O = 1 μA	0.7 V_{DD}		V
V_{IL}	Low Level Input Voltage	V_O = 0.5V or V_{DD} − 1V, I_O = 1 μA		0.3 V_{DD}	V
V_{OH}	High Level Output Voltage	V_I = V_{DD} or GND, I_O = 1 μA	V_{DD} −0.05		V
V_{OL}	Low Level Output Voltage	V_I = V_{DD} or GND, I_O = 1 μA		0.05	V
I_{OH}	High Level Output Current	V_I = V_{DD} or GND, V_O = V_{DD} − 0.8V	− 4		mA
I_{OL}	Low Level Output Current	V_I = V_{DD} or GND, V_O = 0.4V	4		mA
V_{IH}TTL	Min. High Level TTL I/P Voltage (for TTL Input Option)	V_O = 0.5V or V_{DD} − 1V, I_O = 1 μA	2		V
V_{IL}TTL	Max. Low Level TTL I/P Voltage (for TTL Input Option)	V_O = 0.5V or V_{DD} − 1V, I_O = 1 μA		0.8	V
I_I	Input Current (Without Pull-Up Resistor)	V_I = V_{DD} or GND		±1	μA
I_{CC}	Supply Current	V_I = V_{DD} or GND, T_A = 25°C		100	μA

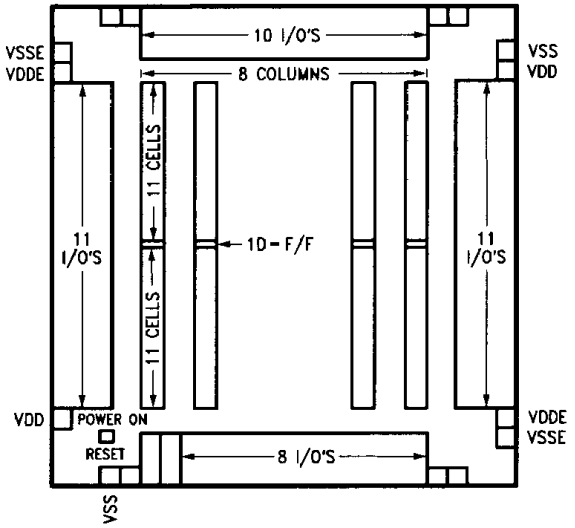
2.7 AC ELECTRICAL CHARACTERISTICS V_{DD} = 5V, T_A = 25°C, 2μ process.

Symbol	Parameter	Min	Max	Units
t_{PLH} t_{PHL}	Output Buffer (Non-Inverting, non-TRI-STATE) t_r = t_f = 5 ns, 0V–5V C_L = 15 pF	1.1 1.2	3.5 4.2	ns ns
t_{PLH} t_{PHL}	Input Buffer (TTL Type, Non-Inverting) at t_r = t_f = 5 ns, 0V–3V C_L = 1 pF	0.75 1.10	2.95 3.2	ns ns
t_{PLH} t_{PHL}	Input Buffer (CMOS Type, Inverting) at t_r = t_f = 5 ns, 0V–5V C_L = 1 pF	0.55 0.50	1.75 1.40	ns ns
t_{PLH} t_{PHL} t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output TRI-STATE (Non-Inverting) at t_r = t_f = 5 ns 0V–5V C_L = 50 pF R_L = 1 kΩ Delays Measured at 50% Point Between Start and Target Voltage	1.9 2.5 2.8 1.9 7.2 7.0	6.0 6.8 7.8 6.0 8.3 8.2	ns ns ns ns ns ns ns
t_{PLH} t_{PHL} t_{PHL} t_{PLH}	Internal 2-Input NAND at t_r = t_f = 5 ns, 0V–5V Load Equivalent to Fan-Out of 3 and 100 mils of Interconnect As Above with C_L = 0 pF	0.4 0.8 0.20 0.15	1.55 2.30 0.75 0.55	ns ns ns ns

3.0 Topology and Routing Resource Distribution

The specific topology and routing resource distribution have been tailored for each family member. Architectural considerations include the ratio of inputs and I/Os to total cell count, power consumption and package inductance to power pins (for simultaneous switching outputs) and routing resources consistant with automatic place and route software. Internal cell utilizations of greater than 85% can be expected. Individual topologies and a family summary follow.

6206 Die Structure



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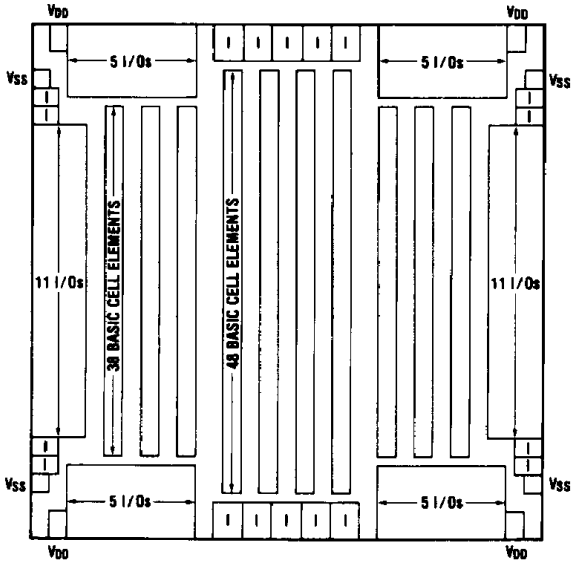
6212 Die Structure



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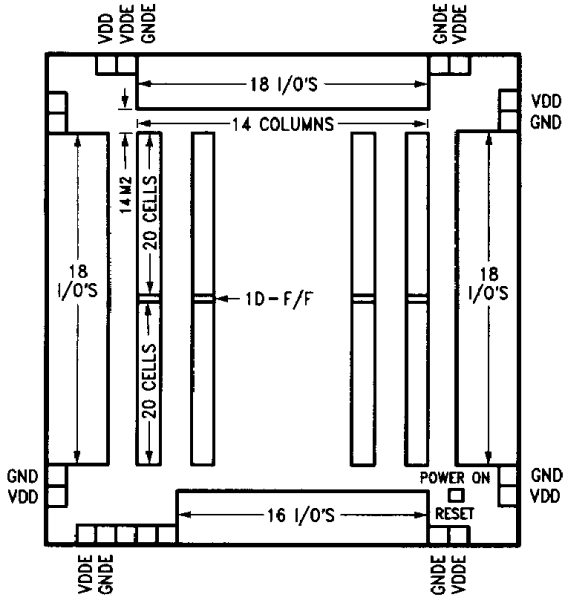
6218 Die Structure



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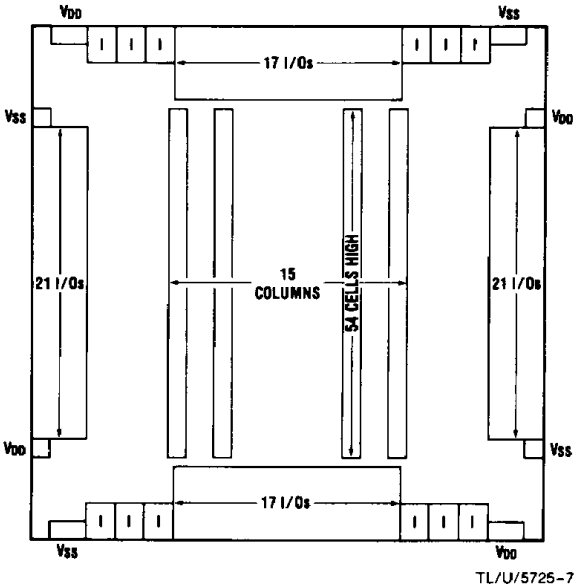
6225 Die Structure



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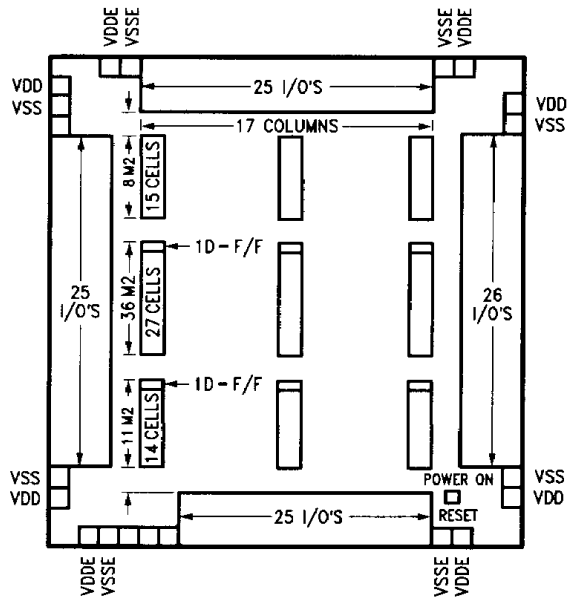
6232 Die Structure



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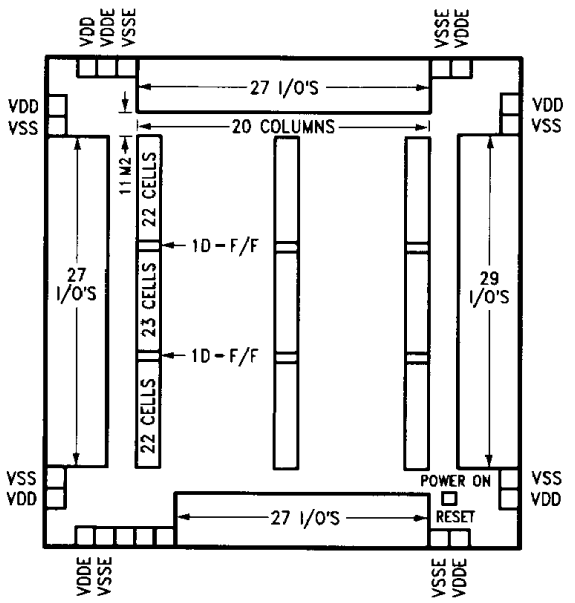
6244 Die Structure



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4.0 On-Chip Test Circuitry

Each of the SCX gate arrays is provided with dedicated on-chip test circuitry. This circuitry forces all the outputs to specific states to facilitate output parametric testing. These parametric tests include leakage and current sourcing/sinking measurements on all output pins.

The on-chip test circuitry is enabled by a dedicated test mode control (TMC) pin. This pin is set aside for testing and cannot be used for any other purpose on the 6212 and 6225. However, for the enhanced devices (6244, 6232, 6218 and 6206), the extra TMC pin can be avoided by means of an internal TMC decoding circuit of the user's design. In addition, an optional internal control signal derived from the TMC pin is now available. This can be used, for example, as a set or reset control signal to the internal logic.

The self-test capability has been further expanded and enhanced on the 6k-gate 6260. It has an additional 2,500 gates dedicated to provide an on-chip maintenance system that includes chip self-test, system interconnect-test, logic analyzer, and system check-sum modes. This self-test feature on the 6260 is unique from the rest of the SCX family as well as in the industry. A low at this input will activate the on-chip test circuitry. When the on-chip test circuitry is activated, the states of all outputs are determined by two other inputs; these are TRI-STATE test control (TSTC) and data test (DT). The TSTC and DT can share input pins with the user's design. They are only active when the TMC is enabled. The TSTC input has precedence over the DT input.

The TMC input is active for the following discussion.

When the TSTC input is active, all the output buffers are put into a high impedance mode. When TSTC is not active, the states of the output buffers are determined by the DT input. These two inputs can be assigned to any of the input pins.

On-Chip Test Circuitry Truth Table

TMC	DT	TSTC	Output
0	X	Active	TRI-STATE
0	Non-Active	Non-Active	1
0	Active	Non-Active	0

Definition of Test Input States

	Non-Inverting Macros	Inverting Macros
Non-Active	0	1
Active	1	0

5.0 Macros

Three types of macros are available for designers to use: hardware macros, software macros (National Semiconductor standard library), and user generated software macros.

5.1 HARDWARE MACROS

The SCX family of gate arrays offers an extensive library of hardware macros (Table I). Each macro has been fully characterized and functionally proven. The designer can select those macros that most efficiently implement the design. The electrical performance of the macros is characterized at two sets of conditions: best and worst-case. Under each set of conditions, the output loading is specified at 0 pF and 1.0 pF. The 1.0 pF load is equivalent to a fan-out of 3 and includes 100 mils length of metal interconnect. A single input load is equivalent to 0.13 pF and is defined as a load factor of 1.

National Semiconductor has very tight wafer fabrication guidelines. However, process parameters still do vary from wafer-to-wafer, lot-to-lot. The electrical specifications of the macros take into account such variations.

TABLE I. Table of Macros

Function	Macro Name
GATES	
Triple 2-Input NAND	C001 (S1)
Dual 3-Input NAND	C002 (S2)
Dual 2-Input NAND/AND	C003 (S3)
Triple 2-Input NOR	C004 (S4)
Dual 3-Input NOR	C005 (S5)
Dual 2-Input NOR/OR	C006 (S6)
Single 2-Input Exclusive-OR	C053 (S53)
2-Input 2-Wide OR-NAND with Complement	C014 (S14)
2-Input 2-Wide AND-NOR with Complement	C015 (S15)
Triple 4-Input NAND	C017 (D1)
Single 5-Input NAND (2X)	C018 (D2)
Triple 3-Input NAND with Complement	C019 (D3)
Triple 4-Input NOR	C020 (D4)
Single 5-Input NOR (2X)	C021 (D5)
Triple 3-Input NOR with Complement	C022 (D6)
4-Input Exclusive-OR	C046 (T2)
3-Input Exclusive-OR	C047 (D10)
Single 2-Input Exclusive-NOR	C048 (S21)
5-Input NAND-AND	C057 (D57)
5-Input NOR-OR	C058 (D58)
3-Input Exclusive-NOR	C800 (D800)
8-Input AND/NAND	C830 (D830)
8-Input OR/NOR	C878 (D878)
BUFFERS	
Triple 2X Buffer	C007 (S7)
Quad Inverter	C008 (S8)
Dual TRI-STATE Inverting Buffer	C009 (S9)
Single Non-Inverting TRI-STATE Buffer	C010 (S10)
Schmitt Trigger	C025 (S24)
Quad Inverter Buffer	C043 (S20)
Dual Triple Inverter Buffer	C044 (S19)
1-3 Buffer	C045 (S22)
3-1 Buffer	C061 (S23)
2-2 Buffer	C049 (S18)
4-Input Exclusive-OR Buffer (2X)	C801 (T801)
Quad Pulldown with Common Enable	C808 (S808)
Quad Pulldown with 6-Input Enable Decode	C811 (D811)
Quad Pullup with 6-Input Enable Decode	C812 (D812)
Quad Pullup with Common Enable	C832 (S832)

Function	Macro Name
LATCHES	
NAND R/S Latch with 2-Input NAND	C012 (S12)
NOR R/S Latch with 2-Input NOR	C013 (S13)
D-Latch with Set/Reset	C062 (D11)
1-Bit Transparent D-Latch with Reset and Enable	C026 (D12)
Triple R/S NAND Latch	C027 (D7)
Triple R/S NOR Latch	C031 (D8)
FLIP-FLOP	
D Flip-Flop	C023 (D9)
D Flip-Flop with Set and Reset	C024 (T1)
D Flip-Flop with Reset and Parallel Load	C034 (Q4)
D Flip-Flop with Set/Reset Master Slave	C051 (T3)
D Flip-Flop with Set/Reset Buffered	C060 (T60)
D Flip-Flop with Reset (Q Output Only)	C064 (D64)
Multiplexed D Flip-Flop with Reset	C035 (Q35)
J-K Flip-Flop with Reset and Set	C037 (F37)
J-K Flip-Flop with Set/Reset Master Slave	C052 (Q2)
T Flip-Flop with Inverter Reset	C036 (Q6)
T Flip-Flop with Reset	C861 (Q861)
REGISTERS AND COUNTERS	
2-Bit Serial In/Out and Parallel Out Shift Register	C039 (F1)
2-Bit Serial/Parallel Shift Register	C042 (H4)
Universal Shift Register State	C194 (F194)
Up-Down Counter Stage with Parallel Load	C038 (F2)
4-Bit Binary Counter Control Logic	C871 (Q871)
MULTIPLEXER & DEMULTIPLEXER	
2-to-1 Multiplexer with Single Control Input	C056 (S56)
4-to-1 TRI-STATE Multiplexer with Enable Low	C028 (T4)
4-to-1 Multiplexer with Complement Output	C029 (T5)
1-to-4 Decoder with Active Low Outputs and Enable Input	C033 (Q3)
3-to-8 Decoder	C138 (H138)
8-Channel Digital Multiplexer	C151 (H151)
Quad 2-Input Multiplexer	C158 (Q158)
Quad 2-Channel TRI-STATE Multiplexer	C257 (Q257)

TABLE I. Table of Macros (Continued)

Function	Macro Name
ARITHMETIC FUNCTIONS	
4-Bit Parity Checker	C030 (T6)
1-Bit Full Adder	C032 (T7)
1-Bit ALU with 7 Functions	C040 (H2)
2-Bit Magnitude Comparator	C041 (H3)

Function	Macro Name
INPUTS AND OUTPUTS	
Inputs Only (36)	See I/O Macro Table
Outputs Only (9)	See I/O Macro Table
Bidirectional (72)	See I/O Macro Table
Oscillator Macros (3)	See I/O Macro Table

Notes on Macro Name

Note 1: Cell Count S = 1 cell (3 gates) Q = 4 cells (12 gates)
D = 2 cells (6 gates) F = 5 cells (15 gates)
T = 3 cells (9 gates) H = 6 cells (18 gates)

Note 2: The 'C000' designator is a common reference used between National Semiconductor and its alternate source for the purpose of consistency with users.

TABLE II. I/O Macro Table

I/O Macro Type	Input Macro	Output Macro	Input Drive			Output Drive			Each Capable of		
			1X	7X	15X	1 mA	2 mA	4 mA	V	D	N
Input Only (36 Macros)	TTL		X	X	X				X	X	X
	CMOS (INV)		X	X	X				X	X	X
	CMOS (NINV)		X	X	X				X	X	X
	Schmitt		X	X	X				X	X	X
Output Only (9 Macros)		NINV				X	X	X			
		INV				X	X	X			
		Open Drain				X	X	X			
Bidirectional (72 Macros)	TTL	NINV	X			X	X	X	X	X	X
	CMOS (INV)	NINV	X			X	X	X	X	X	X
	CMOS (NINV)	NINV	X			X	X	X	X	X	X
	Schmitt	NINV	X			X	X	X	X	X	X
	TTL	INV	X			X	X	X	X	X	X
	CMOS (INV)	INV	X			X	X	X	X	X	X
	CMOS (NINV)	INV	X			X	X	X	X	X	X
	Schmitt	INV	X			X	X	X	X	X	X
Oscillator (3 Macros)						X	X	X			

V = Pull-Up; D = Pull-Down; N = Neither Pull-Up nor Pull-Down

5.2 PERIPHERAL MACROS

Interfacing to the SCX gate arrays is done through the peripheral buffers. There are two types of peripheral cells; input only and bi-directional I/O cells (Table II). The peripheral macros are not included in the count of internally available cells.

The buffers are located around the periphery of the die and the exact configuration is dependent on the particular family member under consideration. Reference section 3 for specific locations of input and I/O cells.

6.0 Software Macros

In addition to the pre-designed hardware macros, National Semiconductor offers a library of software macros. These software macros emulate the functions of the popular 7400 and 4000 logic families. From the designer's vantage point, these software macros are utilized as though they were hardware macros. The actual implementation of these higher order functions is handled by the design automation tools in a process that virtually expands the software macro into its hardware macro primitives.

Since the software macros reside in the design automation system, a designer may copy a software macro into his design, modify it to meet some special consideration, rename it, then reference it as a special or new software macro. This procedure is coordinated with National's Technology Centers.

National Semiconductor adds popular software macros to the existing library as required to meet user needs.

A representative list is shown in Table III. The cell count is a 'will not exceed' number, unused portions of cells are available for use in unrelated portions of the design.

6.1 SOFTWARE MACROS (USER GENERATED)

The user always has the option of generating higher order software macros. This is true regardless of where the user decides to interface with the design automation system.

At the workstation level, the user simply creates the desired function from existing hardware macros, stores the function under a unique identifier name, then recalls it as a block of logic as required.

In the text file mode of schematic capture the user defines the higher order function in terms of the basic hardware macros. These higher order (custom) functions are then 'called' in the same manner as any other software macro.

TABLE III. Software Macros

Device	Cell Count	Device	Cell Count	Device	Cell Count	Device	Cell Count
7400	1.3	7495	13.0	74191	22.0	74399	12.0
7402	1.3	7496	18.0	74192	23.0	74445	7.6
7403	1.3	74100	4.5	74193	22.0	74490	13.0
7404	1.5	74101	6.0	74194	20.0	74521	12.0
7405	1.5	74102	5.0	74195	12.0	74533	12.0
7406	2.0	74103	8.0	74196	23.0	74534	21.0
7407	6.0	74106	8.0	74197	41.0	74540	4.5
7408	2.0	74107	8.0	74198	21.0	74541	6.5
7409	2.0	74108	8.5	74199	26.0	74543	27.0
7410	1.5	74109	8.0	74237	12.0	74544	27.0
7411	2.0	74112	8.0	74240	4.5	74550	57.0
7412	1.5	74113	8.0	74241	6.5	74551	57.0
7414	6.0	74114	8.5	74242	4.5	74563	12.5
7415	1.5	74116	17.0	74243	4.5	74564	21.0
7416	2.0	74125	3.0	74244	8.7	74568	28.0
7417	4.0	74126	3.0	74245	6.5	74569	26.0
7420	1.3	74128	3.0	74251	13.0	74573	13.0
7421	1.3	74132	1.3	74253	6.5	74574	21.0
7422	1.3	74133	3.0	74256	19.0	74589	48.0
7425	3.3	74134	3.5	74257	6.0	74590	57.0
7426	1.33	74135	8.0	74258	3.0	74592	58.0
7427	1.5	74136	4.0	74259	14.0	74593	66.0
7428	3.3	74137	12.0	74260	4.0	74595	37.0
7430	2.0	74138	6.7	74261	29.0	74597	51.0
7432	1.3	74139	6.0	74266	4.0	74640	8.5
7433	3.3	74145	7.6	74273	25.0	74643	12.5
7437	3.3	74147	15.0	74279	2.7	74646	12.5
7438	3.3	74148	9.3	74280	7.0	74648	8.5
7440	2.0	74149	15.5	74283	22.0	74670	60.0
7442	7.6	74150	15.0	74289	84.0	74688	11.0
7443	7.6	74151	6.5	74290	17.0	744002	1.3
7444	7.6	74152	9.0	74292	138.0	744017	21.0
7445	7.6	74153	6.5	74293	17.0	744020	44.0
7446	17.0	74154	13.0	74294	74.0	744024	22.0
7447	17.0	74155	6.0	74295	14.0	744040	38.0
7448	17.0	74156	6.0	74298	13.0		
7451	2.0	74157	5.0	74299	43.0		
7458	2.0	74158	5.0	74323	48.0		
7464	3.3	74159	13.0	74350	16.0		
7465	3.3	74160	22.0	74354	30.0		
7470	6.0	74161	19.5	74356	30.0		
7471	6.7	74162	22.0	74363	13.0		
7472	6.8	74163	20.0	74364	21.0		
7473	8.0	74164	26.0	74365	5.0		
7474	6.0	74165	23.0	74366	3.5		
7475	4.5	74166	25.0	74367	5.0		
7476	8.0	74168	22.0	74368	3.5		
7477	4.5	74169	20.0	74373	13.0		
7478	8.0	74170	40.0	74374	21.0		
7483	12.0	74172	57.0	74375	4.0		
7485	12.0	74173	15.0	74377	26.0		
7486	4.0	74174	19.0	74378	20.0		
7489	84.0	74175	19.0	74379	14.0		
7490	13.0	74180	9.8	74386	4.0		
7491	17.0	74181	41.7	74390	26.0		
7492	13.3	74182	15.0	74393	24.0		
7493	13.0	74189	84.0	74395	14.0		
7494	13.0	74190	23.0	74398	12.0		

7.0 Packaging

The SCX family of microCMOS gate arrays is offered in a very wide variety of packages. The user is provided with many choices in terms of both package type and lead count. The package types offered include ceramic pin grid arrays (PGA), leaded ceramic chip carriers (LDCC), leadless ceramic chip carriers (LCC), plastic leaded chip carriers (PCC), ceramic DIPs, and plastic DIPs.

The availability of such a large variety of packages gives the user flexibility in making the following choices:

—Ceramic versus plastic

—Through-hole mount versus surface mount

The specific packages offered are listed in Table IVa.

Surface mounting of multi-lead components is rapidly gaining popularity. To provide the user flexibility, National Semiconductor offers its CMOS gate arrays in several surface mount package options: leaded and leadless ceramic chip carrier and the plastic leaded chip carrier.

Surface mounting refers to component attachment, whereby the component leads or pads rest on the surface of the PCB instead of the traditional approach of inserting the leads into through-holes which go through the board. With surface mounting there are solder pads on the PCB which align with the leads or pads on the component. The resulting solder joint forms both the mechanical and electrical connections.

The primary reason for surface mounting is to allow leads to be placed closer together than the 0.100 inch standard for DIPs with through-hole mounting. Through-hole mounting on smaller than 0.100 inch space is difficult to achieve in production and is generally avoided. The move to 0.050 inch lead spacing offered with the current generation of surface mounted components, along with a switch from a dual-in-line format to a quad format, has achieved a threefold increase in component mounting density. A need to achieve greater density is a major driving force in today's marketplace.

Learning how to surface mount components to printed circuit boards requires the user to implement an assembly process not typically associated with through-hole insertion/wave soldering assembly methods.

Surface mounting involves three basic process steps:

1) Application of solder or solder paste to the printed circuit board

2) Positioning of the component onto the printed circuit

3) Reflowing of the solder or solder paste.

Table IVb lists the manufacturers currently offering sockets for each of the advanced package options listed in this data sheet. A matrix of which manufacturers to contact for each socket option is provided. The listing is divided into test/burn-in and production categories. There may be some individual sockets that will cover both requirements.

TABLE IVa. Gate Array Package Options

Package Type	Pins	6206	6212	6218	6225	6232	6244	6260
Plastic DIP, N	20	X						
	28	X	X	X	X			
	40	X	X	X	X	X	X	
	48	X	X	X	X	X	X	
Ceramic DIP, D (Side Braze)	20	X						
	28	X	X	X	X			
	40	X	X	X	X	X	X	
	48	X	X	X	X	X	X	
Plastic Leaded Chip Carrier, PCC	28	X	X	X	X			
	44	X	X	X	X	X	X	
	68		X	X	X	X	X	
	84			X	X	X	X	
	124				X	X	X	
Ceramic Leaded Chip Carrier, LDCC	124				X	X	X	X
Ceramic Leadless Chip Carrier, LCC	28	X	X	X	X			
	44	X	X	X	X	X		
	68		X	X	X	X	X	
	84			X	X	X	X	
	124				X	X	X	X
Ceramic Pin Grid Array, PGA	68		X	X	X	X	X	
	84			X	X	X	X	
	124				X	X	X	X
	172							X

TABLE IVb. Socket Vendors

Package Type	Test/Burn-In	Production
Ceramic Pin Grid Array	Amp, Textool, Yamaichi, Thomas & Betts	Amp, Yamaichi Thomas & Betts
Leaded Ceramic Chip Carrier	Yamaichi	Yamaichi
Leadless Ceramic Chip Carrier	Amp, Plastronics, Textool	Amp, Plastronics
Plastic Chip Carrier	Textool	Amp, Burndy, Robinson/Nugent

Vendor Location and Telephone

Amp Inc.
Harrisburg, PA
(715) 564-0100

Plastronics
Irving, TX
(214) 258-1906

Robinson/Nugent
New Albany, IN
(812) 945-0211

Burndy
Norwalk, CT
(203) 838-4444

Textool
Irving, TX
(214) 259-2678

Thomas & Betts
Raritan, NJ
(210) 469-4000

Yamaichi
c/o Napenthe Dist.
Palo Alto, CA
(415) 856-9332

8.0 Propagation Delays

Propagation delays in CMOS arrays are a function of several factors:

- Supply voltage
- Junction temperature
- Process tolerance
- Fan-out loading
- Interconnection routing
- Input signal direction

To assist the designer in evaluating circuit performance under all operating conditions, National Semiconductor guarantees DC and AC parametrics over the full voltage and temperature range, as well as best-case and worst-case propagation delays. Process tolerance is included in the specifications.

Delays other than three for fan-out loading may be extrapolated for loads other than shown.

For example: a 2-input NAND (S1) drives six loads. What is the worst-case LO to HI delay?

From Table V

t_{PLH} for 0 pF = 0.75 ns (0 loads)

t_{PLH} for 1 pF = 2.40 ns (3 loads)

The delay per load = 2.40 − 0.75)/3 = 0.55 ns

Total delay = base delay (0 load) + six loads

4.05 ns = 0.75 ns + 6 (0.55 ns)

What is the delay if the power supply is maintained at 5V and junction temperature is 80°C (approximately 65°C ambient)?

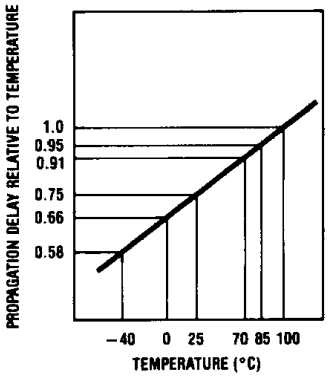

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FIGURE 3. CMOS Propagation Delays as a Function of Temperature

From scaling factors (Table IV note):

Worst-case junction temperature = 100°C

New junction temperature = 80°C

$$\text{Improvement factor} = \frac{0.3\%}{°C}(100°C - 80°C) = 6\%$$

Worst-case voltage = 4.5V

New voltage = 5.0V

$$\text{Improvement factor} = \frac{2\%}{0.1V}(5.0V - 4.5V) = 10\%$$

Derating factor = (1 − 0.06)(1 − 0.1) = 0.846

Total delay (scaled) = 4.05(0.846) = 3.43 ns

This form of calculation is handy for making estimates of critical paths during the initial design phase and can be used as a guide to determine estimated performance of NSC's 2μ process. The actual AC performance prediction will be provided by the design automation system after the designer has functionally verified his design in the logic simulator.

Propagation delays as a function of temperature and supply voltage are shown in *Figures 3* and *4* respectively. Utilization of these curves will speed the estimation of performance at other than specified values.

Representative macro types for the 2μ process (Table V) are presented for comparison. Reference SCX family macro library book for complete specifications.

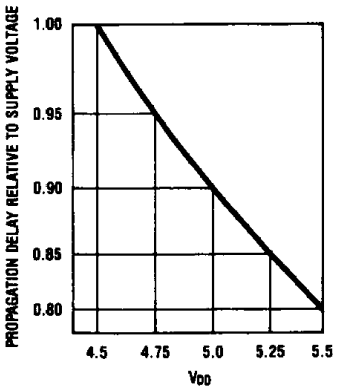

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FIGURE 4. CMOS Propagation Delays as a Function of Supply Voltage

Best-Case	Worst-Case
Temperature = −40°C Supply Voltage = 5.5V Extreme Process Parameters	Temperature = 100°C Supply Voltage = 4.5V Extreme Process Parameters

TABLE V. 2μ

Symbol	Function	LF	Best-Case		Worst-Case		C_{LOAD} (pF)
			t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}	
S1	2-NAND	1	0.095 0.39	0.19 0.67	0.75 2.40	0.95 4.05	0 1
S2	3-NAND	1	0.09 0.37	0.27 0.92	0.95 2.65	1.65 5.75	0 1
S4	2-NOR	1	0.16 0.62	0.15 0.51	1.1 4.15	0.95 2.85	0 1
S5	3-NOR	1	0.23 0.85	0.16 0.52	1.65 6.1	1.13 3.05	0 1
S7	Clock Buffer	2	0.07 0.24	0.13 0.33	0.45 1.45	0.55 1.65	0 1
S8	Inverter	1	0.095 0.36	0.16 0.52	0.6 2.35	0.75 2.6	0 1
S11	2-XOR	2	0.11 0.54	0.16 0.53	2.6 5.8	2.5 5.65	0 1
D9	D Flip-Flop CLK to Q	1 3	0.71 1.02	0.59 0.94	5.12 7.0	4.38 6.25	0 1
	CLK to Q_B		0.35 0.64	0.54 0.98	2.38 5.37	3.3 6.62	0 1
S9	TRI-STATE Inverter	1	0.18 0.60	0.18 0.70	1.2 4.25	1.35 4.15	0 1
S10	TRI-STATE Buffer	2	0.30 0.53	0.27 0.53	1.9 3.4	1.8 3.4	0 1
I_4	Inverting Input Buffer	CMOS	0.23 0.45	0.19 0.39	0.85 2.30	0.70 1.80	0 1
I_1	Input Buffer	TTL	0.33 0.60	0.39 0.78	2.0 3.70	2.45 4.80	0 1
I_6	Short Circuit Input	CMOS	0.04 0.15	0.04 0.15	0.07 0.50	0.07 0.50	0 1
IO_1	Input	TTL	0.33 0.60	0.39 0.78	2.0 3.7	2.45 4.8	0 1
	Output*	7	0.62 1.15	0.78 1.55	4.4 7.0	5.75 9.75	15 50
IO_2	Input (Inverting)	CMOS	0.23 0.45	0.19 0.39	0.85 2.30	0.70 1.80	0 1
	Output*	7	0.62 1.15	0.78 1.55	4.40 7.0	5.75 9.75	15 50
IO_3	Short Circuit Input	CMOS	0.04 0.15	0.04 0.15	0.07 0.50	0.07 0.50	0 1
	Output*		0.62 1.15	0.78 1.55	4.40 7.0	5.75 9.75	15 50
IO_4	Output	7	0.65 1.17	0.63 1.45	4.75 8.25	4.5 8.25	15 50

Note: All delays in nanoseconds.
*TRI-STATE active mode.

$t_r = t_f$ = 2.5 ns for 2-micron.
Voltage Derate = 2.0%/100 mV from 4.5V.
Temperature Derate = 0.3%/°C from 100°C.

LF = Load Factor.
1LF = 0.13 pF.

9.0 Design Automation System

The design automation system offers the end user a variety of interface points and techniques.

Figure 6 shows the standard gate array development flow and responsibilities. Alternative flows are available and are presented in Section 11.

The standard flow consists of four major quadrants. They are the user's site, user's responsibilities, National Semiconductor's technology center, National Semiconductor's responsibility. These represent the 'where' and 'who' aspects of task responsibility and location.

User Site

Logic design and definition are the user's responsibility and are completed at his/her site.

The design file consists of the netlist (wiring diagram) and the test vectors (pattern file). Each can be generated in a text file or as the output from a 'workstation'. The syntax of these files is in the 'hardware design language'.

The evaluation and acceptance of the completed prototypes are done by the user at his/her facilities. National Semiconductor offers technical assistance if necessary.

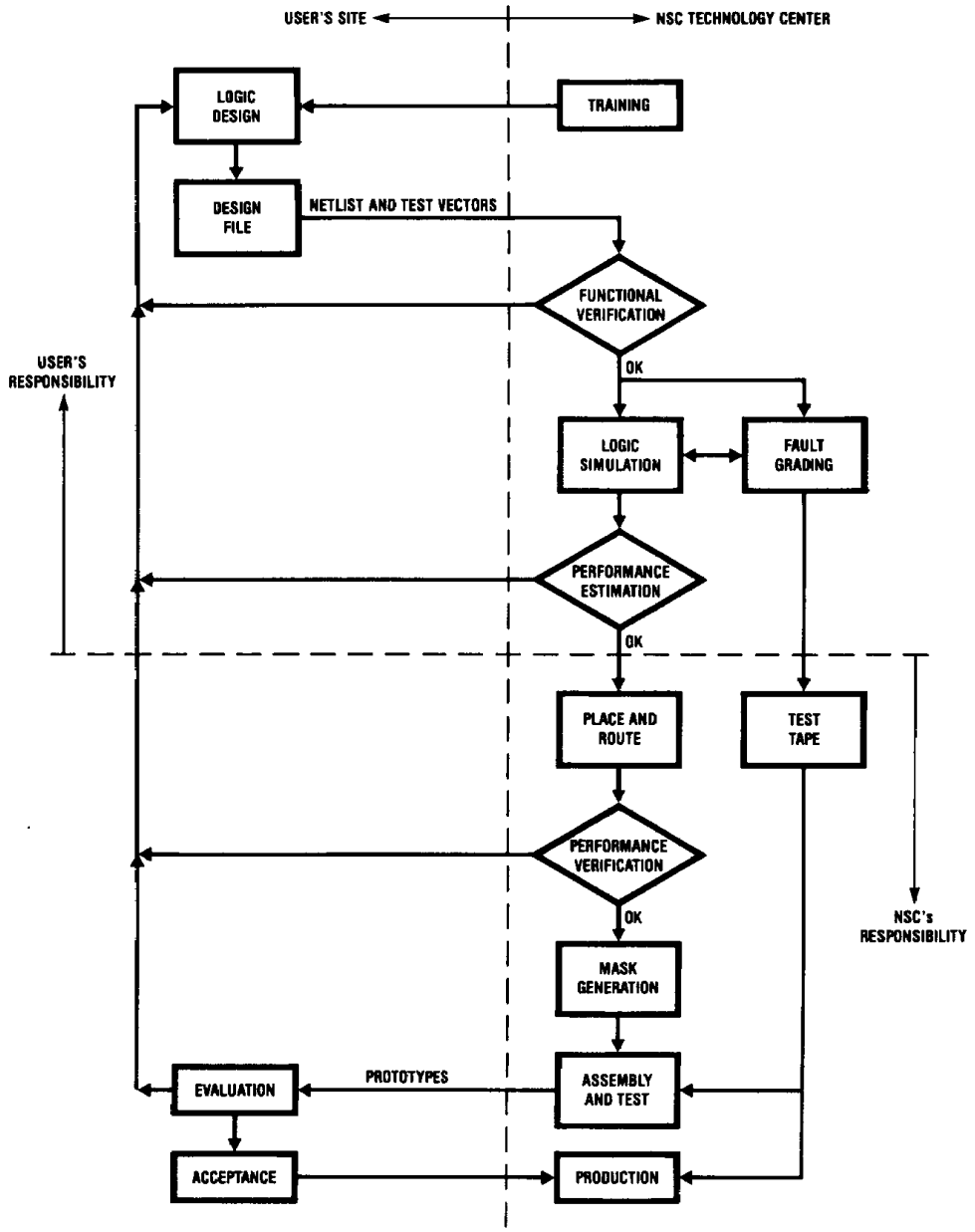

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FIGURE 6. Standard Gate Array Development Process and Responsibilities

National Semiconductor Technology Center

Training includes actual interaction with the design automation system and, depending on the level of user experience, requires from three to five days to complete. All of the considerations necessary for the successful completion of the design are covered during the training. Topics such as, hardware (i.e., speed, power, pinouts) and software considerations (i.e., logic simulation, fault grading, critical path analysis) are tailored to meet the user's needs. Training is provided at the closest technology center. Contact the local sales representative for the location nearest you.

Functional verification of the logic is accomplished by submitting the netlist and pattern files to the logic simulator. The simulator will predict the output results of the specified logic for the applied vectors. The designer can then determine if the specified logic meets the design objectives. Simulation under actual 'loaded' conditions occurs after functional verification and fault grading. Functional verification is the responsibility of the user.

Fault grading is a measure of the ability of the supplied vectors to detect induced logic errors (i.e., on-chip shorts). The vectors supplied eventually become the functional portion of the final production test tape. It is important that the fault grading figure of merit reach 85%. Fault grading is the responsibility of the user.

Performance estimation is the prediction that the logic simulator makes by considering actual macro loading and a projection of the interconnect lengths. This projection is based on an algorithm which relates fan-out to probable trace length. Performance estimation is the responsibility of the user.

Place and route are the actual implementation of the user's design file. Two pieces of design automation software are used to complete the routing.

Automatic place and route software completes the majority of interconnects and in most cases completes the entire array.

Interactive graphics software is used to complete any unrouted interconnects.

Place and route are the responsibility of National Semiconductor.

Performance verification is the rerunning of the 'performance estimation' software with the actual cell placements and associated trace lengths. Performance verification is the responsibility of the user.

Mask generation, wafer fab, assembly and test are completed by National Semiconductor.

Prototype evaluation and acceptance are the responsibility of the user.

National Semiconductor has a large staff of applications and consulting engineers available to assist users at any point in the array development process.

9.5 WORKSTATION SUPPORT

The above capabilities, specifically the front-end design functions (such as schematic capture, netlist entry, logic simulation and timing estimation), are also available on the Valid, Daisy, and Mentor workstations. Such capabilities will be extended to other popular CAE design stations such as CAE Systems and the IBM PC.

To allow workstation users to properly interface with the SCX-series gate arrays, National provides a workstation software design kit. It consists of a set of floppy discs containing the logic symbols of all the macros, a netlist extractor and model timing data for pre-layout simulation and timing estimation. This design kit is developed, distributed, maintained and updated solely by National.

Some of the more time-consuming tasks such as fault grading, auto-place-and-route and post-layout logic verification are performed on the mainframe computer. A typical design flow between the workstation and mainframe is illustrated in *Figure 7*. Generally, there are three design paths as follows:

- Path A—schematic capture on user's workstation; then transfer of unsimulated design files (netlist and test vectors) to NSC's mainframe for logic simulation, fault grading and place-and-route.
- Path B—schematic capture, logic simulation and timing verification on user's workstation; then transfer of *simulated* design files to NSC's mainframe for resimulation (one pass), fault grading and place-and-route.
- Path C—schematic capture, logic simulation, timing verification and place-and-route on user's workstation; then transfer of database file to NSC's mainframe for resimulation (one pass), fault grading and PG tape generation. (This is a future capability.)

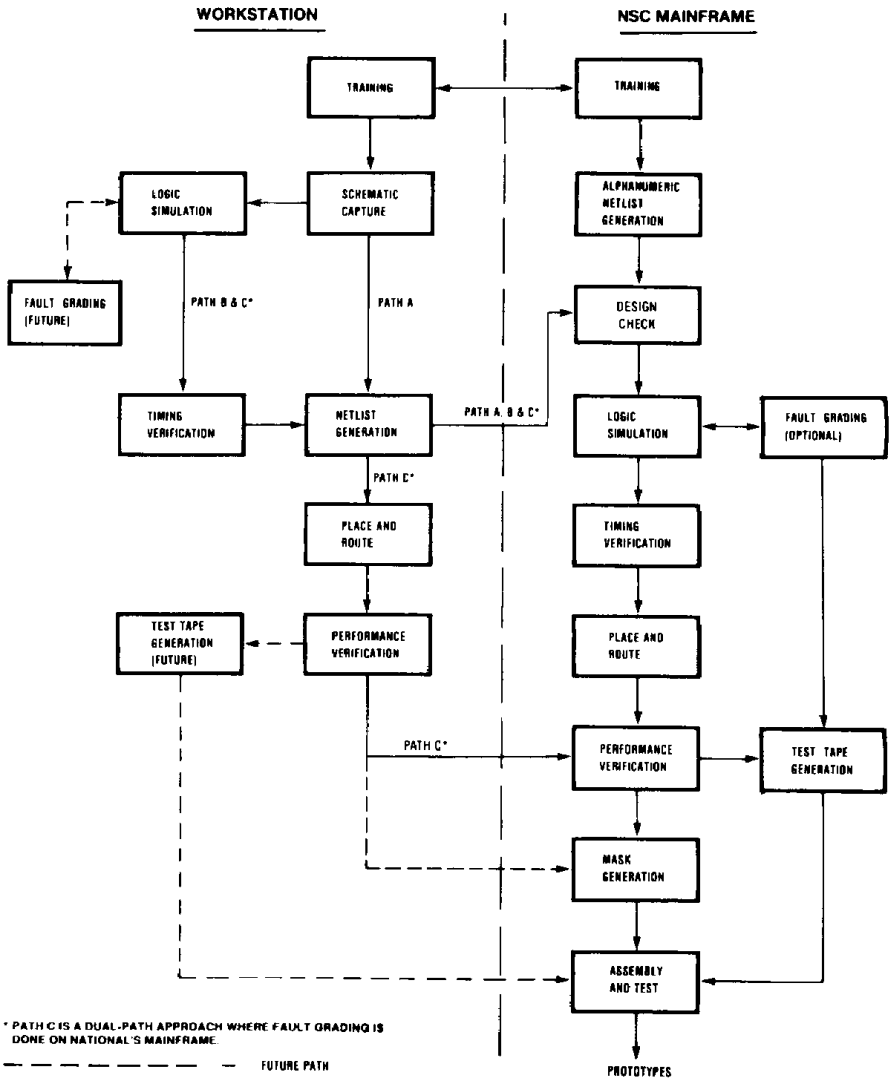

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FIGURE 7. National's Workstation-to-Mainframe Semi-Custom Design Flow

10.0 Design Example

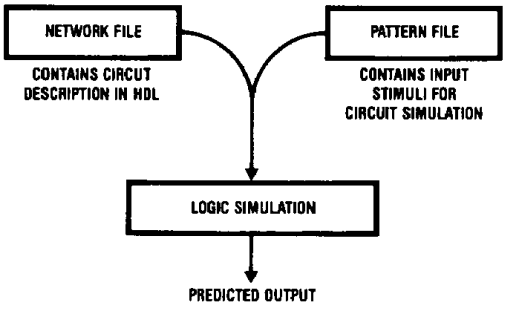
The two most popular ways of interfacing to the design automation system are 1) alphanumeric text entry and 2) workstation output. A different example will be given for each. In either case the design automation system requires two basics files to operate.

Network (File): The network file is the 'wiring diagram' of the design. It represents how the array is to be 'wired'. More specifically, it is the manner in which the hardware macros are interconnected. The syntax of the network file is specified by a hardware design language (HDL).

Pattern (File): The pattern file represents the stimuli or sequence of signals used to exercise the design specified by the network file. The pattern file ultimately becomes the functional portion of the final test tape used to screen production devices.

The logic simulator operates on the network and pattern files and predicts the logic output as a function of the pattern file.

Data Entry



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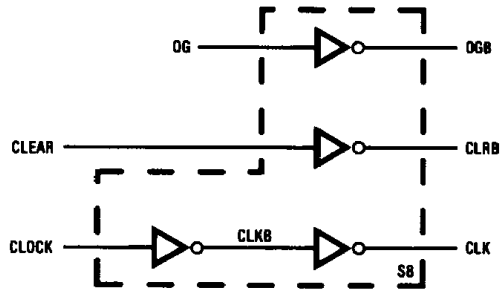
The simulator has two modes of operation. The first mode is used to verify the logical integrity of the design. The second mode considers capacitive circuit loading and anticipated wire lengths. The result of the second mode is the performance that can be expected after the circuit has been placed and routed.

The basic form of a network file is as follows:

```
$NETWORK              (*BEGIN A NETWORK FILE*)
$ INP INA INB ETC.    (*LIST ALL INPUT NAMES*)
$  OUT OUTA OUTB ETC. (*LIST ALL OUTPUT NAMES*)
        •
        •
        •
MACRO CALLS                (*SPECIFY MACROS AND
                               INTERCONNECTS*)
        •
        •
        •
$$*       COMMENTS    (*MAKE COMMENTS*)
        •
        •
        •
```

The macro call syntax for the following circuit fragment is as specified.



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```
$SUBU  S8
          └──(* SPECIFIES A PARTICULAR
                  MACRO TYPE *)
       └──(* SPECIFIES A HARDWARE MACRO *)

$$AN0        (* CIRCUIT NAME ASSOCIATED WITH
          └──────ABOVE MACRO *)

                  ┌──(* DELIMITER *)
CLKB CLK CLRB OGB / CLOCK CLKB CLEAR OG
                  └──(* INPUTS TO MACRO ELEMENTS *)
       └──(* OUTPUTS FROM MACRO ELEMENTS *)
```

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If the designer were using the alphanumeric text mode of data entry, each unique macro and macro type would be specified in the above manner until the entire network had been specified.

In the workstation mode of schematic capture the designer would call and name each desired macro, then graphically interconnect each macro in the required fashion. The workstation would then 'compile' the schematic into the network file.

10.1 TEXT MODE

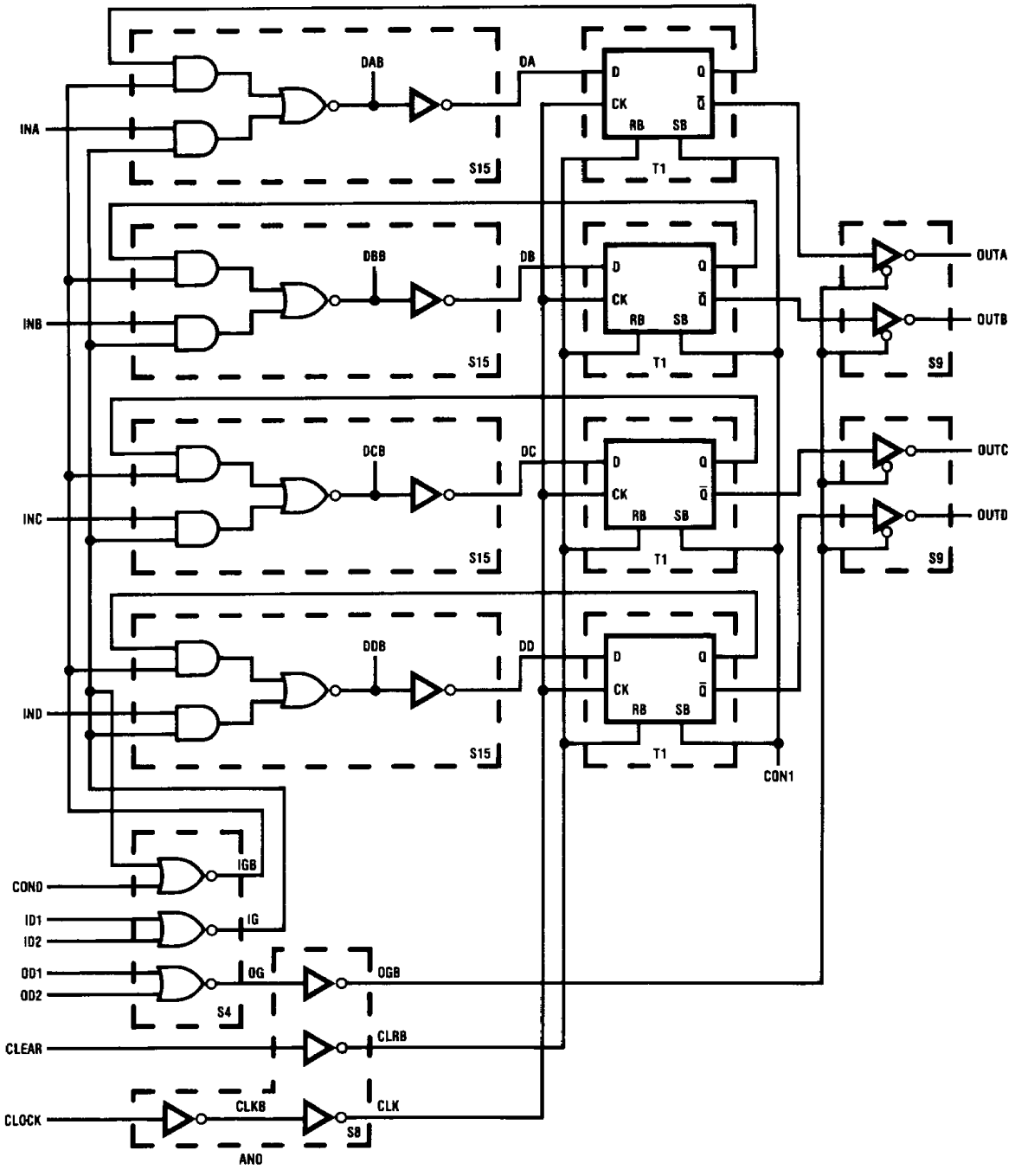

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FIGURE 8. The Design of a Four-Bit Latch with TRI-STATE Output is Presented.

Listing 1

```
$$★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★
$NETWORK
$INPUT  INA  INB  INC  ID1  ID2  OD1  OD2  CLOCK  CLEAR
$OUTPUT  OUTA  OUTB  OUTC  OUTD
$$★  DM74173  MACRO
$SUBU  S8
$$AN0
CLKB  CLK  CLRB  OGB  /  CLOCK  CLKB  CLEAR  OG
$SUBU  S4
$$AN1
IG  IGB  OG  /  ID1  ID2  IG  CON0  OD1  OD2
$SUBU  S15
$$AN2
DAB  DA  /  INA  IG  IGB  QA
$SUBU  S15
$$AN3
DBB  DB  /  INB  IG  IGB  QB
$SUBU  S15
$$AN4
DCB  DC  /  INC  IG  IGB  QC
$SUBU  /  S15
$$AN5
DDB  DD  /  IND  IG  IGB  QD
$SUBU  T1
$$AN6
QA  QAB  /  CON1  DA  CLK  CLRB
$SUBU  T1
$$AN7
QB  QBB  /  CON1  DB  CLK  CLRB
$SUBU  T1
$$AN8
QC  QCB  /  CON1  DC  CLK  CLRB
$SUBU  T1
$$AN9
QD  QDB  /  CON1  DD  CLK  CLRB
$SUBU  S9
$$AN10
OUTA  OUTB  /  QAB  OGB  QBB  OGB
$SUBU  S9
$$AN11
OUTC  OUTD  /  QCB  OGB  QDB  OGB
$$★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★
```

10.2 WORKSTATION MODE

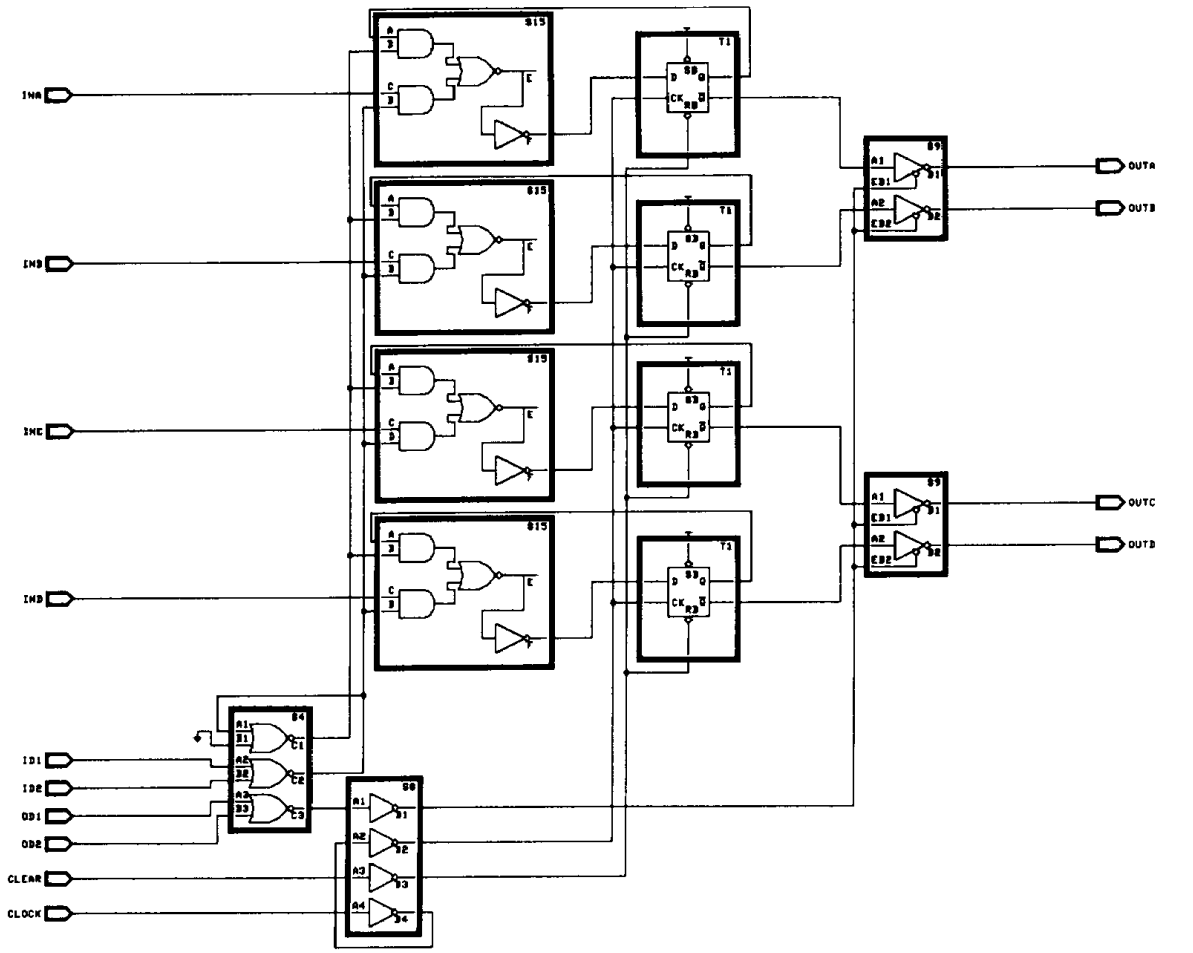

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FIGURE 9

Listing 2

```
$NETWORK
$INPUT  CLEAR  CLOCK  ID1  ID2  INA  INB  INC  IND  OD1  OD2
$OUTPUT  OUTA  OUTB  OUTC  OUTD
$$★
$SUBU  S4
$$XCMP  1
XSIG29  XSIG27  XSIG18  /  XSIG27  GND  ID1  ID2  OD1  OD2
$$★
$SUBU  T1
$$XCMP  10
XSIG33  XSIG41  /  VCC  XSIG34  XSIG20  XSIG21
$$★
$SUBU  S9
$$XCMP  11
OUTA  OUTB  /  XSIG41  XSIG22  XSIG40  XSIG22
$$★
$SUBU  S9
$$XCMP  12
OUTC  OUTD  /  XSIG39  XSIG22  XSIG38  XSIG22
$$★
$SUBU  S8
$$XCMP  2
XSIG22  XSIG20  XSIG21  XSIG19  /  XSIG18  XSIG19  CLEAR  CLOCK
$$★
$SUBU  S15
$$XCMP  3
OPEN-1  XSIG37  /  XSIG30  XSIG29  IND  XSIG27
$$★
$SUBU  S15
$$XCMP  4
OPEN-2  XSIG36  /  XSIG31  XSIG29  INC  XSIG27
$$★
$SUBU  S15
$$XCMP  5
OPEN-3  XSIG35  /  XSIG32  XSIG29  INB  XSIG27
$$★
$SUBU  S15
$$XCMP  6
OPEN-4  XSIG34  /  XSIG33  XSIG29  INA  XSIG27
$$★
$SUBU  T1
$$XCMP  7
XSIG30  XSIG38  /  VCC  XSIG37  XSIG20  XSIG21
$$★
$SUBU  T1
$$XCMP  8
XSIG31  XSIG39  /  VCC  XSIG36  XSIG20  XSIG21
$$★
$SUBU  T1
$$XCMP  9
XSIG32  XSIG40  /  VCC  XSIG35  XSIG20  XSIG21
$$★
```

10.3 PATTERN FILE

```
$CYCLE = 1000  1000 REPRESENTS THE NUMBER OF INTERVALS PER CYCLE  1 INTERVAL = 100 PICOSECONDS
$$★★★★★★★★★★★★★★★★★★★★★★★★
$$★  PATTERN FILE CODING FOLLOWS
$$★★★★★★★★★★★★★★★★★★★★★★★★
$$★  PATTERN FILE FOR TESTING DM74173
$$★  TEST SHOULD SWEEP 16 CYCLES
     CLEAR  HI  1-2
     INA  HI  1 3 5 7 11-12
     INB  HI  1 3 5 7 11-12
     INC  HI  1 3 5 7 11-12
     IND  HI  1 3 5 7 11-12   } INPUT SIGNALS USED TO SIMULATE THE NETWORK
     ID1  HI  1 3 5-6
     ID2  LO  1 3 7-8
     OD1  HI  5-6 13-14
     OD2  HI  7-8 15-16
     CLOCK  LO  RPT  (01:  1-16)  SINGLE CLOCK REPEATING 01 THROUGH CYCLE 16

     CIRCUIT INPUTS HI AT SPECIFIED CYCLE. LOW AT ALL OTHER CYCLES
     CIRCUIT INPUT LO AT SPECIFIED CYCLE. HI AT ALL OTHER CYCLES
```

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10.4 SIMULATOR OUTPUT

	INPUTS AS SPECIFIED BY PATTERN FILE					OUTPUTS AS SPECIFIED BY PATTERN FILE
	IIII NNNN ABCD	II DD 1 2	OO DD 1 2	C L E A R	C L O C K	OOOO UUUU TTTT ABCD
1	1111	10	00	1	0	XXXX
**157	1111	10	00	1	0	0000
2	0000	01	00	1	1	0000
3	1111	10	00	0	0	0000
4	0000	01	00	0	1	0000
5	1111	11	10	0	0	0000
**134	1111	11	10	0	0	ZZZZ
6	0000	11	10	0	1	ZZZZ
7	1111	00	01	0	0	ZZZZ
8	0000	00	01	0	1	ZZZZ
9	0000	01	00	0	0	ZZZZ
**140	0000	01	00	0	0	1111
10	0000	01	00	0	1	1111
11	1111	01	00	0	0	1111
12	1111	01	00	0	1	1111
13	0000	01	10	0	0	1111
**129	0000	01	10	0	0	ZZZZ
14	0000	01	10	0	1	ZZZZ
15	0000	01	01	0	0	ZZZZ
16	0000	01	01	0	1	ZZZZ

SEQUENTIAL NUMBERS REPRESENT TIME CYCLES

ZZZZ = HIGH IMPEDANCE STATE
1111 = HIGH STATE
0000 = LOW STATE

**Intermittent numbers represent settling time in hundred-picoseconds that occur between time cycles.

11.0 Alternative Interfaces

Flexibility in the design automation system allows a variety of user/vendor interfaces. Options include:

- User supplies schematic, timing diagrams and parametric specifications. National Semiconductor implements the array (Turn-Key design).
- User 'captures' the design at his facility or at a National Semiconductor technology center. National Semiconductor supports a wide range of communication protocols for interfacing to industrial (mainframe) or personal computers. These are available with or without error control and communication rates of 300 to 9600 baud.
- User follows basic array development flow specified in *Figure 6.*
- User generates logic simulator compatible files from his workstation. Completes the array using National Semiconductor's design automation system.
- User generates compatible design files and logic verification in his/her simulator, then interfaces to design automation system at either fault grading, performance estimation, or 'place and route'.
- User supplies completed design files from National Semiconductor's alternate source, effectively entering design automation system just prior to digitizing.
- User provides all design files necessary for mask generation, essentially a 'customer owned tooling' (COT) approach.

12.0 Training and Technical Services

To facilitate users to design with National's CMOS gate arrays, training is offered on a regular basis at National's worldwide technology centers. At the new Santa Clara training/design center, multiple workstations are used to complement the basic training. Additional workstations located in private offices are also available for customers to enter, capture and verify their designs. As part of the technical services, experienced design consultants from National will be available at the training/design center to provide on-the-spot engineering assistance.

The training, workstation design kit and other technical services are provided by National's Training, Layout, Consulting (TLC) Group. Overall technical customer-support services include the following:

- Customer training
- Technical documentation
- Design assistance
- Simulation support
- Workstation support
- Turnkey design
- Place-and-Route implementation
- Mainframe software qualification
- Workstation software qualification

For any technical assistance, contact National's Applications Group at (408) 721-4614.

13.0 Technology Centers

National Semiconductor Headquarters,
2900 Semiconductor Drive, Santa Clara, California 95051
(408) 721-4614, TWX: (910) 339-9240

National Semiconductor Corp.
111 So. Bedford Street, Suite 200
Burlington, MA 01803
Telephone: (617) 273-0964

National Semiconductor S.A.
Expansion 1000
28. rue de la Redoute
F-92260 Fontenay-aux-Roses, France
Telephone: 33-1-660-8140
Telex: 842-250959

National Semiconductor GmbH
Industriestrasse 10
D-8080 Fuerstenfeldbruck, W. Germany
Telephone: 49-8141-103-1
Telex: 841-527649

National Semiconductor AB
Box 2016
Stensaetravaegen 4/II TR
S-12702 Stockholm, Sweden
Telephone: 46-8-970190
Telex: 854-10731

National Semiconductor UK. Ltd
The Maples
Kembrey Park
Swindon SN 2 6UT
Wilts, England
Telephone: 44-793-614141
Telex: 851-444674

National Semiconductor SPA
Via Solferino 19
I-20121 Milan, Italy
Telephone: 39-2-3452046
Telex: 332835

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-6090
Tel: (408) 721-5000
TWX: (910) 339-9240

National Semiconductor GmbH
Westendstrasse 193-195
D-8000 Munchen 21
West Germany
Tel: (089) 5 70 95 01
Telex: 522772

NS Japan Ltd.
4-403 Ikebukuro,
Toshima-ku,
Tokyo 171, Japan
Tel: (03) 988-2131
FAX: 011-81-3-988-1700

National Semiconductor Hong Kong Ltd.
Southeast Asia Marketing
Austin Tower, 4th Floor
22-26 Austin Avenue
Tsimshatsui, Kowloon, H.K.
Tel: 3-7231290, 3-7243645
Cable: NSSEAMKTG
Telex: 52996 NSSEA HX

National Semiconductores Do Brasil Ltda.
Av. Brig. Faria Lima, 830
8 Andar
01452 Sao Paulo, SP. Brasil
Tel: (55/11) 212-5066
Telex: 391-1131931 NSBR BR

National Semiconductor (Australia) PTY, Ltd.
21/3 High Street
Bayswater, Victoria 3153
Tel: (03) 729-6333
Telex: AA32096