KS82C55A

PROGRAMMABLE PERIPHERAL INTERFACE

FEATURES/BENEFITS

- **Pin and functional compatibility with the industry standard 8255A**
- **Provides support for 8080/85, 8086/8 and 80186 286/386**
- **Very high speed — 5MHz, 8MHz and 10MHz version**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **24 programmable I/O pins**
- **Direct bit set/reset capability**
- **Bidirectional bus operation**
- **Enhanced control word read capability**
- **Bus-hold circuitry on all I/O ports eliminates pull-up resistors**

DESCRIPTION

The KS82C55A Programmable Peripheral Interface is a high performance CMOS device offering pin for pin functional compatibility with the industry standard 8255A. It includes 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. Bus hold circuitry on all I/O ports together with TTL compatibility over the full temperature range eliminates the need for pull-up resistors.

The KS82C55A is a general purpose programmable I/O device designed for use with many different microprocessors. Also makes it an attractive addition in portable systems or systems with low power standby modes.

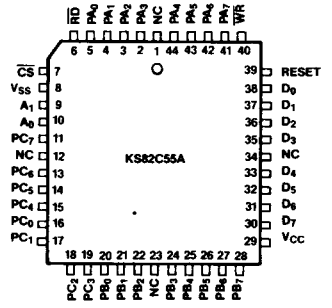

Figure 1a: 44-Pin PLCC Configuration

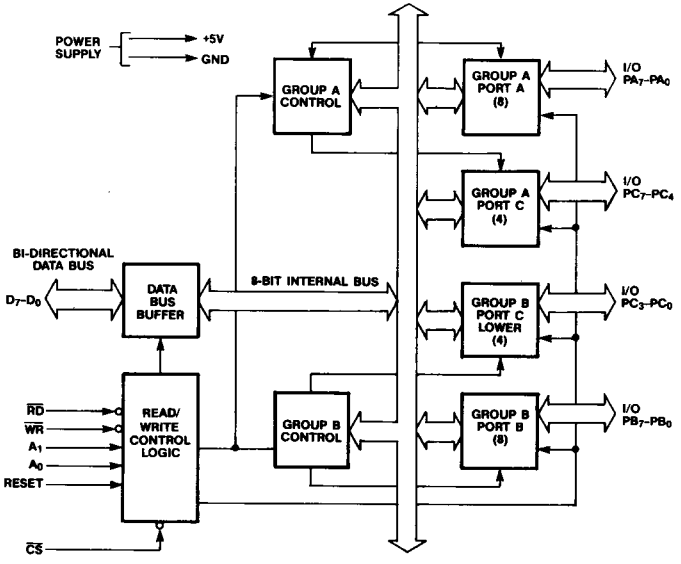

Figure 2: KS82C55A Block Diagram

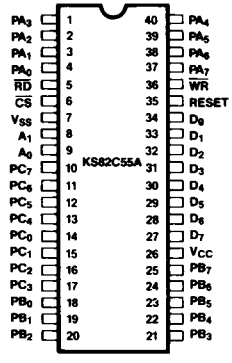

Figure 1b: 40-Pin DIP Configuration

Table 1a: 44-Pin PLCC Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	NC	9	A_1	17	PC_1	25	PB_4	33	D_4	41	PA_7
2	PA_3	10	A_0	18	PC_2	26	PB_5	34	NC	42	PA_6
3	PA_2	11	PC_7	19	PC_3	27	PB_6	35	D_3	43	PA_5
4	PA_1	12	NC	20	PB_0	28	PB_7	36	D_2	44	PA_4
5	PA_0	13	PC_6	21	PB_1	29	V_{CC}	37	D_1		
6	$\overline{RD}$	14	PC_5	22	PB_2	30	D_7	38	D_0		
7	$\overline{CS}$	15	PC_4	23	NC	31	D_6	39	RESET		
8	V_{SS}	16	PC_0	24	PB_3	32	D_5	40	$\overline{WR}$		

Table 1b: 40-Pin DIP Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	PA_3	8	A_1	15	PC_1	22	PB_4	29	D_5	36	$\overline{WR}$
2	PA_2	9	A_0	16	PC_2	23	PB_5	30	D_4	37	PA_7
3	PA_1	10	PC_7	17	PC_3	24	PB_6	31	D_3	38	PA_6
4	PA_0	11	PC_6	18	PB_0	25	PB_7	32	D_2	39	PA_5
5	$\overline{RD}$	12	PC_5	19	PB_1	26	V_{CC}	33	D_1	40	PA_4
6	$\overline{CS}$	13	PC_4	20	PB_2	27	D_7	34	D_0		
7	V_{SS}	14	PC_0	21	PB_3	28	D_6	35	RESET		

FUNCTIONAL DESCRIPTION

General

The KS82C55A is a programmable peripheral interface device designed for use in high speed, low power microcomputer systems. It is a general purpose I/O component which functions to interface peripheral equipment to the microcomputer system bus. The functional configuration of the KS82C55A is programmed by the system software such that no external logic is necessary to interface peripheral devices.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the KS82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. The data bus buffer also transfers control words and status information.

Read/Write and Control Logic

This block manages all of the internal and external transfers of both Data and Control or Status Words. It accepts inputs from the CPU Address and Control buses and issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the system software. The CPU outputs a Control Word to the KS82C55A. The Control Word contains information such as code, bit set, bit reset, etc., that initializes the functional configuration of the KS82C55A.

Each of the Control blocks (Group A and Group B) accepts commands from the Read/Write Control Logic, receives Control Words from the internal data bus and issues the proper commands to its associated ports.

- Control Group A - Port A and Port C upper (C_7-C_4)
- Control Group B - Port B and Port C lower (C_3-C_0)

Table 2: Pin Descriptions

<table>
<tr><th>Symbol</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>A_0, A_1</td><td>I</td><td>Address: These input signals in conjunction with $\overline{RD}$ and $\overline{WR}$, control the selection of one of the three ports or the Control Word Registers.
<table>
<tr><th>A_1</th><th>A_0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th><th>Input Operation (Read)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Port A - Data Bus</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Port B - Data Bus</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Port C - Data Bus</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Control Word - Data Bus</td></tr>
</table>
<table>
<tr><th>A_1</th><th>A_0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th><th>Output Operation (Write)</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port A</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port B</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port C</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Control</td></tr>
</table>
<table>
<tr><th>A_1</th><th>A_0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th><th>Disable Function</th></tr>
<tr><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>Data Bus - 3-State</td></tr>
<tr><td>X</td><td>X</td><td>1</td><td>1</td><td>0</td><td>Data Bus - 3-State</td></tr>
</table></td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip Select: A low on this input enables the KS82C55A to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.</td></tr>
<tr><td>D_{0-7}</td><td>I/O</td><td>Data Bus: Bi-directional, 3-state data bus lines, connected to system data bus.</td></tr>
<tr><td>PA_{0-7}</td><td>I/O</td><td>Port A, Pins 0-7: An 8-bit data output latch/buffer and an 8-bit data input buffer.</td></tr>
<tr><td>PB_{0-7}</td><td>I/O</td><td>Port B, Pins 0-7: An 8-bit data output latch/buffer and an 8-bit data input buffer.</td></tr>
<tr><td>PC_{0-3}</td><td>I/O</td><td>Port C, Pins 0-3: Lower nibble of an 8-bit data output latch/buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.</td></tr>
<tr><td>PC_{4-7}</td><td>I/O</td><td>Port C, Pins 4-7: Upper nibble of Port C.</td></tr>
<tr><td>$\overline{RD}$</td><td>I</td><td>Read Control: This input is low during CPU read operations.</td></tr>
<tr><td>$\overline{WR}$</td><td>I</td><td>Write Control: This input is low during CPU write operations.</td></tr>
<tr><td>RESET</td><td>I</td><td>Reset: A high on this input clears the control register and all ports are set to the input mode.</td></tr>
<tr><td>V_{CC}</td><td>—</td><td>Power: 5V ± 10% DC Supply.</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>Ground: 0V.</td></tr>
</table>

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The Control Word Register can be both written and read as shown in the address decode table in the pin descriptions (Table 2). The Control Word format for both read and write operations is shown in Figure 8. Bit D_7 will always be a logic ONE when the Control Word is read, as this implies control word mode information.

Ports A, B, and C

The KS82C55A contains three 8-bit ports (A, B, and C). All three ports can be configured in a wide variety of functional characteristics by the system software, but each also has its own special features.

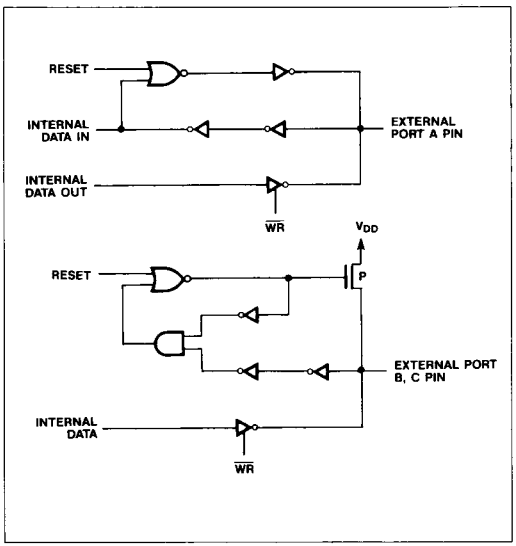
Port A: One 8-bit data output buffer and one 8-bit input buffer. Both pull-up and pull-down bus-hold devices are present on Port A.

Port B: One 8-bit data output buffer and one 8-bit data input buffer. Only pull-up bus-hold devices are present on Port B.

Port C: One 8-bit data output buffer and one 8-bit data input buffer (no latch for input). Port C can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only pull-up bus-hold devices are present on Port C.

See Figure 3 for the bus-hold circuit configuration for Ports A, B, and C.

Figure 3: Port A, B, C, Bus-Hold Configuration



OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

- Mode 0 - Basic Input/Output
- Mode 1 - Strobed Input/Output
- Mode 2 - Bidirectional Bus

When the Reset input goes high, all ports will be set to the input mode with all 24 port lines held at a logic one level by the internal bus hold devices. After the reset is removed, no additional initialization is required for the KS82C55A to remain in the input mode. No pull-up or pull-down devices are required. During execution, any of the other modes may be selected by using a single output instruction. This allows a single KS82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined such that their functional definition can be tailored to almost any I/O structure. For example, Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, and Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single output instruction. This feature reduces the software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation as if they were data output ports.

Interrupt Control Functions

When the KS82C55A is operating in Mode 1 or Mode 2, control signals are provided for use as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop using the Bit Set/Reset function of Port C.

This function allows the Programmer to Enable or Disable a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

Figure 4: Mode Definitions & Bus Interface

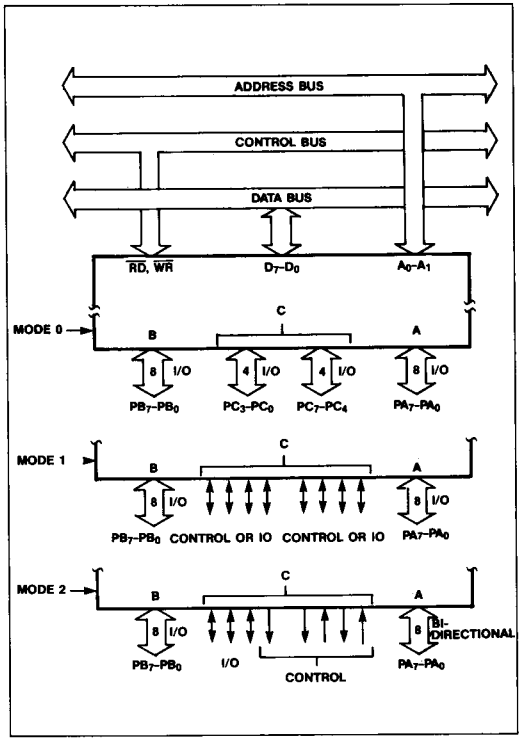
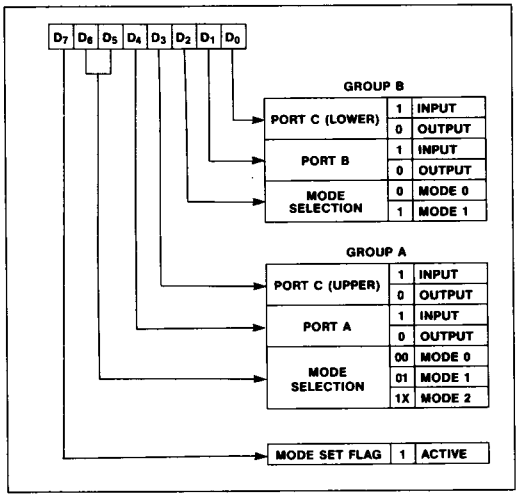


Figure 5: Mode Definition Format



INTE Flip-Flop Definition:

(Bit-Set) - INTE is Set - Interrupt enable
(Bit-Reset) - INTE is Reset - Interrupt disable

Note: All mask flip-flops are automatically reset during mode selection and device reset.

Mode 0 (Basic Input/Output)

This mode provides simple input and output operations for each of the three ports. No handshaking is required. Data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations are possible in this mode.

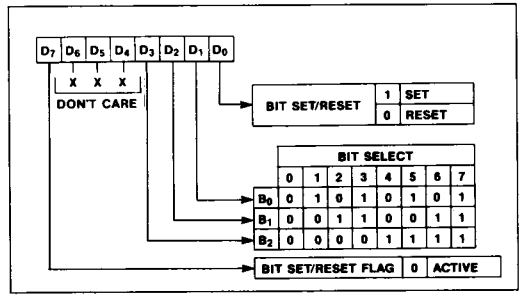
Mode 1 (Strobed Input/Output)

This mode transfers I/O data to or from a specified port in conjunction with strobes or handshaking signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these handshaking signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Figure 6: Bit Set/Reset Format

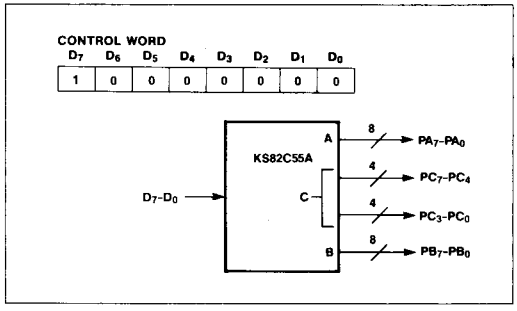


Input Control Signal Definitions

$\overline{STB}$ (Strobe Input): A LOW on this input loads data into the input latch.

IBF (Input Buffer Full F/F): A HIGH on this output indicates that the data has been loaded into the input latch. IBF is set by the STB input being LOW and is RESET by the rising edge of the $\overline{RD}$ input.

Figure 7: Mode 0 Configuration



INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ being a ONE, IBF is a ONE, and INTE is a ONE. It is RESET by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the Port.

INTE A: Controlled by bit Set/Reset of PC_4.

INTE B: Controlled by bit Set/Reset of PC_2.

Output Control Signal Definition

OBF (Output Buffer Full F/F): The OBF output will go LOW to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the $\overline{WR}$ input and reset by the ACK input being low.

ACK (Acknowledge Input): A LOW on this input informs the KS82C55A that the data from Port A or Port B has been accepted. (i.e., a response from the peripheral device indicating that it has received the data output by the CPU).

Table 3: Mode 0 Port Definition

Control Word #	Control Word Bits								Port Direction			
		Group A				Group B			Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	PA_7-PA_0	PC_7-PC_4	PC_3-PC_0	PB_7-PB_0
0	1	0	0	0	0	0	0	0	OUTPUT	OUTPUT	OUTPUT	OUTPUT
1	1	0	0	0	0	0	0	1	OUTPUT	OUTPUT	INPUT	OUTPUT
2	1	0	0	0	0	0	1	0	OUTPUT	OUTPUT	OUTPUT	INPUT
3	1	0	0	0	0	0	1	1	OUTPUT	OUTPUT	INPUT	INPUT
4	1	0	0	0	1	0	0	0	OUTPUT	INPUT	OUTPUT	OUTPUT
5	1	0	0	0	1	0	0	1	OUTPUT	INPUT	INPUT	OUTPUT
6	1	0	0	0	1	0	1	0	OUTPUT	INPUT	OUTPUT	INPUT
7	1	0	0	0	1	0	1	1	OUTPUT	INPUT	INPUT	INPUT
8	1	0	0	1	0	0	0	0	INPUT	OUTPUT	OUTPUT	OUTPUT
9	1	0	0	1	0	0	0	1	INPUT	OUTPUT	INPUT	OUTPUT
10	1	0	0	1	0	0	1	0	INPUT	OUTPUT	OUTPUT	INPUT
11	1	0	0	1	0	0	1	1	INPUT	OUTPUT	INPUT	INPUT
12	1	0	0	1	1	0	0	0	INPUT	INPUT	OUTPUT	OUTPUT
13	1	0	0	1	1	0	0	1	INPUT	INPUT	INPUT	OUTPUT
14	1	0	0	1	1	0	1	0	INPUT	INPUT	OUTPUT	INPUT
15	1	0	0	1	1	0	1	1	INPUT	INPUT	INPUT	INPUT

INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a ONE, $\overline{OBF}$ is a ONE and INTE is a ONE. It is Reset by the falling edge of $\overline{WR}$.

INTE A: Controlled by bit Set/Reset of PC_4.

INTE B: Controlled by bit Set/Reset of PC_2.

Mode 2 (Strobed Bidirectional Bus I/O)

This mode provides a means for communicating with a peripheral device on a single 8-bit bus to facilitate both transmitting and receiving of data (bi-directional bus I/O). Handshaking signals maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-Bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status of the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU for input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full): The $\overline{OBF}$ output will go LOW to indicate that the CPU has written data into Port A.

$\overline{ACK}$ (Acknowledge): A LOW on this input enables the 3-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE1 (The INTE Flip-Flop Associated with OBF): Controlled by bit Set/Reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input): A LOW on this input loads data into the input latch.

IBF (Input Buffer Full F/F): A HIGH on this output indicates that data has been loaded into the input latch.

INTE2 (The INTE Flip-Flop Associated with IBF): Controlled by bit Set/Reset of PC_4.

Figure 8: Mode 1 Input

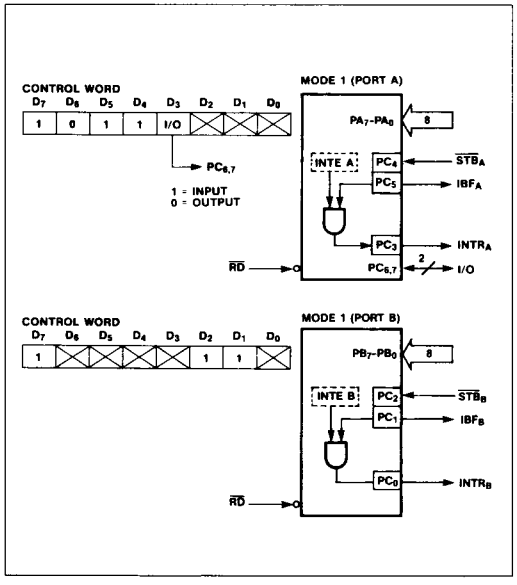
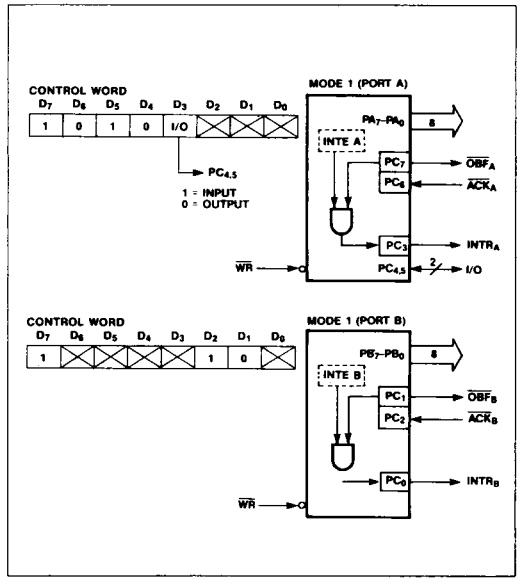


Figure 9: Mode 1 Output



Special Mode Combination Considerations

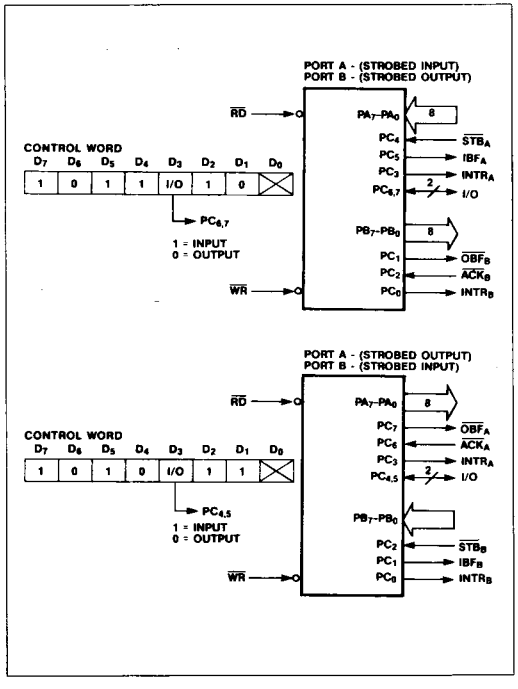
Several combinations of modes are possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a Set Mode command.

The state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus during a read of Port C. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC_2, PC_4, and PC_6 bit positions as shown in Table 4.

Through a Write Port C command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a Write Port C command, and the interrupt enable flags cannot be accessed. The Set/Reset Port C Bit command must be used to write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag.

With a Set/Reset Port C Bit command, any Port C line programmed as an output (including INTR, IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, are not affected by a Set/Reset Port C Bit command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the Set/Reset Port C Bit command will affect the Group A and Group B interrupt enable flags (see Table 5).

Figure 10: Combinations of Mode 1



Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. Thus the KS82C55A can directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the KS82C55A is in Modes 1 or 2, Port C generates or accepts handshaking signals with the peripheral device. Reading Port C allows the programmer to test or verify the status of each peripheral device and change the program flow accordingly.

There is not special instruction to read the status information from Port C. This function is performed by executing a normal read operations of Port C.

Figure 11: Mode Control Word

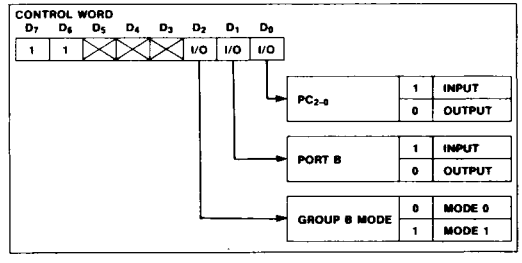


Figure 12: Mode 2

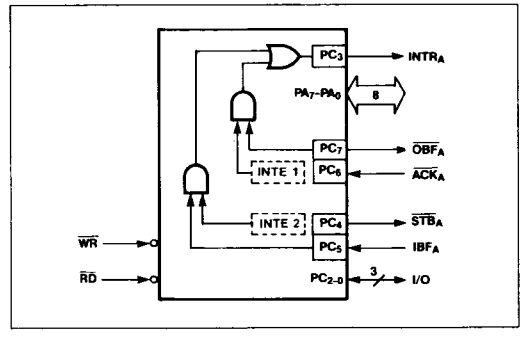


Figure 13: Mode 1/4 Combinations

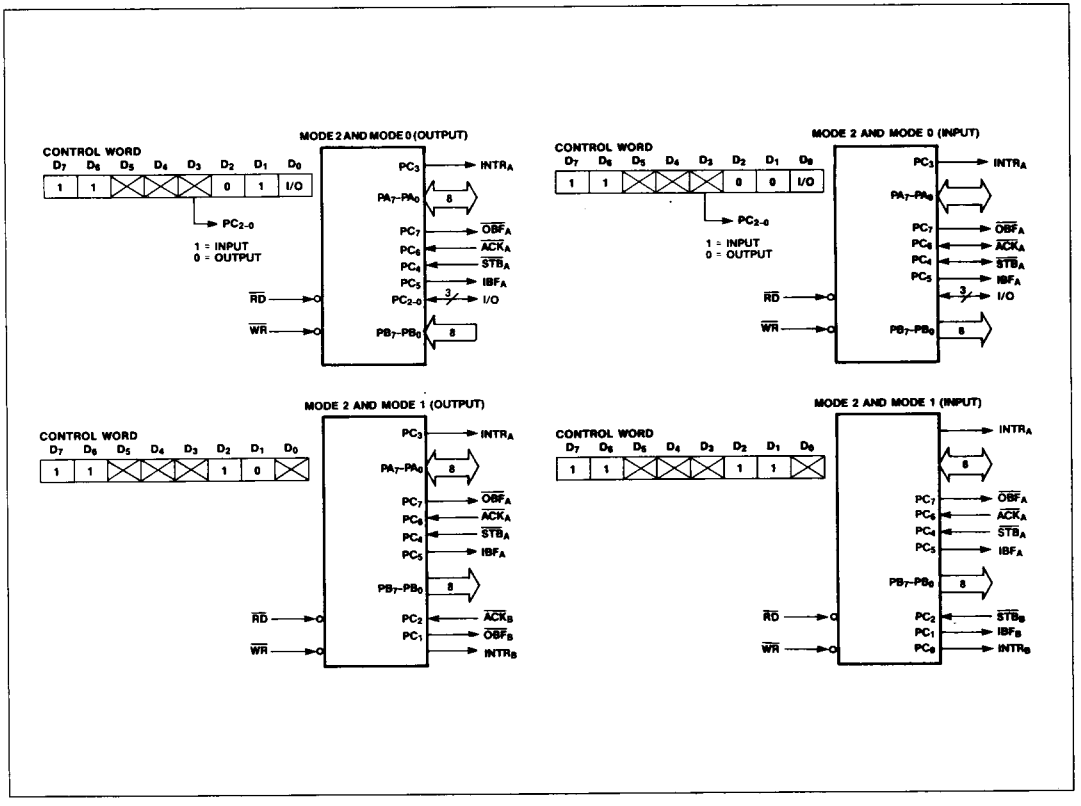


Figure 14: Mode 1 Status Word Format

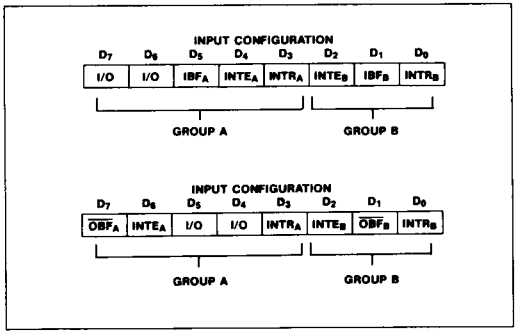


Figure 15: Mode 2 Status Word Format

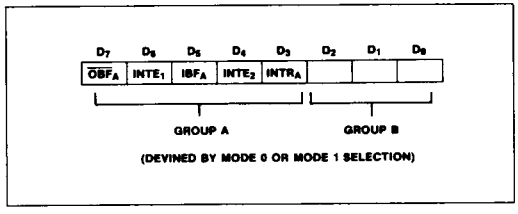


Table 4: Mode Definition Summary

PORT		MODE 0	MODE 1				MODE 2
PORT A	PA_0 PA_1 PA_2 PA_3 PA_4 PA_5 PA_6 PA_7	All IN or All OUT	All IN or All OUT				All BIDIRECTIONAL
PORT B	PB_0 PB_1 PB_2 PB_3 PB_4 PB_5 PB_6 PB_7	All IN or All OUT	All IN or All OUT				MODE 0 or MODE 1 only
			A IN, B IN	A IN, B OUT	A OUT, B IN	A OUT, B OUT	
PORT C	PC_0 PC_1 PC_2 PC_3 PC_4 PC_5 PC_6 PC_7	All IN or All OUT All IN or All OUT	$INTR_B$ IBF_B STB_B $INTR_A$ STB_A IBF_A I/O I/O	$INTR_B$ OBF_B ACK_B $INTR_A$ STB_A IBF_A I/O I/O	$INTR_B$ IBF_B STB_B $INTR_A$ I/O I/O ACK_A OBF_A	$INTR_B$ OBF_B ACK_B $INTR_A$ I/O I/O ACK_A OBF_A	I/O I/O I/O $INTR_A$ STB_A IBF_A ACK_A OBF_A

Table 5: Interrupt Enable Flags in Modes 1 and 2

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (Mode)
$INTE_B$	PC_2	$\overline{ACK}_B$ (Output Mode 1) or STB_B (Input Mode 1)
$INTE_{A2}$	PC_4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
$INTE_{A1}$	PC_6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

APPLICATIONS

The KS82C55A is a very powerful device for interfacing peripheral equipment to the microcomputer system. It is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a service routine associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the KS82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the interface characteristics of the I/O device for both data transfer and timing, and matching this information to the examples and tables in the Operational Description, a Control Word can easily be developed to intialize the KS82C55A to exactly fit the application. Figures 16 through 22 illustrate a few examples of typical KS82C55A applications.

Figure 16: Keyboard and Display Interface

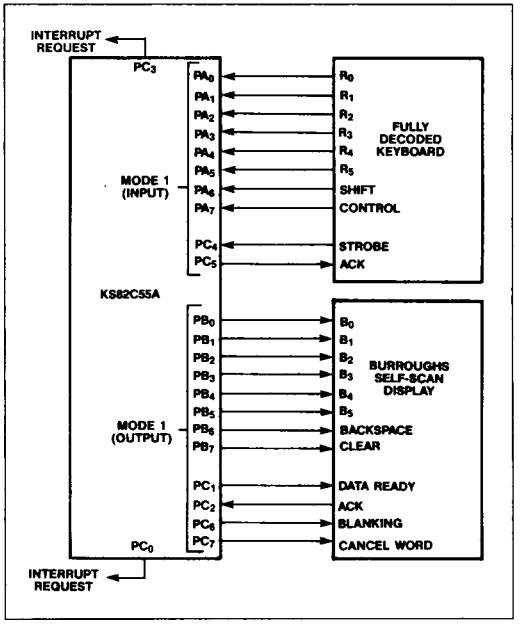


Figure 17: Printer Interface

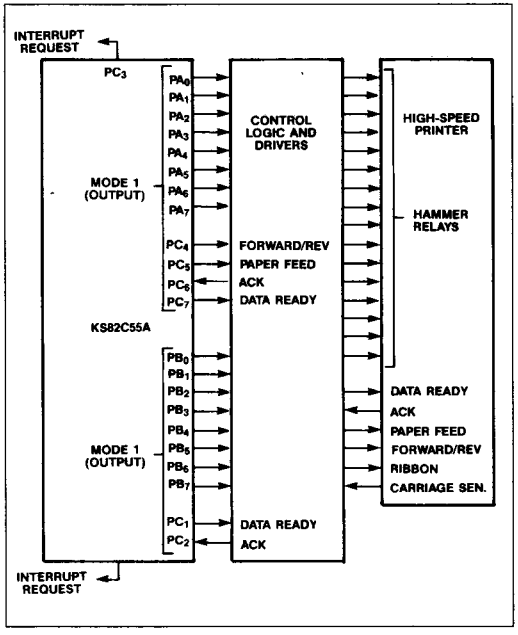


Figure 18: Keyboard and Terminal Address Interface

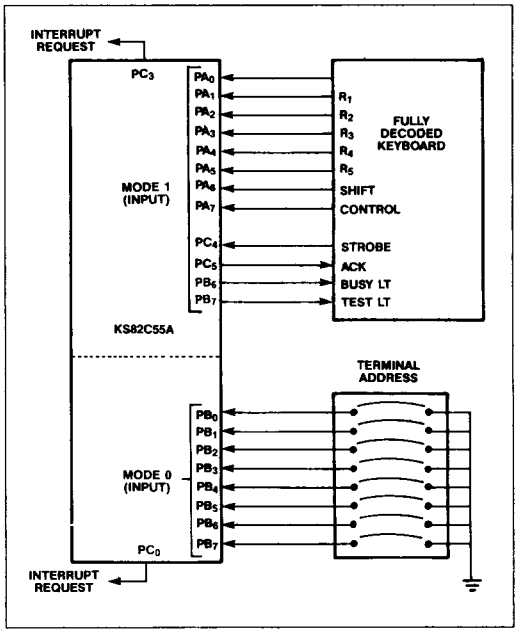


Figure 19: D/A, A/D

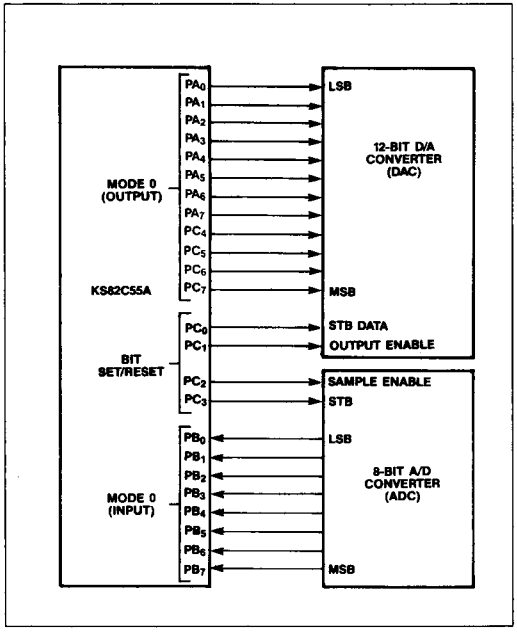


Figure 20: Basic Floppy Disc Interface

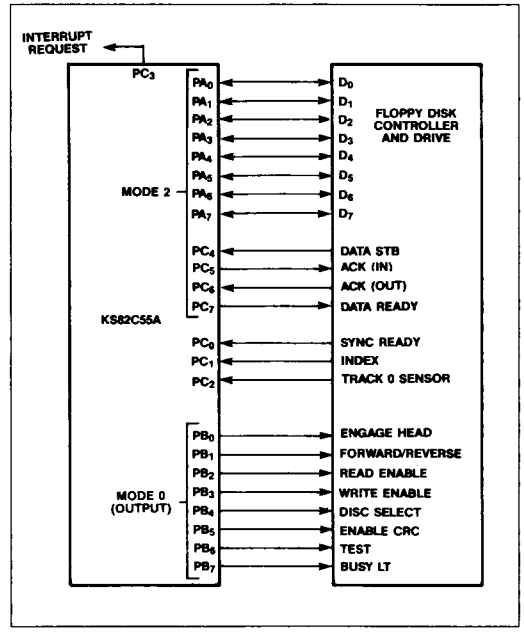


Figure 21: Basic CRT Controller Interface

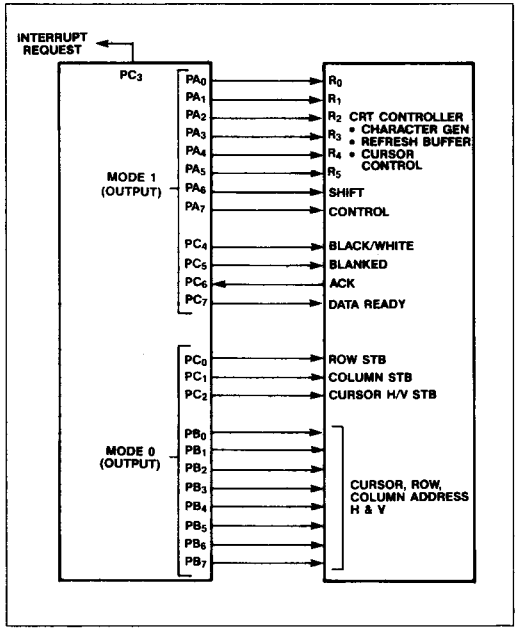


Figure 22: Machine Tool Controller

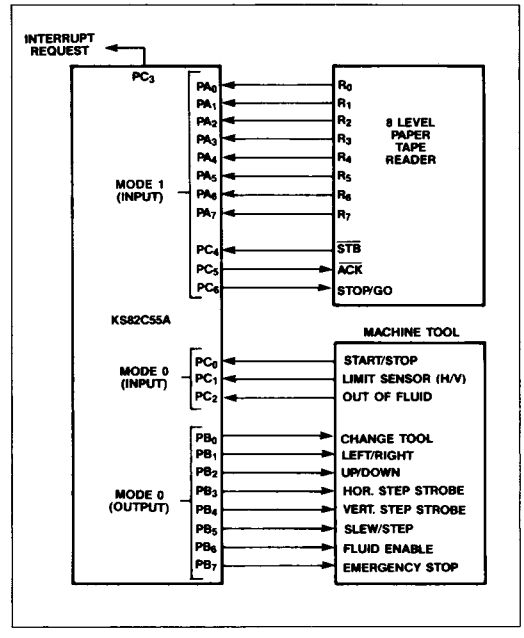


Table 6: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 7: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS} - 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8: Capacitance (T_A = 25°C, V_{CC} = 0V, V_{IN} = +5V or V_{SS})

Symbol	Parameter	Test Conditions	Typ	Units
$C_{I/O}$	I/O Capacitance	Unmeasured Pins Returned to V_{SS}	20	pF
C_{IN}	Input Capacitance		10	pF

Table 9: DC Characterisitcs (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Unit
			Min	Max	
I_{CC}	V_{CC} Supply Current	(Note 3)		10	mA
I_{CCSB}	V_{CC} Supply Current-Standby	V_{CC} = 5.5V, V_{IN} = V_{CC} or V_{SS} Port Conditions: If I/P = Open/High — O/P = Open Only With Data Bus = High/Low — CS = High — Reset = Low Pure Inputs = Low/High		10	μA
I_{DAR}	Darlington Drive Current	Ports A, B, C R_{EXT} = 750Ω, V_{EXT} = 1.5V	±2.5		mA
I_{IL}	Input Leakage Current	V_{IN} = V_{CC} to 0V (Note 1)		±1	μA
I_{OFL}	Output Float Leakage Current	V_{IN} = V_{CC} to 0V (Note 2)		±10	μA
I_{PHH}	Port Hold High Leakage Current	V_{OUT} = 3.0V (Ports A, B, C)	-50	-300	μA
I_{PHHO}	Port Hold High Overdrive Current	V_{OUT} = 3.0V	+350		μA
I_{PHL}	Port Hold Low Leakage Current	V_{OUT} = 1.0V (Port A Only)	+50	+300	μA
I_{PHLO}	Port Hold Low Overdrive Current	V_{OUT} = 0.8V	-350		μA
V_{IH}	Input High Voltage		2.0	V_{CC}	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -2.5mA I_{OH} = -100μA	3.0 V_{CC} - 0.4		V V
V_{OL}	Output LOW Voltage	I_{OL} = 2.5mA		0.4	V

Notes: 1. Pins A1, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Reset. 2. Data Bus; Ports B, C. 3. Outputs Open.

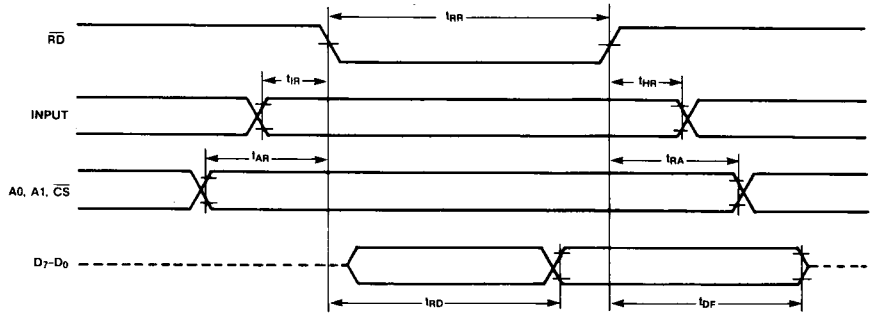
Table 10: AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits (8MHz)		Limits (10MHz)		Units
			Min	Max	Min	Max	
t_{AD}	$\overline{ACK}$ = 0 to Output			175		125	ns
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1			150		100	ns
t_{AK}	$\overline{ACK}$ Pulse Width		200		100		ns
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1			150		100	ns
t_{AR}	Address Strobe Before $\overline{RD}$↓		0		0		ns
t_{AW}	Address Strobe Before $\overline{WR}$↓		0		0		ns
t_{DF}	$\overline{RD}$ ≠ Data Floating $\overline{RD}$↑ to Data Floating		10	75	10	75	ns
t_{DW}	Data Setup Time Before $\overline{WR}$↑		100		50		ns
t_{HR}	Peripheral Data After $\overline{RD}$		0		0		ns
t_{IR}	Peripheral Data Before $\overline{RD}$		0		0		ns
t_{KD}	$\overline{ACK}$ = 1 to Output Float		20	250	20	175	ns
t_{PH}	Peripheral Data After $\overline{STB}$ High		50		40		ns
t_{PS}	Peripheral Data Before $\overline{STB}$ High		20		20		ns
t_{RA}	Address Hold Time After $\overline{RD}$↑		0		0		ns
t_{RD}	Data Delay from $\overline{RD}$↓			120		95	ns
t_{RES}	Reset Pulse Width	See Note 2	500		400		ns
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0			150		120	ns
t_{RIT}	$\overline{RD}$ = 0 to INTR = 0			200		160	ns
t_{RR}	$\overline{RD}$ Pulse Width		150		100		ns
t_{RV}	Recovery Time Between $\overline{RD}$/$\overline{WR}$		200		100		ns
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1			150		100	ns
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1			150		100	ns
t_{ST}	$\overline{STB}$ Pulse Width		100		50		ns
t_{WA}	Address Hold Time After $\overline{WR}$↑	Ports A & B Port C	20 20		10 10		ns ns
t_{WB}	$\overline{WR}$ = 1 to Output			350		150	ns
t_{WD}	Data Hold Time After $\overline{WR}$↑	Ports A & B Port C	30 30		20 20		ns ns
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0	See Note 1		200		160	ns
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0			150		120	ns
t_{WW}	$\overline{WR}$ Pulse Width		100		70		ns

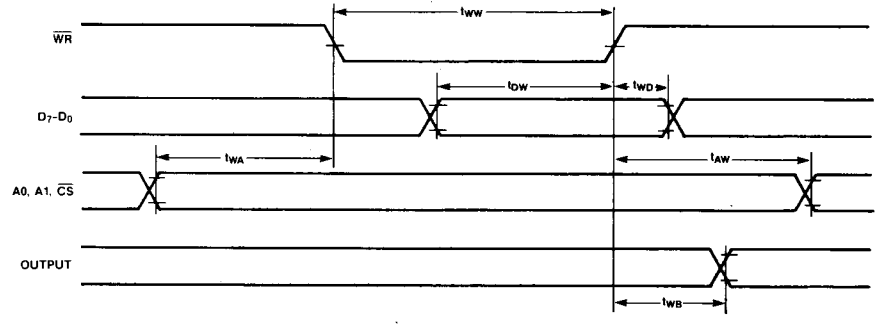
Notes: 1. INTR↑ may occur as early as $\overline{WR}$↓.
2. Width of initial Reset pulse after power on must be at least 50μsec. Subsequent Reset pulses may be 500ns minimum.

Figure 23: Timing Diagrams

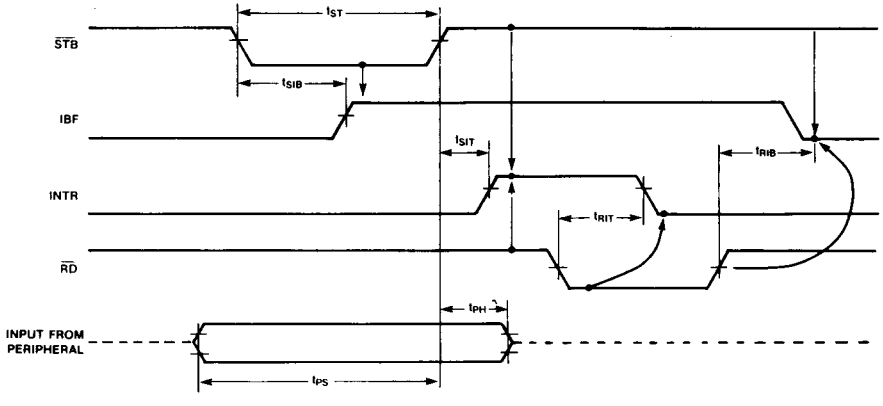
a) Mode 0 (Basic Input)



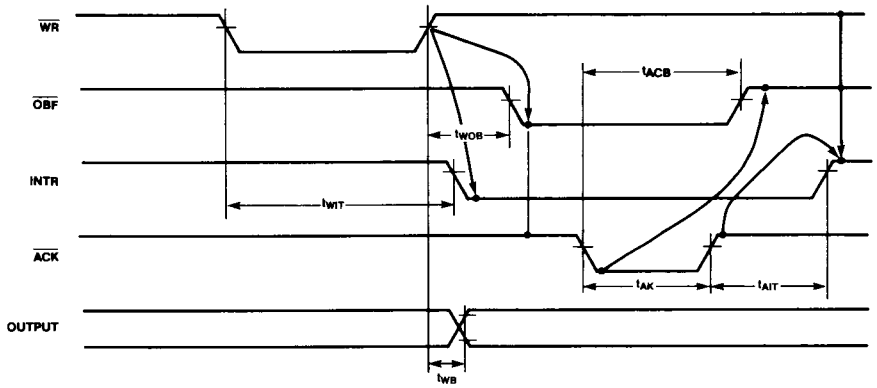
b) Mode 0 (Basic Output)



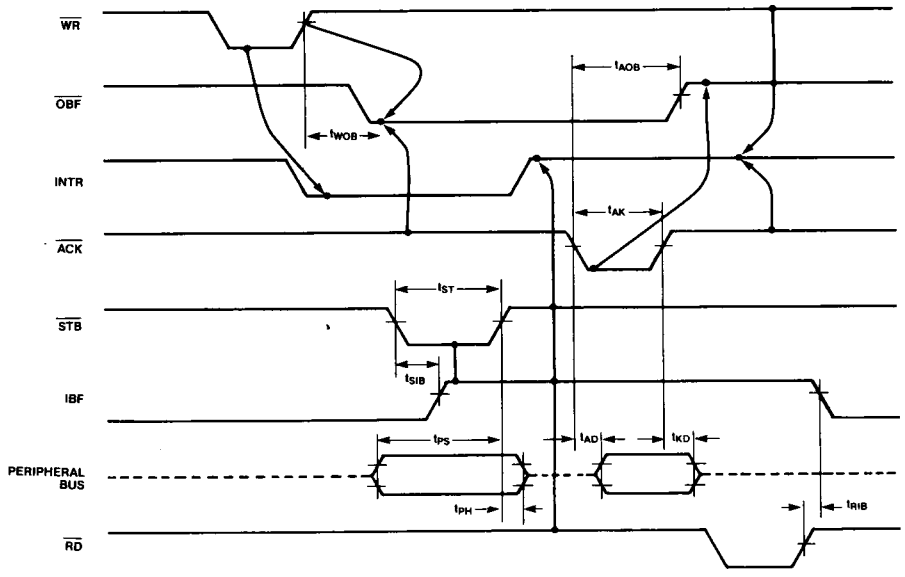
c) Mode 1 (Strobed Input)



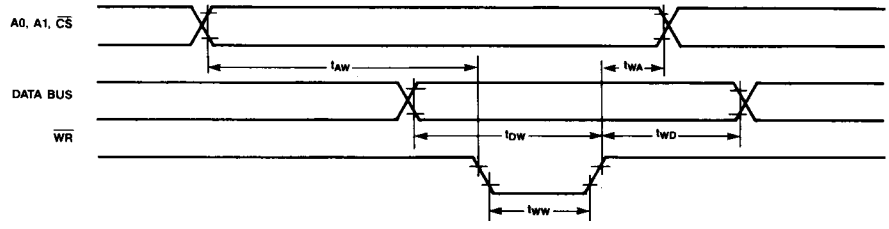
d) Mode 1 (Strobed Output)



e) Mode 2 (Bidirectional)



f) Write Timing



g) Read Timing

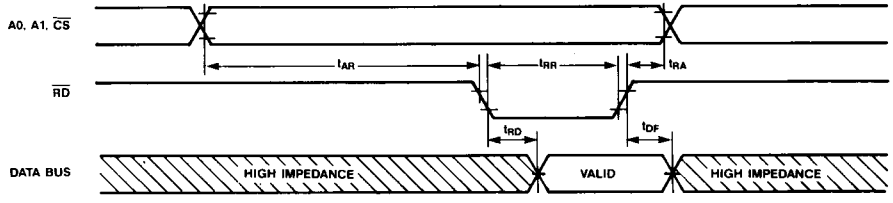
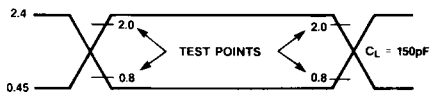
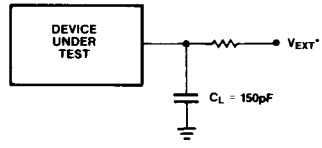


Figure 24: AC Testing I/O Waveform



A.C. Testing Inputs are driven at 2.4V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at 2.0V for a logic 1 and 0.8V for logic 0.

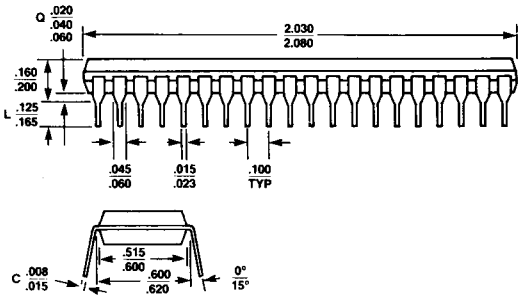
Figure 25: AC Testing Load Circuit



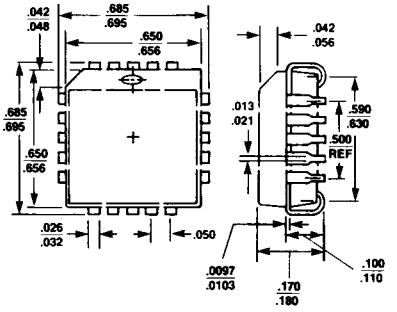
* V_{EXT} is set at various voltages during testing to guarantee the specification. C_L includes jig capacitance.

PACKAGE DIMENSIONS

Units: Inches



Plastic Package



PLCC Package

ORDERING INFORMATION & PRODUCT CODE DIMENSIONS

KS 82C55A X X X

SAMSUNG SEMICONDUCTOR

Part Number

Speed
-8 8MHz
-10 10MHz

Packaging
P — Plastic DIP
L — Plastic Leaded Chip Carrier (PLCC)

Temperature
C — Commercial (0°C to +70°C)
I — Industrial (–40°C to +85°C)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Products Group.