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RTL8201F-CG
RTL8201FN-CG
RTL8201FL-CG

SINGLE-CHIP/PORT 10/100MBPS ETHERNET PHYCEIVER

PRELIMINARY DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.7	2010/03/15	Preliminary release.
0.8	2010/06/25	Added RTL8201FL-GR product information. Revised section 7 Register Descriptions, page 14. Revised section 8.5 LED Functions, page 27. Added section 8.10 Automatic Polarity Correction, page 32. Added section 8.12 Wake-On-LAN (WOL), page 33. Revised section 9.1.3 Power On and PHY Reset Sequence, page 39. Revised section 9.3 Crystal Characteristics, page 47. Revised Table 45 Oscillator Requirements, page 48. Added section 9.5 Clock Requirements, page 48. Revised section 10.2 RTL8201FN (QFN-48), page 50. Added 11.1 RTL8201F Series Selection Guide, page 52.
0.9	2010/07/16	Revised section 9.1.3 Power On and PHY Reset Sequence, page 39. Revised section 9.2 AC Characteristics, page 41. Added Table 22 Page4 Register 16 EEE Capability Enable Register, page 19. Added Table 23 Page4 Register 21 EEE Capability Register, page 20.
0.91	2010/08/11	Revised section 9.2.3 RMII Transmission and Reception Cycle Timing, page 45.

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1. General Description

The RTL8201F/RTL8201FN/RTL8201FL-CG are single-chip/single-port 10/100Mbps Ethernet PHYceivers that support:

- MII (Media Independent Interface)
- RMII (Reduced Media Independent Interface)

The RTL8201F/FN/FL implements all 10/100M Ethernet Physical-layer functions including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD), 10Base-TX Encoder/Decoder, and Twisted-Pair Media Access Unit (TPMAU). The RTL8201F/FN/FL also support auto MDIX.

A PECL (Pseudo Emitter Coupled Logic) interface is supported to connect with an external 100Base-FX fiber optical transceiver. The chip utilizes an advanced CMOS process to meet low voltage and low power requirements. With on-chip DSP (Digital Signal Processing) technology, the chip provides excellent performance under all operating conditions.

Note: Version differences are listed in section 11 Ordering Information, page 52.

2. Features

- Supports IEEE 802.3az Draft 3.2 (EEE)
- 100Base-TX IEEE 802.3u Compliant
- 10Base-T IEEE 802.3 Compliant
- Supports MII mode
- Supports RMII mode
- Full/half duplex operation
- Twisted pair or fiber mode output
- Supports Auto-Negotiation
- Supports power down mode
- Supports Link Down Power Saving
- Supports Base Line Wander (BLW) compensation
- Supports auto MDIX
- Supports Interrupt function
- Supports Wake-On-LAN (WOL) (RTL8201FN only)
- Adaptive Equalization
- Automatic Polarity Correction
- LEDs
  - RTL8201F and RTL8201FL provides two network status LEDs
  - RTL8201FN provide three network status LEDs
- Supports flow control
- Supports 25MHz external crystal or OSC
- Supports 50MHz external Clock input
- Provides 50MHz clock source for MAC
- Low power supply 1.05V and 3.3V; 1.05V is generated by an internal regulator
- 0.11µm CMOS process
- Packages:
  - 32-pin MII/RMII QFN 'Green' package (RTL8201F)
  - 48-pin MII/RMII QFN 'Green' package (RTL8201FN)
  - 48-pin MII/RMII LQFP 'Green' package (RTL8201FL)

3. Applications

- DTV (Digital TV)
- MAU (Media Access Unit)
- CNR (Communication and Network Riser)
- Game Console
- Printer and Office Machine
- DVD Player and Recorder
- Ethernet Hub
- Ethernet Switch

In addition, the RTL8201F/FN/FL can be used in any embedded system with an Ethernet MAC that needs a UTP physical connection or Fiber PECL interface to an external 100Base-FX optical transceiver module.

4. Block Diagram

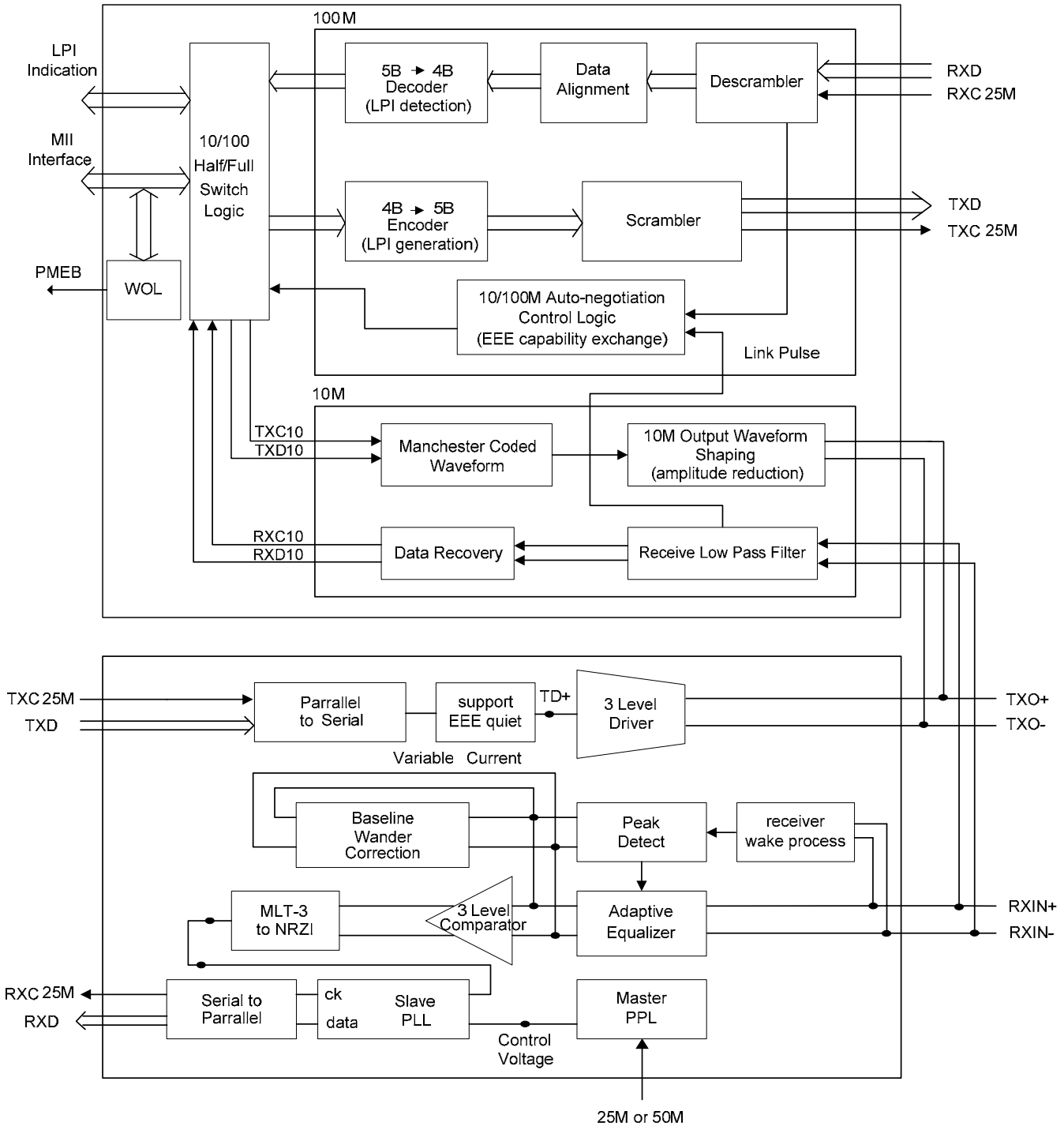


Figure 1. Block Diagram

5. Pin Assignments

5.1. RTL8201F (32-Pin)

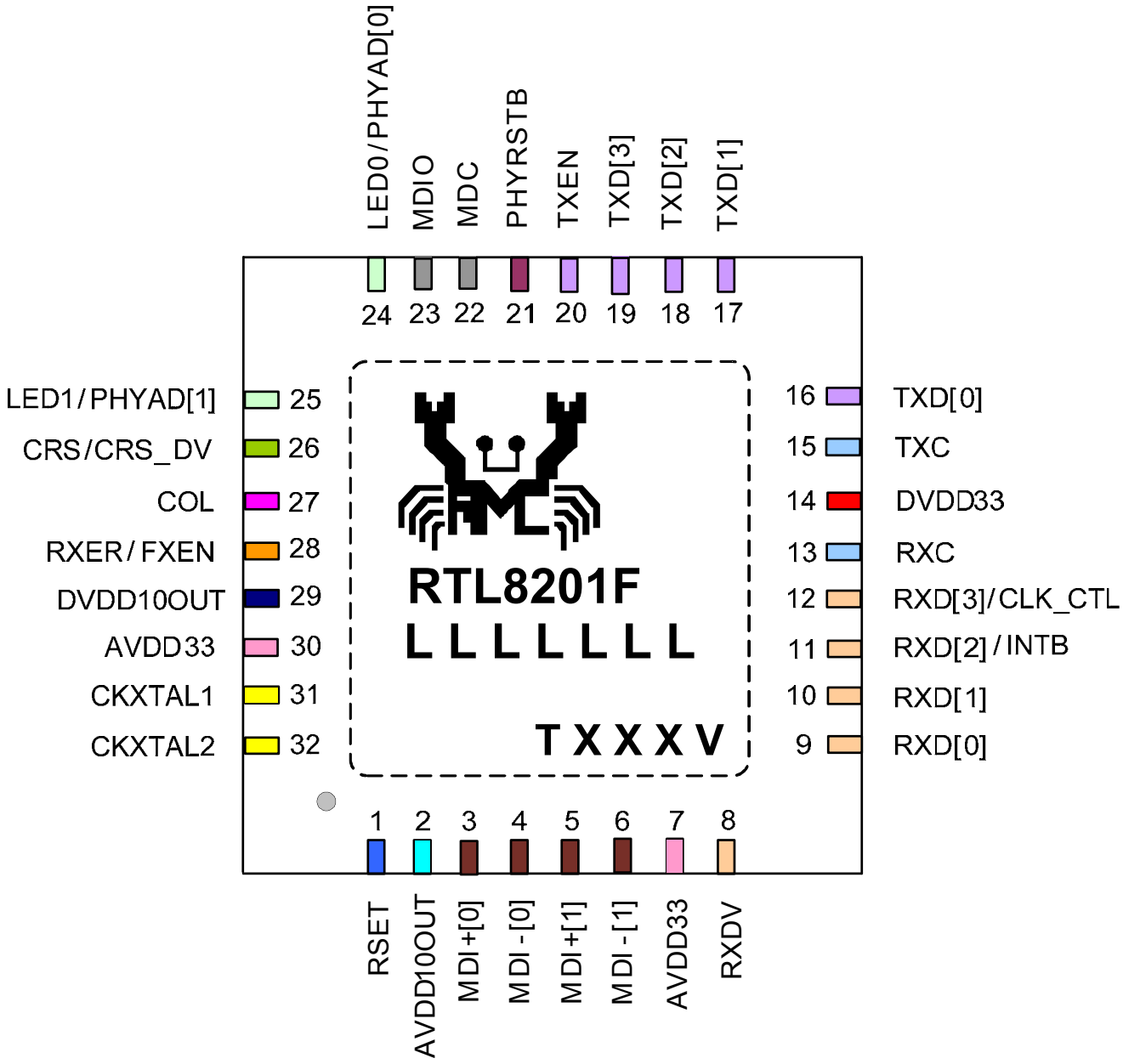


Figure 2. RTL8201F QFN-32 Pin Assignments

5.2. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 2. The version is shown in the location marked 'V'.

5.3. RTL8201FN (48-Pin)

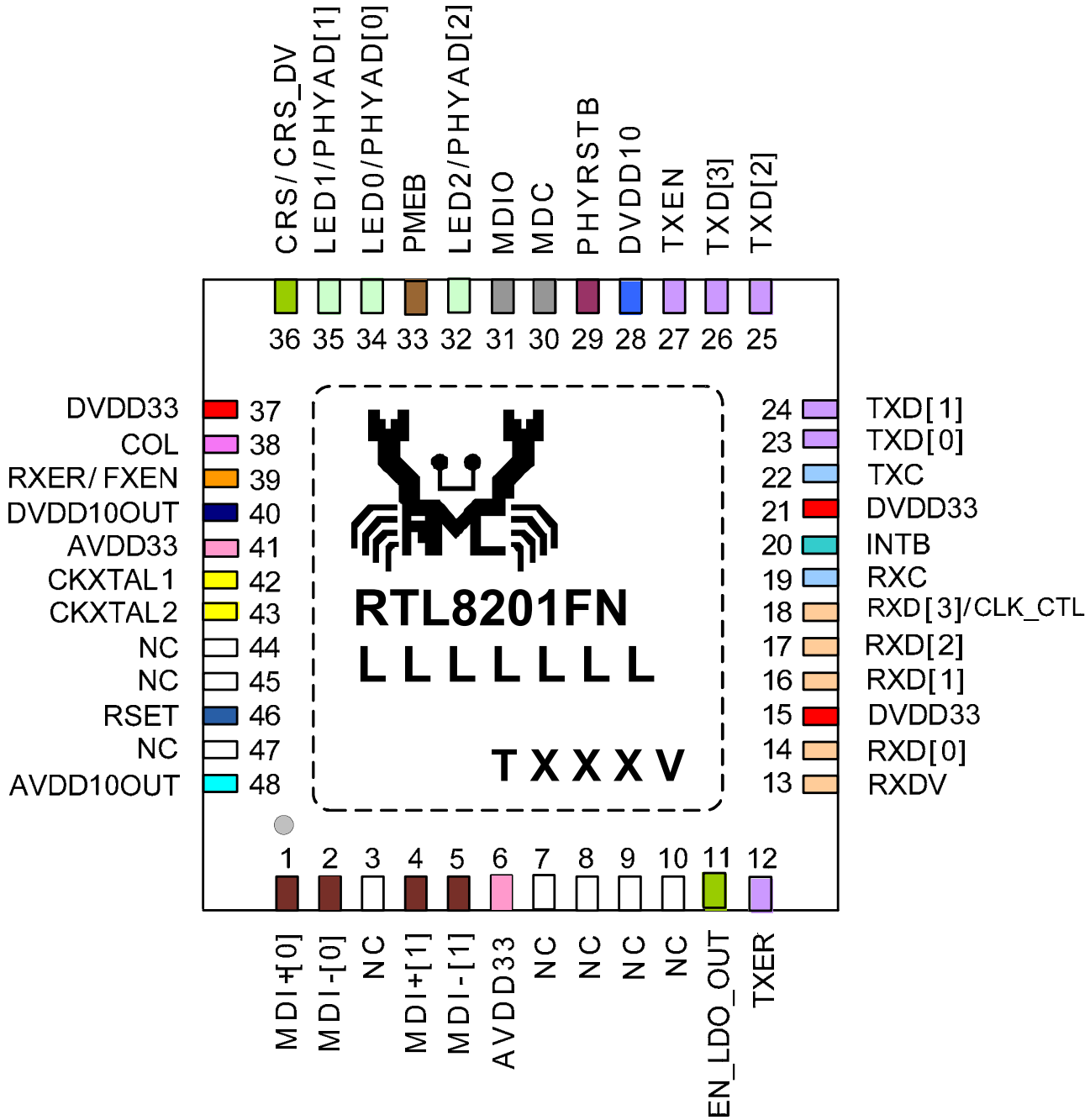


Figure 3. RTL8201FN QFN-48 Pin Assignments

5.4. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3. The version is shown in the location marked 'V'.

5.5. RTL8201FL (48-Pin)

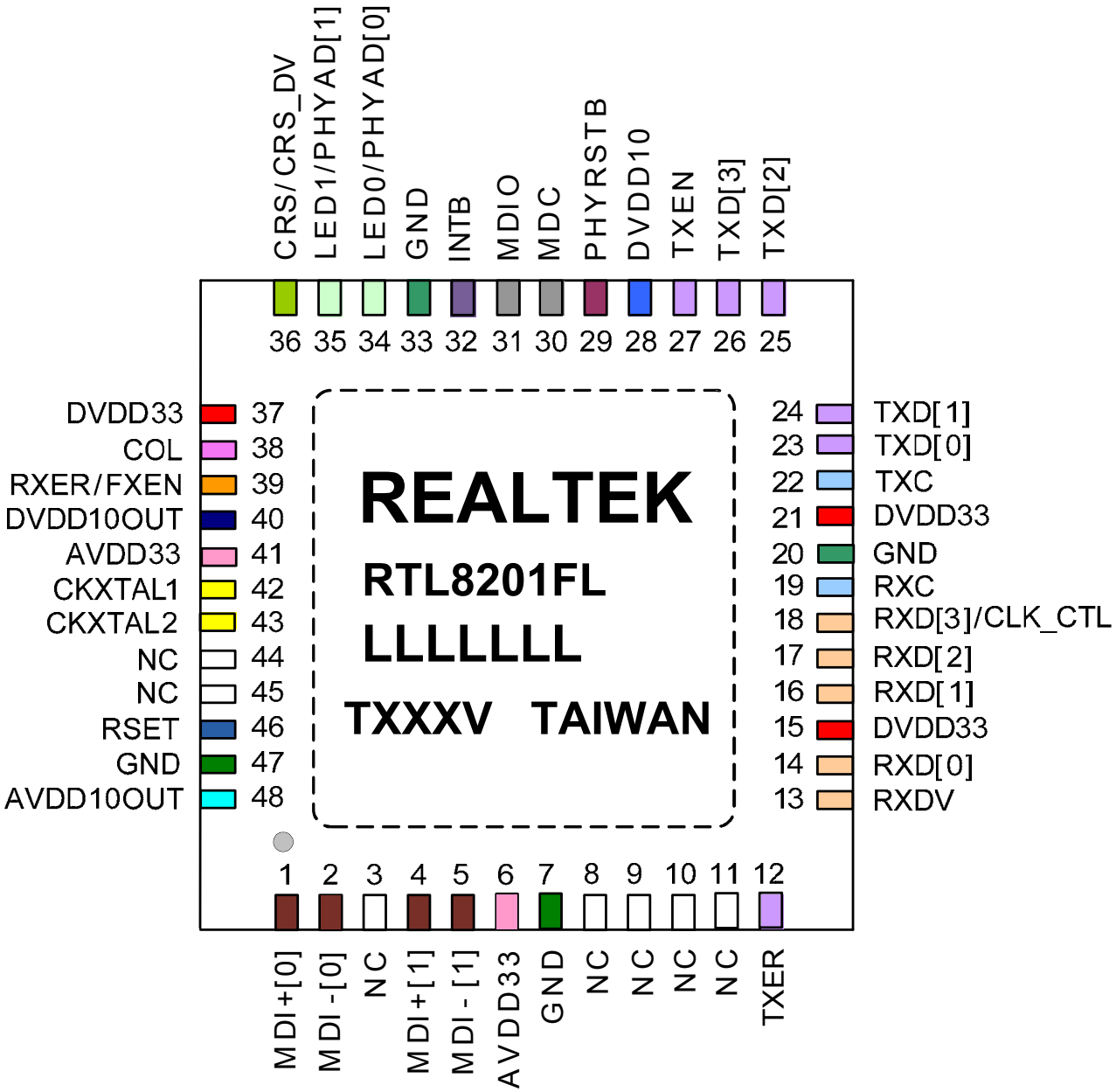


Figure 4. RTL8201FL LQFP-48 Pin Assignments

5.6. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 4. The version is shown in the location marked 'V'.

6. Pin Descriptions

I: Input

O: Output

P: Power

PU: Internal Pull up during power on reset

D: Open Drain output

LI: Latched Input during Power up or Reset

IO: Bi-directional input and output

HZ: High impedance during power on reset

PD: Internal Pull down during power on reset

6.1. MII Interface

Table 1. MII Interface

Name	Type	Pin No. (8201F)	Pin No. (8201FN)	Pin No. (8201FL)	Description
TXC	O/PD	15	22	22	Transmit Clock. This pin provides a continuous clock as a timing reference for TXD [3:0] and TXEN signals. TXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode.
TXEN	I/PD	20	27	27	Transmit Enable. The input signal indicates the presence of valid nibble data on TXD [3:0]. An internal weakly pulled low resistor prevents the bus floating.
TXER	I/PD	-	12	12	Transmit Error.
TXD[0] TXD[1] TXD[2] TXD[3]	I/PD I/PD I/PD I/PD	16 17 18 19	23 24 25 26	23 24 25 26	Transmit Data. The MAC will source TXD [0:3] synchronous with TXC when TXEN is asserted. An internal weakly pulled low resistor prevents the bus floating.
RXC	O/PD	13	19	19	Receive Clock. This pin provides a continuous clock reference for RXDV and RXD [0:3] signals. RXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode.
COL	LI/O/PD	27	38	38	Collision Detect. COL is asserted high when a collision is detected on the media.
CRS/ CRS_DV	O/PD	26	36	36	Carrier Sense. This pin's signal is asserted high if the media is not in Idle state.

Name	Type	Pin No. (8201F)	Pin No. (8201FN)	Pin No. (8201FL)	Description
RXDV	LI/O/PD	8	13	13	Receive Data Valid. This pin's signal is asserted high when received data is present on the RXD [3:0] lines. The signal is de-asserted at the end of the packet. The signal is valid on the rising edge of the RXC. This pin should be pulled low when operating in MII mode. 0: MII mode 1: RMII mode An internal weakly pulled low resistor sets this to the default of MII mode. It is possible to use an external 4.7KΩ pulled high resistor to enable RMII mode. After power on, the pin operates as the Receive Data Valid pin.
RXD[0] RXD[1] RXD[2] RXD[2]/ INTB	O/PD	9 10 - 11	14 16 17 -	14 16 17 -	Receive Data. These are the four parallel receive data lines aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY). *Note: The RTL8201F Pin11 is named RXD[2]/INTB. When in RMII mode, this pin is used for the interrupt function. See Table 8, page 13 for INTB descriptions.*
RXD[3]/ CLK_CTL	LI/O/PU	12	18	18	Receive Data. This is the parallel receive data line aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY). RXD[3]/CLK_CTL pin is the Hardware strap in RMII Mode. 1: REF_CLK input mode 0: REF_CLK output mode
RXER/ FXEN	LI/O/PD	28	39	39	Receive Error. If a 5B decode error occurs, such as invalid /J/K/, invalid /T/R/, or invalid symbol, this pin will go high. Fiber/UTP Enable. This pin's status is latched at power on reset to determine the media mode to operate in. 1: Fiber mode 0: UTP mode An internal weakly pulled low resistor sets this to the default of UTP mode. It is possible to use an external 4.7KΩ pulled high resistor to enable fiber mode. After power on, the pin operates as the Receive Error pin.

6.2. Serial Management Interface

Table 2. Serial Management Interface

Name	Type	Pin No. (8201F)	Pin No. (8201FN)	Pin No. (8201FL)	Description
MDC	I/PU	22	30	30	Management Data Clock. This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks. The clock rate can be up to 2.5MHz. Use an internal weakly pulled high resistor to prevent the bus floating.
MDIO	IO/PU	23	31	31	Management Data Input/Output. This pin provides the bi-directional signal used to transfer management information.

6.3. RMII Interface

Table 3. RMII Interface

Name	Type	Pin No. (8201F)	Pin No. (8201FN)	Pin No. (8201FL)	Description
TXC	IO/PD	15	22	22	Synchronous 50MHz Clock Reference for Receive, Transmit, and Control Interface. The direction is decided by Page 0 Register 25. The default direction is reference clock input mode.
CRS/ CRS_DV	O/PD	26	36	36	Carrier Sense/Receive Data Valid. CRS_DV shall be asserted by the PHY when the receive medium is non-idle.
TXEN	I/PD	20	27	27	Transmit Enable.
TXD[0:1]	I/PD	16, 17	23, 24	23, 24	Transmit Data.
RXD[0:1]	O/PD	9, 10	14, 16	14, 16	Receive Data.
RXER/ FXEN	LI/O/PD	28	39	39	Receive Error. RX_ER is a required output of the PHY, but is an optional input for the MAC.

6.4. Clock Interface

Table 4. Clock Interface

Name	Type	Pin No. (8201F)	Pin No. (8201FN)	Pin No. (8201FL)	Description
CKXTAL2	O	32	43	43	25MHz Crystal Output. This pin provides the 25MHz crystal output. If an external 25MHz/50MHz oscillator or clock is used, connect CKXTAL2 to the oscillator or clock output (see section 9.4 Oscillator Requirements, page 48).
CKXTAL1	I	31	42	42	25MHz Crystal Input. This pin provides the 25MHz crystal input. It must be left open when an external 25MHz/50MHz oscillator or clock drives CKXTAL2.

6.5. 10Mbps/100Mbps Network Interface

Table 5. 10Mbps/100Mbps Network Interface

Name	Type	Pin No. (8201F)	Pin No. (8201FN)	Pin No. (8201FL)	Description
MDI+[0] MDI-[0]	IO	3 4	1 2	1 2	Transmit Output. Differential transmit output pair shared by 100Base-TX, 100Base-FX, and 10Base-T modes. When configured as 100Base-TX, output is an MLT-3 encoded waveform. When configured as 100Base-FX, the output is pseudo-ECL level.
RSET	I	1	46	46	Transmit Bias Resistor Connection. This pin should be pulled to GND by a 2.49KΩ (1%) resistor to define driving current for the transmit DAC. The resistance value may be changed, depending on experimental results of the RTL8201F.
MDI+[1] MDI-[1]	IO	5 6	4 5	4 5	Receive Input. Differential receive input pair shared by 100Base-TX, 100Base-FX, and 10Base-T modes.

6.6. Device Configuration Interface

Table 6. Device Configuration Interface

Name	Type	Pin No. (8201F)	Pin No. (8201FN)	Pin No. (8201FL)	Description
RXDV	LI/O/ PD	8	13	13	Receive Data Valid. This pin's signal is asserted high when received data is present on the RXD [3:0] lines. The signal is de-asserted at the end of the packet. The signal is valid on the rising edge of the RXC. This pin should be pulled low when operating in MII mode. 0: MII mode 1: RMII mode An internal weakly pulled low resistor sets this to the default of MII mode. It is possible to use an external 4.7KΩ pulled high resistor to enable RMII mode. After power on, the pin operates as the Receive Data Valid pin.
LED0/ PHYAD[0] LED1/ PHYAD[1] LED2/ PHYAD[2]	LI/O/ HZ	24 25 -	34 35 32	34 35 -	PHY Address and Customized LED Settings. Sets the PHY address for the device. Traditional LED Function selection.

LED [1:0]	00	01	10	11
LED0	ACT_{ALL}	$Link_{ALL}$/ ACT_{ALL}	Link10/ ACT_{ALL}	LINK10 /ACT_{10}
LED1	LINK100	LINK100	LINK100	LINK10 0/ACT_{100}
LED2	Reserved	Reserved	Reserved	Reserved

Name	Type	Pin No. (8201F)	Pin No. (8201FN)	Pin No. (8201FL)	Description
RXD[3]/ CLK_CTL	LI/O/PU	12	18	18	Receive Data. This is the parallel receive data line aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY). RXD [3]/CLK_CTL pin is the Hardware strap in RMII Mode. 1: REF_CLK input mode 0: REF_CLK output mode
CLK_CTL	LI/O/PU	-	-	-	This Pin is the Hardware Strap in RMII Mode. 1: REF_CLK input mode 0: REF_CLK output mode
RXER/ FXEN	LI/O/PD	28	39	39	Fiber/UTP Interface. This pin's status is latched at power on reset to determine the media mode to operate in. 1: Fiber mode 0: UTP mode An internal weakly pulled low resistor sets this to the default of UTP mode. It is possible to use an external 4.7KΩ pulled high resistor to enable fiber mode.
EN_LDO_ OUT	LI/O/ PU	-	11	-	LDO Mode Strap 1: LDO enable 2: LDO disable

6.7. Power and Ground Pins

Table 7. Power and Ground Pins

Name	Type	Pin No. (8201F)	Pin No. (8201FN)	Pin No. (8201FL)	Description
AVDD33	P	7, 30	6, 41	6, 41	3.3V Analog Power Input. 3.3V power supply for analog circuit; should be well decoupled.
DVDD33	P	14	15, 21, 37	15, 21, 37	3.3V Digital Power Input. 3.3V power supply for digital circuit.
DVDD10	P	-	28	28	1.05V Digital Power.
AVDD10OUT	O	2	48	48	Power Output. Be sure to connect a 0.1µF ceramic capacitor for decoupling purposes. The connection method is outlined in 8.9 3.3V Power Supply and Voltage Conversion Circuit, page 32.
DVDD10OUT	O	29	40	40	Power Output. Be sure to connect a 0.1µF ceramic capacitor for decoupling purposes. The connection method is outlined in 8.9 3.3V Power Supply and Voltage Conversion Circuit, page 32.
GND	P	-	-	7, 20, 33, 47	Ground. Should be connected to a larger GND plane.

6.8. Reset and Other Pins

Table 8. Reset and Other Pins

Name	Type	Pin No. (8201F)	Pin No. (8201FN)	Pin No. (8201FL)	Description
PHYRSTB	I/HZ	21	29	29	RESETB. Set low to reset the chip. For a complete reset, this pin must be asserted low for at least 10ms.
INTB	D	-	20	32	Interrupt. Set low if link status changed, duplex changed, or auto negotiation failed. Active Low. This pin is an open-drain design, and for default value should be pulled high by an external 4.7KΩ. If not used, keep floating.
RXD[2]/INTB	O/PD	11	-	-	Interrupt. Set low if link status changed, duplex changed, or auto negotiation failed. Active Low. This pin is an open-drain design, and for default value should be pulled high by an external 4.7KΩ. If not used, keep floating. *Note: This pin is used for the interrupt function only when in the RMII mode.*
PMEB	O	-	33	-	Power Management Enable Set low if received a magic packet or wake up frame; active low.

6.9. NC (Not Connected) Pins

Table 9. NC (Not Connected) Pins

Name	Type	Pin No. (8201F)	Pin No. (8201FN)	Pin No. (8201FL)	Description
NC	-	-	3, 7, 8, 9, 10, 44, 45, 47	3, 8, 9, 10, 11, 44, 45	Not Connected.

7. Register Descriptions

This section describes the functions and usage of the registers available in this file. In this section the following abbreviations are used.

RW: Read/Write

RW/EFUS: Read/Write/eFUSE burnable

RO: Read Only

RW/LI: Read/Write/Latch in

7.1. Register 0 Basic Mode Control Register

Table 10. Register 0 Basic Mode Control Register

Address	Name	Description	Mode	Default
0:15	Reset	This bit sets the status and control registers of the PHY in the default state. This bit is self-clearing. 1: Software reset 0: Normal operation	RW	0
0:14	Loopback	This bit enables loopback of transmit data nibbles TXD3:0 to the receive data path. 1: Enable loopback 0: Normal operation	RW	0
0:13	Speed Selection	This bit sets the network speed. 1: 100Mbps 0: 10Mbps After completing auto negotiation, this bit will reflect the Speed status. 1: 100Base-T 0: 10Base-T When 100Base-FX mode is enabled, this bit=1 and is read only.	RW	1
0:12	Auto Negotiation Enable	This bit enables/disables the NWay auto-negotiation function. 1: Enable auto-negotiation; bits 0:13 and 0:8 will be ignored 0: Disable auto-negotiation; bits 0:13 and 0:8 will determine the link speed and the data transfer mode, respectively When 100Base-FX mode is enabled, this bit=0 and is read only.	RW	1
0:11	Power Down	This bit turns down the power of the PHY chip, including the internal crystal oscillator circuit. The MDC, MDIO is still alive for accessing the MAC. 1: Power down 0: Normal operation	RW	0
0:10	Isolate	1: Electrically isolate the PHY from MII/GMII/RGMII/RSGMII. PHY is still able to respond to MDC/MDIO. 0: Normal operation	RW	0
0:9	Restart Auto Negotiation	This bit allows the NWay auto-negotiation function to be reset. 1: Re-start auto-negotiation 0: Normal operation	RW	0
0:8	Duplex Mode	This bit sets the duplex mode if auto-negotiation is disabled (bit 0:12=0). 1: Full duplex 0: Half duplex After completing auto-negotiation, this bit will reflect the duplex status. 1: Full duplex 0: Half duplex	RW	1
0:7~0	Reserved	Reserved.	-	-

7.2. Register 1 Basic Mode Status Register

Table 11. Register 1 Basic Mode Status Register

Address	Name	Description	Mode	Default
1:15	100Base-T4	1: Enable 100Base-T4 support 0: Suppress 100Base-T4 support	RO	0
1:14	100Base_TX_FD	1: Enable 100Base-TX full duplex support 0: Suppress 100Base-TX full duplex support	RO	1
1:13	100Base_TX_HD	1: Enable 100Base-TX half duplex support 0: Suppress 100Base-TX half duplex support	RO	1
1:12	10Base_T_FD	1: Enable 10Base-T full duplex support 0: Suppress 10Base-T full duplex support	RO	1
1:11	10_Base_T_HD	1: Enable 10Base-T half duplex support 0: Suppress 10Base-T half duplex support	RO	1
1:10~7	Reserved	Reserved.	-	-
1:6	MF Preamble Suppression	The RTL8201F/FN/FL will accept management frames with preamble suppressed. A minimum of 32 preamble bits are required for the first management interface read/write transaction after reset. One idle bit is required between any two management transactions as per IEEE 802.3u specifications.	RO	1
1:5	Auto Negotiation Complete	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	RO	0
1:4	Remote Fault	1: Remote fault condition detected (cleared on read) 0: No remote fault condition detected When in 100Base-FX mode, this bit means an in-band signal Far-End-Fault has been detected (see 8.11 Far End Fault Indication, page 32).	RO	0
1:3	Auto-Negotiation Ability	1: PHY is able to perform auto-negotiation 0: PHY is not able to perform auto-negotiation	RO	1
1:2	Link Status	1: Valid link established 0: No valid link established	RO	0
1:1	Jabber Detect	1: Jabber condition detected 0: No jabber condition detected	RO	0
1:0	Extended Capability	1: Extended register capable (permanently=1) 0: Not extended register capable	RO	1

7.3. Register 2 PHY Identifier Register 1

Table 12. Register 2 PHY Identifier Register 1

Address	Name	Description	Mode	Default
2:15~0	OUI	Composed of the 6th to 21st bits of the Organizationally Unique Identifier (OUI), respectively.	RO	001Ch

7.4. Register 3 PHY Identifier Register 2

Table 13. Register 3 PHY Identifier Register 2

Address	Name	Description	Mode	Default
3:15~10	OUI_LSB	Assigned to the 0 through 5th bits of the OUI.	RO	110010
3:9~4	Model Number	Model Number	RO	000001
3:3~0	Revision Number	Revision Number	RO	0110

7.5. Register 4 Auto-Negotiation Advertisement Register (ANAR)

This register contains the advertised abilities of this device as they will be transmitted to its link partner during auto-negotiation.

Table 14. Register 4 Auto-Negotiation Advertisement Register (ANAR)

Address	Name	Description	Mode	Default
4:15	Next Page	Next Page Bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page	RO	0
4:14	Acknowledge	1: Acknowledge reception of link partner capability data word 0: Do not acknowledge reception	RO	0
4:13	Remote Fault	1: Advertise remote fault detection capability 0: Do not advertise remote fault detection capability	RW	0
4:12~11	Reserved	Reserved.	-	-
4:10	Pause	1: Advertises that the mac2 has flow control capability 0: Without flow control capability	RW	0
4:9	100Base-T4	1: 100Base-T4 is supported by local node 0: 100Base-T4 not supported by local node	RO	0
4:8	100Base-TX-FD	1: 100Base-TX full duplex is supported by local node 0: 100Base-TX full duplex not supported by local node	RW	1
4:7	100Base-TX	1: 100Base-TX is supported by local node 0: 100Base-TX not supported by local node	RW	1
4:6	10Base-T-FD	1: 10Base-T full duplex supported by local node 0: 10Base-T full duplex not supported by local node	RW	1
4:5	10Base-T	1: 10Base-T is supported by local node 0: 10Base-T not supported by local node	RW	1
4:4~0	Selector Field	Binary Encoded Selector Supported by This Node. Currently only CSMA/CD 00001 is specified. No other protocols are supported.	RW	00001

7.6. Register 5 Auto-Negotiation Link Partner Ability Register (ANLPAR)

This register contains the advertised abilities of the Link Partner as received during auto-negotiation. The content changes after a successful auto-negotiation if Next-pages are supported.

Table 15. Register 5 Auto-Negotiation Link Partner Ability Register (ANLPAR)

Address	Name	Description	Mode	Default
5:15	Next Page	Next Page Bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page	RO	0
5:14	Acknowledge	1: Link partner acknowledges reception of local node's capability data word 0: No acknowledgement	RO	0
5:13	Remote Fault	1: Link partner is indicating a remote fault 0: Link partner is not indicating a remote fault	RO	0
5:12	Reserved	Reserved.	-	-
5:11	Asymmetric Pause	1: Asymmetric Flow control supported by Link Partner 0: No Asymmetric flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability.	RO	0
5:10	Pause	1: Flow control supported by Link Partner 0: No flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability (read only).	RO	0
5:9	100Base-T4	1: 100Base-T4 is supported by link partner 0: 100Base-T4 not supported by link partner	RO	0
5:8	100Base-TX-FD	1: 100Base-TX full duplex is supported by link partner 0: 100Base-TX full duplex not supported by link partner	RO	0
5:7	100Base-TX	1: 100Base-TX is supported by link partner 0: 100Base-TX not supported by link partner This bit will also be set if the link in 100Base is established by parallel detection.	RO	0
5:6	10Base-T-FD	1: 10Base-T full duplex is supported by link partner 0: 10Base-T full duplex not supported by link partner	RO	0
5:5	10Base-T	1: 10Base-T is supported by link partner 0: 10Base-T not supported by link partner This bit will also be set if the link in 10Base-T is established by parallel detection.	RO	0
5:4~0	Selector Field	Link Partner's Binary Encoded Node Selector. Currently only CSMA/CD 00001 is specified.	RO	00001

7.7. Register 6 Auto-Negotiation Expansion Register (ANER)

This register contains additional status for NWay auto-negotiation.

Table 16. Register 6 Auto-Negotiation Expansion Register (ANER)

Address	Name	Description	Mode	Default
6:15~5	Reserved	Reserved.	-	-
6:4	Parallel Detection Fault	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	RO	0
6:3	Link Partner Next Page Ability	1: Link Partner is Next Page ability 0: Link Partner is not Next Page ability	RO	0
6:2	Local Next Page Ability	1: Next Page is ability 0: Next Page is not ability	RO	0
6:1	Page Received	1: A New Page has been received 0: A New Page has not been received	RO	0
6:0	Link Partner Auto-Negotiation Ability	If Auto-Negotiation is enabled, this bit means: 1: Link Partner is Auto-Negotiation ability 0: Link Partner is not Auto-Negotiation ability	RO	0

7.8. Register 23 Force Link and Bypass Scrambler Register

Table 17. Register 23 Force Link and Bypass Scrambler Register

Address	Name	Description	Mode	Default
23:15~9	Reserved	Reserved.	-	-
23:8	Sel_jumbo16K	Support 16K Jumbo Frame Selection.	RW	0
23:7~6	Reserved	Reserved.	-	-
23:5	Bp4B5B	Bypass 4B5B Function.	RW	0
23:4	Bpscr	Bypass Scrambler.	RW	0
23:3~0	Reserved	Reserved.	-	-

7.9. Register 24 Receiver Error Mask Register (REMR)

Table 18. Register 24 Receiver Error Mask Register (REMR)

Address	Name	Description	Mode	Default
24:15	Enpwrsave	Enable Power Saving Mode.	RW	1
24:14	Anaoff	Set to 1 to power down the analog function of transmitter and receiver.	RW	0
24:13	Encodeerr	Assertion of this bit causes a code error detection to be reported.	RW	0
24:12	Enpmeerr	Assertion of this bit causes a pre-mature end error detection to be reported.	RW	0
24:11	Enlinkerr	Assertion of this bit causes a link error detection to be reported.	RW	0
24:10~0	Reserved	Reserved.	-	-

7.10. Register 28 Fiber Mode and Loopback Register

Table 19. Register 28 Fiber Mode and Loopback Register

Address	Name	Description	Mode	Default
28:15~6	Reserved	Reserved.	-	-
28:5	Fxmode	Enable Fiber Mode.	RW	0
28:4~3	Reserved	Reserved.	-	-
28:2	En_autoMDIX	Enable Auto MDIX Function.	RW	1
28:1	Force_MDI	Force MDI/MDIX Mode. If Enable auto MDIX function disable, 1: Force MDI 0: Force MDIX	RW	1
28:0	Reserved	Reserved.	-	-

7.11. Register 30 SNR Display Register

Table 20. Register 30 SNR Display Register

Address	Name	Description	Mode	Default
30:15~4	Reserved	Reserved.	-	-
30:3~0	SNR_O	These 4-Bits Show the Signal to Noise Ratio Value.	RO	0000

7.12. Register 31 Page Select Register

Table 21. Register 31 Page Select Register

Address	Name	Description	Mode	Default
31:15~8	Reserved	Reserved for Internal Testing.	-	-
31:7~0	PAGE SEL	Select Page Address: 00000000~11111111.	RW	00000000

7.13. Page 4 Register 16 EEE Capability Enable Register

Table 22. Page4 Register 16 EEE Capability Enable Register

Address	Name	Description	Mode	Default
16:15~14	Reserved	Reserved.	-	-
16:13	EEE_10_cap	Enable EEE 10M capability	RW	0
16:12	EEE_nway_en	Enable next page exchange in NWay for EEE 100M	RW	0
16:11	EEE_en	Force EEE 100M	RW	0
16:10	EEE_force_en	Let EEE_en to decide EEE 100M	RW	0
16:9	Tx_quiet_en	Enable ability to turn off power100TX when TX in quiet state. This bit is recommended to set 1 when EEE support.	RW	0
16:8	Rx_quiet_en	Enable ability to turn off power100RX when RX in quiet state. This bit is recommended to set 1 when EEE support.	RW	0
16:7:0	Reserved	Reserved.	-	-

7.14. Page 4 Register 21 EEE Capability Register

Table 23. Page4 Register 21 EEE Capability Register

Address	Name	Description	Mode	Default
21:15~1	Reserved	Reserved.	-	-
21:0	EEE_100_cap	NWay result to indicate link partner both support EEE 100M.	RO	0

7.15. Page 7 Register 16 RMII Mode Setting Register (RMSR)

Table 24. Page7 Register 16 RMII Mode Setting Register (RMSR)

Address	Name	Description	Mode	Default
16:15~13	Reserved	Reserved.	-	-
16:12	Rg_rmii_clkdir	This Bit Sets the Type of TXC in RMII Mode. 0: Output 1: Input	RW/EFUS	1
16:11~8	Rg_rmii_tx_offset	Adjust RMII TX Interface Timing.	RW/EFUS	1111
16:7~4	Rg_rmii_rx_offset	Adjust RMII RX Interface Timing.	RW/EFUS	1111
16:3	RMII Mode	0: MII Mode 1: RMII Mode	RW/EFUS	0
16:2	Rg_rmii_rxdv_sel	0: CRS/CRS_DV pin is CRS_DV signal 1: CRS/CRS_DV pin is RXDV signal	RW/EFUS	0
16:1	Rg_rmii_rxdsel	0: RMII data only 1: RMII data with SSD Error	RW/EFUS	1
16:0	Reserved	Reserved.	-	-

7.16. Page 7 Register 17 Customized LEDs Setting Register

This register is for setting customized LEDs. The Table 25 shows the customized LED matrix table.

Table 25. Customized LED Matrix Table

	LINK			ACT
	10M	100M	1000M	
LED0	Bit0	Bit1	Bit2	Bit3
LED1	Bit4	Bit5	Bit6	Bit7
LED2	Bit8	Bit9	Bit10	Bit11

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Selected Speed LINK+ACT

Note1: 1000M speed LINK and ACT are not used for the RTL8201F/FN/FL.
Note2: The RTL8201F/FL only supports LED0 and LED1. The RTL8201FN supports LED0, LED1, and LED2.

Table 26. Page7 Register 17 Customized LEDs Setting Register

Address	Name	Description	Mode	Default
17:15~12	Reserved	Reserved.	-	-
17:11~8	LED_sel2	Customized LED2 Setting. Set Bit3 (Page7 Register 19; Table 28, page 22) to 1 to enable customized LED function.	RW	0000
17:7~4	LED_sel1	Customized LED1 Setting. Set Bit3 (Page7 Register 19; Table 28, page 22) to 1 to enable customized LED function.	RW	0000
17:3~0	LED_sel0	Customized LED0 Setting. Set Bit3 (Page7 Register 19; Table 28, page 22) to 1 to enable customized LED function.	RW	0000

7.17. Page 7 Register 18 EEE LEDs Enable Register

Table 27. Page7 Register 18 EEE LEDs Enable Register

Address	Name	Description	Mode	Default
18:15~3	Reserved	Reserved.	-	-
18:2	EEE_LED_en2	Enable LED2 in EEE/LPI Mode.	RW	0
18:1	EEE_LED_en1	Enable LED1 in EEE/LPI Mode.	RW	0
18:0	EEE_LED_en0	Enable LED0 in EEE/LPI Mode.	RW	0

7.18. Page 7 Register 19 Package Indicator, LEDs Function Register

Table 28. Page7 Register 19 Package Indicator and LEDs Function Register

<table>
<tr><th>Address</th><th>Name</th><th>Description</th><th>Mode</th><th>Default</th></tr>
<tr><td>19:15~14</td><td>Rg_pkg</td><td>00: Package is RTL8201FL
01: Package is RTL8201FN
11: Package is RTL8201F</td><td>RW/LI</td><td>00</td></tr>
<tr><td>19:13~6</td><td>Reserved</td><td>Reserved.</td><td>-</td><td>-</td></tr>
<tr><td>19:5~4</td><td>LED_sel[1:0]</td><td>Traditional LED Function Selection.
<table>
<tr><td>LED_sel</td><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td>LED0</td><td>ACT_{ALL}</td><td>$Link_{ALL}$/ ACT_{ALL}</td><td>Link10/ ACT_{ALL}</td><td>LINK10 /ACT_{10}</td></tr>
<tr><td>LED1</td><td>LINK100</td><td>LINK100</td><td>LINK100</td><td>LINK100/ ACT_{100}</td></tr>
<tr><td>LED2</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
</table></td><td>RW</td><td>11</td></tr>
<tr><td>19:3</td><td>Customized_LED</td><td>Customized LED Enable.
1: Customized LED function enable
0: Customized LED function disable
See the section 8.5.6 Customized LED, page 29 for detail.</td><td>RW</td><td>0</td></tr>
<tr><td>19:2~1</td><td>Reserved</td><td>Reserved.</td><td>-</td><td>-</td></tr>
<tr><td>19:0</td><td>En10mlpi</td><td>Enable 10M LPI LED Function.</td><td>RW</td><td>0</td></tr>
</table>

7.19. Page 7 Register 20 MII TX Isolate Register

Table 29. Page7 Register 20 MII TX Isolate Register

Address	Name	Description	Mode	Default
20:15	Rg_tx_isolate_en	Isolate MII TX Path Signals when TX Idle.	RW	0
20:14~0	Reserved	Reserved.	-	-

8. Functional Description

The RTL8201F/FN/FL PHYceiver is a physical layer device that integrates 10Base-T and 100Base-TX/100Base-FX functions, and some extra power management features. This device supports the following functions:

- MII interface with MDC/MDIO management interface to communicate with the MAC
- IEEE 802.3u clause 28 Auto-Negotiation ability
- Supports Flow control ability indication in cooperation with MAC
- Speed, duplex, auto-negotiation ability configurable by hard wire or MDC/MDIO
- Power Down mode support
- 4B/5B transform
- Scrambling/De-scrambling
- NRZ to NRZI, NRZI to MLT-3
- Manchester Encode and Decode for 10Base-T operation
- Clock and Data recovery
- Adaptive Equalization
- Automatic Polarity Correction
- Far End Fault Indication (FEFI) in fiber mode
- Network status LEDs
- Wake-On-LAN (WOL) (RTL8201FN only)
- Energy Efficient Ethernet (EEE)

8.1. MII and Management Interface

8.1.1. Data Transition

To set the RTL8201F/FN/FL for MII mode operation, pull the COL pin low.

The MII (Media Independent Interface) is an 18-signal interface (as described in IEEE 802.3u) supplying a standard interface between the PHY and MAC layer.

This interface operates at two frequencies, 25MHz and 2.5MHz, to support 100Mbps/10Mbps bandwidth for both transmit and receive functions.

Transmission

The MAC asserts the TXEN signal. It then changes byte data into 4-bit nibbles and passes them to the PHY via TXD[3:0]. The PHY will sample TXD[3:0] synchronously with TXC – the transmit clock signal supplied by the PHY – during the interval TXEN is asserted.

Reception

The PHY asserts the RXEN signal. It passes the received nibble data RXD[3:0] clocked by RXC. CRS and COL signals are used for collision detection and handling.

In 100Base-TX mode, when the decoded signal in 5B is not IDLE, the CRS signal will assert. When 5B is recognized as IDLE it will be de-asserted. In 10Base-T mode, CRS will assert when the 10M preamble has been confirmed and will be de-asserted when the IDLE pattern has been confirmed.

The RXDV signal will be asserted when decoded 5B are /J/K/ and will be de-asserted if the 5B are /T/R/ or IDLE in 100Mbps mode. In 10Mbps mode, the RXDV signal is the same as the CRS signal.

The RXER (Receive Error) signal will be asserted if any 5B decode errors occur, e.g., an invalid J/K, invalid T/R, or invalid symbol. This pin will go high for one or more clock periods to indicate to the reconciliation sublayer that an error was detected somewhere in the frame.

8.1.2. Serial Management Interface

The MAC layer device can use the MDC/MDIO management interface to control a maximum of 4 (RTL8201F/FL) or 8 (RTL8201FN) devices, configured with different PHY addresses (00b to 11b for the RTL8201F/FL; 000b to 111b for the RTL8201FN).

During a hardware reset, the logic levels of pins 34/24, 35/25, and 32/22 (only RTL8201FN) are latched to be set as the PHY address for management communication via the serial interface. The read and write frame structure for the management interface is illustrated in Figure 5 and Figure 6.

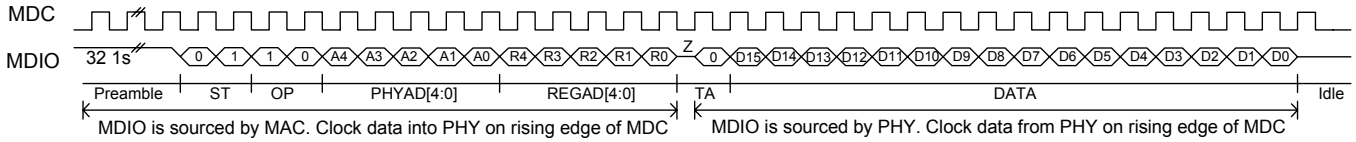


Figure 5. Read Cycle

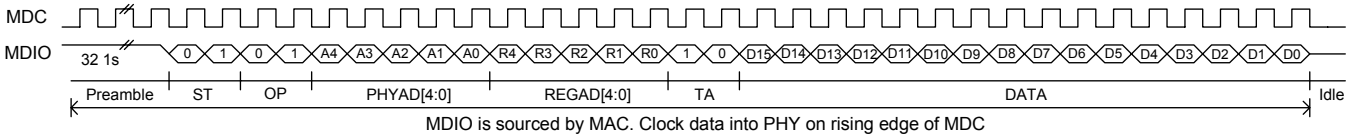


Figure 6. Write Cycle

Table 30. Serial Management

Name	Description
Preamble	32 Contiguous Logical 1's Sent by the MAC on MDIO, along with 32 Corresponding Cycles on MDC. This provides synchronization for the PHY.
ST	Start of Frame. Indicated by a 01 pattern.
OP	Operation Code. Read: 10 Write: 01
PHYAD	PHY Address. Up to 4 PHYs can be connected to one MAC. This 2-bit field selects which PHY the frame is directed to.
REGAD	Register Address. This is a 5-bit field that sets which of the 32 registers of the PHY this operation refers to.
TA	Turnaround. This is a 2-bit-time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY remain in a high-impedance state for the first bit time of the turnaround. The PHY drives a zero bit during the second bit time of the turnaround of a read transaction.
DATA	Data. These are the 16 bits of data.
IDLE	Idle Condition. Not truly part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logical '1'.

8.2. Interrupt (RTL8201FN/FL Only)

Whenever there is a status change on the media detected by the RTL8201FN/FL, they will drive the interrupt pin (INTB) low to issue an interrupt event. The MAC senses the status change and accesses the registers (P1:R16) through the MDC/MDIO interface in response.

Once these status registers (P1:R16) have been read by the MAC through the MDC/MDIO, the INTB is de-asserted. The RTL8201FN/FL interrupt function removes the need for continuous polling through the MDC/MDIO management interface.

8.3. Auto-Negotiation and Parallel Detection

The RTL8201F/FN/FL supports IEEE 802.3u clause 28 Auto-negotiation for operation with other transceivers supporting auto-negotiation. The RTL8201F/FN/FL can auto-detect the link partner's abilities and determine the highest speed/duplex configuration possible between the two devices. If the link partner does not support auto-negotiation, then the RTL8201F/FN/FL will enable half-duplex mode and enter parallel detection mode. The RTL8201F/FN/FL will default to transmitting FLP (Fast Link Pulse) and wait for the link partner to respond. If the RTL8201F/FN/FL receives a FLP, then the auto-negotiation process will continue. If it receives an NLP (Normal Link Pulse), then the RTL8201F/FN/FL will change to 10Mbps and half-duplex mode. If it receives a 100Mbps IDLE pattern, it will change to 100Mbps and half-duplex mode.

8.3.1. Setting the Medium Type and Interface Mode to MAC

Table 31. Setting the Medium Type and Interface Mode to MAC

FXEN	RXDV	Operation Mode
H	L	Fiber Mode and MII Mode
H	H	Fiber Mode and RMII Mode
H	X	Fiber Mode and MII Mode
L	L	UTP Mode and MII Mode
L	H	UTP Mode and RMII Mode
L	X	UTP Mode and MII Mode

8.4. Flow Control Support

The RTL8201F/FN/FL supports flow control indications. The MAC can program the MII register to indicate to the PHY that flow control is supported. When the MAC supports the Flow Control mechanism, the OS sets bit 10 of the ANAR register via the MAC using the MDC/MDIO interface; then the RTL8201F/FN/FL will add the ability to its NWay ability. If the Link partner also supports Flow Control, the RTL8201F/FN/FL can recognize the Link partner's NWay ability by examining bit 10 of the ANLPAR (register 5).

8.5. LED Functions

The RTL8201FN support three LED signals, and the RTL8201F and RTL8201FL supports two LED signals, in four configurable operation modes. The following sections describe the various LED actions.

8.5.1. Link Monitor

The Link Monitor senses link integrity, such as LINK10, LINK100, LINK10/ACT, or LINK100/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists.

8.5.2. RX LED

In 10/100Mbps mode, blinking of the RX LED indicates that receive activity is occurring.

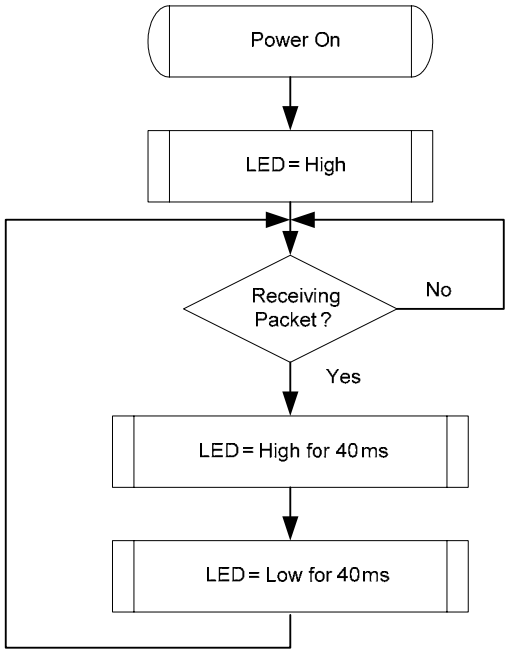


Figure 7. RX LED

8.5.3. TX LED

In 10/100Mbps mode, blinking of the TX LED indicates that transmit activity is occurring.

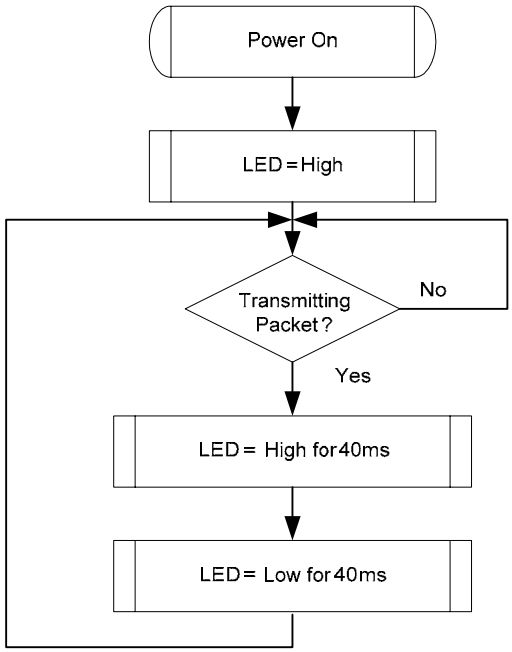


Figure 8. TX LED

8.5.4. TX/RX LED

In 10/100Mbps mode, blinking of the TX/RX LED indicates that both transmit and receive activity is occurring.

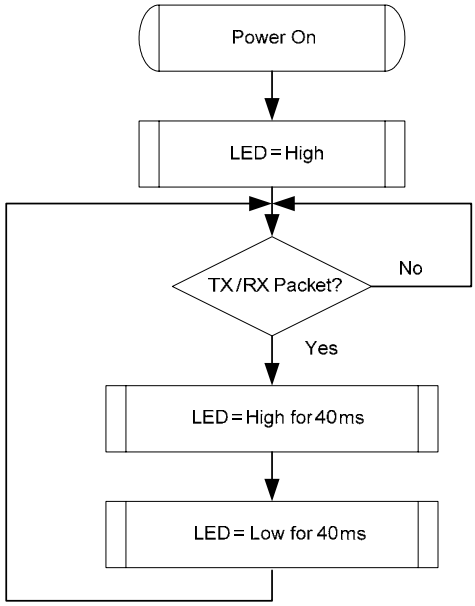


Figure 9. TX/RX LED

8.5.5. LINK/ACT LED

In 10/100Mbps mode, blinking of the LINK/ACT LED indicates that the RTL8201F/FN/FL is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.

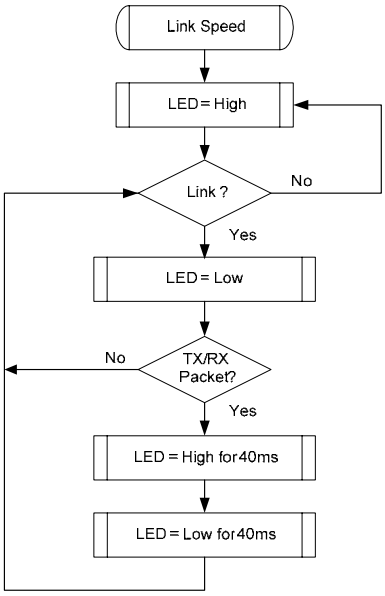


Figure 10. LINK/ACT LED

8.5.6. Customized LED

The RTL8201F/FN/FL supports programmable LEDs in 10/100Mbps mode. This function can be enabled/disabled via page7, reg19[3] register (Figure 11).

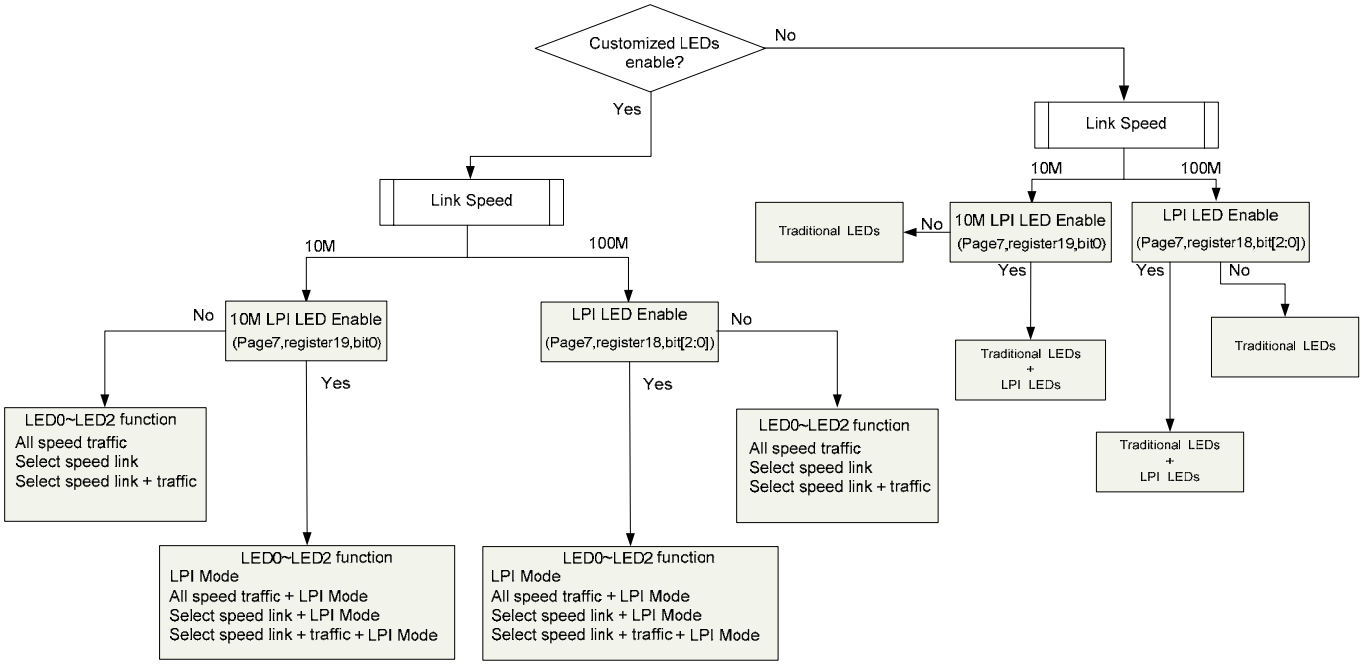


Figure 11. Customized LED with/without LPI LED Mode

8.6. Power Down, Link Down, and Power Saving Modes

Three types of Power Saving mode operation are supported. This section describes how to implement each mode through software.

Table 32. Power Saving Mode Pin Settings

Mode	Description
Analog Off	Setting bit 14 of register 24 to 1 will put the RTL8201F/FN/FL into analog off state. In analog off state, the RTL8201F/FN/FL will power down all analog functions such as transmit, receive, PLL, etc. However, the internal 25MHz crystal oscillator will not be powered down. Digital functions in this mode are still available to allow reacquisition of analog functions
LDPS	Setting bit 15 of register 24 to 1 will put the RTL8201F/FN/FL into LDPS (Link Down Power Saving) mode. In LDPS mode, the RTL8201F/FN/FL will detect the link status to decide whether or not to turn off the transmit function. If the link is off, FLP or 100Mbps IDLE/10Mbps NLP will not be transmitted. However, some signals similar to NLP will be transmitted. Once the receiver detects leveled signals, it will stop the signal and transmit FLP or 100Mbps IDLE/10Mbps NLP again. This can cut power used by 60%~80% when the link is down.
PWD	Setting bit 11 of register 0 to 1 puts the RTL8201F/FN/FL into Power Down Mode (PWD). This is the maximum power saving mode while the RTL8201F/FN/FL is still 'live'. In PWD mode, the RTL8201F/FN/FL will turn off all analog/digital functions except the MDC/MDIO management interface. Therefore, if the RTL8201F/FN/FL is put into PWD mode and the MAC wants to recall the PHY, it must create the MDC/MDIO timing by itself (this is done by software).

8.7. Media Interface

8.7.1. 100Base-TX Transmit and Receive Operation

100Base-TX Transmit

Transmit data in 4-bit nibbles (TXD[3:0]) clocked at 25MHz (TXC) is transformed into 5B symbol code (4B/5B encoding). Scrambling, serializing, and conversion to 125MHz, and NRZ to NRZI then takes place. After this process, the NRZI signal is passed to the MLT-3 encoder, then to the transmit line driver. The transmitter will first assert TXEN. Before transmitting the data pattern, it will send a /J/K/ symbol (Start-of-frame delimiter), the data symbol, and finally a /T/R/ symbol known as the End-Of-Frame delimiter. For better EMI performance, the seed of the scrambler is based on the PHY address. In a hub/switch environment, each RTL8201F/FN/FL will have different scrambler seeds and so spread the output of the MLT-3 signals.

100Base-TX Receive

The received signal is compensated by the adaptive equalizer to make up for signal loss due to cable attenuation and Inter Symbol Interference (ISI). Baseline Wander Correction monitors the process and dynamically applies corrections to the process of signal equalization. The Phase Locked Loop (PLL) then recovers the timing information from the signals and from the receive clock. With this, the received signal is sampled to form NRZI (Non-Return-to-Zero Inverted) data. The next steps are the NRZI to NRZ (Non-Return-to-Zero) process, unscrambling of the data, serial to parallel and 5B to 4B conversion, and passing of the 4B nibble to the MII interface.

8.7.2. 100Base-FX Fiber Transmit and Receive Operation

The RTL8201F/FN/FL can be configured to 100Base-FX mode via hardware configuration. The hardware 100Base-FX setting takes priority over NWay settings. A scrambler is not required in 100Base-FX.

100Base-FX Transmit

Di-bits of TXD are processed as 100Base-TX except without a scrambler before the NRZI stage. Instead of converting to MLT-3 signals, as in 100Base-TX, the serial data stream is driven out as NRZI PECL signals, which enter the fiber transceiver in differential-pair form.

100Base-FX Receive

The signal is received through PECL receiver inputs from the fiber transceiver and directly passed to the clock recovery circuit for data/clock recovery. The scrambler/de-scrambler is bypassed in 100Base-FX.

8.7.3. 10Base-T Transmit and Receive Operation

10Base-T Transmit

Transmit data in 4-bit nibbles (TXD[3:0]) clocked at 2.5MHz (TXC) is first fed to a parallel-to-serial converter, then the 10Mbps NRZ signal is sent to a Manchester encoder. The Manchester encoder converts the 10Mbps NRZ data into a Manchester Encoded data stream for the TP transmitter and adds a Start of Idle pulse (SOI) at the end of the packet as specified in IEEE 802.3. Finally, the encoded data stream is shaped by a band-limited filter embedded in the RTL8201F/FN/FL and then transmitted.

10Base-T Receive

In 10Base-T receive mode, the Manchester decoder in the RTL8201F/FN/FL converts the Manchester encoded data stream into NRZ data by decoding the data and stripping off the SOI pulse. Then the serial NRZ data stream is converted to a parallel 4-bit nibble signal (RXD[0:3]).

8.8. Reset and Transmit Bias

The RTL8201F/FN/FL can be reset by pulling the PHYRSTB pin low for about 10ms, then pulling the pin high. It can also be reset by setting bit 15 of register 0 to 1, and then setting it back to 0. Reset will clear the registers and re-initialize them. The media interface will disconnect and restart the auto-negotiation/parallel detection process.

The RSET pin must be pulled low by a 2.49KΩ resistor with 1% accuracy to establish an accurate transmit bias. This will affect the signal quality of the transmit waveform. Keep its circuitry away from other clock traces and transmit/receive paths to avoid signal interference.

8.9. 3.3V Power Supply and Voltage Conversion Circuit

The RTL8201F/FN/FL is fabricated in a 0.11µm process. The core circuit needs to be powered by 1.05V, however, the digital IO and DAC circuits need a 3.3V power supply. Regulators are embedded in the RTL8201F/FN/FL to convert 3.3V to 1.05V.

Note: An external 1.05V power supply is not suggested for the RTL8201F/FL, as the internal regulators cannot be disabled (the RTL8201F/FL does not have an EN_LDO_OUT pin to disable the internal 1.05V power supply), and the two 1.05V power sources may conflict.

As with many commercial voltage conversion devices, the 1.05V output pin of this circuit requires the use of an output capacitor (0.1µF X5R low-ESR ceramic capacitor is recommended) as part of the device frequency compensation.

The analog and digital ground planes should be as large and intact as possible. If the ground plane is large enough, the analog and digital grounds can be separated, which is the ideal configuration. However, if the total ground plane is not sufficiently large, partition of the ground plane is not a good idea. In this case, all the ground pins can be connected together to a larger single and intact ground plane.

Note: The embedded 1.05V LDO is designed for PHYceiver device internal use only. Do not provide this power to other devices.

8.10. Automatic Polarity Correction

The RTL8201F/FN/FL automatically corrects polarity errors on the receive pairs in 10Base-T mode (polarity is irrelevant in 100Base-TX mode). In 10Base-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. Detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link goes down.

8.11. Far End Fault Indication

The MII Reg.1.4 (Remote Fault) is the Far End Fault Indication (FEFI) bit when 100FX mode is enabled, and indicates when a FEFI has been detected. FEFI is an alternative in-band signaling method that is composed of 84 consecutive ‘1’s followed by one ‘0’. When the RTL8201F/FN/FL detects this pattern three times, Reg.1.4 is set, which means the transmit path (the Remote side’s receive path) has a problem. On the other hand, if an incoming signal fails to cause a ‘Link OK’, the RTL8201F/FN/FL will start sending this pattern, which in turn causes the remote side to detect a Far End Fault. This means that the receive path has a problem from the point of view of the RTL8201F/FN/FL. The FEFI mechanism is used only in 100Base-FX mode.

8.12. Wake-On-LAN (WOL) (RTL8201FN Only)

8.12.1. Magic Packet and Wake up Frame Format

The RTL8201FN can monitor the network for a Wakeup Frame or a Magic Packet, and notify the system via the PMEB (Power Management Event; 'B' means low active) pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs. The PMEB pin must be connected with a 4.7k-ohm resistor and pulled up to 3.3V or 5V. When the Wakeup Frame or a Magic Packet is sent to the PHY, the PMEB pin will be set low to notify the system to wake up. Refer to the WOL application note for details.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8201FN, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8201FN.
- The received Magic Packet does not contain a CRC error.
- The Magic Packet pattern matches; i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8201FN, e.g., a broadcast, multicast, or unicast address to the current RTL8201FN.
- The received Wakeup Frame does not contain a CRC error.
- The 16-bit CRC of the received Wakeup Frame matches the 16-bit CRC of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8201FN is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet.

8.12.2. Active Low Wake-On-LAN

When the PHY receives a Wakeup Frame or a Magic Packet from the link partner, the PMEB pin will go low and the MAC will wake up after a T cycle. The PMEB pin will be reset to high via the system or MAC (Figure 12 and Figure 13).

Refer to the RTL8201FN_WOL_Application_Note for details.

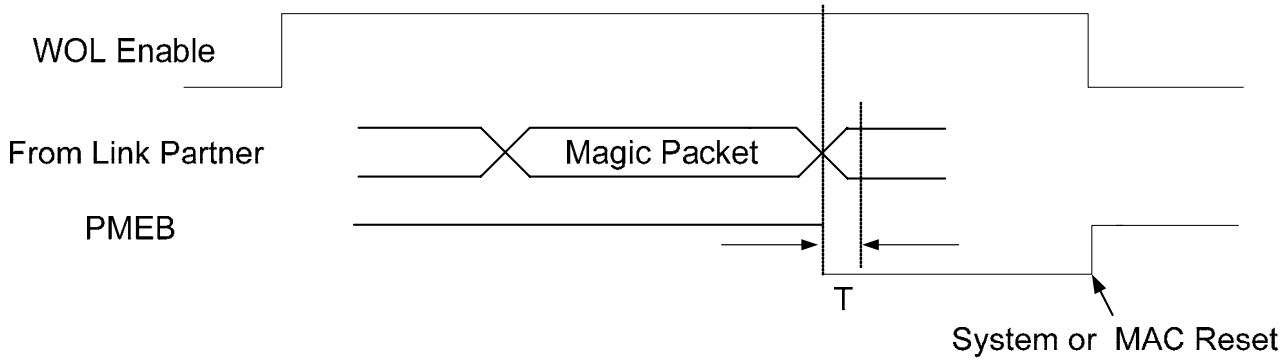


Figure 12. Active Low When Receiving a Magic Packet

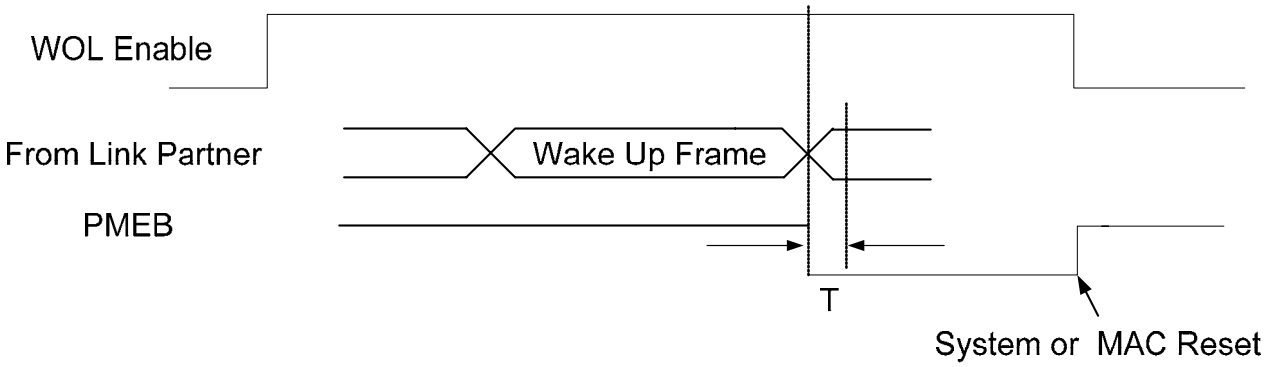


Figure 13. Active Low When Receiving a Wakeup Frame

8.12.3. Pulse Low Wake-On-LAN

When the PHY receives a Wakeup Frame or a Magic Packet from the link partner, the PMEB pin will go low for a period (84ms, 168ms (default), 336ms, or 672ms; set through the MDC/MDIO), and will wake up after a T cycle (Figure 14 and Figure 15).

Refer to the RTL8201FN_WOL_Application_Note for details.

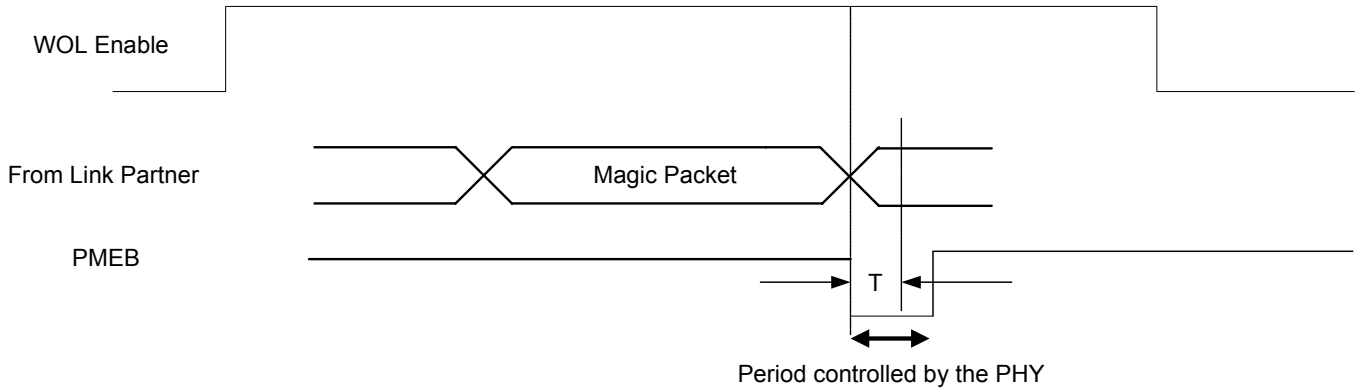


Figure 14. Pulse Low When Receiving a Magic Packet

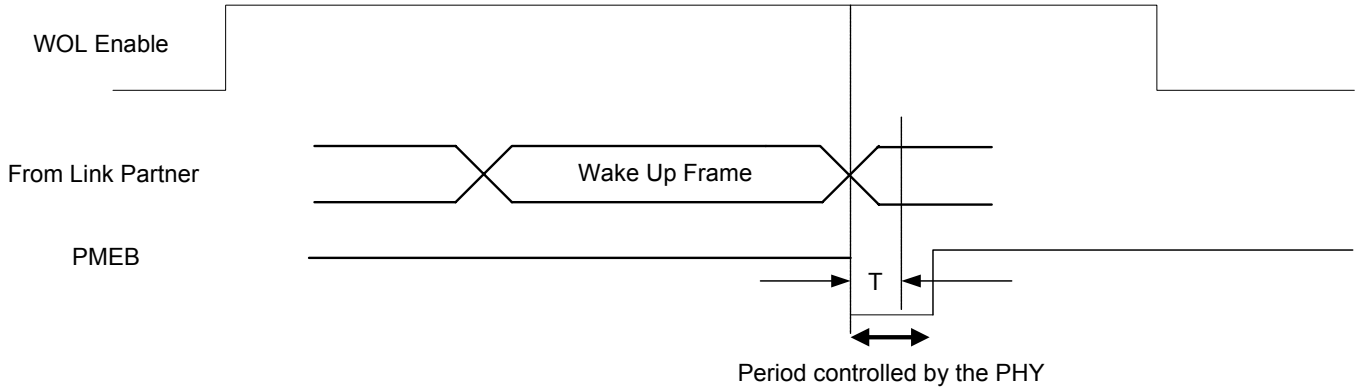


Figure 15. Pulse Low When Receiving a Wakeup Frame

8.12.4. Wake-On-LAN Pin Types (Only RTL8201FN in MII Mode)

Table 33. Wake-On-LAN Pin Types (Only RTL8201FN in MII Mode)

Name	Type	Normal			WOL Enable
		100M	10M	Idle	
TXC	O/PD	25M CLK Output	2.5M CLK Output	2.5M CLK Output	O (2.5M/25M)/L/PD[1]
TXEN	I/PD	I	I	I	I/PD
TXD[0:3]	I/PD	I	I	I	I/PD
RXC	O/PD	25M CLK Output	2.5M CLK Output	2.5M CLK Output	O (2.5M/25M)/PD[2]
COL	LI/O/PD	O	O	O	O or PD[2]
CRS	LI/O/PD	O	O	O	O or PD[2]
RXDV	LI/O/PD	O	O	O	O or PD[2]
RXD[0:3]	O/PD	O	O	O	O or PD[2]
RXER	LI/O/PD	O	O	O	O or PD[2]
MDC	I/PU	I	I	I	I/PU
MDIO	IO/PU	IO	IO	IO	IO/PU

Note1: If TX Isolate=1, the TXC is halted and the pin type is 'L'.
Set page0, register0, and bit10=0 to change the TXC pin type to 'PD'.
Note2: If RX Isolate=1, all the MII RX interfaces are halted and the pin types are 'PD'.

8.12.5. Wake-On-LAN Pin Types (Only RTL8201FN in RMII Mode)

Table 34. Wake-On-LAN Pin Types (Only RTL8201FN in RMII Mode)

Name	Type	Normal			WOL Enable
		100M	10M	Idle	
TXC (REF_CLK)[1]	IO/PD	50M CLK Input/Output	50M CLK Input/Output	50M CLK Input/Output	I/O (50M)[2]
TXEN	I/PD	I	I	I	I/PD
TXD[0:1]	I/PD	I	I	I	I/PD
CRS_DV	LI/O/PD	O	O	O	O or PD[3]
RXD[0:1]	O/PD	O	O	O	O or PD[3]
RXER	LI/O/PD	O	O	O	O or PD[3]
MDC	I/PU	I	I	I	I/PU
MDIO	IO/PU	IO	IO	IO	IO/PU

Note1: If TXC (REF_CLK) is in input mode (MAC to PHY), the REF_CLK cannot stop at WOL Enable.
Note2: When REF_CLK is in output mode (PHY to MAC), the REF_CLK cannot halt (always toggles 50MHz out). To set the TXC pin type to 'PD', set page0, register0, bit10=0.
Note3: If RX Isolate=1, all RMII RX interfaces are halted and the pin types are 'PD'.

8.13. Energy Efficient Ethernet (EEE)

The RTL8201F/FN/FL supports IEEE 802.3az Draft 3.2, also known as Energy Efficient Ethernet (EEE), at 10Mbps and 100Mbps. This standard is being developed by the IEEE 802.3az Task Force, and should be finalized by September 2010. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. When packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled; however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

Refer to http://ieee802.org/3/interims/index.html for more details.

Refer to the ‘Ethernet Transceiver (R)MII (R)GMII-EEE App Notes’ for EEE MII/RMII power saving mode register settings.

9. Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 35. Absolute Maximum Ratings

Item	Minimum	Maximum
Supply Voltage	-0.4V	3.7V
Storage Temperature	-55°C	125°C

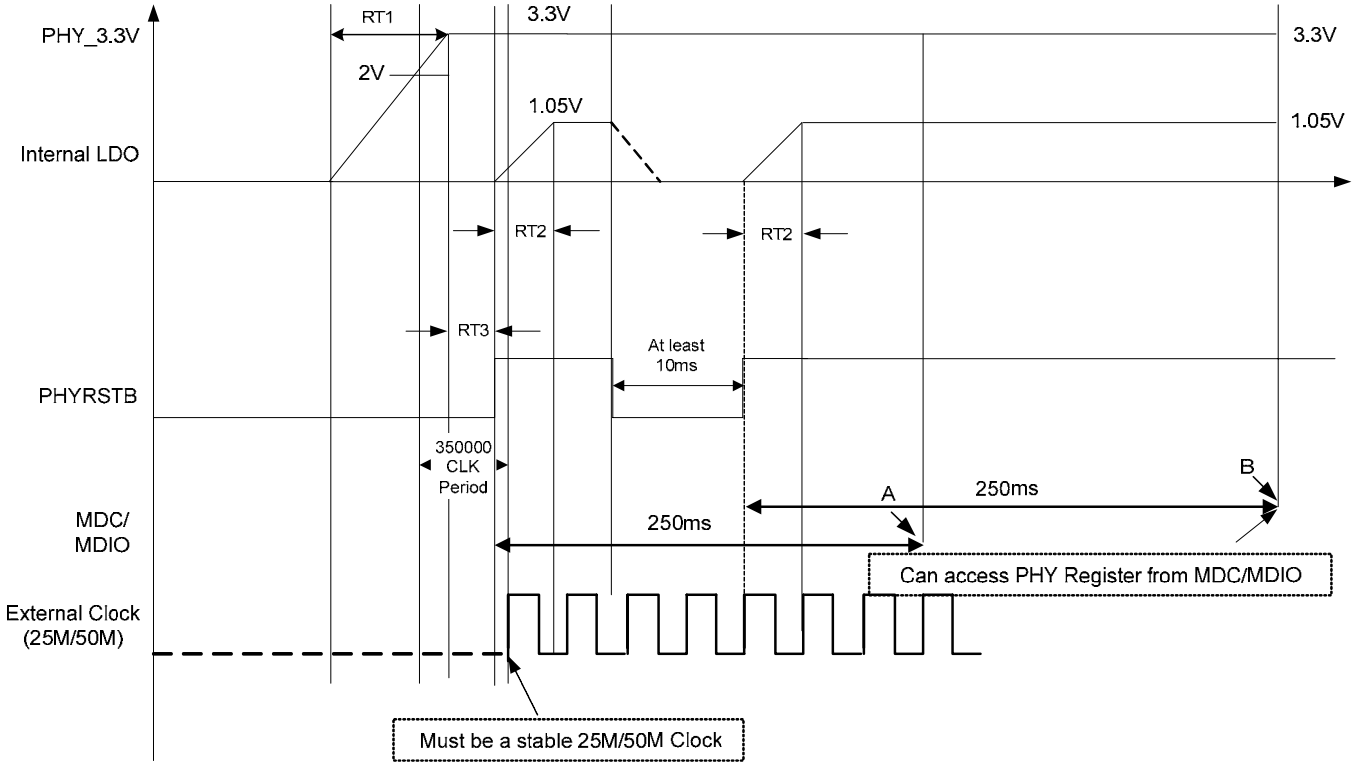
9.1.2. Operating Conditions

Table 36. Operating Conditions

Item	Condition	Minimum	Typical	Maximum
Vcc 3.3V	3.3V Supply Voltage	2.97V	3.3V	3.63V
T_A	Ambient Operating Temperature	0°C	-	70°C

9.1.3. Power On and PHY Reset Sequence

The RTL8201F/FN/FL needs 250ms power on time. After 250ms it can access the PHY register from MDC/MDIO.



Note1: If there is no PHY Reset sequence, the MAC can access the PHY Register at point A.
Note2: If there is a PHY Reset sequence, the MAC can access the PHY Register at point B.

Figure 16. Power On and PHY Reset Sequence

Table 37. Power On and PHY Reset Sequence

Symbol	Description	Minimum	Maximum
Rt1	3.3V Rise Time@ Power On Sequence	100µs	-
Rt2*	1.05V Rise Time@ Power On and PHY Reset Sequence	100µs	-
Rt3	PHYRSTB De-Assert after PHY_3.3V Stable	80µs	-

Note: Rt2 requires 100µs Rise Time only when using an external 1.05V power supply.

9.1.4. Power Dissipation

The whole system power dissipation (including regulator loss) is shown in Table 38.

Table 38. Power Dissipation (Whole System)

Symbol	Condition	RTL8201F	RTL8201FN	RTL8201FL	Unit
P_{10IDLE}	10Base-T Idle (EEE not Enabled)	TBD	29	TBD	mW
P_{10EEE}	10Base-T Full Duplex with EEE	TBD	78.5	TBD	mW
P_{10F}	10Base-T Full Duplex (EEE not Supported)	TBD	115	TBD	mW
$P_{100IDLE}$	100Base-T Idle (EEE not Enabled)	TBD	122.5	TBD	mW
P_{100EEE}	100Base-T Idle with EEE	TBD	66.5	TBD	mW
P_{100F}	100Base-T Full Duplex (EEE not supported)	TBD	132.5	TBD	mW
P_{LDPS}	Link Down Power Saving	TBD	12.5	TBD	mW
P_{PHYRST}	PHY Reset	TBD	3.3	TBD	mW

9.1.5. Input Voltage: Vcc

Table 39. Input Voltage: Vcc

Symbol	Condition		Minimum	Maximum
TTL V_{IH}	Input High Voltage	-	0.5*Vcc	Vcc +0.5V
TTL V_{IL}	Input Low Voltage	-	-0.5V	0.7V
TTL V_{OH}	Output High Voltage	IOH=-8mA	0.65*Vcc	Vcc
TTL V_{OL}	Output Low Voltage	IOL=8mA	-	0.7V
TTL I_{OZ}	Tri-State Leakage	Vout=Vcc or GND	-110µA	10µA
I_{IN}	Input Current	Vin=Vcc or GND	-1µA	10µA
I_{PL}	Input Current with Internal Weakly Pulled Low Resistor	Vin=Vcc or GND	-1µA	100µA
I_{PH}	Input Current with Internal Weakly Pulled High Resistor	Vin=Vcc or GND	-110µA	10µA
PECL V_{IH}	PECL Input High Voltage	-	Vdd -1.16V	Vdd -0.88V
PECL V_{IL}	PECL Input Low Voltage	-	Vdd -1.81V	Vdd -1.47V
PECL V_{OH}	PECL Output High Voltage	-	Vdd -1.02V	-
PECL V_{OL}	PECL Output Low Voltage	-	-	Vdd -1.62V

9.2. AC Characteristics

All output timing assumes equivalent loading between 10pF and 25pF that includes PCB layout traces and other connected devices (e.g., MAC).

9.2.1. MII Transmission Cycle Timing

Table 40. MII Transmission Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1	TXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_2	TXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_3	TXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t_4	TXEN, TXD[0:3] Setup to TXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	5	-	-	ns
t_5	TXEN, TXD[0:3] Hold After TXCLK Rising Edge	100Mbps	0	-	-	ns
		10Mbps	0	-	-	ns
t_6	TXEN Sampled to CRS High	100Mbps	-	-	40	ns
		10Mbps	-	-	400	ns
t_7	TXEN Sampled to CRS Low	100Mbps	-	-	160	ns
		10Mbps	-	-	2000	ns
t_8	Transmit Latency	100Mbps	60	70	140	ns
		10Mbps	-	-	2000	ns
t_9	Sampled TXEN Inactive to End of Frame	100Mbps	-	100	170	ns
		10Mbps	-	-	-	ns

Figure 17 and Figure 18 and show an example of a packet transfer from MAC to PHY on the MII interface.

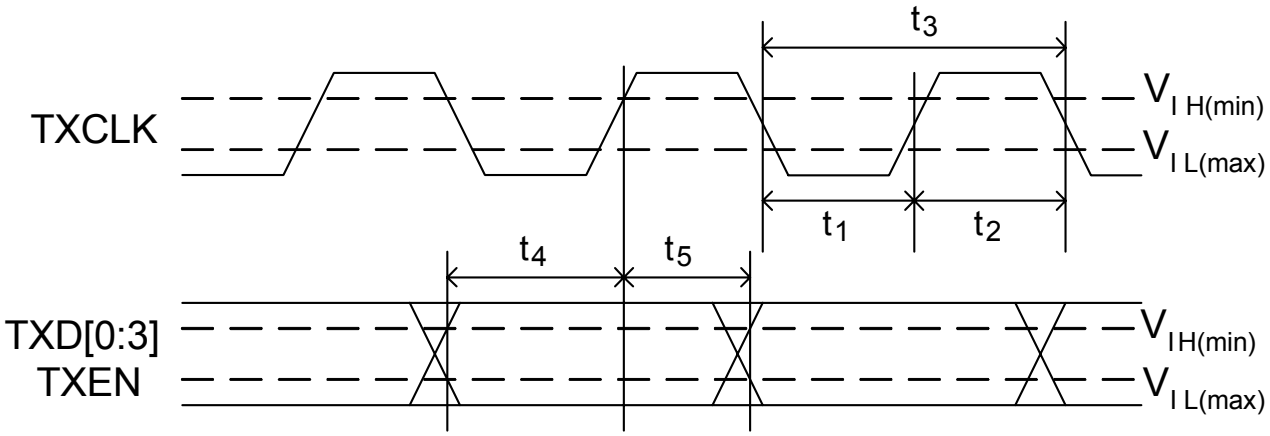


Figure 17. MII Transmission Cycle Timing-1

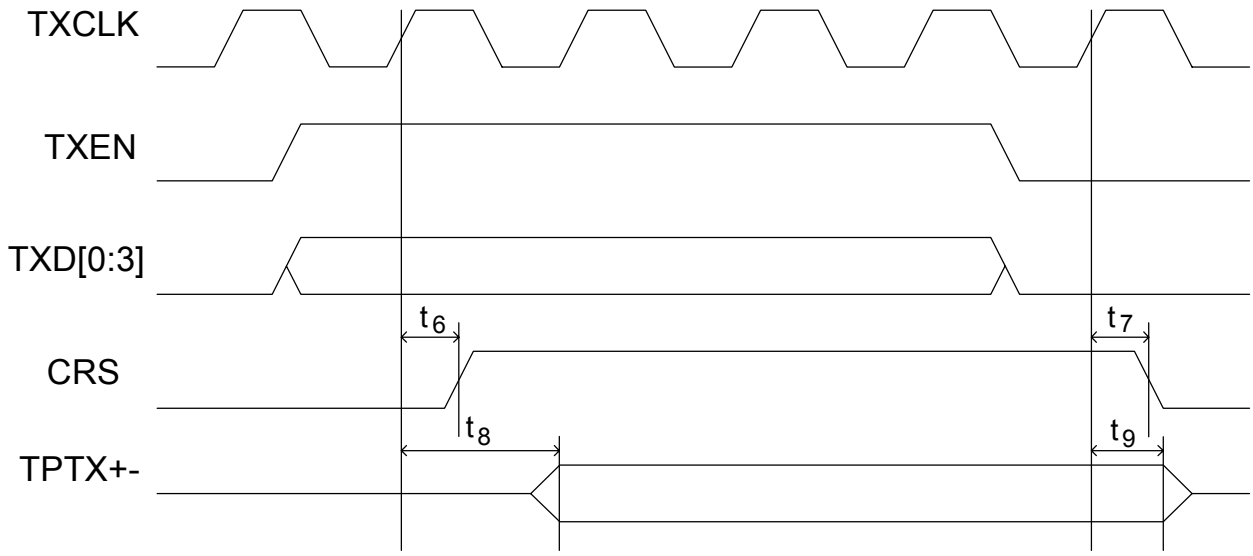


Figure 18. MII Transmission Cycle Timing-2

9.2.2. MII Reception Cycle Timing

Table 41. MII Reception Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1	RXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_2	RXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_3	RXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t_4	RXER, RXDV, RXD[0:3] Setup to RXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t_5	RXER, RXDV, RXD[0:3] Hold After RXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t_6	Receive Frame to CRS High	100Mbps	-	-	130	ns
		10Mbps	-	-	2000	ns
t_7	End of Receive Frame to CRS Low	100Mbps	-	-	240	ns
		10Mbps	-	-	1000	ns
t_8	Receive Frame to Sampled Edge of RXDV	100Mbps	-	-	150	ns
		10Mbps	-	-	3200	ns
t_9	End of Receive Frame to Sampled Edge of RXDV	100Mbps	-	-	120	ns
		10Mbps	-	-	1000	ns

Figure 19 and Figure 20 show an example of a packet transfer from PHY to MAC on the MII interface.

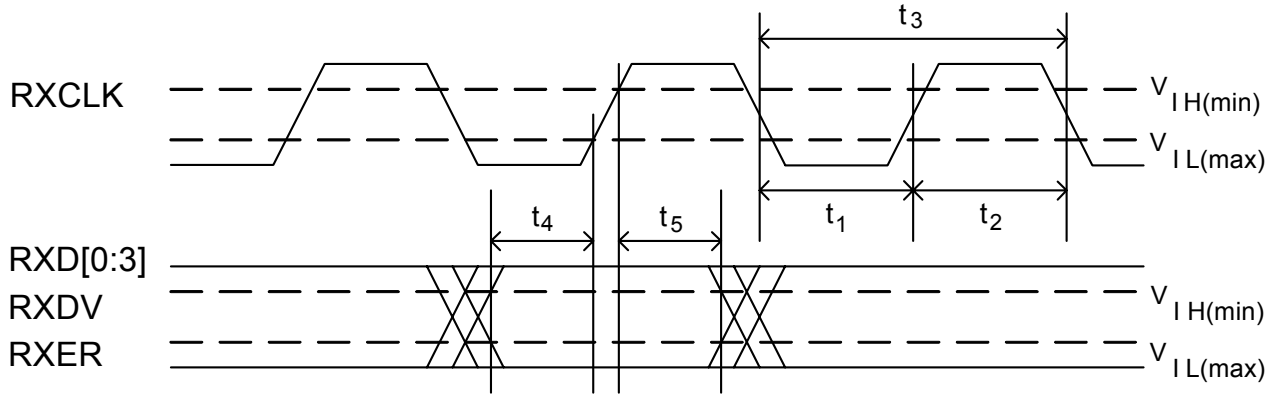


Figure 19. MII Reception Cycle Timing-1

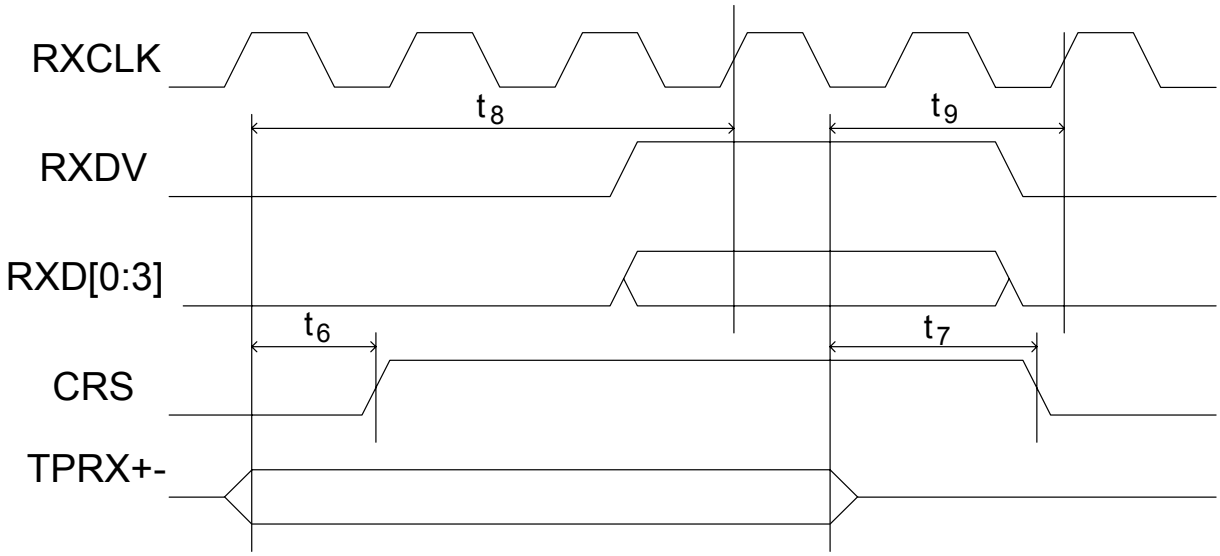


Figure 20. MII Reception Cycle Timing-2

9.2.3. RMII Transmission and Reception Cycle Timing

Table 42. RMII Transmission and Reception Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	-	50	-	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	-	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN Setup Time to REFCLK	4	-	-	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN Hold Time from REFCLK	2	-	-	ns
T_ipsu_rx_rmii	RXD[1:0]/CRS_DV/RXER Setup Time to REFCLK	4	-	-	ns
T_iphd_rx_rmii	RXD[1:0]/CRS_DV/RXER Hold Time from REFCLK	2	-	-	ns

Note1: RMII TX timing can be adjusted by setting page7, register16[11:8]; the minimum adjustable resolution is 2ns.
Note2: RMII RX timing can be adjusted by setting page7, register16[7:4]; the minimum adjustable resolution is 2ns.

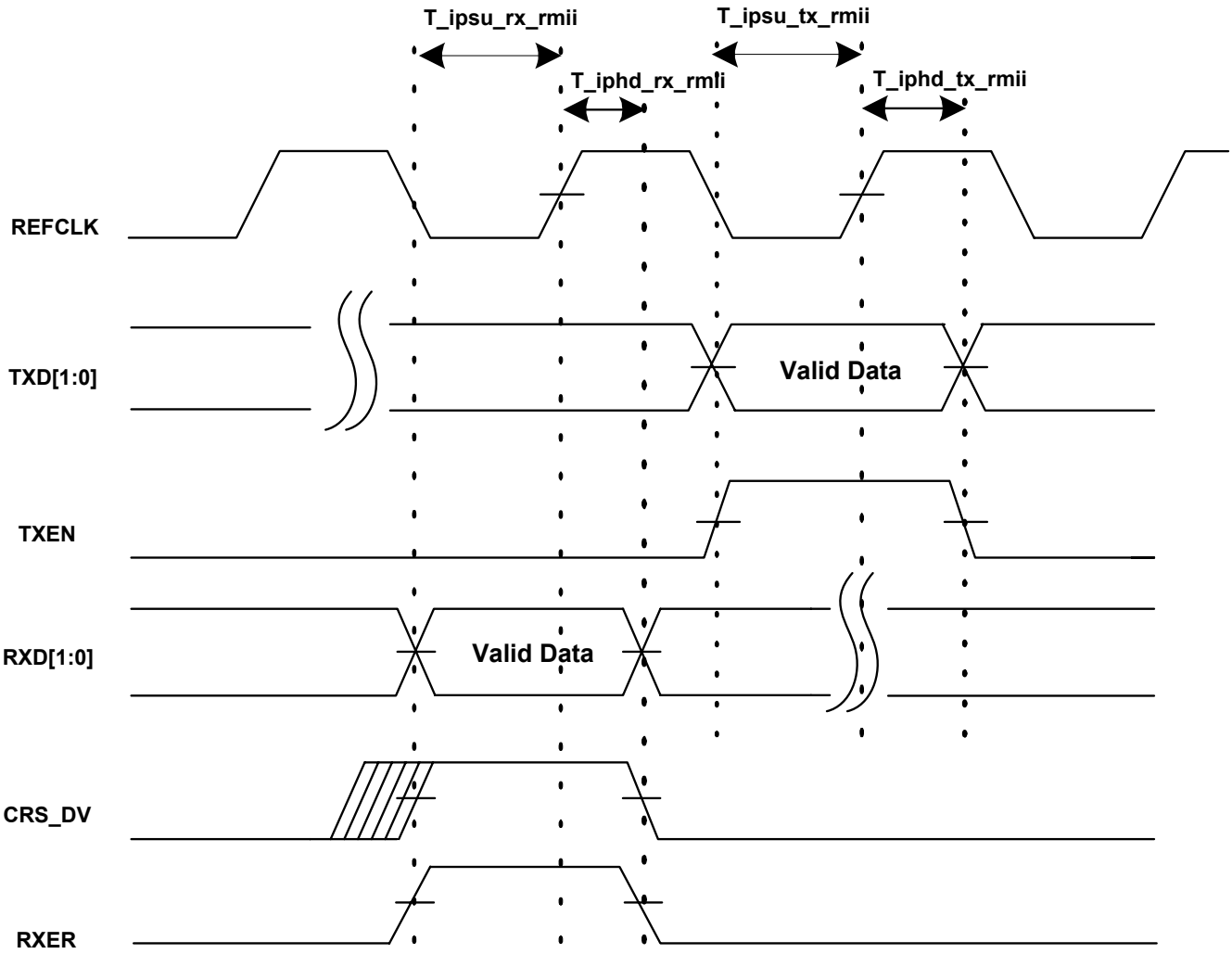


Figure 21. RMII Transmission and Reception Cycle Timing

9.2.4. MDC/MDIO Timing

Table 43. MDC/MDIO Timing

Symbol	Description	Minimum	Maximum	Unit
t_1	MDC High Pulse Width	160	-	ns
t_2	MDC Low Pulse Width	160	-	ns
t_3	MDC Period	400	-	ns
t_4	MDIO Setup to MDC Rising Edge	10	-	ns
t_5	MDIO Hold Time from MDC Rising Edge	10	-	ns
t_6	MDIO Valid from MDC Rising Edge	0	300	ns

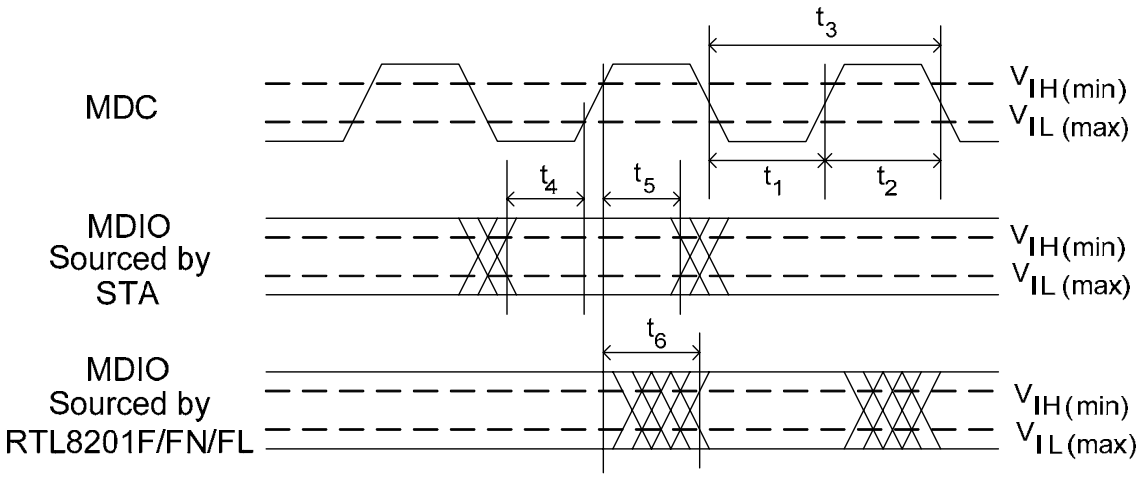


Figure 22. MDC/MDIO Timing

9.2.5. Transmission without Collision

Figure 23 shows an example of a packet transfer from MAC to PHY.

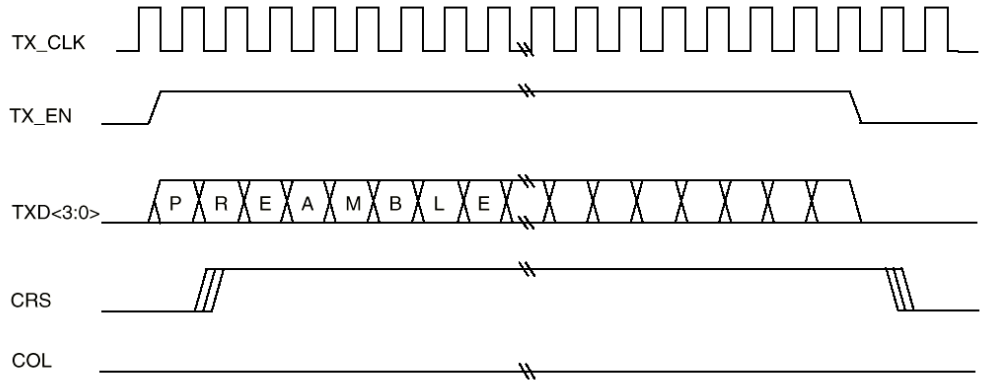


Figure 23. MAC to PHY Transmission without Collision

9.2.6. Reception without Error

Figure 24 shows an example of a packet transfer from PHY to MAC.

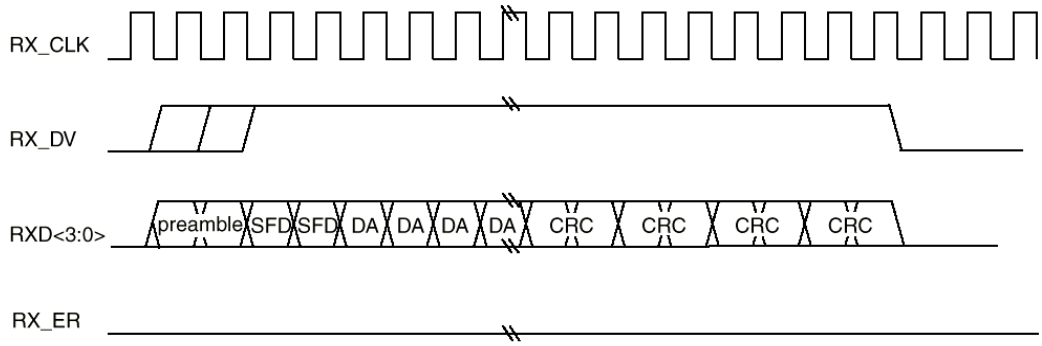


Figure 24. PHY to MAC Reception Without Error

9.3. Crystal Characteristics

Table 44. Crystal Characteristics

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Stability	Parallel Resonant Crystal Frequency Stability, Fundamental Mode, AT-Cut Type. T_a=0°C~70°C.	-30	-	+30	ppm
F_{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=25°C.	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
DL	Drive Level.	-	-	0.3	mW
Jitter	Broadband Peak to Peak Jitter[1, 2]	-	-	500	ps

Note 1: 25KHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.

9.4. Oscillator Requirements

Table 45. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25/50	-	MHz
Frequency Stability	Ta = 0°C~+70°C	-30	-	30	ppm
Frequency Tolerance	Ta = 25°C	-50	-	50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak to Peak Jitter[1, 2]	-	-	-	500	ps
Vpeak-to-peak	-	3.15	3.3	3.45	V
Rise Time (10%~90%)	-	-	-	10	ns
Fall Time (10%~90%)	-	-	-	10	ns
Operating Temperature Range	-	0	-	70	°C

Note 1: 25KHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.

9.5. Clock Requirements

Table 46. Clock Requirements

Parameter	Minimum	Typical	Maximum	Unit
Frequency	-	25/50	-	MHz
Frequency Stability	-30	-	30	ppm
Frequency Tolerance	-50	-	50	ppm
Duty Cycle	40	-	60	%
Broadband Peak to Peak Jitter[1, 2]	-	-	500	ps
Vp-p	3.15	3.3	3.45	V
Rise Time (10%~90%)	-	-	3	ns
Fall Time (10%~90%)	-	-	3	ns

Note 1: 25KHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.

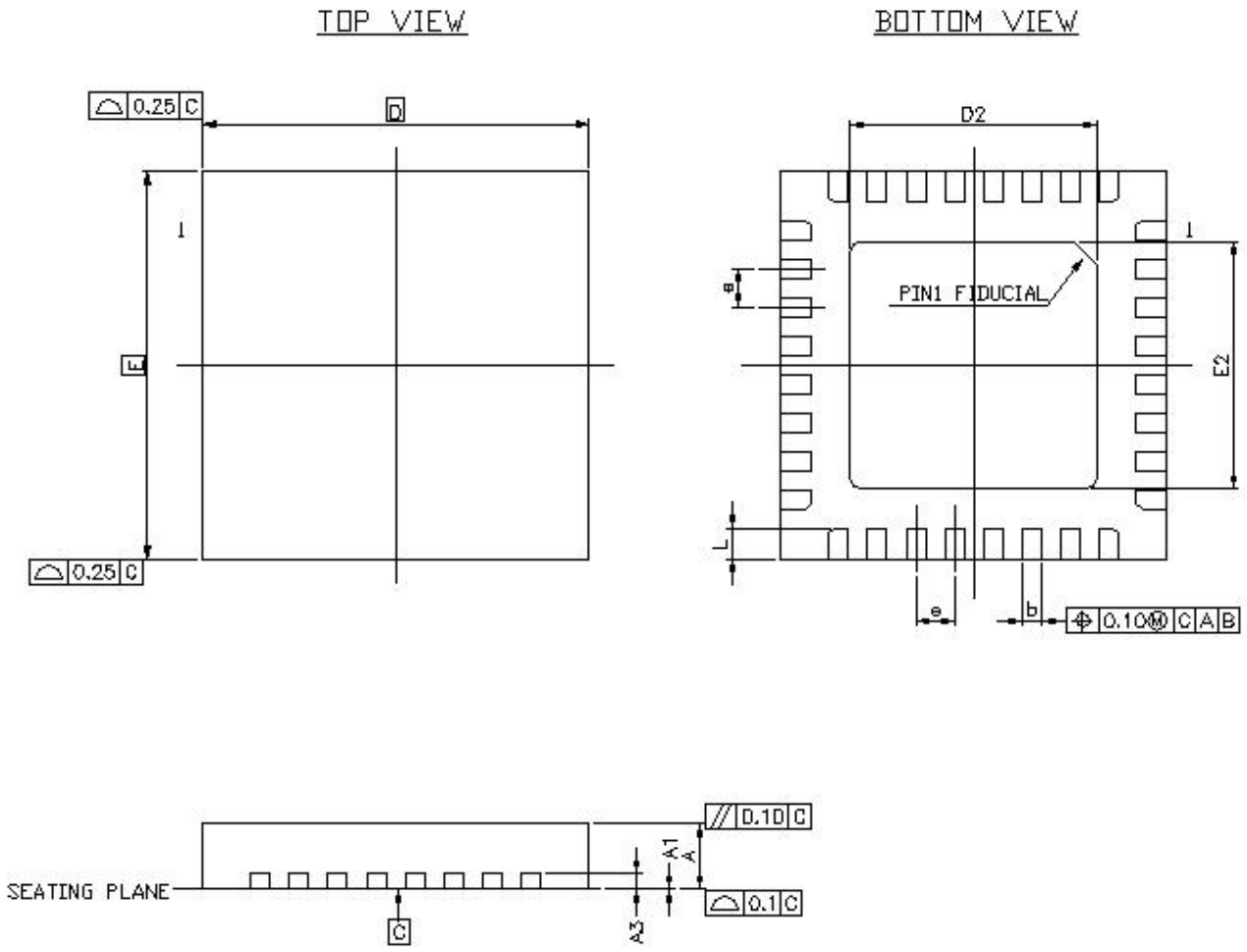
9.6. Transformer Characteristics

Table 47. Transformer Characteristics

Parameter	Transmit End	Receive End
Turn Ratio	1:1 CT	1:1 CT
Inductance (min.)	350µH @ 8mA	350µH @ 8mA

10. Mechanical Dimensions

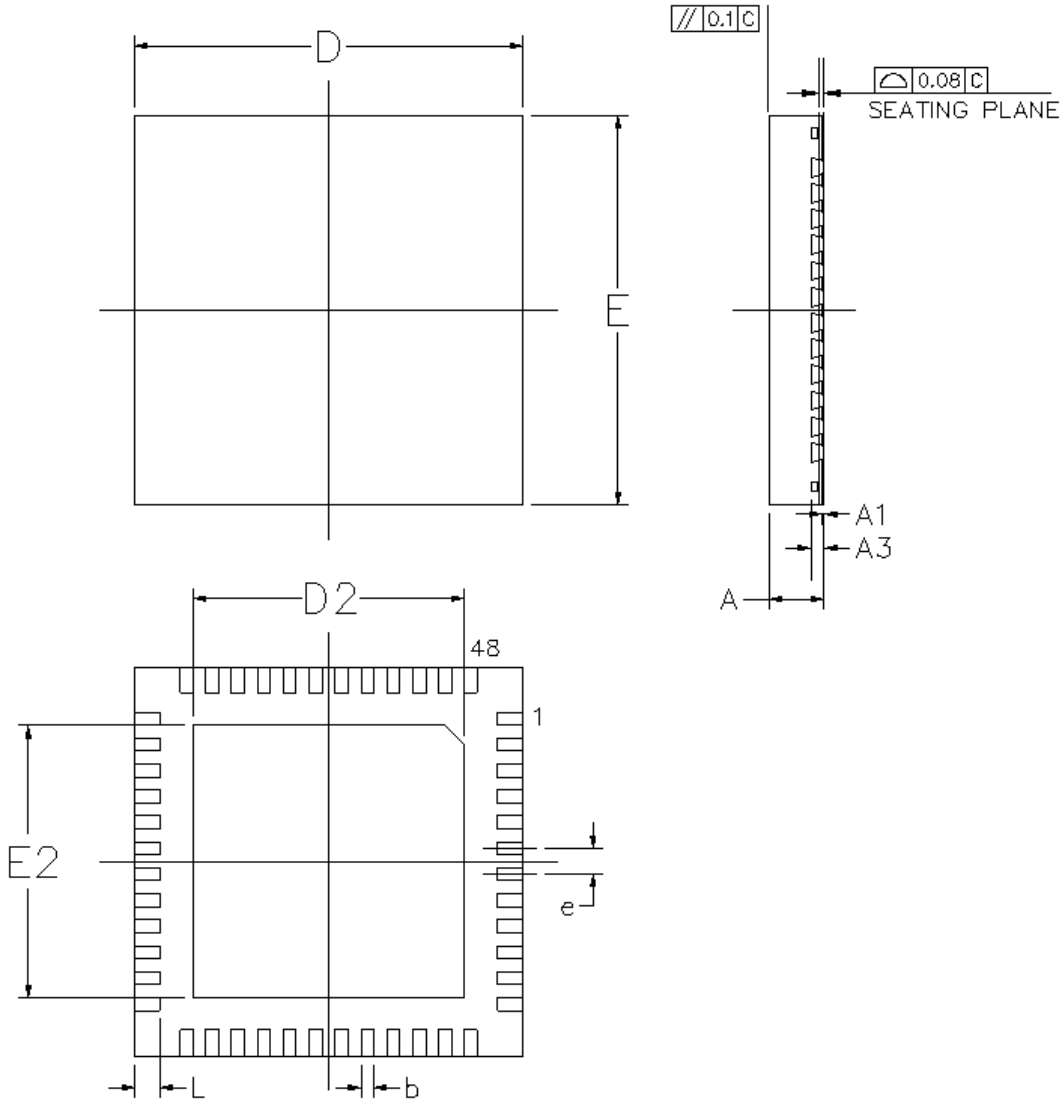
10.1. RTL8201F (QFN-32)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3		0.20REF			0.008REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
c	-	-	0.6	-	-	0.024
D/E		5.00BSC			0.197BSC	
D_2/E_2	3.10	3.35	3.60	0.122	0.132	0.142
e		0.50BSC			0.020BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

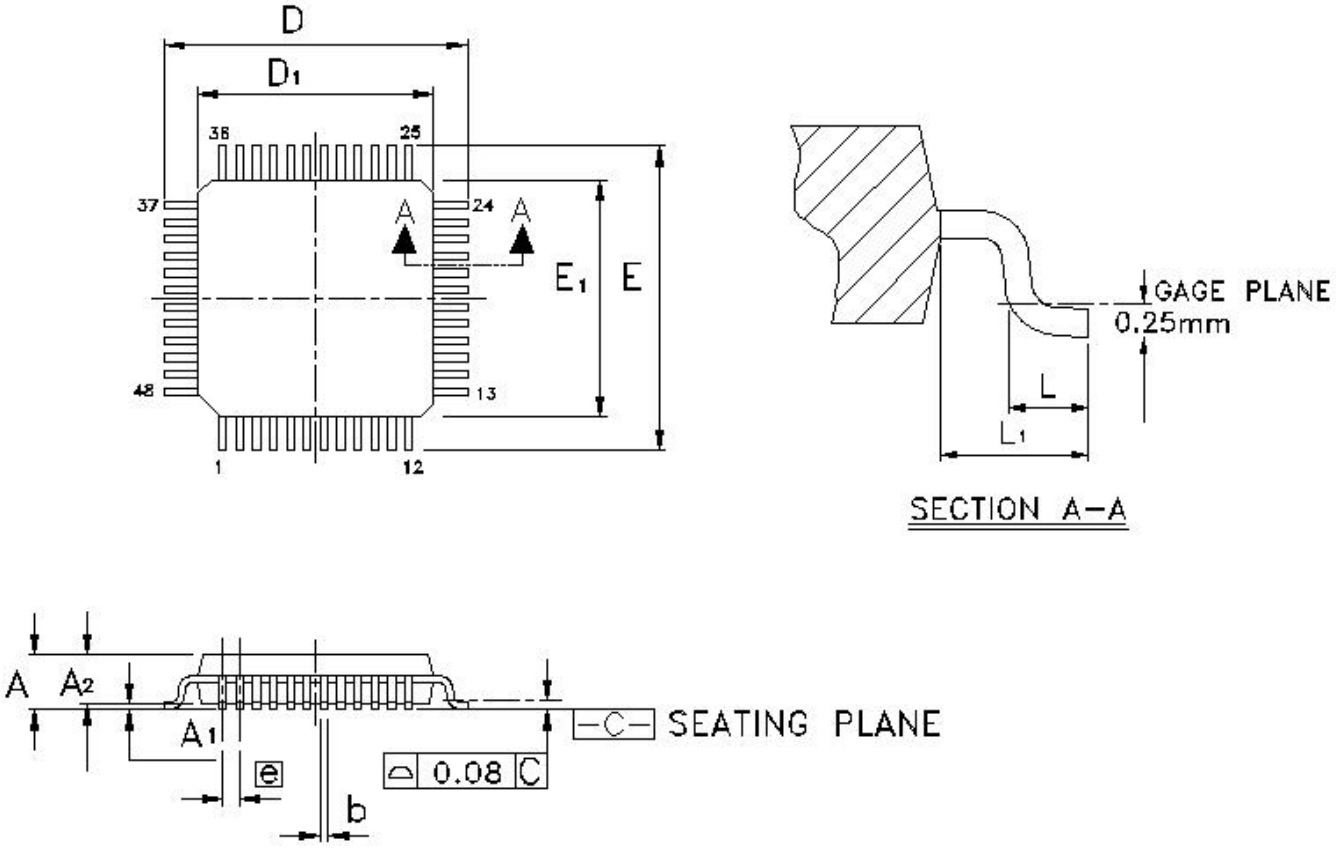
10.2. RTL8201FN (QFN-48)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3		0.20REF			0.008REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		6.00BSC			0.236BSC	
D_2/E_2	4.05	4.4	4.65	0.163	0.173	0.183
e		0.40BSC			0.016BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

10.3. RTL8201FL (LQFP-48)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A_1	0.05	-	0.15	0.002	-	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
D/E	9.00BSC			0.354BSC		
D_1/E_1	7.00BSC			0.276BSC		
e	0.50BSC			0.020BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MS-026.

11. Ordering Information

Table 48. Ordering Information

Part Number	Package	Status
RTL8201F-CG	32-Pin QFN 'Green' Package (for details see Table 49, below)	
RTL8201FN-CG	48-Pin QFN 'Green' Package (for details see Table 49, below)	
RTL8201FL-CG	48-Pin LQFP 'Green' Package (for details see Table 49, below)	

Note: See page 5, 6, and 7 for package identification.

11.1. RTL8201F Series Selection Guide

Table 49. RTL8201F Series Selection Guide

Part Number	Interface	Package	WOL (PMEB Pin)	REF_CLK Direction H/W Strap	EEE	INTB	Number of LEDs	Co-Layout Solution
RTL8201F-CG	RMII MII	QFN32	No	Yes	Yes	Yes*	2	RTL8201E(-VC)
RTL8201FN-CG	RMII MII	QFN48	Yes	Yes	Yes	Yes	3	RTL8211D RTL8211E RTL8201EN-VC
RTL8201FL-CG	RMII MII	LQFP48	No	Yes	Yes	Yes	2	RTL8211CL RTL8201EL RTL8201EL-VC

Note: The RTL8201F INTB pin is used for the interrupt function only when in the RMII mode.

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