RTL8187L

IEEE 802.11a/b/g Wireless LAN Network Interface Controller with USB 2.0 Interface

General Description

The Realtek RTL8187L, fully complying with IEEE 802.11a/b/g specifications, is a low-profile highly integrated cost-effective Wireless LAN USB 2.0 network interface controller that integrates a USB 2.0 PHY, SIE (Serial Interface Engine), 8051 MCU, a Wireless LAN MAC, and a Direct Sequence Spread Spectrum/OFDM baseband processor onto one chip. It provides USB high speed (480Mbps), and full speed (12Mbps), and supports 4 endpoints for transfer pipes. To reduce protocol overhead, the RTL8187L supports Short InterFrame Space (SIFS) burst mode to send packets back-to-back. A protection mechanism prevents collisions among 802.11b nodes.

Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK), and Orthogonal Frequency Division Multiplexing (OFDM) baseband processing are implemented to support all IEEE 802.11a, 802.11b, and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available, along with complementary code keying to provide data rates of 1, 2, 5.5, and 11Mbps, with long or short preamble. A high-speed Fast Fourier Transform (FFT)/Inverse Fast Fourier Transform (IFFT), combined with BPSK, QPSK, 16QAM and 64QAM modulation of the individual sub-carriers, provides data rates of 6, 9, 12, 18, 24, 36, 48 and 54Mbps, with rate-compatible punctured convolutional coding with a coding rate of 1/2, 2/3, and 3/4.

An enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder are built-in to alleviate severe multipath effects. Efficient IQ-imbalance calibration, DC offset, phase noise, frequency offset, and timing offset compensation reduce radio frequency front-end impairments. Selectable digital transmit and receiver FIR filters are provided to meet the requirements of transmit spectrum masks, and to reject adjacent channel interference, respectively. Both in the transmitter and receiver, programmable scaling in the digital domain trades the quantization noise against the increased probability of clipping. Robust signal detection, symbol boundary detection, and channel estimation perform well at the minimum sensitivity.

The RTL8187L supports fast receiver Automatic Gain Control (AGC) and antenna diversity functions, and an adaptive transmit power control function to obtain better performance in the analog portions of the transceiver. It also has on-chip digital-to-analog converters and analog-to-digital converters for analog I and Q inputs and outputs, transmit TSSI and receiver RSSI inputs, and transmit and receiver AGC outputs.

The RTL8187L is highly integrated and requires no 'glue' logic or external memory. It keeps network maintenance costs low and eliminates usage barriers.

Features

- 128-pin LQFP and 128-pin LQFP Lead (Pb)-Free package
- State machine implementation without external memory (RAM, flash) requirement
- Complies with IEEE 802.11a/b/g standards
- Supports descriptor-based buffer management
- Integrated Wireless LAN MAC and Direct Sequence Spread Spectrum/OFDM Baseband Processor in one chip
- Enhanced signal detector, adaptive frequency domain equalizer, and soft-decision Viterbi decoder to alleviate severe multipath effects
- Processing Gain compliant with FCC
- On-Chip A/D and D/A converters for I/Q Data, AGC, and Adaptive Power Control
- Supports both transmit and receive Antenna Diversity
- Data rates of 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, and 54Mbps
- Supports 40MHz OSC as the internal clock source. The frequency deviation of the OSC must be within 25 PPM on IEEE 802.11g and 20 PPM on IEEE 802.11a
- Supports Wake-On-LAN (WOL) function and remote wake-up (Magic Packet and Microsoft® wake-up frame)
- Supports 4 WOL signals (active high, active low, positive pulse, and negative pulse)
- IEEE 802.11g protection mechanisms for both RTS/CTS and CTS-to-self
- Burst-mode support for dramatically enhanced throughput
- DSSS with DBPSK and DQPSK, CCK modulations and demodulations supported with long and short preamble

- OFDM with BPSK, QPSK, 16QAM and 64QAM modulations and demodulations supported with rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, and 3/4
- Efficient IQ-imbalance calibration, DC offset, phase noise, frequency offset and timing offset compensation reduce analog front-end impairments
- Selectable digital transmit and receiver FIR filters provided to meet transmit spectrum mask requirements and to reject adjacent channel interference
- Programmable scaling both in transmitter and receiver to trade quantization noise against the increased probability of clipping
- Fast receiver Automatic Gain Control (AGC) & antenna diversity functions
- Hardware-based IEEE 802.11i encryption/decryption engine, including 64-bit/128-bit WEP, TKIP, and AES
- Supports Wi-Fi alliance WPA and WPA2 security
- Contains two large independent transmit and receive FIFO buffers
- Advanced power saving mode when the LAN and wakeup function are not used
- Uses 93C46 (64*16-bit EEPROM) or 93C56 (128*16-bit EEPROM) to store resource configuration and ID parameter data
- LED pins for various network activity indications
- Two GPIO pins supported
- Supports digital loopback capability on both ports
- Scatter and gather operation
- Complies with USB Specification 2.0
    - Supports Full-speed (12Mbps) and High-speed (480Mbps)
- Embedded standard 8051 CPU with enhanced features:
    - Four cycles per instruction
    - Variable clock speed cuts power consumption
- Supports USB remote wake-up feature
- Supports 4 endpoints:
    - 64-Byte buffer for control endpoint
    - 512-Byte buffer for bulk IN endpoint
    - Two 512-Byte buffers for bulk OUT endpoint
- 3.3V and 1.8V power supplies required
- 5V tolerant I/Os
- 0.18μm CMOS process

Applications

- USB Dongle WLAN adapter
- Embedded WLAN solution in notebook, desktop, mobile phone, and motherboard