Reverse engineered chipset registers (by tiseno100)

BIOS talks to E0-E1h for configuration.

The registers are extremely similar to another documented ALD chipset (93C488)

https://theretroweb.com/chipsets/1040

Ports E0-E1h Memory Control

00-03h: Bank 0 - 3 configuration

04h: Shadow control 1, access control

05h: Shadow control 2, write protected control

06h: 384K relocation control

07-08h: Reserved

09h: DRAM timing 1

0Ah: DRAM timing 2

0Bh: DRAM timing 3

0Ch: DRAM timing 4

0Dh: Write cycle control

0Eh: Reserved

0Fh: Reserved? BIOS write B1h

10-11h: Cache control

Ports 22-23h Potentially ISA Control

Can't make any sense out of it.

Refer to the 93C488 Datasheet for details

May be inaccurate. I can't confirm it 100% but it's the best extract I could make with whatever information I could get by the datasheet and the BIOS

PCI slot devices might be 1Eh and 1Fh. It seems to have no PCI device dummy in there or at least didn't found it. By datasheet it seems to lack it in general "which violates the PCI standard"(Confirmation needed)