Product Brief
February 2006
Revision 1.3

PC87427 ServerI/O with SensorPath™ Health Monitoring

General Description

The Winbond PC87427 is targeted for a wide range of servers, workstations and high-end desktops that use the Low Pin Count (LPC) bus for the host interface and an SMBus® interface for either a Baseboard Management Controller (BMC) or mini-BMC (mBMC), both of which are optional.

For LPC and SMBus access, the PC87427 features a fast X-Bus, over which boot flash and I/O devices can be accessed. The PC87427 supports X-Bus address line forcing (to 0 or 1) to create memory windows for BIOS data storage.

When V_{SB} exists, the BMC or mBMC can access the PC87427 and its fast X-Bus via SMBus. The SMBus also controls serial port float, RTC access, and serial port interconnection (snoop and take-over modes). In addition, the PC87427 provides routing of up to two selected LPC I/O port transactions to the GPIO Extension Port.

The PC87427 provides a V_{SB}-powered high-frequency clock for on-chip peripherals; it also provides a configurable high-frequency clock for other V_{SB}-powered platform components.

The PC87427 supports SensorPath health monitor interface to LMxx sensors, fan monitoring and control, and a chassis intrusion detector.

The System Wake-Up Control (SWC) module supports flexible wake-up and power-off request mechanisms for all platforms (i.e., with or without BMC/mBMC).

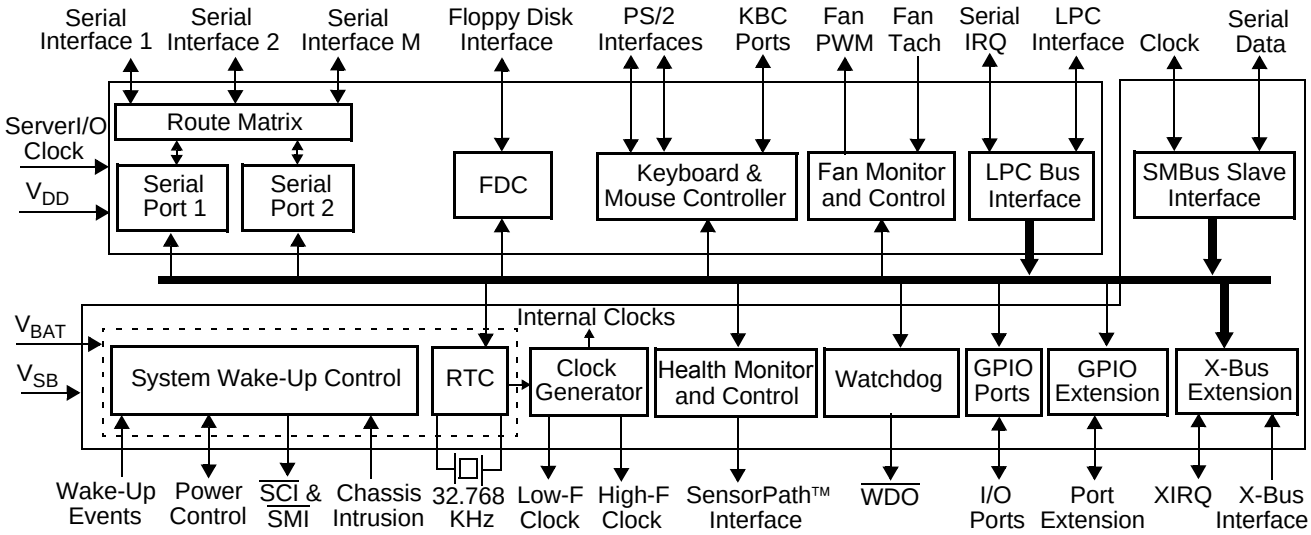
The PC87427 supports both I/O and memory mapping of module registers and enables building legacy-free systems.

The PC87427 also incorporates a Floppy Disk Controller (FDC), two serial ports (UARTs), a Keyboard and Mouse Controller (KBC), General-Purpose Input/Output (GPIO), GPIO extension for additional off-chip GPIO ports, and an interrupt serializer for parallel IRQs.

Outstanding Features

- Legacy-reduced Advanced I/O, optimized for high-end platforms. Legacy modules: FDC, two Serial Ports (UARTs) and a Keyboard and Mouse Controller (KBC).
- SensorPath system health support for LMxx sensors, fan monitor/control, and chassis intrusion detection, for all platforms (i.e., with or without a BMC or mBMC).
- 8/16-bit fast X-Bus extension for boot flash, memory and I/O.
- I/O-mapped and memory-mapped registers.
- V_{SB}-powered SMBus access to modules and fast X-Bus.
- Two sets of BIOS code and data support, for main and back-up BIOS.
- Extremely low current consumption in Battery Backup mode.
- Serial Interface for manageability (Serial Interface M). Two-to-one multiplexing of Serial Ports 1 and 2.
- 52 GPIO ports with a variety of wake-up events, plus GPIO extension for additional off-chip GPIO ports.
- Watchdog for autonomous system recovery for BIOS Boot process and for operating system use.
- 128-pin TFBGA package (for blade applications) and 128-pin PQFP package.

Block Diagram



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Features

System Health Support

- SensorPath interface to sensors optimizes digital/analog partitioning
  - Simplifies board design and routing
  - Supports distributed sensors and centralized control
  - Off-loads SMBus, faster boot time
- Fan Monitor and Control (FMC)
  - Four PWM-based fan controls
  - Eight 16-bit resolution tachometer inputs
  - Software or local temperature feedback control
- Chassis intrusion detection

Bus Interfaces

- LPC Bus Interface
  - Based on Intel's *LPC Interface Specification Revision 1.1, August, 2002*
  - Synchronous cycles using up to 33 MHz bus clock
  - 8-bit I/O and 8-bit Memory read and write cycles
  - Up to four 8-bit DMA channels
  - Serial IRQ
  - Supports bootable memory
  - Supports LPC and FWH boot transactions
  - Supports registers memory and I/O mapping
- SMBus Interface
  - Compliant with *SMBus Specification Revision 2.0, August 3, 2000*
  - Enables a system controller to access the internal functions and the fast X-Bus extension
  - Proprietary commands for read/write byte from/to:
    - Internal register
    - X-Bus I/O device
    - X-Bus memory device
  - Slave address:
    - One of two values selected by strap
    - Programmable through the LPC bus
    - V_{BAT} backed-up
  - Supports $\overline{\text{SMBALERT}}$
  - Concurrent access with the LPC bus
  - V_{SB} powered
  - Optional internal pull-up on the two SMBus pins
- Fast X-Bus Extension
  - Supports I/O and memory read/write operations
  - 8- or 16-bit data bus, 28-bit addressing
  - Accessible from both LPC bus and SMBus
  - V_{SB} powered
  - Boot configuration selected by straps
  - Programmable protection control for access from the LPC bus
  - Supports three XIRQ external interrupts
  - Multiplexed address-data lines:
    - Four direct address lines
    - Partial non-multiplexed option
  - Four chip-select outputs, each supporting multiple zones:
    - Two BIOS memory zones (up to 32 Mbytes total)
    - Two user-defined memory zones (up to 32 Mbytes total)
    - Four user-defined I/O zones
  - Address line forcing (to 0 or 1) for access to two BIOS code and data sets
  - Optional indirect addressing of memory
  - $\overline{\text{XRD}}$-XEN or $\overline{\text{XWR}}$-XR/$\overline{\text{W}}$ mode support
  - Supports both slow and fast devices
  - For faster transactions in 16-bit data bus, strobe signals for address latches change automatically only when the address is changed
- Configuration Control
  - Compliant with *PC2001 Specification Revision 1.0, 1999-2000*
  - Compliant with *Hardware Design Guide Version 3.0 for Microsoft Windows 2000 Server, June 30 2000*
  - Plug and Play (PnP) Configuration register structure
  - Base Address strap, to setup the address of the Index-Data register pair
  - Flexible resource allocation for all logical devices:
    - Relocatable base address
    - 15 IRQ routing options to serial IRQ
    - Up to four optional 8-bit DMA channels
  - SMBus control over pin multiplexing, module disable and output TRI-STATE® for all Legacy modules

Legacy Modules

- Serial Ports 1 and 2
  - Software compatible with the 16550A and the 16450
  - Supports shadow register for write-only bit monitoring
  - UART data rates up to 1.5 Mbaud
  - Three sets of Serial Interface pins
    - Serial Interface 1
    - Snoop or Take-over connection of Serial Interface M
    - Two-to-one multiplexing of Serial Ports 1 and 2 to Serial Interface 2
- Floppy Disk Controller (FDC)
  - Programmable write protect
  - Supports FM and MFM modes
  - Supports Enhanced mode command for three-mode Floppy Disk Drive (FDD)
  - Perpendicular recording drive support for 2.88 MB
  - Burst and Non-Burst modes
  - Full support for IBM Tape Drive Register (TDR) implementation of AT and PS/2 drive types
  - 16-byte FIFO
  - Error-free handling of data overrun and underrun

Features (Continued)

- — Software compatible with the PC8477, which contains a superset of the FDC functions in the μDP8473, NEC μPD765A/B and N82077
- — High-performance digital separator
- — Supports standard 5.25" and 3.5" FDDs
- — Supports one FDD
- — Supports fast tape drives (2 Mbps) and standard tape drives (1 Mbps, 500 Kbps and 250 Kbps)

■ Keyboard and Mouse Controller (KBC)
- — 8-bit microcontroller, software compatible with 8042AH and PC87911
- — Standard interface (60h, 64h, IRQ1 and IRQ12)
- — Supports two external swapable PS/2 interfaces for keyboard and mouse
- — Five programmable, dedicated, quasi-bidirectional I/O lines (Fast GA20/P21, $\overline{\text{KBRST}}$/P20, P12, P16, P17)

General-Purpose I/O Module

■ 52 General-Purpose I/O (GPIO) Ports
- — Individually assigned to either LPC or SMBus control
- — 45 ports individually configured as input or output
- — 7 output ports
- — Programmable features for each output pin:
  - ❑ Drive type (open-drain, push-pull or TRI-STATE)
  - ❑ TRI-STATE on V_{DD}-fall detection for pins driving V_{DD}-supplied devices
- — Programmable option for internal pull-up resistor on each input pin
- — Lock option for the configuration and data of each output pin
- — 16 GPIO ports generate IRQ/$\overline{\text{SIOSMI}}$/$\overline{\text{SIOSCI}}$ for wake-up events, with individual:
  - ❑ Enable control
  - ❑ Polarity and edge/level selection
  - ❑ Debounce mechanism
- — V_{SB} powered
- — Low-cost external GPIO port extension via a serial bus
- — I/O ports transactions routing to the GPIO port extension

■ Real-Time Clock
- — DS1287, MC146818 and PC87911 compatible
- — Battery-backed 242-byte CMOS RAM, in two banks (accessed through 70-71h and 72-73h)
- — Selective lock mechanisms for the RTC RAM
- — Y2K-compliant calendar, including century and automatic leap-year adjustment
- — Time of day in seconds, minutes and hours, which allows a 12-hour or 24-hour format with optional adjustment for daylight saving time
- — Separated SMBus access to RTC RAM and RTC Control D register
- — Battery level measurement

Power Management

■ Supports *ACPI Specification Revision 3.0, September 2, 2004*

■ System Wake-Up Control (SWC)
- — Wake-up request on detection of:
  - ❑ Preprogrammed Keyboard or Mouse sequence
  - ❑ External modem ring from $\overline{\text{RI1}}$ or $\overline{\text{RI2}}$ on serial ports
  - ❑ Predetermined RTC date and time alarm
  - ❑ General-Purpose Input Events from up to 16 GPIO pins
  - ❑ IRQs of internal logical devices
- — Optional routing of power-up request to SERIRQ, $\overline{\text{SIOSMI}}$, $\overline{\text{SIOSCI}}$, $\overline{\text{PWBTOUT}}$ and $\overline{\text{ONCTL}}$
- — Routing control per input/output event combination
- — Outputs enable/disable per event and system state combination (ACPI Sx states)
- — Implements bank “b” of the ACPI registers
- — Suspend modes via software emulation (control)
- — Battery-backed event-logic configuration
- — Power Button support, featuring:
  - ❑ On/Off control
  - ❑ Power-off, 4-second override
  - ❑ Power Button output
- — Sleep Button support

■ Power Supply On/Off control
- — Supports Legacy- and ACPI-compatible Power Button
- — Direct power supply control in response to wake-up events
- — Programmable Crowbar time-out for “On” request
- — On/Off control via software emulation
- — Power-fail recovery

■ Enhanced Power Management (PM), including:
- — Special configuration registers for power down
- — Reduced current leakage from pins
- — Low-power CMOS technology
- — Capability for disabling all modules

■ Keyboard Events
- — Wake-up on any key
- — Supports programmable 8-byte sequence “password” for Power Management
- — Simultaneous recognition of three programmable keys (sequences): “Power”, “Sleep” and “Resume”

■ Power Active Timers
- — Two power-on, elapsed-time counters for the main (V_{DD}) and standby (V_{SB}) power supplies
- — 32-bit counters, clocked by a 1-second clock
- — V_{BAT} backed-up counters

Features

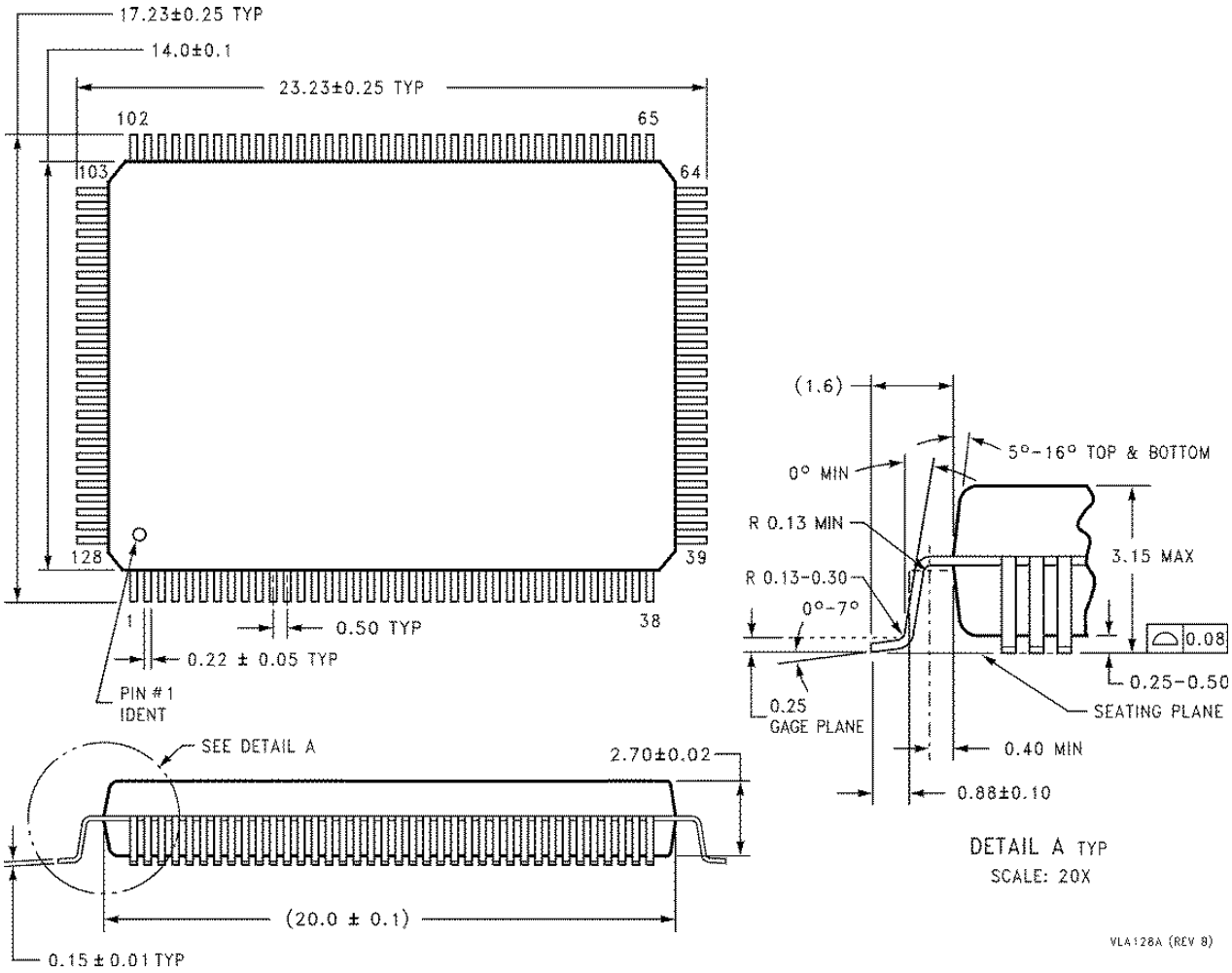
- Watchdog
  - Compliant with *Watchdog Timer Hardware Requirements for Microsoft Windows .NET Server, April 2002*
  - Autonomous system reset and programmable address line forcing on expiration of watchdog timer
  - Generates a 100 ms pulse at $\overline{\text{WDO}}$ pin

Clocking, Supply and Package Information

- Strap Input Controlled Operating Modes
  - Base Address ($\overline{\text{BADDR}}$) for the PnP Index-Data register pair
  - Input clock presence ($\overline{\text{CKIN48}}$) select
  - X-Bus configuration ($\overline{\text{XCNF2-0}}$) select
  - SMBus slave address ($\overline{\text{SMBSA}}$) select
  - High frequency clock selection ($\overline{\text{HFCKS}}$)
- Testability
  - XOR tree structure
    - Includes all the device pins (except the supply pins, oscillator pins and CHASSIS pin)
    - Selected at power-up by strap input ($\overline{\text{TEST}}$)
  - TRI-STATE device pins, selected at power-up by strap input ($\overline{\text{TRIS}}$)
- Clocks
  - LPC clock input (up to 33 MHz)
  - ServerI/O modules clock: 48 MHz input or internal clock multiplier
  - 32.768 KHz crystal
  - On-chip low-frequency clock generator:
    - 32.768 KHz for RTC, System Wake-Up Control (SWC), Power Active timers and the high-frequency clock generator
    - Very low power consumption
    - V_{BAT} powered
  - On-chip high-frequency clock generator:
    - Based on the 32.768 KHz clock
    - V_{SB} powered
  - Clock outputs:
    - LFCKOUT - 32.768 KHz or 1 Hz
    - HFCKOUT - configurable up to 48 MHz. The default frequency 6, 10, 24 or 40 MHz, configurable by strap.
- Protection
  - All pins are 5V tolerant and back-drive protected (except the LPC bus pins)
  - Separate battery pin that includes an internal UL protection resistor
  - GPIO multiplexing configuration lock
- Power Supply
  - 3.3V supply operation
  - Separate pins for main (V_{DD}) and standby (V_{SB}) power supplies
  - Backup battery input for RTC, SWC and Power Active timers
  - Separate pin for core voltage filtering (V_{CORF})
  - Reduced standby power consumption
  - Very low power consumption for RTC and timers (0.9 µA typical) from backup battery
- Packages
  - 128-pin PQFP
  - 128-pin TFBGA

Physical Dimensions

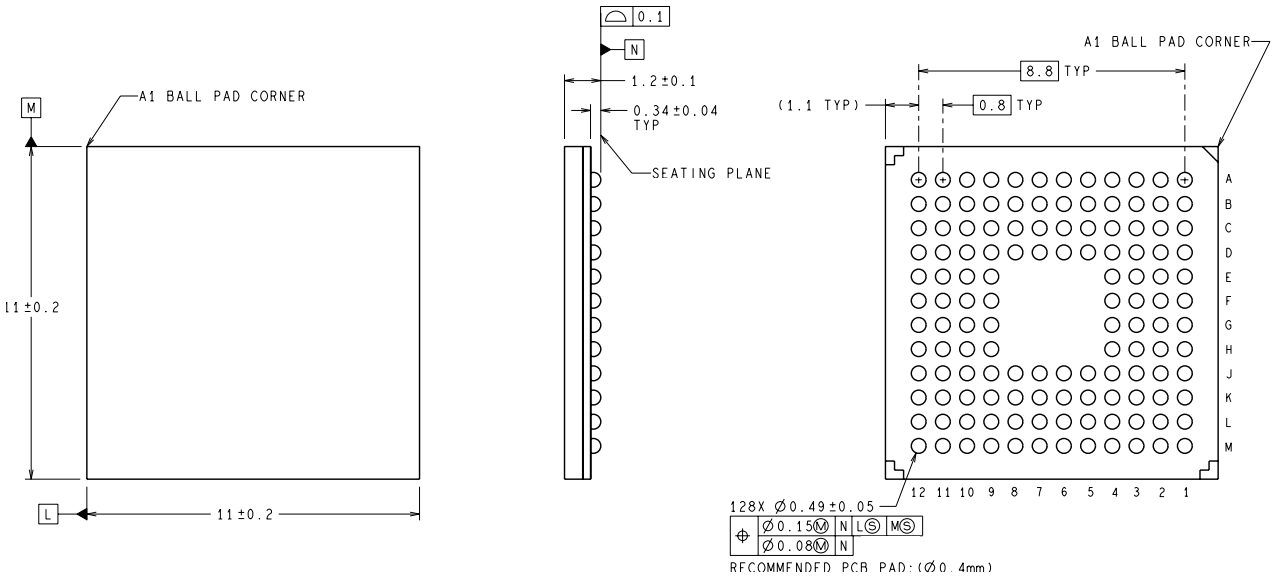
All dimensions are in millimeters



Plastic Quad Flatpack (PQFP), JEDEC

Physical Dimensions (continued)

All dimensions are in millimeters



128-Pin Thin Fine Pitch Ball Grid Array (TFBGA)

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Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

For Advanced PC Product Line information contact: APC.Support@winbond.com

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