National Semiconductor

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Revision 1.1

PC8374L
SensorPath™ SuperI/O with Glue Functions

General Description

The National Semiconductor PC8374L Advanced I/O product is a member of the PC837x SuperI/O family. All PC837x devices are highly integrated and are pin and software compatible, thus providing drop-in interchangeability and enabling a variety of assembly options using only a single motherboard and BIOS.

PC8374L integration allows for a smaller system board size and saves on total system cost.

The PC8374L includes legacy SuperI/O functions, system glue functions, health monitoring and control, commonly used functions such as GPIO, and ACPI-compliant Power Management support.

The PC8374L integrates miscellaneous analog and digital system glue functions to reduce the number of discrete components required. The host communicates with the functions integrated in the PC8374L device through an LPC Bus Interface.

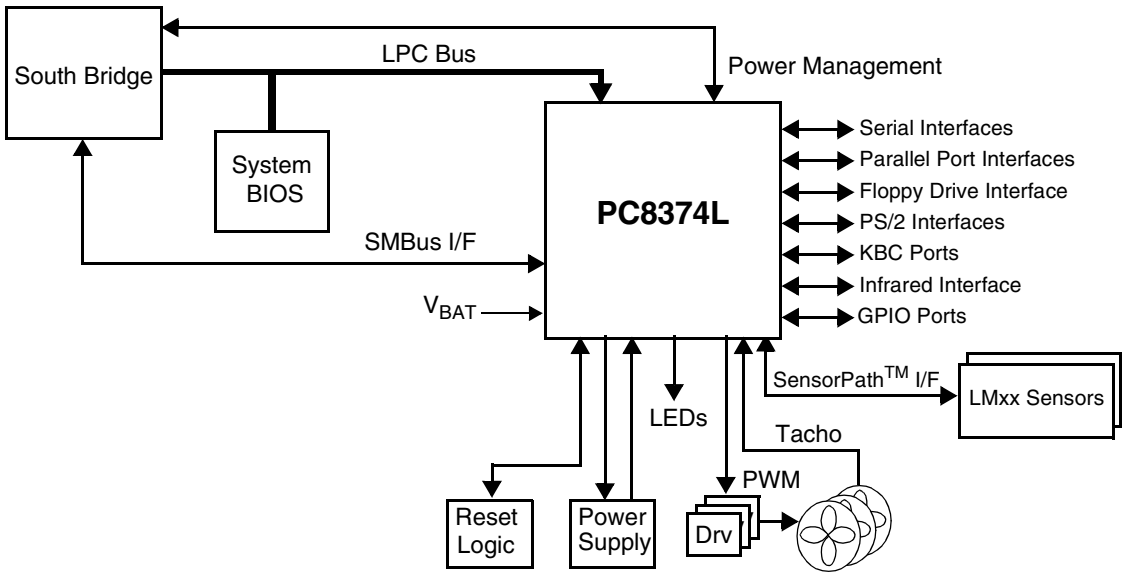
The PC8374L extended wake-up support complements the ACPI controller in the chipset. The System Wake-Up Control (SWC) module, powered by V_{SB3}, supports a flexible wake-up mechanism.

The PC8374L supports both I/O and memory mapping of module registers and enables building legacy-free systems.

Outstanding Features

- SensorPath™ interface to LMxx sensor devices for system health support
- Fan monitor and control
- Heceta6-compatible register set, accessible via the LPC interface and SMBus
- Glue functions to complement the South Bridge functionality
- V_{SB3}-powered Power Management with 19 wake-up sources
- Controls three LED indicators
- 16 GPIO ports with a variety of wake-up options
- I/O-mapped and memory-mapped registers
- Legacy modules: Parallel Port, Floppy Disk Controller (FDC), two Serial Ports, Slow InfraRed Port and a Keyboard and Mouse Controller (KBC)
- LPC interface, based on Intel's *LPC Interface Specification Revision 1.1, August 2002*
- *PC01 Revision 1.0* and *Advanced Configuration and Power Interface (ACPI) Specification Revision 2.0* compliant
- 128-pin PQFP package

Block Diagram



Features

System Health Support

- SensorPath interface to sensors optimizes digital/analog partitioning
  - Simplifies board design and routing
  - Supports distributed sensors and centralized control
  - Health monitoring is self-contained and requires minimal host attention
  - Faster boot time
  - Off loads SMBus, and enables ASF compliance
- Fan Monitor and Control
  - Three PWM-based fan controls
  - Four 16-bit resolution tachometer inputs
  - Software or local temperature feedback control
- Heceta6-compatible register set accessible via the LPC interface and SMBus
  - Supports the following combinations of LMxx devices:
    - LM96011 and optional LM95010
    - LM96012
    - LM96010
  - Simultaneous read support via LPC interface and SMBus

Glue Functions

- Generates the power-related signals:
  - Main Power good
  - Power distribution control (for switching between Main and Standby regulators)
  - Resume reset (Master Reset) according to the 5V standby supply status
  - Main power supply turn on ($\overline{PS\_ON}$)
- Voltage translation between 2.5V or 3.3V levels (DDC) and 5V levels (VGA) for the SMBus serial clock and data signals
- Isolation circuitry for the SMBus serial clock and data signals
- Buffers $\overline{PCI\_RESET}$ to generate two reset output signals
- Buffers $\overline{PCI\_RESET}$ to generate IDE reset output.
- Generates "highest active supply" reference voltage
  - Based on 3.3V and 5V Main supplies
  - Based on 3.3V and 5V Standby supplies
- High-current LED driver control for Hard Disk Drive activity indication
- Software selectable alternative functionality, through pin multiplexing

General-Purpose I/O (GPIO) Ports

- All 16 GPIO ports powered by V_{SB3}
- Each pin individually configured as input or output
- Programmable features for each output pin:
  - Drive type (open-drain, push-pull or TRI-STATE®)
  - TRI-STATE on detection of falling V_{DD3} for V_{SB3}-powered pins driving V_{DD}-supplied devices
- Programmable option for internal pull-up resistor on each input pin (some with internal pull-down resistor option)
- Lock option for the configuration and data of each output pin
- 15 GPIO ports generate IRQ/$\overline{SIOPME}$ for wake-up events; each GPIO has separate:
  - Enable control of event status routing to IRQ
  - Enable control of event status routing to $\overline{SIOPME}$ (via SWC)
  - Polarity and edge/level selection
    - Programmable debouncing

Power Management

- Supports *ACPI Specification Revision 2.0b, July 27, 2000*
- System Wake-Up Control (SWC)
  - Optional routing of events to generate SCI ($\overline{SIOPME}$) on detection of:
    - Keyboard or Mouse events
    - Ring Indication $\overline{RI}$ on each of the two serial ports
    - General-Purpose Input Events from 15 GPIO pins
    - IRQs of the Keyboard and Mouse Controller
    - IRQs of the other internal modules
  - Optional routing of the SCI ($\overline{SIOPME}$) to generate IRQ (SERIRQ)
  - Implements the GPE1_BLK of the ACPI General Purpose (Generic) Register blocks with "child" events
  - V_{SB3}-powered event detection and event-logic configuration
- Enhanced Power Management (PM), including:
  - Special configuration registers for power down
  - Low-leakage pins
  - Low-power CMOS technology
  - Ability to disable all modules
  - High-current LED drivers control (two LEDs) for power status indication with:
    - Standard blinking, controlled by software
    - Advanced blinking, controlled by power supply status, sleep state or software
    - Special blinking, controlled by power supply status, sleep state and software bit
  - V_{BAT}-powered indication of the Main power supply state before an AC power failure
- Keyboard Events
  - Wake-up on any key
  - Supports programmable 8-byte sequence "Password" or "Special Keys" for Power Management
  - Simultaneous recognition of three programmable keys (sequences): "Power", "Sleep" and "Resume"
  - Wake-up on mouse movement and/or button click

Bus Interface

- LPC Bus Interface
  - Based on Intel's *LPC Interface Specification Revision 1.1, August 2002*
  - I/O, Memory and 8-bit Firmware Memory read and write cycles
  - Up to four 8-bit DMA channels
  - Serial IRQ (SERIRQ)
  - Supports registers memory and I/O mapping

Features (Continued)

- Configuration Control
  - PnP Configuration Register structure
  - *PC01 Specification Revision 1.0, 1999-2000* compliant
  - Base Address strap ($\overline{\text{BADDR}}$) to setup the address of the Index-Data register pair (defaults to 2Eh/2Fh)
  - Flexible resource allocation for all logical devices:
    - Relocatable base address
    - 15 IRQ routing options to serial IRQ
    - Up to four optional 8-bit DMA channels
  - Configurable feature sets:
    - Software selectable
    - V_{SB3}-powered pin multiplexing

Legacy Modules

- Serial Ports 1 and 2
  - Software-compatible with the NS16550A and NS16450
  - Support shadow register for write-only bit monitoring
  - Data rates up to 1.5 Mbaud
- Serial Infrared Port (SIR)
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - HP-SIR
  - ASK-IR option of SHARP-IR
  - DASK-IR option of SHARP-IR
  - Consumer Remote Control supports RC-5, RC-6, NEC, RCA and RECS 80
- IEEE 1284-compliant Parallel Port
  - ECP, with Level 2 (14 mA sink and source output buffers)
  - Software or hardware control
  - Enhanced Parallel Port (EPP) compatible with EPP 1.7 and EPP 1.9
  - Supports EPP as mode 4 of the Extended Control Register (ECR)
  - Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
  - Supports a demand DMA mode mechanism and a DMA fairness mechanism for improved bus utilization
  - Protection circuit that prevents damage to the parallel port when a printer connected to it is powered up or is operated at high voltages (in both cases, even if the PC8374L is in power-down state)
- Floppy Disk Controller (FDC)
  - Software compatible with the PC8477 (the PC8477 contains a superset of the FDC functions in the μDP8473, NEC μPD765A/B and N82077 devices)
  - Error-free handling of data overrun and underrun
  - Programmable write protect
  - Supports FM and MFM modes
  - Supports Enhanced mode command for three-mode Floppy Disk Drive (FDD)
  - Perpendicular recording drive support for 2.88 MBytes
  - Burst (16-byte FIFO) and Non-Burst modes
  - Full support for IBM Tape Drive Register (TDR) implementation of AT and PS/2 drive types
  - High-performance digital separator
  - Supports fast tape drives (2 Mbps) and standard tape drives (1 Mbps, 500 Kbps and 250 Kbps)
- Keyboard and Mouse Controller (KBC)
  - 8-bit microcontroller, software compatible with 8042AH and PC87911
  - Standard interface (60h, 64h, IRQ1 and IRQ12)
  - Supports two external swapable PS/2 interfaces for keyboard and mouse
  - Programmable, dedicated quasi-bidirectional I/O lines (GA20/P21, $\overline{\text{KBRST}}$/P20)

Clocking, Supply, and Package Information

- Clocks
  - LPC (PCI) clock input (up to 33 MHz)
  - On-chip Clock Generator:
    - Generates 48 MHz clock
    - Generates 32.768 KHz internal clock
    - V_{SB3} powered
    - Based on the 14.31818 MHz clock input
- Protection
  - All pins are 5V tolerant and back-drive protected (except LPC bus pins)
  - High ESD protection of all the pins
  - Pin multiplexing selection lock
  - Configuration register lock
- Testability
  - XOR tree structure
    - Includes all the pins (except supply, analog and not connected pins)
    - Selected at power-up by strap input ($\overline{\text{TEST}}$)
  - TRI-STATE pins, selected at power-up by strap input ($\overline{\text{TRIS}}$)
- Power Supply
  - 3.3V supply operation
  - Separate pin pairs for main (V_{DD3}) and standby (V_{SB3}) power supplies
  - Backup battery input (V_{BAT}) for SWC indications
  - Low standby power consumption
  - Very low power consumption from backup battery (less than 0.5 μA)
- Package
  - 128-pin PQFP

Revision Record

Revision Date	Status	Comments
March 17, 2003	Draft Revision 0.03	First Draft of Arch. Spec.
April 15, 2003	Draft Revision 0.1	Add Serial InfraRed Port Update all sections
June 7, 2003	Draft Revision 0.3	Change Clock generator and CLOCKCF register Add Heceta6 Emulation module and complementing configuration registers: H6_SMBCF, SIOCFB, and its logical device (LDN=08h) configuration registers Define ETC (Enhanced Thermal Control) behavior Change DC spec of GPIOE10-13 Add IN_{TS2} buffer type Correct $\overline{LPCPD}$ timing Correct LPC t_{VAL} Rename the following functions: GPO24 to GPO41, GPIOE25 to GPIOE24, GPIOE26 to GPIOE25, GPIOE27 to GPIOE26 Change in GPCFG2 register Correct memory map support for SWC Typos and clarifications
June 22, 2003	Draft Revision 0.5	Rename Port Angeles 3 to PC87374L Rename 3V_DDCSCL, 3V_DDCSDA to CC_DDCSCL, CC_DDCSDA Support 2.5V SMBus on CC_DDCS*nn* pins Update Clock Domains Section, changes in CLOCKCF register, High-Frequency Clock Timing, Low-Frequency Clock Timing SIOCFB register is changed to be powered by V_{BAT} Register 61h for LDN=08h: H6_LPC_EMUL is changed Hecteta6 Emulation: changed Table 62, changed Tachometer Reading registers Changed FMC Registers: FT_CTL, FT_LOW, FT_HYST and FT_RNG Change SOUT2 buffer type to $O_{4/8}$ Added XOR Tree delay Update AC spec: V_{SB} Power-Up reset, V_{DD} Power-Up reset, Main Power Good, Resume Reset, $\overline{PS\_ON}$ Add Power Consumption numbers Add SMBus timing, InfraRed Port timing Typos and clarifications
August 2, 2003	Draft Revision 0.6	Remove HMC and FMC modules Remove SCK_BJT_GATE, $\overline{LPCPD}$, GPIOE15, GPIOE26-20, GPIO37-30, GPO41-40 signals Pins 52, 102, 123 are NC (Not Connected) Allow multiple pin locations for GPIO signals and rename pins with GPIOs, change default PU/PD, allow routing of a GPIOE input to a GPIO output Removed SIOCFB register SIOCF4[2:1], CLOCKCF[0] are reserved, change in SIOCF3[1:0], SIOCF4[5:3] Change drive capability of GPIOE00 (on pin 118) and GPIOE07 (on pin 128) Change PWRGD_3V functionality Rename PC87374L to PC8374L Rename Heceta 6 Emulation to Health Management H6_SCL and H6_SDA pins renamed to HMSCL and HMSDA pins, respectively V_{BAT} pin should be connected to V_{SB3} (and not V_{SS}), when battery backup features are unused LED mode selection is not dependent on V_{BAT} existence Typos and clarifications

Revision Record (Continued)

Revision Date	Status	Comments
August 12, 2003	Draft Revision 0.7	Change PWRGD_3V functionality Add details to SERIAL PORT 2 (SP2) WITH INFRARED Section Change in HMSMBCF register Typos and clarifications Health Management: Added support for more LMxx devices - see overview Section 9.2.2 - added a table of temp channel association. New HM registers: Status Register 3-4, Monitoring Control, Extended FANPWM Control 1-2, Tachometer Monitoring Control, Channels Vdd configuration, Temp Critical Limit Zone1-3,Temp Zone1-3 Gain and Offset Correction. New HM LPC registers:HMINT_STS3, HMINT_EN#, HMSENS_STS3, HMS_EN1-3, SMI/SCI_ROUT. Functional description updated. Temp Reading registers updated.
October 13, 2003	Draft Revision 0.8	Maximum PWM duty cycle, Fans setting time to the maximum duty cycle, Changed default mode of LED control Correct Table 3 on page 18 Rename LMxx sensor device Removed FPRST Changed reset value of FANTACH registers to FF Changed reset value of FANOFF to 1 Added Package Thermal Information Typos and clarifications
November 20, 2003	Preliminary Revision 0.9	• Changes to the Health Management Chapter • Device Characteristics: Minimum value of t_{CH}, t_{CL} reduced to 20 ns • Typos and Clarifications
February 3, 2004	Preliminary Revision 1.0	• Added LM sensor devices • Changed V_{BAT} external capacitor requirement to 1 µF • Typos and Clarifications
May 2004	Preliminary Revision 1.1	• Glue Functions: Removed 2.5V voltage divider circuit for SM-Bus Voltage Translation system diagram • Typos and Clarifications

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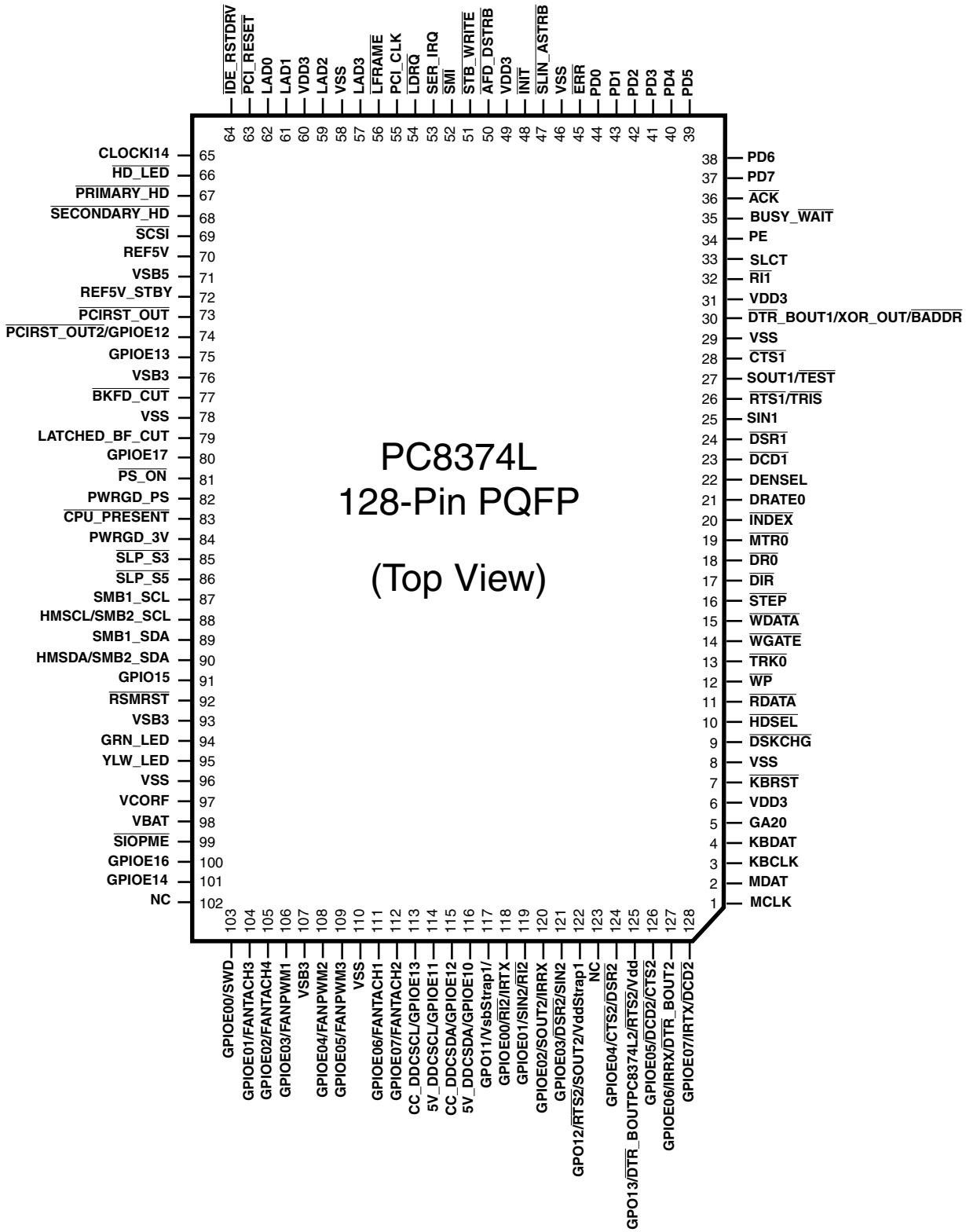
1.0 Signal/Pin Connection and Description

1.1 CONNECTION DIAGRAM



Plastic Quad Flatpack (PQFP), JEDEC

Order Number PC8374L0xxx/VLA

Package Number VLA128A

Note: 'xxx' stands for the following Keyboard Controller Microcodes:
IBW - for AMI IBU - for Intel
IBM - for IBM ICG - for Dell
ICK - for Phoenix

1.0 Signal/Pin Connection and Description (Continued)

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	MCLK	33	SLCT	65	CLOCKI14	97	V_{CORF}
2	MDAT	34	PE	66	$\overline{HD\_LED}$	98	V_{BAT}
3	KBCLK	35	BUSY_$\overline{WAIT}$	67	$\overline{PRIMARY\_HD}$	99	$\overline{SIOPME}$
4	KBDAT	36	$\overline{ACK}$	68	$\overline{SECONDARY\_HD}$	100	GPIOE16
5	GA20	37	PD7	69	$\overline{SCSI}$	101	GPIOE14
6	V_{DD3}	38	PD6	70	REF5V	102	NC
7	$\overline{KBRST}$	39	PD5	71	V_{SB5}	103	GPIOE00/SWD
8	V_{SS}	40	PD4	72	REF5V_STBY	104	GPIOE01/FANTACH3
9	$\overline{DSKCHG}$	41	PD3	73	$\overline{PCIRST\_OUT}$	105	FANTACH4/GPIOE02
10	$\overline{HDSEL}$	42	PD2	74	$\overline{PCIRST\_OUT2}$/GPIOE12	106	GPIOE03/FANPWM1
11	$\overline{RDATA}$	43	PD1	75	GPIOE13	107	V_{SB3}
12	$\overline{WP}$	44	PD0	76	V_{SB3}	108	GPIOE04/FANPWM2
13	$\overline{TRK0}$	45	$\overline{ERR}$	77	$\overline{BKFD\_CUT}$	109	GPIOE05/FANPWM3
14	$\overline{WGATE}$	46	V_{SS}	78	V_{SS}	110	V_{SS}
15	$\overline{WDATA}$	47	$\overline{SLIN\_ASTRB}$	79	LATCHED_BF_CUT	111	GPIOE06/FANTACH1
16	$\overline{STEP}$	48	$\overline{INIT}$	80	GPIOE17	112	GPIOE07/FANTACH2
17	$\overline{DIR}$	49	V_{DD3}	81	$\overline{PS\_ON}$	113	CC_DDCSCL/GPIOE13
18	$\overline{DR0}$	50	$\overline{AFD\_DSTRB}$	82	PWRGD_PS	114	5V_DDCSCL/GPIOE11
19	$\overline{MTR0}$	51	$\overline{STB\_WRITE}$	83	$\overline{CPU\_PRESENT}$	115	CC_DDCSDA/GPIOE12
20	$\overline{INDEX}$	52	$\overline{SMI}$	84	PWRGD_3V	116	5V_DDCSDA/GPIOE10
21	DRATE0	53	SER_IRQ	85	$\overline{SLP\_S3}$	117	GPO11/VsbStrap1
22	DENSEL	54	$\overline{LDRQ}$	86	$\overline{SLP\_S5}$	118	GPIOE00/$\overline{RI2}$/IRTX
23	$\overline{DCD1}$	55	PCI_CLK	87	SMB1_SCL	119	GPIOE01/SIN2/$\overline{RI2}$
24	$\overline{DSR1}$	56	$\overline{LFRAME}$	88	SMB2_SCL/HMSCL	120	GPIOE02/SOUT2/IRRX
25	SIN1	57	LAD3	89	SMB1_SDA	121	GPIOE03/$\overline{DSR2}$/SIN2
26	$\overline{RTS1}$/$\overline{TRIS}$	58	V_{SS}	90	SMB2_SDA/HMSDA	122	GPO12/$\overline{RTS2}$/SOUT2/ VddStrap1
27	SOUT1/$\overline{TEST}$	59	LAD2	91	GPIO15	123	NC
28	$\overline{CTS1}$	60	V_{DD3}	92	$\overline{RSMRST}$	124	GPIOE04/$\overline{CTS2}$/$\overline{DSR2}$
29	V_{SS}	61	LAD1	93	V_{SB3}	125	GPO13/$\overline{DTR}$_BOUT2/ $\overline{RTS2}$/VddStrap2
30	$\overline{DTR}$_BOUT1/$\overline{BADDR}$/ XOR_OUT	62	LAD0	94	GRN_LED	126	GPIOE05/$\overline{DCD2}$/$\overline{CTS2}$
31	V_{DD3}	63	$\overline{PCI\_RESET}$	95	YLW_LED	127	GPIOE06/IRRX/ $\overline{DTR}$_BOUT2
32	$\overline{RI1}$	64	$\overline{IDE\_RSTDRV}$	96	V_{SS}	128	GPIOE07/IRTX/$\overline{DCD2}$

1.0 Signal/Pin Connection and Description (Continued)

1.2 BUFFER TYPES AND SIGNAL/PIN DIRECTORY

The signal DC characteristics of the pins described in Section 1.4 on page 21 are denoted by buffer type symbols, which are defined in Table 1 and described in further detail in Section 10.2 on page 213.

Table 1. Buffer Types

Symbol	Description
IN_T	Input, TTL compatible
IN_{TS}	Input, TTL compatible, with 250 mV Schmitt Trigger
IN_{TS2}	Input, TTL compatible, with 200 mV Schmitt Trigger
IN_{TS4}	Input, TTL compatible, with 400 mV Schmitt Trigger
IN_{PCI}	Input, PCI 3.3V compatible
IN_{SM}	Input, SMBus compatible
IN_{ULR}	Input, power, resistor protected (not characterized)
AI	Input, analog (0-5.5V tolerant)
$O_{p/n}$	Output, TTL/CMOS compatible, push-pull buffer capable of sourcing *p* mA and sinking *n* mA
OD_n	Output, TTL/CMOS compatible, open-drain buffer capable of sinking *n* mA
O_{PCI}	Output, PCI 3.3V compatible,
AO	Output, analog (0-5.5V tolerant)
SW_{SM}	Input/Output switch, SMBus compatible
PWR	Power pin
GND	Ground pin

1.3 PIN MULTIPLEXING

Table 2 shows only multiplexed pins, their associated functional blocks and the configuration bits for the selection of the multiplexed options used in the PC8374L.

Table 2. Pin Multiplexing Configuration

Pin	Default Signal	Function Block	Alternate Signal	Function Block	Alternate Signal	Function Block	Configuration Select	Strap or Wake-Up	Function Block
26	$\overline{\text{RTS1}}$	Serial Port 1						$\overline{\text{TRIS}}$	Config (Straps)
27	SOUT1							$\overline{\text{TEST}}$	
30	$\overline{\text{DTR}}$_BOUT1		XOR_OUT	Config			$\overline{\text{TEST}}$ (strap)	$\overline{\text{BADDR}}$	
74	$\overline{\text{PCIRST\_OUT2}}$	Glue	GPIOE12	GPIO			SIOCF4.nPCIRSTO2	GPIOE12	SWC
75	GPIOE13	GPIO						GPIOE13	
103	SWD	HM	GPIOE00	GPIO			SIOCF4.nSWD	GPIOE00	SWC
104	GPIOE01	GPIO	FANTACH3	HM			SIOCF2.TACH3EN	GPIOE01	SWC
105	GPIOE02		FANTACH4				SIOCF2.TACH4EN	GPIOE02	
106	GPIOE03		FANPWM1				SIOCF3.PWM1EN	GPIOE03	
108	GPIOE04		FANPWM2				SIOCF3.PWM2EN	GPIOE04	
109	GPIOE05		FANPWM3				SIOCF3.PWM3EN	GPIOE05	
111	GPIOE06		FANTACH1				SIOCF2.TACH1EN	GPIOE06	
112	GPIOE07		FANTACH2				SIOCF2.TACH2EN	GPIOE07	
113	CC_DDCSCL	Glue	GPIOE13	GPIO			SIOCF2.GPIO03EN	GPIOE13	
114	5V_DDCSCL		GPIOE11					GPIOE11	
115	CC_DDCSDA		GPIOE12					GPIOE12	
116	5V_DDCSDA		GPIOE10					GPIOE10	
117	GPO11	GPIO						VsbStrap1[1]	Strap

Table 2. Pin Multiplexing Configuration (Continued)

Pin	Default Signal	Function Block	Alternate Signal	Function Block	Alternate Signal	Function Block	Configuration Select	Strap or Wake-Up	Function Block
118	GPIOE00	GPIO	$\overline{RI2}$	Serial Port 2	IRTX	InfraRed	SIOCF3.373COMP AND SIOCF3.SP2EN AND SIOCF3.IREN	$\overline{RI2}$	SWC
119	GPIOE01		SIN2		$\overline{RI2}$	Serial Port 2	SIOCF3.373COMP AND SIOCF3.SP2EN	$\overline{RI2}$	
120	GPIOE02		SOUT2		IRRX	InfraRed	SIOCF3.373COMP AND SIOCF3.SP2EN AND SIOCF3.IREN		
121	GPIOE03		$\overline{DSR2}$		SIN2	Serial Port 2	SIOCF3.373COMP AND SIOCF3.SP2EN		
122	GPO12		$\overline{RTS2}$		SOUT2			VddStrap1[2]	Config (Straps)
124	GPIOE04		$\overline{CTS2}$		$\overline{DSR2}$				
125	GPO13		$\overline{DTR}$_BOUT2		$\overline{RTS2}$			VddStrap2	Config (Straps)
126	GPIOE05		$\overline{DCD2}$		$\overline{CTS2}$				
127	GPIOE06		IRRX	InfraRed	$\overline{DTR}$_BOUT 2		SIOCF3.373COMP AND SIOCF3.SP2EN AND SIOCF3.IREN		
128	GPIOE07		IRTX		$\overline{DCD2}$				

1. V_{SB} strap input. Reserved for National use.
2. V_{DD} strap input. Reserved for National use.

1.0 Signal/Pin Connection and Description (Continued)

The following table shows the selection of GPIOs on their respective pins:

Table 3. GPIO Selection on Pins

GPIO	Configuration Bits					Selected On Pin	Comments
GPIOE00	SIOCF4.7	SIOCF3.0	SIOCF3.1	SIOCF3.2			
	0	X	0	0		118	Default
	0		1			None	
	1		0			Undefined	
	1		1			103	
	0	0	X	1		118	
	0	1				None	
	1	0				Undefined	
	1	1				103	
GPIOE01	SIOCF2.1	SIOCF3.1					
	0	0				104	Default
	0	1				104	
	1	0				119	
	1	1				None	
GPIOE02	SIOCF4.6	SIOCF2.2	SIOCF3.0	SIOCF3.1	SIOCF3.2		
	0	X	X	0	0	120	Default
	0	X		1		None	
	1	0		0		105	
	1	0		1		105	
	1	1		0		120	
	1	1		1		None	
	0	X	0	X	1	120	
	0	X	1			None	
	1	0	0			105	
	1	0	1			105	
	1	1	0			120	
	1	1	1			None	
GPIOE03	SIOCF3.5	SIOCF3.1					
	0	0				106	Default
	0	1				106	
	1	0				121	
	1	1				None	

1.0 Signal/Pin Connection and Description (Continued)

Table 3. GPIO Selection on Pins (Continued)

GPIO	Configuration Bits					Selected On Pin	Comments
GPIOE04	SIOCF3.6	SIOCF3.1					
	0	0				108	Default
	0	1				108	
	1	0				124	
	1	1				None	
GPIOE05	SIOCF3.7	SIOCF3.1					
	0	0				109	Default
	0	1				109	
	1	0				126	
	1	1				None	
GPIOE06	SIOCF2.4	SIOCF3.0	SIOCF3.1	SIOCF3.2			
	0	0	X	0		111	Default
	0	1				111	
	1	0				127	
	1	1				None	
	0	X	0	1		111	
	0		1			111	
	1		0			127	
	1		1			None	
GPIOE07	SIOCF2.5	SIOCF3.0	SIOCF3.1	SIOCF3.2			
	0	0	X	0		112	Default
	0	1				112	
	1	0				128	
	1	1				None	
	0	X	0	1		112	
	0		1			112	
	1		0			128	
	1		1			None	
GPIOE10	SIOCF3.4	SIOCF2.0					
	0	0				None	Default
		1				116	
	1	X				None	
GPIOE11, GPO11	SIOCF2.0						
	0					117	Default
	1					114	

1.0 Signal/Pin Connection and Description (Continued)

Table 3. GPIO Selection on Pins (Continued)

GPIO	Configuration Bits				Selected On Pin	Comments
GPIOE12, GPO12	SIOCF2.0	SIOCF3.1	SIOCF4.4			
	0	0	0		122	Default
	0	X	1		74	
	0	1	0		None	
	1	X	0		115	
	1	X	1		Undefined	
GPIOE13, GPO13	SIOCF2.0	SIOCF3.1	SIOCF4.3			
	0	X	0		75	Default
	0	0	1		125	
	0	1	1		None	
	1	X	X		113	

1.0 Signal/Pin Connection and Description (Continued)

1.4 DETAILED SIGNAL/PIN DESCRIPTIONS

This section describes all signals of the PC8374L device. The signals are organized by functional group.

1.4.1 LPC Interface

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
LAD3-0	57, 59, 61-62	I/O	IN_{PCI}/O_{PCI}	V_{DD3}	**LPC Address-Data.** Multiplexed command, address bi-directional data and cycle status.
PCI_CLK	55	I	IN_{PCI}	V_{DD3}	**LPC Clock.** PCI clock used for the LPC bus (up to 33 MHz).
$\overline{\text{LFRAME}}$	56	I	IN_{PCI}	V_{DD3}	**LPC Frame.** Low pulse indicates the beginning of a new LPC cycle or termination of a broken cycle.
$\overline{\text{LDRQ}}$	54	O	O_{PCI}	V_{DD3}	**LPC DMA Request.** Encoded DMA request for LPC interface.
$\overline{\text{PCI\_RESET}}$	63	I	IN_{PCI}	V_{DD3}	**LPC Reset.** PCI system reset used for the LPC bus (Hardware Reset).
SER_IRQ	53	I/O	IN_{PCI}/O_{PCI}	V_{DD3}	**Serial IRQ.** The interrupt requests are serialized over a single pin, where each IRQ level is delivered during a designated time slot.
$\overline{\text{SMI}}$	52	O	OD_6	V_{DD3}	**System Management Interrupt.** Active (low) level indicates that an SMI occurred. External pull-up resistor to V_{DD3} is required.

1.4.2 Serial Port 1 and Serial Port 2 (UART1 and UART2)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{\text{CTS1}}$	28	I	IN_{TS}	V_{DD3}	**Clear to Send.** When low, indicates that the modem or other data transfer device is ready to exchange data.
$\overline{\text{CTS2}}$	124 or 126	I	IN_{TS}	V_{DD3}	
$\overline{\text{DCD1}}$	23	I	IN_{TS}	V_{DD3}	**Data Carrier Detected.** When low, indicates that the modem or other data transfer device has detected the data carrier.
$\overline{\text{DCD2}}$	126 or 128	I	IN_{TS}	V_{DD3}	
$\overline{\text{DSR1}}$	24	I	IN_{TS}	V_{DD3}	**Data Set Ready.** When low, indicates that the data transfer device, e.g., modem, is ready to establish a communications link.
$\overline{\text{DSR2}}$	121 or 124	I	IN_{TS}	V_{DD3}	
$\overline{\text{DTR}}$_BOUT1	30	O	$O_{4/8}$	V_{DD3}	**Data Terminal Ready.** When low, indicates to the modem or other data transfer device that the corresponding UART is ready to establish a communications link. After a system reset, these pins provide the $\overline{\text{DTR}}$ function and set these signals to inactive high. **Baud Output.** Provides the associated serial channel baud rate generator output signal if test mode is selected, i.e., bit 7 of EXCR1 register is set.
$\overline{\text{DTR}}$_BOUT2	125 or 127	O	$O_{4/8}$	V_{DD3}	
$\overline{\text{RI1}}$	32	I	IN_{TS}	V_{DD3}	**Ring Indicator.** When low, indicates that a telephone ring signal was received by the modem. These pins are monitored during V_{DD} power-off for wake-up event detection.
$\overline{\text{RI2}}$	118 or 119	I	IN_{TS}	V_{DD3}	
$\overline{\text{RTS1}}$	26	O	$O_{4/8}$	V_{DD3}	**Request to Send.** When low, indicates to the modem or other data transfer device that the corresponding UART device is ready to exchange data. A system reset sets these signals to inactive high.
$\overline{\text{RTS2}}$	122 or 125	O	$O_{4/8}$	V_{DD3}	
SIN1	25	I	IN_{TS}	V_{DD3}	**Serial Input.** Receives composite serial data from the communications link (peripheral device, modem or other data transfer device).
SIN2	119 or 121	I	IN_{TS}	V_{DD3}	

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
SOUT1	27	O	$O_{4/8}$	V_{DD3}	**Serial Output.** Sends composite serial data to the communications link (peripheral device, modem or other data transfer device). These signals are set active high after a system reset.
SOUT2	120 or 122	O	$O_{4/8}$	V_{DD3}	

1.4.3 InfraRed Port

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
IRRX	127 or 120	I	IN_{TS}	V_{DD3}	**InfraRed Receive.** InfraRed serial input data.
IRTX	128 or 118	O	$O_{6/12}$	V_{DD3}	**InfraRed Transmit.** InfraRed serial output data.

1.4.4 Parallel Port

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{ACK}$	36	I	IN_T	V_{DD3}	**Acknowledge.** Pulsed low by the printer to indicate that it has received data from the parallel port.
$\overline{AFD\_DSTRB}$	50	O	OD_{14}, $O_{14/14}$	V_{DD3}	**$\overline{AFD}$ - Automatic Feed.** When low, instructs the printer to automatically feed a line after printing each line. This pin is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **$\overline{DSTRB}$ - Data Strobe (EPP).** Active low; used in EPP mode to denote a data cycle. When the cycle is aborted, $\overline{DSTRB}$ becomes inactive (high).
BUSY_$\overline{WAIT}$	35	I	IN_T	V_{DD3}	**Busy.** Set high by the printer when it cannot accept another character. **Wait.** In EPP mode, the parallel port device uses this active low signal to extend its access cycle.
$\overline{ERR}$	45	I	IN_T	V_{DD3}	**Error.** Set active low by the printer when it detects an error.
$\overline{INIT}$	48	O	OD_{14}, $O_{14/14}$	V_{DD3}	**Initialize.** When low, initializes the printer. This signal is in TRI-STATE after a 1 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin.
PD7-0	37-44	I/O	$IN_T/O_{14/14}$	V_{DD3}	**Parallel Port Data.** Transfers data to and from the peripheral data bus and the appropriate parallel port data register. These signals have a high current drive capability.
PE	34	I	IN_T	V_{DD3}	**Paper End.** Set high by the printer when it is out of paper. This pin has an internal weak pull-up or pull-down resistor.
SLCT	33	I	IN_T	V_{DD3}	**Select.** Set active high by the printer when the printer is selected.
$\overline{SLIN\_ASTRB}$	47	O	OD_{14}, $O_{14/14}$	V_{DD3}	**$\overline{SLIN}$ - Select Input.** When low, selects the printer. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **$\overline{ASTRB}$ - Address Strobe (EPP).** Active low, used in EPP mode to denote an address cycle. When the cycle is aborted, $\overline{ASTRB}$ becomes inactive (high).

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{\text{STB\_WRITE}}$	51	O	OD_{14}, $O_{14/14}$	V_{DD3}	**$\overline{\text{STB}}$ - Data Strobe.** When low, Indicates to the printer that valid data is available at the printer port. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **$\overline{\text{WRITE}}$ - Write Strobe.** Active low, used in EPP mode to denote an address or data write cycle. When the cycle is aborted, $\overline{\text{WRITE}}$ becomes inactive (high).

1.4.5 Floppy Disk Controller (FDC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
DENSEL	22	O	OD_{12} $O_{6/12}$	V_{DD3}	**Density Select.** Indicates that a high FDC density data rate (500 Kbps, 1 Mbps or 2 Mbps) or a low density data rate (250 or 300 Kbps) is selected.
$\overline{\text{DIR}}$	17	O	OD_{12} $O_{6/12}$	V_{DD3}	**Direction.** Determines the direction of the Floppy Disk Drive (FDD) head movement (active = step in; inactive = step out) during a seek operation.
$\overline{\text{DR0}}$	18	O	OD_{12} $O_{6/12}$	V_{DD3}	**Drive Select.** Active low signal controlled by bit 0 of the Digital Output Register (DOR).
DRATE0	21	O	OD_{12} $O_{6/12}$	V_{DD3}	**Data Rate.** Reflects the value of bit 0 of either Configuration Control Register (CCR) or Data Rate Select Register (DSR), whichever was written to last.
$\overline{\text{DSKCHG}}$	9	I	IN_{TS}	V_{DD3}	**Disk Change.** Indicates that the drive door was opened.
$\overline{\text{HDSEL}}$	10	O	OD_{12} $O_{6/12}$	V_{DD3}	**Head Select.** Selects which side of the FDD is accessed. Active (low) selects side 1; inactive selects side 0.
$\overline{\text{INDEX}}$	20	I	IN_{TS}	V_{DD3}	**Index.** Indicates the beginning of an FDD track.
$\overline{\text{MTR0}}$	19	O	OD_{12} $O_{6/12}$	V_{DD3}	**Motor Select.** Active low motor enable signal for drive 0, controlled by bit D4 of the Digital Output Register (DOR).
$\overline{\text{RDATA}}$	11	I	IN_{TS}	V_{DD3}	**Read Data.** Raw serial input data stream read from the FDD.
$\overline{\text{STEP}}$	16	O	OD_{12} $O_{6/12}$	V_{DD3}	**Step.** Issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
$\overline{\text{TRK0}}$	13	I	IN_{TS}	V_{DD3}	**Track 0.** Indicates to the controller that the head of the selected floppy disk drive is at track 0.
$\overline{\text{WDATA}}$	15	O	OD_{12} $O_{6/12}$	V_{DD3}	**Write Data.** Carries out the pre-compensated serial data that is written to the FDD. Pre-compensation is software selectable.
$\overline{\text{WGATE}}$	14	O	OD_{12} $O_{6/12}$	V_{DD3}	**Write Gate.** Enables the write circuitry of the selected FDD. $\overline{\text{WGATE}}$ is designed to prevent glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
$\overline{\text{WP}}$	12	I	IN_{TS}	V_{DD3}	**Write Protected.** Indicates that the disk in the selected drive is write protected.

1.0 Signal/Pin Connection and Description (Continued)

1.4.6 Keyboard and Mouse Controller (KBC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
KBCLK	3	I/O	IN_{TS}/OD_{14}	V_{DD3}	**Keyboard Clock.** Keyboard clock signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD3} power-off for wake-up event detection.
KBDAT	4	I/O	IN_{TS}/OD_{14}	V_{DD3}	**Keyboard Data.** Keyboard data signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD3} power-off for wake-up event detection.
MCLK	1	I/O	IN_{TS}/OD_{14}	V_{DD3}	**Mouse Clock.** Mouse clock signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD3} power-off for wake-up event detection.
MDAT	2	I/O	IN_{TS}/OD_{14}	V_{DD3}	**Mouse Data.** Mouse data signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD3} power-off for wake-up event detection.
$\overline{KBRST}$	7	I/O	IN_T/OD_8, $O_{4/8}$	V_{DD3}	**KBD Reset.** Keyboard reset (P20) quasi-bidirectional output.
GA20	5	I/O	IN_T/OD_8, $O_{4/8}$	V_{DD3}	**Gate A20.** KBC gate A20 (P21) quasi-bidirectional output.

1.4.7 General-Purpose I/O (GPIO)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
GPIOE00	103	I/O	IN_{TS}/ OD_8, $O_{4/8}$	V_{SB3}	**General-Purpose I/O Ports.** Each pin is configured independently as input or I/O, with or without static pull-up (and some also with or without static pull-down) and with either open-drain or push-pull output type. These pins have event detection capability to generate a wake-up event or an interrupt. **Note:** If GPIOE12 is configured (on pin 74) make sure that the pin's default function does not interfere with the circuit connected to the GPIO. Failure to do so may result in irreversible damage to the chip.
	118		IN_{TS}/ OD_{12}, $O_{6/12}$	V_{DD3}	
GPIOE01-06	104-106, 108-109, 111		IN_{TS}/ OD_8, $O_{4/8}$	V_{SB3}	
	119-121, 124, 126-127			V_{DD3}	
GPIOE07	112		IN_{TS}/ OD_8, $O_{4/8}$	V_{SB3}	
	128		IN_{TS}/ OD_{12}, $O_{6/12}$	V_{DD3}	
GPIOE10-13	116, 114, 115, 113		IN_{TS2}/ OD_6, $O_{3/6}$	V_{SB3}	
GPIOE12-13	74-75		IN_{TS}/ OD_8, $O_{4/8}$		
GPIOE14, GPIOE16-17	101, 100, 80				
GPIO15	91		IN_{TS}/ OD_8, $O_{4/8}$		**General-Purpose I/O Port.** This pin is configured independently as input or I/O with or without static pull-up and with either open-drain or push-pull output type.
GPO11	117	O	OD_8, $O_{4/8}$		**General-Purpose Output Port.** This pin is configured independently as output, with or without static pull-up and with either open-drain or push-pull output type.
GPO12-13	122, 125			V_{DD3}	

1.0 Signal/Pin Connection and Description (Continued)

1.4.8 Health Management (HM)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
SWD	103	I/O	IN_{SM}/OD_6	V_{SB3}	**SensorPath Data.** Bidirectional, SensorPath Data interface signal to LMxx sensor device(s). An internal pull-up for this pin is optional.
HMSCL	88	I/O	IN_{SM}/OD_6	V_{SB3}	**Health Management SMBus Serial Clock.** Serial clock signal. External pull-up resistor is required.
HMSDA	90	I/O	IN_{SM}/OD_6	V_{SB3}	**Health Management SMBus Serial Data.** Serial data signal. External pull-up resistor is required.
FANTACH1-4	111-112, 104-105	I	IN_{TS}	V_{DD3}	**Fan Inputs.** Used to feed the fan's tachometer pulse to the Fan Speed Monitor.
FANPWM1-3	106, 108-109	O	OD_{12},$O_{6/12}$	V_{DD3}	**Fan Outputs.** Pulse Width Modulation (PWM) signals, used to control the speed of cooling fans by controlling the voltage supplied to the fan motors.

1.4.9 System Wake-Up Control (SWC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
GPIOE00-07	103-106, 108-109, 111-112	I	IN_{TS}	V_{SB3}	**Wake-Up Inputs.** Generates a wake-up event. These pins have programmable debouncing. When the pin is not used, the internal pull-up resistor must be enabled to allow the pin to be left not connected.
	118-121, 124, 126-128			V_{DD3}	
GPIOE10-13	116, 114, 115, 113		IN_{TS2}	V_{SB3}	
GPIOE12-13	74-75		IN_{TS}		
GPIOE14, GPIOE16-17	101, 100, 80				
$\overline{RI1}$ $\overline{RI2}$	32, 118 or 119	I	IN_{TS}	V_{SB3}	**Ring Indicator Wake-Up.** When low, generates a wake-up event, indicating that a telephone ring signal was received by the modem.
KBCLK	3	I	IN_{TS}	V_{SB3}	**Keyboard Clock Wake-Up.** Generates a wake-up event when a specific keyboard sequence is detected.
KBDAT	4	I	IN_{TS}	V_{SB3}	**Keyboard Data Wake-Up.** Generates a wake-up event when a specific keyboard sequence is detected.
MCLK	1	I	IN_{TS}	V_{SB3}	**Mouse Clock Wake-Up.** Generates a wake-up event when a specific mouse action is detected.
MDAT	2	I	IN_{TS}	V_{SB3}	**Mouse Data Wake-Up.** Generates a wake-up event when a specific mouse action is detected.
$\overline{SIOPME}$	99	O	OD_8, $O_{4/8}$	V_{SB3}	**Power Management Event (SCI).** Active level indicates that a wake-up event occurred, causing the system to exit its current sleep state. This signal has programmable polarity (default is active low).
$\overline{SLP\_S3}$, $\overline{SLP\_S5}$	85, 86	I	IN_{TS4}	V_{SB3}	**Sleep States 3 to 5.** Active (low) level indicates the system is in one of the sleep states S3 or S5. These signals are generated by an external ACPI controller.
YLW_LED, GRN_LED	95, 94	O	OD_{24}	V_{SB3}	**Power LEDs.** Yellow and green LED drivers. Each indicates the Main power status or blinks under software control.

1.0 Signal/Pin Connection and Description (Continued)

1.4.10 Clock

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
CLOCKI14	65	I	IN_{TS}	V_{DD3}	**High-Frequency Clock Input.** 14.31818 MHz clock for the on-chip, 48 MHz Clock Generator (for the Legacy modules).

1.4.11 Glue Functions

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
REF5V	70	O	AO	V_{SB3}	**Main Highest Active Supply, Reference Output.** Reference voltage equal to the highest voltage between V_{DD5} and V_{DD3}. External pull-up resistor to V_{DD5} is required.
REF5V_STBY	72	O	AO	V_{SB3}	**Standby Highest Active Supply, Reference Output.** Reference voltage equal to the highest voltage between V_{SB5} and V_{SB3}. External pull-up resistor to V_{SB5} is required.
$\overline{\text{PS\_ON}}$	81	O	OD_6	V_{SB3}	**Main Power Supply On/Off Control.** Active (low) level turns the main power supply (V_{DD}) on. External pull-up resistor to V_{SB5} is required.
PWRGD_PS	82	I	IN_{TS4}	V_{SB3}	**Power Good Signal from the Power Supply.** Active level indicates the Main power supply voltage is valid.
PWRGD_3V	84	O	$O_{3/6}$	V_{SB3}	**Power Good Output.** Active level indicates: Main supply voltage is valid and the system is in a higher than S3 sleep state.
$\overline{\text{CPU\_PRESENT}}$	83	I	IN_{TS4}	V_{SB3}	**CPU Present.** Active (low) level indicates a processor is currently plugged in.
$\overline{\text{BKFD\_CUT}}$	77	O	OD_6	V_{SB3}	**Backfeed-Cut Control.** Power distribution control (when switching between main and standby regulators) for system transition into and out of the S3 sleep state. External pull-up resistor to V_{SB5} is required.
LATCHED_BF_CUT	79	O	$O_{14/14}$	V_{SB3}	**Latched Backfeed-Cut.** Power distribution control (when switching between main and standby regulators) for system transition into and out of the S5 sleep state.
VSB5	71	I	AI	V_{SB3}	**Standby 5V Power Supply.** Used for Resume Reset generation (Range: 0-5.5V, Backdrive protected).
$\overline{\text{RSMRST}}$	92	O	$O_{3/6}$	V_{SB3}	**Resume Reset.** Power-Up reset signal based on the V_{SB5} supply voltage.
$\overline{\text{PRIMARY\_HD}}$	67	I	IN_{TS4}	V_{DD3}	**Primary Drive.** Active (low) level indicates that the primary IDE drive is active.
$\overline{\text{SECONDARY\_HD}}$	68	I	IN_{TS4}	V_{DD3}	**Secondary Drive.** Active (low) level indicates that the secondary IDE drive is active.
$\overline{\text{SCSI}}$	69	I	IN_{TS4}	V_{DD3}	**SCSI Drive.** Active (low) level indicates that the SCSI drive is active.
$\overline{\text{HD\_LED}}$	66	O	OD_{12}	V_{DD3}	**Hard Drive LED.** Red LED driver. When low, indicates that at least one drive is active.
CC_DDCSCL	113	I/O	SW_{SM}	V_{SB3}	**Chipset Cluster (2.5V or 3.3V) Level DDC Serial Clock.** SMBus serial clock signal with 2.5V or 3.3V logic levels for Data Display Channel (DDC) interface. External pull-up resistor to V_{DD3} or 2.5V is required.
5V_DDCSCL	114	I/O	SW_{SM}	V_{SB3}	**5V Level DDC Serial Clock.** SMBus serial clock signal with 5V logic levels for VGA monitor interface. External pull-up resistor to V_{DD5} is required.

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
CC_DDCSDA	115	I/O	SW_{SM}	V_{SB3}	**Chipset Cluster (2.5V or 3.3V) Level DDC Serial Data.** SMBus serial data signal with 2.5V or 3.3V logic levels for DDC interface. External pull-up resistor to V_{DD3} or 2.5V is required.
5V_DDCSDA	116	I/O	SW_{SM}	V_{SB3}	**5V Level DDC Serial Data.** SMBus serial data signal with 5V logic levels for VGA monitor interface. External pull-up resistor to V_{DD5} is required.
SMB1_SCL	87	I/O	SW_{SM}	V_{SB3}	**Bus 1 Serial Clock.** Serial clock signal of SMBus 1 (3.3V logic levels). External pull-up resistor to the 3.3V supply is required.
SMB2_SCL	88	I/O	SW_{SM}	V_{SB3}	**Bus 2 Serial Clock.** Serial clock signal of SMBus 2 (3.3V logic levels). External pull-up resistor to the 3.3V supply is required.
SMB1_SDA	89	I/O	SW_{SM}	V_{SB3}	**Bus 1 Serial Data.** Serial data signal of SMBus 1 (3.3V logic levels). External pull-up resistor to the 3.3V supply is required.
SMB2_SDA	90	I/O	SW_{SM}	V_{SB3}	**Bus 2 Serial Data.** Serial data signal of SMBus 2 (3.3V logic levels). External pull-up resistor to the 3.3V supply is required.
$\overline{\text{PCIRST\_OUT}}$	73	O	$O_{14/14}$	V_{SB3}	**PCI Reset Output.** PCI system reset. $\overline{\text{PCIRST\_OUT}}$ is a buffered copy of $\overline{\text{PCI\_RESET}}$ when V_{DD3} is on, and it is held at low level when V_{DD3} is off.
$\overline{\text{PCIRST\_OUT2}}$	74	O	$O_{14/14}$	V_{SB3}	**PCI Reset Output 2.** PCI system reset (same behavior as $\overline{\text{PCIRST\_OUT}}$ above).
$\overline{\text{IDE\_RSTDRV}}$	64	O	OD_6	V_{DD3}	**IDE Reset Output.** IDE drive reset. $\overline{\text{IDE\_RSTDRV}}$ is a buffered copy of $\overline{\text{PCI\_RESET}}$ when V_{DD3} is on, and it is floating when V_{DD3} is off.

1.0 Signal/Pin Connection and Description (Continued)

1.4.12 Configuration Straps and Testing

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{\text{BADDR}}$	30	I	IN_{TS}	V_{DD3}	**Base Address.** Sampled at V_{DD} Power-Up reset to determine the base address of the configuration Index-Data register pair, as follows: – No pull-down resistor (default) - 2Eh-2Fh – 10 KΩ[1] external pull-down resistor - 4Eh-4Fh The external pull-down resistor must be connected to V_{SS}.
VsbStrap1	117	I	IN_{TS}	V_{SB3}	**Vsb Strap 1.** Reserved strap input function for National use.
VddStrap1	122	I	IN_{TS}	V_{DD3}	**Vdd Strap 1.** Reserved strap input function for National use.
VddStrap2	125	I	IN_{TS}	V_{DD3}	**Vdd Strap 2.** General-Purpose strap input function.
$\overline{\text{TRIS}}$	26	I	IN_{TS}	V_{DD3}	**TRI-STATE Device.** Sampled at V_{DD} Power-Up reset to force the device to float all its output and I/O pins, as follows: – No pull-down resistor (default) - normal pin operation – 10 KΩ[1] external pull-down resistor - floating device pins The external pull-down resistor must be connected to V_{SS}. When $\overline{\text{TRIS}}$ is set to 0 (by an external pull-down resistor), $\overline{\text{TEST}}$ must be 1 (left unconnected).
$\overline{\text{TEST}}$	27	I	IN_{TS}	V_{DD3}	**XOR Tree Test Mode.** Sampled at V_{DD} Power-Up reset to force the device pins into a XOR tree configuration, as follows: – No pull-down resistor (default) - normal device operation – 10 KΩ[1] external pull-down resistor - pins configured as XOR tree. When $\overline{\text{TEST}}$ is set to 0 (by an external pull-down resistor), $\overline{\text{TRIS}}$ must be 1 (left unconnected).
XOR_OUT	30	O	$O_{4/8}$	V_{DD3}	**XOR Tree Output.** All the device pins (except not connected pins, power type and analog type pins) are internally connected in a XOR tree structure.

1. Because the strap function is multiplexed with the Serial Port pins, a CMOS transceiver device is recommended for Serial Port functionality; in this case, the value of the external pull-down resistor is 10 KΩ. If, however, a TTL transceiver device is used, the value of the external pull-down resistor must be 470Ω, and since the Serial Port pins are not able to drive this load, the external pull-down resistor must be disconnected t_{EPLV} after V_{DD3} power-up (see “VDD Power-Up Reset” on page 221).

1.4.13 Power and Ground

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
V_{SS}	8, 29, 46, 58, 78, 96, 110	I	GND		**Ground.** Ground connection for both core logic and I/O buffers, for the Main, Standby and Battery power supplies.
V_{DD3}	6, 31, 49, 60	I	PWR		**Main 3.3V Power Supply.** Powers the I/O buffers of the legacy peripherals and the LPC interface.
V_{SB3}	76, 93, 107	I	PWR		**Standby 3.3V Power Supply.** Powers the I/O buffers of the GPIO ports, SWC, Glue Functions, Health Management and the on-chip Core power converter.
V_{CORF}	97	I/O	PWR		**On-Chip Core Power Converter Filter.** On-chip Core power converter output. An external 1 µF ceramic filter capacitor must be connected between this pin and V_{SS}.

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
V_{BAT}	98	I	IN_{ULR}		**Battery Power Supply.** When V_{SB3} is off, this supply provides battery back-up to some of the SWC registers. When the functions powered by V_{BAT} are not used, the V_{BAT} pin must be connected to V_{SB3}. The pin is connected to the internal logic through a series resistor for UL-compliant protection.
V_{SB5}	71	I	PWR		**Standby 5V Power Supply.** Used for Resume Reset generation in the Glue Logic.

1.0 Signal/Pin Connection and Description (Continued)

1.5 INTERNAL PULL-UP AND PULL-DOWN RESISTORS

The signals listed in Table 4 have internal pull-up (PU) and/or pull-down (PD) resistors. The internal resistors are optional for those signals indicated as “Programmable”. See Section 10.3 on page 218 for the values of each resistor type.

Table 4. Internal Pull-Up and Pull-Down Resistors

Signal	Pin(s)	Power Well	Type	Comments
Health Management (HM)				
SWD	103	V_{SB}	PU_{1K25}	Programmable[1]
Parallel Port				
$\overline{ACK}$	36	V_{DD3}	PU_{220}	
$\overline{AFD\_DSTRB}$	50	V_{DD3}	PU_{440}	
BUSY_$\overline{WAIT}$	35	V_{DD3}	PD_{120}	
$\overline{ERR}$	45	V_{DD3}	PU_{220}	
$\overline{INIT}$	48	V_{DD3}	PU_{440}	
PE	34	V_{DD3}	PU_{220}/PD_{120}	Programmable
SLCT	33	V_{DD3}	PD_{120}	
$\overline{SLIN\_ASTRB}$	47	V_{DD3}	PU_{440}	
$\overline{STB\_WRITE}$	51	V_{DD3}	PU_{440}	
Keyboard and Mouse Controller (KBC)				
$\overline{KBRST}$	7	V_{DD3}	PU_{30}	
GA20	5	V_{DD3}	PU_{30}	
System Wake-Up Control (SWC)				
$\overline{SIOPME}$	99	V_{SB3}	PU_{30}	Programmable[2]
General-Purpose Input/Output (GPIO) Ports				
GPIOE00	103	V_{SB}	PU_{1K25}	Programmable[3]
	118	V_{DD3}	PU_{30}/PD_{30}	Programmable[4]
GPIOE01-06	104-106, 108-109, 111	V_{SB3}	PU_{30}	Programmable[1]
	119-121, 124, 126-127	V_{DD3}		
GPIOE07	112	V_{SB3}	PU_{30}	Programmable[5]
	128	V_{DD3}	PU_{30}/PD_{30}	Programmable[4]
GPIOE10-11	116, 114	V_{SB3}	PU_{30}	Programmable[6]
GPIOE12	115	V_{SB3}	PU_{30}	Programmable[6]
	74			
GPIOE13	113	V_{SB3}	PU_{30}	Programmable[6]
	75		PU_{90}	Programmable[1]
GPIOE14	101	V_{SB3}	PU_{30}/PD_{30}	Programmable[4]
GPIO15, GPIOE16	91, 100	V_{SB3}	PU_{30}	Programmable[5]
GPIOE17	80	V_{SB3}	PU_{30}	Programmable[1]

1.0 Signal/Pin Connection and Description (Continued)

Table 4. Internal Pull-Up and Pull-Down Resistors (Continued)

Signal	Pin(s)	Power Well	Type	Comments
GPO11	117	V_{SB3}	PU_{30}	Programmable[1]
GPO12-13	122, 125	V_{DD3}	PU_{30}	Programmable[1]
Glue Functions				
PWRGD_PS	82	V_{SB3}	PU_{90}	
$\overline{\text{CPU\_PRESENT}}$	83	V_{SB3}	PU_{90}	
$\overline{\text{PRIMARY\_HD}}$	67	V_{DD3}	PU_{90}	
$\overline{\text{SECONDARY\_HD}}$	68	V_{DD3}	PU_{90}	
$\overline{\text{SCSI}}$	69	V_{DD3}	PU_{90}	
Strap Configuration				
$\overline{\text{BADDR}}$	30	V_{DD3}	PU_{30}	Strap[7]
$\overline{\text{TRIS}}$	26	V_{DD3}	PU_{30}	Strap[7]
$\overline{\text{TEST}}$	27	V_{DD3}	PU_{30}	Strap[7]
VsbStrap1	117	V_{SB3}	PU_{30}	Strap[8]
VddStrap1	122	V_{DD3}	PU_{30}	Strap[7]
VddStrap2	125	V_{DD3}	PU_{30}	Strap[7]

1. Default at reset: enabled.
2. Enabled only when the OD_6 buffer type is selected (OD_6 is the default at reset).
3. Alternate function at reset: enabled.
4. Default at reset: PD enabled.
5. Default at reset: disabled.
6. Alternate function at reset: disabled.
7. Active only during V_{DD} Power-Up reset.
8. Active only during V_{SB} Power-Up reset.

2.0 Power, Reset and Clocks

2.1 POWER

2.1.1 Power Planes

The PC8374L device has four power planes (wells), as shown in the table below:

Table 5. Power Planes

Power Plane	Description	Power Pins	Ground Pins
Main	Powers the I/O buffers for the external signals[1] of the Legacy modules (Serial Ports, InfraRed Port, Parallel Port, FDC, KBC), on-chip High-Frequency Clock Generator and the LPC interface, including the buffered reset outputs	V_{DD3}	V_{SS}
Standby	Powers the I/O buffers for the external signals[1] of the GPIO ports, SWC, Health Management, Glue Functions and the on-chip Core power converter	V_{SB3}	V_{SS}
Core	Powers the internal (core) logic of all the device modules	V_{CORF}[2]	V_{SS}
Backup[3]	Powers some of the SWC functions and Health Management configuration	V_{BAT}	V_{SS}

1. See the tables in Section 1.4 (pages 21–28), specifically the *Power Well* column.
2. V_{CORF} is generated from V_{SB3} by an on-chip power converter.
3. Bits powered by V_{BAT} are functional when V_{SB3} is on, regardless of the state of V_{BAT} power. However, if V_{BAT} fails, the value of these bits remains valid only as long as V_{SB3} is on.

For correct operation, V_{SB3} must be applied before V_{DD3}.

The battery backup voltage (V_{BAT}) powers some of the SWC functions and Health Management configuration even when the V_{SB3} voltage is absent due to either power failure or disconnection of the external AC input power. When the functions powered by V_{BAT} are not used, the V_{BAT} pin must be connected to V_{SB3}.

To meet the UL standard requirements, a series resistor (R_{UL}) is implemented.

2.1.2 Power States

The PC8374L device has four power states:

- **Battery Fail** - Backup power plane is powered off (V_{BAT} is inactive). This power state applies only to the SWC functions and Health Management configuration powered by V_{BAT}.
- **Power Fail** - Main, Standby and Core power planes are powered off (V_{DD3}, V_{SB3} and V_{CORF} are inactive).
- **Power Off** - Main power plane is powered off; the Standby and Core power planes are on (V_{DD3} is inactive; V_{SB3} and V_{CORF} are active).
- **Power On** - Main, Standby and Core power planes are powered on (V_{DD3}, V_{SB3} and V_{CORF} are active).

The following power state is illegal:

- The Main power plane is powered on and the Standby and Core power planes are off (i.e., V_{DD3} is active; V_{SB} and V_{CORF} are inactive). Operation is not guaranteed; however, at power-on/off, the device may temporarily enter this power state due to the different rise/fall times of the V_{DD3} and V_{SB3} power supplies.

Table 6 summarizes the power states described above.

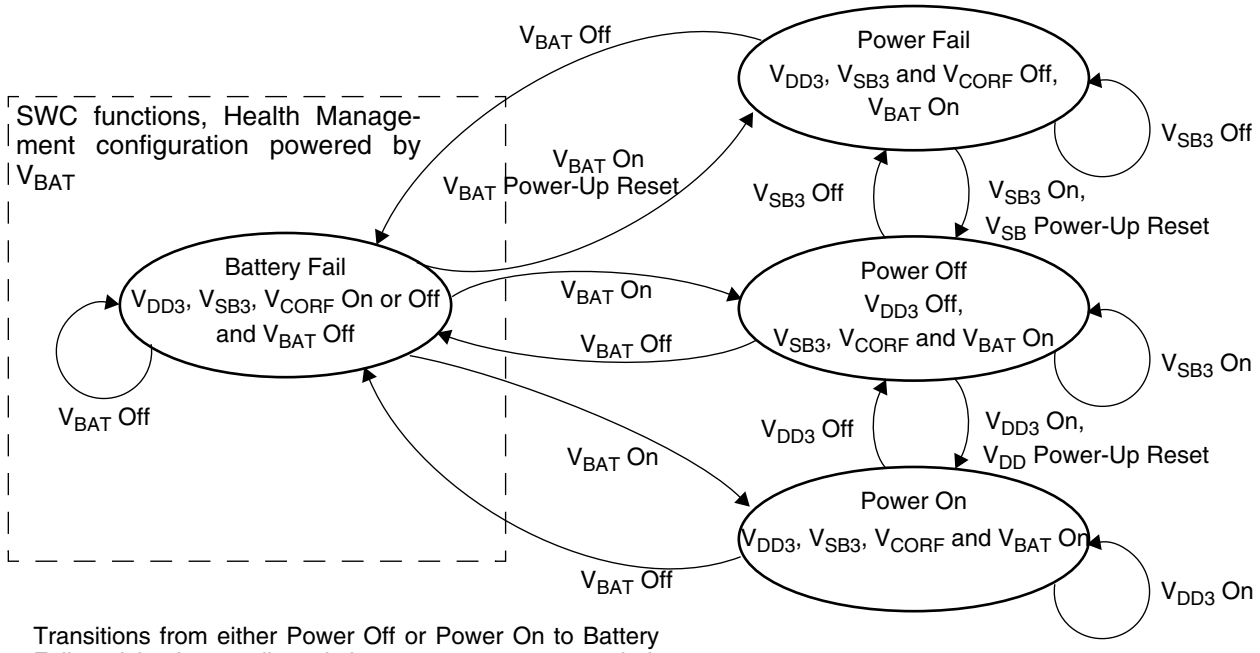
2.0 Power, Reset and Clocks (Continued)

Table 6. Power States and Related Power Planes

Power State	Main (V_{DD3})	Standby (V_{SB3})	Core (V_{CORF})[1]	V_{BAT}
Battery Fail[2]	On or Off	On or Off	On or Off	Off
Power Fail	Off	Off	Off	On or Off
Power Off	Off	On	On	On or Off
Power On	On	On	On	On or Off
Illegal[3]	On	Off	Off	On or Off

1. V_{CORF} is generated from V_{SB3}; therefore, both voltages are on or off at approximately the same time.
2. This power state applies only to the SWC functions and Health Management configuration powered by V_{BAT}.
3. Operation is not guaranteed and register data may be corrupted. However, at power-on/off, the device may temporarily enter this power state due to the different rise/fall times of the V_{DD3} and V_{SB3} power supplies.

Figure 1 shows the power state transitions:



Transitions from either Power Off or Power On to Battery Fail and back are allowed, however not recommended, since they cause data loss in the V_{BAT}-powered registers, after V_{SB3} is turned off (Power Fail).

Figure 1. Power State Transitions

2.1.3 Power Connection and Layout Guidelines

The PC8374L requires a power supply voltage of 3.3V ± 10% for both the V_{DD3} and V_{SB3} supplies. The on-chip Core power converter generates a voltage below 3V for the internal logic. The device is designed to operate with a Lithium backup battery supplying up to 3.6V. Therefore, it includes an internal current-limiting resistor on the V_{BAT} input to prevent the battery from shorting, as required by the UL regulations. If the system implementation does not require backup power for the PC8374L device, the V_{BAT} pin must be connected to V_{SB3}.

V_{DD3}, V_{SB3}, V_{CORF} and V_{BAT} use a common ground return marked V_{SS}.

To obtain the best performance, bear in mind the following recommendations.

2.0 Power, Reset and Clocks (Continued)

Ground Connection. The following items must be connected to the ground layer (V_{SS}) as close to the device as possible:

- The ground return (V_{SS}) pins
- The decoupling capacitors of the Main power supply (V_{DD3}) pins
- The decoupling capacitors of the Standby power supply (V_{SB3}) pins
- The decoupling capacitor of the Standby 5V supply (V_{SB5}) pin
- The decoupling capacitor of the on-chip Core power converter (V_{CORF}) pin
- The decoupling capacitor of the Backup battery (V_{BAT}) pin

Note that a low-impedance ground layer also improves noise isolation.

Decoupling Capacitors. The following decoupling capacitors must be used in order to reduce EMI and ground bounce:

- Main power supply (V_{DD3}): Place one capacitor of 0.1 µF on each V_{DD3}-V_{SS} pin pair as close to the pin as possible. In addition, place one 10–47 µF tantalum capacitor on the common net as close to the chip as possible.
- Standby power supply (V_{SB3}): Place one capacitor of 0.1 µF on each V_{SB3}-V_{SS} pin pair as close to the pin as possible. In addition, place one 10–47 µF tantalum capacitor on the common net as close to the chip as possible.
- Standby 5V supply (V_{SB5}): Place one capacitor of 0.1 µF on the V_{SB5}-V_{SS} pin pair as close to the pin as possible.
- On-chip Core power converter (V_{CORF}): Place one 1 µF ceramic capacitor on the V_{CORF}-V_{SS} pin pair as close to the pin as possible.
- Backup battery (V_{BAT}): Place one capacitor of 0.1 µF on the V_{BAT} pin as close to the pin as possible.

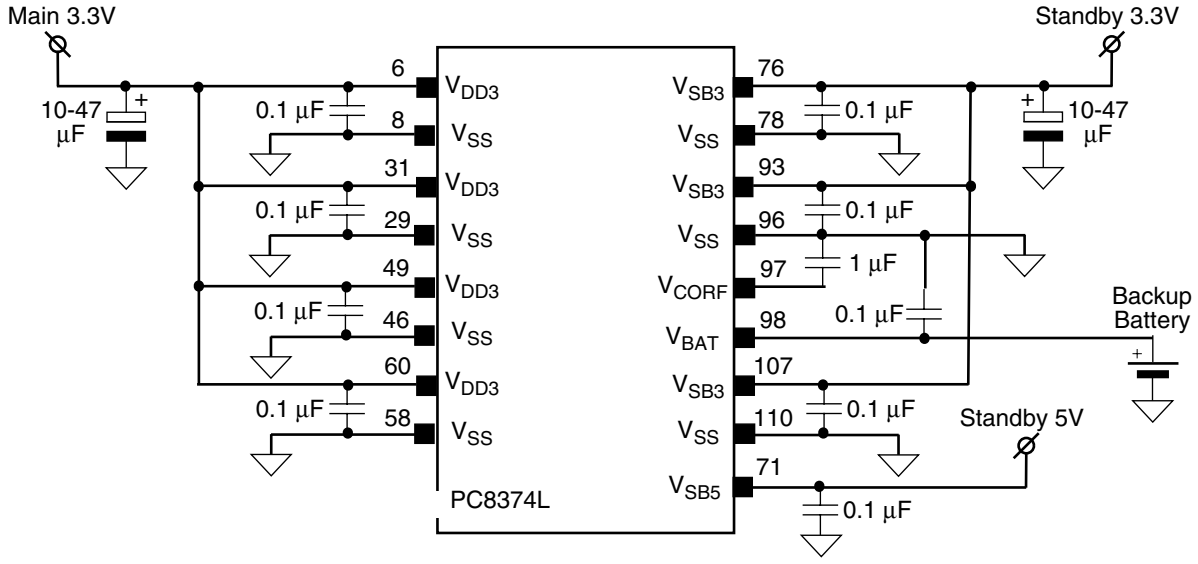


Figure 2. Decoupling Capacitors Connection

2.2 RESET SOURCES AND TYPES

The PC8374L device has five reset sources:

- **V_{BAT} Power-Up Reset** - activated when V_{BAT} is powered up, if V_{SB3} is off.
- **V_{SB} Power-Up Reset** - activated when V_{SB3} is powered up.
- **V_{DD} Power-Up Reset** - activated when V_{DD3} is powered up.
- **Hardware Reset** - activated when the $\overline{\text{PCI\_RESET}}$ input is asserted (low).
- **Software Reset** - triggered by SWRST bit in SIOCF1 register (see Section 3.7.5 on page 54); SWRST bit is set by the host through the LPC interface.

2.0 Power, Reset and Clocks (Continued)

Unless otherwise noted, reset references throughout the modules of the PC8374L devices default to the following resets:

- For V_{BAT}-retained functions (some SWC, Health Management configuration): V_{BAT} Power-Up reset (within the limitations described in Section 2.2.1).
- For V_{SB3}-powered functions (GPIO ports, SWC, Health Management, Glue Functions and some Configuration Control): V_{SB} Power-Up reset (within the limitations described in Section 2.2.2).
- For V_{DD3}-powered functions (Legacy modules, LPC, on-chip Clock Generator and some Configuration Control): V_{DD} Power-Up reset, Hardware Reset or Software Reset (within the limitations described in Sections 2.2.3, 2.2.4 and 2.2.5).

The following sections detail the sources and effects of the various PC8374L resets.

2.2.1 V_{BAT} Power-Up Reset

V_{BAT} Power-Up reset is generated by an internal circuit when V_{BAT} power is applied, if V_{SB3} is off. An active V_{BAT} Power-Up reset signal is generated following a rise in the V_{BAT} until the level of the V_{BAT} power higher than V_{BATLOW} is detected (see Section 10.1.5 on page 213). A V_{BAT} Power-Up reset is generated independently of the state of the V_{DD3} power supply. When V_{BAT} Power-Up reset is active, it resets the registers whose values are retained by V_{BAT} (some of the SWC, Health Management configuration).

2.2.2 V_{SB} Power-Up Reset

V_{SB} Power-Up reset is generated by an internal circuit when V_{SB3} power is applied. The V_{SB} Power-Up reset time (t_{IRST}) lasts either 17 cycles of the 32 KHz clock domain or until the $\overline{\text{PCI\_RESET}}$ signal is de-asserted, whichever occurs first. External devices must wait at least t_{IRST} before accessing the PC8374L device.

Note that the 32 KHz clock domain starts toggling $t_{32KW} + t_{32KVAL}$ after V_{SB3} power-up. This delay must be added to the 17 clock cycles (see “Low-Frequency Clock Timing” on page 223).

V_{SB} Power-Up reset performs the actions listed below and all the actions performed by V_{DD} Power-Up reset (see Section 2.2.3). Note that V_{DD3} must be active during V_{SB3} power-up for all V_{DD} Power-Up reset actions to be performed:

- Puts pins with V_{SB3} strap options into TRI-STATE and enables their internal pull-up resistors
- Samples the logic levels of the V_{SB3} strap pins
- Samples the levels of the V_{BAT} power pin
- Activates the relevant circuits in SWC according to the level of the V_{BAT} power pin
- Loads default values to the V_{BAT}-powered bits, if V_{BAT} is off
- Resets all lock bits in configuration registers, Health Management and SWC
- Loads default values to VDDLOAD bits in the GPIO configuration registers
- Loads default values to the V_{SB3}-powered bits in the configuration registers, SWC, Health Management and GPIO
- Sets up the pull-up or pull-down option and the default source for the V_{SB3}-powered multiplexed output pins

2.2.3 V_{DD} Power-Up Reset

V_{DD} Power-Up reset is generated by an internal circuit when V_{DD3} power is turned on. V_{DD} Power-Up reset time (t_{IRST}) lasts until the $\overline{\text{PCI\_RESET}}$ signal is de-asserted. The Hardware reset ($\overline{\text{PCI\_RESET}}$) must be asserted for a minimum of 10 ms to ensure that the PC8374L device operates correctly.

External devices must wait at least t_{IRST} before accessing the PC8374L. If the host processor accesses the PC8374L during this time, the PC8374L LPC interface ignores the transaction (that is, it does not return a SYNC handshake).

V_{DD3} Power-Up reset performs the following actions:

- Puts pins with strap options into TRI-STATE and enables their internal pull-up resistors
- Samples the logic levels of the strap pins
- Executes all the actions performed by the Hardware reset (see Section 2.2.4)

2.2.4 Hardware Reset

Hardware reset is activated by the assertion (low) of the $\overline{\text{PCI\_RESET}}$ input while V_{DD3} is “good”. When V_{DD3} power is off, the PC8374L device ignores the level of the $\overline{\text{PCI\_RESET}}$ input. However, the $\overline{\text{PCIRST\_OUT}}$ and $\overline{\text{PCIRST\_OUT2}}$ outputs reflect the $\overline{\text{PCI\_RESET}}$ input and thus are active (low). In addition, the Hardware reset ($\overline{\text{PCI\_RESET}}$) must be asserted after V_{SB} power-up, as described in Section 2.2.2.

2.0 Power, Reset and Clocks (Continued)

Hardware reset performs the following actions:

- Resets all lock bits in configuration registers, Health Management and SWC
- Sets up the pull-up or pull-down option and the default source for the V_{DD3}-powered multiplexed output pins
- Executes all the actions performed by the Software reset (see Section 2.2.5)

2.2.5 Software Reset

The Software reset is triggered by the host setting SWRST bit in SIOCF1 register (see Section 3.7.5 on page 54) via the LPC interface. The Host Software reset performs the following actions:

- Loads default values to the V_{DD3}-powered unlocked bits in the Configuration Control.
- Loads default values to the V_{SB3}-powered unlocked GPIO Configuration and Data bits for those GPIO ports with VDDLOAD = 1. VDDLOAD bit is not affected.
- Resets all the V_{DD3}-powered logical devices.
- Loads default values to all the V_{DD3}-powered module registers, unless explicitly specified otherwise.

2.3 CLOCK DOMAINS

Table 7 shows the PC8374L clock domains.

Table 7. Clock Domains of the PC8374L

Clock Domain	Frequency	Power Plane	Source	Usage
LPC	Up to 33 MHz	V_{DD3}	LPC clock input (PCI_CLK)	LPC bus Interface and Configuration Registers
48 MHz	48 MHz	V_{DD3}	On-Chip Clock Generator	Legacy functions (Serial Ports, InfraRed Port, Parallel Port, FDC, KBC)
Standby	48 MHz	V_{SB3}	On-Chip Clock Generator	Health Management Module
SW_360	360 KHz	V_{SB3}	On-Chip Clock Generator	Health Management Module
32 KHz	32.768 KHz	V_{SB3}	On-Chip Clock Generator	SWC, GPIO and Glue Functions

The LPC and 48 MHz clock domains, and the modules using them, are supplied by the Main power plane. Therefore, these clock domains are active only when the V_{DD3} power supply is on.

The Standby and SW_360 clock domains are sourced by the on-chip Clock Generator. The clock domains become active a certain time after first V_{DD3} power-up following V_{SB3} power-up, and they remain active as long as V_{SB3} exists.

The 32 KHz clock domain is sourced by the on-chip Clock Generator, which is supplied by the Standby power plane. The 32 KHz clock domain is active when the V_{SB3} power supply is on.

2.3.1 LPC Domain

The LPC clock signal at the PCI_CLK pin must become valid (to the extent specified in “PCI_CLK and PCI_RESET” on page 224) before the end of the V_{DD} Power-Up reset (see Section 2.2.3).

2.3.2 48 MHz Domain

The 48 MHz clock domain is sourced by the on-chip Clock Generator. The software must wait for CKVALID bit (see Section 3.7.11 on page 59) to be set before it enables the Legacy functions (Serial Ports, InfraRed Port, Parallel Port, FDC, KBC).

2.3.3 Standby Domain

The on-chip Clock Generator is the source of the Standby clock domain and all the other clock domains derived from it: SW_360 and 32 KHz.

Note that the Health Management is functional only after first V_{DD3} power-up following V_{SB3} power-up. The SWC, GPIO and Glue are functional on V_{SB3} power up.

The Standby clock is scaled-down by a fixed divider to generate the SW_360 clock domain used by the Health Management module. In addition, the Standby clock is supplied directly to the Health Management module for the generation of PWM output signals in the high frequency range. The 32 KHz clock domain is also derived from a scaled-down divider of the Standby clock.

2.0 Power, Reset and Clocks (Continued)

Specifications

Clock Generator wake-up time is 33 msec (maximum). This is measured from $\overline{\text{PCI\_RESET}}$ deassertion until the internal 48 MHz clock is stable. When V_{DD3} exists, tolerance (long term deviation) of the output clock, relative to the 14.31818 MHz clock, is ±110 ppm. Total tolerance is therefore ± (input reference clock tolerance + 110 ppm). Cycle-by-cycle variance is 0.4 nsec (maximum). When only V_{SB3} exists, tolerance (long term deviation) of the output clock is ± 10%.

2.4 TESTABILITY SUPPORT

The PC8374L device supports two testing techniques:

- In-Circuit Testing (ICT)
- XOR Tree Testing

2.4.1 ICT

The In-Circuit Testing (ICT) technique, also known as “bed-of-nails”, injects logic patterns to the input pins of the devices mounted on the tested board. It then checks their outputs for the correct logic levels.

The PC8374L supports this testing technique by floating (putting in TRI-STATE) all the device pins. This prevents “back-driving” the PC8374L pins by the ICT tester when a device normally controlled by PC8374L is tested (device inputs are driven by the ICT tester).

To enter TRI-STATE mode, the $\overline{\text{TRIS}}$ pin must be pulled low (by a 10 KΩ resistor to V_{SS}), and the $\overline{\text{TEST}}$ pin must be left unconnected after both V_{DD3} and V_{SB3} power supplies are turned on. In addition, the $\overline{\text{PCI\_RESET}}$ pin must be held low for at least 10 ms (see “VSB Power-Up Reset” on page 219 and “VDD Power-Up Reset” on page 221). After $\overline{\text{PCI\_RESET}}$ is deasserted, all the device output and I/O pins are floated (put in TRI-STATE); exceptions to this are the power supply pins (V_{DD3}, V_{SB3}, V_{SS}, V_{CORF}, V_{BAT}), analog pins (V_{SB5}, REF5V, REF5V_STBY), $\overline{\text{RSMRST}}$, which do not float in TRI-STATE mode.

2.4.2 XOR Tree Testing

When the PC8374L device is mounted on a board, it can be tested using the XOR Tree technique. This test also checks the correct connection of the device pins to the board.

To enter XOR Tree mode, the $\overline{\text{TEST}}$ pin must be pulled low (by a 10 KΩ resistor to V_{SS}), and the $\overline{\text{TRIS}}$ pin must be left unconnected after both V_{DD3} and V_{SB3} power supplies are turned on. In addition, the $\overline{\text{PCI\_RESET}}$ pin must be held low for at least 10 ms (see “VSB Power-Up Reset” on page 219 and “VDD Power-Up Reset” on page 221). After $\overline{\text{PCI\_RESET}}$ is deasserted, the device pins (including the $\overline{\text{PCI\_RESET}}$, $\overline{\text{TRIS}}$ and $\overline{\text{TEST}}$ pins) are connected in a XOR Tree configuration and are isolated from the internal PC8374L functions.

In XOR Tree mode, all PC8374L device pins are configured as inputs, except the last pin in the tree, which is the XOR_OUT output. The buffer type of the input pins participating in the XOR tree, is IN_T (Input, TTL compatible), regardless of the buffer type of these pins in normal device operation mode (see Section 1.4 on page 21). The input pins are chained through XOR gates, as shown in Figure 3. The power supply pins (V_{DD3}, V_{SB3}, V_{SS}, V_{CORF}, V_{BAT}), the analog pins (V_{SB5}, REF5V, REF5V_STBY, $\overline{\text{RSMRST}}$) and the not connected pins (NC) are excluded from the XOR tree.

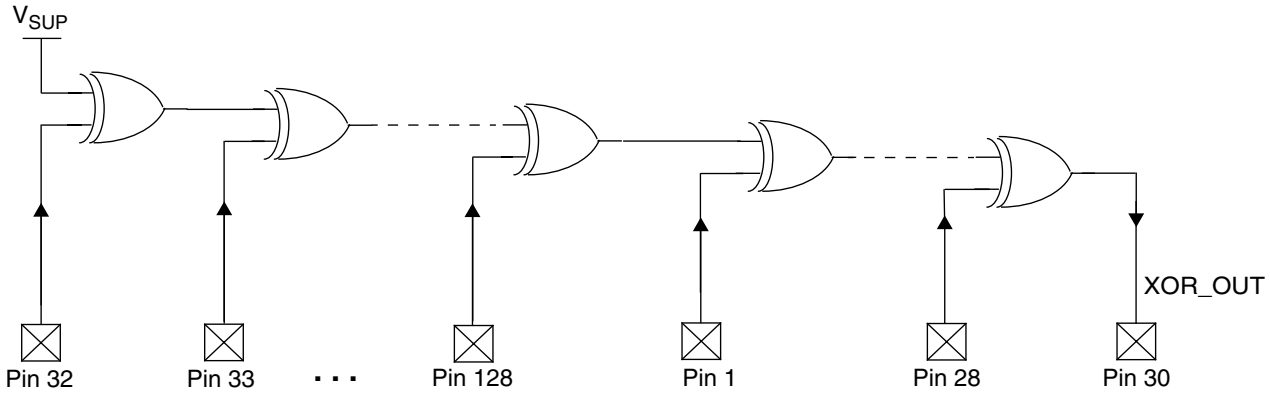


Figure 3. XOR Tree (Simplified Diagram)

The XOR tree starts with pin 32, continues incrementally with pin 33 (the next pin in ascending order) through pins 128, 1, and 28, and ends with pin 30 (XOR_OUT).

The maximum propagation delay through the XOR tree, from pin 32 to XOR_OUT is 200 ns.

3.0 Device Architecture and Configuration

The PC8374L SuperI/O device includes a collection of legacy and proprietary functional blocks. Each functional block is described in a separate chapter. This chapter describes the structure of the PC8374L SuperI/O device and provides all logical device specific information, including specific implementation of generic blocks, system interface and device configuration.

3.1 OVERVIEW

The PC8374L SuperI/O consists of the following: nine logical devices, the host interface, the Glue Functions and a central set of configuration registers.

The host, via the LPC Bus interface, can access the modules. This interface supports I/O Read/Write, Memory Read/Write, 8-bit Memory Firmware Read/Write, and 8-bit DMA transactions of the LPC bus (see Section 5.2 on page 109).

The central configuration register set is ACPI compliant and supports PnP configuration. The configuration registers are structured as a subset of the Plug and Play Standard registers, defined in Appendix A of the *Plug and Play ISA Specification, Revision 1.0a* by Intel® and Microsoft®. All system resources assigned to the functional blocks (Memory address space, I/O address space, IRQ numbers and DMA channels) are configured in and managed by the central configuration register set. In addition, some function-specific parameters are configurable through the configuration registers and distributed to the functional blocks through special control signals.

3.2 CONFIGURATION STRUCTURE AND ACCESS

The configuration structure is based on a set of banked registers that are accessed via a pair of specialized registers.

3.2.1 The Index-Data Register Pair

Access to the PC8374L configuration registers is via an Index-Data register pair, using only two system I/O byte locations. The base address of this register pair is determined during reset according to the state of the hardware strapping option on the $\overline{\text{BADDR}}$ pin. Table 8 shows the selected base addresses as a function of $\overline{\text{BADDR}}$.

Table 8. $\overline{\text{BADDR}}$ Strapping Options

$\overline{\text{BADDR}}$	I/O Address	
	Index Register	Data Register
1 (default)	2Eh	2Fh
0	4Eh	4Fh

The Index register is an 8-bit read/write register located at the selected base address (Base+0). It is used as a pointer to the configuration register file and holds the index of the configuration register that is currently accessible via the Data register. Reading the Index register returns the last value written to it (or the default of 00h after reset).

The Data register is an 8-bit register (Base+1) used as a data path to any configuration register. Accessing the Data register actually accesses the configuration register that is currently pointed to by the Index register.

3.2.2 Banked Logical Device Registers Structure

Each functional block is associated with a Logical Device Number (LDN). The configuration registers are grouped into banks, where each bank holds the standard configuration registers of the corresponding logical device. Table 9 shows the LDN values of the PC8374L functional blocks. Any value not listed is reserved.

Figure 4 shows the structure of the standard configuration register file. The LDN and PC8374L configuration registers are not banked and are accessed by the Index-Data register pair only, as described above. However, the device control and device configuration registers are duplicated over nine banks, corresponding to the nine logical devices. Therefore, accessing a specific register in a specific bank is performed by two-dimensional indexing, where the LDN register selects the bank (or logical device) and the Index register selects the register within the bank. Accessing the Data register while the Index register holds a value of 30h or higher actually accesses the configuration registers of the logical device selected by the LDN register and pointed to by the Index register.

3.0 Device Architecture and Configuration (Continued)

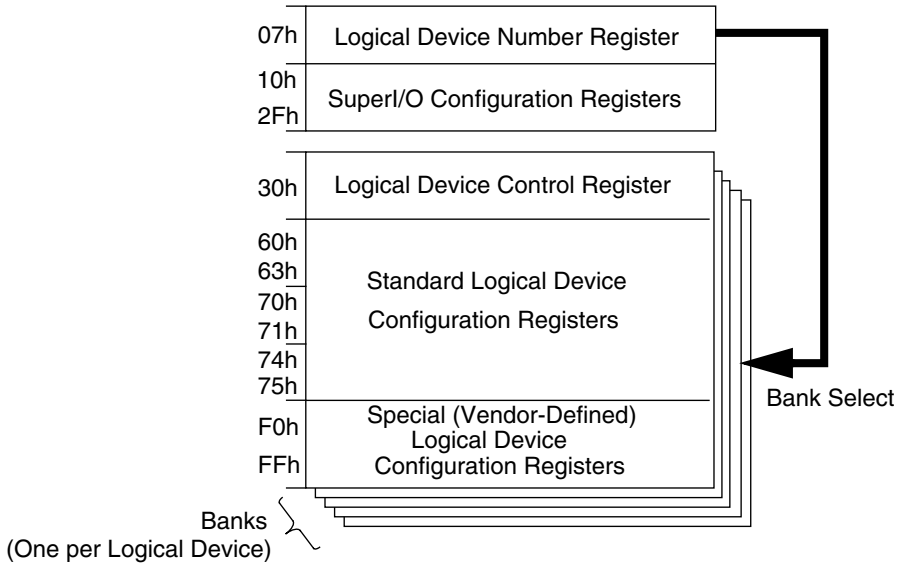


Figure 4. Structure of Standard Configuration Register File

Table 9. Logical Device Number (LDN) Assignments

LDN	Functional Block
00h	Floppy Disk Controller (FDC)
01h	Parallel Port (PP)
02h	Serial Port 2 (SP2) and InfraRed Port
03h	Serial Port 1 (SP1)
04h	System Wake-Up Control (SWC)
05h	Keyboard and Mouse Controller (KBC) - Mouse Interface
06h	Keyboard and Mouse Controller (KBC) - Keyboard Interface
07h	General-Purpose I/O (GPIO) Ports
08h	Health Management

Write accesses to unimplemented registers (i.e., accessing the Data register while the Index register points to a non-existing register) are ignored. Read accesses return 00h on all addresses, except for 74h and 75h (DMA configuration registers), which returns 04h (indicating no DMA channel). The configuration registers are accessible immediately after reset.

3.2.3 Standard Configuration Register Definitions

In the registers below, any undefined bit is reserved. Unless otherwise noted, the following definitions also hold true:

- All registers are read/write.
- All reserved bits return 0 on reads, except where noted otherwise. To prevent unpredictable results, do not modify these bits. Use read-modify-write to prevent the values of reserved bits from being changed during write.
- Write-only registers must not use read-modify-write during updates.

3.0 Device Architecture and Configuration (Continued)

Table 10. Standard General Configuration Registers

Index	Register Name	Description
07h	Logical Device Number	This register selects the current logical device. See Table 9 for valid numbers. All other values are reserved.
10h	Memory Mapping Control	Enables the memory mapping of the device and configuration registers.
12h	Memory Base Address 1	Indicates selected Memory Base address bits 23-16.
13h	Memory Base Address 2	Indicates selected Memory Base address bits 31-24.
20h-2Fh	PC8374L Configuration	PC8374L configuration registers and ID registers.

Table 11. Logical Device Activate Register

Index	Register Name	Description
30h	Activate	Bits 7-1: Reserved Bit 0: Logical device activation control (see Section 3.3 on page 48) 0: Disabled 1: Enabled

Table 12. Memory Space Configuration Registers

Index	Register Name	Description
50h	Memory Base Descriptor	Controls the mapping of a logical device to I/O or to memory when MEMEN bit in MEMMAP register is set to 1 (see Section 3.7.1 on page 52). Bit 0: Logical device mapping control (see Section 3.3 on page 48) 0: Logical device is mapped to I/O space (default) 1: Logical device is mapped to Memory space Bits 7-1: Reserved

Table 13. I/O Space Configuration Registers

Index	Register Name	Description
60h	I/O Port Base Address Bits 15–8 Descriptor 0	Indicates selected I/O lower limit address bits 15–8 for I/O Descriptor 0.
61h	I/O Port Base Address Bits 7–0 Descriptor 0	Indicates selected I/O lower limit address bits 7–0 for I/O Descriptor 0.
62h	I/O Port Base Address Bits 15–8 Descriptor 1	Indicates selected I/O lower limit address bits 15–8 for I/O Descriptor 1.
63h	I/O Port Base Address Bits 7–0 Descriptor 1	Indicates selected I/O lower limit address bits 7–0 for I/O Descriptor 1.

3.0 Device Architecture and Configuration (Continued)

Table 14. Interrupt Configuration Registers

Index	Register Name	Description
70h	Interrupt Number and Wake-Up on IRQ Enable	Indicates selected interrupt number. Bits 7-5: Reserved. Bit 4: Enables a Power Management event ($\overline{\text{SIOPME}}$) from the IRQ of the logical device. When enabled, IRQ assertion sets the respective *XXX*_IRQ_STS bit (*XXX* is MOD, MS or KBD) in the GPE1_STS_3 register (see Section 4.4.7 on page 103). 0: Disabled (default) 1: Enabled **Note:** If the BIOS routine that sets IRQ does not use a Read-Modify-Write sequence, it might reset bit 4. To ensure that the system wakes up, the BIOS must set bit 4 before the system goes to sleep. Bits 3-0: These bits select the interrupt number. A value of 1 selects IRQ1. A value of 15 selects IRQ15. IRQ0 is not a valid interrupt selection and represents no interrupt selection. **Note:** Avoid selecting the same interrupt number (except 0) for different Logical Devices, as it causes the PC8374L device to behave unpredictably.
71h	Interrupt Request Type Select	Indicates the type and polarity of the interrupt request number selected in the previous register. If a logical device supports only one type of interrupt, the corresponding bit is read-only. Bits 7-2: Reserved. Bit 1: Polarity of interrupt request selected in previous register 0: Low polarity 1: High polarity Bit 0: Type of interrupt request selected in previous register 0: Edge 1: Level

Table 15. DMA Configuration Registers

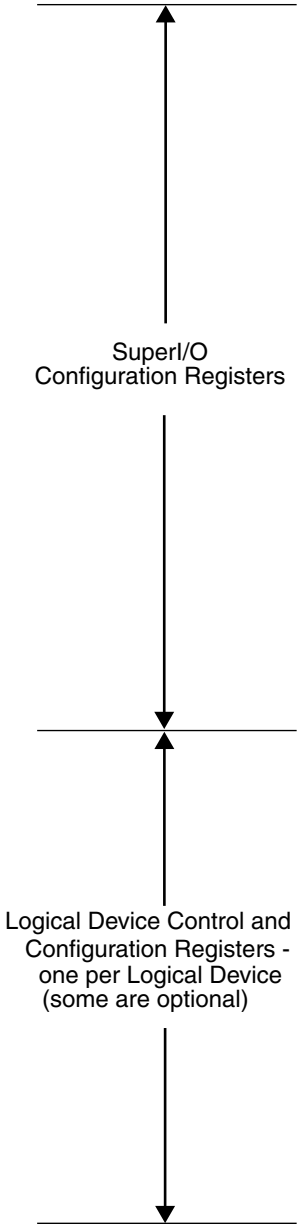
Index	Register Name	Description
74h	DMA Channel Select 0	Indicates selected DMA channel for DMA 0 of the logical device (0 is the first DMA channel if more than one DMA channel is used). Bits 7-3: Reserved. Bits 2-0: These select the DMA channel for DMA 0. The valid choices are 3-0, where: - A value of 0 selects DMA channel 0, 1 selects channel 1, etc. - A value of 4 indicates that no DMA channel is active. - The values 5-7 are reserved. **Note:** Avoid selecting the same DMA channel (except 4) for different logical devices, as it causes the PC8374L device to behave unpredictably.
75h	DMA Channel Select 1	Indicates selected DMA channel for DMA 1 of the logical device (1 is the second DMA channel if more than one DMA channel is used). Bits 7-3: Reserved. Bits 2-0: These select the DMA channel for DMA 1. The valid choices are 3-0, where: - A value of 0 selects DMA channel 0, 1 selects channel 1, etc. - A value of 4 indicates that no DMA channel is active. - The values 5–7 are reserved. **Note:** Avoid selecting the same DMA channel (except 4) for different logical devices, as it causes the PC8374L device to behave unpredictably.

3.0 Device Architecture and Configuration (Continued)

Table 16. Special Logical Device Configuration Registers

Index	Register Name	Description
F0h-FFh	Logical Device Configuration	Special (vendor-defined) configuration options.

3.2.4 Standard Configuration Registers



Index	Register Name
07h	Logical Device Number
10h	Memory Space Configuration
12h-13h	Memory Base Address (MEM_BASE)
20h	SuperI/O ID
21h	SuperI/O Configuration 1
22h	SuperI/O Configuration 2
23h	SuperI/O Configuration 3
24h	SuperI/O Configuration 4
25h	Reserved
26h	SuperI/O Configuration 6
27h	SuperI/O Revision ID
28h	Reserved
29h	Clock Generator Control
2A	Health Management SMBus Configuration
2Bh-2Dh	Reserved
2Eh-2Fh	Reserved exclusively for National use
30h	Logical Device Control (Activate)
50h	Memory Base Descriptor
60h	I/O Base Address Descriptor 0 Bits 15-8
61h	I/O Base Address Descriptor 0 Bits 7-0
62h	I/O Base Address Descriptor 1 Bits 15-8
63h	I/O Base Address Descriptor 1 Bits 7-0
70h	Interrupt Number and Wake-Up on IRQ Enable
71h	IRQ Type Select
74h	DMA Channel Select 0
75h	DMA Channel Select 1
F0h-FFh	Vendor-Defined Logical Device Configuration

Figure 5. Configuration Register Map

3.0 Device Architecture and Configuration (Continued)

SuperI/O Configuration Registers

The PC8374L SuperI/O configuration registers at indexes 20h (SuperI/O ID) and 27h (SuperI/O Revision ID) are used for part identification. The other configuration registers are used for global power management and selecting pin multiplexing options. For details, see Section 3.7 on page 52.

Logical Device Control and Configuration Registers

A subset of these registers is implemented for each logical device. See the functional block descriptions in the following sections.

Control Registers

The only implemented control register for each logical device is the Activate register at index 30h. Bit 0 of the Activate register controls the activation of the associated functional block. Activation enables access to the functional block's runtime registers and attaches its system resources, which are unassigned as long as it is not activated. Other effects may apply on a function-specific basis (such as clock enable and active pinout signaling). Access to the configuration register of the logical device is enabled even when the logical device is not activated.

Standard Configuration Registers

The standard configuration registers manage the PnP resource allocation to the functional blocks. The I/O port base address descriptor 0 is a pair of registers at Index 60–61h that hold the first 16-bit base address for the register set of the functional block. An optional 16-bit second base-address (descriptor 1) at index 62–63h is used for logical devices with more than one continuous register set. Interrupt Number and Wake-Up on IRQ Enable (index 70h) and IRQ Type Select (index 71h) allocate an IRQ line to the block and control its type. DMA Channel Select 0 (index 74h) allocates a DMA channel to the block, where applicable. DMA Channel Select 1 (index 75h) allocates a second DMA channel, where applicable.

Vendor-Defined Logical Device Configuration Register

The vendor-defined logical device registers start at index F0h and control function-specific parameters such as operation modes, power saving modes, pin TRI-STATE, clock rate selection and non-standard extensions to generic functions.

3.2.5 Default Configuration Setup

The default configuration setup of the PC8374L device is determined by the four reset types described in Section 2.2 on page 34. See the specific register descriptions for the bits affected by each reset source.

In the event of a V_{SB3} Power-Up reset, the following default configuration is set up:

- All lock bits in the configuration registers are reset (the protected bits are unlocked).
- All the unlocked bits in the configuration registers powered by the V_{SB3} plane are reset to their default values.

In the event of a V_{DD3} Power-Up (also induced by V_{SB3} Power-Up reset) or Hardware reset, the PC8374L device wakes up with the following default configuration setup:

- The configuration base address is 2Eh or 4Eh, according to the $\overline{\text{BADDR}}$ strap pin value, as shown in Table 8 on page 38.
- All lock bits in the configuration registers are reset (the protected bits are unlocked).
- All the actions performed by the Software reset are executed.

If a Software reset occurs, the PC8374L device wakes up with the following default configuration setup:

- All the unlocked bits in the configuration registers powered by the V_{DD3} plane are reset to their default values.
- All logical devices are disabled (the Activation bit is reset) and the V_{SB3}-powered logical devices (GPIO, SWC, and Health Management) remain functional but their registers cannot be accessed by the host.
- Standard configuration registers of all logical devices are set to their default values.
- National Semiconductor proprietary functions are not assigned with any default resources, and the default values of their base addresses are all 00h.
- All Legacy devices (Serial Ports, InfraRed Port, Parallel Port, Floppy Disk Controller, and Keyboard and Mouse Controller) are reset. Default values are loaded into the Legacy module runtime registers.

3.0 Device Architecture and Configuration (Continued)

3.2.6 Memory Space Mapping

The PC8374L device configuration registers and Logical Device registers can be mapped to either I/O or memory space. The memory mapping control register (MEMMAP; see Section 3.7.1 on page 52) enables the device memory mapping, and allows memory mapping of PC8374L control and configuration registers at I/O indexes 10h-2Fh, and logical device configuration registers at I/O indexes 30h-FFh. Each logical device register can be enabled separately for memory access by memory base descriptor at I/O index 50h.

The memory base address MEM_BASE of the PC8374L device is determined by MEMADR1 and MEMADR2 registers, which hold the high 15-bits of 32-bits memory address (see Section 3.7.2 and Section 3.7.3 on page 53). Address bit 31 is reserved to 1; this limits the PC8374L device memory mapping to the high 2GB of memory space. Address bits 0-15 are used for mapping of PC8374L device registers; this allows the PC8374L device a linear address space with total of 64K.

Note: The maximum value for MEM_BASE+64K should not exceed 4G-64K-1=FFFEFFFFh to avoid overlapping with the BIOS memory area (see Figure 6 on page 45); that is, the maximum value of MEM_BASE should not exceed FFFDFFFFh.

Operating System device drivers must be responsible for performing physical-to-virtual memory-address translation, including allocation of selectors that point to the PC8374L device. The device may be accessed in Protected mode by creating a selector with the physical address defined in MEMADR1 and MEMADR2 registers, and a maximum size of 64K.

Table 17 and Table 18 show how to access the memory mapped registers of PC8374L device. Table 17 shows the memory address to registers of Logical Devices with one bank, such as GPIO. This method allows access to up to 1024 registers in each Logical Device that is organized as one bank.

Table 17. PC8374L Register Memory Address

31	30 24	23 16	15	14 10	9 0
Reserved	**MEM_BASE**		**Window**	**Logical Device Number**	**Register Offset**
1	xxx xxxx	xxxx xxxx	x	xxx xx	xx xxxx xxxx

Table 18 shows the memory address to PC8374L device control and configuration registers and to registers of Logical Devices with several banks. This method allows access to up to 32 banks (and up to 32 registers in each bank) in Logical Devices that are organized in banks.

Table 18. PC8374L Register Memory Address to Logical Device with Register Banks

31	30 24	23 16	15	14 10	9 5	4 0
Reserved	**MEM_BASE**		**Window**	**Logical Device Number**	**Bank Number**	**Register Offset**
1	xxx xxxx	xxxx xxxx	x	xxx xx	xx xxx	x xxxx

Window bit provides duplicate addresses for registers, to be used for read and write accesses. This resolves the problem of PCI/LPC transaction buffering by some chip-sets. For example, this feature can be used to insure the order of transactions for Write 1-to-Clear or Read-to-Clear registers.

Table 19 shows the Logical Device Number (LDN) field used by memory transactions for each PC8374L internal function that can be enabled for memory transactions. Note that most of these LDNs are equivalent to those assigned by the plug-and-play configuration, but they are not functionally identical.

Table 19. Logical Device Number (LDN) Assignment for Memory Space Mapping

LDN	Functional Block
04h	System Wake-Up Control (SWC) Register Offset Bit 9 = 0: SWC Registers Register Offset Bit 9 = 1: ACPI Registers
07h	General-Purpose I/O (GPIO) Ports
08h	Health Management

3.0 Device Architecture and Configuration (Continued)

Two types of memory transactions are supported: LPC memory read/write and LPC FWH memory read/write. The PC8374L can respond to only one transaction type at a time. The active type is controlled by TYPESEL bit in MEMADR2 register (see Section 3.7.3 on page 53). When the active type is FWH, the PC8374L responds only to transactions where the IDSEL value matches MEMFWHID field in MEMADR2 register. In this case the value of the least significant bit of MEMFWHID is also used as bit 27 of MEM_BASE, which is the most significant bit of the FWH address.

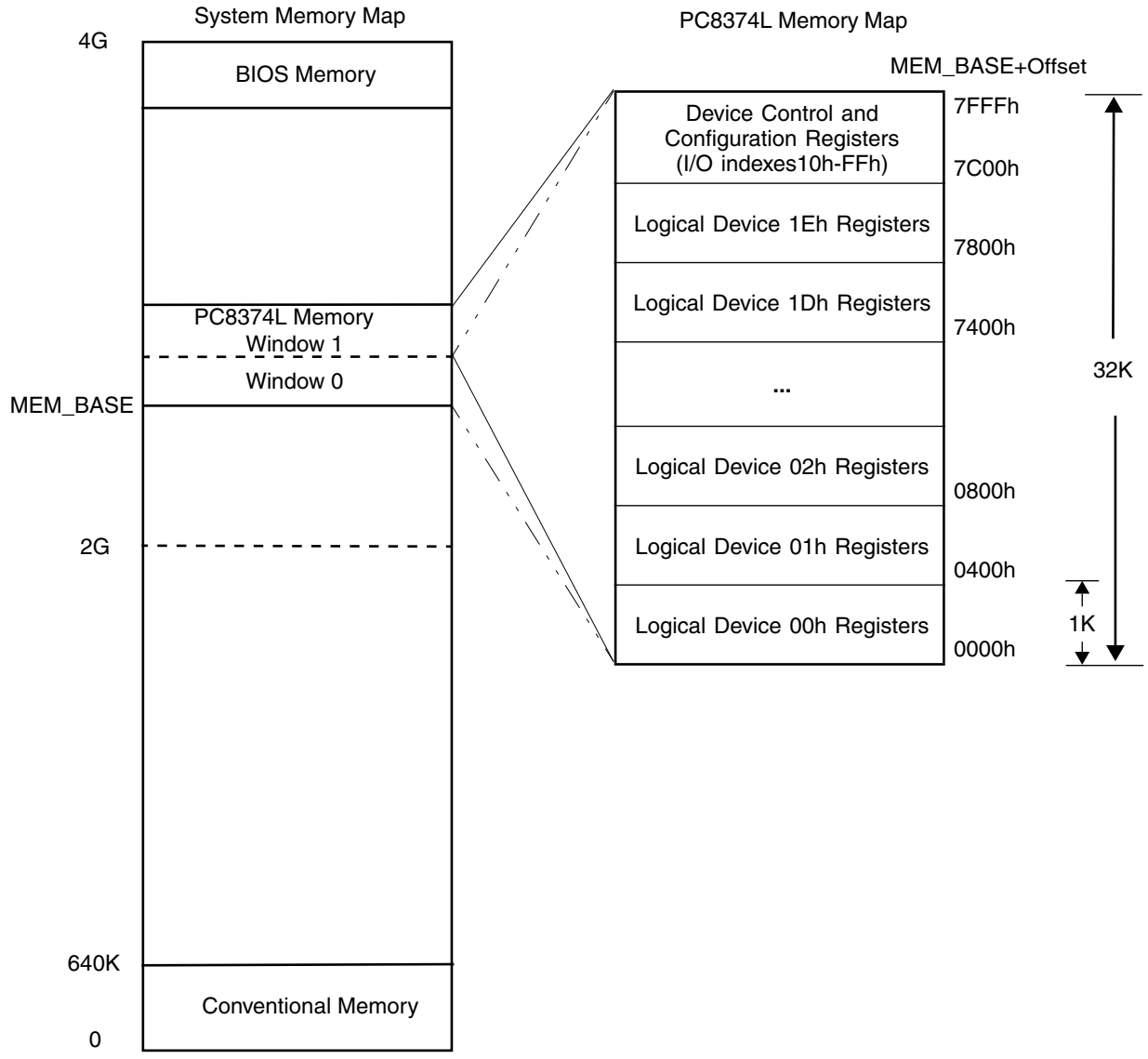


Figure 6. PC8374L Memory Address Map

Figure 6 shows the memory address map for PC8374L device. The device control and configuration registers (I/O indexes 10h-2Fh) and Logical Device control and configuration registers (I/O indexes 30h-FFh) are located in the last 2K of the device memory range.

Figure 7 shows the memory address map of Logical Devices with register banks.

The PC8374L device control and configuration registers (I/O indexes 10h-2Fh) are located in last 32 bytes of the memory mapping, when their memory mapping is enabled by MEMMAP register (see Section 3.7.1 on page 52). Table 20 shows the memory physical addresses of these registers.

Table 20. Memory Physical Addresses of Device Configuration Registers

Register	I/O Index	Memory Physical Address
PC8374L Configurations	10h-2Fh	MEM_BASE+7FE0h to MEM_BASE+7FFFh

3.0 Device Architecture and Configuration (Continued)

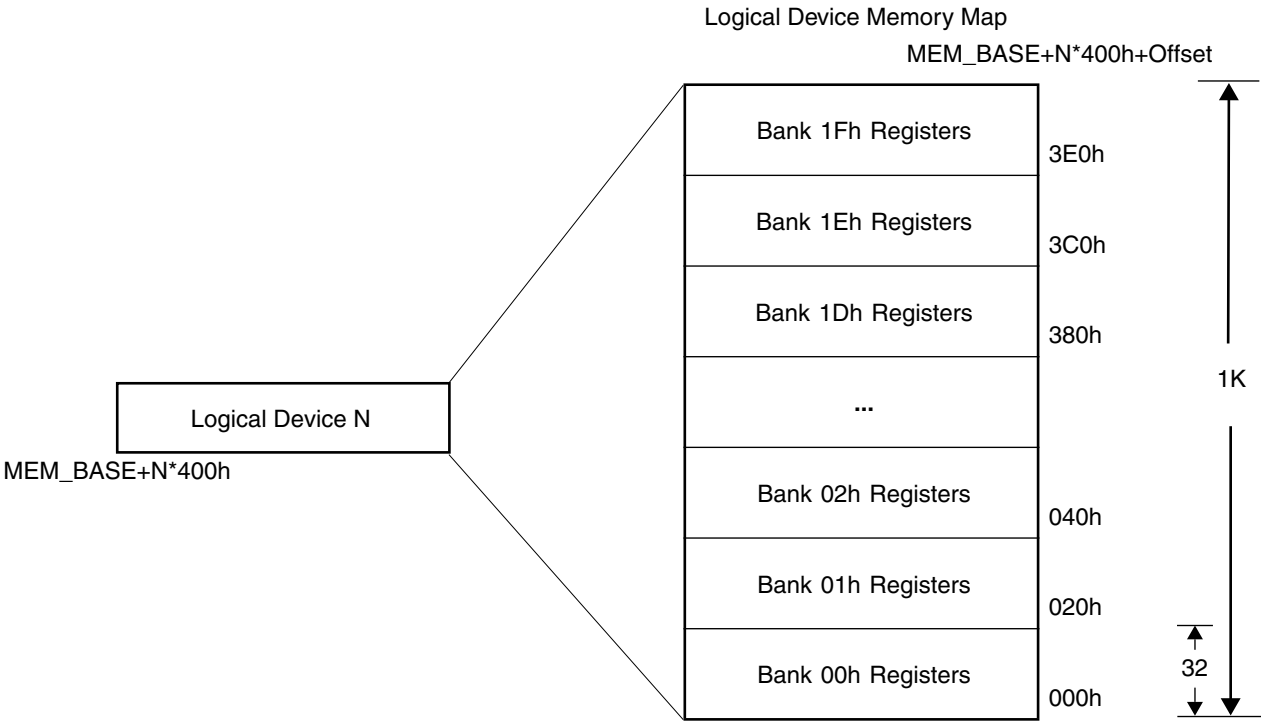


Figure 7. Logical Device Memory Map with Register Banks

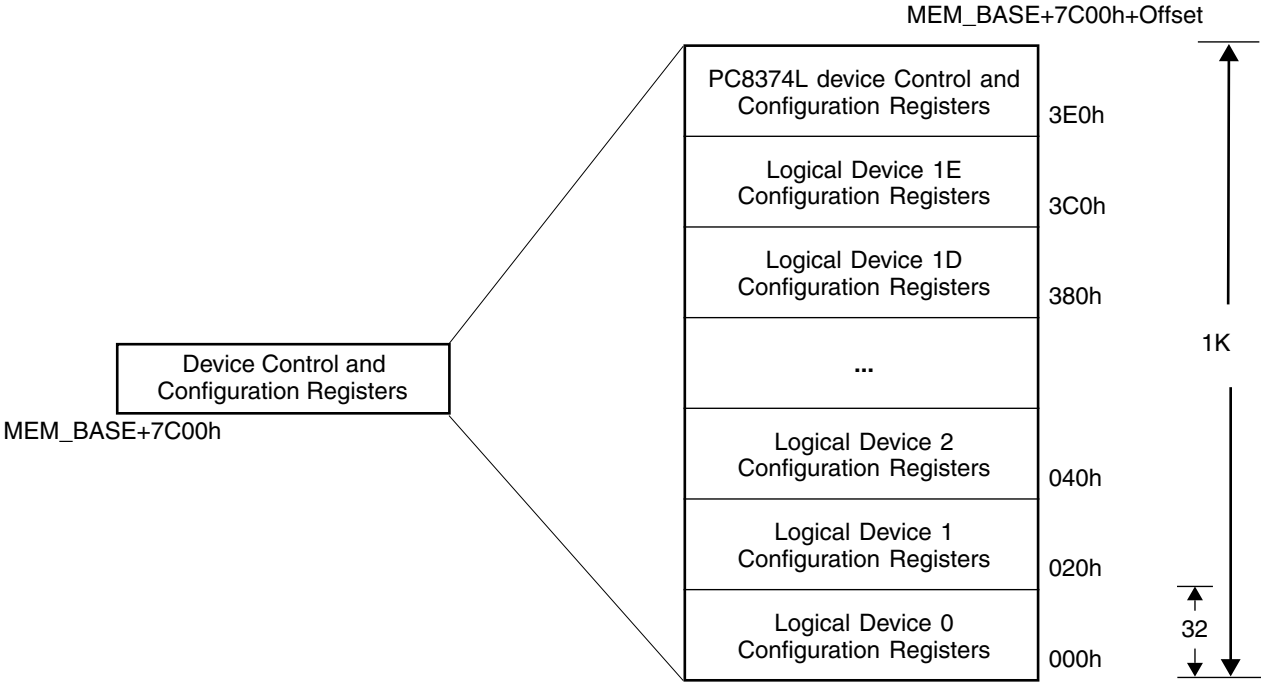


Figure 8. Control and Configuration Memory Map

3.0 Device Architecture and Configuration (Continued)

The memory mapping of Logical Devices control and configuration registers (I/O indexes 30h-FFh) are enabled by MEMMAP register (see Section 3.7.1 on page 52). When enabled for memory access, these registers are grouped to 32 byte banks, one for each Logical Device as shown on Figure 8. Table 21 provides the conversion between I/O offsets and memory offsets of these registers for Logical Device number N. The offsets specified in the table should be added to MEM_BASE+7C00h+N*20h to get the memory physical address

Table 21. Memory Physical Addresses of Logical Device Configuration Registers

Register	I/O Index	Memory Offset
Logical Device Control (Activate)	30h	00h
Memory Base Descriptor	50h	01h
I/O Base Address Descriptor 0 Bits 15-8	60h	03h
I/O Base Address Descriptor 0 Bits 7-0	61h	04h
I/O Base Address Descriptor 1 Bits 15-8	62h	05h
I/O Base Address Descriptor 1 Bits 7-0	63h	06h
I/O Base Address Descriptor 2 Bits 15-8	64h	07h
I/O Base Address Descriptor 2 Bits 7-0	65h	08h
I/O Base Address Descriptor 3 Bits 15-8	66h	09h
I/O Base Address Descriptor 3 Bits 7-0	67h	0Ah
Interrupt Number and Wake-Up on IRQ Enable	70h	0Bh
IRQ Type Select	71h	0Ch
DMA Channel Select 0	74h	0Dh
DMA Channel Select 1	75h	0Eh
Device Specific Logical Device Configuration	F0h - FFh	10h to 1Fh

3.0 Device Architecture and Configuration (Continued)

3.3 MODULE CONTROL

Module control is performed primarily through the Activation bit (bit 0 of index 30h) of each logical device.

3.3.1 Module Enable/Disable

Module control is performed primarily through the Activation bit (bit 0 of index 30h) of each logical device. The operation of each module can be controlled by the host.

Module enable/disable by the host through the LPC bus is controlled by the following bits:

- Activation bit (bit 0) in index 30h of the Standard configuration registers (see Section 3.2.3 on page 39)
- Fast Disable bit in SIOCF6 register; for the FDC, Parallel Port and Serial Port (1 and 2) / InfraRed Port modules only (see Section 3.7.9 on page 57)
- Global Enable bit (GLOBEN) in SIOCF1 register (see Section 3.7.5 on page 54)

A module is enabled only if all of these bits are set to their “enable” value.

When a module is disabled, the following takes place:

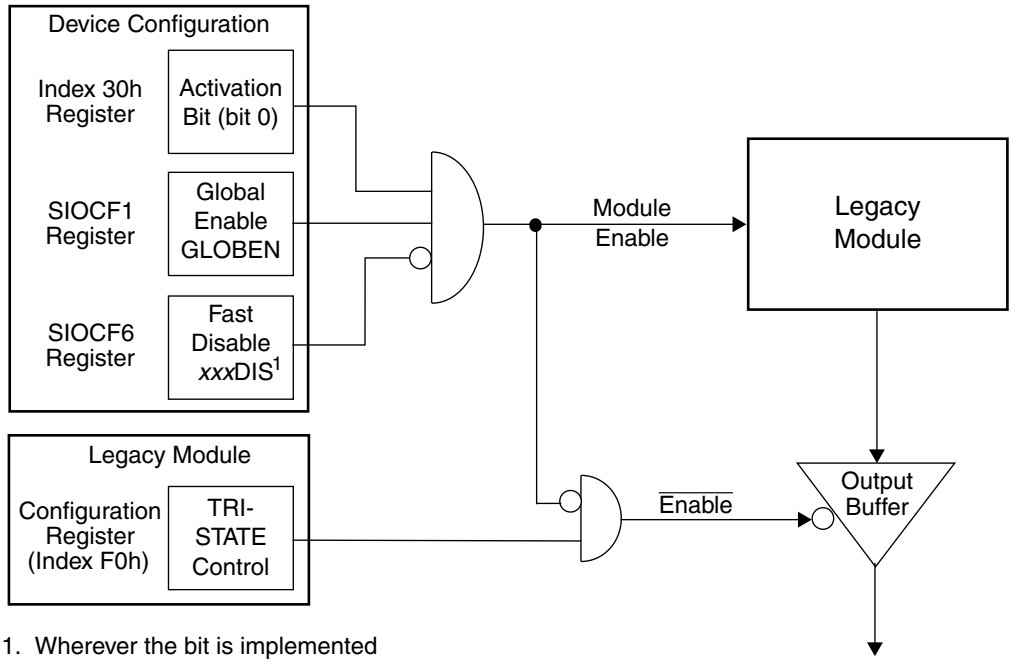
- The host system resources of the logical device (IRQ, DMA and runtime address range) are unassigned.
- Access to the standard- and device-specific Logical Device configuration registers through the LPC bus remains enabled.
- Access to the module’s runtime registers through the LPC bus is disabled (transactions are ignored; SYNC cycle is not generated).

Note that disabling a V_{DD3}-powered module (FDC, Parallel Port, Serial Ports, InfraRed Port, KBC) stops the module’s internal clock to lower the power consumption; as a result, the module is not functional. V_{SB}-powered modules remain functional.

3.3.2 Floating Module Output

The pins of the Legacy modules (Serial Ports, Parallel Port, Floppy Disk Controller, Keyboard and Mouse Controller) can be floated. When the TRI-STATE Control bit (bit 0) is set in the specific module configuration register (at index F0h of the specific Logical Device in the configuration space) **and** the module is disabled (see Section 3.3.1), the module output signals are floated and the I/O signals are configured as inputs (note that the logic level at the inputs is ignored by the module, which is disabled).

Figure 9 shows the control mechanism for floating the pins of a Legacy module.



1. Wherever the bit is implemented

Figure 9. Control of Floating Legacy Module Pins

3.0 Device Architecture and Configuration (Continued)

3.4 INTERNAL ADDRESS DECODING

A full 16-bit address decoding is applied when accessing the configuration I/O space as well as the registers of the functional blocks. However, the number of configurable bits in the base address registers varies for each logical device.

The lower 1, 2, 3, 4 or 5 address bits are decoded in the functional block to determine the offset of the accessed register within the logical device's I/O range of 2, 4, 8, 16 or 32 bytes, respectively. The rest of the bits are matched with the base address register to decode the entire I/O range allocated to the logical device. Therefore, the lower bits of the base address register are forced to 0 (read-only), and the base address is forced to be 2, 4, 8, 16 or 32 byte-aligned, according to the size of the I/O range.

The base address of the FDC, Serial Port 1, Serial Port 2, InfraRed Port, and KBC are limited to the I/O address range of 00h to 7FXh only (bits 15-11 are forced to 0). The Parallel Port base address is limited to the I/O address range of 00h to 3F8h. The addresses of all of the non-legacy logical devices, including the Health Management, SWC and GPIO, are configurable within the full 16-bit address range (up to FFFXh).

In some special cases, other address bits are used for internal decoding (such as bit 2 in the KBC and bit 10 in the Parallel Port). The KBC has two I/O base addresses with some implied dependency between them. For more details, see the description of the base address register for each logical device.

3.0 Device Architecture and Configuration (Continued)

3.5 PROTECTION

The PC8374L device provides features to protect the hardware configuration from changes made by application software running on the host.

The protection is activated by the software setting a “sticky” lock bit. Each lock bit protects a group of configuration bits located either in the same register or in different registers. When the lock bit is set, the lock bit and all the protected bits become read-only and cannot be further modified by the host through the LPC bus. All the lock bits are reset by Power-Up reset, thus unlocking the protected configuration bits.

The bit locking protection mechanism is optional. The protected groups of configuration bits are described below.

3.5.1 Multiplexed Pins Configuration Lock

Protects the configuration of all the multiplexed device pins.

Lock bit: LOCKMCF in SIOCF1 register (Device Configuration).

Protected bits: LOCKMCF and IOWAIT in SIOCF1 register, and all bits in SIOCF2, SIOCF3 and SIOCF4 registers (Device Configuration).

3.5.2 GPIO Ports Configuration Lock

Protects the configuration (but not the data) of all the GPIO Ports.

Lock bit: LOCKGCF in SIOCF1 register (Device Configuration).

Protected bits for each GPIO Port:LOCKGCF in SIOCF1 register, and all bits in GPCFG1 (except LOCKCFP bit), GPEVR, GPCFG2 and GPMODE registers (Device Configuration).

3.5.3 Fast Disable Configuration Lock

Protects the Fast Disable bits for all the Legacy modules.

Lock bit: LOCKFDS in SIOCF6 register (Device Configuration).

Protected bits: All bits in SIOCF6 register (except General-Purpose Scratch bits) and GLOBEN bit in SIOCF1 register (Device Configuration).

3.5.4 Clock Control Lock

Protects the Clock Generator control bits.

Lock bit: LOCK in CLOCKCF register (Device Configuration).

Protected bits: All bits in CLOCKCF register (Device Configuration).

3.5.5 GPIO Port Lock

Protects the configuration **and** data of all the GPIO Ports.

Lock bit: LOCKCFP in GPCFG1 register, for each GPIO Port (Device Configuration).

Protected bits for each GPIO Port: LOCKCFP, PDNCTL, PUPCTL, OUTTYPE and OUTENA in GPCFG1 register; all bits in GPCFG2 register (Device Configuration); the corresponding bit (to the port pin) in GPDO and GPDIO registers (GPIO Ports).

3.5.6 Health Management Configuration Lock

Protects the configuration of the Health Management module.

Lock bit: LOCKHCF in HMCFG1 register (Device Configuration).

Protected bits: All bits in HMCFG1 register (including LOCKHCF bit itself) (Device Configuration).

3.5.7 SWC Configuration Lock

Protects the configuration of the SWC module, including the Keyboard and Mouse wake-up configuration.

Lock bit: LOCKSCF in SWC_CTL register (System Wake-Up Control).

Protected bits: BLINK and GRN_YLW bits in SLEDCTL register; all bits in SWC_CTL, ALEDCTL, LEDBLNK, XLEDCTL, KBDWKCTL, PS2CTL andPS2KEY0–7 registers (System Wake-Up Control).

3.0 Device Architecture and Configuration (Continued)

3.6 REGISTER TYPE ABBREVIATIONS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register (data written to this address is sent to a different register).
- W = Write (see above).
- RO = Read-only.
- WO = Write-only. Reading from the bit returns 0.
- R/WC = Read/Write any value to Clear. Writing any value to a bit clears it to 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

In the registers below, use one of the following methods to handle the reserved bits:

- Write 0 to reserved bits, unless another “required value” is specified. This method can be used for registers containing bits of all types.
- Use read-modify-write to preserve the values of the reserved bits. This method can be used only for registers containing bits of R/W, RO, R/W1C and R/W1S types.

3.0 Device Architecture and Configuration (Continued)

3.7 PC8374L CONFIGURATION REGISTERS

This section describes the PC8374L configuration and ID registers (i.e., registers with first level indexes in the range of 10h–2Fh).

3.7.1 Memory Mapping Control Register (MEMMAP)

Power Well: V_{DD3}

Location: Index 10h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**MEMEN**	**LOCKMEM**	**Reserved**			**BIODIS**	**LDMEMEN**	**CFGMEMEN**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W or RO	**MEMEN (Memory Mapping Enable).** When set to 1, enables memory mapping. MEMADR1 and MEMADR2 registers must be configured before this bit is set to 1. 0: Memory mapping is disabled (default) 1: Memory mapping is enabled
6	R/W1S	**LOCKMEM** (**Lock Memory Mapping Configuration).** When set to 1, locks the configuration registers of memory mapping: MEMMAP, MEMADR1 and MEMADR2. Once set, the bit can be cleared only by V_{DD3} Power-Up reset. 0: R/W bits are enabled for write (default) 1: All bits of MEMMAP, MEMADR1 and MEMADR2 registers are RO
5-3		**Reserved.**
2	R/W or RO	**BIODIS (I/O Base Address Disable).** When set to 1, disables selected 2Eh/2Fh or 4Eh/4Fh addresses acknowledged on LPC, and prevents any I/O transaction to PC8374L device. The bit disables the PC8374L 2Eh/2Fh or 4Eh/4Fh I/O mapping only when MEMEN, LDMEMEN and CFGMEMEN bits are all set to 1. 0: The 2Eh/2Fh or 4Eh/4Fh I/O mapping is enabled (default) 1: The 2Eh/2Fh or 4Eh/4Fh I/O mapping is disabled
1	R/W or RO	**LDMEMEN (Enable Memory Mapping of Logical Devices Configuration Registers).** When set to 1, enables the memory mapping of Logical Devices Configuration registers (I/O index 30h-FFh). When cleared, all Logical Devices Configuration registers are I/O mapped. The bit enables memory mapping only when MEMEN bit is set to 1. 0: All Logical Devices Configuration registers are I/O mapped (default) 1: All Logical Devices Configuration registers are Memory mapped **Note:** When this bit is 1 (and MEMEN is 1), I/O mapping of the Logical Devices Configuration registers is still enabled (in addition to the memory mapping) when BIODIS is 0 or CFGMEMEN is 0.
0	R/W or RO	**CFGMEMEN (Enable Memory Mapping of Control and Configuration Registers).** When set to 1, enables the memory mapping of device control and configuration registers (I/O index 10h-2Fh). When cleared, the device control and configuration registers are I/O mapped. The bit enables memory mapping only when MEMEN bit is set to 1. 0: All control and configuration registers are I/O mapped (default). 1: All control and configuration registers are Memory mapped. **Note:** When this bit is 1 (and MEMEN is 1), I/O mapping of the device control and configuration registers is still enabled (in addition to the memory mapping) when BIODIS is 0 or LDMEMEN is 0.

3.0 Device Architecture and Configuration (Continued)

3.7.2 Memory Base Address Register 1 (MEMADR1)

Power Well: V_{DD3}
Location: Index 12h
Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Memory Base Address 1**							
Reset	00							

Bit	Description
7-0	**Memory Base Address 1.** This register indicates selected Memory Base address bits 23-16.

3.7.3 Memory Base Address Register 2 (MEMADR2)

Power Well: V_{DD3}
Location: Index 13h
Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**TYPESEL**	**MEMFWHID**				**Memory Base Address 2**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**TYPESEL (Transaction Type Select).** Selects the transaction type decoded for memory addresses. For address decoding of the Memory Base address, bit 31 value is 1 regardless of TYPESEL value, thus limiting the Memory Base Address to high 2G memory space. 0: Transactions type is LPC Memory Read/Write (default) 1: Transactions type is LPC FWH Memory Read/Write
6-3	**MEMFWHID (Memory FWH ID).** • When TYPESEL is 0: Indicates selected Memory Base address bits 30-27. • When TYPESEL is 1: indicates the IDSEL of the Firmware Memory transactions to which the PC8374L responds. The least significant bit of this field is also used as Memory Base address bit 27.
2-0	**Memory Base Address 2.** Indicates selected Memory Base address bits 26-24.

3.7.4 SuperI/O ID Register (SID)

This register contains the identity number of the device family. The PC8374L family is identified by the value F1.

Power Well: V_{SB3}
Location: Index 20h
Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Family ID**							
Reset	F1							

Bit	Description
7–0	**Family ID.** Identifies a family of devices with similar functionality but with different implemented options.

3.0 Device Architecture and Configuration (Continued)

3.7.5 SuperI/O Configuration 1 Register (SIOCF1)

Power Well: V_{DD3}

Location: Index 21h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKMCF**	**LOCKGCF**	**Reserved**		**IOWAIT**		**SWRST**	**GLOBEN**
Reset	0	0	0	1	0	0	0	1

Bit	Type	Description
7	R/W1S	**LOCKMCF (Lock Multiplexing Configuration).** When set to 1, locks itself, IOWAIT field in SIOCF1 register, and registers SIOCF2, SIOCF3 and SIOCF4 by disabling writing to all bits in these registers. Once set, the bit can be cleared by Hardware reset. 0: R/W bits are enabled for write (default) 1: All bits are RO
6	R/W1S	**LOCKGCF (Lock GPIO Pins Configuration).** When set to 1,locks the configuration registers of all GPIO pins (see Section 3.14.2 on page 74) by disabling writes to all their bits (including the LOCKGCF bit itself). The locked registers include the GPCFG1 (except LOCKCFP bit), GPEVR, GPCFG2 and GPMODE registers of all GPIO pins. Once set, this bit can be cleared by Hardware reset. 0: R/W bits are enabled for write (default) 1: All bits are RO
5-4		**Reserved.**
3-2	R/W or RO	**IOWAIT (Number of I/O Wait States).** Sets the number of wait states for I/O transactions through the LPC bus. **Bits 3 2 Number of Wait States** 0 0: 0 (default) 0 1: 2 1 0: 6 1 1: 12
1	R/W	**SWRST (Software Reset).** When set to 1, triggers the Software reset sequence (see Section 2.2.5 on page 36), after which it returns to 0. Read always returns 0. The bit is not influenced by the value of LOCKMCF. 0: Inactive (default) 1: Trigger the Software reset sequence
0	R/W or RO	**GLOBEN (Global Device Enable).** Enables the disabling of all logical devices by changing a single bit (to 0). In addition, when the bit is set to 1, it enables the operation of all the logical devices of the PC8374L, as long as the logical device is itself enabled (see Table 9 on page 39). The behavior of the different devices is explained in Section 3.3 on page 48. 0: All logical devices in the PC8374L device are forced to be disabled and their resources are released. 1: Enables each PC8374L logical device that is itself enabled (default); see Section 3.3.1 on page 48.

3.0 Device Architecture and Configuration (Continued)

3.7.6 SuperI/O Configuration 2 Register (SIOCF2)

Power Well: V_{SB3}

Location: Index 22h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**PMEPOL**	**PMETYPE**	**TACH2EN**	**TACH1EN**	**Reserved**	**TACH4EN**	**TACH3EN**	**GPIO03EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**PMEPOL ($\overline{\text{SIOPME}}$ Polarity).** Selects the polarity of the $\overline{\text{SIOPME}}$ signal. 0: $\overline{\text{SIOPME}}$ is active low (default) 1: $\overline{\text{SIOPME}}$ is active high
6	**PMETYPE ($\overline{\text{SIOPME}}$ Buffer Type).** Selects the output buffer type of the $\overline{\text{SIOPME}}$ pin. 0: Output is open-drain and the pull-up resistor is enabled (default) 1: Output is push-pull (the pull-up resistor is disabled)
5	**TACH2EN (FANTACH2 Multiplex Control).** Selects the function connected to pin GPIOE07/FANTACH2. 0: GPIOE07 port: GPIO (default) 1: FANTACH2: Health Management For correct selection of the GPIO on this pin, also see Table 3 on page 18.
4	**TACH1EN (FANTACH1 Multiplex Control).** Selects the function connected to pin GPIOE06/FANTACH1. 0: GPIOE06 port: GPIO (default) 1: FANTACH1: Health Management For correct selection of the GPIO on this pin, also see Table 3 on page 18.
3	**Reserved.**
2	**TACH4EN (FANTACH4 Multiplex Control).** Selects the function connected to the GPIOE02/FANTACH4 pin. 0: GPIOE02 port: GPIO (default) 1: FANTACH4: Health Management For correct selection of the GPIO on this pin, also see Table 3 on page 18.
1	**TACH3EN (FANTACH3 Multiplex Control).** Selects the function connected to the GPIOE01/FANTACH3 pin. 0: GPIOE01 port: GPIO (default) 1: FANTACH3: Health Management For correct selection of the GPIO on this pin, also see Table 3 on page 18.
0	**GPIO03EN (GPIOE10-GPIOE13 Multiplex Control).** Selects the functions connected to pins 113-116. 0: 5V_DDCSDA, 5V_DDCSCL, CC_DDCSDA, CC_DDCSCL: Glue Functions (default) 1: GPIOE10-GPIOE13 ports: GPIO For correct selection of GPIOs on these pins, also see Table 3 on page 18.

3.0 Device Architecture and Configuration (Continued)

3.7.7 SuperI/O Configuration 3 Register (SIOCF3)

Power Well: Varies per bit

Location: Index 23h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**PWM3EN**	**PWM2EN**	**PWM1EN**	**Reserved**		**373COMP**	**SP2EN**	**IREN**
Reset	0	0	0	0	0	0	0	0
Power Well	V_{BAT}[1]	V_{BAT}[1]	V_{BAT}[1]	V_{SB3}	V_{BAT}[1]	V_{SB3}	V_{SB3}	V_{SB3}

1. See Sections 2.1 and 2.2

Bit	Description
7	**PWM3EN (FANPWM3 Multiplex Control).** Selects the function connected to the GPIOE05/FANPWM3 pin. 0: GPIOE05 port: GPIO (default) 1: FANPWM3: Health Management For correct selection of this GPIO on this pin, also see Table 3 on page 18.
6	**PWM2EN (FANPWM2 Multiplex Control).** Selects the function connected to the GPIOE04/FANPWM2 pin. 0: GPIOE04 port: GPIO (default) 1: FANPWM2: Health Management For correct selection of this GPIO on this pin, also see Table 3 on page 18.
5	**PWM1EN (FANPWM1 Multiplex Control).** Selects the function connected to the GPIOE03/FANPWM1 pin. 0: GPIOE03 port: GPIO (default) 1: FANPWM1: Health Management For correct selection of this GPIO on this pin, also see Table 3 on page 18.
4-3	**Reserved.**
2	**373COMP (PC87373 Compatibility Mode).** Selects Serial Port 2 and InfraRed Port pinout. **Signal Name** — **373COMP Pinout** — **Bit = 0** — **Bit = 1** $\overline{RI2}$ — 118 — 119 SIN2 — 119 — 121 SOUT2 — 120 — 122 $\overline{DSR2}$ — 121 — 124 $\overline{RTS2}$ — 122 — 125 $\overline{CTS2}$ — 124 — 126 $\overline{DTR}$_BOUT2 — 125 — 127 $\overline{DCD2}$ — 126 — 128 IRRX — 127 — 120 IRTX — 128 — 118
1	**SP2EN (Serial Port 2 Multiplex Control).** Selects either GPIO or Serial Port 2. 0: Selects the following GPIO signals: GPIOE01, GPIOE03, GPO12, GPIOE04, GPO13, GPIOE05 **and**: — when 373COMP bit = 0: GPIOE00, GPIOE02 — when 373COMP bit = 1: GPIOE06, GPIOE07 1: Selects Serial Port 2 signals For correct selection of GPIOs on these pins, also see Table 3 on page 18.
0	**IREN (InfraRed Multiplex Control).** Selects InfraRed Port or GPIO. 0: GPIOE02, GPIOE00 (when 373COMP bit is 1) **or** GPIOE06, GPIOE07 (when 373COMP bit is 0) (default) 1: IRRX, IRTX signals For correct selection of GPIOs on these pins, also see Table 3 on page 18.

3.0 Device Architecture and Configuration (Continued)

3.7.8 SuperI/O Configuration 4 Register (SIOCF4)

Power Well: V_{SB3}

Location: Index 24h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**nSWD**	**Reserved**		**nPCIRSTO2**	**Reserved**			**VddStrap2**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**nSWD (SingleWire Data Multiplex Control).** Selects SWD or GPIO. 0: SWD: Health Management (default) 1: GPIOE00 For correct selection of the GPIO on this pin, also see Table 3 on page 18.
6	**Reserved.** Must be written with 1 to have GPIO or FANTACH4 functionality on pin 105.
5	**Reserved.**
4	**nPCIRSTO2 (PCI Reset Out 2 Multiplex Control).** Selects $\overline{\text{PCIRST\_OUT2}}$ or GPIO. 0: $\overline{\text{PCIRST\_OUT2}}$: Glue Functions (default) 1: GPIOE12 For correct selection of the GPIO on this pin, also see Table 3 on page 18. **Note:** When using GPIOE12, check that its respective default function fits the system usage of this GPIO. Failing to do so may result in irreversible damage to the chip.
3-1	**Reserved.**
0	**VddStrap2.** VddStrap2 strap pin Status. Read-Only bit. The bit holds the sampled VddStrap2 pin value at V_{DD3} power up.

3.7.9 SuperI/O Configuration 6 Register (SIOCF6)

This register provides a fast way to disable one or more modules without having to access the Activate register of each (see Section 3.3.1 on page 48).

Power Well: V_{DD3}

Location: Index 26h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKFDS**	**General-Purpose Scratch**		**Reserved**	**SER1DIS**	**SER2DIS**	**PARPDIS**	**FDCDIS**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W1S	**LOCKFDS (Lock Fast Disable Configuration).** When set to 1, locks itself, SER1DIS, SER2DIS, PARPDIS and FDCDIS bits in this register and GLOBEN bit in SIOCF1 register by disabling writing to all of these bits. Once set, this bit can be cleared by Hardware reset. 0: R/W bits are enabled for write (default) 1: All bits (except bits 6-5) are RO
6-5	R/W	**General-Purpose Scratch.**
4		**Reserved.**

3.0 Device Architecture and Configuration (Continued)

Bit	Type	Description
3	R/W or RO	**SER1DIS (Serial Port 1 Disable).** When set to 1, forces the Serial Port 1 module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
2	R/W or RO	**SER2DIS (Serial Port 2 Disable).** When set to 1, forces the Serial Port 2 with InfraRed Port module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
1	R/W or RO	**PARPDIS (Parallel Port Disable).** When set to 1, forces the Parallel Port module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
0	R/W or RO	**FDCDIS (Floppy Disk Controller Disable).** When set to 1, forces the Floppy Disk Controller module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled

3.7.10 SuperI/O Revision ID Register (SRID)

This register contains the ID number of the specific family member (Chip ID) and the chip revision number (Chip Rev). The PC8374L is identified by the value '000'. The Chip Rev is incremented on each revision.

Power Well: V_{SB3}

Location: Index 27h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Chip ID**			**Chip Rev**				
Reset	0	0	0	X	X	X	X	X

Bit	Description
7-5	**Chip ID.** Identifies a specific device of a family.
4-0	**Chip Rev.** Identifies the device revision.

3.0 Device Architecture and Configuration (Continued)

3.7.11 Clock Generator Control Register (CLOCKCF)

Power Well: Varies per bit

Location: Index 29h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCK**	**Reserved**		**CKVALID**	**Reserved**			
Reset	0	0	0	0	0	0	0	1
Power Well	V_{SB3}	V_{SB3}	V_{SB3}	V_{SB3}	V_{SB3}	V_{SB3}	V_{SB3}	V_{BAT}[1]

1. See Sections 2.1 and 2.2

Bit	Type	Description
7	R/W1S	**LOCK (Lock Enable).** When set to 1, locks the configuration register CLOCKCF by disabling writing to all its bits (including to the LOCK bit itself). Once set, this bit can be cleared by Hardware reset. 0: The R/W bits are enabled for write (default) 1: All the bits are RO
6-5		**Reserved.**
4	RO	**CKVALID (Valid Clock Generator, Clock Status).** Indicates the status of the on-chip Clock Generator and controls the generator output clock signal. The PC8374L modules residing on the 48 MHz clock domain may be enabled (see Section 3.3.1 on page 48) only after this bit is read high (generator clock is valid). 0: On first V_{DD3} power-up (after V_{SB3} power-up): Generator output clock frozen (default); On any other V_{DD3} power-up: only 48 MHz clock domain frozen (default). 1: All generator output clocks active (stable and toggling).
3-0		**Reserved.**
0		**Reserved.** Must be written with 1.

3.7.12 Health Management SMBus Configuration (HMSMBCF) Register

This register may be written only once. All eight bits must be updated in a single write operation, after which the data in the register becomes read-only. The register is reset only by V_{SB} Power-Up reset following battery loss. The write lock is released on any V_{SB} Power-Up reset.

Power Well: V_{BAT} (See Sections 2.1 and 2.2)

Location: Index 2Ah

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**HM_SMBSADD**						
Reset	0	0	1	0	1	1	1	0

Bit	Description
7	**Reserved.**
6-0	**HM_SMBSADD (Health Management SMBus Slave Address).** Defines the slave address on the HM SMBus for the PC8374L. This address, once programmed by the host, is preserved as long as the V power is active. The 7-bit slave address is used to access the Health Management module of the PC8374L. A non-zero value read from this field indicates that HM_SMBSADD contains a valid slave address. **Section 8.4.1 on page 142**

3.0 Device Architecture and Configuration (Continued)

3.8 FLOPPY DISK CONTROLLER (FDC) CONFIGURATION

3.8.1 General Description

The generic FDC is a standard FDC with a digital data separator and is DP8473 and N82077 software compatible. The PC8374L FDC supports 14 of the 17 standard FDC signals described in the generic Floppy Disk Controller (FDC) chapter, including the following (see Section 9.1 on page 192):

- FM and MFM modes are supported.
- A logic 1 is returned during LPC I/O read cycles by all register bits reflecting the state of floating (TRI-STATE) FDC pins.

Exceptions to standard FDC are:

- Automatic media sense using MSEN0 and MSEN1 signals is not supported.
- DRATE1 is not supported.
- $\overline{DR1}$ is not supported.
- $\overline{MTR1}$ is not supported.

The FDC functional block registers are shown in Section 9.1 on page 192. All of these registers are V_{DD3} powered.

3.8.2 Logical Device 0 (FDC) Configuration

Table 22 lists the configuration registers that affect the FDC. Only the last two registers (F0h and F1h) are described here. See Section 3.2.3 on page 39 for descriptions of the other configuration registers. All of these registers are V_{DD3} powered.

Table 22. FDC Configuration Register

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 48).	R/W	V_{DD3}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read-only, ‘00000’.	R/W	V_{DD3}	03h
61h	Base Address LSB register. Bits 2 and 0 (for A2 and A0) are read-only, ‘00’.	R/W	V_{DD3}	F2h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD3}	06h
71h	Interrupt Type. Bit 1 is read/write; other bits are read-only.	R/W	V_{DD3}	03h
74h	DMA Channel Select.	R/W	V_{DD3}	02h
75h	Report no second DMA assignment.	RO	V_{DD3}	04h
F0h	FDC Configuration register.	R/W	V_{DD3}	24h
F1h	Drive ID register.	R/W	V_{DD3}	00h
F8h	FDC Configuration register (mirror of the register at index F0h).	R/W	V_{DD3}	24h

3.0 Device Architecture and Configuration (Continued)

3.8.3 FDC Configuration Register

This register is reset to 24h.

Power Well: V_{DD3}

Location: Indexes F0h and F8h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TDR Register Mode**	**DENSEL Polarity Control**	**FDC 2Mbps Enable**	**Write Protect**	**PC-AT or PS/2 Drive Mode Select**	**Reserved**	**TRI-STATE Control**
Reset	0	0	1	0	0	1	0	0

Bit	Type	Description
7		**Reserved.**
6	R/W	**TDR Register Mode.** 0: PC-AT-Compatible Drive mode; i.e., bits 7-2 of the TDR are '111111' (default) 1: Enhanced Drive mode
5	R/W	**DENSEL Polarity Control.** 0: Active low for 500 Kbps or 1 or 2 Mbps data rates 1: Active high for 500 Kbps or 1 or 2 Mbps data rates (default)
4	R/W	**FDC 2Mbps Enable.** Is set only when a 2 Mbps drive is used. 0: 2 Mbps disabled and the FDC clock is 24 MHz (default) 1: 2 Mbps enabled and the FDC clock is 48 MHz
3	R/W	**Write Protect.** Enables forcing of write protect functionality by software. When set, writes to the floppy disk drive are disabled. This effect is identical to an active $\overline{WP}$ signal. 0: Write protected according to $\overline{WP}$ signal (default) 1: Write protected regardless of value of $\overline{WP}$ signal
2	R/W	**PC-AT or PS/2 Drive Mode Select.** 0: PS/2 Drive mode 1: PC-AT Drive mode (default)
1		**Reserved.**
0	R/W	**TRI-STATE Control.** When this bit is set to 1 and the logical device is inactive, the logical device output pins are in TRI-STATE (see Section 3.3.2 on page 48). 0: Normal outputs (default) 1: TRI-STATE outputs when the logical device is inactive

3.0 Device Architecture and Configuration (Continued)

3.8.4 Drive ID Register

This register is reset to 00h. This register controls bits 5 and 4 of the TDR register in Enhanced mode.

Power Well: V_{DD3}
Location: Index F1h
Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**						**Drive 0 ID**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-2	**Reserved.**
1-0	**Drive 0 ID.** When drive 0 is accessed, these bits are reflected on bits 5-4 of the TDR register, respectively.

Usage Hints: Some BIOS implementations support FDDs with automatic media sense; in this case, bit 5 of TDR register in Enhanced mode is interpreted as valid media sense when it is cleared to 0. If drive 0 and/or drive 1 do not support automatic media sense, bits 1 and/or 3 of the Drive ID register must be set to 1 (to indicate non-valid media sense). When Drive 0 or Drive 1 is selected, the Drive ID bit is reflected on bit 5 of TDR register in Enhanced mode.

3.0 Device Architecture and Configuration (Continued)

3.9 PARALLEL PORT (PP) CONFIGURATION

3.9.1 General Description

The PC8374L Parallel Port supports all IEEE1284 standard communication modes: Compatibility (also known as Standard or SPP), Bi-directional (known also as PS/2), FIFO, EPP (also known as mode 4) and ECP (with an optional Extended ECP mode).

The Parallel Port includes two groups of runtime registers (see Section 9.2 on page 194):

- A group of 21 registers at first level offset, sharing 14 entries. Three of these registers (at offsets 403h, 404h and 405h) are used only in Extended ECP mode.
- A group of four registers, used only in Extended ECP mode, is accessed by a second level offset.

The desired mode is selected by the ECR runtime register (offset 402h). The selected mode determines which runtime registers are used and which address bits are used for the base address. The Parallel Port functional block registers are shown in Section 9.2 on page 194. All of these registers are V_{DD3} powered.

3.9.2 Logical Device 1 (PP) Configuration

Table 23 lists the configuration registers that affect the Parallel Port. Only the last register (F0h) is described here. See Section 3.2.3 on page 39 for descriptions of the other configuration registers. All of these registers are V_{DD3} powered.

Table 23. Parallel Port Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 48).	R/W	V_{DD3}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read-only, '00000'. Bit 2 (for A10) must be '0'.	R/W	V_{DD3}	02h
61h	Base Address LSB register. Bits 1 and 0 (A1 and A0) are read-only, '00'. For ECP mode 4 (EPP) or when using Extended registers, bit 2 (A2) must also be '0'.	R/W	V_{DD3}	78h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD3}	07h
71h	Interrupt Type: - Bits 7-2 are read-only. - Bit 1 is a read/write bit. - Bit 0 is read-only. It reflects the interrupt type dictated by the Parallel Port operation mode. The bit is set to 1 (level interrupt) in Extended mode and cleared (edge interrupt) in all other modes.	R/W	V_{DD3}	02h
74h	DMA Channel Select.	R/W	V_{DD3}	04h
75h	Report no second DMA assignment.	RO	V_{DD3}	04h
F0h	Parallel Port Standard Configuration register.	R/W	V_{DD3}	F2h
F8h	Parallel Port Modified Configuration register.	R/W	V_{DD3}	07h

3.0 Device Architecture and Configuration (Continued)

3.9.3 Parallel Port Standard Configuration Register

This register is reset to F2h.

Power Well: V_{DD3}

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Parallel Port Mode Select**			**Extended Register Access**	**Reserved**		**Power Mode Control**	**TRI-STATE Control**
Reset	1	1	1	1	0	0	1	0

Bit	Description
7-5	**Parallel Port Mode Select.** The mode selected by writing to these bits is reflected by bits 3-0 in the Parallel Port Modified Configuration Register (see Section 3.9.4 on page 65). **Bits 7 6 5 Mode** 0 0 0: SPP-Compatible mode. PD7-0 are always output signals 0 0 1: SPP Extended mode. PD7-0 direction is controlled by software 0 1 0: EPP 1.7 mode 0 1 1: EPP 1.9 mode 1 0 0: ECP mode (IEEE1284 register set), with no support for EPP mode 1 0 1: Reserved 1 1 0: Reserved 1 1 1: ECP mode (IEEE1284 register set), with EPP mode selectable as mode “100” (default) Selection of EPP 1.7 or 1.9 in ECP mode “100” is controlled by bit 4 of the Control2 configuration register of the Parallel Port at offset 02h. **Note:** Before setting bits 7-5, enable the Parallel Port and set CTR/DCR (at base address + 2) to C4h.
4	**Extended Register Access.** 0: Registers at base (address) + 403h, base + 404h and base + 405h are not accessible (reads and writes are ignored) 1: Registers at base (address) + 403h, base + 404h and base + 405h are accessible. This option supports runtime configuration within the Parallel Port address space (default).
3-2	**Reserved.**
1	**Power Mode Control.** When the logical device is active: 0: Parallel Port clock disabled. ECP modes and EPP time-out are not functional when the logical device is active. Registers are maintained. 1: Parallel Port clock enabled. All operation modes are functional when the logical device is active (default).
0	**TRI-STATE Control.** When this bit is set to 1 and the logical device is inactive, the logical device output pins are in TRI-STATE (see Section 3.3.2 on page 48). 0: Normal outputs (default) 1: TRI-STATE outputs when the logical device is inactive

3.0 Device Architecture and Configuration (Continued)

3.9.4 Parallel Port Modified Configuration Register

This register is reset to 07h.

Power Well: V_{DD3}

Location: Index F8h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**Parallel Port Mode Select**			
Reset	0	0	0	0	0	1	1	1

Bit	Description
7-4	**Reserved.**
3-0	**Parallel Port Mode Select.** The mode selected by writing to these bits is reflected by bits 7-5 in the Parallel Port Standard Configuration Register (see Section 3.9.3 on page 64). **Bits 3 2 1 0 Mode** 0 0 0 1: SPP Extended mode. PD7-0 direction is controlled by software 0 0 1 0: EPP 1.9 mode 0 1 0 0: ECP mode (IEEE1284 register set), with no support for EPP mode 1 0 0 0: SPP-Compatible mode. PD7-0 are always output signals 0 1 1 1: ECP mode (IEEE1284 register set), with EPP mode selectable as mode “0100” (default) 1 0 1 0: EPP 1.7 mode Other: Reserved (writing a reserved value causes unpredictable behavior of the Parallel Port) Selection of EPP 1.7 or 1.9 in ECP mode “0100” is controlled by bit 4 of Control2 configuration register of the Parallel Port at offset 02h. **Note:** Before setting bits 3-0, enable the Parallel Port and set CTR/DCR (at base address + 2) to C4h.

3.0 Device Architecture and Configuration (Continued)

3.10 SERIAL PORT 2 WITH INFRARED CONFIGURATION

3.10.1 General Description

Serial Port 2 provides UART functionality by supporting serial data communication with remote peripheral device or modem. The functional blocks can function as a standard 16450 or 16550 or as an Extended UART.

Serial Port 2 includes four register banks, each containing eight runtime registers, as shown in Section 9.3 on page 196. All of these registers are V_{DD3} powered.

3.10.2 Logical Device 2 (SP2) Configuration

Table 24 lists the configuration registers that affect Serial Port 2. Only the last register (F0h) is described here. See Section 3.2.3 on page 39 for descriptions of the other configuration registers. All of these registers are V_{DD3} powered.

Table 24. Serial Port 2 with InfraRed Port Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 48).	R/W	V_{DD3}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read-only, 00000b.	R/W	V_{DD3}	02h
61h	Base Address LSB register. Bit 2-0 (for A2-0) are read-only, 000b.	R/W	V_{DD3}	F8h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD3}	03h
71h	Interrupt Type. Bit 1 is R/W; other bits are read-only.	R/W	V_{DD3}	03h
74h	DMA Channel Select 0 (RX_DMA).	R/W	V_{DD3}	04h
75h	DMA Channel Select 1 (TX_DMA).	R/W	V_{DD3}	04h
F0h	Serial Port 2 Configuration 1 register.	R/W	V_{DD3}	02h

3.0 Device Architecture and Configuration (Continued)

3.10.3 Serial Port 2 Configuration 1 Register

This register is reset to 02h.

Power Well: V_{DD}

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Bank Select Enable**	**Reserved**				**Busy Indicator**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable**. Enables bank switching for Serial Port 2. 0: All attempts to access the extended registers in Serial Port 2 are ignored (default) 1: Enables bank switching for Serial Port 2
6-3	**Reserved.**
2	**Busy Indicator.** This read-only bit can be used by power management software to decide when to power-down the Serial Port 2 logical device. 0: No transfer in progress (default) 1: Transfer in progress
1	**Power Mode Control.** The logical device can be active in two modes: 0: Low Power mode: When the logical device is active in Low Power mode, - The Serial Port 2 clock is disabled. - The output signals are set to their default states. - The $\overline{RI}$ input signal can be programed to generate an interrupt. - Registers are maintained (unlike the activation bit in Index 30h, which also prevents access to Serial Port 2 registers). 1: Normal Power mode: When the logical device is active in Normal Power mode, - Serial Port 2 clock enabled. - Serial Port 2 is functional when the logical device is active (default).
0	**TRI-STATE Control.** When this bit is set to 1 and the logical device is inactive, the logical device output pins are in TRI-STATE (see Section 3.3.2 on page 48). Exception to this is the IRTX pin, which is driven to 0 when InfraRed is inactive and is not affected by this bit. 0: Normal outputs (default) 1: TRI-STATE outputs when the logical device is inactive

3.0 Device Architecture and Configuration (Continued)

3.11 SERIAL PORT 1 CONFIGURATION

3.11.1 General Description

Serial Port 1 provides UART functionality by supporting serial data communication with a remote peripheral device or a modem. The functional blocks can function as a standard 16450 or 16550 or as an Extended UART.

Serial Port 1 includes four register banks, each containing eight runtime registers, as shown in Section 9.3 on page 196. All registers are V_{DD3} powered.

3.11.2 Logical Device 3 (SP1) Configuration

Table 25 lists the configuration registers that affect Serial Port 1. Only the last register (F0h) is described here. See Section 3.2.3 on page 39 for descriptions of the other configuration registers. All of these registers are V_{DD3} powered.

Table 25. Serial Port 1 Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 48).	R/W	V_{DD3}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read-only, '00000'.	R/W	V_{DD3}	03h
61h	Base Address LSB register. Bits 2-0 (for A2-0) are read-only, '000'.	R/W	V_{DD3}	F8h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD3}	04h
71h	Interrupt Type. Bit 1 is R/W; other bits are read-only.	R/W	V_{DD3}	03h
74h	Report no DMA Assignment.	RO	V_{DD3}	04h
75h	Report no DMA Assignment.	RO	V_{DD3}	04h
F0h	Serial Port 1 Configuration register.	R/W	V_{DD3}	02h

3.0 Device Architecture and Configuration (Continued)

3.11.3 Serial Port 1 Configuration Register

This register is reset to 02h.

Power Well: V_{DD3}

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Bank Select Enable**	**Reserved**				**Busy Indicator**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable**. Enables bank switching for Serial Port 1. 0: All attempts to access the extended registers in Serial Port 1 are ignored (default) 1: Enables bank switching for Serial Port 1
6-3	**Reserved.**
2	**Busy Indicator.** This read-only bit can be used by power management software to decide when to power down the Serial Port 1 logical device. 0: No transfer in progress (default) 1: Transfer in progress
1	**Power Mode Control.** The logical device can be active in two modes: 0: Low Power mode: When the logical device is active in Low Power mode, - The Serial Port 1 clock is disabled. - The output signals are set to their default states. - The $\overline{RI}$ input signal can be programed to generate an interrupt. - Registers are maintained (unlike the activation bit in Index 30h, which also prevents access to the Serial Port 1 registers). 1: Normal Power mode: When the logical device is active in Normal Power mode, - Serial Port 1 clock enabled. - Serial Port 1 is functional when the logical device is active (default).
0	**TRI-STATE Control.** When this bit is set to 1 and the logical device is inactive, the logical device output pins are in TRI-STATE (see Section 3.3.2 on page 48). 0: Normal outputs (default) 1: TRI-STATE outputs when the logical device is inactive

3.0 Device Architecture and Configuration (Continued)

3.12 SYSTEM WAKE-UP CONTROL (SWC) CONFIGURATION

3.12.1 General Description

System Wake-Up Control provides wake-up and power management functionality according to the ACPI specification (see Section 4.1 on page 81). Its registers are V_{SB3} powered.

3.12.2 Logical Device 4 (SWC) Configuration

Table 26 lists the configuration registers that affect the SWC. See Section 3.2.3 on page 39 for a detailed description of these registers. All of these registers are V_{DD3} powered.

Table 26. System Wake-Up Control (SWC) Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate. When bit 0 is cleared, the runtime registers of this logical device are not accessible (see Section 3.3.1 on page 48).[1]	R/W	V_{DD3}	00h
50h	Memory Base Descriptor.	R/W	V_{DD3}	00h
60h	SWC Base Address MSB register.	R/W	V_{DD3}	00h
61h	SWC Base Address LSB register. Bits 3-0 (for A3-0) are read-only, ‘0000’.	R/W	V_{DD3}	00h
62h	GPE1_BLK Base Address MSB register.	R/W	V_{DD3}	00h
63h	GPE1_BLK Base Address LSB register. Bits 3-0 (for A3-0) are read-only, ‘0000’.	R/W	V_{DD3}	00h
70h	Interrupt Number.	R/W	V_{DD3}	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read-only.	R/W	V_{DD3}	03h
74h	Report no DMA assignment.	RO	V_{DD3}	04h
75h	Report no DMA assignment.	RO	V_{DD3}	04h

1. The logical device runtime registers are maintained and all wake-up detection mechanisms are functional.

3.0 Device Architecture and Configuration (Continued)

3.13 KEYBOARD AND MOUSE CONTROLLER (KBC) CONFIGURATION

3.13.1 General Description

The KBC is implemented physically as a single hardware module and houses two separate logical devices: a Mouse controller (Logical Device 5) and a Keyboard controller (Logical Device 6). The KBC is functionally equivalent to the industry standard 8042A Keyboard controller. Technical references for the standard 8042A Keyboard Controller may serve as detailed technical references for the KBC.

The Keyboard and Mouse Controller runtime registers are described in Section 9.5 on page 206. All registers are V_{DD3} powered.

3.13.2 Logical Devices 5 and 6 (Mouse and Keyboard) Configuration

Tables 27 and 28 list the configuration registers that affect the Mouse and Keyboard logical devices. Only the last register (F0h) is described here. See Section 3.2.3 on page 39 for descriptions of the other configuration registers. The KBC module is activated and the access to the runtime registers (pointed at by the base addresses at indexes 60h-63h) is enabled when either the Mouse logical device (5) or the Keyboard logical device (6) is activated (by setting the activation bit at index 30h). Because the IRQ configuration resources are separate for each logical device (Mouse or Keyboard), the specific logical device must be activated to enable its IRQ resources. All of these registers are V_{DD3} powered, with the exception of the KBC Configuration register (F0h), which is both V_{DD3} and V_{SB3} powered.

Table 27. Mouse Configuration Registers

Index	Mouse Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.2.3 on page 39). When the Mouse of the KBC is inactive, the IRQ selected by the Mouse Interrupt Number and Wake-Up on IRQ Enable register (index 70h) are not asserted.	R/W	V_{DD3}	00h
70h	Mouse Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD3}	0Ch
71h	Mouse Interrupt Type. Bits 1,0 are read/write; other bits are read-only.	R/W	V_{DD3}	02h
74h	Report no DMA assignment.	RO	V_{DD3}	04h
75h	Report no DMA assignment.	RO	V_{DD3}	04h

Table 28. Keyboard Configuration Registers

Index	Keyboard Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.2.3 on page 39). When the Keyboard of the KBC is inactive, the IRQ selected by the Keyboard Interrupt Number and Wake-Up on IRQ Enable register (index 70h) are not asserted.	R/W	V_{DD3}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read-only, '00000'.	R/W	V_{DD3}	00h
61h	Base Address LSB register. Bits 2-0 (for A2-0) are read-only, '000'.	R/W	V_{DD3}	60h
62h	Command Base Address MSB register. Bits 7-3 (for A15-11) are read-only, '00000'.	R/W	V_{DD3}	00h
63h	Command Base Address LSB. Bits 2-0 (for A2-0) are read-only, '100'.	R/W	V_{DD3}	64h
70h	KBD Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD3}	01h
71h	KBD Interrupt Type. Bits 1,0 are read/write; others are read-only.	R/W	V_{DD3}	02h
74h	Report no DMA assignment.	RO	V_{DD3}	04h
75h	Report no DMA assignment.	RO	V_{DD3}	04h
F0h	KBC Configuration register.	R/W	V_{DD3}/V_{SB3}	40h

3.0 Device Architecture and Configuration (Continued)

3.13.3 KBC Configuration Register

This register is reset to 40h.

Power Well: V_{DD3} and V_{SB3} (see Note 1)

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**KBC Clock Source**		**Reserved**		**SWAP**[1]	**Reserved**		**TRI-STATE Control**
Reset	0	1	0	0	0	0	0	0

1. This bit is powered from the V_{SB3} well and is reset by V_{SB3} Power-Up reset.

Bit	Description
7-6	**KBC Clock Source.** The clock source can be changed only when the KBC is inactive (disabled). **Bits 7 6 Source** 0 0: 8 MHz 0 1: 12 MHz (default) 1 0: 16 MHz 1 1: Reserved
5-4	**Reserved.**
3	**SWAP (Swap Keyboard and Mouse Inputs).** When this bit is set, the keyboard signals (KBCLK and KBDAT) are swapped with the mouse signals (MCLK and MDAT). This bit is used both by the KBC module and by the Keyboard/Mouse Wake-Up Detector in the SWC module. The bit is reset to the default value by V_{SB3} Power-Up reset only. 0: No swapping (default) 1: Swaps the keyboard and mouse signals
2-1	**Reserved.**
0	**TRI-STATE Control**. When this bit is set, the Keyboard pins (KBCLK, KBDAT) and the Mouse pins (MCLK, MDAT) are in TRI-STATE (see Section 3.3.2 on page 48), if both the Keyboard and the Mouse logical devices are inactive. 0: Normal outputs (default) 1: TRI-STATE outputs when the Keyboard and the Mouse logical devices are inactive

Usage Hints:

1. To change the clock frequency of the KBC:
   a. Disable the KBC logical devices.
   b. Change the frequency setting.
   c. Enable the KBC logical devices.
2. Before swapping between the Keyboard and Mouse Interface pins, disable the KBC logical devices and their pins. After swapping, the software must issue a synchronization command to the Keyboard and Mouse through the KBC to regain synchronization with these devices.

3.0 Device Architecture and Configuration (Continued)

3.14 GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PORTS CONFIGURATION

3.14.1 General Description

The GPIO functional block includes 16 pins arranged in two ports:

- Port 0 contains eight GPIOE pins (i.e., GPIO pins with event detection).
- Port 1 contains seven GPIOE pin and one GPIO pin.

The two ports (excluding GPIO15) have full event detection capability, enabling them to trigger an IRQ and/or $\overline{SMI}$. In addition, through the SWC functional block, they can trigger the $\overline{SIOPME}$ signal.

A configuration option to route GPIOE16 input to GPIOE11 (or GPO11) output is supported. When enabled, GPIOE11 outputs the data appearing on GPIOE16, ignoring its data output register. For proper operation, GPIOE11 and GPIOE16 need both to be configured correctly. Undefined results otherwise.

The runtime registers associated with the ports are arranged in the GPIO address space as shown in Table 29. Each GPIO port with wake-up event detection capability has five runtime registers. The GPIO base address is 32-byte aligned. Address bits 4-0 are used to indicate the register offset.

The runtime registers implemented in the PC8374L devices are shown in Table 29. All of these registers are V_{SB3} powered.

Table 29. Runtime Registers in GPIO Address Space

Offset	Mnemonic	Register Name	Port	Power Well	Type	
					SEPDIO = 1	SEPDIO = 0
00h	GPDO0	GPIO Data Out 0	0	V_{SB3}	R/W	RO
01h	GPDI0	GPIO Data In 0		V_{SB3}	RO	RO
02h	GPEVEN0	GPIO Event Enable 0		V_{SB3}	R/W	RO
03h	GPEVST0	GPIO Event Status 0		V_{SB3}	R/W1C	RO
04h	GPDO1	GPIO Data Out 1	1	V_{SB3}	R/W	RO
05h	GPDI1	GPIO Data In 1		V_{SB3}	RO	RO
06h	GPEVEN1	GPIO Event Enable 1		V_{SB3}	R/W	RO
07h	GPEVST1	GPIO Event Status 1		V_{SB3}	R/W1C	RO
15h	GPDIO0	GPIO Data In/Out 0	0	V_{SB3}	R/W	R/W
16h	GPDIO1	GPIO Data In/Out 1	1	V_{SB3}	R/W	R/W

3.0 Device Architecture and Configuration (Continued)

3.14.2 Logical Device 7 (GPIO) Configuration

Table 30 lists the configuration registers that affect the GPIO. Only the last five registers (F0h-F3h and F8h) are described here. See Section 3.2.3 on page 39 for a detailed description of the other configuration registers. The standard configuration registers are powered by V_{DD3}; however, the specific configuration registers are powered by V_{SB3}.

Table 30. GPIO Configuration Register

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.2.3 on page 39).	R/W	V_{DD3}	00h
50h	Memory Base Descriptor.	R/W	V_{DD3}	00h
60h	Base Address MSB register.	R/W	V_{DD3}	00h
61h	Base Address LSB register. Bits 4-0 (for A4-0) are read-only, '00000'.	R/W	V_{DD3}	00h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD3}	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read-only.	R/W	V_{DD3}	03h
74h	Report no DMA assignment.	RO	V_{DD3}	04h
75h	Report no DMA assignment.	RO	V_{DD3}	04h
F0h	GPIO Pin Select register (GPSEL).	R/W	V_{SB3}	00h
F1h	GPIO Pin Configuration register 1 (GPCFG1).	Varies per bit	V_{SB3}	See text
F2h	GPIO Pin Event Routing register (GPEVR).	R/W or RO	V_{SB3}	00h
F3h	GPIO Pin Configuration register 2 (GPCFG2).	R/W or RO	V_{SB3}	See text
F8h	GPIO Mode Select register (GPMODE).	R/W or RO	V_{SB3}	01h

Figure 10 shows the organization of registers GPCFG1-2, GPEVR and GPMODE:

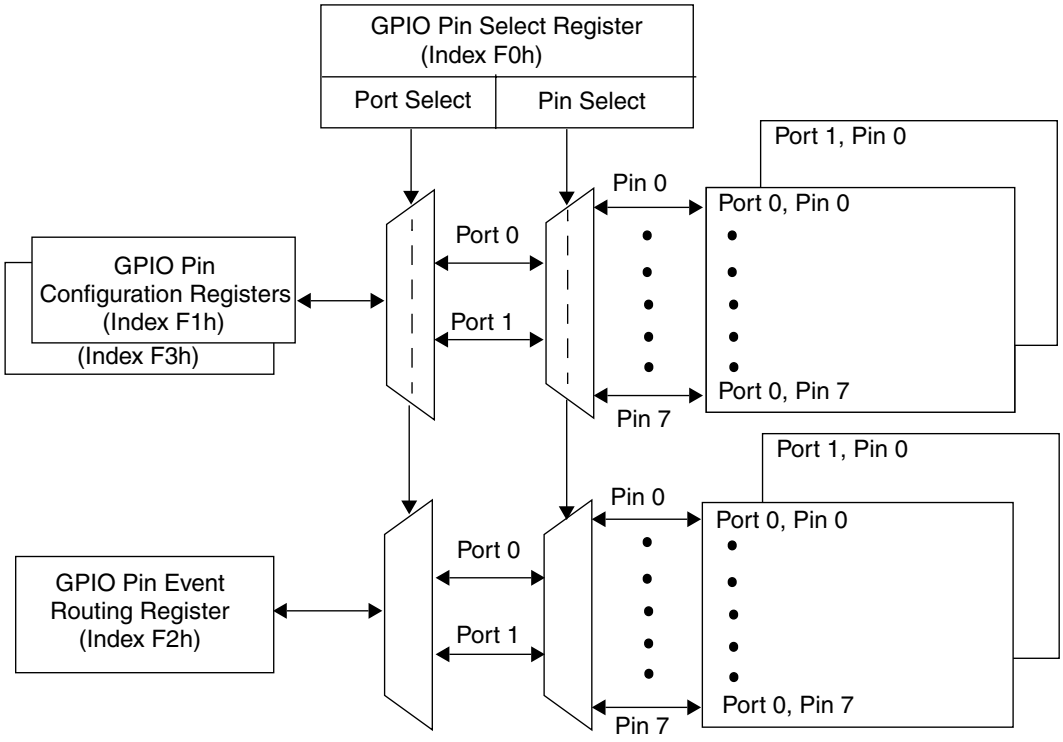


Figure 10. Organization of GPIO Pin Registers GPCFG1-2, GPEVR and GPMODE

3.0 Device Architecture and Configuration (Continued)

3.14.3 GPIO Pin Select Register (GPSEL)

This register selects the GPIO pin (port number and bit number) to be configured (i.e., which register is accessed via the GPIO pin configuration registers). GPSEL is reset to 00h.

Power Well: V_{SB3}

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**PORTSEL**			**Reserved**	**PINSEL**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved.**
6-4	**PORTSEL (Port Select).** Selects the GPIO port to be configured: **Bits** **6 5 4 Mode** 0 0 0: Port 0 (default) 0 0 1: Port 1 010-111: Reserved
3	**Reserved.**
2-0	**PINSEL (Pin Select).** Selects the GPIO pin of the selected port to be configured: **Bits** **2 1 0 Mode** 0 0 0: Pin 0 (default) 001-111: Binary value of pin numbers 1-7, respectively

3.14.4 GPIO Pin Configuration Register 1 (GPCFG1)

This register reflects, for both read and write, the register currently selected by the GPIO Pin Select register. All of the GPIO pin configuration registers have a common bit structure, as shown below.

Power Well: V_{SB3}

Location: Index F1h

Type: Varies per bit

Ports 0 to 1 (With Wake-Up Event Detection Capability)

Bit	7	6	5	4	3	2	1	0
Name	**PDNCTL**	**EVDBNC**	**EVPOL**	**EVTYPE**	**LOCKCFP**	**PUPCTL**	**OUTTYPE**	**OUTENA**
Reset	see Table 31	0	0	0	0	see Table 31	0	0

Bit	Type	Description
7	R/W or RO	**PDNCTL (Pull-Down Control).** Controls the internal pull-down resistor of the selected GPIO pin (see Section 6.2 on page 111). 0: Disabled (for default value, see Table 31) 1: Enabled (for default value, see Table 31) Undefined results when both the PDNCTL bit and the PUPCTL bit are set to 1.

3.0 Device Architecture and Configuration (Continued)

Bit	Type	Description
6	R/W or RO	**EVDBNC (Event Debounce Enable).** Enables the debounce circuit in the event input path of the selected GPIO pin. The event is detected after a predetermined debouncing period (see Section 6.3 on page 113). 0: Disabled (default) 1: Enabled Reserved for Port 1, Pin 5.
5	R/W or RO	**EVPOL (Event Polarity).** Defines the polarity of the wake-up signal that issues an event from the selected GPIO pin (see Section 6.3 on page 113). 0: Falling edge or low level input (default) 1: Rising edge or high level input Reserved for Port 1, Pin 5.
4	R/W or RO	**EVTYPE (Event Type).** Defines the type of the wake-up signal that issues an event from the selected GPIO pin (see Section 6.3 on page 113). 0: Edge input (default) 1: Level input Reserved for Port 1, Pin 5.
3	R/W1S	**LOCKCFP (Lock Configuration of Pin).** When set to 1, locks the GPIO pin configuration and data (also see Section 6.4 on page 115) by disabling writing to itself, to GPCFG1 register bits PDNCTL, PUPCTL, OUTTYPE and OUTENA, to all of the bits of GPCFG2 register and to the corresponding bit in GPDO and GPDIO registers. Once set, this bit can be cleared by Hardware reset. 0: R/W bits are enabled for write (default) 1: All bits are RO
2	R/W or RO	**PUPCTL (Pull-Up Control).** Controls the internal pull-up resistor of the selected GPIO pin (see Section 6.2 on page 111). 0: Disabled (for default value, see Table 31) 1: Enabled (for default value, see Table 31) Undefined results when both the PDNCTL bit and the PUPCTL bit are set to 1.
1	R/W or RO	**OUTTYPE (Output Type).** Controls the output buffer type of the selected GPIO pin (see Section 6.2 on page 111). 0: Open-drain (default) 1: Push-pull
0	R/W or RO	**OUTENA (Output Enable).** Controls the output buffer of the selected GPIO pin (see Section 6.2 on page 111). 0: TRI-STATE (default) 1: Output buffer enabled

Table 31. Reset Values for PUPCTL and PDNCTL Bits

GP(I)O(E)*nn*	00	01-06	07	10	11-13	14	15-16	17
PUPCTL	0	1	0	0	1	0	0	1
PDNCTL	1	No Pull-Down	1	No Pull-Down		1	No Pull-Down	

3.0 Device Architecture and Configuration (Continued)

3.14.5 GPIO Event Routing Register (GPEVR)

This register reflects, for both read and write, the register currently selected by the GPIO Pin Select register. It enables the routing of the GPIO event (see Section 6.3.2 on page 114) to an IRQ and/or $\overline{SMI}$ signal. It is implemented for Ports 0 to 1, which have wake-up event detection capability. GPEVR is reset to 00h.

Power Well: V_{SB3}

Location: Index F2h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**						**EV2SMI**	**EV2IRQ**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-2	**Reserved.**
1	**EV2SMI (Event to SMI Routing).** Controls the routing of the event from the selected GPIO pin to $\overline{SMI}$ (see Section 6.3.2 on page 114). 0: Disabled (default) 1: Enabled
0	**EV2IRQ (Event to IRQ Routing).** Controls the routing of the event from the selected GPIO pin to IRQ (see Section 6.3.2 on page 114). 0: Disabled (default) 1: Enabled

3.14.6 GPIO Pin Configuration Register 2 (GPCFG2)

This register reflects, for both read and write, the register currently selected by the GPIO Pin Select register. It controls the connection of the GPIO pin to a V_{DD}-powered load.

Power Well: V_{SB3}

Location: Index F3h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**VDDLOAD**	**Reserved**			
Reset	0	0	0	see Table 32	0	0	0	0

Bit	Description
7-5	**Reserved.**
4	**VDDLOAD (V_{DD3}-Powered Load).** Indicates that the selected GPIO pin is connected to a device powered by V_{DD3}. When this bit is 1, the input and output buffers (including the internal pull-up/pull-down) of the selected GPIO pin are disabled whenever V_{DD3} power to the PC8374L device falls below a certain value (see Section 10.1.5 on page 213). 0: GPIO pin connected to a V_{SB3}-powered load (default): The configuration and data of the GPIO pin are reset by V_{SB3} Power-Up reset (see Section 2.2 on page 34). 1: GPIO pin connected to a V_{DD3}-powered load: The configuration (excepting the VDDLOAD bit) and data of the GPIO pin are reset by V_{DD} Power-Up reset, Hardware reset or Software reset (see Section 2.2 on page 34).
3-0	**Reserved.**

Table 32. Reset Values for VDDLOAD Bit

GP(I)O(E)*nn*	00	01-07	10	11-12	13-17
VDDLOAD	1	0	0	1	0

3.0 Device Architecture and Configuration (Continued)

3.14.7 GPIO Mode Select Register (GPMODE)

This register controls the operation mode of the GPIO runtime registers (see Section 6.1 on page 110). GPMODE is reset to 01h. It also enables routing of GPIOE16 input to GPIOE11 (or GPO11) output.

Power Well: V_{SB3}

Location: Index F8h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**GPIN2GPO**	**Reserved**						**SEPDIO**
Reset	0	0	0	0	0	0	0	1

Bit	Description
7	**GPIN2GPO.** Route GPIOE16 input pin to GPIOE11 (or GPO11) output pin. 0: Routing disabled (default) 1: Routing enabled
6-1	**Reserved.**
0	**SEPDIO (Separate Data I/O Select).** Selects the operation mode of the GPIO runtime registers by controlling the GPDO, GPEVEN and GPEVST runtime registers to read-only. 0: Common Data I/O mode (GPDO, GPEVEN and GPEVST registers are read-only, and data written to them is ignored) 1: Separate Data I/O mode (default)

3.0 Device Architecture and Configuration (Continued)

3.15 HEALTH MANAGEMENT (HM) CONFIGURATION

3.15.1 General Description

3.15.2 Logical Device 8 (HM) Configuration

Table 33 lists the configuration registers that affect the Health Management Module. See Section 3.2.3 on page 39 for a detailed description of these registers. The standard configuration registers are powered by V_{DD3}; however, the specific configuration registers are powered by V_{SB3}.

Table 33. Health Management (HM) Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate. When bit 0 is cleared, the runtime registers of this logical device are not accessible (see Section 3.3.1 on page 48).[1]	R/W	V_{DD3}	00h
50h	Memory Base Descriptor.	R/W	V_{DD3}	00h
60h	HM_LPC Base Address MSB register.	R/W	V_{DD3}	00h
61h	HM_LPC Base Address LSB register. Bits 3-0 (for A3-0) are read-only, '0000'.	R/W	V_{DD3}	00h
70h	Interrupt Number.	R/W	V_{DD3}	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read-only.	R/W	V_{DD3}	03h
74h	Report no DMA assignment.	RO	V_{DD3}	04h
75h	Report no DMA assignment.	RO	V_{DD3}	04h
F0h	Health Management Configuration register 1 (HMCFG1).	Varies per bit	V_{SB3}	05h

1. The logical device runtime registers are maintained and all sensor monitoring mechanisms are functional.

3.15.3 Health Management Configuration Register 1 (HMCFG1)

This register is reset to 01h.

Power Well: Varies per bit

Location: Index F0h

Type: Varies per bit

Note: The FANOUTx_INV bits are configurable via the HM module runtime registers.

Bit	7	6	5	4	3	2	1	0
Name	**LOCKHCF**	**FANOUT2_ OTYPE**	**FANOUT2_ INV**	**FANOUT1_ OTYPE**	**FANOUT1_ INV**	**FANOUT0_ OTYPE**	**FANOUT0_ INV**	**INT_PU_EN**
Reset	0	0	0	0	0	0	0	1
Power Well	V_{DD3}	V_{BAT}[1]	V_{BAT}[1]	V_{BAT}[1]	V_{BAT}[1]	V_{BAT}[1]	V_{BAT}[1]	V_{SB3}

1. See Sections 2.1 and 2.2

Bit	Type	Description
7	R/W1S	**LOCKHCF (Lock Health Management Configuration).** When set to 1, locks the bits of HMCFG1 register (including LOCKHCF bit itself) by disabling writing to them. Once set, this bit can be cleared by Hardware reset. 0: R/W bits are enabled for write (default) 1: All bits are RO

3.0 Device Architecture and Configuration (Continued)

Bit	Type	Description
6	R/W or RO	**FANOUT2_OTYPE (FANOUT2 Output Type).** Controls the output buffer type of the FANPWM3 output. 0: Push-pull (default) 1: Open-drain
5	RO	**FANOUT2_INV (FANOUT2 Output Invert).** When this bit is set to 1, the signal at the FANPWM3 output is inverted. 0: Normal signal (default) 1: Inverted signal
4	R/W or RO	**FANOUT1_OTYPE (FANOUT1 Output Type).** Controls the output buffer type of the FANPWM2 output. 0: Push-pull (default) 1: Open-drain
3	RO	**FANOUT1_INV (FANOUT1 Output Invert).** When this bit is set to 1, the signal at the FANPWM2 output is inverted. 0: Normal signal (default) 1: Inverted signal
2	R/W or RO	**FANOUT0_OTYPE (FANOUT0 Output Type).** Controls the output buffer type of the FANPWM1 output. 0: Push-pull (default) 1: Open-drain
1	RO	**FANOUT0_INV (FANOUT0 Output Invert).** When this bit is set to 1, the signal at the FANPWM1 output is inverted. 0: Normal signal (default) 1: Inverted signal
0	R/W or RO	**INT_PU_EN (Internal Pull-Up Enable).** Controls the internal pull-up resistors on the SWD signal. 0: Disabled 1: Enabled (default)

4.0 System Wake-Up Control (SWC)

4.1 OVERVIEW

The System Wake-Up Control (SWC) supports the *ACPI Specification, Revision 2.0, Feb. 2, 1999.*

The SWC functional block receives external events from the system; it also receives internal events from the functional blocks of the PC8374L device. Based on these events, the SWC generates the Power Management SCI interrupt ($\overline{SIOPME}$) and the system interrupt (IRQ). In addition, it controls two LED indicators.

The SWC receives the following external events:

- 15 V_{SB}-powered General-Purpose Input/Output events (GPIOE17-16, GPIOE14-10 and GPIOE07-00).
- Modem Ring events ($\overline{RI1}$ and $\overline{RI2}$).
- Mouse movement and button pressing events (via MCLK and MDAT).
- Advanced key pressing events from the Keyboard (via KBCLK and KBDAT).

The SWC receives the following internal events:

- Keyboard and Mouse interrupt event (IRQ).
- Module interrupt (IRQ) event from the Legacy functional blocks (FDC, Parallel Port, Serial Ports 1 and 2 and InfraRed Port) and Health Management.
- Fan alarm from the Health Management module
- Alarms from the Health Management module

The SWC implements the ACPI generic register group (General-Purpose Event 1 group) with “child” events.

The SWC generates the Power Management Event signal (the ACPI interrupt, $\overline{SIOPME}$) and the system interrupt (IRQ) based on the external and internal events and on the routing information written into the General-Purpose Event 1 register group. The ACPI-compatible SCI interrupt ($\overline{SIOPME}$) and the system interrupt (IRQ) are independent of the current sleep state.

The SWC receives sleep state information via the $\overline{SLP\_S3}$ and $\overline{SLP\_S5}$ pins from an external ACPI controller and receives power supply status information via PWRGD_PS pin from the system power supply.

In addition, the SWC controls two LED indicators. The Standard LED Control option is used to provide blinking or constantly lit LEDs. The Advanced LED Control option provides programmable blink based on the current sleep state information or on the status of the V_{SB3} and V_{DD3} power supplies. The Special LED Control option provides blinking or constantly lit LEDs, based on the current sleep state information or on the status of the Main Power Supply and on a software controlled bit.

The SWC includes the Last Power State Special Power Management function. This function saves the system power state when an AC power failure occurs.

The SWC module is powered by the V_{SB3} and V_{BAT} planes (see Section 2.1.1 on page 32). However, during Power Fail state (i.e., when only V_{BAT} is present), the module functions (event detection, output generation and LEDs control) are disabled and only the V_{BAT}-powered Last Power State function is active.

Figure 11 shows the simplified block diagram of the SWC functional block.

4.0 System Wake-Up Control (SWC) (Continued)

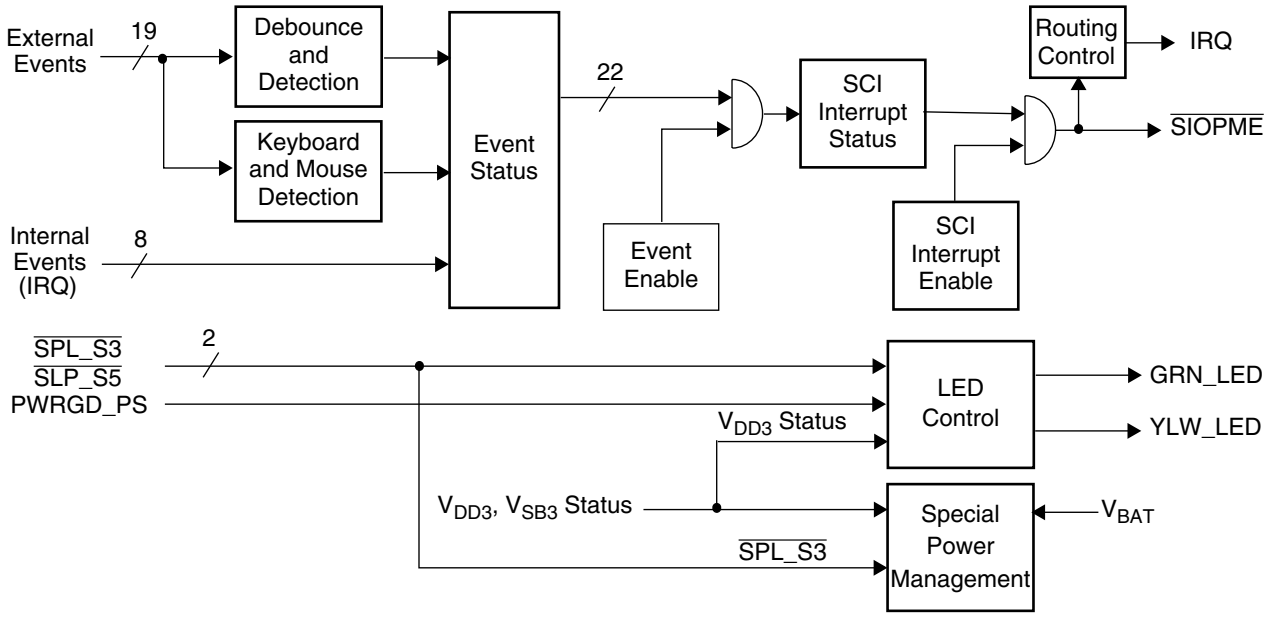


Figure 11. SWC Block Diagram

4.2 FUNCTIONAL DESCRIPTION

4.2.1 External Events

General-Purpose Input/Output Events

The PC8374L device supports 15 V_{SB3}-powered General-Purpose Input/Output events through ports GPIOE00-07 and GPIOE10-17 (excluding GPIO15). V_{DD3}- and V_{SB3}-powered signals can be connected to the GPIO pins to become sources of external events. A V_{DD3}-powered signal, when used to generate an event, is internally disabled for event generation while V_{DD3} power is off. It is also disabled for event generation for t_{EWIV} after V_{DD3} power is restored (see "Wake-Up Inputs at VDD3 Power Switching" on page 236), which prevents the detection of false events during power transitions and while the signal driver is not powered. For the same reasons, a V_{SB3}-powered signal used to generate an event is enabled only t_{EWIV} after V_{SB3} power is on. (When V_{SB3} is off, the whole SWC module is disabled.)

Each GPIOE pin has both programmable polarity and an optional debouncer (see Figure 12). The debouncer is enabled after the reset but can be disabled by software. The debouncing time is longer than 16 ms.

A GPIO event can generate the system interrupt (IRQ) if the event is both enabled and routed to IRQ. The status, event enable and pending event routing bits to IRQ are implemented in the GPIO Port module (see Section 6.3 on page 113). The status bit is set when an event of the programed type (edge or level) is detected.

A GPIO event can also generate the Power Management SCI interrupt ($\overline{\text{SIOPME}}$). The status and event enable bits are implemented in the SWC module (see Figures 12 and 13).

An active level-type event sets the status bit in registers GPE1_STS_0 for ports GPIOE07-00 and GPE1_STS_1 for ports GPIOE17-10 (see Sections 4.4.4 and 4.4.5 on page 101). The status bit remains set even after the event becomes inactive. The status bit is cleared only when the software writes 1 to the bit. If the event is still active when software writes 1, the status bit remains set.

After changing the GPIOE1x pin multiplexing, clear the relevant bits in the GPE1_STS_1 register, to prevent false events (caused by the pin multiplexing switch) from generating a wake-up event.

4.0 System Wake-Up Control (SWC) (Continued)

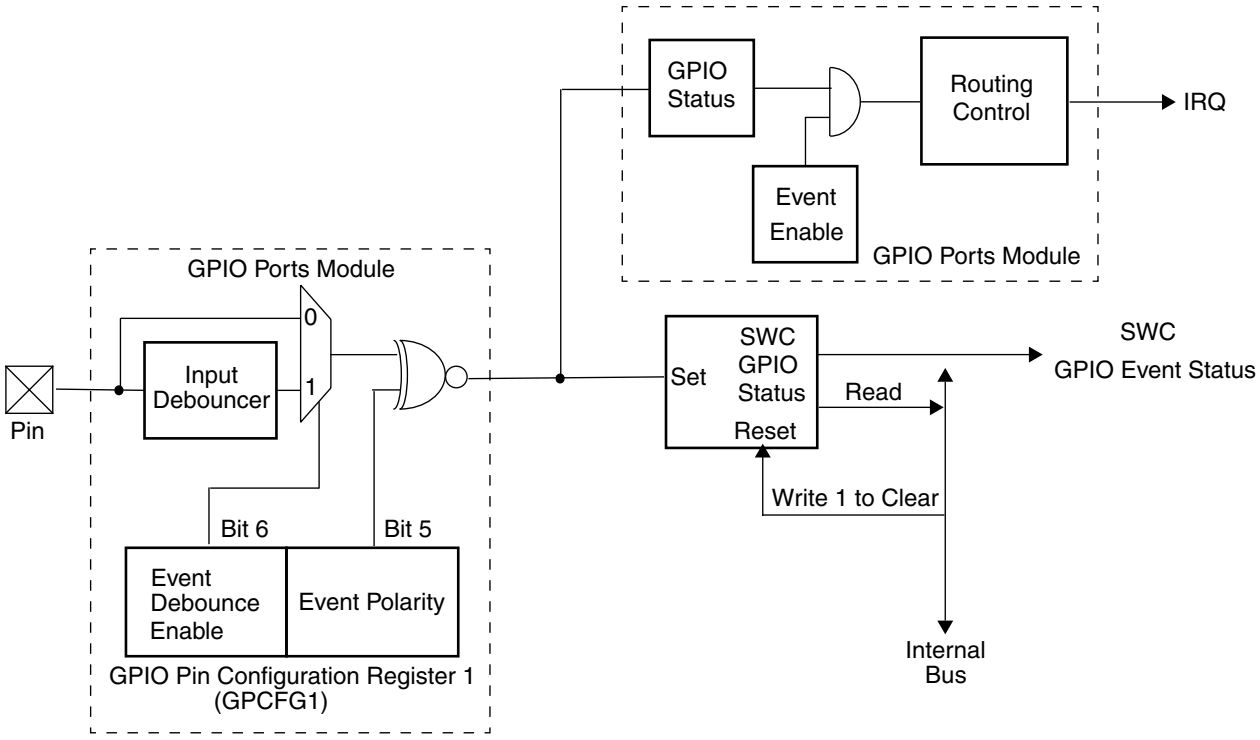


Figure 12. GPIO Events

Modem Ring Events

High-to-low transitions on $\overline{RI1}$ or $\overline{RI2}$ indicate the detection of a ring signal by an external modem connected to the Serial Port 1 or Serial Port 2, respectively. The transitions on $\overline{RI1}$ and $\overline{RI2}$ are detected by the RI Wake-Up Detector powered by V_{SB3}, which works independently of the Serial Port 1 or Serial Port 2 modules (powered by V_{DD3}).

A detected $\overline{RI1}$ or $\overline{RI2}$ transition sets the RI1_EVT_STS or RI2_EVT_STS status bit in GPE1_STS_2 register (see Section 4.4.6 on page 102). The status bit is cleared only when the software writes 1 to it.

The transition detection from $\overline{RI1}$ and $\overline{RI2}$ is enabled (for event generation) t_{EWIV} after V_{SB3} power is on (see "Wake-Up Inputs at VSB3 Power Switching" on page 236). This prevents the detection of false events during V_{SB3} power-On transitions.

Mouse Wake-Up Event

A mouse wake-up event is detected by the Keyboard/Mouse Wake-Up Detector, which monitors the MCLK and MDAT signals. Since the detection mechanisms for keyboard and mouse events are independent, they can be operated simultaneously. Moreover, the Keyboard signals may be swapped with the Mouse signals by setting SWAP bit in KBC Configuration register (see Section 3.13.3 on page 72). The Keyboard/Mouse Wake-Up Detector is powered by V_{SB3} and works independently of the Keyboard Controller module (powered by V_{DD3}).

The mouse event detection mechanism can be programed to detect either a mouse click or movement, a specific mouse click (left or right) or a double-click. To program which mouse action causes an event detection, set MSEVCFG field in PS2CTL register to the required value (see Section 4.3.8 on page 97).

A detected mouse event sets the MS_EVT_STS status bit in GPE1_STS_2 register (see Section 4.4.6 on page 102). The status bit is cleared only when the software writes 1 to it.

Mouse event detection from MCLK and MDAT is enabled (for event generation) t_{EWIV} after V_{SB3} power is on (see "Wake-Up Inputs at VSB3 Power Switching" on page 236). This prevents the detection of false Mouse events during V_{SB3} power-On transitions.

4.0 System Wake-Up Control (SWC) (Continued)

Keyboard Wake-Up Events

Keyboard wake-up events are also detected by the Keyboard/Mouse Wake-Up Detector, which monitors the KBCLK and KBDAT signals. Since the detection mechanisms for keyboard and mouse events are independent, they can be operated simultaneously. Moreover, the Keyboard signals may be swapped with the Mouse signals, by setting SWAP bit in KBC Configuration register (see Section 3.13.3 on page 72). The Keyboard/Mouse Wake-Up Detector is powered by V_{SB3} and works independently of the Keyboard Controller module (powered by V_{DD3}).

The keyboard event detection mechanism can be programed to detect:

- Any keystroke (Fast Any-Key or Special Key Sequence modes).
- A specific programmable sequence of up to eight alphanumeric keystrokes (Password mode).
- Any programmable sequence of up to eight bytes of data received from the keyboard (Special Key Sequence mode).
- Up to three programmable Power Management keys concurrently available, each including a sequence of up to three bytes of data received from the keyboard (Power Management Keys mode).

The Keyboard/Mouse Wake-Up Detector has four operation modes:

- Fast Any-Key mode
- Password mode
- Special Key Sequence mode
- Power Management Keys mode

Up to eight Keyboard Data registers (PS2KEY0-7) are used to define which keyboard data string generates an event. Since the same set of registers is used by three of the four operation modes, only one mode can be selected at a time.

For modes involving more than one keystroke, the maximum delay allowed between pressing two consecutive keys is 4 seconds. A longer delay is interpreted by the Wake-Up Detector as the beginning of a new sequence of keystrokes, which causes the present sequence to be discarded. In all operation modes, pressing a wrong key requires a recovery time of 4 seconds, before a new (correct) sequence may be recognized.

Fast Any-Key Mode. In this mode, pressing any key on the keyboard is identified as a keyboard event and, as a result, KBD_ANYK_STS bit in GPE1_STS_2 register is set (see Section 4.4.6 on page 102). The status bit is cleared only when the software writes 1 to it. The key data contained in the PS2KEY0-7 registers is ignored. To program the Keyboard/Mouse Wake-Up Detector to operate in Fast Any-Key mode, set KBDMODE field in KBDWKCTL register to '01' (see Section 4.3.7 on page 96).

Password Mode. In this mode, the "Break" bytes transmitted by the keyboard are discarded, and only the "Make" keystroke bytes are compared with those programed in the PS2KEY0-7 registers. If the two sets are identical, a keyboard event that sets KBD_EVT1_STS bit in GPE1_STS_2 register is detected (see Section 4.4.6 on page 102). The status bit is cleared only when the software writes 1 to it. Only keys with a "Make" keystroke data of one byte can be included in the sequence to be detected. To program the Keyboard/Mouse Wake-Up Detector to operate in Password mode:

1. Set KBDMODE field in KBDWKCTL register to '00' (see Section 4.3.7 on page 96).
2. Set KBEVCFG field in PS2CTL register to a value that indicates the desired number of alphanumeric keystrokes in the sequence. The programed value = the number of keystrokes + 7. For example, to detect a sequence of two keys, set KBEVCFG to 09h.
3. Program the appropriate subset of the PS2KEY0-7 registers, in sequential order, with the "Make" data bytes of the keys in the sequence. For example, if there are three keys in the sequence and the "Make" keystroke data of these keys are 05h (first), 50h (second) and 44h (third), program PS2KEY0 to 05h, PS2KEY1 to 50h and PS2KEY2 to 44h (the scan codes are only examples).

Special Key Sequence Mode. In this mode, all the bytes transmitted by the keyboard (including "Make" and "Break" bytes) are compared with those programed in the PS2KEY0-7 registers. If the two sets are identical, a keyboard event is detected, as explained in *Password Mode*, above. Special Key Sequence mode enables the detection of any sequence of keystrokes, including "Shift", "Alt" and "Ctl" keys. To program the Keyboard/Mouse Wake-Up Detector to operate in Special Key Sequence mode:

1. Set KBDMODE field in KBDWKCTL register to '00' (see Section 4.3.7 on page 96).
2. Set KBEVCFG field in PS2CTL register to a value that indicates the total number of bytes ("Make" and "Break") in the sequence, minus 1 (i.e., the programed value = the number of bytes - 1). For example, to detect a sequence of three received bytes (i.e., one keystroke), set KBEVCFG to 02h. The minimum value of the KBEVCFG field is 1 (i.e., two bytes).
3. Program the appropriate subset of the PS2KEY0-7 registers, in sequential order, with the data bytes that comprise the sequence. For example, if the number of bytes in the sequence is four, and the values of these bytes are E0h (first), 5Bh (second), E0h (third) and DBh (fourth), program PS2KEY0 to E0h, PS2KEY1 to 5Bh, PS2KEY2 to E0h and PS2KEY3 to DBh (the byte values are only examples).

4.0 System Wake-Up Control (SWC) (Continued)

Special Key Sequence mode also enables detection of any single keystroke. To program the Keyboard/Mouse Wake-Up Detector to wake-up on any single keystroke:

1. Set KBDMODE field in KBDWKCTL register to '00' (see Section 4.3.7 on page 96).
2. Set KBEVCFG field in PS2CTL register to '0001'.
3. Program the PS2KEY0 and PS2KEY1 registers to 00h. This forces the detector to ignore the values of incoming data, thus causing it to detect a keyboard event caused by a single keystroke.

Power Management Mode. In this mode, the PS2KEY0-7 register bank is divided into three groups of registers: PS2KEY0-2, PS2KEY3-5 and PS2KEY6-7. Each group can be programed with different data bytes, allowing the bytes transmitted by the keyboard to be compared simultaneously with three keystroke sequences. If the bytes transmitted by the keyboard (including Make and Break) are identical to the data bytes in one register group, the related keyboard event is detected. The detection of Keyboard Event 1 (data in PS2KEY0-2) sets KBD_EVT1_STS bit; the detection of Keyboard Event 2 (data in PS2KEY3-5) sets KBD_EVT2_STS bit; the detection of Keyboard Event 3 (data in PS2KEY6-7) sets KBD_EVT3_STS bit. All three status bits are in GPE1_STS_2 register (see Section 4.4.6 on page 102). Each status bit is cleared only when the software writes 1 to the bit. This mode enables the detection of any sequence of keys.

To program the Keyboard/Mouse Wake-Up Detector to operate in Power Management Keys mode, proceed as follows:

1. Set KBDMODE field in KBDWKCTL register to '10' (see Section 4.3.7 on page 96).
2. Set each event configuration field (EVT1CFG, EVT2CFG and EVT3CFG) in KBDWKCTL register to a value that indicates the desired number of keystroke data bytes ("Make" and "Break" bytes) in the sequence, for each event. For example, to detect a sequence of two received bytes, set EVTxCFG to 02h.
3. Program each group of the PS2KEY0-7 registers, in sequential order, with the data bytes of the keys in the sequence for each event.

Event Generation. Keyboard event detection from KBCLK and KBDAT is enabled, for event generation, t_{EWIV} after V_{SB3} power is on (see "Wake-Up Inputs at VSB3 Power Switching" on page 236). This prevents the detection of false Keyboard events during V_{SB3} power-On transitions.

Usage Hints:

1. After changing the operation mode of the Keyboard/Mouse Wake-Up Detector, clear the KBD_EVT3_STS, KBD_EVT2_STS, KBD_EVT1_STS, and KBD_ANYK_STS status bits in GPE1_STS_2 register (see Section 4.4.6 on page 102).
2. If a byte sequence that is a "subset" of the byte sequence of another ("superset") Power Management key event is used, the "superset" Power Management key event will never be detected. (The subset sequence has fewer bytes, set by EVTxCFG fields in KBDWKCTL register, than the superset sequence; however, the bytes contained in the subset sequence, as programed in the PS2KEY0-7 registers, are identical to the respective bytes of the superset sequence.)

4.2.2 Internal Events

Keyboard and Mouse IRQ Events

Keyboard and Mouse IRQ events are detected when either the Keyboard IRQ or Mouse IRQ is asserted.

To enable the IRQ of a logical device to generate an IRQ event, the associated Enable bit (bit 4 of the configuration register at index 70h; see Section 3.2.3 on page 39) must be set to 1. Since the Keyboard Controller (KBC) functional block is powered by V_{DD3}, a Keyboard or Mouse IRQ event can occur only when V_{DD3} is present.

An active (level-type) Keyboard IRQ event sets KBD_IRQ_STS status bit; an active Mouse IRQ event sets MS_IRQ_STS status bit. Both status bits are in GPE1_STS_3 register (see Section 4.4.7 on page 103). A status bit is cleared only when the software writes 1 to it. If the IRQ event is active when software writes 1 to the status bit, the status bit remains set.

The ROM code used for the Keyboard Controller generates active high Keyboard and Mouse interrupts, which are used by the SWC module.

Module IRQ Event

A Module IRQ event is detected when one of the Legacy modules (FDC, Parallel Port, Serial Ports 1 and 2. InfraRed Port), or Health Management module — asserts its IRQ.

To enable the IRQ of a logical device to generate an IRQ event, the associated Enable bit (bit 4 of the configuration register at index 70h; see Section 3.2.3 on page 39) must be set to 1. This bit is cleared when V_{DD3} is not present.

MOD_IRQ_STS status bit in GPE1_STS_3 register is set by an IRQ that is asserted by one of the Legacy modules or the Health Management module (see Section 4.4.7 on page 103). The status bit is cleared only when the software writes 1 to it. If the Module IRQ event is active when software writes 1 to the status bit, the bit remains set. When V_{DD3} is not present, the events from the FDC and Serial Ports 1 and 2 are blocked from the status bit. When V_{SB3} is not present, the event from the HM module is blocked from the status bit.

4.0 System Wake-Up Control (SWC) (Continued)

Health Management Events

Health Management events are generated by the Health Management module (HM). These events can create an internal signal routed to the SWC module, to the HM_STS bit in the GPE1_STS_3 register (see Section 4.4.7 on page 103). A status bit is updated only when the software writes 1 to it.

For the list of events and routing to SWC module (to the HM_STS bit), see “SCI and SMI Events Routing” in the “Events Notification” section.

4.2.3 Sleep States

The PC8374L identifies the current system sleep state, by decoding the levels of the $\overline{\text{SLP\_S3}}$ and $\overline{\text{SLP\_S5}}$ pins. The levels of these pins are generated by the system ACPI controller located in an external device. Table 34 shows the decoding of the logic levels of the $\overline{\text{SLP\_S3}}$ and $\overline{\text{SLP\_S5}}$ pins.

Table 34. $\overline{\text{SLP\_S3}}$, $\overline{\text{SLP\_S5}}$ Decoding

$\overline{\text{SLP\_S3}}$	$\overline{\text{SLP\_S5}}$	System Sleep State
1	1	S0, S1 or S2
0	1	S3
0	0	S5
1	0	Illegal combination

4.2.4 SCI and IRQ Interrupts

The SCI ($\overline{\text{SIOPME}}$) pin is the Power Management interrupt defined by ACPI.

All external and internal events are exclusively processed by the SWC to generate the Power Management interrupt, SCI. Each active event sets a status bit in GPE1_STS_0 to GPE1_STS_3 registers (see Sections 4.4.4 to 4.4.7 on page 101).

For each status bit, the SWC holds an enable bit in GPE1_EN_0 to GPE1_EN_3 registers. A set status bit can set PME_STS bit in GPE1_STS register (see Section 4.4.2 on page 100) only when its related enable bit is set. A set PME_STS bit can cause the assertion of the SCI interrupt only when PME_EN bit in GPE1_EN register is set (see Section 4.4.3 on page 100).

The SCI interrupt is independent of the system sleep state.

The $\overline{\text{SIOPME}}$ signal can be inverted to generate an active high SCI interrupt. In addition, the output buffer of the $\overline{\text{SIOPME}}$ pin can be configured as either push-pull or open-drain, to allow sharing with external SCI interrupt sources.

Figure 13 shows SCI generation.

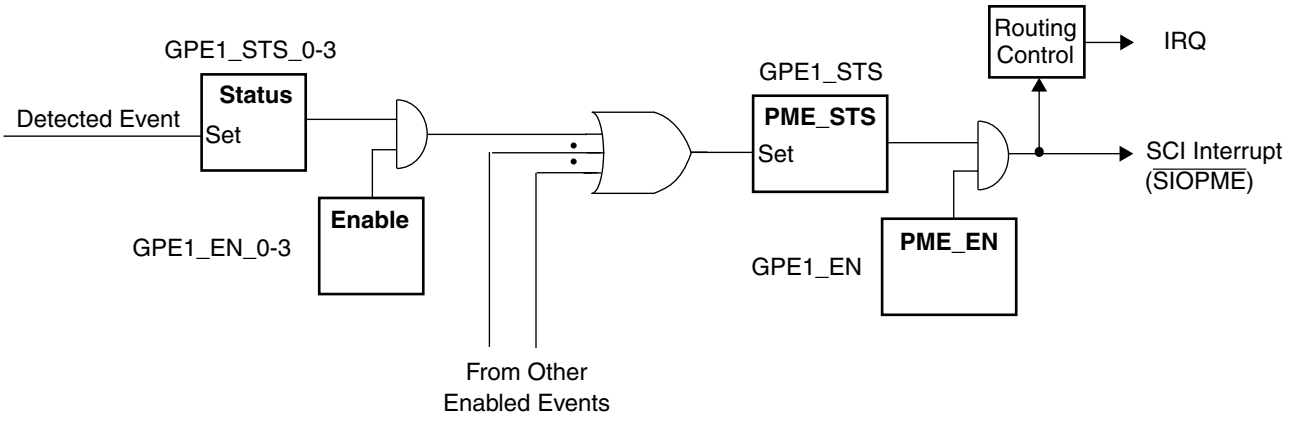


Figure 13. SCI Generation

The SCI interrupt ($\overline{\text{SIOPME}}$) is routed to the system interrupt (IRQ) by setting the Interrupt Number value, in the Interrupt Number register, located at index 70h in the SWC Configuration (see Section 3.12.2 on page 70).

4.0 System Wake-Up Control (SWC) (Continued)

4.2.5 LED Control

The PC8374L device controls the operation of two LED indicators. The two open-drain buffers allow the connection of either two regular LEDs or one dual-color LED.

The LEDs can be connected to PC8374L using one of the configurations shown in Figure 14.

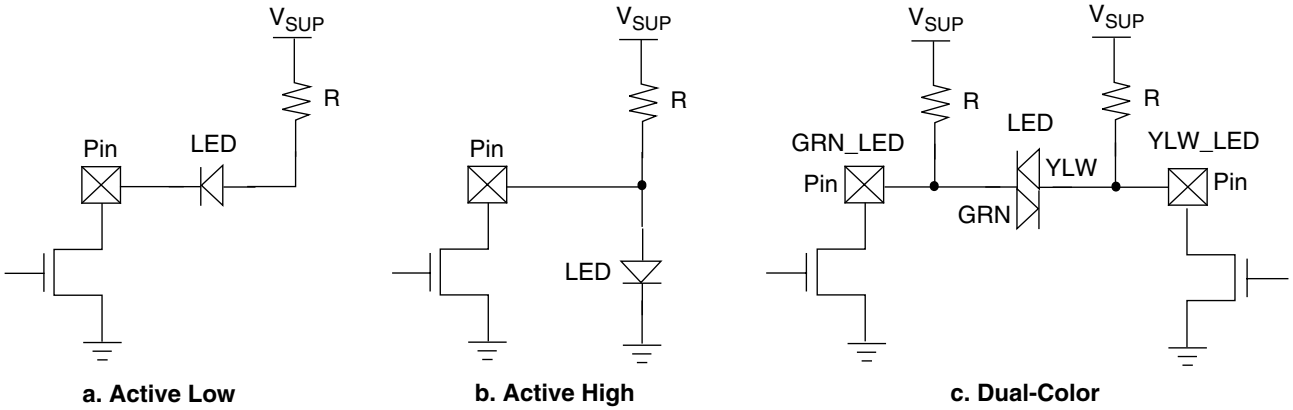


Figure 14. LED Connection Configurations

The LED pins are named GRN_LED (Green LED) and YLW_LED (Yellow LED), although other LED colors can be used.

The PC8374L allows three LED control options, which are selected by LED_OPT field in SWC_CTL register (see Section 4.3.3 on page 92):

- Standard LED control: On/Off and Blink controlled by software or by S5 sleep state
- Advanced LED control: On/Off and Blink controlled by software, by S3 or S5 sleep states, or by the V_{DD3} power supply status
- Special LED control: On/Off and Blink controlled by software, by S3 or S5 sleep states or by the Main power supply status via the PWRGD_PS signal

From the base address of the SWC registers, the register for Standard LED Control is located at offset 00h, the two registers for Advanced LED Control are located at offsets 02h and 03h, and the register for Special LED Control is located at offset 02h (see Section 4.3.1 on page 90). The active control registers are selected by LED_OPT field.

The blink rate and duty cycle of all LED control options are based on a clock, which is obtained by dividing the frequency of the 32 KHz clock domain.

Standard LED Control

In this mode, two regular LEDs must be connected to the GRN_LED and the YLW_LED pins, according to configuration “b” (Active High) in Figure 14.

In this option, LED operation is controlled by the bits of SLEDCTL register (at offset 00h; see Section 4.3.2 on page 91) and by the $\overline{SLP\_S5}$ pin. When the system is in sleep state S5 ($\overline{SLP\_S5}$ = 0), both LEDs are off. GRN_YLW bit selects the active LED (on or blinking) of the two; the other LED is off. BLINK bit selects the operation mode of the active LED as either constantly on or blinking at 0.667 Hz with a duty cycle of 41.7% (on time percent of the blink cycle).

Table 37 on page 91 shows the states of the GRN_LED and YLW_LED pins. The LEDs are connected according to configuration “b” (see Figure 14); therefore, a LED is on when the pin is floated and off when the pin is at low level (0).

Advanced LED Control

In the Advanced LED control option, one dual-color LED or two regular LEDs can be connected to the GRN_LED and the YLW_LED pins, using any of the configurations shown in Figure 14. LEDCFG and LEDPOL bits in ALEDCTL register (at offset 02h; see Section 4.3.4 on page 93) must be set to reflect the connection configuration of the LEDs.

LEDCFG bit selects either configurations “a” and “b” (two regular LEDs are connected between each pin and ground or V_{SUPP}) or configuration “c” (one dual-color LED is connected between the GRN_LED and YLW_LED pins). LEDPOL bit selects the polarity of the On state at both pins (GRN_LED and YLW_LED). Table 35, shows the value of LEDCFG and LEDPOL bits for each LED connection configuration in Figure 14, and also the state of the GRN_LED and YLW_LED pins for which the LED(s) are On.

4.0 System Wake-Up Control (SWC) (Continued)

Table 35. LEDs "On" Polarity as a Function of LEDCFG and LEDPOL

LEDCFG	LEDPOL	GRN_LED	YLW_LED	Connection (See Figure 14)
0	0	TRI-STATE	0	"c", Green anode to GRN_LED pin
0	1	0	TRI-STATE	"c", Yellow anode to GRN_LED pin
1	0	TRI-STATE	TRI-STATE	"b"
1	1	0	0	"a"

The LEDMOD field controls the operation mode of GRN_LED and YLW_LED pins in each system power state (see Table 38 on page 93). The system power state is identified either by the status of the V_{DD3} power supply or by the current system sleep state:

- '00' – The behavior of the GRN_LED and YLW_LED pins is controlled solely by software by the setting of the GRNBLNK and YLWBLNK fields.
- '01' – The behavior of the GRN_LED and YLW_LED pins is controlled by the status of the V_{DD3} supply and by software.
  In the Power Off state (V_{DD3} off), the GRN_LED behaves according to the setting of the GRNBLNK field, but the YLW_LED blinks at a 1 Hz rate with a 50% duty cycle;
  In the Power On state (V_{DD3} on), each LED behaves according to the setting of its xxxBLNK field.
- '10' – The behavior of the GRN_LED and YLW_LED pins is controlled by the S5 sleep state and by software.
  In S5 sleep state, both LEDs are off;
  In S3 - S0 sleep states, each LED behaves according to the setting of its xxxBLNK field.
- '11' – The behavior of the GRN_LED and YLW_LED pins is controlled by the status of the V_{DD3} supply and by software.
  In the Power Off state (V_{DD3} off), both LEDs are off;
  In Power On state (V_{DD3} on), each LED behaves according to the setting of its xxxBLNK field.

The status of the V_{DD3} power supply is detected by internal circuits, which identify the Power Off and Power On states (see Section 2.1.2 on page 32).

The current system sleep state is decoded from the levels of the $\overline{SLP\_S3}$ and $\overline{SLP\_S5}$ pins (see Section 4.2.3 on page 86). Only sleep state S5 is relevant.

The GRNBLNK and YLWBLNK fields in LEDBLNK register (at offset 03h; see Section 4.3.6 on page 95) control the On/Off state or the blinking rate of the GRN_LED and YLW_LED pins, respectively. For each LED pin, a different blink rate can be selected. Different blink rates can also be selected for the dual-color LED mode (LEDCFG = 0).

Special LED Control

Special LED control is the default LED control option. In the Special LED control option, configuration "b" or "c" in Figure 14 can be used.

In this option, LED operation is controlled by the bits of XLEDCTL register (at offset 02h; see Section 4.3.5 on page 94) and by the $\overline{SLP\_S3}$, $\overline{SLP\_S5}$ and PWRGD_PS pins. When the system is in sleep state S5 ($\overline{SLP\_S5}$ = 0), both LEDs are off. When the system is in sleep state S3 ($\overline{SLP\_S3}$ = 0) or S1 (SLP_S1 bit is set), the green LED blinks and the yellow LED is off. The green and yellow LED operation is reversed when the system is in the working state (S0) and the Main power supply is not functional (PWRGD_PS = 0). When the system is in working state (S0) and the Main power supply is within the specified limits, SW_CTL bit selects the active LED (On) of the two, and the other LED is turned off.

The blinking rate of the LEDs is 1 Hz with a duty cycle of 50%.

Table 39 on page 94 shows the states of the GRN_LED and YLW_LED pins. The LEDs are connected according to configuration "b" (see Figure 14 on page 87); therefore, a LED is On when the pin is floated; it is Off when the pin is at low level (0).

4.0 System Wake-Up Control (SWC) (Continued)

4.2.6 Special Power Management Functions

Last Power State

Last Power State function saves the system power state when an AC power failure occurs.

When either the V_{DD3} or V_{SB3} power supply falls below the minimum limit, the SWC samples the value of the $\overline{SLP\_S3}$ signal. If $\overline{SLP\_S3}$ is sampled low, this indicates an orderly shutdown of the Main supply through the S3-S5 sleep states; however, if $\overline{SLP\_S3}$ is sampled high, this indicates a Power Fail condition, caused either by turning off the mechanical switch (G2 state) or by an AC power failure. The sampled value is powered by the V_{BAT} backup supply, which preserves its value throughout the Power Fail condition when both V_{DD3} and V_{SB3} supplies are off (see Section 2.1.2 on page 32) and until AC power returns. When the system exits Power Fail (i.e., when V_{SB3} power is back on), this read-only bit serves as a snapshot of the system state before the power was turned off.

The level of the $\overline{SLP\_S3}$ signal is sampled in LAST_PWR_STATE read-only bit in SWC_CTL register (see Section 4.3.3 on page 92).

In case of a power failure, both V_{DD} and V_{SB} power supplies fall simultaneously. Therefore, the power failure is detected either by V_{DD3} falling below V_{DD3OFF}, or by V_{SB3} falling below V_{SB3OFF}, whichever occurs first.

The LAST_PWR_STATE bit is reset to 0 at V_{BAT} power-up (see Section 2.2.1 on page 35).

Backup Battery Status

This function detects the status of the backup battery (V_{BAT}). When the battery voltage is below the specification ($V_{BAT} < V_{BATLOW}$), GOOD_BAT and LAST_PWR_STATE bits in SWC_CTL register (see Section 4.3.3 on page 92) are reset. In this case, the value of LAST_PWR_STATE bit is incorrect and must be ignored.

If the battery voltage is within specified limits ($V_{BAT} > V_{BATLOW}$), GOOD_BAT bit is set when either the V_{DD3} or the V_{SB3} power supply falls below the minimum limit.

4.0 System Wake-Up Control (SWC) (Continued)

4.3 SWC REGISTERS

The offsets of the SWC registers are related to the base address determined by the SWC Base Address register at indexes 60h-61h in the SWC Logical Device configuration.

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register (data written to this address is sent to a different register).
- W = Write (see above).
- RO = Read-only.
- WO = Write-only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

4.3.1 SWC Register Map

The following table lists the SWC registers. For the SWC register bitmap, see Section 4.5 on page 107. The SWC registers are V_{SB3} powered.

Table 36. SWC Register Map

Offset	Option[1]	Mnemonic	Register Name	Type	Power Well	Section
00h	LED_OPT = 01	SLEDCTL	Standard LED Control	R/W or RO	V_{SB3}	4.3.2
	LED_OPT = other	Reserved				
01h		SWC_CTL	SWC Miscellaneous Control	Varies per bit	Varies per bit	4.3.3
02h	LED_OPT = 00	ALEDCTL	Advanced LED Control	R/W or RO	V_{SB3}	4.3.4
	LED_OPT = 10	XLEDCTL	Special LED Control	R/W or RO	V_{DD3}	4.3.5
	LED_OPT = other	Reserved				
03h	LED_OPT = 00	LEDBLNK	LED Blinking Control	R/W or RO	V_{SB3}	4.3.6
	LED_OPT = other	Reserved				
04h		KBDWKCTL	Keyboard Wake-Up Control	R/W or RO	V_{SB3}	4.3.7
05h		PS2CTL	PS2 Protocol Control	R/W or RO	V_{SB3}	4.3.8
06h		KDSR	Keyboard Data Shift-Register	RO	V_{SB3}	4.3.9
07h		MDSR	Mouse Data Shift-Register	RO	V_{SB3}	4.3.10
08h		PS2KEY0	PS2 Keyboard Key Data 0	R/W, RO	V_{SB3}	4.3.11
09h		PS2KEY1	PS2 Keyboard Key Data 1	R/W, RO	V_{SB3}	4.3.11
0Ah		PS2KEY2	PS2 Keyboard Key Data 2	R/W, RO	V_{SB3}	4.3.11
0Bh		PS2KEY3	PS2 Keyboard Key Data 3	R/W, RO	V_{SB3}	4.3.11
0Ch		PS2KEY4	PS2 Keyboard Key Data 4	R/W, RO	V_{SB3}	4.3.11
0Dh		PS2KEY5	PS2 Keyboard Key Data 5	R/W, RO	V_{SB3}	4.3.11
0Eh		PS2KEY6	PS2 Keyboard Key Data 6	R/W, RO	V_{SB3}	4.3.11
0Fh		PS2KEY7	PS2 Keyboard Key Data 7	R/W, RO	V_{SB3}	4.3.11

1. Selected by LED_OPT field in SWC_CTL register.

4.0 System Wake-Up Control (SWC) (Continued)

4.3.2 Standard LED Control Register (SLEDCTL)

This register configures the standard LED control of the two LEDs connected to pins GRN_LED and YLW_LED of the PC8374L device. It is reset to 03h.

Power Well: V_{SB3}

Location: Offset 00h, when LED_OPT = 01 in the SWC_CTL register

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**						**BLINK**	**GRN_YLW**
Reset	0	0	0	0	0	0	1	1

Bit	Description
7-2	**Reserved.**
1	**BLINK (LEDs Blink Control).** Controls the operation mode (either blinking or constantly on) of the LED selected by GRN_YLW bit. Blinking rate is 0.667 Hz with a duty cycle of 41.7%. When the system is in sleep state S5, both LEDs are forced off regardless of BLINK and GRN_YLW bit values; see Table 37. 0: Selected LED blinking 1: Selected LED constantly on (default)
0	**GRN_YLW (Green-Yellow LED Select).** Selects which of the two LEDs (GRN_LED or YLW_LED) is active. The LED which is not active is off; see Table 37. 0: Yellow LED (connected to YLW_LED pin) selected 1: Green LED (connected to GRN_LED pin) selected (default)

Table 37. GRN_LED and YLW_LED States

$\overline{\text{SLP\_S5}}$ pin	GRN_YLW bit	BLINK bit	GRN_LED pin	YLW_LED pin
0[1]	X[2]	X	0	0
1	0	0	0	Blink
1	0	1	0	TRI-STATE
1	1	0	Blink	0
1	1	1	TRI-STATE	0

1. $\overline{\text{SLP\_S5}}$ = 0: System is in sleep state S5.
2. X is either logic “0” or logic “1”.

4.0 System Wake-Up Control (SWC) (Continued)

4.3.3 SWC Miscellaneous Control Register (SWC_CTL)

This register contains control and status bits for the SWC module. Its reset value depends on the power well of each bit.

Power Well: Varies per bit

Location: Offset 01h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKSCF**	**Reserved**	**GOOD_ BAT**	**Reserved**		**LAST_PWR _STATE**	**LED_OPT**	
Reset	0	0	0	0	0	0	10	
Power Well	V_{SB3}		V_{BAT}			V_{BAT}	V_{BAT}	

Bit	Type	Description
7	R/W1S	**LOCKSCF (Lock SWC Configuration).** When set to 1, locks the BLINK and GRN_YLW bits in SLEDCTL register, and all bits of SWC_CTL, ALEDCTL, LEDBLNK, XLEDCTL, KBDWKCTL, PS2CTL and PS2KEY0–7 registers by disabling writing to them (including to the LOCKSCF bit itself). Once set, this bit can be cleared by Hardware reset. 0: R/W bits are enabled for write (default) 1: All bits are RO
6		**Reserved.**
5	RO	**GOOD_BAT (Battery Good Status).** Indicates the status of the V_{BAT} backup power. The bit is powered by the V_{BAT} backup supply and its value is: • Reset at any time, if $V_{BAT} < V_{BATLOW}$ • Set when either V_{DD3} or V_{SB3} power supply falls below the minimum limit, if $V_{BAT} > V_{BATLOW}$ When the bit is '0', the value of the LAST_PWR_STATE bit is incorrect and must be ignored. 0: Backup battery low, or not connected ($V_{BAT} < V_{BATLOW}$) 1: Backup battery good ($V_{BAT} > V_{BATLOW}$)
4-3		**Reserved.**
2	RO	**LAST_PWR_STATE (Last Power State).** Samples the value of the $\overline{SLP\_S3}$ signal when a power failure occurs. It is powered by the V_{BAT} backup supply, thus preserving its value during a Power Fail condition (see Section 2.1.2 on page 32). After the AC power returns, reading from this bit returns the value of the $\overline{SLP\_S3}$ signal at the time the power failure occurred. The value of this bit must be ignored when GOOD_BAT bit is 0. Writing to this bit is ignored. At V_{BAT} Power-Up reset, LAST_PWR_STATE bit is reset to 0. 0: Orderly system shutdown - Main power off by S3 or S5 sleep states (default) 1: Forced system shutdown - Main power off by Mechanical off (G2 state) or by AC power failure
1-0	R/W or RO	**LED_OPT (LED Control Option Select).** Selects the Advanced, Standard or Special LED control option for the two power LEDs (yellow and green). **Bits 1 0 LED Control Option** 0 0: Advanced: LEDs controlled by the ALEDCTL and LEDBLNK registers at offsets 02h and 03h, respectively 0 1: Standard: LEDs controlled by SLEDCTL register at offset 00h 1 0: Special: LEDs controlled by XLEDCTL register at offset 02h (default) 1 1: Reserved

4.0 System Wake-Up Control (SWC) (Continued)

4.3.4 Advanced LED Control Register (ALEDCTL)

This register configures the advanced LED control of the two LEDs connected to pins GRN_LED and YLW_LED of the PC8374L device. It is reset to 00h.

Power Well: V_{SB3}

Location: Offset 02h, when LED_OPT = 00 in the SWC_CTL register

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**LEDCFG**	**LEDPOL**	**Reserved**		**LEDMOD**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5	**LEDCFG (LED Configuration).** Enables the use of either two regular LEDs, connected to the GRN_LED and YLW_LED pins or one dual-colored LED, connected between the two pins (see Figure 14 on page 87). 0: One dual-colored LED (default) 1: Two regular LEDs
4	**LEDPOL (LED Polarity).** Determines the polarity of GRN_LED and YLW_LED outputs. An active output, according to this bit setting, turns the LED on. For the dual-colored LED configuration, changing the polarity reverses the LED colors. The configurations described here apply to the “two regular LEDs” option only; see Table 35 on page 88). 0: Active high: for connection configuration “b” in Figure 14 on page 87 (default) 1: Active low: for connection configuration “a” in Figure 14 on page 87
3-2	**Reserved.**
1-0	**LEDMOD (LED Operation Mode).** These bits control the operation mode of GRN_LED and YLW_LED in each power state. Table 38 shows the behavior of the two LED outputs as a function of the system power state.

Table 38. GRN_LED and YLW_LED as a Function of the Power State

LEDMOD	V_{DD3} Off[1]	V_{DD3} On[1]	State S5[2]	State S3[2]	States S0 - S2[2]	GRN_LED	YLW_LED
00 (default)	X[3]	X	X	X	X	S/W_GRN[4]	S/W_YLW[5]
01	Yes		X	X	X	S/W_GRN	Blink[6]
		Yes	X	X	X	S/W_GRN	S/W_YLW
10	X	X	Yes			Off	Off
	X	X		Yes		S/W_GRN	S/W_YLW
	X	X			Yes	S/W_GRN	S/W_YLW
11	Yes		X	X	X	Off	Off
		Yes	X	X	X	S/W_GRN	S/W_YLW

1. See Section 2.1.2 on page 32.
2. See Section 4.2.3 on page 86.
3. In this table, X is “Irrelevant”.
4. Controlled by the value of GRNBLNK in the LEDBLNK register.
5. Controlled by the value of YLWBLNK in the LEDBLNK register.
6. Blink rate is 1 Hz with a duty cycle of 50%.

4.0 System Wake-Up Control (SWC) (Continued)

4.3.5 Special LED Control Register (XLEDCTL)

This register configures the Special LED Control of the two LEDs connected to pins GRN_LED and YLW_LED of the PC8374L device. It is reset to 00h.

Power Well: V_{DD3}

Location: Offset 02h, when LED_OPT = 10 in SWC_CTL register

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**						**SLP_S1**	**SW_CTL**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-2	**Reserved.**
1	**SLP_S1 (Sleep State S1 Select).** When set to 1 by the software, indicates that the system will enter an S1 sleep state. The value of this bit controls the operation mode of GRN_LED and YLW_LED, as shown in Table 39. 0: System in working state (S0), or in S3-S5 sleep states (default) 1: System in S1 sleep state
0	**SW_CTL (Software LEDs Control).** Controls the operation mode of GRN_LED and YLW_LED, as shown in Table 39. 0: Normal (default) 1: Bit set by software

Table 39. Special control of the GRN_LED and YLW_LED

System State	$\overline{\text{SLP\_S5}}$ Pin	$\overline{\text{SLP\_S3}}$ Pin	SLP_S1 Bit	PWRGD_PS Pin	SW_CTL Bit	GRN_LED Pin	YLW_LED Pin
Soft Off (S5)	0	X[1]	X	X	X	0	0
Sleep State S3	1	0	X	X	X	Blink[2]	0
Sleep State S1	1	1	1	X	X		
Working (S0), Power not good	1	1	0	0	X	0	Blink
Working (S0), Power good, no SW_CTL	1	1	0	1	0	0	TRI-STATE
Working (S0), Power good, and SW_CTL	1	1	0	1	1	TRI-STATE	0

1. In this table, X is either logic “1” or logic “0”.
2. Blink rate is 1 Hz with a duty cycle of 50%.

4.0 System Wake-Up Control (SWC) (Continued)

4.3.6 LED Blink Control Register (LEDBLNK)

This register controls the advanced blinking rate of the two LEDs connected to pins GRN_LED and YLW_LED of the PC8374L device. It is reset to 70h.

Power Well: V_{SB3}

Location: Offset 03h, when LED_OPT = 00 in the SWC_CTL register

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**GRNBLNK**			**Reserved**	**YLWBLNK**		
Reset	0	1	1	1	0	0	0	0

Bit	Description
7	**Reserved.**
6-4	**GRNBLNK (Green LED Blink Rate).** These bits control the blinking rate of GRN_LED output. **Bits 6 5 4 — Rate (Hz) — Duty Cycle** 0 0 0: Off — Always inactive 0 0 1: 0.25 — 12.5% 0 1 0: 0.5 — 25% 0 1 1: 1 — 50% 1 0 0: 2 — 50% 1 0 1: 3 — 50% 1 1 0: 4 — 50% 1 1 1: On — Always active (default)
3	**Reserved.**
2-0	**YLWBLNK (Yellow LED Blink Rate).** These bits control the blinking rate of YLW_LED output. **Bits 2 1 0 — Rate (Hz) — Duty Cycle** 0 0 0: Off — Always inactive (default) 0 0 1: 0.25 — 12.5% 0 1 0: 0.5 — 25% 0 1 1: 1 — 50% 1 0 0: 2 — 50% 1 0 1: 3 — 50% 1 1 0: 4 — 50% 1 1 1: On — Always active

4.0 System Wake-Up Control (SWC) (Continued)

4.3.7 Keyboard Wake-Up Control Register (KBDWKCTL)

This register configures the keyboard events detected by the Keyboard/Mouse Wake-Up Detector. It is reset to 40h.

Power Well: V_{SB3}

Location: Offset 04h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**KBDMODE**		**EVT3CFG**		**EVT2CFG**		**EVT1CFG**	
Reset	0	1	0	0	0	0	0	0

Bit	Description
7-6	**KBDMODE (Keyboard Mode Select).** Selects one of the keyboard wake-up modes for the Keyboard/Mouse Wake-Up Detector. **Bits 7 6 — Keyboard Wake-Up Mode** 0 0: Special Key Sequence or Password: Configured by bits 3-0 of PS2CTL register 0 1: Fast Any-Key: Indicates that any key was pressed on the keyboard (default) 1 0: Power Management Keys: Configured by bits 5-0 of KBDWKCTL register 1 1: Reserved
5-4	**EVT3CFG (Keyboard Event 3 Configuration).** These bits configure the keyboard data sequence for Keyboard Event 3, which indicates that “PM Key 3” was pressed on the keyboard. The setting of the EVT3CFG field is relevant only if the Keyboard/Mouse Wake-Up Detector is in Power Management Keys mode (KBDMODE = 10). The keyboard data sequence used to detect Keyboard Event 3 is stored in registers PS2KEY6-7, starting with PS2KEY6. **Bits 5 4 — Sequence Length** 0 0: 0 bytes: Keyboard Event 3 disabled (default) 0 1: 1 byte: PS2KEY6 1 0: 2 bytes: PS2KEY6, PS2KEY7 1 1: Reserved
3-2	**EVT2CFG (Keyboard Event 2 Configuration).** These bits configure the keyboard data sequence for Keyboard Event 2, which indicates that “PM Key 2” was pressed on the keyboard. The setting of the EVT2CFG field is relevant only if the Keyboard/Mouse Wake-Up Detector is in Power Management Keys mode (KBDMODE = 10). The keyboard data sequence used to detect Keyboard Event 2 is stored in registers PS2KEY3-5, starting with PS2KEY3. **Bits 3 2 — Sequence Length** 0 0: 0 bytes: Keyboard Event 2 disabled (default) 0 1: 1 byte: PS2KEY3 1 0: 2 bytes: PS2KEY3, PS2KEY4 1 1: 3 bytes: PS2KEY3, PS2KEY4, PS2KEY5
1-0	**EVT1CFG (Keyboard Event 1 Configuration).** These bits configure the keyboard data sequence for Keyboard Event 1, which indicates that “PM Key 1” was pressed on the keyboard. The setting of the EVT1CFG field is relevant only if the Keyboard/Mouse Wake-Up Detector is in Power Management Keys mode (KBDMODE = 10). The keyboard data sequence used to detect Keyboard Event 1 is stored in registers PS2KEY0-2, starting with PS2KEY0. **Bits 1 0 — Sequence Length** 0 0: 0 bytes: Keyboard Event 1 disabled (default) 0 1: 1 byte: PS2KEY0 1 0: 2 bytes: PS2KEY0, PS2KEY1 1 1: 3 bytes: PS2KEY0, PS2KEY1, PS2KEY2

4.0 System Wake-Up Control (SWC) (Continued)

4.3.8 PS2 Protocol Control Register (PS2CTL)

This register configures the keyboard and mouse events detected by the Keyboard/Mouse Wake-Up Detector. It is reset to 10h.

Power Well: V_{SB3}

Location: Offset 05h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**DISPAR**	**MSEVCFG**			**KBEVCFG**			
Reset	0	0	0	1	0	0	0	0

Bit	Description
7	**DISPAR (Disable Parity Check).** This controls the parity checking of the keyboard and mouse data by the Keyboard/Mouse Wake-Up Detector. 0: Enable parity check (default) 1: Disable parity check
6-4	**MSEVCFG (Mouse Event Configuration).** These bits configure the mouse data sequence for the Mouse event. Before setting them to a new value, these bits must be cleared by writing a value of '000'. **Bits 6 5 4 — Event Configuration** 0 0 0: Disable mouse wake-up detection 0 0 1: Wake-up on any mouse movement or button click (default) 0 1 0: Wake-up on left button click 0 1 1: Wake-up on left button double-click 1 0 0: Wake-up on right button click 1 0 1: Wake-up on right button double-click 1 1 0: Wake-up on any button single-click (left, right or middle) 1 1 1: Wake-up on any button double-click (left, right or middle)
3-0	**KBEVCFG (Keyboard Event Configuration).** These bits configure the keyboard data sequence for the Keyboard event indicating that any key or key sequence was pressed on the keyboard. The setting of the KBEVCFG field is relevant only if the Keyboard/Mouse Wake-Up Detector is in either Special Key Sequence or Password mode (KBDMODE = 00). The keyboard data sequence used to detect a Keyboard Event is stored in registers PS2KEY0-7, starting with PS2KEY0. Before setting them to a new value, the KBEVCFG field must be cleared by writing a value of '0000'. **Bits 3 2 1 0 — Event Configuration** 0 0 0 0: Disable keyboard wake-up detection (default) 0 0 0 1 to 0 1 1 1: Special Key Sequence mode consisting of from two to eight PS/2 data bytes, "Make" and "Break" codes (including Shift and Alt keys) 1 0 0 0 to 1 1 1 1: Password Enabled mode with consisting of from one to eight keys "Make" code (excluding Shift and Alt keys)

4.0 System Wake-Up Control (SWC) (Continued)

4.3.9 Keyboard Data Shift Register (KDSR)

When keyboard wake-up detection is enabled, this register stores the keyboard data shifted in from the keyboard during data transmission. It is reset to 00h.

Power Well: V_{SB3}

Location: Offset 06h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Keyboard Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Keyboard Data.**

4.3.10 Mouse Data Shift Register (MDSR)

When mouse wake-up detection is enabled, this register stores the mouse data shifted in from the mouse during data transmission. It is reset to 00h.

Power Well: V_{SB3}

Location: Offset 07h (offset in PC8741x = 17h)

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**Mouse Data**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved.**
2-0	**Mouse Data.**

4.3.11 PS2 Keyboard Key Data 0 to 7 Registers (PS2KEY0-7)

These eight registers (PS2KEY0-7) store the data bytes for Special Key Sequence or Password mode (KBDMODE = 00) or for Power Management Keys mode (KBDMODE = 10) of the Keyboard/Mouse Wake-Up Detector.

In Special Key Sequence or in Password modes, the keyboard data is stored as follows:

- PS2KEY0 register stores the data byte for the first key in the sequence.
- PS2KEY1 register stores the data byte for the second key in the sequence.
- PS2KEY2-7 registers store data bytes for the third to eighth key in the sequence.

For keyboard data storage in Power Management Keys mode, see Section 4.3.7 on page 96.

When one of these registers is set to 00h, it indicates that the value of the corresponding data byte is ignored (i.e., it is not compared with the keyboard data). These registers are reset to 00h.

Power Well: V_{SB3}

Location: Offset 08h to 0Fh

Type: R/W, RO

Bit	7	6	5	4	3	2	1	0
Name	**Data Byte of Key**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Data Byte of Key.**

4.0 System Wake-Up Control (SWC) (Continued)

4.4 ACPI REGISTERS

The ACPI registers are organized in two groups, which are both powered by V_{SB3}. The offsets of the two groups of ACPI registers are related to the base address determined by the Base Address registers at indexes 62h-63h in the SWC device configuration.

The PC8374L device supports the General-Purpose Event 1, ACPI generic register group. This group contains the GPE1_STS and GPE1_EN registers, each with a length of one byte. In addition, the device supports the "child" events of the General-Purpose Event 1 register group in the GPE1_STS_0-GPE1_STS_3 and the GPE1_EN_0-GPE1_EN_3 registers.

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register (data written to this address is sent to a different register).
- W = Write (see above).
- RO = Read-only.
- WO = Write-only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

4.4.1 ACPI Register Map

The following table lists the ACPI registers. All of these registers are V_{SB3} powered.

Table 40. ACPI Register Map

Base Registers	Offset	Mnemonic	Register Name	Type	Power Well	Section
At index 62h, 63h	00h	GPE1_STS	General-Purpose Status 1 Register	R/W1C	V_{SB3}	4.4.2
	01h-03h	Reserved				
	04h	GPE1_EN	General-Purpose Enable 1 Register	R/W	V_{SB3}	4.4.3
	05h-07h	Reserved				
	08h	GPE1_STS_0	General-Purpose Status 1 Register 0	R/W1C	V_{SB3}	4.4.4
	09h	GPE1_STS_1	General-Purpose Status 1 Register 1	R/W1C	V_{SB3}	4.4.5
	0Ah	GPE1_STS_2	General-Purpose Status 1 Register 2	R/W1C	V_{SB3}	4.4.6
	0Bh	GPE1_STS_3	General-Purpose Status 1 Register 3	R/W1C	V_{SB3}	4.4.7
	0Ch	GPE1_EN_0	General-Purpose Enable 1 Register 0	R/W	V_{SB3}	4.4.8
	0Dh	GPE1_EN_1	General-Purpose Enable 1 Register 1	R/W	V_{SB3}	4.4.9
	0Eh	GPE1_EN_2	General-Purpose Enable 1 Register 2	R/W	V_{SB3}	4.4.10
	0Fh	GPE1_EN_3	General-Purpose Enable 1 Register 3	R/W	V_{SB3}	4.4.11

4.0 System Wake-Up Control (SWC) (Continued)

4.4.2 General-Purpose Status 1 Register (GPE1_STS)

This register contains the global Power Management Event status bit. This register belongs to the General-Purpose Event 1 register group of the ACPI generic-feature space registers.

The status bit behaves according to the Sticky Status Bit definition in the ACPI Specification (i.e., the bit is set when the level of the hardware signal is high and is only cleared by the software writing 1 to it).

Power Well: V_{SB3}

Location: Offset 00h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**							**PME_STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-1	**Reserved.**
0	**PME_STS (Power Management Event Status).** Indicates that an enabled Power Management event has occurred. The bit is set if at least one enabled event (in GPE1_EN_0 to GPE1_EN_3 registers) is active (in GPE1_STS_0 to GPE1_STS_3 registers). The bit can be reset by writing 1 only if all the enabled events are inactive. 0: Inactive (default) 1: At least one enabled “child” event was active since this bit was last cleared

4.4.3 General-Purpose Enable 1 Register (GPE1_EN)

This register contains the global Power Management Event enable bit. This register belongs to the General-Purpose Event 1 register group of the ACPI generic-feature space registers. It is reset to 00h.

The enable bit behaves according to the Enable Bit definition in the ACPI Specification (i.e., the bit can be read or written by software).

Power Well: V_{SB3}

Location: Offset 04h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**							**PME_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-1	**Reserved.**
0	**PME_EN (Power Management Event Enable).** Controls SCI ($\overline{\text{SIOPME}}$) generation by a set PME_STS bit. If this bit is set, a set PME_STS bit in GPE1_STS register generates an SCI interrupt. 0: Disable SCI (default) 1: Enable SCI generation by a set PME_STS bit

4.0 System Wake-Up Control (SWC) (Continued)

4.4.4 General-Purpose Status 1 Register 0 (GPE1_STS_0)

This register contains “child” events 0-7 of the GPE1_STS register.

The status bits behave according to the Sticky Status Bit definition in the ACPI Specification (i.e., the bit is set when the hardware signal is high and is only cleared by the software writing 1 to it).

Power Well: V_{SB3}

Location: Offset 08h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**GPIOE07_STS**	**GPIOE06_STS**	**GPIOE05_STS**	**GPIOE04_STS**	**GPIOE03_STS**	**GPIOE02_STS**	**GPIOE01_STS**	**GPIOE00_STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIOE07_STS (GPIOE07 Event Status).** Indicates that an active event has been detected at pin 7 of GPIOE Port 0. The event has programmable polarity and the debounce option (see Section 6.3 on page 113). The bit is set by an active level at the GPIOE07 pin. Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: An active event has occurred
6-0	**GPIOE06_STS to GPIOE00_STS (GPIOE06 to GPIOE00 Event Status).** Same as above for pins 6-0 of GPIOE Port 0.

4.4.5 General-Purpose Status 1 Register 1 (GPE1_STS_1)

This register contains “child” events 8-15 of the GPE1_STS register.

The status bits behave according to the Sticky Status Bit definition in the ACPI Specification (i.e., the bit is set when the hardware signal is high and is only cleared by the software writing 1 to it).

Power Well: V_{SB3}

Location: Offset 09h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**GPIOE17_STS**	**GPIOE16_STS**	**Reserved**	**GPIOE14_STS**	**GPIOE13_STS**	**GPIOE12_STS**	**GPIOE11_STS**	**GPIOE10_STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIOE17_STS (GPIOE17 Event Status).** Indicates that an active event has been detected at pin 7 of GPIOE Port 1. The event has programmable polarity and the debounce option (see Section 6.3 on page 113). The bit is set by an active level at the GPIOE17 pin. Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: An active event has occurred
6	**GPIOE16_STS (GPIOE16 Event Status).** Same as above for pin 6 of GPIOE Port 1.
5	**Reserved.**
4-0	**GPIOE14_STS to GPIOE10_STS (GPIOE14 to GPIOE10 Event Status).** Same as above for pins 4-0 of GPIOE Port 1.

4.0 System Wake-Up Control (SWC) (Continued)

4.4.6 General-Purpose Status 1 Register 2 (GPE1_STS_2)

This register contains “child” events 16-23 of the GPE1_STS register.

The status bits behave according to the Sticky status bit definition in the ACPI Specification (i.e., the bit is set when the level of the hardware signal is high and is only cleared by the software writing 1 to it).

Power Well: V_{SB3}

Location: Offset 0Ah

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**KBD_EVT3_STS**	**KBD_EVT2_STS**	**KBD_EVT1_STS**	**MS_EVT_STS**	**KBD_ANYK_STS**	**RI1_EVT_STS**	**RI2_EVT_STS**	**Reserved**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**KBD_EVT3_STS (Keyboard Event 3 Status).** Indicates that “PM Key 3” was pressed and that the event was identified by the Keyboard/Mouse Wake-Up Detector. The bit is set only if the Keyboard/Mouse Wake-Up Detector is in Power Management Keys mode (see Section 4.3.7 on page 96). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: The “PM Key 3” key was pressed on the keyboard
6	**KBD_EVT2_STS (Keyboard Event 2 Status).** Indicates that “PM Key 2” was pressed and that the event was identified by the Keyboard/Mouse Wake-Up Detector. The bit is set only if the Keyboard/Mouse Wake-Up Detector is in Power Management Keys mode (see Section 4.3.7 on page 96). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: The “PM Key 2” key was pressed on the keyboard
5	**KBD_EVT1_STS (Keyboard Event 1 Status).** Indicates that a keyboard event occurred and was identified by the Keyboard/Mouse Wake-Up Detector. The event type depends on the selected operation mode for the Keyboard/Mouse Wake-Up Detector (see Sections 4.3.7 and 4.3.8 on page 96.): • Pressing any key or a sequence of special keys in Special Key Sequence mode • Pressing a sequence of keys in Password mode • Pressing the “PM Key 1” in Power Management Keys mode Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: A keyboard event occurred
4	**MS_EVT_STS (Mouse Event Status).** Indicates that a mouse event occurred and was identified by the Keyboard/Mouse Wake-Up Detector (see Section 4.3.8 on page 97). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: A mouse event occurred
3	**KBD_ANYK_STS (Keyboard Any-Key Status).** Indicates that a key was pressed and that the event was identified by the Keyboard/Mouse Wake-Up Detector. The bit is set only if the Keyboard/Mouse Wake-Up Detector is in Fast Any-Key mode (see Section 4.3.7 on page 96). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: A keyboard event occurred
2	**RI1_EVT_STS ($\overline{\text{RI1}}$ Event Status).** Indicates that a telephone ring signal was received at Serial Port 1 and the event was identified by the RI Wake-Up Detector. The bit is set by a high-to-low transition at the $\overline{\text{RI1}}$ pin (see Section 4.2.1 on page 82). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: A telephone ring signal was received at Serial Port 1

4.0 System Wake-Up Control (SWC) (Continued)

Bit	Description
1	**RI2_EVT_STS ($\overline{\text{RI2}}$ Event Status).** Indicates that a telephone ring signal was received at Serial Port 2 and the event was identified by the RI Wake-Up Detector. The bit is set by a high-to-low transition at the $\overline{\text{RI2}}$ pin (see Section 4.2.1 on page 82). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: A telephone ring signal was received at Serial Port 2
0	**Reserved.**

4.4.7 General-Purpose Status 1 Register 3 (GPE1_STS_3)

This register contains “child” events 24-31 of the GPE1_STS register.

The status bits behave according to the Sticky Status Bit definition in the ACPI Specification (i.e., the bit is set when the level of the hardware signal is high and is only cleared by the software writing 1 to it).

Power Well: V_{SB3}

Location: Offset 0Bh

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**HM_STS**	**MOD_IRQ _STS**	**MS_IRQ _STS**	**KBD_IRQ _STS**	**Reserved**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5	**HM_STS (HM Alarm Status).** Is set if an event enabled for SCI generation was detected by the Health Management module. For the list of events and routing to SWC module (to the HM_STS bit) see “SCI and SMI Events Routing” in the “Events Notification” section. Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: An enabled event was detected by the Health Management module
4	**MOD_IRQ_STS (Modules IRQ Event Status).** Indicates that an IRQ was generated by one of the Legacy modules (FDC, Parallel Port, Serial Ports 1 and 2, InfraRed Port), or Health Management module. The bit is set only if the IRQ is enabled for wake-up (bit 4 of the Standard configuration register at index 70h) and the related module is active; see Section 3.2.3 on page 39. Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: An enabled IRQ (from one of the Legacy or Health Management modules) is active
3	**MS_IRQ_STS (Mouse IRQ Event Status).** Indicates that an IRQ was generated by the mouse interface section of the KBC module. The bit is set only if the IRQ is enabled for wake-up (bit 4 of the Mouse Logical Device configuration register at index 70h) and the KBC module is active (see Section 3.2.3 on page 39). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: An enabled IRQ from the mouse interface section of the KBC module is active
2	**KBD_IRQ_STS (Keyboard IRQ Event Status).** Indicates that an IRQ was generated by the keyboard interface section of the KBC module. The bit is set only if the IRQ is enabled for wake-up (bit 4 of the Keyboard Logical Device configuration register at index 70h) and the KBC module is active (see Section 3.2.3 on page 39). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: An enabled IRQ from the keyboard interface section of the KBC module is active
1-0	**Reserved.**

4.0 System Wake-Up Control (SWC) (Continued)

4.4.8 General-Purpose Enable 1 Register 0 (GPE1_EN_0)

This register contains “child” events 0-7 of the GPE1_EN register.

The enable bits behave according to the Enable Bit definition in the ACPI Specification (i.e., the bit can be read or written by software).

Power Well: V_{SB3}

Location: Offset 0Ch

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**GPIOE07_EN**	**GPIOE06_EN**	**GPIOE05_EN**	**GPIOE04_EN**	**GPIOE03_EN**	**GPIOE02_EN**	**GPIOE01_EN**	**GPIOE00_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIOE07_EN (GPIOE07 Event Enable).** Enables an active event at pin 7 of GPIOE Port 0 to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event to set PME_STS
6-0	**GPIOE06_EN to GPIOE00_EN (GPIOE06 to GPIOE00 Event Enable).** Same as above for pins 6-0 of GPIOE Port 0.

4.4.9 General-Purpose Enable 1 Register 1 (GPE1_EN_1)

This register contains “child” events 8-15 of the GPE1_EN register.

The enable bits behave according to the Enable Bit definition in the ACPI Specification (i.e., the bit can be read or written by software).

Power Well: V_{SB3}

Location: Offset 0Dh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**GPIOE17_EN**	**GPIOE16_EN**	**Reserved**	**GPIOE14_EN**	**GPIOE13_EN**	**GPIOE12_EN**	**GPIOE11_EN**	**GPIOE10_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIOE17_EN (GPIOE17 Event Enable).** Enables an active event at pin 7 of GPIOE Port 1 to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event to set PME_STS
6	**GPIOE16_EN (GPIOE16 Event Enable).** Same as above for pin 6 of GPIOE Port 1.
5	**Reserved.**
4-0	**GPIOE14_EN to GPIOE10_EN (GPIOE14 to GPIOE10 Event Enable).** Same as above for pins 4-0 of GPIOE Port 1.

4.0 System Wake-Up Control (SWC) (Continued)

4.4.10 General-Purpose Enable 1 Register 2 (GPE1_EN_2)

This register contains “child” events 16-23 of the GPE1_EN register.

The enable bits behave according to the Enable Bit definition in the ACPI Specification (i.e., the bit can be read or written by software).

Power Well: V_{SB3}

Location: Offset 0Eh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**KBD_EVT3_EN**	**KBD_EVT2_EN**	**KBD_EVT1_EN**	**MS_EVT_EN**	**KBD_ANYK_EN**	**RI1_EVT_EN**	**RI2_EVT_EN**	**Reserved**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**KBD_EVT3_EN (Keyboard Event 3 Enable).** Enables the event of pressing “PM Key 3” (on the keyboard) to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of pressing the “PM Key 3” on the keyboard to set PME_STS
6	**KBD_EVT2_EN (Keyboard Event 2 Enable).** Enables the event of pressing “PM Key 2” (on the keyboard) to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of pressing the “PM Key 2” on the keyboard to set PME_STS
5	**KBD_EVT1_EN (Keyboard Event 1 Enable).** Enables the event of pressing any key, key sequence or “PM Key 1” (on the keyboard) to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of pressing a sequence of keys or the “PM Key 1” on the keyboard to set PME_STS
4	**MS_EVT_EN (Mouse Event Enable).** Enables a mouse event identified by the Keyboard/Mouse Wake-Up Detector to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of mouse event identified by the Keyboard/Mouse Wake-Up Detector to set PME_STS
3	**KBD_ANYK_EN (Keyboard Any-Key Enable).** Enables the event of pressing any key (on the keyboard) to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of pressing any key on the keyboard to set PME_STS
2	**RI1_EVT_EN ($\overline{\text{RI1}}$ Event Enable).** Enables a telephone ring, received at Serial Port 1 and identified by the RI Wake-Up Detector, to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of telephone ring event received at Serial Port 1 to set PME_STS
1	**RI2_EVT_EN ($\overline{\text{RI2}}$ Event Enable).** Enables a telephone ring, received at Serial Port 2 and identified by the RI Wake-Up Detector, to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of telephone ring event received at Serial Port 2 to set PME_STS
0	**Reserved.**

4.0 System Wake-Up Control (SWC) (Continued)

4.4.11 General-Purpose Enable 1 Register 3 (GPE1_EN_3)

This register contains “child” events 24-31 of the GPE1_EN register.

The enable bits behave according to the Enable Bit definition in the ACPI Specification (i.e., the bit can be read or written by software).

Power Well: V_{SB3}

Location: Offset 0Fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**HM_EN**	**MOD_IRQ _EN**	**MS_IRQ _EN**	**KBD_IRQ _EN**	**Reserved**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5	**HM_EN (HM Alarm Enable).** Enables an alarm condition detected by the Health Management (HM) module to set the PME_STS bit in GPE_STS register. 0: Disable event (default) 1: Enable event from an alarm condition detected by the HM module to set PME_STS
4	**MOD_IRQ_EN (Modules IRQ Event Enable).** Enables an active IRQ from one of the Legacy modules, Health Management module to set the PME_STS bit in GPE_STS register. 0: Disable event (default) 1: Enable event of an active IRQ to set PME_STS
3	**MS_IRQ_EN (Mouse IRQ Event Enable).** Enables an IRQ generated by the mouse interface section of the KBC module to set the PME_STS bit in GPE_STS register. 0: Disable event (default) 1: Enable event of an IRQ generated by the mouse interface section of the KBC module to set PME_STS
2	**KBD_IRQ_EN (Keyboard IRQ Event Enable).** Enables an IRQ generated by the keyboard interface section of the KBC module to set the PME_STS bit in GPE_STS register. 0: Disable event (default) 1: Enable event of an IRQ generated by the keyboard interface section of the KBC module to set PME_STS
1-0	**Reserved.**

4.0 System Wake-Up Control (SWC) (Continued)

4.5 SYSTEM WAKE-UP CONTROL REGISTER BITMAP

Table 41. SWC Register Map with Base Address at Index 60h, 61h

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	SLEDCTL LED_OPT=01	Reserved						BLINK	GRN_YLW
	Reserved LED_OPT=other	Reserved							
01h	SWC_CTL	LOCKSCF	Reserved	GOOD_ BAT	Reserved		LAST_PW R_STATE	LED_OPT	
02h	ALEDCTL LED_OPT=00	Reserved		LEDCFG	LEDPOL	Reserved		LEDMOD	
	XLEDCTL LED_OPT=10	Reserved						SLP_S1	SW_CTL
	Reserved LED_OPT=other	Reserved							
03h	LEDBLNK LED_OPT=00	Reserved	GRNBLNK			Reserved	YLWBLNK		
	Reserved LED_OPT=other	Reserved							
04h	KBDWKCTL	KBDMODE		EVT3CFG		EVT2CFG		EVT1CFG	
05h	PS2CTL	DISPAR	MSEVCFG			KBEVCFG			
06h	KDSR	Keyboard Data							
07h	MDSR	Reserved					Mouse Data		
08h	PS2KEY0	Data Byte of Key							
09h	PS2KEY1	Data Byte of Key							
0Ah	PS2KEY2	Data Byte of Key							
0Bh	PS2KEY3	Data Byte of Key							
0Ch	PS2KEY4	Data Byte of Key							
0Dh	PS2KEY5	Data Byte of Key							
0Eh	PS2KEY6	Data Byte of Key							
0Fh	PS2KEY7	Data Byte of Key							

4.0 System Wake-Up Control (SWC) (Continued)

Table 42. ACPI Register Map with Base Address at Index 62h, 63h

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	GPE1_STS	Reserved							PME_STS
01h-03h	Reserved	Reserved							
04h	GPE1_EN	Reserved							PME_EN
05h-07h	Reserved	Reserved							
08h	GPE1_STS_0	GPIOE07_STS	GPIOE06_STS	GPIOE05_STS	GPIOE04_STS	GPIOE03_STS	GPIOE02_STS	GPIOE01_STS	GPIOE00_STS
09h	GPE1_STS_1	GPIOE17_STS	GPIOE16_STS	Reserved	GPIOE14_STS	GPIOE13_STS	GPIOE12_STS	GPIOE11_STS	GPIOE10_STS
0Ah	GPE1_STS_2	KBD_EVT3_STS	KBD_EVT2_STS	KBD_EVT1_STS	MS_EVT_STS	KBD_ANYK_STS	RI1_EVT_STS	RI2_EVT_STS	Reserved
0Bh	GPE1_STS_3	Reserved		HM_STS	MOD_IRQ_STS	MS_IRQ_STS	KBD_IRQ_STS	Reserved	
0Ch	GPE1_EN_0	GPIOE07_EN	GPIOE06_EN	GPIOE05_EN	GPIOE04_EN	GPIOE03_EN	GPIOE02_EN	GPIOE01_EN	GPIOE00_EN
0Dh	GPE1_EN_1	GPIOE17_EN	GPIOE16_EN	Reserved	GPIOE14_EN	GPIOE13_EN	GPIOE12_EN	GPIOE11_EN	GPIOE10_EN
0Eh	GPE1_EN_2	KBD_EVT3_EN	KBD_EVT2_EN	KBD_EVT1_EN	MS_EVT_EN	KBD_ANYK_EN	RI1_EVT_EN	RI2_EVT_EN	Reserved
0Fh	GPE1_EN_3	Reserved		HM_EN	MOD_IRQ_EN	MS_IRQ_EN	KBD_IRQ_EN	Reserved	

5.0 LPC Bus Interface

With the exception of the Glue Functions, the host can access all the functional blocks of the PC8374L device through the LPC bus.

5.1 OVERVIEW

The LPC host interface supports I/O Read and Write, Memory Read and Write, 8-bit Firmware Memory Read and Write, and 8-bit DMA transactions, as defined in Intel's *LPC Interface Specification, Revision 1.1*.

5.2 LPC TRANSACTIONS

The LPC interface of the PC8374L device responds to the following LPC transactions:

- I/O read and write cycles
- Memory read and write cycles
- 8-bit Firmware Memory read and write
- 8-bit DMA read and write cycles
- DMA request

5.3 INTERRUPT SERIALIZER

The Interrupt Serializer translates parallel interrupt request (PIRQ) signals received from internal IRQ sources into serial interrupt request data transmitted over the SERIRQ bus. This enables devices that support only parallel IRQs to be integrated into a system that supports only serial IRQs like the LPC bus.

Each internal IRQ is fed into a Mapping, Enable and Polarity Control block, which maps the IRQ to its associated IRQ numbers (see Table 14 on page 41). The resulting IRQs are then fed into the Interrupt Serializer, where they are translated into serial data and then transmitted over the SERIRQ bus. Each interrupt number is assigned a time slot in the SERIRQ frame. Different IRQ sources in the PC8374L device cannot share the same interrupt number and thus cannot share the same time slot in the SERIRQ frame.

When a transition is detected on an IRQ source, the new value of the IRQ source is transmitted over the SERIRQ bus during the corresponding IRQ slot. For example, when a transition on the Serial Port IRQ is detected, the new value of the Serial Port IRQ is transmitted during time slot n of the SERIRQ bus.

6.0 General-Purpose Input/Output (GPIO) Ports

This chapter describes one 8-bit port. A device may include a combination of several ports with different implementations. For device specific implementation, see Section 3.14 on page 73.

6.1 OVERVIEW

The GPIO port is an 8-bit port, connected to eight pins. It features:

- Software capability to control and read pin levels.
- Flexible system notification by several means, based on the pin level or level transition.
- Ability to capture and route events and their associated status.
- Back-drive protected pins.

GPIO port operation is associated with two sets of registers:

- Pin Configuration registers mapped in the Device Configuration space. These registers are used to configure the logical behavior of each pin. There are two or three registers for each GPIO pin: GPIO Pin Configuration registers 1 and 2 (GPCFG1, GPCFG2) and the GPIO Pin Event Routing register (GPEVR).
- Four 8-bit runtime registers: GPIO Data Out (GPDO), GPIO Data In (GPDI), GPIO Event Enable (GPEVEN) and GPIO Event Status (GPEVST). These registers are mapped in the GPIO device I/O space (which is determined by the base address registers in the GPIO Device Configuration). They are used to control and/or read the pin values and to handle system notification. Each runtime register corresponds to the 8-pin port, such that bit 'n' in each one of the four registers is associated with GPIOXn pin, where 'X' is the port number.
- An additional optional runtime register: GPIO Data In/Out (GPDIO). This register is also mapped in the GPIO device I/O space, but at a separate location from the above group of four runtime registers. It contains the same data-out value as the GPDO register and the same data-in value as the GPDI register.

Each GPIO pin is associated with configuration bits and the corresponding bit slice of the four runtime registers, as shown in Figure 15.

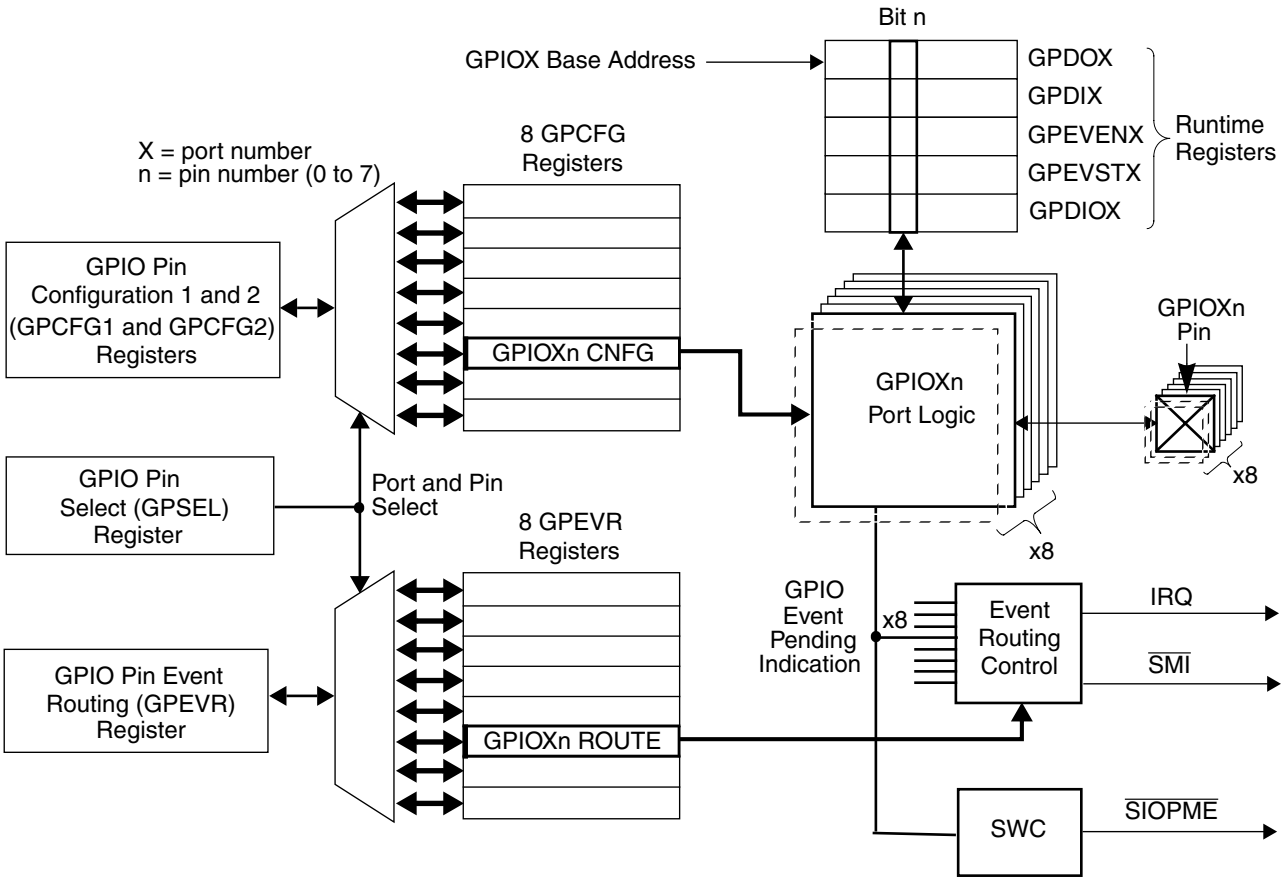


Figure 15. GPIO Port Architecture

6.0 General-Purpose Input/Output (GPIO) Ports (Continued)

The functionality of the GPIO port is divided into:

- Basic functionality: Includes configuration of, writing to and reading from the GPIO pins (described in Section 6.2)
- Enhanced functionality: Includes wake-up event detection and system notification (described in Section 6.3)

In addition, the GPIO port can be operated in one of the following modes:

- Separate Data I/O: Separate registers are available for Data In (GPDI) and for Data Out (GPDO) in addition to the Data In/Out register (GPDIO) and to the enhanced functionality registers (GPEVST and GPEVEN).
- Common Data I/O: Only the Data In/Out register (GPDIO) is available.

6.2 BASIC FUNCTIONALITY

The basic functionality of each GPIO pin is based on four configuration bits and a bit slice of runtime registers GPDO and GPDI (or GPDIO). The configuration and operation of a single pin GPIOXn (pin 'n' in port 'X') is shown in Figure 16 (note that for clarity, the static pull-down resistor is not shown):

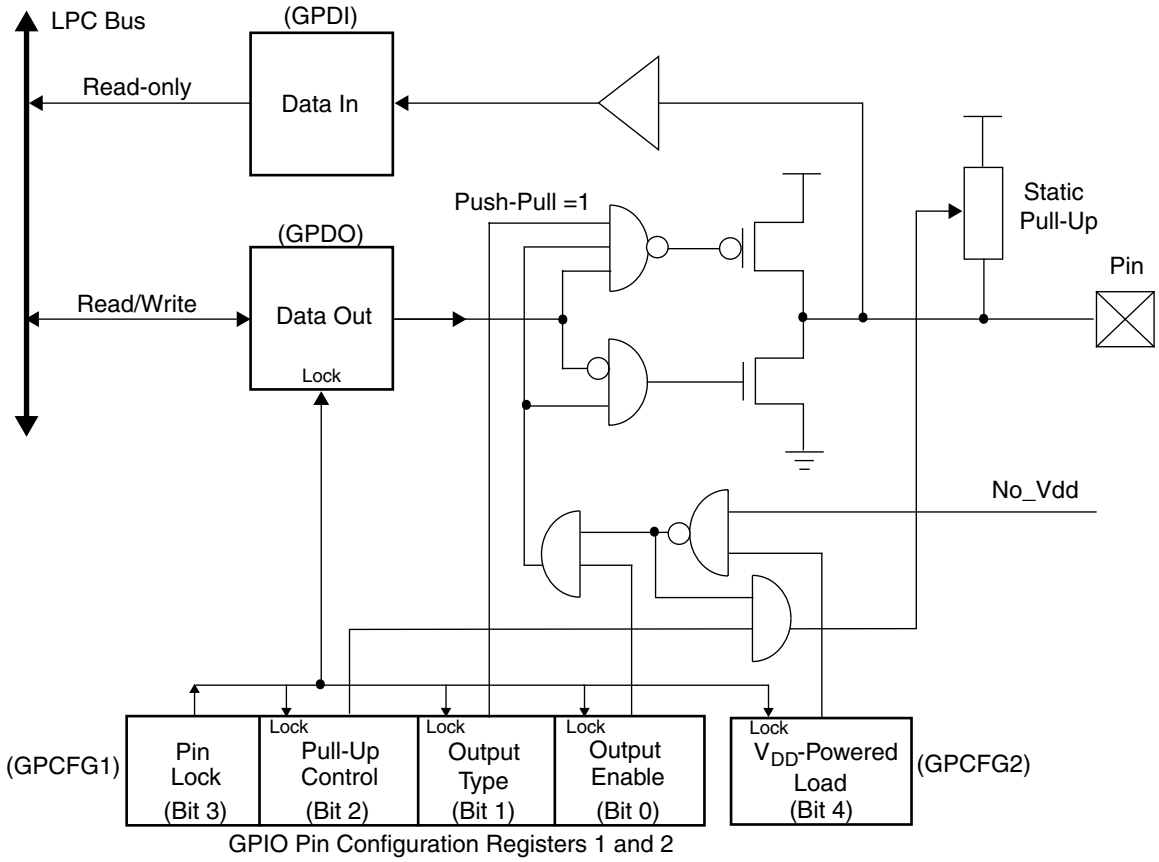


Figure 16. GPIO Basic Functionality

6.2.1 Configuration Options

The GPCFG1 register controls the following basic configuration options, as shown in Figure 16:

- Port Direction: Controlled by Output Enable (bit 0).
- Output Type: Push-pull vs. open-drain; it is controlled by Output Buffer Type (bit 1) by enabling/disabling the upper transistor of the output buffer.
- Static Pull-Up: May be added to any type of port (input, open-drain or push-pull). It is controlled by Pull-Up Control (bit 2)
- Pin Lock: GPIO pin may be locked to prevent any changes in the output value and/or the output configuration. The lock is controlled by bit 3. It disables writes to GPDO and GPDIO registers bits, to bits 7, 3–0 of GPCFG1 register (including the Lock bit itself) and to bit 4 of GPCFG2 register.

6.0 General-Purpose Input/Output (GPIO) Ports (Continued)

The GPCFG2 register controls the Load Protection configuration option:

- V_{DD}-Powered Load: Disables the Output Buffer (if enabled), the Static Pull-Up (if enabled), the Static Pull-Down (if enabled) and the Input Buffer if the specific GPIO pin is connected to a V_{DD}-powered device and V_{DD3} power to the PC8374L is not present (No_Vdd). This function is controlled by the V_{DD}-powered Load bit (bit 4).

6.2.2 Operation

If the output is enabled, the value that is written to the GPDO or GPDIO registers is driven to the pin. Reading from the GPDO register returns its contents regardless of the actual pin value or the port configuration.

The GPDI register is a read-only register. Reading from the GPDI register returns the actual pin value regardless of its source (the port itself or an external device). Writing to this register is ignored.

Reading from the GPDIO register returns the actual pin value regardless of its source.

Activation of the GPIO module is controlled by device-specific configuration bits. When this module is inactive, access through the LPC bus to the runtime registers (GPDI, GPDO and GPDIO) is disabled; however, there is no change in the GPDO and GPDIO values and therefore there is no effect on the outputs of the pins.

The configuration and data registers of each GPIO pin are reset according to the setting of VDDLOAD bit in GPCFG2 register (see Section 3.14.6 on page 77).

6.0 General-Purpose Input/Output (GPIO) Ports (Continued)

6.3 EVENT HANDLING AND SYSTEM NOTIFICATION

The enhanced GPIO port (GPIOE) supports system notification based on event detection. This functionality is based on configuration bits and a bit slice of runtime registers GPEVEN and GPEVST. The configuration and operation of the event detection capability is shown in Figure 17. System notification is described in Section 6.3.2.

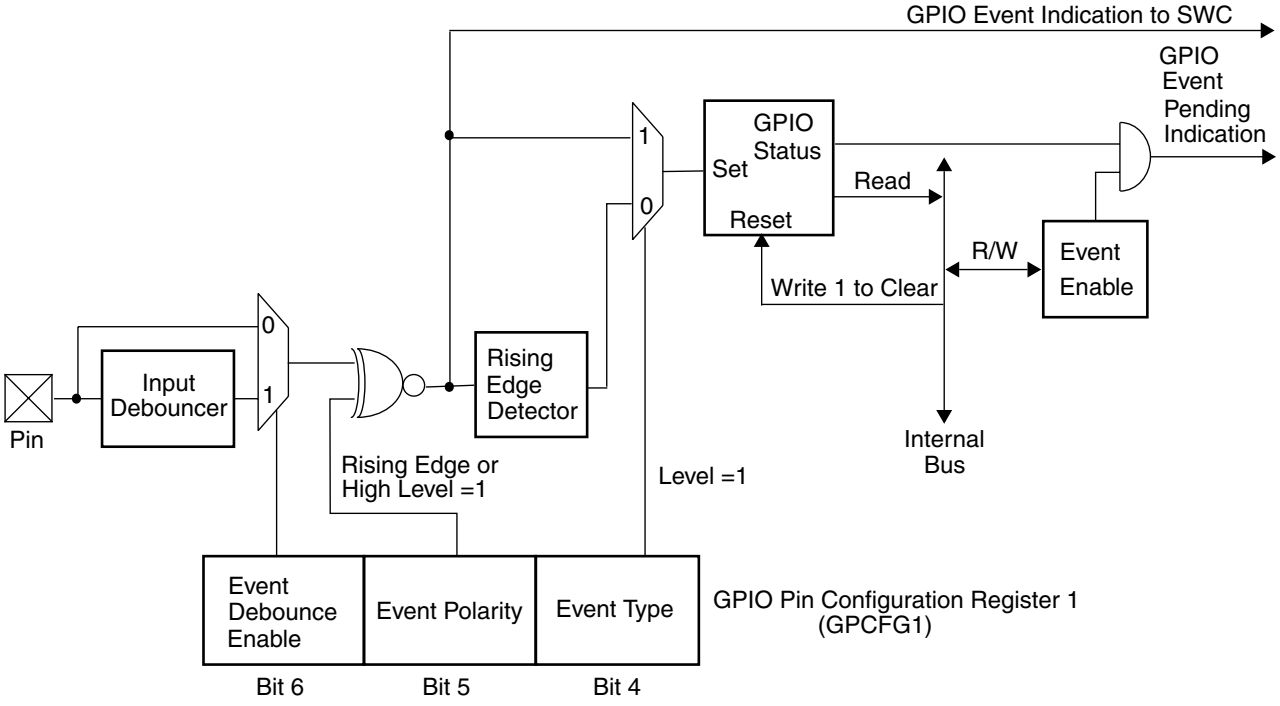


Figure 17. Event Detection

6.3.1 Event Configuration

Each pin in the GPIO port is a potential input event source. The event detection can trigger a system notification on predetermined behavior of the source pin. The GPCFG1 register determines the event detection trigger type for system notification.

Event Debounce Enable

The input signal can be debounced for at least 16 ms, before entering the detector. To ensure that the signal is stable, the signal state is transferred to the event detector only after a debouncing period during which the signal has no transitions. The debouncer adds a delay equal to the debouncing period to both assertion and de-assertion of the event pending indicator (IRQ, $\overline{\text{SMI}}$, SCI). The debounce is controlled by Event Debounce Enable (bit 6 of GPCFG1 register).

Event Type and Polarity

Two trigger types of event detection are supported: edge and level. An edge event may be detected on a source pin transition either from high to low or low to high. A level event may be detected when the source pin is either at high or low level. The trigger type is determined by Event Type (bit 4 of GPCFG1 register). The direction of the transition (for edge) or the polarity of the active level (for level) is determined by Event Polarity (bit 5 of GPCFG1 register).

Active edge refers to a change in a GPIO pin level that matches the Event Polarity bit (1 for rising edge and 0 for falling edge). *Active level* refers to the GPIO pin level that matches the Event Polarity bit (1 for high level and 0 for low level). The corresponding bit in GPEVST register is set by hardware whenever an active edge or an active level is detected regardless of the GPEVEN register setting. Writing 1 to the Status bit clears it to 0. Writing 0 is ignored.

A GPIO pin is in event pending state if an active event has occurred (the corresponding bit in GPEVST register is set) and the corresponding bit in GPEVEN register is set.

6.0 General-Purpose Input/Output (GPIO) Ports (Continued)

6.3.2 System Notification

System notification on GPIO-triggered events is achieved by asserting at least one of the following output pins:

- Interrupt Request (via the Interrupt Serializer in the LPC Bus Interface).
- System Management Interrupt ($\overline{SMI}$).

The system notification for each GPIO pin is controlled by the corresponding bit in GPEVEN register together with the bits of GPEVR register. System notification by a GPIO pin is enabled if the corresponding bit of GPEVEN register is set to 1. The bits of the GPEVR register select the means of system notification (IRQ, $\overline{SMI}$) that the detected GPIO event is routed to. The event routing mechanism is shown in Figure 18.

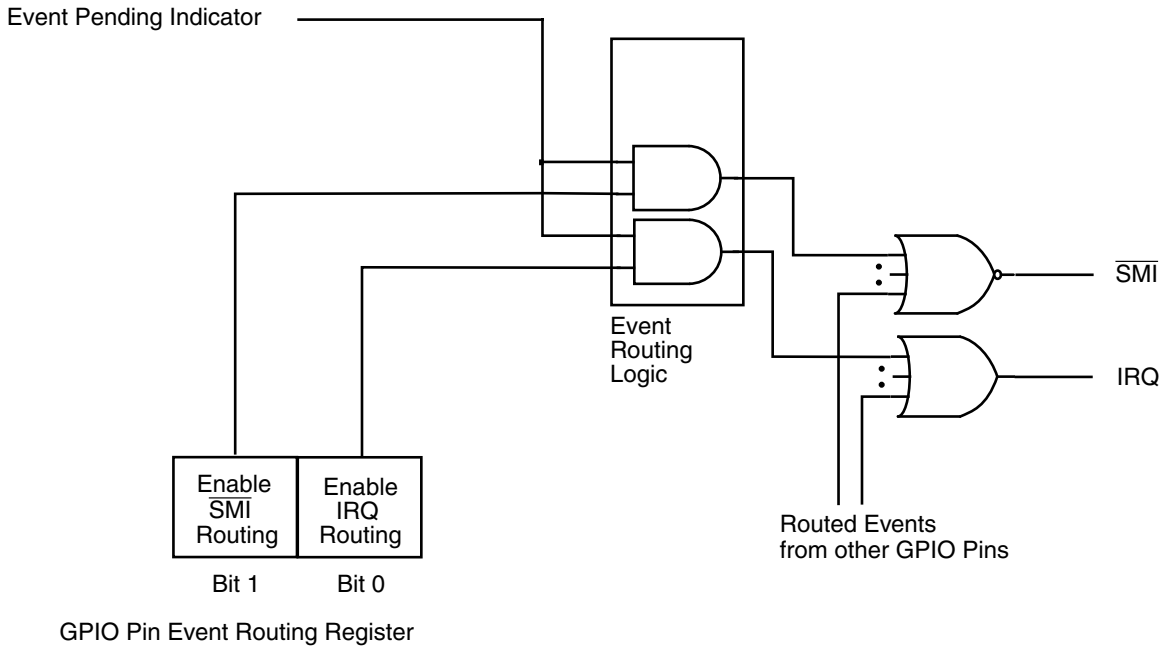


Figure 18. GPIO Event Routing Mechanism for System Notification

The system notification to the target is asserted if at least one GPIO pin is in event pending state.

The selection of the target (for system notification) is determined by the GPEVR register. The specific IRQ number is determined by the IRQ selection procedure of the device configuration. The assertion of IRQ (as a means of system notification) is disabled either when the GPIO functional block is deactivated or when V_{DD3} power is off.

The assertion of $\overline{SMI}$ is independent of the activation of the GPIO functional block.

System notification through IRQ, $\overline{SMI}$ or SCI (see Section 4.2.4 on page 86) can be initiated by software by writing to the Data Out bit (in GPDO or GPDIO register) of a GPIO pin. This is possible only if the output of the corresponding GPIO pin is enabled, pin multiplexing is selected for the GPIO function (see Section 1.3 on page 16) and the GPIO event is routed to IRQ, $\overline{SMI}$ or SCI. System notification is asserted according to the actual level at the GPIO pin driven by the GPIO output and/or by external circuitry. The level driven by the GPIO output should not cause a contention with the level driven by the external circuitry.

A pending edge event may be cleared by clearing the corresponding GPEVST bit. However, a level event source may not be released by software (except for disabling the source) as long as the pin is at active level. When level event is used, it is also recommended to disable the input debouncer.

On deactivation of the GPIO functional block and while V_{DD3} power is off, access through the LPC bus to the runtime registers (GPEVST and GPEVEN) is disabled. All means of system notification that include the target IRQ number are detached from the GPIO and de-asserted.

When V_{DD3} power is off, the status bits of the V_{DD}-powered GPIO pins (VDDLOAD = 1) are cleared, however the status bits of the V_{SB}-powered GPIO pins (VDDLOAD = 0) are not affected.

Before enabling any system notification, it is recommended to set the desired event configuration and then verify that the status registers are cleared.

6.0 General-Purpose Input/Output (GPIO) Ports (Continued)

6.4 GPIO PORT REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register (data written to this address is sent to a different register).
- W = Write (see above).
- RO = Read-only.
- WO = Write-only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

6.4.1 GPIO Pin Configuration Registers Structure

For each GPIO Port, there is a group of eight identical sets of configuration registers. Each set is associated with one GPIO pin. The entire group is mapped to the PnP configuration space. The mapping scheme is based on the GPSEL register (see Section 3.14.3 on page 75), which functions as an index register for the pin, and the selected GPCFG1, GPEVR and GPCFG2 registers, which reflect the configuration of the currently selected pin (see Table 43). All of these registers are V_{SB3} powered.

Table 43. GPIO Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
F0h	GPIO Pin Select register (GPSEL)	R/W	V_{SB3}	00h
F1h	GPIO Pin Configuration register 1 (GPCFG1)	Varies per bit	V_{SB3}	40h
F2h	GPIO Pin Event Routing register (GPEVR)	R/W or RO	V_{SB3}	01h
F3h	GPIO Pin Configuration register 2 (GPCFG2)	R/W or RO	V_{SB3}	00h
F8h	GPIO Mode Select register (GPMODE)	R/W or RO	V_{SB3}	01h

6.4.2 GPIO Port Runtime Register Map

All of these registers are V_{SB3} powered.

Table 44. GPIO Port Runtime Register Map

Offset	Mnemonic	Register Name	Type		Power Well	Reset	Section
			SEPDIO[1] = 1	SEPDIO = 0			
Device specific[2]	GPDO	GPIO Data Out	R/W	RO	V_{SB3}	FFh	6.4.3
Device specific[2]	GPDI	GPIO Data In	RO	RO	V_{SB3}	–	6.4.4
Device specific[2]	GPEVEN	GPIO Event Enable	R/W	RO	V_{SB3}	00h	6.4.5
Device specific[2]	GPEVST	GPIO Event Status	R/W1C	RO	V_{SB3}	00h	6.4.6
Device specific[2]	GPDIO	GPIO Data In/Out	R/W	R/W	V_{SB3}	FFh[3]	6.4.7

1. See Section 3.14.7 on page 78.
2. The location of this register is defined in Section 3.14.1 on page 73.
3. The data read from this register after reset is undefined.

6.0 General-Purpose Input/Output (GPIO) Ports (Continued)

6.4.3 GPIO Data Out Register (GPDO)

Power Well: V_{SB3}

Location: Device specific

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**DATAOUT**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**DATAOUT (Data Out).** Bits 7-0 correspond to pins 7-0 of the specific Port. The value of each bit determines the value driven on the corresponding GPIO pin when its output buffer is enabled. Writing to the bit latches the written data unless the bit is locked by the GPCFG register Lock bit. Reading the bit returns its value regardless of the pin value and configuration. 0: Corresponding pin driven to low 1: Corresponding pin driven or released (according to buffer type selection) to high (default)

6.4.4 GPIO Data In Register (GPDI)

Power Well: V_{SB3}

Location: Device specific

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**DATAIN**							
Reset	X	X	X	X	X	X	X	X

Bit	Description
7-0	**DATAIN (Data In).** Bits 7-0 correspond to pins 7-0 of the specific Port. Reading each bit returns the value of the corresponding GPIO pin. Pin configuration and the GPDO register value may influence the pin value. Write is ignored. 0: Corresponding pin level low 1: Corresponding pin level high

6.4.5 GPIO Event Enable Register (GPEVEN)

Power Well: V_{SB3}

Location: Device specific

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**EVTENA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**EVTENA (Event Enable).** Bits 7-0 correspond to pins 7-0 of the specific Port. Each bit enables system notification by the corresponding GPIO pin. The bit has no effect on the corresponding Status bit in GPEVST register. 0: Event pending by corresponding GPIO pin masked 1: Event pending by corresponding GPIO pin enabled

6.0 General-Purpose Input/Output (GPIO) Ports (Continued)

6.4.6 GPIO Event Status Register (GPEVST)

Power Well: V_{SB3}

Location: Device specific

Type: R/W1C or RO

Bit	7	6	5	4	3	2	1	0
Name	**EVTSTAT**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7–0	**EVTSTAT (Event Status).** Bits 7–0 correspond to pins 7–0 of the specific Port. The setting of each bit is independent of the Event Enable bit in GPEVEN register. An active event sets the Status bit, which may be cleared only by software writing 1 to the bit. 0: No active edge or level detected since last cleared 1: Active edge or level detected

6.4.7 GPIO Data In/Out Register (GPDIO)

Power Well: V_{SB3}

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**DATAINOUT**							
Reset Write	1	1	1	1	1	1	1	1
Reset Read	X	X	X	X	X	X	X	X

Bit	Description
7-0	**DATAINOUT (Data In/Out).** Bits 7-0 correspond to pins 7-0 of the specific Port. The value of each bit determines the value driven on the corresponding GPIO pin when its output buffer is enabled. Writing to the bit latches the written data unless the bit is locked by the GPCFG register Lock bit. Reading each bit returns the value of the corresponding GPIO pin. Pin configuration and the data-out value may influence the pin value. 0: Corresponding pin driven to low; pin level read low. 1: Corresponding pin driven or released (according to buffer type selection) to high; pin level read high (default).

7.0 Glue Functions

This chapter describes the glue functions integrated in the PC8374L device.

7.1 OVERVIEW

This module contains the glue functions. Most of them operate independently of the other functions and of the other modules in the PC8374L device.

The glue functions are divided into three groups:

- Power-related functions:
  - Highest active Main supply reference (REF5V)
  - Highest active Standby supply reference (REF5V_STBY)
  - Resume reset ($\overline{\text{RSMRST}}$)
  - Main power good (PWRGD_3V)
  - Power distribution control ($\overline{\text{BKFD\_CUT}}$, LATCHED_BF_CUT)
  - Main power supply control ($\overline{\text{PS\_ON}}$)
- Miscellaneous functions:
  - Hard-disk LED indicator control ($\overline{\text{HD\_LED}}$)
- SMBus support functions:
  - SMBus voltage translation (CC_DDCSCL, CC_DDCSDA, 5V_DDCSCL, 5V_DDCSDA)
  - SMBus isolation (SMB1_SCL, SMB1_SDA, SMB2_SCL, SMB2_SDA)

Each function is described in the following sections.

7.2 FUNCTIONAL DESCRIPTION

7.2.1 Highest Active Main Supply Reference

This function generates the REF5V analog output signal (see specification in Section 10.2.11 on page 216). When the Main power supply is turned on or off, the REF5V signal tracks either the V_{DD3} or V_{DD5} power supplies, whichever has a higher voltage.

The circuit that generates the REF5V output is composed of two parts:

- One part tracks the V_{DD3} supply voltage and is implemented in the PC8374L device.
- One part tracks the V_{DD5} supply voltage and is implemented by an external resistor connected to the V_{DD5} power supply.

Figure 19 shows a simplified diagram of the circuit that generates the REF5V analog output signal

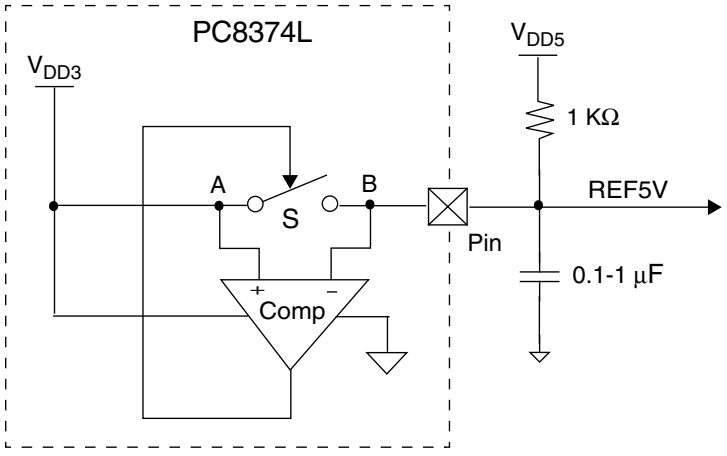


Figure 19. REF5 Generation (Simplified Diagram)

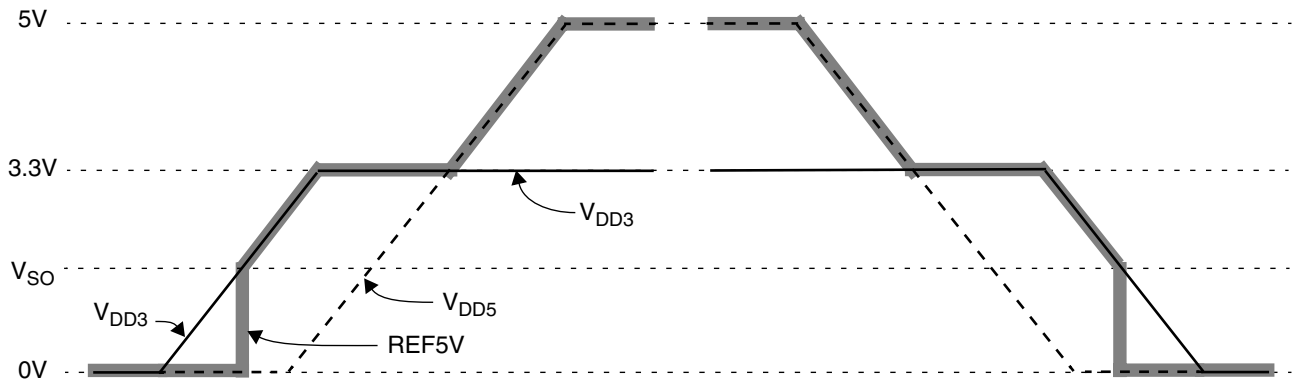
7.0 Glue Functions (Continued)

The voltage levels at both sides of switch "S" are measured by the comparator ("Comp"), which controls the state of the switch as follows:

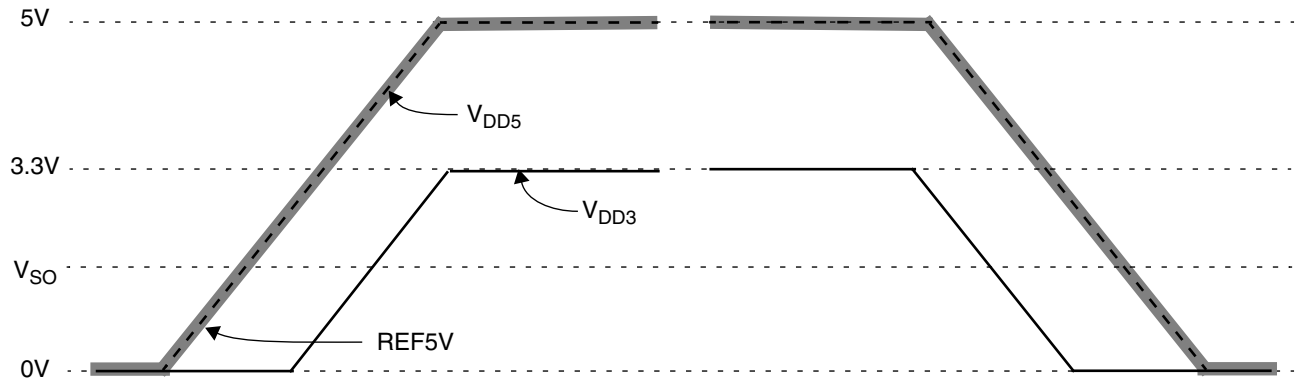
- If $V_A > V_B$, then $V_{DD3} > V_{DD5}$; the switch is **closed**, and the output voltage $V_{REF5V} = V_{DD3}$.
- If $V_A < V_B$, then $V_{DD3} < V_{DD5}$; the switch is **open**, and the output voltage $V_{REF5V} = V_{DD5}$, through the external 1 KΩ resistor, is connected to the V_{DD5} power supply.

The internal circuit is powered from the V_{DD3} supply. For $V_{DD3} < V_{SO}$, switch "S" is **open**; therefore, the V_{REF5V} output tracks only the V_{DD5} supply. Figure 20 shows REF5 output in four cases of V_{DD3} and V_{DD5} ramp up and ramp down.

a. V_{DD3} Ramps Up Before and Ramps Down After V_{DD5}



b. V_{DD3} Ramps Up After and Ramps Down Before V_{DD5}



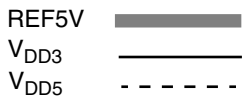


Figure 20. REF5 as a Function of V_{DD3} and V_{DD5}

Table 45 defines the DC characteristics of the REF5 output, relative to the V_{DD3} supply. For the AC characteristics, see "Highest Active Main and Standby Supply Reference" on page 232.

Table 45. REF5V DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SO}	Switch Open, V_{DD3} Voltage Range	$0 < V_{DD5} < 5.5V$	0	1.5[1]	V
V_{TRK}	Output Voltage Tracking of V_{DD3} Voltage[1],	$1.5V < V_{DD3}$, $V_{DD5} < V_{DD3} + 150$ mV	− 150	+ 150	mV

1. Not tested. Guaranteed by characterization.

7.0 Glue Functions (Continued)

7.2.2 Highest Active Standby Supply Reference

This function generates the REF5V_STBY analog output signal (see specification in Section 10.2.11 on page 216). When the Standby power supply is turned on or off, the REF5V_STBY signal tracks either the V_{SB3} or V_{SB5} power supplies, whichever has a higher voltage.

The circuit that generates the REF5V_STBY output is composed of two parts:

- One part tracks the V_{SB3} supply voltage and is implemented in the PC8374L device.
- One part tracks the V_{SB5} supply voltage and is implemented by an external resistor connected to the V_{SB5} power supply.

Figure 21 shows a simplified diagram of the circuit that generates the REF5V_STBY analog output signal

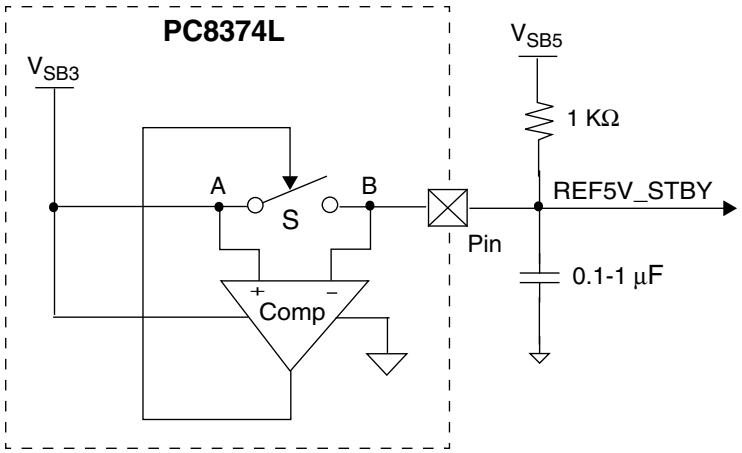


Figure 21. REF5_STBY Generation (Simplified Diagram)

The voltage levels at both sides of switch “S” are measured by the comparator (“Comp”), which controls the state of the switch as follows:

- If $V_A > V_B$, then $V_{SB3} > V_{SB5}$; the switch is **closed** and the output voltage $V_{REF5V\_STBY} = V_{SB3}$
- If $V_A < V_B$, then $V_{SB3} < V_{SB5}$; the switch is **open** and the output voltage $V_{REF5V\_STBY} = V_{SB5}$, through the external 1 KΩ resistor, is connected to the V_{SB5} power supply

The internal circuit is powered from the V_{SB3} supply. For $V_{SB3} < V_{SO}$, switch “S” is **open**; therefore, the V_{REF5V_STBY} output tracks only the V_{SB5} supply. Figure 22 shows the behavior of the REF5V_STBY output in four cases of V_{SB3} and V_{SB5} ramp up and ramp down.

7.0 Glue Functions (Continued)

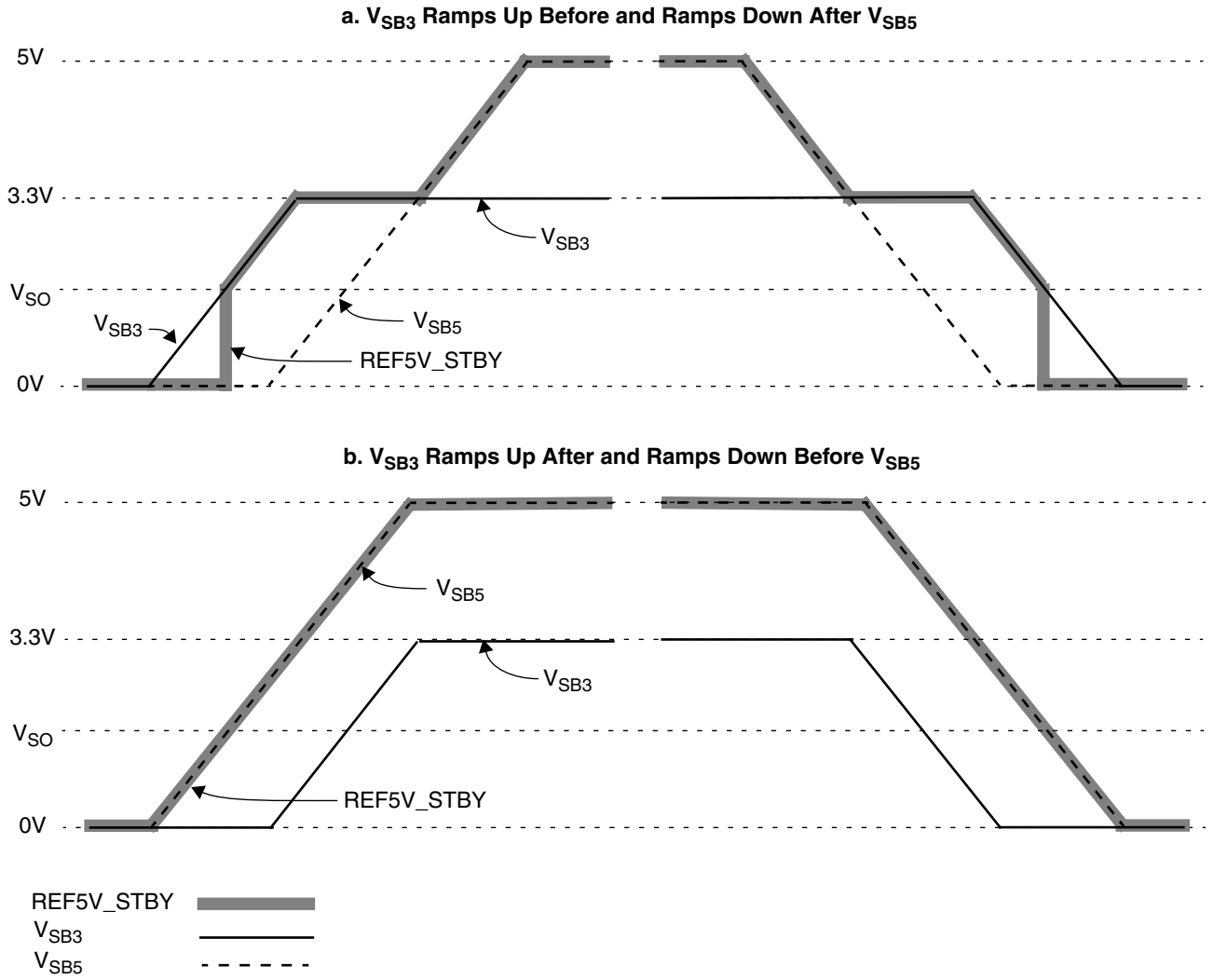


Figure 22. REF5_STBY as a Function of V_{SB3} and V_{SB5}

Table 45 defines the DC characteristics of the REF5_STBY output relative to the V_{SB3} supply. For the AC characteristics, see “Highest Active Main and Standby Supply Reference” on page 232.

Table 46. REF5V_STBY DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SO}	Switch Open, V_{SB3} Voltage Range	$0 < V_{SB5} < 5.5V$	0	1.5[1]	V
V_{TRK}	Output Voltage Tracking of V_{SB3} Voltage[1],	$1.5V < V_{SB3}$, $V_{SB5} < V_{SB3} + 150$ mV	− 150	+ 150	mV

1. Not tested. Guaranteed by characterization.

7.0 Glue Functions (Continued)

7.2.3 Resume Reset

This function generates the $\overline{\text{RSMRST}}$ signal by sensing the voltage level at the V_{SB5} analog input (see specification in Section 10.2.7 on page 215). The $\overline{\text{RSMRST}}$ signal serves both as a Power-Up reset and as a "Brown-Out" reset for the system resume power well (powered by the V_{SB3} or V_{SB5} supplies).

The Resume Reset circuit compares the voltage at the V_{SB5} input with a threshold value (V_{TRIP}). When the V_{SB3} supply voltage is active, the circuit generates the $\overline{\text{RSMRST}}$ active low output signal, as follows:

- When V_{SB5} rises above V_{TRIP}, the $\overline{\text{RSMRST}}$ signal switches from low to high after a t_{RD} delay.
- When V_{SB5} falls below V_{TRIP}, the $\overline{\text{RSMRST}}$ signal switches from high to low after a t_{FD5} delay.
- When a glitch shorter than t_{GA} (the time V_{SB5} is below V_{TRIP}) occurs at the V_{SB5} input, the $\overline{\text{RSMRST}}$ signal is not guaranteed to react (remains high).

The Resume Reset circuit is powered by the V_{SB3} supply. When the V_{SB5} supply voltage is active, the circuit compares the V_{SB3} power supply voltage with the threshold value (V_{SB3ON} or V_{SB3OFF}); see Section 10.1.5 on page 213. As a result, the $\overline{\text{RSMRST}}$ active low output signal is generated, as follows:

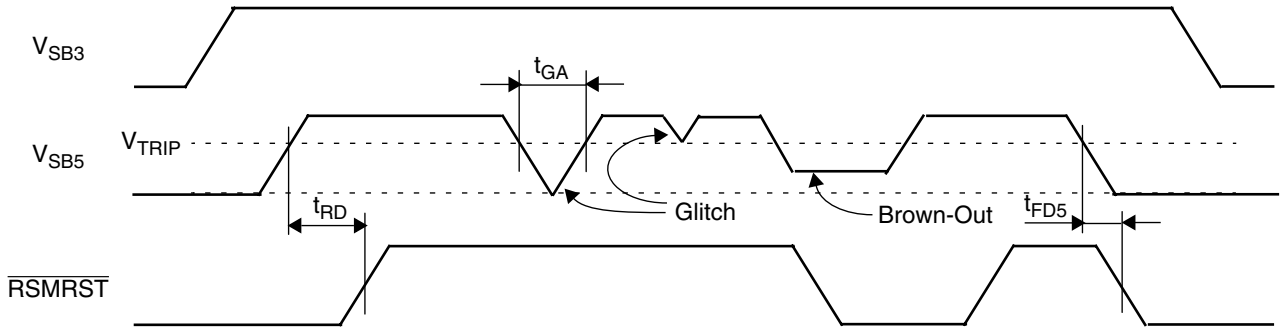
- When V_{SB3} rises above V_{SB3ON}, the $\overline{\text{RSMRST}}$ signal switches from low to high after a t_{RD} delay.
- When V_{SB3} falls below V_{SB3OFF}, the $\overline{\text{RSMRST}}$ signal switches from high to low after a t_{FD3} delay.
- When a glitch shorter than t_{GA} (the time V_{SB3} is below V_{SB3OFF}) occurs at the V_{SB3} input, the $\overline{\text{RSMRST}}$ signal is not guaranteed to react (remains high).

When the V_{SB3} power supply is off, the $\overline{\text{RSMRST}}$ output is at low level (active) having an internal impedance of Z_{OFF}.

The delays in $\overline{\text{RSMRST}}$ switching, generated by the Resume Reset circuit, are independent of the toggling of any of the clock domains of the PC8374L device.

Figure 23 shows the behavior of the $\overline{\text{RSMRST}}$ output at V_{SB3} and V_{SB5} switching.

a. V_{SB5} Switching, V_{SB3} Steady



b. V_{SB3} Switching, V_{SB5} Steady

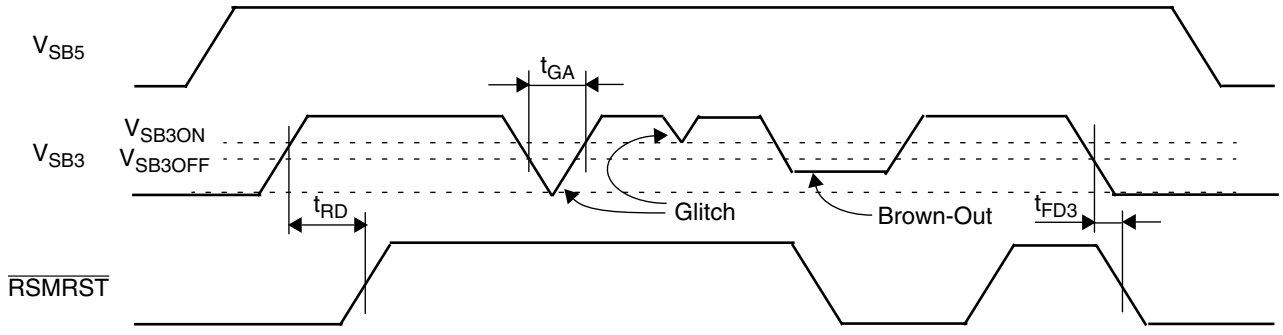


Figure 23. $\overline{\text{RSMRST}}$ at V_{SB5} and V_{SB3} Switching

Table 47 defines the DC characteristics of the Resume Reset circuit. For the AC characteristics, see "Resume Reset" on page 232.

7.0 Glue Functions (Continued)

Table 47. Resume Reset Circuit DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{TRIP}	V_{SB5} Threshold Level	V_{SB3} = 3.3V ±10%	4.05	4.5	V
Z_{OFF}	Output Impedance at V_{SB3} Off[1]	V_{SB3} = 0V, V_{SB5} = 5V ±10%	7	10	KΩ

1. Not tested. Guaranteed by characterization.

7.2.4 Main Power Good

This function generates the PWRGD_3V signal, indicating that the Main power supply voltage is valid. The PWRGD_3V signal indicates to system components that their input power supplies are valid. PWRGD_3V is de-asserted immediately when $\overline{SLP\_S3}$ is asserted or PWRGD_PS is de-asserted. It is asserted with t_{PSD} delay after PWRGD_PS is asserted. Figure 24 shows a simplified diagram of the circuit that generates the PWRGD_3V signal.

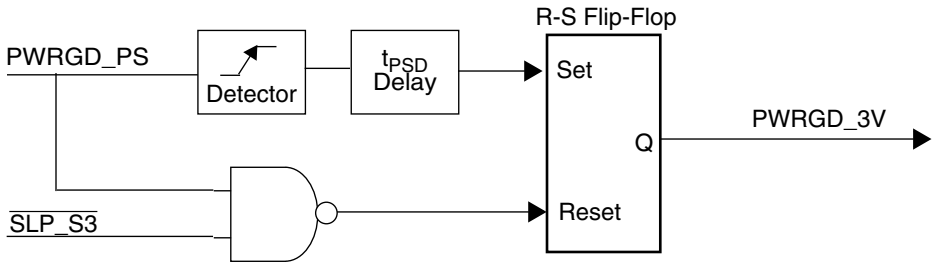


Figure 24. PWRGD_3V Generation (Simplified Diagram)

For the AC characteristics, see “Main Power Good” on page 234.

7.2.5 Power Distribution Control

This function generates the $\overline{BKFD\_CUT}$ and the LATCHED_BF_CUT power distribution control signals.

An active low $\overline{BKFD\_CUT}$ signal is generated when the Main power supply voltage is valid (PWRGD_PS = high) **and** the system is **not** in one of the S3 to S5 sleep states ($\overline{SLP\_S3}$ = high).

The LATCHED_BF_CUT signal is generated from $\overline{BKFD\_CUT}$ and $\overline{SLP\_S5}$ as follows:

- Rising edge of $\overline{BKFD\_CUT}$ while the system is **not** in S5 sleep state ($\overline{SLP\_S5}$ = high) sets LATCHED_BF_CUT to high.
- Falling edge of $\overline{BKFD\_CUT}$ while the system is **not** in S5 sleep state ($\overline{SLP\_S5}$ = high) resets LATCHED_BF_CUT to low.
- When the system is in S5 sleep state ($\overline{SLP\_S5}$ = low), LATCHED_BF_CUT is reset to low.

Figure 25 shows a simplified diagram of the circuit that generates the $\overline{BKFD\_CUT}$ and the LATCHED_BF_CUT signals.

7.0 Glue Functions (Continued)

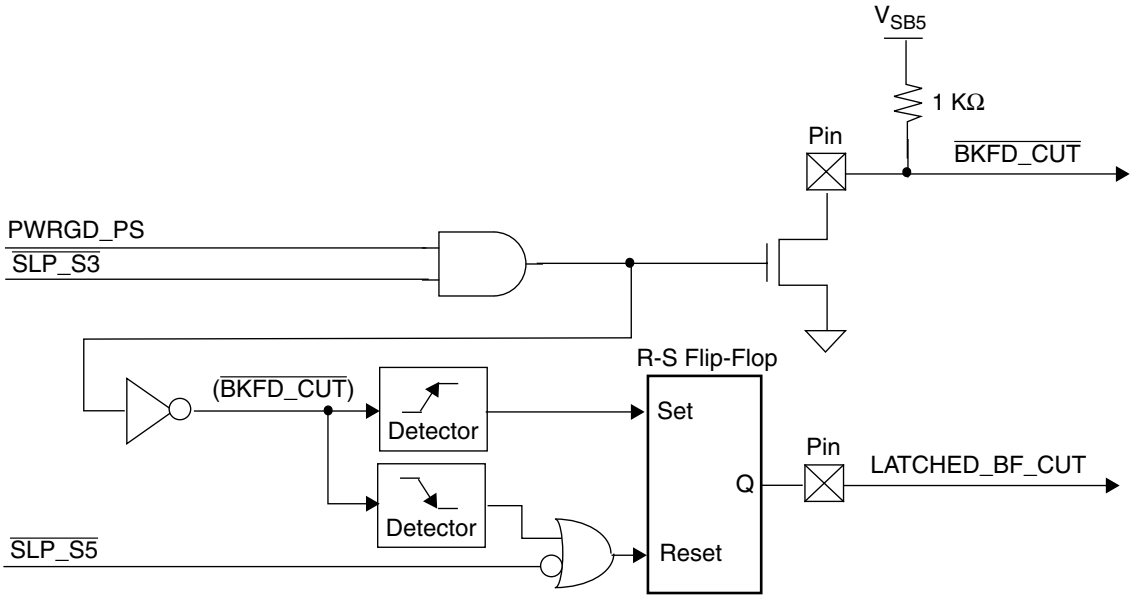


Figure 25. BKFD_CUT and LATCHED_BF_CUT Generation (Simplified Diagram)

For the AC characteristics, see "Power Distribution Control" on page 234.

7.2.6 Main Power Supply Control

This function generates the PS_ON signal, which turns the Main power supply on and off.

The Main power supply is turned on by an active low PS_ON signal, generated when all of the following are true:

- The processor is currently inserted in its socket (CPU_PRESENT = low).
- The system is **not** in one of the S3 to S5 sleep states (SLP_S3 = high).
- None of the conditions for ETC exists (see Section 8.2.10 on page 139).
- If an ETC event has occurred, the system has gone through one of the S3 to S5 sleep states (rising edge on SLP_S3).

Figure 26 shows a simplified diagram of the circuit that generates the PS_ON signal.

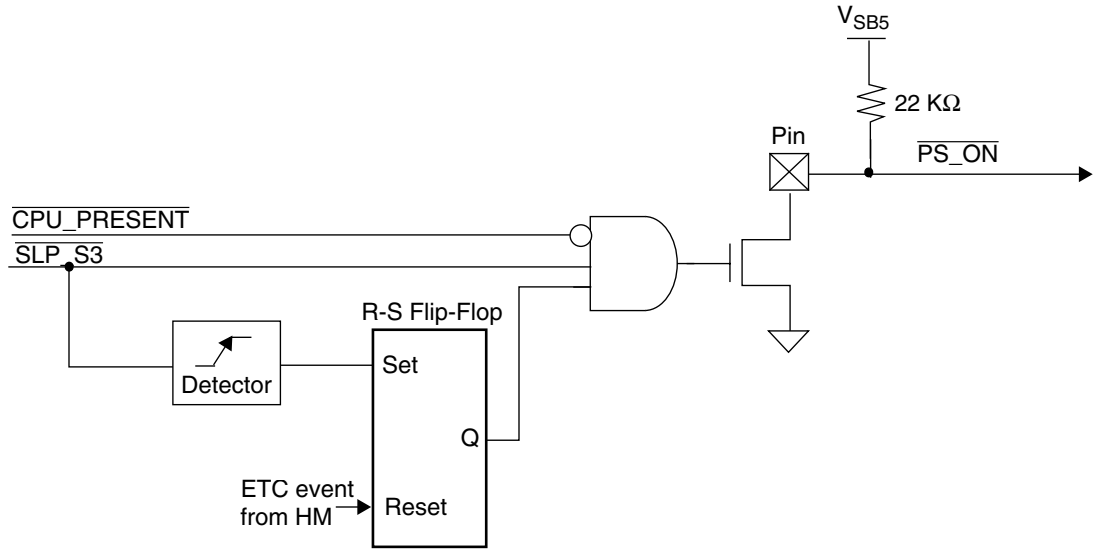


Figure 26. PS_ON Generation (Simplified Diagram)

For the AC characteristics, see "Main Power Supply Control" on page 235.

7.0 Glue Functions (Continued)

7.2.7 Hard-Disk LED Indicator Control

This function generates the $\overline{\text{HD\_LED}}$ signal, which controls the Hard Drive, red LED indicator.

The Hard Drive LED is turned on by an active low $\overline{\text{HD\_LED}}$ signal, generated when at least one of the $\overline{\text{PRIMARY\_HD}}$ **or** $\overline{\text{SECONDARY\_HD}}$ **or** $\overline{\text{SCSI}}$ pins is active (low).

Figure 27 shows a simplified diagram of the circuit that generates the $\overline{\text{HD\_LED}}$ signal.

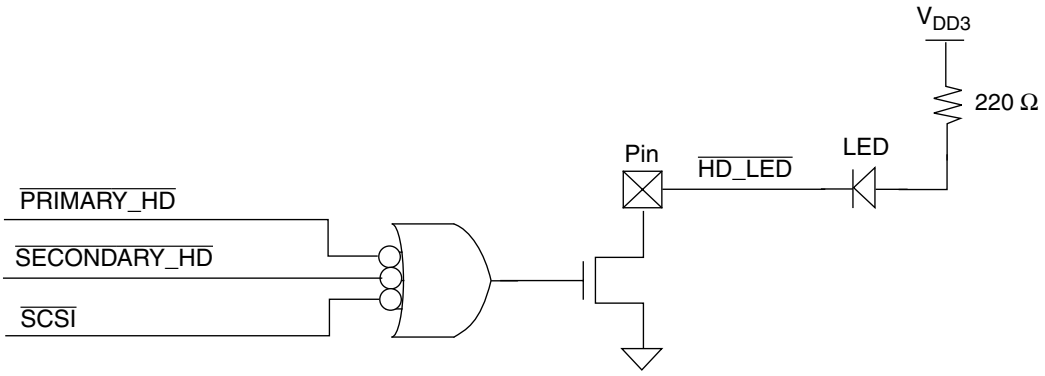


Figure 27. $\overline{\text{HD\_LED}}$ Generation (Simplified Diagram)

7.2.8 SMBus Voltage Translation

This function performs "passive" level translation between the V_{DD3}-powered (or 2.5V-powered) CC_DDCSCL and CC_DDCSDA signals and the V_{DD5}-powered 5V_DDCSCL and 5V_DDCSDA signals, respectively, for interfacing the Data Display Channel.

The signals connected to the CC_DDCSCL, CC_DDCSDA, 5V_DDCSCL and 5V_DDCSDA pins are compatible with Intel's SMBus (*Specification Rev 1.1, Dec. 11, 1998*) two-wire synchronous serial interface specifications.

The CC_DDCSCL and 5V_DDCSCL pins are connected through a switch. This switch is controlled by a Level Translation Control circuit, according to the voltage levels at the CC_DDCSCL and 5V_DDCSCL pins (for the DC characteristics, see Section 10.2.12 on page 216):

- For $V_{IN} < V_{ISC}$ at **either** pin, the switch is closed; therefore, both pins (CC_DDCSCL, and 5V_DDCSCL) are held at low level.
- For $V_{IN} > V_{ISO}$ at **both** pins, the switch is open; therefore, each pin is pulled up to high level by the external resistor connected to V_{DD3} or V_{DD25} (2.5V Main Power) (for the CC_DDCSCL pin) and to V_{DD5} (for the 5V_DDCSCL pin).

In addition, when the V_{DD3} power is off, the switch is open, regardless of the voltage levels at the CC_DDCSCL and 5V_DDCSCL pins.

The CC_DDCSDA and 5V_DDCSDA pins are connected through a similar level translation circuit and behave like CC_DDCSCL and 5V_DDCSCL.

Figure 28 shows simplified a diagram of the circuit that performs SMBus voltage translation.

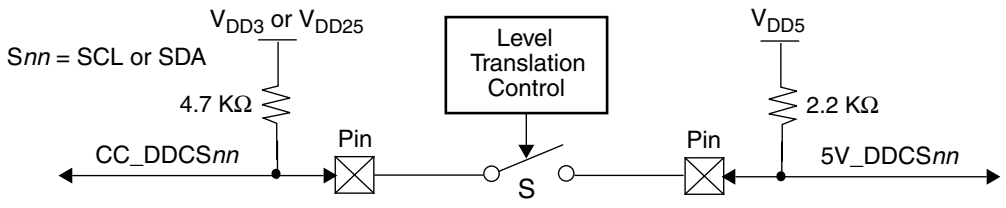


Figure 28. SMBus Voltage Translation for V_{DD3} Tolerant Chipset Cluster (Simplified Diagram)

7.0 Glue Functions (Continued)

7.2.9 SMBus Isolation

When the Main power is off, this function performs “passive” bus isolation between the SMB1_SCL, SMB1_SDA signals and the SMB2_SCL, SMB2_SDA signals respectively. The bus isolation enables the operation of the serial bus section connected to Standby power, if the other serial bus is connected to the Main power and the Main power is off.

The signals connected to the SMB1_SCL, SMB1_SDA, SMB2_SCL and SMB2_SDA pins are compatible Intel's SMBus (*Specification Rev 1.1, Dec. 11, 1998*) two-wire synchronous serial interface specifications.

The SMB1_SCL and SMB2_SCL pins are connected through a switch. This switch is controlled by the voltage levels at the SMB1_SCL and SMB2_SCL pins (for the DC characteristics, see Section 10.2.12 on page 216):

- For $V_{IN} < V_{ISC}$ at **either** pin, the switch is closed; therefore, both pins (SMB1_SCL, and SMB2_SCL) are held at low level.
- For $V_{IN} > V_{ISO}$ at **both** pins, the switch is open; therefore, each pin is pulled up to high level by the external resistor connected to V_{SUP1} (for the SMB1_SCL pin) and to V_{SUP2} (for the SMB2_SCL pin).

In addition, when the Main power supply voltage is not valid (PWRGD_PS = low), the switch is forced open and the unpowered SMB*x*_SCL signal is disconnected from the powered SMB*x*_SCL signal (*x* is either 1 or 2). This isolation between the two signals prevents the loading of the powered SMB*x*_SCL signal by the unpowered SMB*x*_SCL signal.

The SMB1_SDA and SMB2_SDA pins are connected through a similar level isolation circuit and behave like SMB1_SCL and SMB2_SCL.

Figure 29 shows a simplified diagram of the circuit that performs SMBus isolation.

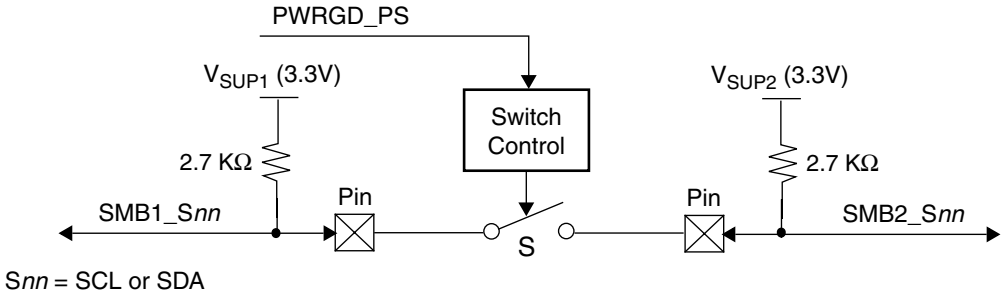


Figure 29. SMBus Isolation (Simplified Diagram)

For the AC characteristics, see “SMBus Voltage Translation and Isolation Timing” on page 235.

8.0 Health Management (HM)

8.1 OVERVIEW

The PC8374L Health Management module ("HM") is the digital component of the System Health Monitor and Control function. The analog component of this function is implemented by external LMxx Sensor devices. Communication between the HM and an external LMxx Sensor is automatic (i.e., there is no need for user intervention/configuration) via the SensorPath bus, working in asynchronous mode.

The HM monitors three temperature channels, five voltage channels, and four tachometer channels.

In addition, it generates three FANPWM fan drive control signals.

The temperature data, together with the tachometer data, can be used to control the FANPWM signals.

The HM automatically reads temperature and voltage data from an LMxx Sensor device. It then compares the data to the limit data set in the Limit registers and sets the corresponding status bits.

Access to the HM is possible through a dedicated SMBus interface (HMSMBus with HMSCL and HMSDA pins) or through the LPC interface.

The HM can automatically use one of the following four LMxx device options to supply temperature and voltage inputs:

- **LM96011** provides two temperature channels (one remote diode, one ambient) and five voltage channels
- **LM96011+LM95010** provides three temperature channels (one remote diode, two ambient) and five voltage channels
- **LM96010** provides three temperature channels (two remote diode, one ambient) and five voltage channels
- **LM96012** provides three temperature channels (two remote diode, one ambient) and no voltage channels

Note: When the LM96011, LM96010 or LM96012 is used, it should be strapped as device number 1.
When the LM95010 is used, it should be strapped as device number 2.

Figure 30 on page 128 shows the HM Block Diagram.

8.2 FUNCTIONAL DESCRIPTION

The HM functions are:

- Sensor Monitoring (voltage channels and temperature channels monitoring)
- Fan monitoring (fan speed measurements)
- Fan control (driving fans)

8.2.1 Health Management Module Access

The HM can be accessed either through the LPC Bus or through a dedicated SMBus (HMSMBus).

For access through the HMSMBus, the HM responds to SMBus transactions addressed according to the SMBus slave address set by the HM SMBus Configuration register (see Section 3.7.12 on page 59). For the SMBus transaction protocols, see Section 8.3 on page 140.

Access through the LPC Bus is done through the HM LPC Access registers. For more details see Section 8.4 on page 141.

Simultaneous write accesses through the LPC Bus and SMBus may cause unpredictable results. However, for simultaneous read accesses, consistency is retained (except for the 16-bit measurement data registers, such as Fan Tachometer Reading 1-3 MSB/LSB).

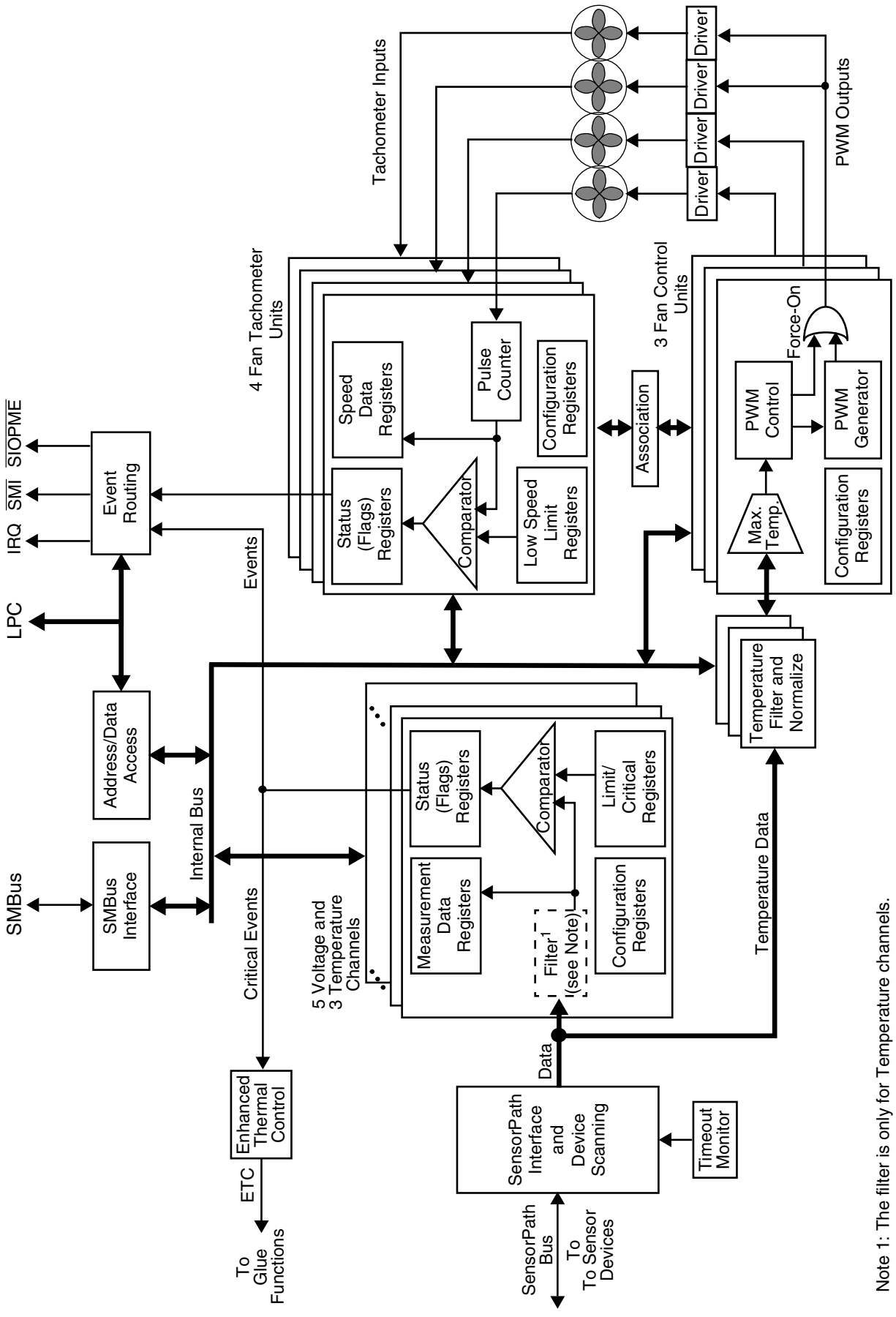
8.2.2 SensorPath Bus

The HM communicates with the LMxx Sensor devices via the SensorPath bus. The HM is the bus master on the SensorPath bus and supports asynchronous mode.

The SensorPath bus uses timing encoding based on a 360 KHz internal clock to provide the following types of bit signals over the bus (the HM supports all five types):

- Data Bit 0
- Data Bit 1
- Start Bit
- Attention Request
- Reset

8.0 Health Management (HM) (Continued)



Note 1: The filter is only for Temperature channels.

Figure 30. Health Management Block Diagram

8.0 Health Management (HM) (Continued)

A “reset” operation on the bus can be initiated by either the HM or the LMxx Sensor devices generating a reset signal. After V_{SB} Power-Up reset, the HM holds the SensorPath bus low, thus resetting the bus. Then, the HM releases the reset from the SensorPath bus. Following this, the HM is ready to respond to “attention requests” from an LMxx Sensor device.

When the HM performs a reset operation on the bus, the reset signal is followed by a sequence of 16 data bits (all 0), without a preceding start bit. If the SensorPath bus remains in reset state (i.e., SWD is held low by an LMxx Sensor device) for more than the maximum reset time allowed, the HM assumes that a major SensorPath bus failure occurred and proceeds accordingly (see Section 8.2.10 on page 139).

When an LMxx Sensor device contains new data, it sends an attention request to the HM. The HM answers the attention request by initiating a read transaction on the SensorPath bus.

If a SensorPath data or start bit collides with an attention request, the data or start bit is automatically resent. In addition, if a parity or acknowledge error occurs on the first transaction attempt, two more successive attempts are made by the HM. If the LMxx Sensor device detects an acknowledge error, it generates an attention request and sets BER bit in the Device Status register. The HM checks BER bit in response to each attention request to determine the cause of the request.

The HM initiates read/write transactions on the SensorPath bus and supports data fields of up to 32 bits.

8.2.3 Temperature Monitoring

Temperature is monitored for three different temperature zones (or channels). The temperature data is updated and stored as a 2’s complement, left-aligned, 8-bit data byte in the Temperature Reading Zone1-3 registers.

The following table shows the association of the LMxx temperature channels to the HM temperature channels for each possible LMxx devices setup:

Table 48. Temperature Channels per LMxx Device

LMxx Device Setup	Temperature Zones		
	Temperature Zone1	Temperature Zone2	Temperature Zone3
LM96011	LM96011 Remote	LM96011 Ambient	-
LM96011+LM95010	LM96011 Remote	LM96011 Ambient	LM95010 Ambient
LM96010	LM96010 First Remote	LM96010 Ambient	LM96010 Second Remote
LM96012	LM96012 First Remote	LM96012 Ambient	LM96012 Second Remote

When Temperature Zone3 is associated with an LM95010 device, the associated Temperature Reading Register represents a value between -127°C (81h) and +127°C (7Fh), with the LSBit representing a value of 1°C. For Temperature Zones 1 and 2, and for Temperature Zone3 when it is not associated with an LM95010 device, the Temperature Reading register depends on the setting of the ZONEn_RANGE bit in the Monitor Control Register (see Section 8.5.54 on page 176).

If ZONEn_RANGE is 0, the LSBit of the Reading register represents a value of 1°C (thus temperature values are between -127°C (81h) and +127°C (7Fh)). If ZONEn_RANGE bit is 1 the LSBit of the Reading register represents a value of 2°C (thus temperature values are between -254°C (81h) and +254°C (7Fh)); see also Figure 37 on page 158. A value of 80h always represents a sensor error.

The temperature data can be gain- and offset-corrected with the values in the Temperature Zone ‘n’ Gain and Offset Correction registers (see Section 8.5.56 on page 178 to Section 8.5.58). The temperature gain correction in the HM can be used to compensate the non-ideality of the thermal diodes (remote diode) connected to the LMxx Sensor devices (see the “Application Hints” section in the respective *LMxx Datasheet*). The offset correction can be used to compensate the PCB trace resistance between the remote diode and the LMxx Sensor device (see “Application Hints” in the respective *LMxx Datasheet*).

The temperature data can be low-pass filtered by setting the TEMP_FILT bit in the Monitoring Control register (see Section 8.5.54 on page 176). The rise time of the filter (0% to 95% of the incoming temperature change) is 673 ms.

The temperature data is compared with configurable low and high limits contained in the Temperature Low Limit Zone1-3 and Temperature High Limit Zone1-3 registers, respectively, and with the critical limit contained in the Temperature Critical Limit Zone1-3 registers. The data format in the limit registers is the same as in the temperature data registers. Note that a value of 80h must not be used as a limit value.

Whenever the temperature data exceeds a low or high limit, a ZONEn_ERR status bit is set in the Status Register 1 (see Section 8.5.23 on page 164), and the ZONEn_STS bit in the HM Sensor Status Register 1 is set (see Section 8.4.8 on page 147). Whenever the temperature data exceeds a critical limit, a CRITn_ERR status bit is set in the Status Register 3 (see Section 8.5.25 on page 166), and the CRITn_STS bit in the HM Sensor Status Register 3 is set (see Section 8.4.12 on page 150).

Temperature data is considered to be in a “Good” state when the data does not exceed any limit. A “Fail” state is when the temperature data exceeds a limit (high, low or critical).

8.0 Health Management (HM) (Continued)

For Low/High Limit: Whenever the temperature data changes state, the associated ZONEn_EV bit in the HM Interrupt Status Register 1 is set (see Section 8.4.4 on page 143). ZONEn_EV can be enabled by the associated ZONEn_EN bit in the HM Interrupt Enable Register 1 (see Section 8.4.6 on page 145) to create an IRQ. ZONEn_EV can also be enabled by the associated xxx_EN bit in the HM SMI/SCI Enable Register 1 (see Section 8.4.13 on page 150) to create an SMI or SCI interrupt.

For Critical Limit: Whenever the temperature data changes state, the associated CRITn_EV bit in the HM Interrupt Status Register 3 is set (see Section 8.4.10 on page 149). CRITn_EV can be enabled by the associated CRITn_EN bit in the HM Interrupt Enable Register 3 (see Section 8.4.11 on page 149) to create an IRQ. CRITn_EV can also be enabled by the associated xxx_EN bit in the HM SMI/SCI Enable Register 3 (see Section 8.4.15 on page 152) to create an SMI or SCI interrupt.

A hysteresis of 4°C can be applied to the limit checking by setting the TEMP_HYST bit in the Monitoring Control register (see Section 8.5.54 on page 176) to 1.

Each of the Temperature channels can be configured as a "V_{DD} Channel" (see Section 8.5.55 on page 177). Temperature Zone1 is configured by default as a V_{DD} channel. When V_{DD3} supply is off, all channels that are configured as V_{DD} channels are disabled. Monitoring for these channels is disabled and all the status bits are reset to 0, including the event bits in the HM Interrupt Status register (see Section 8.4.4 on page 143 and Section 8.4.5). An exception is the status bits associated with the channel critical limits (CRITn_STS), which are not reset when the V_{DD3} supply is off. Channels that are configured as V_{DD} channels are enabled 182 ms after the V_{DD3} supply is turned back on.

8.2.4 Voltage Monitoring

Voltage is monitored for five different voltage channels: 2.5V, Vccp (2.25V), 3.3V, 5V and 12V. The voltage data is updated and stored as an unsigned 8-bit value in the Voltage Reading registers. The data represents a relative value. Nominal voltage value (2.5V for the 2.5V monitoring, 2.25V for Vccp, etc.) is represented by C0h which is 3/4 full-scale (full scale being FFh).

The voltage data is compared with configurable low and high limits contained in the Voltage Low Limit and Voltage High Limit registers, respectively. The data format in the limit registers is the same as in the voltage data registers.

Whenever the voltage data exceeds a limit, an xxx_ERR status bit is set in Status Register 1 and Status Register 2 (see Section 8.5.23 on page 164 to Section 8.5.24), and an xxx_STS bit in the HM Sensor Status Register 1 and HM Sensor Status Register 2 is set (see Section 8.4.8 on page 147 and Section 8.4.9).

Voltage data is considered to be in a "Good" state when the data does not exceed any limit. A "Fail" state is when the voltage data exceeds a limit. Whenever the voltage data changes state, the associated xxx_EV bit in the HM Interrupt Status Register 1 and HM Interrupt Status Register 2 is set (see Section 8.4.4 on page 143 and Section 8.4.5). xxx_EV can be enabled to create an IRQ by the associated xxx_EN bit in the HM Interrupt Enable Register 1 and HM Interrupt Enable Register 2 (see Section 8.4.6 on page 145 and Section 8.4.7). The xxx_EV bit can also be enabled to create an SMI or SCI interrupt by the associated xxx_EN bit in the HM SMI/SCI Enable Register 1 and HM SMI/SCI Enable Register 2 (see Section 8.4.13 on page 150 and Section 8.4.14).

A hysteresis, which is the value of the Voltage Limit register (High or Low) LSBit multiplied by 4 (see Section 8.5.54 on page 176), can be applied to the limit checking by setting the VOLT_HYST bit in the Monitoring Control register to 1.

Each of the Voltage channels can be configured as a "V_{DD} Channel" (see Section 8.5.55 on page 177). Vccp is configured by default as a V_{DD} channel. Whenever V_{DD3} supply is off, the channels configured as V_{DD} channels are disabled. Monitoring for these channels is disabled, and all the status bits are reset to 0, including the event bits in the HM Interrupt Status register (see Section 8.4.4 on page 143 and Section 8.4.5). Channels that are configured as V_{DD} channels are enabled between 91 ms and 182 ms after the V_{DD3} supply is turned back on.

8.2.5 Device Enumeration and HM Channel Association

The three enumeration and HM channel association stages are done in the following order:

1. Device enumeration
2. Extended device enumeration
3. HM channel association

The ready bit in the configuration register (see Section 8.5.22 on page 163) is set to 0 (not-ready) during all three stages.

In any stage, if a SensorPath transaction fails on three successive attempts, the HM assumes a communication error with the LMxx Sensor device occurred and proceeds accordingly (see Section 8.2.10 on page 139).

Device Enumeration

The HM, after V_{SB3} power-up but before it is ready to respond to attention requests, performs device enumeration to identify the LMxx Sensor devices currently connected to the SensorPath bus.

To enumerate the LMxx Sensor devices, the HM reads the Device Number register first from device number 1 and then from device number 2. Note that a read transaction that returns device number=0h indicates a non-existent device number.

If the device enumeration fails to detect any LMxx Sensor device connected to the SensorPath bus, the HM ignores any attention requests generated on the SensorPath bus.

8.0 Health Management (HM) (Continued)

Extended Device Enumeration

Extended Device Enumeration follows the Device Enumeration stage, as follows:

1. If device number 1 exists, the HM reads the device's LM Device ID register and compares it to the LM96011 Device ID value (24h), LM96010 Device ID value (22h) or LM96012 Device ID value (23h).

If the comparison is positive, the HM Channel Association related to the LM96011, LM96010 or LM96012 device takes place, as described in "HM Channel Association", below. If the comparison fails, the HM assumes a communication error with the LMxx Sensor device occurred and proceeds accordingly (see Section 8.2.10 on page 139).

2. If device number 2 exists, the HM reads the device's LM Device ID register and compares it to the LM95010 Device ID value (21h).

If the comparison is positive, the HM Channel Association related to the optional LM95010 device takes place, as described in"HM Channel Association", below.

HM Channel Association

HM Channels are associated with the LMxx sensors according to Table 49 to Table 51.

There are four options:

- **LM96011** provides two temperature channels (one remote diode, one ambient) and five voltage channels
- **LM96011+LM95010** provides three temperature channels (one remote diode, two ambient) and five voltage channels
- **LM96010** provides three temperature channels (two remote diode, one ambient) and five voltage channels
- **LM96012** provides three temperature channels (two remote diode and one ambient) and no voltage channels

The appropriate option is determined by the results of the extended device enumeration.

Table 49. LMxx Sensor Association with HM Channels for LM96011 or LM96011+LM95010

HM Channel	LMxx Sensor		
	Device Number	Function Number	Sensor Number
Temperature Zone1	1	1	SN1 (Thermal diode, 01h)
Temperature Zone2	1	1	SN0 (Local, 00h)
Temperature Zone3[1]	2	1	SN0 (Local, 00h)
Voltage 2.5V	1	2	SN0 (2.5V, 00h)
Voltage Vccp	1	2	SN1 (Vccp, 01h)
Voltage 3.3V	1	2	SN2 (3.3V, 02h)
Voltage 5V	1	2	SN3 (5V, 03h)
Voltage 12V	1	2	SN4 (12V, 04h)

1. Applicable if the optional LM95010 device exists.

Table 50. LMxx Sensor Association with HM Channels for LM96010

HM Channel	LMxx Sensor		
	Device Number	Function Number	Sensor Number
Temperature Zone1	1	1	SN1 (Thermal Diode, 01h)
Temperature Zone2	1	1	SN0 (Local, 00h)
Temperature Zone3	1	1	SN2 (Thermal Diode, 02h)
Voltage 2.5V	1	2	SN0 (2.5V, 00h)
Voltage Vccp	1	2	SN1 (Vccp, 01h)
Voltage 3.3V	1	2	SN2 (3.3V, 02h)
Voltage 5V	1	2	SN3 (5V, 03h)
Voltage 12V	1	2	SN4 (12V, 04h)

8.0 Health Management (HM) (Continued)

Table 51. LMxx Sensor Association with HM Channels for LM96012

HM Channel	LMxx Sensor		
	Device Number	Function Number	Sensor Number
Temperature Zone1	1	1	SN1 (Thermal Diode, 01h)
Temperature Zone2	1	1	SN0 (Local, 00h)
Temperature Zone3	1	1	SN2 (Thermal Diode, 02h)

8.2.6 SensorPath Device Setting and Scanning

SensorPath Devices Setting

For HM support, one LM96011 device, one LM96010 device or one LM96012 device must be connected to the SensorPath bus. If the LM96011 device is connected, an LM95010 device can also be connected (this is optional).

The following settings are performed, depending on the result of the Extended Device Enumeration (see “Extended Device Enumeration” on page 131).

LM96011:
- Function 1 is enabled by setting to 1 EnF1 bit in the Device Control Register (location 0101b).
- Function 2 is enabled by setting to 1 EnF2 bit in the Device Control Register (location 0101b).
- Attention request for function number 1 sensors is enabled by setting ATE bit in Temperature Control register to 1 (location 1010b).
- Temperature sensors SN0 and SN1 are enabled by setting EnS0 and EnS1 in Temperature Control register to 1 (location 1010b).
- Attention request for function number 2 sensors is enabled by setting ATE bit in Voltage Control register to 1 (location 10010b).
- Voltage sensors SN0, SN1, SN2, SN3 and SN4 are enabled by setting EN0, EN1, EN2, EN3 and EN4 in Voltage Control register to 1 (location 10010b).

LM95010:
- Function 1 is enabled by setting to 1 EnF1 bit in the Device Control Register (location 0101b).
- Attention request for function number 1 sensor is enabled by setting ATE bit in Temperature Control register to 1 (location 1010b).
- Temperature sensors SN0 is enabled by setting EnS0 in Temperature Control register to 1 (location 1010b).

LM96010:
- Function 1 is enabled by setting to 1 EnF1 bit in the Device Control Register (location 0101b).
- Function 2 is enabled by setting to 1 EnF2 bit in the Device Control Register (location 0101b).
- Attention request for function number 1 sensors is enabled by setting ATE bit in Temperature Control register to 1 (location 1010b).
- Temperature sensors SN0, SN1 and SN2 are enabled by setting EnS0, EnS1 and EnS2 in Temperature Control register to 1 (location 1010b).
- Attention request for function number 2 sensors is enabled by setting ATE bit in Voltage Control register to 1 (location 10010b).
- Voltage sensors SN0, SN1, SN2, SN3 and SN4 are enabled by setting EN0, EN1, EN2, EN3 and EN4 in Voltage Control register to 1 (location 10010b).

LM96012:
- Function 1 is enabled by setting to 1 EnF1 bit in the Device Control Register (location 0101b).
- Attention request for function number 1 sensors is enabled by setting ATE bit in Temperature Control register to 1 (location 1010b).
- Temperature sensors SN0, SN1 and SN2 are enabled by setting EnS0, EnS1 and EnS2 in Temperature Control register to 1 (location 1010b).

SensorPath Device Scanning

The HM automatically reads the data from the sensors.

After the HM completes device enumeration and setting, it is ready to accept an attention request from an LMxx Sensor device. When an attention request is received, the HM scans all the available LMxx Sensor devices to detect the source of the attention request.

8.0 Health Management (HM) (Continued)

On each LMxx Sensor device scanned, the HM performs the following operations:

1. Reads the “Device Status Register” (Location: 00100b). SF1-3 bits indicate which function requires “attention”.
2. For each LMxx Sensor device function for which an SFx bit is set, the following occurs:
   a. HM reads the contents of the Readout register (Location: FuncBase + 001b).
   b. HM performs temperature sensor processing, as follows:
      i. If EF bit in Readout register is 1, the HM sets to 1 the RD_Fault bit in Status Register 2 (see Section 8.5.24 on page 165) and also sets RD_STS in the HM Sensor Status Register 2 (see Section 8.4.9 on page 148) and RD_EV in the HM Interrupt Status Register 2 (see Section 8.4.5 on page 144). In addition, the temperature data is set to 80h and stored in the associated HM channel register.
      ii. The Readout data is compared with the relevant limits. This step is bypassed if a “sensor error” condition exists.
      iii. The data is stored in the associated HM channel register.
   c. HM performs voltage sensor processing, as follows:
      i. The Readout data is compared with the relevant limits.
      ii. The resulting data is stored in the associated HM channel register.

If a “time-out error” (see “Time-Out Function” below) is detected in an HM channel, the following takes place:

1. The HM aborts the current scanning of the sensors.
2. The SensorPath bus is reset.
3. All the LMxx devices are reset (by writing 1 to the Reset bit in each Device Control Register (location 0101b).
4. Device enumeration and HM channel association are performed.
5. SensorPath device setting is performed.
6. Sensor scanning is restarted on receipt of a new attention request.

Time-Out Function

This function detects either a fatal failure in the LMxx Sensor device or a problem in the SensorPath bus. The maximum time delay (from the previous channel data update) is 728 ms. A new channel data update must occur within this time delay. If a time-out error is detected in device number 1, the HM assumes a communication error with the LMxx Sensor device occurred and proceeds accordingly (see Section 8.2.10 on page 139).

8.2.7 Fan Speed Monitoring

Fan speed is monitored for four different tachometer inputs. The tachometer data is updated every 1 sec and stored as an unsigned 16-bit value in the Fan Tachometer Reading registers (two registers for each tachometer). The data represents the number of 11.111 µs periods (90 KHz) between full fan revolutions. To calculate this value to RPM:

```
(speed in RPM) = 60*90000/(tachometer data)
```

The HM support monitoring of fans that produce either two tachometer pulses per full revolution or one pulse per fan revolution. Configuration is via the TPPRn bit in the Tachometer Monitoring Control register; see Section 8.5.61 on page 180.

The speed measurement can be made in either of two modes:

- Independent of any FANPWM output. The measurement is performed during either one or two tachometer cycles (a tachometer cycle is the period between two consecutive pulses generated by the Fan), according to TPPRn bit in Tachometer Monitoring Control register. The measurement time cannot exceed 1 sec. This mode gives an accurate measurement if the FANPWMn signal does not affect the FANTACHn signal.
- When an associated FANPWM output is at “On” level. The “On” level of the FANPWM signal can be extended to 1/2, one or two tachometer cycles, according to TPPRn bit in Tachometer Monitoring Control register. The “On” level extension cannot exceed 51.2 ms. This mode gives an accurate measurement even if the FANPWMn signal interferes with the FANTACHn signal; however, as the fan accelerates during the “On” level extension, it generates more noise than mode 1.

The mode is configured by the FANn_MODE field in the Tach Mode register (see Section 8.5.60 on page 180). The ASSOCn field in the Tach PWM Association register (see Section 8.5.62 on page 181) associates tachometer measurement with a FANPWM output. To prevent false Fans Force-On generation, if a Tachometer measurement is not associated with any FANPWM, set the corresponding field in the Tach PWM Association register to 11b.

The tachometer data is compared with a configurable low limit contained in the Fan Tachometer Low Limit registers (two registers for each tachometer input). The data format in the limit registers is the same as in the tachometer data registers. In addition, the tachometer data and the number of tachometer cycles (the number of edges of the FANTACHn signal) detected during the measurement time are used to identify a fan stalled condition (see Table 52).

8.0 Health Management (HM) (Continued)

Table 52. Minimum Equivalent Fan Speed for Fan Failure Conditions

Measurement Mode	TPPR	Low Speed Condition		Fan Stalled Condition	
		Speed	FAN_MIN_MSB/LSB Setting	Speed	Condition (TACH_HIGH/LOW = FFFFh, or less than 'n' edges)
Mode 1	1 PPR	100 RPM	D2F0h	100 RPM	3 edges
	2 PPR				5 edges
Mode 2	1 PPR	1300 RPM	1039h	1300 RPM	2 edges
	2 PPR	650 RPM	2073h	650 RPM	

The FSTLMD bit in the associated Extended FANPWM Control register (see Section 8.5.85 on page 190) selects one of the following two options as the fan condition that enables the detection of a fan failure:

- Either a fan stalled condition or a low speed condition. (This option is recommended for Manual and Constantly On fan control; see "Control Modes" in Section 8.2.8.)
- A fan stalled condition only. (This is recommended for Automatic fan control if SPIN_END bit in associated Extended FANPWM Control register is set to 0; in this case, the setting of the Fan Tachometer Low Limit register indicates the fan speed at which the spin-up is ended, and not the low limit for the fan speed; see Section 8.5.85 on page 190.)

Whenever a fan failure is detected, the FANn_STALL status bit in the Status Register 2 (see Section 8.5.24 on page 165) and the FANn_STS bit in the HM Sensor Status Register 2 (see Section 8.4.9 on page 148) are both set to 1. A state is associated with the fan condition: a "Good" state is when neither condition for fan failure occurs; a "Fail" state is when at least one condition for fan failure occurs. Whenever the fan state changes, the FANn_EV bit in the HM Interrupt Status Register 2 is set (see Section 8.4.5 on page 144). FANn_EV can be enabled to create an IRQ by the associated FANn_EN bit in the HM Interrupt Enable Register 2 (see Section 8.4.7 on page 146). FANn_EV can also be enabled to create an SMI or SCI interrupt by the associated xxx_EN bit in the HM SMI/SCI Enable Register 2 (see Section 8.4.13 on page 150).

All status bits and event flags are cleared and fan speed monitoring is disabled while the V_{DD3} power supply is off.

8.2.8 Fan Speed Control

The HM controls fan speeds by creating three FANPWMn outputs. Each output is a Pulse Width Modulation signal that can be used to drive at least one fan. Fan speed control is active only while the V_{DD3} power supply is on.

Start-Up

After V_{DD} Power-Up reset, the FANPWM outputs are kept at 0% duty cycle until one of the following occurs:

- Two seconds elapse from the time that V_{DD3} exists. In this case, the fans are set to the value contained in the associated FANPWMn MAX Duty registers (see Section 8.5.82 on page 189 to Section 8.5.84).
- START bit of the Configuration registers is set (see Section 8.5.22 on page 163). In this case, the FANPWM outputs are controlled according to the FANPWMn Control Configuration registers (see Section 8.5.76 on page 187 to Section 8.5.78).

Control Modes

Fan speed can be controlled using one of four modes, chosen by the MODE field in the FANPWMn Control Configuration registers (see Section 8.5.76 on page 187 to Section 8.5.78):

- Disabled - The fan is stopped.
- Constantly On - The Fan duty cycle is set to the value contained in the associated FANPWMn MAX Duty register.
- Manual - The Fan speed is set by writing the required duty cycle to the FANPWM 'n' Current Duty register; see Section 8.5.17 on page 161 to Section 8.5.19. In the other three modes, these registers are RO and reflect the duty cycle created by the HM. During spin-up, these registers return either 0 or the target duty cycle (according to the SPIN_DUTY bit in the Extended FANPWM Control 1 register).
- Automatic - The FANPWM output is controlled by temperature data of one or more temperature zones (the MODE field also selects the temperature zones for each FANPWM output). In Automatic mode:
  - The HM implements a linear transfer function between the temperature data of the associated zones and the duty cycle of the FANPWM output. The translation between temperature and duty cycle is done in two stages. In the first stage the temperature is translated to unsigned normalized temperature (see Figure 31 on page 135). In the second stage the normalized temperature is translated to a duty cycle value (see Figure 32 on page 135). The use of the normalized temperature is essential if more than one temperature zone supplies temperature information for controlling the fans.

8.0 Health Management (HM) (Continued)

— The generated duty cycle is at its minimum at the low limit of the temperature, defined by the Zone 'n' Temperature Limit (see Section 8.5.63 on page 181 to Section 8.5.65). At, and below, this point the duty cycle is either 0% or another minimum value (the value contained in the FANPWMn Minimum register; see Section 8.5.79 on page 189 to Section 8.5.81). The decision to create a 0% duty-cycle or a minimum duty cycle other than 0% is made according to the MIN_ENn bit in the Min/Off, Spike Smoothing 1 register (see Section 8.5.74 on page 186). Below this point, a configurable hysteresis is applied by the HYSTn field in the Zone1-Zone2, Zone3 Hysteresis registers; see Section 8.5.69 on page 183 to Section 8.5.70.

— If the temperature rises above the low limit, and the FANPWM is at 0% duty cycle, a spin-up process takes place. During spin-up the FANPWM output duty cycle is set to the value contained in the FANPWMn MAX Duty register (see Section 8.5.82 on page 189 to Section 8.5.84). For more information on the spin-up process see "Speed Change Modes" on page 136.

— Between the low-limit and a temperature value of low-limit + range (range is configured by the RANGE field in the Zone 'n' Auto Speed Range and FANPWM 'n' Frequency registers; see Section 8.5.71 on page 183 to Section 8.5.73) the duty-cycle is changed linearly between a value of 0% and the value contained in the FANPWMn MAX Duty register (MAX_PWM field).

The sampled temperature data from each temperature zone is low-pass filtered to prevent temperature spikes from affecting the FANPWM output duty cycle and thus to prevent spurious speed changes of the fans (which cause unpleasant noise). The rise time of the filter (0% to 95% of the incoming temperature change) is defined by the FILTn_EN bit and TEMP_FILTn field in Min/Off, Spike Smoothing 1-2 registers (see Section 8.5.74 on page 186).

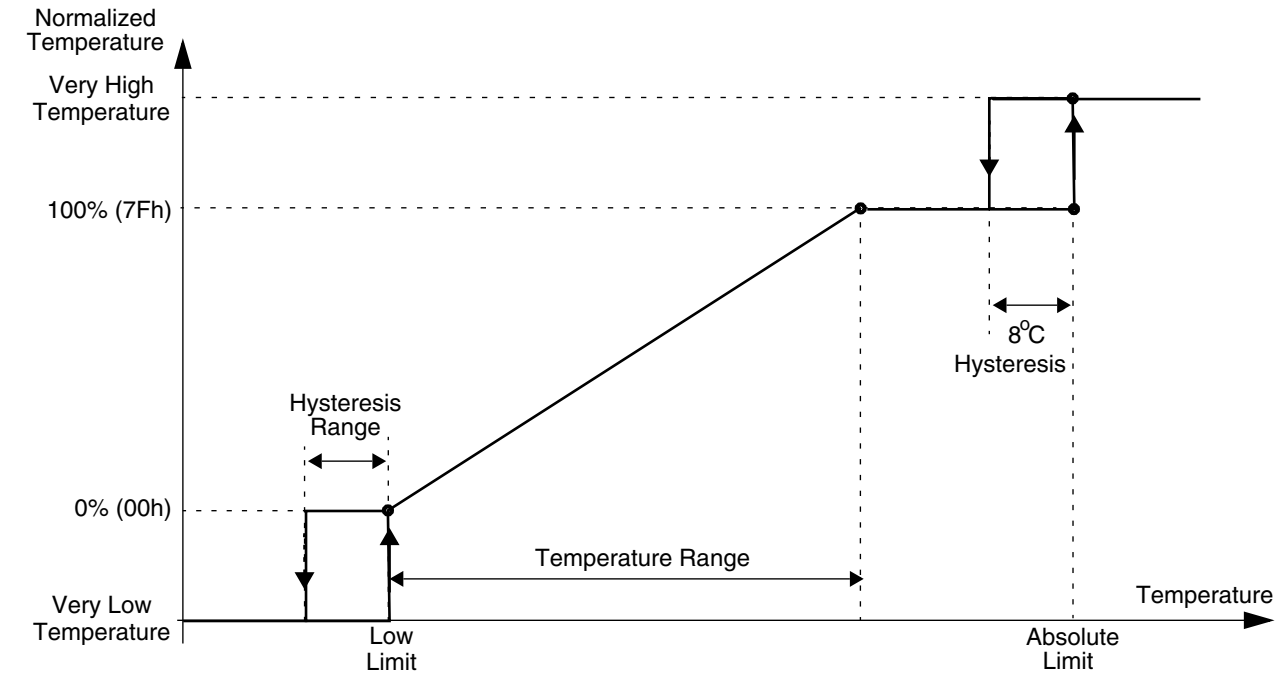


Figure 31. Temperature Normalization

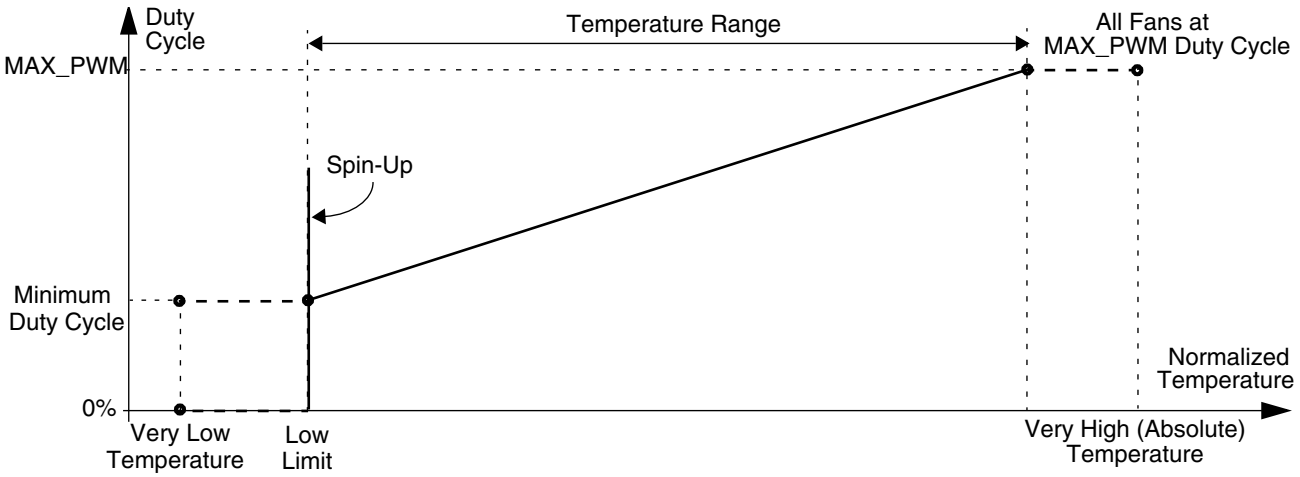


Figure 32. Automatic Fan Control Algorithm

8.0 Health Management (HM) (Continued)

Fan Force-On Conditions

In addition to setting the Constantly On fan mode option via the MODE field in the FANPWMn Control Configuration registers, the duty cycle of each FANPWM output is forced to the value contained in the associated FANPWMn MAX Duty register in one of the following conditions:

- If the value in one of the temperature zones is above the value in its associated Zone 'n' Absolute Temperature Limit.
- If the FANPWM output is in automatic mode, and a communication error with the device containing the associated temperature zone sensor is detected.
- If the FANPWM output is in automatic mode and one of the following occurs:
  - The fan is associated with Temperature Zone1, and a Remote Diode Fault is detected.
  - The fan is associated with Temperature Zone3, an LM96010 or LM96012 device is used, and a Remote Diode Fault is detected.
  - The Temperature Reading Zone 'n' register of its associated Temperature Zone, holds a value of 80h (temperature measurement error).
- If a fan failure is detected, and the fan was neither stopped by configuration (i.e., disabled) nor is spinning-up.

Note: For fans that are not connected or that do not have a tachometer output, make sure the related FANTACHn input is not associated with any FANPWMn output by setting the respective ASSOCn field in the Tach PWM Association register to '11'.

Speed Change Modes

For each FANPWMn output, in all four modes, the speed changes in one of two ways, as configured by the SPD_CHGn bit in the Extended FANPWM Control Register 2 (see Section 8.5.86 on page 191):

- Hard speed-change: The FANPWM duty cycle is updated in one immediate step.
- Soft speed-change: The FANPWM duty cycle is changed in steps of 3.125% duty-cycle until the new duty-cycle is reached. Changes between 0% and the minimum duty cycle (as defined in the FANPWMn Minimum registers) is done in one immediate step (when the fan is stopping or spinning-up). The step duration is determined by the STEP_LEN field in the Extended Control Configuration register. Figures 33 and 34 show a soft speed-change example.

There are two ways to end the spin-up process (configured by the SPIN_END bit in the Extended FANPWM Control Configuration register:

- Time: The spin-up process is ended after the time period defined in the SPIN field in the FANPWMn Control Configuration Register
- Speed or time: The spin-up process is ended after the time period defined in the SPIN field in the FANPWMn Control Configuration Register or after the fan speed value (in the Fan Tachometer Reading 'n' LSB and MSB registers) is either equal to or higher than the value in Fan Tachometer 'n' Low Limit LSB and MSB registers, whichever occurs first. Note that the FSTLMD bit in the associated Extended FANPWM Control register (see Section 8.5.85 on page 190) must be set to 1.

When the spin-up process ends, the FANPWM duty cycle is set to one of the following values:

- The value set in FANPWMn Current Duty register, in Manual Fan Control mode
- The value generated from the current normalized temperature by the automatic algorithm, in Automatic Fan Control mode (this value is updated in the FANPWMn Current Duty register)
- The value set in FANPWMn MAX Duty register, in Continuously On mode

When a speed-change follows the spin-up, the speed-change mode depends on the relation between the duty-cycle at the end of the spin-up ("spin-end DC") and the current duty-cycle that was generated by the automatic algorithm (PWM_DUTY field):

- If PWM_DUTY > spin-end DC, either a hard or a soft speed-change (according to the setting of SPD_CHNGn bit in Extended FANPWM Control Register 2) is performed between the values of spin-end DC and PWM_DUTY.
- If PWM_DUTY < spin-end DC, a hard speed-change (one step) is performed between the values of spin-end DC and PWM_DUTY.

8.0 Health Management (HM) (Continued)

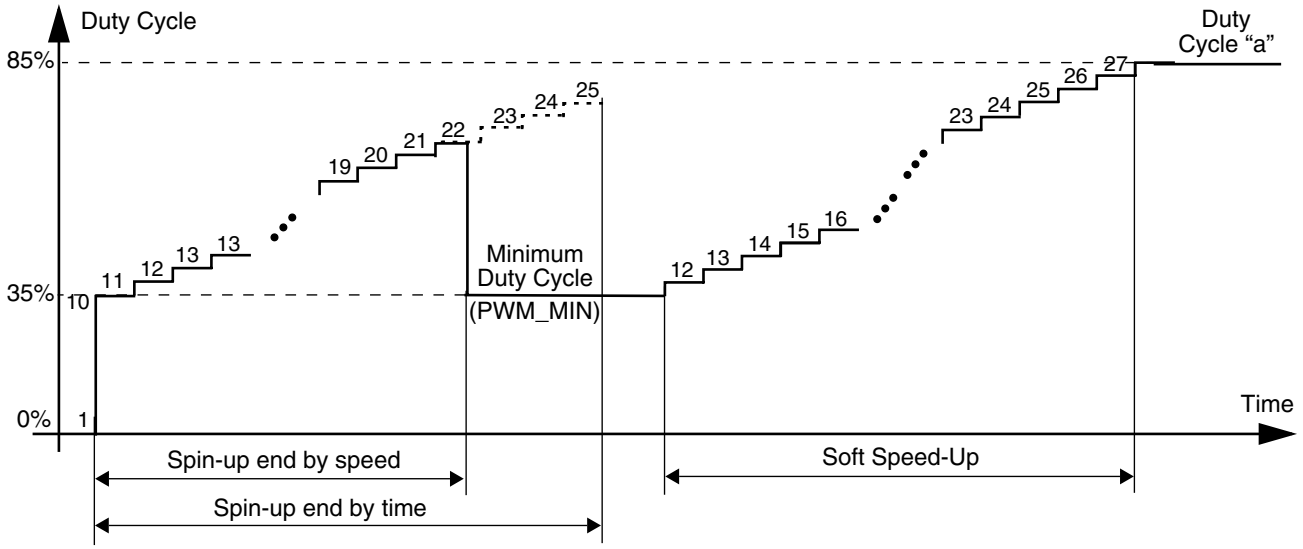


Figure 33. Soft Spin-Up and Soft Speed-Up Example

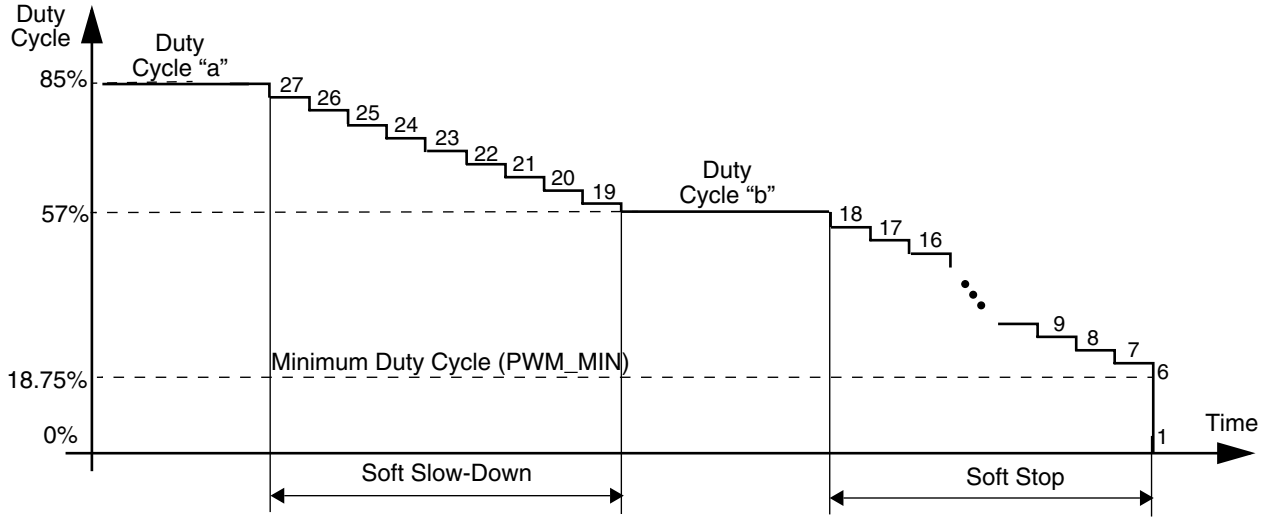


Figure 34. Soft Slow-Down and Soft Stop Example

Other Features

The FANPWM frequency is configured by the FREQ field in the Zone 'n' Auto Speed Range and FANPWMn Frequency registers.

The FANPWM signal polarity (whether 0% duty-cycle represents a low-level or a high-level signal) is configured by INV bit in the FANPWMn Control Configuration registers (see Section 8.5.76 on page 187). INV bit is write-only; its value is reflected in the respective FANOUTn_INV bit in the HMCFG1 register (see Section 3.15.3 on page 79), which is read-only. FANOUTn_INV bit is powered by V_{BAT}, thus preserving the polarity of the FANPWM signal during power failures (i.e., when V_{SB3} power is off).

8.0 Health Management (HM) (Continued)

8.2.9 Event Notification

Event Notification for SMBus Access

The Status Registers 1-3 (see Section 8.5.23 on page 164) contain status bits for the following events:

- Device 1 (LM96011 or LM96010 or LM96012) communication error (DEV1_Fault)
- Device 2 (LM95010) communication error (DEV2_Fault)
- Device 1 (LM96011 or LM96010 or LM96012) Remote Diode fault (RD_Fault)
- Fan failure for the four tachometer inputs (FAN4_STALL-FAN1_STALL)
- Temperature above the critical limit for the three temperature zones (CRIT3_ERR-CRIT1_ERR)
- Temperature outside the low or high limit for the three temperature zones (ZONE3_ERR-ZONE1_ERR)
- Voltage outside the low or high limit for the five voltage channels (5V_ERR, 3.3V_ERR, Vccp_ERR, 2.5V_ERR, 12V_ERR)

When a status bit is set, updated it is disabled, thus preserving its value until the corresponding status register is read via the SMBus. Reading the register re-enables status bit updating with the current event state.

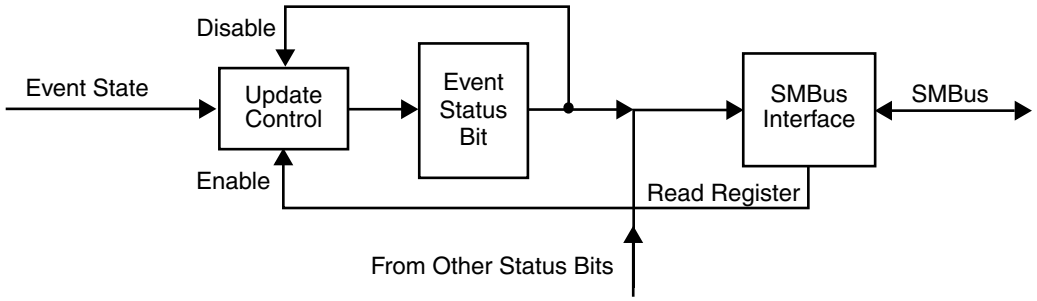


Figure 35. Event Notification for SMBus

Event Notification for LPC Access

The HM Interrupt Status Registers 1-3 (see Section 8.4.4 on page 143) contains event status bits for the following events:

- Device 1 (LM96011 or LM96010 or LM96012) communication changes state between working and not-working (DEV1_EV).
- Device 2 (LM95010) communication changes state between working and not-working (DEV2_EV).
- Device 1 (LM96011 or LM96010 or LM96012) Remote Diode fault changes state between no-fault and fault (RD_EV).
- Tachometer inputs change state between fans running and failed (FAN4_EV-FAN1_EV).
- Temperature zones change state between below and above the critical limit (CRIT3_EV-CRIT1_EV).
- Temperature zones change state between working within limits and exceeding limits (ZONE3_EV-ZONE1_EV).
- Voltage channels change state between working within limits and exceeding limits (5V_EV, 3.3V_EV, Vccp_EV, 2.5V_EVR, 12V_EV).

Note that whenever a state changes these LPC event status bits are set.

These bits can generate an IRQ to the host if the corresponding enable bits are set in the HM Interrupt Enable Registers 1-3 (see Section 8.4.6 on page 145). The HM Interrupt Enable Registers 1-3 are reset by a V_{DD} Power-Up reset, a Hardware reset or a Software reset.

The actual state of each event is held by the corresponding bits in the HM Sensor Status Registers 1-3 (see Section 8.4.8 on page 147).

SCI and SMI Event Routing

All the event status bits in the HMINT_STS1-3 registers (see Section 8.4.4 on page 143) can be divided into two different groups, based on the severity that each status represents:

- Limit Events: 2.5V_EV, Vccp_EV, 3.3V_EV, 5V_EV, ZONE1_EV, ZONE2_EV and ZONE3_EV of HMINT_STS1 register, 12V_EV of HMINT_STS2 register.
- Critical Events: FAN1-4_EV, RD_EV, DEV1_EV, DEV2_EV of HMINT_STS2 register, CRIT1-3_EV of HMINT_STS3 register.

Each of these groups can be routed independently, via the control bits of the Events to SMI/SCI Routing register (see Section 8.4.16 on page 152), to generate an SCI ($\overline{\text{SIOPME}}$) interrupt or an SMI interrupt. The enable bits in the HM SMI/SCI Enable Register 1-3 (see Section 8.4.13 on page 150) enable SMI/SCI generation based on the value of the corresponding event status bit. The SMI and SCI are generated via the SWC module.

8.0 Health Management (HM) (Continued)

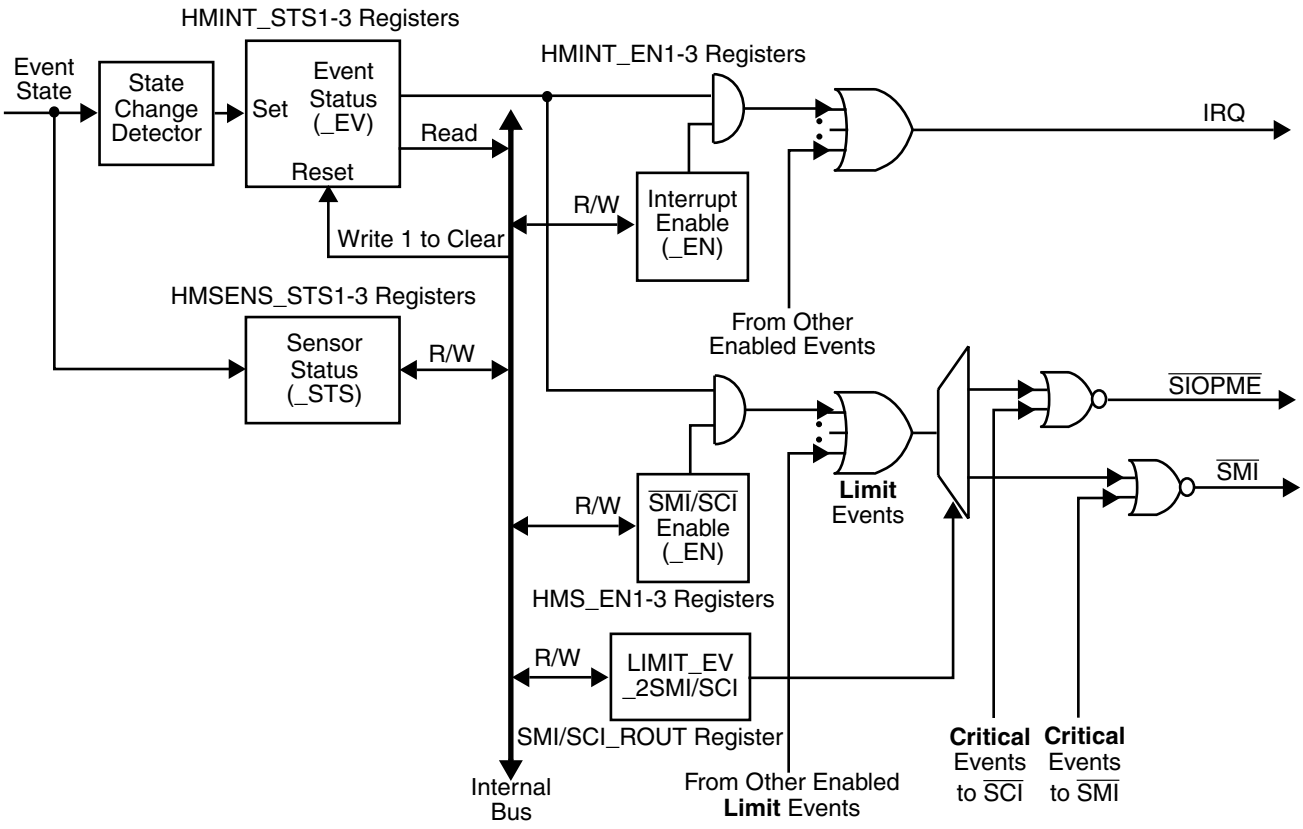


Figure 36. Event Notification for LPC

8.2.10 Enhanced Thermal Control (ETC)

The Enhanced Thermal Control function generates an internal ETC signal for the Glue module. The assertion edge of this signal turns off the Main power supply (V_{DD3}) via the $\overline{PS\_ON}$ pin.

The ETC function is controlled by the following events:

- The temperature data value in Temperature Zone1 is higher than the critical limit set in the Temperature Critical Limit Zone1 register.
- A communication error with Device 1 (LM96011 or LM96010 or LM96012) occurs.
- A major SensorPath Bus failure is detected.

An asserted ETC signal turns off the Main power supply. The resulting ETC signal is deasserted when the V_{DD3} power is off and remains deasserted until both of the following conditions are met:

- The delay time (182 ms) for enabling V_{DD} channels (see Section 8.5.55 on page 177) after the V_{DD3} power is turned on has elapsed.
- The temperature data in Temperature Zone1 was updated with a new value by the LMxx Sensor device

If the temperature data from Device 1 (LM96011 or LM96010 or LM96012) is not updated for 728 ms after V_{DD3} power is on (see "Time-Out Function" on page 133), the HM assumes a communication error with the LMxx Sensor device occurred and asserts ETC.

The ETC is enabled by the ETC_EN bit in the Enhanced Thermal Control Register (see Section 8.5.59 on page 179).

8.2.11 General Configuration

The Configuration register (see Section 8.5.22 on page 163) contains control bits for several general configuration options:

- Disable SMBus write access to the HM registers (SMBR bit).
- Override fan control setting and set all FANPWM outputs to the value contained in the associated FANPWMn MAX Duty registers (OVRID bit).
- Lock some of the configuration registers (LOCK bit).
- Start command for the monitoring functions and FANPWM control functions (START).

8.0 Health Management (HM) (Continued)

When the START bit in Configuration register is 0, sensor monitoring is disabled. However, following V_{SB3} power-up, and after the READY bit becomes 1, Temperature Zone1 is monitored regardless of the state of the START bit. If the temperature data of Temperature Zone1 is above the default value of the Temperature Critical Limit Zone1 register (+110°C), ETC is asserted turning the Main power supply off. In addition, the CRIT1_ERR bit in Status Register 3 is set to 1. This feature protects the CPU from overheating at V_{SB3} power-up before the HM is configured by the software for the first time.

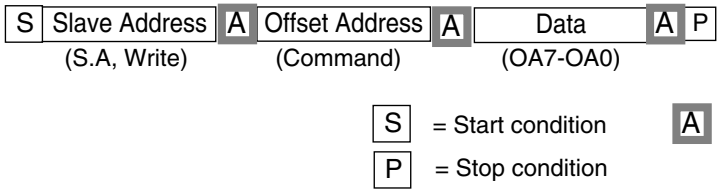
The LOCK_LIM bit in the Monitoring Control Register (see Section 8.5.54 on page 176) can lock the Limit registers.

8.3 HM SMBUS ACCESS

This section describes the SMBus transactions protocol used by the HM (see also Section 8.2.1 on page 127).

8.3.1 Write Transaction

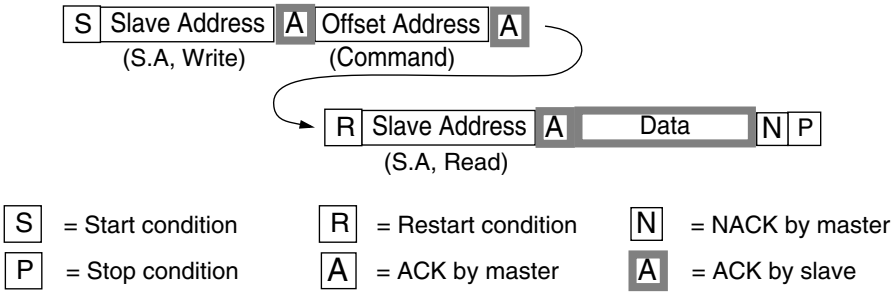
This transaction writes a byte of data to an HM register. The specific register is accessed using an 8-bit offset address.



8.3.2 Read Transaction

This transaction reads a byte of data from an HM register. The specific register is accessed using an 8-bit offset address. This transaction is executed in two stages:

1. The master executes an SMBus write transaction, which conveys the Offset Address information to the HM. During this stage, the data is read from the specific register into a read buffer. This stage has no Stop condition.
2. Following a Restart condition, the master executes an SMBus read transaction. During this stage the data is transferred from the read buffer to the master.



8.0 Health Management (HM) (Continued)

8.4 HM LPC ACCESS REGISTERS

The HM LPC Access Registers, described in this section, can be accessed by the host through the LPC Bus. The offsets of these registers are related to the base address determined by the Base Address registers at Index 60-61h in the HM device configuration (see Section 3.15 on page 79).

The following abbreviations are used to indicate the register type:

- R/W = Read/Write.
- RO = Read-Only.
- WO = Write-Only. Reading from the bit returns 0.
- R/W1C =Read/Write 1 to Clear. Writing 1 to a bit clears it. Writing 0 has no effect.

Table 53. HM LPC Access Registers

Offset	Mnemonic	Name	Type	Power Well	Section
00h	HMADDR	HM Address Register	R/W	V_{DD3}	8.4.1
01h	HMDATA	HM Data Register	R/W	V_{DD3}	8.4.2
02h	HMSTS	HM Status and Command Register	Varies per bit	V_{DD3}	8.4.3
03h	HMINT_STS1	HM Interrupt Status Register 1	R/W1C	V_{SB3}	8.4.4
04h	HMINT_STS2	HM Interrupt Status Register 2	R/W1C	V_{SB3}	8.4.5
05h	HMINT_EN1	HM Interrupt Enable Register 1	R/W	V_{DD3}	8.4.6
06h	HMINT_EN2	HM Interrupt Enable Register 2	R/W	V_{DD3}	8.4.7
07h	HMSENS_STS1	HM Sensor Status Register 1	RO	V_{SB3}	8.4.8
08h	HMSENS_STS2	HM Sensor Status Register 2	RO	V_{SB3}	8.4.9
09h	HMINT_STS3	HM Interrupt Status Register 3	R/W1C	V_{SB3}	8.4.10
0Ah	HMINT_EN3	HM Interrupt Enable Register 3	R/W	V_{DD3}	8.4.11
0Bh	HMSENS_STS3	HM Sensor Status Register 3	RO	V_{SB3}	8.4.12
0Ch	HMS_EN1	HM SMI/SCI Enable Register 1	R/W	V_{SB3}	8.4.13
0Dh	HMS_EN2	HM SMI/SCI Enable Register 2	R/W	V_{SB3}	8.4.14
0Eh	HMS_EN3	HM SMI/SCI Enable Register 3	R/W	V_{SB3}	8.4.15
0Fh	SMI/SCI_ROUT	Alarms to SMI/SCI Routing Register	R/W	V_{SB3}	8.4.16

Read/Write Operations

The HM registers are used for write and read accesses as follows:

- Write operation:
  1. Poll HMSTS.BUSY bit until it is 0.
  2. Write the address (index) of the target HM register to HMADDR register.
  3. Write the data value to HMDATA register. In response HMSTS.BUSY is set.
  4. The transaction is completed when HMSTS.BUSY returns to 0.
- Read operation:
  1. Poll HMSTS.BUSY bit until it is 0.
  2. Write the address (index) of the target HM register to HADDR register.
  3. Set HMSTS.STRT_RD to initiate read transaction. In response HMSTS.BUSY is set.
  4. Poll HMSTS.BUSY bit until it is 0.
  5. Read HMDATA register.

8.0 Health Management (HM) (Continued)

8.4.1 HM Address Register (HMADDR)

Power Well: V_{DD3}
Location: Offset 00h
Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**ADDR**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**ADDR.** Address of the HM register to be accessed (valid addresses appear in the address column in Table 54 on page 153). An exception are the Status Register 1-3 (addresses 41h, 42h and 73h respectively), which are disabled for access by LPC bus (reserved). Read access to reserved or undefined registers (not a valid address) returns 0. Write access to reserved or undefined registers is ignored. ADDR field can be updated only when the BUSY bit in HMSTS register (see Section 8.4.3 on page 142) is 0; otherwise, the transaction will have unpredictable results

8.4.2 HM Data Register (HMDATA)

Power Well: V_{DD3}
Location: Offset 01h
Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**DATA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**DATA.** Data to be read or written from/to the accessed HM register, whose address is ADDR in HMADDR register. Writing to this register automatically triggers the access to the HM register. Writing the DATA field while the BUSY bit in HMSTS register is 1 is ignored; reading the DATA field while the BUSY bit is 1 returns unpredictable data.

8.4.3 HM Status and Command Register (HMSTS)

Power Well: V_{DD3}
Location: Offset 02h
Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**						**START_RD**	**BUSY**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7-2		**Reserved.**
1	WO	**START_RD.** Writing 1 to this bit initiates a read access from the HM register with address HMADDR.ADDR. Writing 1 to START_RD is allowed only when BUSY bit is 0; otherwise, the write can have unpredictable results.
0	RO	**BUSY.** HM Interface busy. 0: HMDATA register contains valid read data or HM is ready for write access 1: HM is busy

8.0 Health Management (HM) (Continued)

8.4.4 HM Interrupt Status Register 1 (HMINT_STS1)

Event status register 1.

Power Well: V_{SB3}

Location: Offset 03h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**ZONE3_EV**	**ZONE2_EV**	**ZONE1_EV**	**5V_EV**	**3.3V_EV**	**Vccp_EV**	**2.5V_EV**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved.**
6	**ZONE3_EV.** Is set to 1 when a Temperature Zone3 monitoring event occurs. 0: No state change from the last time this bit was cleared (default) 1: Temperature changed state from the last time this bit was cleared
5	**ZONE2_EV.** Is set to 1 when a Temperature Zone2 monitoring event occurs. 0: No state change from the last time this bit was cleared (default) 1: Temperature changed state from the last time this bit was cleared
4	**ZONE1_EV.** Is set to 1 when a Temperature Zone1 monitoring event occurs. 0: No state change from the last time this bit was cleared (default) 1: Temperature changed state from the last time this bit was cleared
3	**5V_EV.** Is set to 1 when a 5V input voltage monitoring event occurs. 0: No state change from the last time this bit was cleared (default) 1: Voltage changed state from the last time this bit was cleared
2	**3.3V_EV.** Is set to 1 when a 3.3V input voltage monitoring event occurs. 0: No state change from the last time this bit was cleared (default) 1: Voltage changed state from the last time this bit was cleared
1	**Vccp_EV.** Is set to 1 when a Vccp input voltage monitoring event occurs. 0: No state change from the last time this bit was cleared (default) 1: Voltage changed state from the last time this bit was cleared
0	**2.5V_EV.** Is set to 1 when a 2.5V input voltage monitoring event occurs. 0: No state change from the last time this bit was cleared (default) 1: Voltage changed state from the last time this bit was cleared

8.0 Health Management (HM) (Continued)

8.4.5 HM Interrupt Status Register 2 (HMINT_STS2)

Event status register 2.

Power Well: V_{SB3}

Location: Offset 04h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**DEV2_EV**	**RD_EV**	**FAN4_EV**	**FAN3_EV**	**FAN2_EV**	**FAN1_EV**	**DEV1_EV**	**12V_EV**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**DEV2_EV (Device 2 Event).** Is set to 1 when a communication event with the optional LM95010 device occurs. 0: No communication event occurred since the last time this bit was cleared (default) 1: Communication event occurred
6	**RD_EV (Remote Diode Event).** Is set to 1 when a physical connection event on one of the Remote Diodes of the Temperature Zones occurs (For LM96011: Zone1; for LM96010 or LM96012: Zone1 or Zone3). 0: No Remote Diode event occurred since the last time this bit was cleared (default) 1: Remote Diode physical connection event occurred
5	**FAN4_EV.** Is set to 1 when a Fan Tachometer Reading 4 monitoring event occurs. 0: No fan state change from the last time this bit was cleared (default) 1: Fan changed state from the last time this bit was cleared
4	**FAN3_EV.** Is set to 1 when a Fan Tachometer Reading 3 monitoring event occurs. 0: No fan state change from the last time this bit was cleared (default) 1: Fan changed state from the last time this bit was cleared
3	**FAN2_EV.** Is set to 1 when a Fan Tachometer Reading 2 monitoring event occurs. 0: No fan state change from the last time this bit was cleared (default) 1: Fan changed state from the last time this bit was cleared
2	**FAN1_EV.** Is set to 1 when a Fan Tachometer Reading 1 monitoring event occurs. 0: No fan state change from the last time this bit was cleared (default) 1: Fan changed state from the last time this bit was cleared
1	**DEV1_EV (Device 1 Event).** Is set to 1 when a communication event with the LM96011, LM96010 or LM96012 occurs. 0: No communication event occurred since the last time this bit was cleared (default) 1: Communication event occurred
0	**12V_EV.** Is set to 1 when a 12V input voltage monitoring event occurs. 0: No state change from the last time this bit was cleared (default) 1: Voltage changed state from the last time this bit was cleared

8.0 Health Management (HM) (Continued)

8.4.6 HM Interrupt Enable Register 1 (HMINT_EN1)

Interrupt enable register 1.

Power Well: V_{DD3}

Location: Offset 05h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**ZONE3_EN**	**ZONE2_EN**	**ZONE1_EN**	**5V_EN**	**3.3V_EN**	**Vccp_EN**	**2.5V_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved.**
6	**ZONE3_EN.** When set to 1, enables IRQ generation on setting of ZONE3_EV of HMINT_STS1 register. 0 Disable IRQ (default) 1: Enable IRQ
5	**ZONE2_EN.** When set to 1, enables IRQ generation on setting of ZONE2_EV of HMINT_STS1 register. 0: Disable IRQ (default) 1: Enable IRQ
4	**ZONE1_EN.** When set to 1, enables IRQ generation on setting of ZONE1_EV of HMINT_STS1 register. 0: Disable IRQ (default) 1: Enable IRQ
3	**5V_EN.** When set to 1, enables IRQ generation on setting of 5V_EV of HMINT_STS1 register. 0: Disable IRQ (default) 1: Enable IRQ
2	**3.3V_EN.** When set to 1, enables IRQ generation on setting of 3.3V_EV of HMINT_STS1 register. 0: Disable IRQ (default) 1: Enable IRQ
1	**Vccp_EN.** When set to 1, enables IRQ generation on setting of Vccp_EV of HMINT_STS1 register. 0: Disable IRQ (default) 1: Enable IRQ
0	**2.5V_EN.** When set to 1, enables IRQ generation on setting of 2.5V_EV of HMINT_STS1 register. 0: Disable IRQ (default) 1: Enable IRQ

8.0 Health Management (HM) (Continued)

8.4.7 HM Interrupt Enable Register 2 (HMINT_EN2)

Interrupt enable register 2.

Power Well: V_{DD3}

Location: Offset 06h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**DEV2_EN**	**RD_EN**	**FAN4_EN**	**FAN3_EN**	**FAN2_EN**	**FAN1_En**	**DEV1_EN**	**12V_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**DEV2_EN.** When set to 1, enables IRQ generation on setting of DEV2_EV of HMINT_STS2 register. 0: Disable IRQ (default) 1: Enable IRQ
6	**RD_EN.** When set to 1, enables IRQ generation on setting of RD_EV of HMINT_STS2 register. 0: Disable IRQ (default) 1: Enable IRQ
5	**FAN4_EN.** When set to 1, enables IRQ generation on setting of FAN4_EV of HMINT_STS2 register. 0: Disable IRQ (default) 1: Enable IRQ
4	**FAN3_EN.** When set to 1, enables IRQ generation on setting of FAN3_EV of HMINT_STS2 register. 0: Disable IRQ (default) 1: Enable IRQ
3	**FAN2_EN.** When set to 1, enables IRQ generation on setting of FAN2_EV of HMINT_STS2 register. 0: Disable IRQ (default) 1: Enable IRQ
2	**FAN1_EN.** When set to 1, enables IRQ generation on setting of FAN1_EV of HMINT_STS2 register. 0: Disable IRQ (default) 1: Enable IRQ
1	**DEV1_EN.** When set to 1, enables IRQ generation on setting of DEV1_EV of HMINT_STS2 register. 0: Disable IRQ (default) 1: Enable IRQ
0	**12V_EN.** When set to 1, enables IRQ generation on setting of 12V_EV of HMINT_STS2 register. 0: Disable IRQ (default) 1: Enable IRQ

8.0 Health Management (HM) (Continued)

8.4.8 HM Sensor Status Register 1 (HMSENS_STS1)

Sensor status register 1.

Note: All status bits in this register are reset when START bit of the Configuration register is reset.

Power Well: V_{SB3}

Location: Offset 07h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**ZONE3_STS**	**ZONE2_STS**	**ZONE1_STS**	**5V_STS**	**3.3V_STS**	**Vccp_STS**	**2.5V_STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved.**
6	**ZONE3_STS.** Is set to 1 when the temperature of Temperature Zone3 exceeds the limits. 0: Temperature does not exceed any respective limit (default) 1: Temperature exceeds a respective limit
5	**ZONE2_STS.** Is set to 1 when the temperature of Temperature Zone2 exceeds the limits. 0: Temperature does not exceed any respective limit (default) 1: Temperature exceeds a respective limit
4	**ZONE1_STS.** Is set to 1 when the temperature of Temperature Zone1 exceeds the limits. 0: Temperature does not exceed any respective limit (default) 1: Temperature exceeds a respective limit
3	**5V_STS.** Is set to 1 when 5V input voltage exceeds the limits. 0: Voltage does not exceed any respective limit (default) 1: Voltage exceeds a respective limit
2	**3.3V_STS.** Is set to 1 when 3.3V input voltage exceeds the limits. 0: Voltage does not exceed any respective limit (default) 1: Voltage exceeds a respective limit
1	**Vccp_STS.** Is set to 1 when Vccp input voltage exceeds the limits. 0: Voltage does not exceed any respective limit (default) 1: Voltage exceeds a respective limit
0	**2.5V_STS.** Is set to 1 when 2.5V input voltage exceeds the limits. 0: Voltage does not exceed any respective limit (default) 1: Voltage exceeds a respective limit

8.0 Health Management (HM) (Continued)

8.4.9 HM Sensor Status Register 2 (HMSENS_STS2)

Sensor status register 2.

Note: All status bits in this register are reset when START bit of the Configuration register is reset.

Power Well: V_{SB3}

Location: Offset 08h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**DEV2_STS**	**RD_STS**	**FAN4_STS**	**FAN3_STS**	**FAN2_STS**	**FAN1_STS**	**DEV1_STS**	**12V_STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**DEV2_STS.** Is set to 1 when a communication problem with the optional LM95010 device exists. 0: The optional LM95010 device does not exist or exists with valid communication (default) 1: A communication problem with LM95010
6	**RD_STS.** Is set to 1 when there is a physical connection fault in one of the Remote Diodes of the Temperature Zones occur (for LM96011: Zone1; for LM96010 or LM96012: Zone1 or Zone3). 0: Proper connection of Remote Diode (default) 1: Remote Diode connection fault
5	**FAN4_STS.** Is set to 1 when Fan 4 is either stalled or running at low speed (according to the FSTLMD bit in the associated Extended FANPWM Control register; see Section 8.5.85 on page 190). 0: Fan operating normally (default) 1: Fan is either stalled or running at low speed
4	**FAN3_STS.** Is set to 1 when Fan 3 is either stalled or running at low speed (according to the FSTLMD bit in the associated Extended FANPWM Control register). 0: Fan operating normally (default) 1: Fan is either stalled or running at low speed
3	**FAN2_STS.** Is set to 1 when Fan 2 is either stalled or running at low speed (according to the FSTLMD bit in the associated Extended FANPWM Control register). 0: Fan operating normally (default) 1: Fan is either stalled or running at low speed
2	**FAN1_STS.** Is set to 1 when Fan 1 is either stalled or running at low speed (according to the FSTLMD bit in the associated Extended FANPWM Control register). 0: Fan operating normally (default) 1: Fan is either stalled or running at low speed
1	**DEV1_STS.** Is set to 1 when a communication problem with the LM96011, LM96010 or LM96012 device exists. 0: Communication with LM96011, LM96010 or LM96012 is functional (default) 1: Communication problem with LM96011, LM96010 or LM96012
0	**12V_STS.** Is set to 1 when 12V input voltage exceeds the limits. 0: Voltage not does not exceed any respective limit (default) 1: Voltage exceeds a respective limit

8.0 Health Management (HM) (Continued)

8.4.10 HM Interrupt Status Register 3 (HMINT_STS3)

Event status register 3.

Note: All status bits in this register are reset when START bit of the Configuration register is reset.

Power Well: V_{SB3}

Location: Offset 09h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**CRIT3_EV**	**CRIT2_EV**	**CRIT1_EV**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved.**
2	**CRIT3_EV.** Is set to 1 when a Temperature Zone3 critical monitoring event occurs. 0: No critical temperature state change from the last time this bit was cleared (default) 1: Critical temperature state changed from the last time this bit was cleared
1	**CRIT2_EV.** Is set to 1 when a Temperature Zone2 critical monitoring event occurs. 0: No critical temperature state change from the last time this bit was cleared (default) 1: Critical temperature state changed from the last time this bit was cleared
0	**CRIT1_EV.** Is set to 1 when a Temperature Zone1 critical monitoring event occurs. 0: No critical temperature state change from the last time this bit was cleared (default) 1: Critical temperature state changed from the last time this bit was cleared

8.4.11 HM Interrupt Enable Register 3(HMINT_EN3)

Interrupt enable register 3.

Power Well: V_{DD3}

Location: Offset 0Ah

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**CRIT3_EN**	**CRIT2_EN**	**CRIT1_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved.**
2	**CRIT3_EN.** When set to 1, enables IRQ generation on setting of CRIT3_EV of HMINT_STS3 register. 0: Disable IRQ (default) 1: Enable IRQ
1	**CRIT2_EN.** When set to 1, enables IRQ generation on setting of CRIT2_EV of HMINT_STS3 register. 0: Disable IRQ (default) 1: Enable IRQ
0	**CRIT1_EN.** When set to 1, enables IRQ generation on setting of CRIT1_EV of HMINT_STS3 register. 0: Disable IRQ (default) 1: Enable IRQ

8.0 Health Management (HM) (Continued)

8.4.12 HM Sensor Status Register 3 (HMSENS_STS3)

Sensor status register 1.

Power Well: V_{SB3}

Location: Offset 0Bh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**CRIT3_STS**	**CRIT2_STS**	**CRIT1_STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved.**
2	**CRIT3_STS.** Is set to 1 when Temperature Zone3 temperature exceeds the critical limit. 0: Temperature does not exceed critical limit (default) 1: Temperature exceeds critical limit
1	**CRIT2_STS.** Is set to 1 when Temperature Zone2 temperature exceeds the critical limit. 0: Temperature does not exceed critical limit (default) 1: Temperature exceeds critical limit
0	**CRIT1_STS.** Is set to 1 when Temperature Zone1 temperature exceeds the critical limit. 0: Temperature does not exceed critical limit (default) 1: Temperature exceeds critical limit

8.4.13 HM SMI/SCI Enable Register 1 (HMS_EN1)

SMI/SCI Interrupt enable register 1.

Power Well: V_{SB3}

Location: Offset 0Ch

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**ZONE3_EN**	**ZONE2_EN**	**ZONE1_EN**	**5V_EN**	**3.3V_EN**	**Vccp_EN**	**2.5V_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved.**
6	**ZONE3_EN.** When set to 1, enables SMI/SCI generation on setting of ZONE3_EV of HMINT_STS1 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
5	**ZONE2_EN.** When set to 1, enables SMI/SCI generation on setting of ZONE2_EV of HMINT_STS1 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
4	**ZONE1_EN.** When set to 1, enables SMI/SCI generation on setting of ZONE1_EV of HMINT_STS1 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
3	**5V_EN.** When set to 1, enables SMI/SCI generation on setting of 5V_EV of HMINT_STS1 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI

8.0 Health Management (HM) (Continued)

Bit	Description
2	**3.3V_EN.** When set to 1, enables SMI/SCI generation on setting of 3.3V_EV of HMINT_STS1 register. 0: Disable SMI/SCI (default) 1: Enable IRSMI/SCIQ
1	**Vccp_EN.** When set to 1, enables SMI/SCI generation on setting of Vccp_EV of HMINT_STS1 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
0	**2.5V_EN.** When set to 1, enables SMI/SCI generation on setting of 2.5V_EV of HMINT_STS1 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI

8.4.14 HM SMI/SCI Enable Register 2 (HMS_EN2)

SMI/SCI enable register 2.

Power Well: V_{SB3}

Location: Offset 0Dh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**DEV2_EN**	**RD_EN**	**FAN4_EN**	**FAN3_EN**	**FAN2_EN**	**FAN1_En**	**DEV1_EN**	**12V_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**DEV2_EN.** When set to 1, enables SMI/SCI generation on setting of DEV2_EV of HMINT_STS2 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
6	**RD_EN.** When set to 1, enables SMI/SCI generation on setting of RD_EV of HMINT_STS2 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
5	**FAN4_EN.** When set to 1, enables SMI/SCI generation on setting of FAN4_EV of HMINT_STS2 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
4	**FAN3_EN.** When set to 1, enables SMI/SCI generation on setting of FAN3_EV of HMINT_STS2 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
3	**FAN2_EN.** When set to 1, enables SMI/SCI generation on setting of FAN2_EV of HMINT_STS2 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
2	**FAN1_EN.** When set to 1, enables SMI/SCI generation on setting of FAN1_EV of HMINT_STS2 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
1	**DEV1_EN.** When set to 1, enables SMI/SCI generation on setting of DEV1_EV of HMINT_STS2 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
0	**12V_EN.** When set to 1, enables SMI/SCI generation on setting of 12V_EV of HMINT_STS2 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI

8.0 Health Management (HM) (Continued)

8.4.15 HM SMI/SCI Enable Register 3(HMS_EN3)

SMI/SCI enable register 1.

Power Well: V_{SB3}

Location: Offset 0Eh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**CRIT3_EN**	**CRIT2_EN**	**CRIT1_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved.**
2	**CRIT3_EN.** When set to 1, enables SMI/SCI generation on setting of CRIT3_EV of HMINT_STS3 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
1	**CRIT2_EN.** When set to 1, enables SMI/SCI generation on setting of CRIT2_EV of HMINT_STS3 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI
0	**CRIT1_EN.** When set to 1, enables SMI/SCI generation on setting of CRIT1_EV of HMINT_STS3 register. 0: Disable SMI/SCI (default) 1: Enable SMI/SCI

8.4.16 Events to SMI/SCI Routing Register (SMI/SCI_ROUT)

Power Well: V_{SB3}

Location: 0Fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**						**CRIT_EV_ 2SMI/SCI**	**LIMIT_EV_ 2SMI/SCI**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-2	**Reserved.**
1	**CRIT_EV_2SMI/SCI (Critical Events to SMI or SCI).** Enables critical events to generate an SMI or SCI interrupt for the following events when the respective bits in the HMS_EN1-3 registers are set: FAN1-4_EV, RD_EV, DEV1_EV, DEV2_EV of HMINT_STS2 register, CRIT1-3_EV of HMINT_STS3 register. 0: SMI is generated 1: SCI ($\overline{\text{SIOPME}}$) is generated
0	**LIMIT_EV_2SMI/SCI (Limit Events to SMI or SCI).** Enables limit events to generate an SMI or SCI interrupt for the following events when the respective bits in the HMS_EN1-3 registers are set: 2.5V_EV, Vccp_EV, 3.3V_EV, 5V_EV, ZONE1-3_EV of HMINT_STS1 register, 12V_EV of HMINT_STS2. 0: SMI is generated 1: SCI ($\overline{\text{SIOPME}}$) is generated

8.0 Health Management (HM) (Continued)

8.5 HEALTH MANAGEMENT REGISTERS

The HM registers implement health monitoring and control functionality.

Reads to reserved and undefined registers return 0. Writes to reserved and undefined registers are ignored.

Table 54 lists all HM registers. The description of each register is grouped according to register functionality. The Status Register 1-3 (address 41h, 42h and 73h respectively) are not accessible from LPC.

All these registers are V_{SB3} powered and thus are reset by V_{SB} Power-Up reset.

Table 54. Health Management Registers

Address	Register Name	Type	Section
20h	Voltage Reading 2.5V	RO	8.5.1
21h	Voltage Reading Vccp	RO	8.5.2
22h	Voltage Reading 3.3V	RO	8.5.3
23h	Voltage Reading 5V	RO	8.5.4
24h	Voltage Reading 12V	RO	8.5.5
25h	Temperature Reading Zone1	RO	8.5.6
26h	Temperature Reading Zone2	RO	8.5.7
27h	Temperature Reading Zone3	RO	8.5.8
28h	Fan Tachometer Reading 1 LSB	RO	8.5.9
29h	Fan Tachometer Reading 1 MSB	RO	8.5.10
2Ah	Fan Tachometer Reading 2 LSB	RO	8.5.11
2Bh	Fan Tachometer Reading 2 MSB	RO	8.5.12
2Ch	Fan Tachometer Reading 3 LSB	RO	8.5.13
2Dh	Fan Tachometer Reading 3 MSB	RO	8.5.14
2Eh	Fan Tachometer Reading 4 LSB	RO	8.5.15
2Fh	Fan Tachometer Reading 4 MSB	RO	8.5.16
30h	FANPWM1 Current Duty	R/W or RO[1]	8.5.17
31h	FANPWM2 Current Duty	R/W or RO[1]	8.5.18
32h	FANPWM3 Current Duty	R/W or RO[1]	8.5.19
33h-3Dh	Reserved		
3Eh	COMPANY ID	RO	8.5.20
3Fh	Version	RO	8.5.21
40h	Configuration	R/W	8.5.22
41h	Status Register 1	RO	8.5.23
42h	Status Register 2	RO	8.5.24
43h	Tach Mode	R/W	8.5.60
44h	Voltage Low Limit 2.5V	R/W or RO[2]	8.5.27
45h	Voltage High Limit 2.5V	R/W or RO[2]	8.5.28
46h	Voltage Low Limit Vccp	R/W or RO[2]	8.5.29
47h	Voltage High Limit Vccp	R/W or RO[2]	8.5.30
48h	Voltage Low Limit 3.3V	R/W or RO[2]	8.5.31

8.0 Health Management (HM) (Continued)

Address	Register Name	Type	Section
49h	Voltage High Limit 3.3V	R/W or RO[2]	8.5.32
4Ah	Voltage Low Limit 5V	R/W or RO[2]	8.5.33
4Bh	Voltage High Limit 5V	R/W or RO[2]	8.5.34
4Ch	Voltage Low Limit 12V	R/W or RO[2]	8.5.35
4Dh	Voltage High Limit 12V	R/W or RO[2]	8.5.36
4Eh	Temperature Low Limit Zone1	R/W or RO[2]	8.5.37
4Fh	Temperature High Limit Zone1	R/W or RO[2]	8.5.38
50h	Temperature Low Limit Zone2	R/W or RO[2]	8.5.39
51h	Temperature High Limit Zone2	R/W or RO[2]	8.5.40
52h	Temperature Low Limit Zone3	R/W or RO[2]	8.5.41
53h	Temperature High Limit Zone3	R/W or RO[2]	8.5.42
54h	Fan Tachometer1 Low Limit LSB	R/W or RO[2]	8.5.43
55h	Fan Tachometer1 Low Limit MSB	R/W or RO[2]	8.5.44
56h	Fan Tachometer2 Low Limit LSB	R/W or RO[2]	8.5.45
57h	Fan Tachometer2 Low Limit MSB	R/W or RO[2]	8.5.46
58h	Fan Tachometer3 Low Limit LSB	R/W or RO[2]	8.5.47
59h	Fan Tachometer3 Low Limit MSB	R/W or RO[2]	8.5.48
5Ah	Fan Tachometer4 Low Limit LSB	R/W or RO[2]	8.5.49
5Bh	Fan Tachometer4 Low Limit MSB	R/W or RO[2]	8.5.50
5Ch	FANPWM1 Control Configuration	R/W or RO[3]	8.5.76
5Dh	FANPWM2 Control Configuration	R/W or RO[3]	8.5.77
5Eh	FANPWM3 Control Configuration	R/W or RO[3]	8.5.78
5Fh	Zone1 Auto Speed Range and FANPWM1 Frequency	R/W or RO[3]	8.5.71
60h	Zone2 Auto Speed Range and FANPWM2 Frequency	R/W or RO[3]	8.5.72
61h	Zone3 Auto Speed Range and FANPWM3 Frequency	R/W or RO[3]	8.5.73
62h	Min/Off, Spike Smoothing 1	R/W or RO[3]	8.5.74
63h	Min/Off, Spike Smoothing 2	R/W or RO[3]	8.5.75
64h	FANPWM1 Minimum	R/W or RO[3]	8.5.79
65h	FANPWM2 Minimum	R/W or RO[3]	8.5.80
66h	FANPWM3 Minimum	R/W or RO[3]	8.5.81
67h	Zone1 Temperature Limit	R/W or RO[3]	8.5.63
68h	Zone2 Temperature Limit	R/W or RO[3]	8.5.64
69h	Zone3 Temperature Limit	R/W or RO[3]	8.5.65

8.0 Health Management (HM) (Continued)

Address	Register Name	Type	Section
6Ah	Zone1 Absolute Temperature Limit	R/W or RO[3]	8.5.66
6Bh	Zone2 Absolute Temperature Limit	R/W or RO[3]	8.5.67
6Ch	Zone3 Absolute Temperature Limit	R/W or RO[3]	8.5.68
6Dh	Zone1, Zone2 Hysteresis	R/W or RO[3]	8.5.69
6Eh	Zone3 Hysteresis	R/W or RO[3]	8.5.70
6Fh	Tach PWM Association	R/W	8.5.62
70h	FANPWM1 Maximum Duty	R/W or RO[3]	8.5.82
71h	FANPWM2 Maximum Duty	R/W or RO[3]	8.5.83
72h	FANPWM3 Maximum Duty	R/W or RO[3]	8.5.84
73h	Status Register 3	RO	8.5.25
74h	Status Register 4	RO	8.5.26
75h	Monitoring Control	R/W or RO[3]	8.5.54
76h	Extended FANPWM Control 1	R/W or RO[3]	8.5.85
77h	Extended FANPWM Control 2	R/W or RO[3]	8.5.86
78h	Tachometer Monitoring Control	R/W or RO[3]	8.5.61
79h	Channels V_{DD} Configuration	R/W or RO[3]	8.5.55
7Ah	Temperature Critical Limit Zone1	R/W or RO[2]	8.5.51
7Bh	Temperature Critical Limit Zone1	R/W or RO[2]	8.5.52
7Ch	Temperature Critical Limit Zone2	R/W or RO[2]	8.5.53
7Dh	Temperature Zone1 Gain and Offset Correction	R/W or RO[3]	8.5.56
7Eh	Temperature Zone2 Gain and Offset Correction	R/W or RO[3]	8.5.57
7Fh	Temperature Zone3 Gain and Offset Correction	R/W or RO[3]	8.5.58
80h	Enhanced Thermal Control	R/W or RO[3]	8.5.59
81h-FFh	Reserved		

1. Read-only, when fan control is not in manual mode.
2. Locked by the LOCK_LIM bit in the Monitoring Control register.
3. Locked by the LOCK bit in the Configuration register.

8.0 Health Management (HM) (Continued)

8.5.1 Voltage Reading 2.5V

Reflects current voltage of 2.5V monitoring.

Location: 20h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**VOLT_DATA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**VOLT_DATA.** The high byte of the voltage data measured by the associated LMxx Sensor device. The data is interpreted as a left-aligned positive value: MSBit of the LMxx Voltage Readout register maps to bit 7 of VOLT_DATA field.

8.5.2 Voltage Reading Vccp

Reflects current voltage of Vccp monitoring.

Location: 21h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**VOLT_DATA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**VOLT_DATA.** The high byte of the voltage data measured by the associated LMxx Sensor device. The data is interpreted as a left-aligned positive value: MSBit of the LMxx Voltage Readout register maps to bit 7 of VOLT_DATA field.

8.5.3 Voltage Reading 3.3V

Reflects current voltage of 3.3V monitoring.

Location: 22h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**VOLT_DATA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**VOLT_DATA.** The high byte of the voltage data measured by the associated LMxx Sensor device. The data is interpreted as a left-aligned positive value: MSBit of the LMxx Voltage Readout register maps to bit 7 of VOLT_DATA field.

8.0 Health Management (HM) (Continued)

8.5.4 Voltage Reading 5V

Reflects current voltage of 5V monitoring.

Location: 23h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**VOLT_DATA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**VOLT_DATA.** The high byte of the voltage data measured by the associated LMxx Sensor device. The data is interpreted as a left-aligned positive value: MSBit of the LMxx Voltage Readout register maps to bit 7 of VOLT_DATA field.

8.5.5 Voltage Reading 12V

Reflects current voltage of 12V monitoring.

Location: 24h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**VOLT_DATA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**VOLT_DATA.** The high byte of the voltage data measured by the associated LMxx Sensor device. The data is interpreted as a left-aligned positive value: MSBit of the LMxx Voltage Readout register maps to bit 7 of VOLT_DATA field.

8.5.6 Temperature Reading Zone1

Reflects current Zone1 temperature.

Location: 25h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**TEMP_DATA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**TEMP_DATA.** The high byte of the Temperature Zone1 data measured by the associated LMxx Sensor device. The data is converted to a left-aligned 2's complement value. The value represented in this register is dependent on the setting of the ZONE1_RANGE bit in the Monitor Control Register (see Section 8.5.54 on page 176). If ZONE1_RANGE is 0 the LSBit of this register represents a value of 1°C (temperature values are between -127°C (81h) and +127°C (7Fh)). If ZONE1_RANGE bit is 1 the LSBit of this register represents a value of 2°C (temperature values are between -254°C (81h) and +254°C (7Fh)). A value of 80h represents a sensor error. **Notes:** 1. TEMP_DATA is obtained by translating the Temperature Readout register data from the LMxx Sensor device, according to the algorithm shown in Figure 37 on page 158. Limit checking is done only after the temperature data has been modified (if necessary). 2. The temperature data can be low-pass filtered by setting the TEMP_FILT bit in the Monitoring Control register (see Section 8.5.54 on page 176).

8.0 Health Management (HM) (Continued)

LMxx Readout register data: LM96011/LM96010/LM96012, 16-bit format temperature data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB	128°C	64°C	32°C	16°C	8°C	4°C	2°C	1°C	0.5°C	0	0	0	0	0	0

Active bits

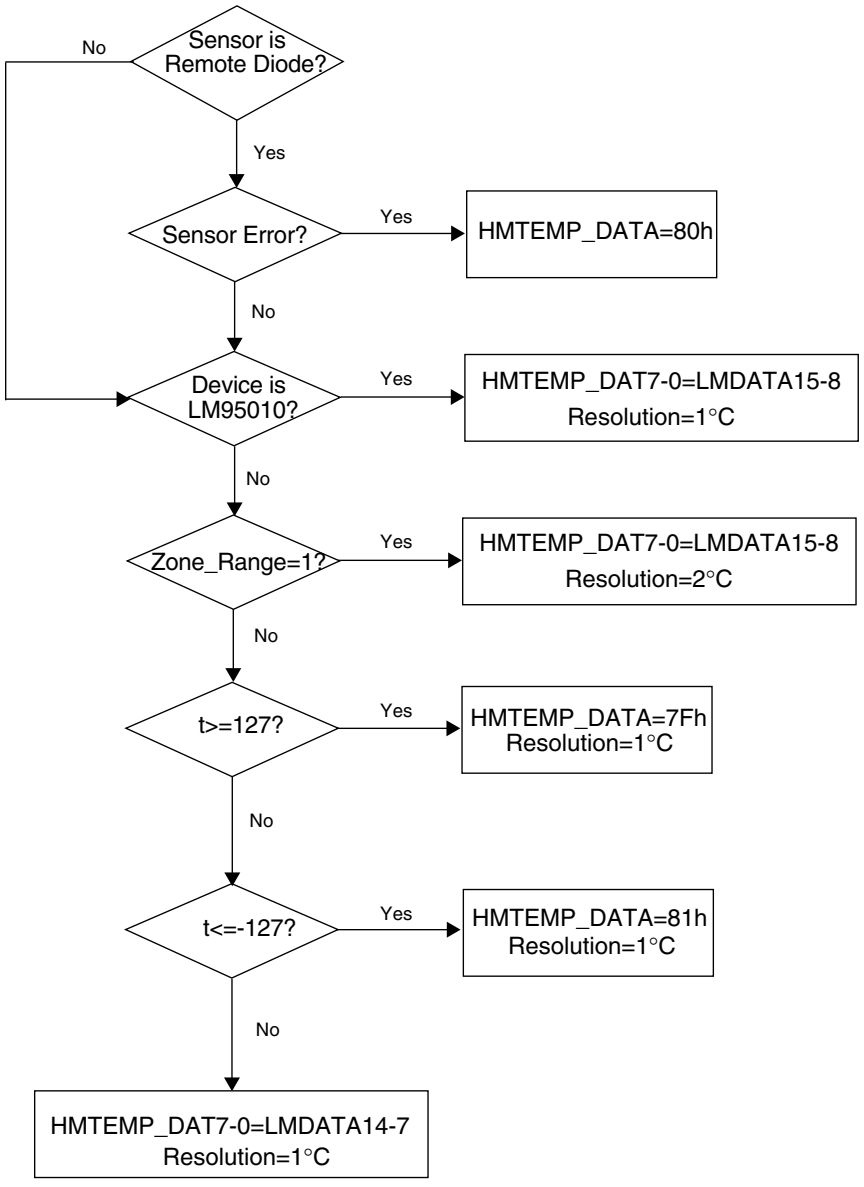
HM Temperature Reading Zone 'n' data: HM, TEMP_DATA field, 8-bit format temperature data

ZONEn_RANGE = 0

7	6	5	4	3	2	1	0
MSB	64°C	32°C	16°C	8°C	4°C	2°C	1°C

ZONEn_RANGE = 1

7	6	5	4	3	2	1	0
MSB	128°C	64°C	32°C	16°C	8°C	4°C	2°C



t = numerical value of LM96011/LM96010/LM96012 format temperature data

Figure 37. Temperature Data Translation from LMxx Device to HM Temperature Zone Registers

8.0 Health Management (HM) (Continued)

8.5.7 Temperature Reading Zone2

Reflects current Zone2 temperature.

Location: 26h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**TEMP_DATA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**TEMP_DATA.** Same as TEMP_DATA of Temperature Reading Zone1 register, but for Zone2.

8.5.8 Temperature Reading Zone3

Reflects current Zone3 temperature.

Location: 27h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**TEMP_DATA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**TEMP_DATA.** Same as TEMP_DATA of Temperature Reading Zone1 register, but for Zone3. Also, if only an LM96011 device is connected to the SensorPath Bus and an optional LM95010 device is not present, this field shows a value of 80h.

8.5.9 Fan Tachometer Reading 1 LSB

Contains the number of 90 KHz clock cycles during a full fan revolution, LSB byte.

Location: 28h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**TACH_LOW**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**TACH_LOW.** The low byte of 90 KHz clock cycles during a full fan revolution of Fan Tachometer 1. If the fan is not spinning, the fan is spinning-up or there is a speed measurement error, the value returned in the MSByte and LSByte, together, is FFFFh. Note that correct results depend on using fans that produce two tachometer pulses per full revolution or one pulse per fan revolution (configured by the TPPR1 bit in the Tachometer Monitoring Control register; see Section 8.5.61 on page 180). Whenever TACH_LOW register is read, the high byte of the tachometer Reading (TACH_HIGH) is latched to save the current fan speed value until TACH_HIGH register is read. Therefore, TACH_LOW must be read first and TACH_HIGH must be read immediately after. Note that internally, only one latch is used for all fan tachometer readings. The two bytes of a tachometer data must be read before reading the next tachometer data; otherwise, the read data may be incorrect. The fan speed data is updated every 1s.

8.0 Health Management (HM) (Continued)

8.5.10 Fan Tachometer Reading 1 MSB

Contains the number of 90 KHz clock cycles during a full fan revolution, MSB byte.

Location: 29h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**TACH_HIGH**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**TACH_HIGH.** The high byte of 90 KHz clock cycles during a full fan revolution of Fan Tachometer 1. If the fan is not spinning or there is a speed measurement error, the value returned in the MSByte and LSByte, together, is FFFFh.

8.5.11 Fan Tachometer Reading 2 LSB

Contains the number of 90 KHz clock cycles during a full fan revolution, LSB byte.

Location: 2Ah

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**TACH_LOW**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**TACH_LOW.** Same as TACH_LOW of Fan Tachometer Reading 1 LSB register, but for Fan Tachometer 2.

8.5.12 Fan Tachometer Reading 2 MSB

Contains the number of 90 KHz clock cycles during a full fan revolution, MSB byte.

Location: 2Bh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**TACH_HIGH**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**TACH_HIGH.** Same as TACH_HIGH of Fan Tachometer Reading 1 MSB register, but for Fan Tachometer 2.

8.5.13 Fan Tachometer Reading 3 LSB

Contains the number of 90 KHz clock cycles during a full fan revolution, LSB byte.

Location: 2Ch

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**TACH_LOW**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**TACH_LOW.** Same as TACH_LOW of Fan Tachometer Reading 1 LSB register, but for Fan Tachometer 3.

8.0 Health Management (HM) (Continued)

8.5.14 Fan Tachometer Reading 3 MSB

Contains the number of 90 KHz clock cycles during a full fan revolution, MSB byte.

Location: 2Dh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**TACH_HIGH**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**TACH_HIGH.** Same as TACH_HIGH of Fan Tachometer Reading 1 MSB register, but for Fan Tachometer 3.

8.5.15 Fan Tachometer Reading 4 LSB

Contains the number of 90 KHz clock cycles during a full fan revolution, LSB byte.

Location: 2Eh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**TACH_LOW**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**TACH_LOW.** Same as TACH_LOW of Fan Tachometer Reading 1 LSB register, but for Fan Tachometer 4.

8.5.16 Fan Tachometer Reading 4 MSB

Contains the number of 90 KHz clock cycles during a full fan revolution, MSB byte.

Location: 2Fh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**TACH_HIGH**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**TACH_HIGH.** Same as TACH_HIGH of Fan Tachometer Reading 1 MSB register, but for Fan Tachometer 4.

8.5.17 FANPWM1 Current Duty

Current FANPWM1 duty cycle.

Location: 30h

Type: R/W or RO (Becomes read-only when FANPWM1 Configuration is not set for manual mode.)

Bit	7	6	5	4	3	2	1	0
Name	**PWM_DUTY**							
Reset	1	1	1	1	1	1	1	1

8.0 Health Management (HM) (Continued)

Bit	Description
7-0	**PWM_DUTY.** Holds the current value of the duty cycle of the associated FANPWM signal. The behavior of this field depends on the FANPWM Control Configuration register: • In Manual mode, PWM_DUTY field is R/W: the value written selects the duty cycle of the FANPWM output. • In all other modes, PWM_DUTY field is RO: its value indicates the current duty cycle of the FANPWM output. During spin-up PWM_DUTY field is 0. A value of 00h represents 0% duty cycle; a value of FFh represents 100% duty cycle.

8.5.18 FANPWM2 Current Duty

Current FANPWM2 duty cycle.

Location: 31h

Type: R/W or RO (Becomes read-only when FANPWM2 Configuration is not set for manual mode.)

Bit	7	6	5	4	3	2	1	0
Name	**PWM_DUTY**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**PWM_DUTY.** Same as PWM_DUTY of FANPWM1 Current Duty register, but for FANPWM2.

8.5.19 FANPWM3 Current Duty

Current FANPWM3 duty cycle.

Location: 32h

Type: R/W or RO (Becomes read-only when FANPWM3 Configuration is not set for manual mode.)

Bit	7	6	5	4	3	2	1	0
Name	**PWM_DUTY**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**PWM_DUTY.** Same as PWM_DUTY of FANPWM1 Current Duty register, but for FANPWM3.

8.5.20 Company ID

Company identification number.

Location: 3Eh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**COMP_ID**							
Reset	0	0	0	0	0	0	0	1

Bit	Description
7-0	**COMP_ID.** Company identification number: 01h.

8.0 Health Management (HM) (Continued)

8.5.21 Version

Version and stepping identifiers.

Location: 3Fh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**VER**				**STEP**			
Reset	0	1	1	0	1	0	0	0

Bit	Description
7-4	**VER.** HM version.
3-0	**STEP.** HM version stepping. For A0 stepping, the value is 1000b; for A1 it is 1001b; for A2 it is 1010b, etc.

8.5.22 Configuration

Configuration register.

Location: 40h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**SMBR**	**OVRID**	**READY**	**LOCK**	**START**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7-5	R/W	**Reserved.**
4	R/W	**SMBR (SMBus Read).** When set to 1, access through the SMBus is read-only. This bit can be set only through the LPC Bus. It is read-only for access through the SMBus. 0: Full SMBus access to the HM registers (default) 1: Read-only SMBus access to the HM registers
3	R/W	**OVRID (Override FANPWM Configuration).** When set to 1, all FANPWM outputs are set to the value contained in the MAX_PWM field of the associated FANPWMn MAX Duty registers (see Section 8.5.82 on page 189 to Section 8.5.84) regardless of LOCK bit. 0: FANPWM outputs are controlled by Fan Control Configuration register; see Section 8.5.76 on page 187 to Section 8.5.78 (default) 1: FANPWM outputs are set to MAX_PWM duty cycle
2	RO	**READY.** Is set to 1 when the HM is ready for operation. While Ready is 0 Health monitoring and Fan control functions are disabled. 0: The HM is reset or initializing (default) 1: The HM is enabled and ready for operation
1	R/W or RO	**LOCK.** When set to 1, locks itself and the following HM registers: FANPWM1-3 Control Configuration, Fan1-3 Auto Speed Range and PWM Frequency, Min/Off Spike Smoothing 1-2, FANPWM1-3 Minimum, Zone1-Zone3 Temperature Limit, Zone1-Zone3 Absolute temperature Limit, Zone1, Zone2, Zone3 Hysteresis, Extended FANPWM Control 1, Extended FANPWM Control 2, Monitoring Control, Tachometer Monitoring Control, Channels V_{DD} Configuration, Temperature Zones1-3 Gain and Offset Correction, FANPWM1-3 Maximum Duty. This bit is reset by Hardware reset. 0: All R/W HM registers are enabled for write (default) 1: Specified HM registers are RO

8.0 Health Management (HM) (Continued)

Bit	Type	Description
0	R/W	**START.** When this bit is reset to 0, monitoring and FANPWM output control functions based on the limit and parameter registers are disabled, and all status bits in Status Registers 1,2 and 3 are cleared. In this case, all registers not locked by LOCK can be modified, but they do not affect the Health monitor and control functions of the HM. START bit is always writable regardless of LOCK bit. When this bit is set to 1, Monitoring and FANPWM output control functions based on limit and parameter registers are enabled. START bit is reset to 0 by a V_{SB} Power-Up reset. Then, HM performs the following: • After READY bit becomes 1, Temperature Zone1 is monitored (although START bit is 0). If a temperature above +110°C is detected, ETC is asserted (see Section 8.2.10 on page 139), which turns the Main power supply off. • The FANPWM outputs are at 0% duty cycle; they are set to a different value after either of the following occurs: — Two seconds elapsed since the V_{DD3} power has been turned on (FANPWM outputs are set to the value contained in the associated FANPWMn MAX Duty registers) — START bit is set to 1

8.5.23 Status Register 1

Event status register 1. This register is accessible only through SMBus.

Note: All status bits in this register are reset when START bit of the Configuration register is reset.

Location: 41h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**STAT_REG2_ERR**	**ZONE3_ERR**	**ZONE2_ERR**	**ZONE1_ERR**	**5V_ERR**	**3.3V_ERR**	**Vccp_ERR**	**2.5V_ERR**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**STAT_REG2_ERR.** Is set to 1 if one of the bits in Status Register 2 is set. Once set, the bit is cleared only after the Status Register 2 is read and then, the Status Register 1 is read. 0: No event is set in Interrupt Status Register 2 (default) 1: At least one of the event bits in Status Register 2 is set
6	**ZONE3_ERR.** Is set to 1 when Zone3 temperature is less than the limit set in the corresponding Low Temp register (see Section 8.5.41 on page 172) or greater than the limit set in the corresponding High Temp register (see Section 8.5.42 on page 172). Once set, the bit is updated again only after this register is read. 0: Temperature does not exceed any respective (default) 1: Temperature exceeds a respective limit
5	**ZONE2_ERR.** Is set to 1 when Zone2 temperature is less than the limit set in the corresponding Low Temp register (see Section 8.5.39 on page 171) or greater than the limit set in the corresponding High Temp register (see Section 8.5.40 on page 172). Once set, the bit is updated again only after this register is read. 0: Temperature does not exceed any respective limit (default) 1: Temperature exceeds a respective limit
4	**ZONE1_ERR.** Is set to 1 when Zone1 temperature is less than the limit set in the corresponding Low Temp register (see Section 8.5.37 on page 171) or greater than the limit set in the corresponding High Temp register (see Section 8.5.38 on page 171). Once set, the bit is updated again only after this register is read. 0: Temperature does not exceed any respective limit (default) 1: Temperature exceeds a respective limit

8.0 Health Management (HM) (Continued)

Bit	Description
3	**5V_ERR.** Is set to 1 when 5V input voltage is less than the limit set in the corresponding Low Limit register (see Section 8.5.33 on page 169) or greater than the limit set in the corresponding High Limit register (see Section 8.5.34 on page 170). Once set, the bit is updated again only after this register is read. 0: Voltage does not exceed any respective limit (default) 1: Voltage exceeds a respective limit
2	**3.3V_ERR.** Is set to 1 when 3.3V input voltage is less than the limit set in the corresponding Low Limit register (see Section 8.5.31 on page 169) or greater than the limit set in the corresponding High Limit register (see Section 8.5.32 on page 169). Once set, the bit is updated again only after this register is read. 0: Voltage does not exceed any respective limit (default) 1: Voltage exceeds a respective limit
1	**Vccp_ERR.** Is set to 1 when Vccp input voltage is less than the limit set in the corresponding Low Limit register (see Section 8.5.29 on page 168) or greater than the limit set in the corresponding High Limit register (see Section 8.5.30 on page 168). Once set, the bit is updated again only after this register is read. 0: Voltage does not exceed any respective limit (default) 1: Voltage exceeds a respective limit
0	**2.5V_ERR.** Is set to 1 when 2.5V input voltage is less than the limit set in the corresponding Low Limit register (see Section 8.5.27 on page 167) or greater than the limit set in the corresponding High Limit register (see Section 8.5.28 on page 168). Once set, the bit is updated again only after this register is read. 0: Voltage does not exceed any respective limit (default) 1: Voltage exceeds a respective limit

8.5.24 Status Register 2

Event status register 2.This register is accessible only through the SMBus.

Note: All status bits in this register are reset when START bit of the Configuration register is reset.

Location: 42h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**DEV2_Fault**	**RD_Fault**	**FAN4_ STALL**	**FAN3_ STALL**	**FAN2 STALL**	**FAN1_ STALL**	**DEV1_Fault**	**12V_ERR**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**DEV2_Fault (Device 2 Fault).** Is set to 1 when a communication problem with the optional LM95010 device occurs. Once set, the bit is updated again only after this register is read. 0: The optional LM95010 device does not exist or exists with valid communication (default) 1: A communication problem with LM95010
6	**RD_Fault (Remote Diode Fault).** Is set to 1 when there is a physical connection fault in one of the Remote Diodes of the Temperature Zones occur (for LM96011: Zone1; for LM96010 or LM96012: Zone1 or Zone3). Once set, the bit is updated again only after this register is read. 0: Proper connection of Remote Diode (default) 1: Remote Diode connection fault
5	**FAN4_STALL.** Is set to 1 when Fan 4 is either stalled or running at low speed (according to the FSTLMD bit in the associated Extended FANPWM Control register; see Section 8.5.85 on page 190). Once set, the bit is updated again only after this register is read. 0: Fan operating normally (default) 1: Fan is either stalled or running at low speed

8.0 Health Management (HM) (Continued)

Bit	Description
4	**FAN3_STALL.** Is set to 1 when Fan 3 is either stalled or running at low speed (according to the FSTLMD bit in the associated Extended FANPWM Control register; see Section 8.5.85 on page 190). Once set, the bit is updated again only after this register is read. 0: Fan operating normally (default) 1: Fan is either stalled or running at low speed
3	**FAN2_STALL.** Is set to 1 when Fan 2 is either stalled or running at low speed (according to the FSTLMD bit in the associated Extended FANPWM Control register; see Section 8.5.85 on page 190). Once set, the bit is updated again only after this register is read. 0: Fan operating normally (default) 1: Fan is either stalled or running at low speed
2	**FAN1_STALL.** Is set to 1 when Fan 1 is either stalled or running at low speed (according to the FSTLMD bit in the associated Extended FANPWM Control register; see Section 8.5.85 on page 190). Once set, the bit is updated again only after this register is read. 0: Fan operating normally (default) 1: Fan is either stalled or running at low speed
1	**DEV1_Fault (Device 1 Fault).** Is set to 1 when a communication problem with the LM96011, LM96010 or LM96012 device occurs. Once set, the bit is updated again only after this register is read. 0: Communication with LM96011/LM96010/LM96012 is functional (default) 1: Communication problem with LM96011/LM96010/LM96012
0	**12V_ERR.** Is set to 1 when 12V input voltage is less than the limit set in the corresponding Low Limit register (see Section 8.5.35 on page 170) or greater than the limit set in the corresponding High Limit register (see Section 8.5.36 on page 170). Once set, the bit is updated again only after this register is read. 0: Voltage does not exceed any respective limit (default) 1: Voltage exceeds a respective limit

8.5.25 Status Register 3

Event status register 3. This register is accessible only through SMBus.

Note: All status bits in this register are reset when START bit of the Configuration register is reset.

Location: 73h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**CRIT3_ERR**	**CRIT2_ERR**	**CRIT1_ERR**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved.**
2	**CRIT3_ERR.** Is set to 1 when Zone3 temperature is more than the limit set in the corresponding Temperature Critical Limit register (see Section 8.5.53 on page 175). Once set, the bit is updated again only after this register is read. 0: Temperature does not exceed the critical limit (default) 1: Temperature exceeds the critical limit
1	**CRIT2_ERR.** Is set to 1 when Zone2 temperature is more than the limit set in the corresponding Temperature Critical Limit register (see Section 8.5.52 on page 175). Once set, the bit is updated again only after this register is read. 0: Temperature does not exceed the critical limit (default) 1: Temperature exceeds the critical limit

8.0 Health Management (HM) (Continued)

Bit	Description
0	**CRIT1_ERR.** Is set to 1 when Zone1 temperature is more than the limit set in the corresponding Temperature Critical Limit register (see Section 8.5.51 on page 175). Once set, the bit is updated again only after this register is read. 0: Temperature does not exceed the critical limit (default) 1: Temperature exceeds the critical limit

8.5.26 Status Register 4

Location: 74h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**FAN4_OFF**	**FAN3_OFF**	**FAN2_OFF**	**FAN1_OFF**
Reset	0	0	0	0	1	1	1	1

Bit	Description
7-4	**Reserved.**
3	**FAN4_OFF.** When set, this bit indicates for Fan Tachometer 4 that the associated FANPWM signal (see Section 8.5.62 on page 181) driving the fan is in one of the following states: • Fan turned off: The Duty Cycle of the associated FANPWM output is 0% • Fan spinning-up: The rotational speed of the fan driven by the associated FANPWM output is increasing from 0 • Fan stopping: The rotational speed of the fan driven by the associated FANPWM output is decreasing to 0 When FAN4_OFF bit is set, Fan Tachometer 4 registers are set to FFFFh, and the following bits are set to 0: FAN4_STALL status bit of Status Register 2 (see Section 8.5.24 on page 165), and FAN4_STS of HM Sensor Status Register 2 (see Section 8.4.9 on page 148). When FAN4_OFF bit returns to 0, the status bits and Fan Tachometer registers are released (can be updated). 0: Fan rotating 1: Fan off, spinning-up or stopping (default)
2-0	**FAN3_OFF - FAN1_OFF.** Same as FAN4_OFF for Fan Tachometer 3-1.

8.5.27 Voltage Low Limit 2.5V

Voltage low limit for 2.5V voltage monitoring.

Location: 44h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**LOW_LIMIT**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**LOW_LIMIT.** The low limit value to which the associated voltage input data is compared. If the voltage input data is lower than LOW_LIMIT, the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.4 on page 143, Section 8.4.8 on page 147, and Section 8.5.23 on page 164).

8.0 Health Management (HM) (Continued)

8.5.28 Voltage High Limit 2.5V

Voltage high limit for 2.5V voltage monitoring.

Location: 45h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**HIGH_LIMIT**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**HIGH_LIMIT.** The high limit value to which the associated voltage input data is compared. If the voltage input data is higher than HIGH_LIMIT, the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.4 on page 143, Section 8.4.8 on page 147, and Section 8.5.23 on page 164).

8.5.29 Voltage Low Limit Vccp

Voltage low limit for Vccp voltage monitoring.

Location: 46h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**LOW_LIMIT**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**LOW_LIMIT.** The low limit value to which the associated voltage input data is compared. If the voltage input data is lower than LOW_LIMIT, the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.4 on page 143, Section 8.4.8 on page 147, and Section 8.5.23 on page 164).

8.5.30 Voltage High Limit Vccp

Voltage high limit for Vccp voltage monitoring.

Location: 47h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**HIGH_LIMIT**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**HIGH_LIMIT.** The high limit value to which the associated voltage input data is compared. If the voltage input data is higher than HIGH_LIMIT, the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.4 on page 143, Section 8.4.8 on page 147, and Section 8.5.23 on page 164).

8.0 Health Management (HM) (Continued)

8.5.31 Voltage Low Limit 3.3V

Voltage low limit for 3.3V voltage monitoring.

Location: 48h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**LOW_LIMIT**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**LOW_LIMIT.** The low limit value to which the associated voltage input data is compared. If the voltage input data is lower than LOW_LIMIT, the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.4 on page 143, Section 8.4.8 on page 147, and Section 8.5.23 on page 164).

8.5.32 Voltage High Limit 3.3V

Voltage high limit for 3.3V voltage monitoring.

Location: 49h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**HIGH_LIMIT**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**HIGH_LIMIT.** The high limit value to which the associated voltage input data is compared. If the voltage input data is higher than HIGH_LIMIT, the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.4 on page 143, Section 8.4.8 on page 147, and Section 8.5.23 on page 164).

8.5.33 Voltage Low Limit 5V

Voltage low limit for 5V voltage monitoring.

Location: 4Ah

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**LOW_LIMIT**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**LOW_LIMIT.** The low limit value to which the associated voltage input data is compared. If the voltage input data is lower than LOW_LIMIT, the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.4 on page 143, Section 8.4.8 on page 147, and Section 8.5.23 on page 164).

8.0 Health Management (HM) (Continued)

8.5.34 Voltage High Limit 5V

Voltage high limit for 5V voltage monitoring.

Location: 4Bh

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**HIGH_LIMIT**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**HIGH_LIMIT.** The high limit value to which the associated voltage input data is compared. If the voltage input data is higher than HIGH_LIMIT, the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.4 on page 143, Section 8.4.8 on page 147, and Section 8.5.23 on page 164).

8.5.35 Voltage Low Limit 12V

Voltage low limit for 12V voltage monitoring.

Location: 4Ch

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**LOW_LIMIT**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**LOW_LIMIT.** The low limit value to which the associated voltage input data is compared. If the voltage input data is lower than LOW_LIMIT, the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.5 on page 144, Section 8.4.9 on page 148, and Section 8.5.24 on page 165).

8.5.36 Voltage High Limit 12V

Voltage high limit for 12V voltage monitoring.

Location: 4Dh

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**HIGH_LIMIT**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**HIGH_LIMIT.** The high limit value to which the associated voltage input data is compared. If the voltage input data is higher than HIGH_LIMIT, the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.5 on page 144, Section 8.4.9 on page 148, and Section 8.5.24 on page 165).

8.0 Health Management (HM) (Continued)

8.5.37 Temperature Low Limit Zone1

Temperature low limit for Zone1 temperature monitoring.

Location: 4Eh

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**LOW_LIMIT**							
Reset	1	0	0	0	0	0	0	1

Bit	Description
7-0	**LOW_LIMIT.** The low limit value to which the associated temperature input data is compared. If the temperature input data is lower than LOW_LIMIT, the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.5 on page 144, Section 8.4.9 on page 148, and Section 8.5.24 on page 165). LOW_LIMIT format is the same as the format of the corresponding Temperature Reading Zone1 register (see Section 37 on page 158). This format is dependent on the setting of the ZONE1_RANGE bit in the Monitor Control Register (see Section 8.5.54 on page 176). The default value is 81h (-127°C for 1°C resolution, -254°C for 2°C resolution). **Note:** A value of 80h must not be used.

8.5.38 Temperature High Limit Zone1

Temperature high limit for Zone1 temperature monitoring.

Location: 4Fh

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**HIGH_LIMIT**							
Reset	0	1	1	1	1	1	1	1

Bit	Description
7-0	**HIGH_LIMIT.** The high limit value to which the associated temperature input data is compared. If the temperature input data is higher than HIGH_LIMIT, the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.5 on page 144, Section 8.4.9 on page 148, and Section 8.5.24 on page 165). HIGH_LIMIT format is the same as the format of the corresponding Temperature Reading Zone1 register (see Section 37 on page 158). This format is dependent on the setting of the ZONE1_RANGE bit in the Monitor Control Register (see Section 8.5.54 on page 176). The default value is 7Fh (127°C for 1°C resolution, 254°C for 2°C resolution). **Note:** A value of 80h must not be used.

8.5.39 Temperature Low Limit Zone2

Temperature low limit for Zone2 temperature monitoring.

Location: 50h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**LOW_LIMIT**							
Reset	1	0	0	0	0	0	0	1

Bit	Description
7-0	**LOW_LIMIT.** Same as LOW_LIMIT in Temperature Low Limit Zone1, but for Temperature Zone2.

8.0 Health Management (HM) (Continued)

8.5.40 Temperature High Limit Zone2

Temperature high limit for Zone2 temperature monitoring.

Location: 51h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**HIGH_LIMIT**							
Reset	0	1	1	1	1	1	1	1

Bit	Description
7-0	**HIGH_LIMIT.** Same as HIGH_LIMIT in Temperature Low Limit Zone1, but for Temperature Zone2.

8.5.41 Temperature Low Limit Zone3

Temperature low limit for Zone3 temperature monitoring.

Location: 52h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**LOW_LIMIT**							
Reset	1	0	0	0	0	0	0	1

Bit	Description
7-0	**LOW_LIMIT.** Same as LOW_LIMIT in Temperature Low Limit Zone1, but for Temperature Zone3.

8.5.42 Temperature High Limit Zone3

Temperature high limit for Zone3 temperature monitoring.

Location: 53h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**HIGH_LIMIT**							
Reset	0	1	1	1	1	1	1	1

Bit	Description
7-0	**HIGH_LIMIT.** Same as HIGH_LIMIT in Temperature Low Limit Zone1, but for Temperature Zone3.

8.0 Health Management (HM) (Continued)

8.5.43 Fan Tachometer1 Low Limit LSB

LSB of lowest permitted fan speed value.

Location: 54h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**FAN_MIN_LSB**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**FAN_MIN_LSB.** Contains the low byte of the Fan Tachometer value, which indicates the lowest permitted fan speed value setting. If the number of clock cycles counted in one fan revolution is higher than the Fan Tachometer value (FAN_MIN_LSB and FAN_MIN_MSB), the associated FANn_xxx bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are set to 1 (see Section 8.4.5 on page 144, Section 8.4.9 on page 148, and Section 8.5.24 on page 165). These status bits are never set to 1 if the Fan Tachometer Low Limit value is FFFFh. If the associated FANPWM output is set to Automatic fan control and if the SPIN_END bit in related Extended FANPWM Control register is set to 0, the Fan Tachometer Low Limit registers (FAN_MIN_LSB and FAN_MIN_MSB) indicate the fan speed at which the spin-up is ended (see Section 8.5.85 on page 190). In this case, a fan speed below the set value does **not** set the FANn_xxx bits to 1; a fan speed above the set value indicates the end of spin-up process (see “Speed Change Modes” on page 136). The two LSBits of this field are irrelevant and can be set to any value. For correct operation when writing a new value to the Low Limit registers, the Limit LSB register must be written before the Limit MSB register. Note that internally, only one latch is used for all Limit writing. The two bytes of a tachometer limit must be written before writing the next tachometer limit; otherwise, the written data may be incorrect.

8.5.44 Fan Tachometer1 Low Limit MSB

LSB of lowest permitted fan speed value.

Location: 55h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**FAN_MIN_MSB**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**FAN_MIN_MSB.** Contains the high byte of the Fan Tachometer value which indicates either the lowest permitted fan speed value setting or the fan speed at which the spin-up is ended.

8.5.45 Fan Tachometer2 Low Limit LSB

LSB of lowest permitted fan speed value.

Location: 56h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**FAN_MIN_LSB**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**FAN_MIN_LSB.** Same as FAN_MIN_LSB of Fan Tachometer1 Low Limit LSB register, but for Fan Tachometer 2.

8.0 Health Management (HM) (Continued)

8.5.46 Fan Tachometer2 Low Limit MSB

LSB of lowest permitted fan speed value.

Location: 57h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**FAN_MIN_MSB**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**FAN_MIN_MSB.** Same as FAN_MIN_MSB of Fan Tachometer1 Low Limit LSB register, but for Fan Tachometer 2.

8.5.47 Fan Tachometer3 Low Limit LSB

LSB of lowest permitted fan speed value.

Location: 58h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**FAN_MIN_LSB**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**FAN_MIN_LSB.** Same as FAN_MIN_LSB of Fan Tachometer1 Low Limit LSB register, but for Fan Tachometer 3.

8.5.48 Fan Tachometer3 Low Limit MSB

LSB of lowest permitted fan speed value.

Location: 59h

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**FAN_MIN_MSB**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**FAN_MIN_MSB.** Same as FAN_MIN_MSB of Fan Tachometer1 Low Limit LSB register, but for Fan Tachometer 3.

8.5.49 Fan Tachometer4 Low Limit LSB

LSB of lowest permitted fan speed value.

Location: 5Ah

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**FAN_MIN_LSB**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**FAN_MIN_LSB.** Same as FAN_MIN_LSB of Fan Tachometer1 Low Limit LSB register, but for Fan Tachometer 4.

8.0 Health Management (HM) (Continued)

8.5.50 Fan Tachometer4 Low Limit MSB

LSB of lowest permitted fan speed value.

Location: 5Bh

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**FAN_MIN_MSB**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**FAN_MIN_MSB.** Same as FAN_MIN_MSB of Fan Tachometer1 Low Limit LSB register, but for Fan Tachometer 4.

8.5.51 Temperature Critical Limit Zone1

Temperature critical limit for Zone1 temperature monitoring.

Location: 7Ah

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**CRIT_LIMIT**							
Reset	0	1	1	0	1	1	1	0

Bit	Description
7-0	**CRIT_LIMIT.** The critical limit value to which the associated temperature input data is compared. If the temperature input data is higher than CRIT_LIMIT the corresponding bits in the HM Interrupt Status register, HM Sensor Status Register and Status Register are updated/set (see Section 8.4.10 on page 149, Section 8.4.12 on page 150, and Section 8.5.25 on page 166). CRIT_LIMIT format is the same as the format of the corresponding Temperature Reading Zone1 register (note that this format is configurable). The default value is 6Eh (110°C for 1°C resolution, 220°C for 2°C resolution).

8.5.52 Temperature Critical Limit Zone2

Temperature critical limit for Zone2 temperature monitoring.

Location: 7Bh

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**CRIT_LIMIT**							
Reset	0	1	1	0	1	1	1	0

Bit	Description
7-0	**CRIT_LIMIT.** Same as CRIT_LIMIT in Temperature Critical Limit Zone1, but for Temperature Zone2.

8.5.53 Temperature Critical Limit Zone3

Temperature critical limit for Zone3 temperature monitoring.

Location: 7Ch

Type: R/W or RO (Becomes read-only when LOCK_LIM bit in the Monitoring Control register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**CRIT_LIMIT**							
Reset	0	1	1	0	1	1	1	0

Bit	Description
7-0	**CRIT_LIMIT.** Same as CRIT_LIMIT in Temperature Critical Limit Zone1, but for Temperature Zone3.

8.0 Health Management (HM) (Continued)

8.5.54 Monitoring Control

Location: 75h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**LOCK_LIM**	**VOLT_HYST**	**TEMP_HYST**	**Reserved**	**TEMP_FILT**	**ZONE3_ RANGE**	**ZONE2_ RANGE**	**ZONE1_ RANGE**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**LOCK_LIM**. When set to 1, locks itself and the following HM Limit registers: Voltage Low Limit (2.5V, Vccp, 3.3V, 5V, 12V), Voltage High Limit (2.5V, Vccp, 3.3V, 5V, 12V), Temperature Low Limit Zone1-3, Temperature High Limit Zone1-3, Fan Tachometer1-4 Low Limit LSB, Fan Tachometer1-4 Low Limit MSB, Temperature Critical Limit Zone1-3. This bit is reset by Hardware reset. 0: All R/W HM Limit registers are enabled for write (default) 1: Specified HM Limit registers are RO
6	**VOLT_HYST (Voltage Channels, Hysteresis).** Selects whether hysteresis is used when the voltage data in Voltage Reading registers is compared with the Voltage Low Limit and Voltage High Limit registers. 0: No hysteresis (default) 1: The hysteresis is equal to the LSBit multiplied by 4 of the (High or Low) Voltage Limit register
5	**TEMP_HYST (Temperature Channels, Hysteresis).** Selects whether hysteresis is used when the temperature data in Temperature Reading registers is compared with the Temperature Low Limit, Temperature High Limit and Temperature Critical Limit registers. Temperature hysteresis value is independent on the setting of the ZONE1_RANGE bit (bit 0, below). 0: No hysteresis (default) 1: Hysteresis of 4°C
4	**Reserved.**
3	**TEMP_FILT (Temperature Data Filter).** Selects whether a low-pass filter is applied to the temperature data read from the LMxx Sensor device. If this bit is 1, the temperature data is filtered before it is stored in the Temperature Reading Zone ‘n’ register. 0: No filter (default) 1: A low-pass filter with 673 ms rise time (0% to 95% of the incoming temperature change) is applied to the temperature channels
2	**ZONE3_RANGE.** Configures the temperature range shown in the Temperature Reading Zone3 register. The LSBit of the LMxx temperature MSByte represents a value of 2°C. When ZONE3_RANGE is 0, the LMxx temperature data is truncated to -127°C<=value<=127°C, with the LSB of the Temperature Reading register representing a value of 1°C. When ZONE3_RANGE is 1, the LMxx MSByte is translated to the Temperature Reading registers and represents a value such that -255°C<=value<=255°C, with the LSBit having a value of 2°C (see Figure 37 on page 158). **Note:** This bit is not relevant when an LM95010 device is used. 0: 1°C resolution for Temperature Reading register (default) 1: 2°C resolution for Temperature Reading register
1	**ZONE2_RANGE.** Same as ZONE3_RANGE, but for Zone2. This bit is always relevant (i.e., it is not dependent on the LMxx device used).
0	**ZONE1_RANGE.** Same as ZONE3_RANGE, but for Zone1. This bit is always relevant (i.e., it is not dependent on the LMxx device used).

8.0 Health Management (HM) (Continued)

8.5.55 Channel V_{DD} Configuration

Location: 79h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**ZONE3_VDD**	**ZONE2_VDD**	**ZONE1_VDD**	**12V_VDD**	**5V_VDD**	**3.3V_VDD**	**Vccp_VDD**	**2.5V_VDD**
Reset	0	0	1	0	0	0	1	0

Bit	Description
7	**ZONE3_VDD.** Is set to 1 to configure Zone3 Temperature Channel as a V_{DD} channel. In this case, when the V_{DD3} supply is off, monitoring of this channel is disabled and all the status bits are reset to 0 (except for the flags associated with the channel's critical limit). Monitoring is enabled and status bits are released, 182 ms after the V_{DD3} supply is turned back on. 0: Channel is not a V_{DD} channel (default) 1: Channel is a V_{DD} channel
6	**ZONE2_VDD.** Is set to 1 to configure Zone2 Temperature Channel as a V_{DD} channel. In this case, when the V_{DD3} supply is off, monitoring of this channel is disabled and all the status bits are reset to 0 (except for the flags associated with the channel's critical limit). Monitoring is enabled and status bits are released, 182 ms after the V_{DD3} supply is turned back on. 0: Channel is not a V_{DD} channel (default) 1: Channel is a V_{DD} channel
5	**ZONE1_VDD.** Is set to 1 to configure Zone1 Temperature Channel as a V_{DD} channel. In this case, when the V_{DD3} supply is off, monitoring of this channel is disabled and all the status bits are reset to 0 (except for the flags associated with the channel's critical limit). Monitoring is enabled and status bits are released, 182 ms after the V_{DD3} supply is turned back on. 0: Channel is not a V_{DD} channel 1: Channel is a V_{DD} channel (default)
4	**12V_VDD.** Is set to 1 to configure 12V Voltage Channel as a V_{DD} channel. In this case, when the V_{DD3} supply is off, monitoring of this channel is disabled and all the status bits are reset to 0. Monitoring is enabled and status bits are released, 182 ms after the V_{DD3} supply is turned back on. 0: Channel is not a V_{DD} channel (default) 1: Channel is a V_{DD} channel
3	**5V_VDD.** Is set to 1 to configure 5V Voltage Channel as a V_{DD} channel. In this case, when the V_{DD3} supply is off, monitoring of this channel is disabled and all the status bits are reset to 0. Monitoring is enabled and status bits are released, 182 ms after the V_{DD3} supply is turned back on. 0: Channel is not a V_{DD} channel (default) 1: Channel is a V_{DD} channel
2	**3.3V_VDD.** Is set to 1 to configure 3.3V Voltage Channel as a V_{DD} channel. In this case, when the V_{DD3} supply is off, monitoring of this channel is disabled and all the status bits are reset to 0. Monitoring is enabled and status bits are released, 182 ms after the V_{DD3} supply is turned back on. 0: Channel is not a V_{DD} channel (default) 1: Channel is a V_{DD} channel
1	**Vccp_VDD.** Is set to 1 to configure Vccp Voltage Channel as a V_{DD} channel. In this case, when the V_{DD3} supply is off, monitoring of this channel is disabled and all the status bits are reset to 0. Monitoring is enabled and status bits are released, 182 ms after the V_{DD3} supply is turned back on. 0: Channel is not a V_{DD} channel. 1: Channel is a V_{DD} channel (default)
0	**2.5V_VDD.** Is set to 1 to configure 2.5V Voltage Channel as a V_{DD} channel. In this case, when the V_{DD3} supply is off, monitoring of this channel is disabled and all the status bits are reset to 0. Monitoring is enabled and status bits are released, 182 ms after the V_{DD3} supply is turned back on. 0: Channel is not a V_{DD} channel (default) 1: Channel is a V_{DD} channel

8.0 Health Management (HM) (Continued)

8.5.56 Temperature Zone1 Gain and Offset Correction

Temperature gain and offset correction for Zone1 temperature monitoring.

Location: 7Dh

Type: R/W (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**GAIN**		**Reserved**		**OFFSET**			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**GAIN (Gain Correction).** Controls the gain correction applied to Zone1 temperature data. The incoming temperature data (after format modification, see Section 8.5.6 on page 157) is gain-corrected by multiplying by the gain correction value. **Bits 7 6 Gain Correction Value** 0 1: 1.0078125 dec. (1.0000001b) 0 0: 1 (no gain correction - default) 1 1: 0.9921875 dec. (0.1111111b) 1 0: 0.9843750 dec. (0.1111110b) In case of a sensor connection error (for Remote Diode sensor only), the incoming temperature data is not corrected according to GAIN field (the temperature data is set to 80h).
5-4	**Reserved.**
3-0	**OFFSET (Offset Correction).** Contains the offset correction value that is added (with sign) to the Zone1 temperature data. The incoming temperature data (after format modification, see Section 8.5.6 on page 157) is offset-corrected. The binary value of OFFSET field is interpreted as 4-bit, 2's complement value, with a resolution of 1°C/LSBit. The incoming temperature data is not corrected according to OFFSET field (i.e., the temperature data is set to 80h) if a sensor connection error occurs (for Remote Diode sensor only). **Bits 3-0 Offset Value (for Sensor Types '01' and '10')** 7h: +7°C 6h: +6°C . . . . 1h: +1°C 0h: 0°C (no offset correction - default) Fh: –1°C . . . . 9h: –7°C 8h: –8°C

8.5.57 Temperature Zone2 Gain and Offset Correction

Temperature gain and offset correction for Zone2 temperature monitoring.

Location: 7Eh

Type: R/W (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**GAIN**		**Reserved**		**OFFSET**			
Reset	0	0	0	0	0	0	0	0

8.0 Health Management (HM) (Continued)

Bit	Description
7-6	**GAIN (Gain Correction).** Same as GAIN in Temperature Zone1 Gain and Offset Correction register, but for Temperature Zone2.
5-4	**Reserved.**
3-0	**OFFSET (Offset Correction).** Same as OFFSET in Temperature Zone1 Gain and Offset Correction register, but for Temperature Zone2.

8.5.58 Temperature Zone3 Gain and Offset Correction

Temperature gain and offset correction for Zone3 temperature monitoring.

Location: 7Fh

Type: R/W (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**GAIN**		**Reserved**		**OFFSET**			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**GAIN (Gain Correction).** Same as GAIN in Temperature Zone1 Gain and Offset Correction register, but for Temperature Zone3.
5-4	**Reserved.**
3-0	**OFFSET (Offset Correction).** Same as OFFSET in Temperature Zone1 Gain and Offset Correction register, but for Temperature Zone3.

8.5.59 Enhanced Thermal Control Register

Location: 80h

Type: R/W (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**							**ETC_EN**
Reset	0	0	0	0	0	0	0	1

Bit	Description
7-1	**Reserved**
0	**ETC_EN**. When set to 1, the ETC internal signal is asserted if one of the following conditions is true: • The temperature data value in Temperature Zone1 is higher than the critical limit set in the Temperature Critical Limit Zone1 register. • A communication error with Device 1 (LM96011 or LM96010 or LM96012) occurs. • A major SensorPath Bus failure is detected. An asserted ETC signal turns off the Main power supply (via the Glue module). The resulting ETC signal is disabled when the V_{DD3} power is off and remains disabled until both of the following conditions are met: • The delay time (182 ms) for enabling V_{DD} channels (see Section 8.5.55 on page 177) after V_{DD3} power is turned on, has elapsed. • The temperature data in Temperature Zone1 was updated with a new value by the LMxx Sensor device If the temperature data from Device 1 (LM96011 or LM96010 or LM96012) is not updated for 728 ms after V_{DD3} power is on (see “Time-Out Function” on page 133), the HM assumes a communication error with the LMxx Sensor device occurred and asserts ETC. 0: Disable assertion of ETC 1: Enable assertion of ETC (default)

8.0 Health Management (HM) (Continued)

8.5.60 Tach Mode

Location: 43h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**FAN4_ MODE**	**FAN3_ MODE**	**FAN2_ MODE**	**FAN1_ MODE**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3-0	**FAN4_MODE-FAN1_MODE.** Sets Fan4-Fan1 monitoring mode according to Table 55.

Table 55. Fan Monitoring Configuration

FANn_MODE	Description
0	Measurements performed independently of any FANPWM output (default). Each measurement lasts one or two tachometer cycles, according to TPPR bit in Tachometer Monitoring Control register.
1	Measurements performed when the associated[1] FANPWM is at “On” level. The “On” level of the FANPWM signal can be extended to 1/2, one or two tachometer cycles, according to TPPR bit. A successful measurement requires only 1/2 a tachometer cycle.

1. See Tach PWM Association Register in Section 8.5.62 on page 181.

8.5.61 Tachometer Monitoring Control

Location: 78h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**TPPR4**	**TPPR3**	**TPPR2**	**TPPR1**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3	**TPPR4 (Tachometer Pulses Per Revolution 4).** Selects the number of pulses per fan revolution generated by FANTACH4 (and thus the division factor for the normalization of the fan speed data in the Fan Tachometer Reading 4 registers). 0: Two pulses per revolution (default) 1: One pulse per revolution
2	**TPPR3 (Tachometer Pulses Per Revolution 3).** Same as TPPR4, but for FANTACH3.
1	**TPPR2 (Tachometer Pulses Per Revolution 2).** Same as TPPR4, but for FANTACH2.
0	**TPPR1 (Tachometer Pulses Per Revolution 1).** Same as TPPR4, but for FANTACH1.

8.0 Health Management (HM) (Continued)

8.5.62 Tach PWM Association

Location: 6Fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**ASSOC4**		**ASSOC3**		**ASSOC2**		**ASSOC1**	
Reset	1	0	1	0	0	1	0	0

Bit	Description
7-6	**ASSOC4.** Sets FANTACH4 monitoring association with a PWM output according to Table 56 (default 10b).
5-4	**ASSOC3.** Sets FANTACH3 monitoring association with a PWM output according to Table 56 (default 10b).
3-2	**ASSOC2.** Sets FANTACH2 monitoring association with a PWM output according to Table 56 (default 01b).
1-0	**ASSOC1.** Sets FANTACH1 monitoring association with a PWM output according to Table 56 (default 00b).

Table 56. Fan Monitoring Association

ASSOC	Meaning
00	Measurements associated with FANPWM1
01	Measurements associated with FANPWM2
10	Measurements associated with FANPWM3
11	FANTACH is not associated with any FANPWM[1]

1. Use this value for the fans that are not connected or that do not have tachometer output.

8.5.63 Zone1 Temperature Limit

Location: 67h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**ZTEMP_LOW**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**ZTEMP_LOW.** Selects the temperature value for the low limit of the area in which the generated FANPWM duty cycle is proportional to the zone temperature. When the associated temperature equals this limit the fan is turned on (if it is not on already). When the temperature exceeds this limit, the fan speed will increase linearly as a function of temperature over the range defined in the associated Zone1 Auto Speed Range and FANPWM1 Frequency register (see Section 8.5.71 on page 183). The format of ZTEMP_LOW field is 8-bit left-aligned 2's complement value with the LSB being 1°C or 2°C, according to the setting of the ZONE1_RANGE bit in the Monitor Control Register (see Section 8.5.54 on page 176). Valid values for this field are: 81h (-127°C) to 7Fh (+127°C) for 1°C resolution, and 81h (-254°C) to 7Fh (+254°C) for 2°C resolution. A value of 80h is invalid.

8.0 Health Management (HM) (Continued)

8.5.64 Zone2 Temperature Limit

Location: 68h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**ZTEMP_LOW**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**ZTEMP_LOW.** Same as ZTEMP_LOW in Zone1 Temperature Limit register, but for Zone2.

8.5.65 Zone3 Temperature Limit

Location: 69h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**ZTEMP_LOW**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**ZTEMP_LOW.** Same as ZTEMP_LOW in Zone1 Temperature Limit register, but for Zone3.

8.5.66 Zone1 Absolute Temperature Limit

Location: 6Ah

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**ZTEMP_ABS**							
Reset	0	1	1	0	0	1	0	0

Bit	Description
7-0	**ZTEMP_ABS.** Selects the temperature value for the absolute limit. When the associated zone temperature is above the absolute limit, the duty cycle of all the FANPWM outputs is forced to full on (i.e., the value contained in the FANPWM1 MAX Duty register). When the zone temperature returns below the absolute limit, an 8°C hysteresis is provided. ZTEMP_ABS format is the same as the format of the corresponding Temperature Reading Zone1 register (see Section 8.5.6 on page 157). This format is dependent on the setting of the ZONE1_RANGE bit in the Monitor Control Register (see Section 8.5.54 on page 176). The default value is 64h (100°C for 1°C resolution, 200°C for 2°C resolution). Valid values for this field are from 81h to 7Fh. A value of 80h disables the Absolute Limit.

8.5.67 Zone2 Absolute Temperature Limit

Location: 6Bh

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**ZTEMP_ABS**							
Reset	0	1	1	0	0	1	0	0

Bit	Description
7-0	**ZTEMP_ABS.** Same as ZTEMP_ABS in Zone1 Absolute Temperature Limit register, but for Zone2.

8.0 Health Management (HM) (Continued)

8.5.68 Zone3 Absolute Temperature Limit

Location: 6Ch

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**ZTEMP_ABS**							
Reset	0	1	1	0	0	1	0	0

Bit	Description
7-0	**ZTEMP_ABS.** Same as ZTEMP_ABS in Zone1 Absolute Temperature Limit register, but for Zone3.

8.5.69 Zone1, Zone2 Hysteresis

Location: 6Dh

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**HYST1**				**HYST2**			
Reset	0	1	0	0	0	1	0	0

Bit	Description
7-4	**HYST1.** Selects the temperature value of the hysteresis used to process the associated zone temperature when the temperature is lower than the low limit set in Zone1 Temperature Limit register. If the temperature falls from above the Limit to below it, the fan remains at the minimum FANPWM duty cycle until the temperature has fallen an hysteresis amount below the Limit. **Value** **Description** 0d: No hysteresis 1d-15d: Hysteresis of 1°C to 15°C (default = 4°C)
3-0	**HYST2.** Same as HYST1, but for Zone2.

8.5.70 Zone3 Hysteresis

Location: 6Eh

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**HYST3**				**Reserved**			
Reset	0	1	0	0	0	1	0	0

Bit	Description
7-4	**HYST3.** Same as HYST1 in Zone1, Zone2 Hysteresis register, but for Zone3.
3-0	**Reserved.**

8.5.71 Zone1 Auto Speed Range and FANPWM1 Frequency

Location: 5Fh

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**RANGE**				**FREQ**			
Reset	1	1	0	0	0	1	0	0

8.0 Health Management (HM) (Continued)

Bit	Description
7-4	**Range.** Sets temperature range over which the associated FANPWM duty cycle is changed linearly as a function of temperature. The lower temperature limit of this range is determined, according to the Min/Off bit in the associated Min/Off, Spike Smoothing register, either by the associated Zone Temperature Limit (see Section 8.5.63 on page 181) whose the duty cycle is 0 or by the value in the associated FANPWM Minimum Duty. The upper temperature limit of this range is “Zone Temperature Limit” + Range. At this limit, the duty cycle is the value contained in the FANPWM1 MAX Duty register. The range is set according to Table 57.
3-0	**FREQ.** Sets FANPWM frequency selection according to Table 58.

8.0 Health Management (HM) (Continued)

Table 57. Range Configuration

Range	Temperature Range (°C)
'0000'	0
'0001'	2
'0010'	3
'0011'	4
'0100'	5
'0101'	7
'0110'	8
'0111'	10
'1000'	13
'1001'	16
'1010'	20
'1011'	27
'1100'	32 (default)
'1101'	40
'1110'	53
'1111'	80

Table 58. PWM Configuration

Frequency	PWM Frequency
'0000'	10 Hz
'0001'	15 Hz
'0010'	23 Hz
'0011'	30 Hz
'0100'	38 Hz (default)
'0101'	47 Hz
'0110'	62 Hz
'0111'	94 Hz
'1000'	23.5 KHz
'1001'	
'1010'	
'1011'	26.8 KHz
'1100'	
'1101'	31.2 KHz
'1110'	37.5 KHz
'1111'	47 KHz

8.5.72 Zone2 Auto Speed Range and FANPWM2 Frequency

Location: 60h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**RANGE**				**FREQ**			
Reset	1	1	0	0	0	1	0	0

Bit	Description
7-4	**Range.** Same as Range in Zone1 Auto Speed Range and FANPWM2 Frequency register, but for Zone2.
3-0	**FREQ.** Sets FANPWM frequency selection according to Table 58 on page 185.

8.5.73 Zone3 Auto Speed Range and FANPWM3 Frequency

Location: 61h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**RANGE**				**FREQ**			
Reset	1	1	0	0	0	1	0	0

Bit	Description
7-4	**Range.** Same as Range in Zone1 Auto Speed Range and FANPWM2 Frequency register, but for Zone3.
3-0	**FREQ.** Sets FANPWM frequency selection according to Table 58 on page 185.

8.0 Health Management (HM) (Continued)

8.5.74 Min/Off, Spike Smoothing 1

Location: 62h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**MIN_EN3**	**MIN_EN2**	**MIN_EN1**	**Reserved**	**FILT1_EN**	**TEMP_FILT1**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**MIN_EN3.** Enables using Minimum PWM Duty Cycle 3 (see Section 8.5.81 on page 189) for FANPWM3 when the measured temperature falls below the Zone ‘n’ Temperature Limit register. 0: FANPWM duty cycle at 0% when the temperature is below limit (default) 1: FANPWM duty cycle at Minimum PWM Duty Cycle when the temperature is below limit
6	**MIN_EN2.** Enables using Minimum PWM Duty Cycle 2 (see Section 8.5.80 on page 189) for FANPWM2 when the measured temperature falls below the Zone ‘n’ Temperature Limit register. 0: FANPWM duty cycle at 0% when the temperature is below limit (default) 1: FANPWM duty cycle at Minimum PWM Duty Cycle when the temperature is below limit
5	**MIN_EN1.** Enables using Minimum PWM Duty Cycle 1 (see Section 8.5.79 on page 189) for FANPWM1 when the measured temperature falls below the Zone ‘n’ Temperature Limit register. 0: FANPWM duty cycle at 0% when the temperature is below limit (default) 1: FANPWM duty cycle at Minimum PWM Duty Cycle when the temperature is below limit
4	**Reserved.**
3	**FILT1_EN.** Enable temperature filtering for Zone1.
2-0	**TEMP_FILT1.** Sets temperature low-pass filtering for temperature input to FANPWM1 Duty Cycle generator according to Table 59 on page 186. Filter rise time is from 0% to 95% of the input temperature change. This field may be changed only when the START bit in Configuration register is set to 0.

Table 59. Temperature Filtering Configuration

TEMP_FILT	Rise Time [sec]
‘000’	24.4(default)
‘001’	13.8
‘010’	8.4
‘011’	6.4
‘100’	3.6
‘101’	1.4
‘110’	1.0
‘111’	0.62

8.5.75 Min/Off, Spike Smoothing 2

Location: 63h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**FILT2_EN**	**TEMP_FILT2**			**FILT3_EN**	**TEMP_FILT3**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**FILT2_EN.** Enable temperature filtering for Zone2.

8.0 Health Management (HM) (Continued)

Bit	Description
6-4	**TEMP_FILT2.** Sets temperature low-pass filtering for temperature input to FANPWM2 Duty Cycle generator according to Table 59. Filter rise time is from 0% to 95% of the input temperature change. This field may be changed only when the START bit in Configuration register is set to 0.
3	**FILT3_EN.** Enable temperature filtering for Zone3.
2-0	**TEMP_FILT3.** Sets temperature low-pass filtering for temperature input to FANPWM3 Duty Cycle generator according to Table 59. Filter rise time is from 0% to 95% of the input temperature change. This field may be changed only when the START bit in Configuration register is set to 0.

8.5.76 FANPWM1 Control Configuration

Location: 5Ch

Type: Varies per bit (The R/W bits become read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**MODE**			**INV**	**SPIN**			
Reset	0	1	1	0	0	0	1	0

Bit	Type	Description
7-5	R/W or RO	**MODE.** Sets fan operation mode and temperature zone association according to Table 60. In Auto Mode the FANPWM duty cycle is controlled by the temperature data supplied by the associated Zone or by the hottest of the associated Zones. In Manual Mode the FANPWM is controlled by the contents of the associated PWM Current Duty Register.
4	WO	**INV (FANPWM1 Output Invert).** Sets polarity of FANPWM1 output signal. The value of INV is reflected by the respective (read-only) FANOUTn_INV bit in the HMCFG1 register (see Section 3.15.3 on page 79). INV bit is write-only; reading it returns an unpredictable value. 0: Normal signal - 100% duty cycle represents a high-level signal (default) 1: Inverted signal - 100% duty cycle represents a low-level signal
3-0	R/W or RO	**SPIN.** Sets maximum spin-up time according to Table 61. During spin-up, the FANPWM duty cycle is the value contained in the associated FANPWMn MAX Duty register.

Table 60. Fan Operating Mode Configuration

MODE	Meaning
'000'	FANPWM on Zone1 auto
'001'	FANPWM on Zone2 auto
'010'	FANPWM on Zone3 auto
'011'	FANPWM always on full (default)
'100'	FANPWM disabled
'101'	FANPWM controlled by hottest of zones 2,3
'110'	FANPWM controlled by hottest of zones 1,2,3
'111'	FANPWM manually controlled

8.0 Health Management (HM) (Continued)

Table 61. Spin-Up Configuration

SPIN	Spin-Up Time
'0000'	0
'0001'	91 ms
'0010'	182 ms (default)
'0011'	364 ms
'0100'	728 ms
'0101'	1.45 s
'0110'	2.91 s
'0111'	5.82 s
'1000'	11.65 s
'1001'	23.3 s
Others	Reserved

8.5.77 FANPWM2 Control Configuration

Location: 5Dh

Type: Varies per bit (The R/W bits become read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**MODE**			**INV**	**SPIN**			
Reset	0	1	1	0	0	0	1	0

Bit	Type	Description
7-5	R/W or RO	**MODE.** Same as MODE in FANPWM1 Control Configuration register, but for FANPWM2.
4	WO	**INV (FANPWM2 Output Invert).** Same as INV in FANPWM1 Control Configuration register, but for FANPWM2.
3-0	R/W or RO	**SPIN.** Same as SPIN in FANPWM1 Control Configuration register, but for FANPWM2.

8.5.78 FANPWM3 Control Configuration

Location: 5Eh

Type: Varies per bit (The R/W bits become read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**MODE**			**INV**	**SPIN**			
Reset	0	1	1	0	0	0	1	0

Bit	Type	Description
7-5	R/W or RO	**MODE.** Same as MODE in FANPWM1 Control Configuration register, but for FANPWM3.
4	WO	**INV (FANPWM3 Output Invert).** Same as INV in FANPWM1 Control Configuration register, but for FANPWM3.
3-0	R/W or RO	**SPIN.** Same as SPIN in FANPWM1 Control Configuration register, but for FANPWM3.

8.0 Health Management (HM) (Continued)

8.5.79 FANPWM1 Minimum

Location: 64h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**PWM_MIN**							
Reset	1	0	0	0	0	0	0	0

Bit	Description
7-0	**PWM_MIN.** Holds the value of the minimum duty cycle of the FANPWM signal. This value is used to generate the FANPWM output in Automatic mode if the zone temperature is lower than the low limit set in the associated Zone Temperature Limit register and the associated MIN_EN bit in the associated Min/Off, Spike Smoothing register is set to 1. The default is 80h=50% duty cycle.

8.5.80 FANPWM2 Minimum

Location: 65h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**PWM_MIN**							
Reset	1	0	0	0	0	0	0	0

Bit	Description
7-0	**PWM_MIN.** Same as PWM_MIN in FANPWM1 Minimum register, but for FANPWM2.

8.5.81 FANPWM3 Minimum

Location: 66h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**PWM_MIN**							
Reset	1	0	0	0	0	0	0	0

Bit	Description
7-0	**PWM_MIN.** Same as PWM_MIN in FANPWM1 Minimum register, but for FANPWM3.

8.5.82 FANPWM1 Maximum Duty

FANPWM1 maximum duty cycle.

Location: 70h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**MAX_PWM**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**MAX_PWM.** Holds the maximum allowed duty-cycle for the associated FANPWM signal. It affects all modes except manual mode (in manual mode, the maximum allowed duty-cycle is always 100%). A value of 01h represents 0.4% duty cycle, a value of FFh represents 100% duty cycle. The value 00h is reserved. The default is 100% duty-cycle. **Note:** After START bit in the Configuration register is set, changes to this register take effect only when the FANPWM1 duty cycle is updated.

8.0 Health Management (HM) (Continued)

8.5.83 FANPWM2 Maximum Duty

FANPWM2 maximum duty cycle.

Location: 71h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**MAX_PWM**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**MAX_PWM.** Same as MAX_PWM of FANPWM1 Maximum Duty register, but for FANPWM2.

8.5.84 FANPWM3 Maximum Duty

FANPWM3 maximum duty cycle.

Location: 72h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**MAX_PWM**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**MAX_PWM.** Same as MAX_PWM of FANPWM1 Maximum Duty register, but for FANPWM3.

8.5.85 Extended FANPWM Control 1

Location: 76h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**FSTLMD**	**SPIN_END**	**SPIN_DUTY**	**STEP_LEN**			
Reset	0	0	1	0	0	0	0	0

Bit	Description
7	**Reserved.**
6	**FSTLMD (FAN_STALL Mode).** Selects the fan conditions causing the detection of a fan failure, which sets both the FANn_STALL status bit in the Status Register 2 (see Section 8.5.24 on page 165), and the FANn_STS bit in the HM Sensor Status Register 2 (see Section 8.4.9 on page 148) to 1. 0: Either a fan stalled condition or a low speed condition, whichever occurs first (default) 1: A fan stalled condition only

8.0 Health Management (HM) (Continued)

Bit	Description
5	**SPIN_END (Spin-Up End Select).** Selects the condition used by the HM to end the spin-up process. When the condition is met, the spin-up process ends and the FANPWM duty cycle is set to one of the following values: • The value set in FANPWMn Current Duty register, in Manual Fan Control mode • The value generated from the current normalized temperature by the automatic algorithm, in Automatic Fan Control mode (this value is updated in the FANPWMn Current Duty register) • The value set in FANPWMn MAX Duty register, in Continuously On mode The conditions are: 0: Whichever occurs first: either the spin-up time (set in SPIN field in the FANPWMn Control Configuration register) has ended or the current fan speed is equal to or higher than either the minimum value of all the associated Fan Tachometer 'n' Low Limit (LSB and MSB) registers. 1: Spin-up time has ended (default).
4	**SPIN_DUTY.** Determines the value shown in the FANPWM1-3 Current Duty registers (see Section 8.5.17 on page 161 to Section 8.5.19) during spin-up. 0: FANPWMn Current Duty registers show 0 during spin-up (default) 1: FANPWMn Current Duty registers show the target duty cycle during spin-up
3-0	**STEP_LEN.** The step length used for soft speed-change of the FANPWM duty-cycle (the steps performed above the minimum duty cycle value). 00h: Reserved 01h - 0Fh: The duration of a "soft" step equals the STEP_LEN value, multiplied by 22.75 ms (default is 08h=182 ms)

8.5.86 Extended FANPWM Control 2

Location: 77h

Type: R/W or RO (Becomes read-only when LOCK bit in the Configuration register is set.)

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**SPD_CHG3**	**SPD_CHG2**	**SPD_CHG1**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved.**
2	**SPD_CHG3.** Sets the speed-change mode for FANPWM3 output for all fan control modes. 0: Hard speed change - the speed change is done in one single and immediate step (default) 1: Soft speed change - speed change is done in steps of 3.125% duty-cycle **Note:** Speed change between a duty-cycle of 0% and the minimum duty-cycle (which is defined in the FANPWM3 Minimum register) is done in one immediate step.
1	**SPD_CHG2.** Same as SPD_CHG3 for FANPWM2.
0	**SPD_CHG1.** Same as SPD_CHG3 for FANPWM1.

9.0 Legacy Functional Blocks

This chapter briefly describes the following blocks, which provide legacy device functions:

- Floppy Disk Controller (FDC)
- Parallel Port (PP)
- Serial Port1 and 2 (SP1 and SP2)
- Keyboard and Mouse Controller (KBC)

For details on the general implementation of each legacy block, see the *SuperI/O Legacy Functional Blocks* Datasheet.

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write.
- R = Read from register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read-only.
- WO = Write-only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

9.1 FLOPPY DISK CONTROLLER (FDC)

9.1.1 General Description

The generic FDC is a standard FDC with a digital data separator; it is software compatible with the µDP8473 and N82077. The PC8374L FDC supports 14 of the 17 standard FDC signals described in the generic Floppy Disk Controller (FDC) chapter, including:

- FDC supports FM and MFM modes. To select either mode, set bit 6 of the first command byte when writing to/reading from a diskette, where:
  - 0 = FM mode
  - 1 = MFM mode
- A logic 1 is returned during LPC I/O read cycles by all register bits, reflecting the state of floating (TRI-STATE) FDC pins.

Exceptions to standard FDC are:

- Automatic media sense using MSEN0 and MSEN1 signals is not supported.
- DRATE1 is not supported.
- $\overline{\text{DR1}}$ is not supported.
- $\overline{\text{MTR1}}$ is not supported.

9.0 Legacy Functional Blocks (Continued)

Table 62 lists the FDC functional block registers. All registers are V_{DD3} powered.

Table 62. FDC Register Map

Offset[1]	Mnemonic	Register Name	Type
00h	SRA	Status A	RO
01h	SRB	Status B	RO
02h	DOR	Digital Output	R/W
03h	TDR	Tape Drive	R/W
04h	MSR	Main Status	R
	DSR	Data Rate Select	W
05h	FIFO	Data (FIFO)	R/W
06h		N/A	X
07h	DIR	Digital Input	R
	CCR	Configuration Control	W

1. From the 8-byte aligned FDC base address.

9.1.2 FDC Bitmap Summary

The FDC supports two system operation modes: PC-AT mode and PS/2 mode. Unless specifically indicated otherwise, all fields in all registers are valid in both operation modes.

Table 63. FDC Bitmap Summary

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	SRA[1]	IRQ Pending	Reserved	Step	$\overline{\text{TRK0}}$	Head Select	$\overline{\text{INDEX}}$	$\overline{\text{WP}}$	Head Direction
01h	SRB[1]	Reserved		Drive Select 0 Status	$\overline{\text{WDATA}}$	$\overline{\text{RDATA}}$	$\overline{\text{WGATE}}$	$\overline{\text{MTR1}}$	$\overline{\text{MTR0}}$
02h	DOR	Reserved		Motor Enable 1	Motor Enable 0	DMAEN	Reset Controller	Drive Select	
03h	TDR	Reserved						Tape Drive Select 1,0	
	TDR[2]	Reserved (must be 1111)				Logical Drive Exchange		Tape Drive Select 1,0	
04h	MSR	RQM	Data I/O Direction	Non-DMA Execution	Command in Progress	Reserved		Drive 1 Busy	Drive 0 Busy
	DSR	Software Reset	Low Power	Reserved	Precompensation Delay Select			Data Transfer Rate Select	
05h	FIFO	Data Bits							
07h	DIR[3]	$\overline{\text{DSKCHG}}$	Reserved						
	DIR[1]	$\overline{\text{DSKCHG}}$	Reserved				DRATE 1,0 Status		High Density
07h	CCR	Reserved						DRATE1,0	

1. Applicable only in PS/2 Mode.
2. Applicable only in Enhanced TDR Mode.
3. Applicable only in PC-AT Compatible Mode.

9.0 Legacy Functional Blocks (Continued)

9.2 PARALLEL PORT

9.2.1 General Description

The Parallel Port supports all IEEE1284 standard communication modes:

- Compatibility (known also as Standard or SPP)
- Bi-directional (known also as PS/2)
- FIFO
- EPP (known also as Mode 4)
- ECP (with an optional Extended ECP mode)

9.2.2 Parallel Port Register Map

The Parallel Port includes two groups of runtime registers, as follows:

- A group of 21 registers at first level offset, sharing 14 entries. Three of these registers (at offsets 403h, 404h and 405h) are used only in Extended ECP mode.
- A group of four registers, used only in Extended ECP mode, accessed by a second level offset.

EPP and second level offset registers are available only when the base address is 8-byte aligned.

The desired mode is selected by the ECR runtime register (offset 402h). The selected mode determines which runtime registers and which address bits are used for the base address. See Tables 64 and 65 for a listing of all registers, their offset addresses and the associated modes. All registers are V_{DD3} powered.

Table 64. Parallel Port Registers at First Level Offset

Offset	Mnemonic	Mode(s)	Register Name	Type
00h	DATAR	0,1	Data	R/W
	AFIFO	3	ECP FIFO (Address)	W
	DTR	4	Data (for EPP)	R/W
01h	DSR	All, except 4	Status	RO
	STR	4	Status (for EPP)	RO
02h	DCR	All, except 4	Control	R/W
	CTR	4	Control (for EPP)	R/W
03h	ADDR	4	EPP Address	R/W
04h	DATA0	4	EPP Data Port 0	R/W
05h	DATA1	4	EPP Data Port 1	R/W
06h	DATA2	4	EPP Data Port 2	R/W
07h	DATA3	4	EPP Data Port 3	R/W
400h	CFIFO DFIFO TFIFO CNFGA	2 3 6 7	PP Data FIFO ECP Data FIFO Test FIFO Configuration A	W R/W R/W RO
401h	CNFGB	7	Configuration B	RO
402h	ECR	All	Extended Control	R/W
403h	EIR[1]	0,1,2,3	Extended Index	R/W
404h	EDR[1]	0,1,2,3	Extended Data	R/W
405h	EAR[1]	0,1,2,3	Extended Auxiliary Status	R/W

1. These registers are extended to the standard IEEE1284 registers. They are only accessible when enabled by bit 4 of the Parallel Port Configuration register (see Section 3.9.3 on page 64).

9.0 Legacy Functional Blocks (Continued)

Table 65. Parallel Port Registers at Second Level Offset

Offset	Mnemonic	Register Name	Type
00h	Control0	Extended Control 0	R/W
02h	Control2	Extended Control 1	R/W
04h	Control4	Extended Control 4	R/W
05h	PP Confg0	Configuration 0	R/W

9.2.3 Parallel Port Bitmap Summary

The Parallel Port functional block bitmaps are grouped according to first and second level offsets.

Table 66. Parallel Port Bitmap Summary for First Level Offset

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
000h	DATAR	Data Bits							
	AFIFO	Address Bits							
001h	DSR	Printer Status	$\overline{\text{ACK}}$ Status	PE Status	SLCT Status	$\overline{\text{ERR}}$ Status	Reserved		EPP Time-Out Status
002h	DCR	Reserved		Direction Control	Interrupt Enable	PP Input Control	Printer Initialization Control	Automatic Line Feed Control	Data Strobe Control
003h	ADDR	EPP Device or Register Selection Address Bits							
004h	DATA0	EPP Device or R/W Data							
005h	DATA1	EPP Device or R/W Data							
006h	DATA2	EPP Device or R/W Data							
007h	DATA3	EPP Device or R/W Data							
400h	CFIFO	Data Bits							
400h	DFIFO	Data Bits							
400h	TFIFO	Data Bits							
400h	CNFGA	Reserved				Bit 7 of PP Confg0	Reserved		
401h	CNFGB	Reserved	Interrupt Request Value	Interrupt Select			Reserved	DMA Channel Select	
402h	ECR	ECP Mode Control			ECP Interrupt Mask	ECP DMA Enable	ECP Interrupt Service	FIFO Full	FIFO Empty
403h	EIR	Reserved					Second Level Offset		
404h	EDR	Data Bits							
405h	EAR	FIFO Tag	Reserved						

9.0 Legacy Functional Blocks (Continued)

Table 67. Parallel Port Bitmap Summary for Second Level Offset

Register		Bits							
Second Level Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	Control0	Reserved		DCR Register Live	Freeze Bit	Reserved			EPP Time-Out Interrupt Mask
02h	Control2	SPP Compatibility	Channel Address Enable	Reserved	Revision 1.7 or 1.9 Select	Reserved			
04h	Control4	Reserved	PP DMA Request Inactive Time			Reserved	PP DMA Request Active Time		
05h	PP Confg0	Bit 3 of CNFGA	Demand DMA Enable	ECP IRQ Channel Number			PE Internal Pull-Up or Pull-Down	ECP DMA Channel Number	

9.3 SERIAL PORT 1 (SP1)

9.3.1 General Description

The Serial Port functional block supports serial data communication with a remote peripheral device or modem using a wired interface. The Serial Port can function in one of three modes:

- 16450-Compatible mode (Standard 16450)
- 16550-Compatible mode (Standard 16550)
- Extended mode

Extended mode provides advanced functionality for the UART.

The Serial Port provides receive and transmit channels that can operate concurrently in full-duplex mode. It performs all functions required to conduct parallel data interchange with the system and composite serial data exchange with the external data channel, including:

- Format conversion between the internal parallel data format and the external programmable composite serial format
- Serial data timing generation and recognition
- Parallel data interchange with the system using a choice of bidirectional data transfer mechanisms
- Status monitoring for all phases of communication activity
- Complete MODEM-control capability.

Existing 16550-based legacy software is completely and transparently supported. Module organization and specific fallback mechanisms switch the module to 16550-Compatible mode on reset or when initialized by 16550 software.

9.3.2 Register Bank Overview

Four register banks, each containing eight registers, control Serial Port operation. All registers use the same 8-byte address space to indicate offsets 00h through 07h. The active bank must be selected by the software.

The register bank organization enables access to the banks as required for activation of all module modes, while maintaining transparent compatibility with 16450 or 16550 software.

The Bank Selection register (BSR) selects the active bank and is common to all banks as shown in Figure 38. Therefore, each bank defines seven new registers.

The default bank selection after system reset is 0.

9.0 Legacy Functional Blocks (Continued)

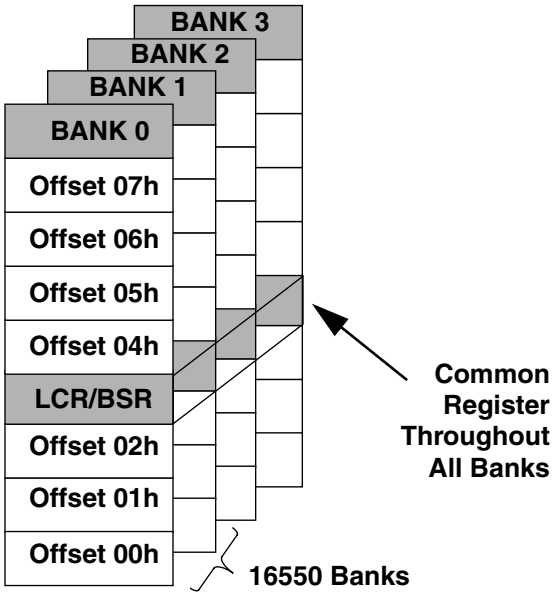


Figure 38. Register Bank Architecture

9.3.3 SP1 Register Maps

Table 68. Bank 0 Register Map

Offset	Mnemonic	Register Name	Type
00h	RXD	Receiver Data	RO
	TXD	Transmitter Data	W
01h	IER	Interrupt Enable	R/W
02h	EIR	Event Identification	R
	FCR	FIFO Control	W
03h	LCR	Link Control	W
	BSR	Bank Select	R/W
04h	MCR	Modem/Mode Control	R/W
05h	LSR	Link Status	R/W
06h	MSR	Modem Status	R
07h	SPR	Scratch Pad	R/W
	ASCR	Auxiliary Status and Control	RO

9.0 Legacy Functional Blocks (Continued)

Table 69. Bank 1 Register Map

Offset	Mnemonic	Register Name	Type
00h	LBGD(L)	Legacy Baud Generator Divisor (Low Byte)	R/W
01h	LBGD(H)	Legacy Baud Generator Divisor (High Byte)	R/W
02h		Reserved	
03h	LCR/BSR	Link Control/ Bank Select	R/W
04h-07h		Reserved	

Table 70. Bank 2 Register Map

Offset	Mnemonic	Register Name	Type
00h	BGD(L)	Baud Generator Divisor (Low Byte)	R/W
01h	BGD(H)	Baud Generator Divisor (High Byte)	R/W
02h	EXCR1	Extended Control 1	R/W
03h	BSR	Bank Select	R/W
04h	EXCR2	Extended Control 2	R/W
05h		Reserved	
06h	TXFLV	TX_FIFO Level	RO
07h	RXFLV	RX_FIFO Level	RO

Table 71. Bank 3 Register Map

Offset	Mnemonic	Register Name	Type
00h	MRID	Module Identification and Revision ID	RO
01h	SH_LCR	Shadow of LCR	RO
02h	SH_FCR	Shadow of FIFO Control	RO
03h	BSR	Bank Select	R/W
04h-07h		Reserved	

9.0 Legacy Functional Blocks (Continued)

9.3.4 SP1 Bitmap Summary

Table 72. Bank 0 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	RXD	RXD7-0							
00h	TXD	TXD7-0							
01h	IER[1]	Reserved				MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
	IER[2]	Reserved		TXEMP_IE	Reserved	MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
02h	EIR[1]	FEN1-0		Reserved		RXFT	IPR1-0		IPF
	EIR[2]	Reserved		TXEMP_EV	Reserved	MS_EV	LS_EV	TXLDL_EV	RXHDL_EV
	FCR[1]	RXFTH1-0		Reserved			TXSR	RXSR	FIFO_EN
	FCR[2]	RXFTH1-0		TXFTH1-0		Reserved	TXSR	RXSR	FIFO_EN
03h	LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
	BSR	BKSE	BSR6-0						
04h	MCR[1]	Reserved			LOOP	ISEN/ DCDLP	RILP	RTS	DTR
	MCR[2]	Reserved				TX_DFR	Reserved	RTS	DTR
05h	LSR	ER_INF	TXEMP	TXRDY	BRK	FE	PE	OE	RXDA
06h	MSR	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
07h	SPR[1]	Scratch Data							
	ASCR[2]	Reserved							RXF_TOUT

1. Non-Extended mode.
2. Extended mode.

Table 73. Bank 1 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	LBGD(L)	LBGD7-0							
01h	LBGD(H)	LBGD15-8							
02h		Reserved							
03h	LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
	BSR	BKSE	BSR6-0						
04h-07h		Reserved							

9.0 Legacy Functional Blocks (Continued)

Table 74. Bank 2 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	BGD(L)	BGD7-0							
01h	BGD(H)	BGD15-8							
02h	EXCR1	BTEST	Reserved	ETDLBK	LOOP	Reserved			EXT_SL
03h	BSR	BKSE	BSR6-0						
04h	EXCR2	LOCK	Reserved	PRESL1-0		Reserved			
05h		Reserved							
06h	TXFLV	Reserved			TFL4-0				
07h	RXFLV	Reserved			RFL4-0				

Table 75. Bank 3 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	MRID	MID3-0				RID3-0			
01h	SH_LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
02h	SH_FCR	RXFTH1-0		TXFTH1-0		Reserved	TXSR	RXSR	FIFO_EN
03h	BSR	BKSE	BSR6-0						
04-07h		Reserved							

9.4 SERIAL PORT 2 (SP2)

9.4.1 General Description

This functional block provides advanced, versatile serial communications features with IR capabilities. It supports four modes of operation: UART, Sharp-IR, IrDA 1.0 SIR (hereafter SIR), and Consumer Electronic IR (also called TV Remote or Consumer remote control, hereafter CEIR). In UART mode, the Serial Port can function in 16450-Compatible mode, 16550-Compatible mode, or Extended mode. This chapter describes general implementation of the Enhanced Serial Port with Fast IR. For device specific implementation, see *Device Architecture and Configuration* in the datasheet of the relevant device.

Existing 16550-based legacy software is completely and transparently supported. Organization and specific fallback mechanisms switch the Serial Port to 16550-Compatible mode on reset, or when initialized by 16550 software.

The Serial Port has two DMA channels; the device can use either one or both of them. One channel is required for IR based applications, since IR communication works in half duplex fashion. Two channels would normally be needed to handle high-speed, full duplex, UART based applications.

9.4.2 Register Bank Overview

Eight register banks, each containing eight registers, control Serial Port operation. All registers use the same 8-byte address space to indicate offsets 00h-07h. The active bank must be selected by the software.

The register bank organization enables access to the banks as required for activation of all module modes, while maintaining transparent compatibility with 16450 or 16550 software.

The Bank Selection register (BSR) selects the active bank and is common to all banks. See Figure 39. Therefore, each bank defines seven new registers.

The default bank selection after system reset is 0.

9.0 Legacy Functional Blocks (Continued)

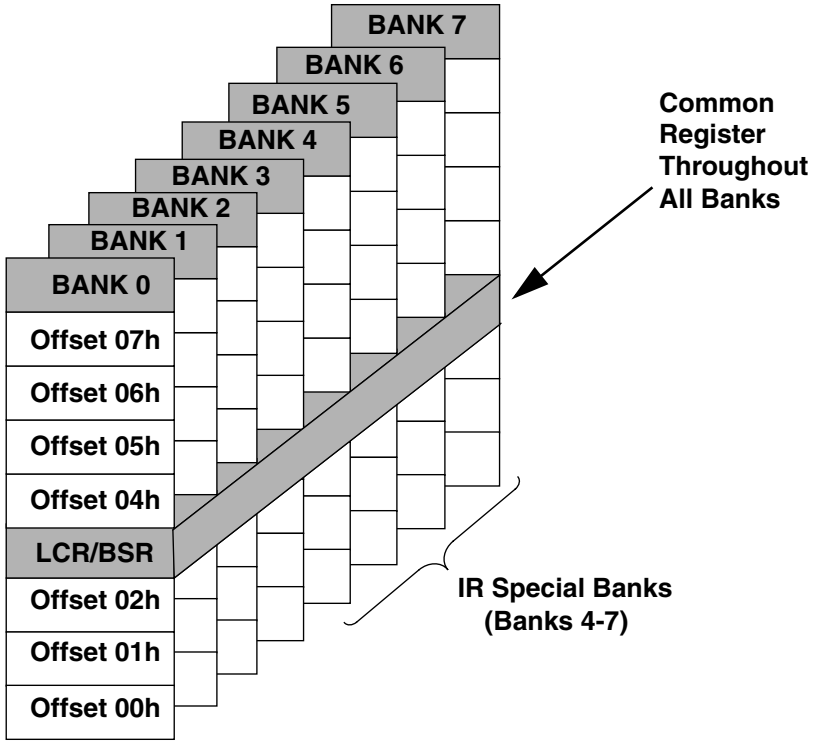


Figure 39. SP2 Register Bank Architecture

Table 76 shows the main functions of the registers in each bank. Banks 0-3 control both UART and IR modes of operation; banks 4-7 control and configure the IR modes only.

Table 76. Register Bank Summary

Bank	UART Mode	IR Mode	Main Functions
0	✓	✓	Global Control and Status
1	✓	✓	Legacy Bank
2	✓	✓	Alternative Baud Generator Divisor, Extended Control and Status
3	✓	✓	Module Revision ID and Shadow registers
4		✓	IR mode setup
5		✓	IR Control
6		✓	IR Physical Layer Configuration
7		✓	CEIR and Optical Transceiver Configuration

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read-Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

9.0 Legacy Functional Blocks (Continued)

9.4.3 SP2 Register Map

Table 77. Bank 0 Register Map

Offset	Mnemonic	Register Name	Type
00h	RXD	Receiver Data	RO
	TXD	Transmitter Data	W
01h	IER	Interrupt Enable	R/W
02h	EIR	Event Identification	R
	FCR	FIFO Control	W
03h	LCR	Link Control	W
	BSR	Bank Select	R/W
04h	MCR	Modem/Mode Control	R/W
05h	LSR	Link Status	R/W
06h	MSR	Modem Status	R
07h	SPR	Scratch Pad	R/W
	ASCR	Auxiliary Status and Control	Varies per bit

Table 78. Bank 1 Register Map

Offset	Mnemonic	Register Name	Type
00h	LBGD(L)	Legacy Baud Generator Divisor (Low Byte)	R/W
01h	LBGD(H)	Legacy Baud Generator Divisor (High Byte)	R/W
02h		Reserved	
03h	LCR/BSR	Link Control/Bank Select	R/W
04h - 07h		Reserved	

Table 79. Bank 2 Register Map

Offset	Mnemonic	Register Name	Type
00h	BGD(L)	Baud Generator Divisor (Low Byte)	R/W
01h	BGD(H)	Baud Generator Divisor (High Byte)	R/W
02h	EXCR1	Extended Control1	R/W
03h	BSR	Bank Select	R/W
04h	EXCR2	Extended Control 2	R/W
05h		Reserved	
06h	TXFLV	TX_FIFO Level	RO
07h	RXFLV	RX_FIFO Level	RO

9.0 Legacy Functional Blocks (Continued)

Table 80. Bank 3 Register Map

Offset	Mnemonic	Register Name	Type
00h	MRID	Module Identification and Revision ID	RO
01h	SH_LCR	Shadow of LCR	RO
02h	SH_FCR	Shadow of FIFO Control	RO
03h	BSR	Bank Select	R/W
04h-07h		Reserved	

Table 81. Bank 4 Register Map

Offset	Mnemonic	Register Name	Type
00-01h		Reserved	
02h	IRCR1	IR Control 1	R/W
03h	BSR	Bank Select	R/W
04-07h		Reserved	

Table 82. Bank 5 Register Map

Offset	Mnemonic	Register Name	Type
00h-02h		Reserved	
03h	BSR	Bank Select	R/W
04h	IRCR2	IR Control 2	R/W
05h-07h		Reserved	

Table 83. Bank 6 Register Map

Offset	Mnemonic	Register Name	Type
00h	IRCR3	IR Control 3	R/W
01h		Reserved	
02h	SIR_PW	SIR Pulse Width Control	R/W
03h	BSR	Bank Select	R/W
04-07h		Reserved	

Table 84. Bank 7 Register Map

Offset	Mnemonic	Register Name	Type
00h	IRRXDC	IR Receiver Demodulator Control	R/W
01h	IRTXMC	IR Transmitter Modulator Control	R/W
02h	RCCFG	CEIR Configuration	R/W
03h	BSR	Bank Select	R/W
04h	IRCFG1	IR Interface Configuration 1	R/W
05h-06h		Reserved	
07h	IRCFG4	IR Interface Configuration 4	R/W

9.0 Legacy Functional Blocks (Continued)

9.4.4 SP2 Bitmap Summary

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Table 85. Bank 0 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	RXD	RXD7-0							
00h	TXD	TXD7-0							
01h	IER[1]	Reserved				MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
	IER[2]	Reserved		TXEMP_IE	DMA_IE	MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
02h	EIR[1]	FEN1-0		Reserved		RXFT	IPR1-0		IPF
	EIR[2]	Reserved		TXEMP_EV	DMA_EV	MS_EV	LS_EV/ TXHLT_EV	TXLDL_EV	RXHDL_EV
	FCR[1]	RXFTH1-0		Reserved			TXSR	RXSR	FIFO_EN
	FCR[2]	RXFTH1-0		TXFTH1-0		Reserved	TXSR	RXSR	FIFO_EN
03h	LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
	BSR	BKSE	BSR6-0						
04h	MCR[1]	Reserved			LOOP	ISEN/ DCDLP	RILP	RTS	DTR
	MCR[2]	MDSL2-0			Reserved	TX_DFR	DMA_EN	RTS	DTR
05h	LSR	ER_INF	TXEMP	TXRDY	BRK	FE	PE	OE	RXDA
06h	MSR	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
07h	SPR[1]	Scratch Data							
	ASCR[2]	Reserved	TXUR	RXACT	RXWDG	Reserved	S_EOT	Reserved	RXF_TOUT

1. Non-Extended mode.
2. Extended mode.

Table 86. Bank 1 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	LBGD(L)	LBGD7-0							
01h	LBGD(H)	LBGD15-8							
02h		Reserved							
03h	LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
	BSR	BKSE	BSR6-0						
04-07h		Reserved							

9.0 Legacy Functional Blocks (Continued)

Table 87. Bank 2 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	BGD(L)	BGD7-0							
01h	BGD(H)	BGD15-8							
02h	EXCR1	BTEST	Reserved	ETDLBK	LOOP	DMASWP	DMATH	DMANF	EXT_SL
03h	BSR	BKSE	BSR6-0						
04h	EXCR2	LOCK	Reserved	PRESL1-0		Reserved			
05h		Reserved							
06h	TXFLV	Reserved			TFL4-0				
07h	RXFLV	Reserved			RFL4-0				

Table 88. Bank 3 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	MRID	MID3-0				RID3-0			
01h	SH_LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
02h	SH_FCR	RXFTH1-0		TXFTH1-0		Reserved	TXSR	RXSR	FIFO_EN
03h	BSR	BKSE	BSR6-0						
04-07h		Reserved							

Table 89. Bank 4 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h-01h		Reserved							
02h	IRCR1	Reserved				IR_SL1-0		Reserved	
03h	BSR	BKSE	BSR6-0						
04h-07h		Reserved							

Table 90. Bank 5 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00-02h	Reserved								
03h	BSR	BKSE	BSR6-0						
04h	IRCR2	Reserved			AUX_IRRX	Reserved		IRMSSL	IR_FDPLX
05-07h	Reserved								

9.0 Legacy Functional Blocks (Continued)

Table 91. Bank 6 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	IRCR3	SHDM_DS	SHDM_DS	Reserved					
01h		Reserved							
02h	SIR_PW	Reserved				SPW3-0			
03h	BSR	BKSE	BSR6-0						
04-07h		Reserved							

Table 92. Bank 7 Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	IRRXDC	DBW2-0			DFR4-0				
01h	IRTXMC	MCPW2-0			MCFR4-0				
02h	RCCFG	R_LEN	T_OV	RXHSC	RCDM_DS	Reserved	TXHSC	RC_MMD1-0	
03h	BSR	BKSE	BSR6-0						
04h	IRCFG1	STRV_MS	SIRC2-0			IRID3	IRIC2-0		
05h		Reserved							
06h		Reserved							
07h	IRCFG4	Reserved		IRSL0_DS	RXINV	IRSL12_DS	Reserved		

9.5 SERIAL PORT 2 (SP2) WITH INFRARED

9.5.1 General Description

This functional block (SP2) provides advanced, versatile serial communications features with IR capabilities. It supports four modes of operation: UART, Sharp-IR, IrDA 1.0 SIR (hereafter SIR) and Consumer Electronic IR (also called TV Remote or Consumer remote control, hereafter CEIR). In UART mode, the Serial Port can function in 16450-Compatible mode, 16550-Compatible mode, or Extended mode.

Existing 16550-based legacy software is completely and transparently supported. Organization and specific fallback mechanisms switch the Serial Port to 16550-Compatible mode on reset, or when initialized by 16550 software.

9.5.2 UART Register Bank Overview

Eight register banks, each containing eight registers, control Serial Port operation. All registers use the same 8-byte address space to indicate offsets 00h through 07h. The active bank must be selected by the software.

The register bank organization enables access to the banks as required for activation of all module modes, while maintaining transparent compatibility with 16450 or 16550 software.

The Bank Selection register (BSR) selects the active bank and is common to all banks. See Figure 40. Therefore, each bank defines seven new registers.

9.0 Legacy Functional Blocks (Continued)

The default bank selection after system reset is 0.

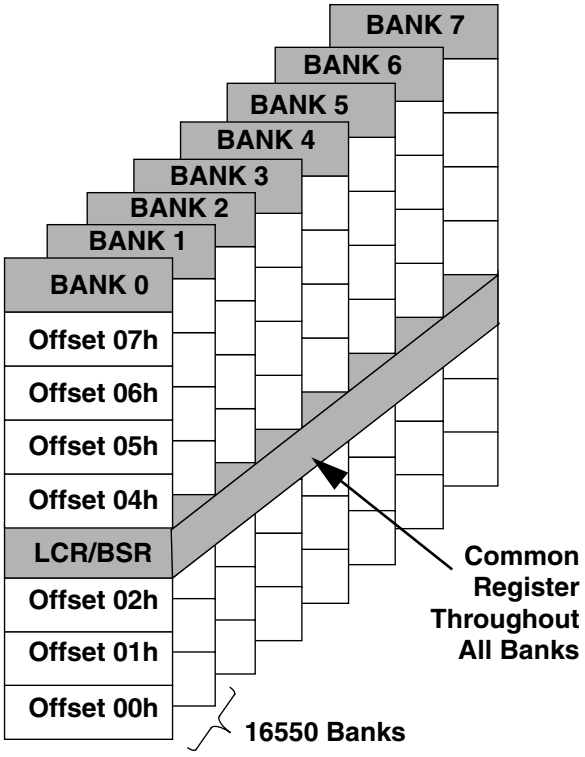


Figure 40. Register Bank Architecture

Table 93 shows the main functions of the registers in each bank. Banks 0-3 control both UART and IR modes of operation; banks 4-7 control and configure the IR modes only.

Table 93. Register Bank Summary

Bank	UART Mode	IR Mode	Main Functions
0	✓	✓	Global Control and Status
1	✓	✓	Legacy Bank
2	✓	✓	Alternative Baud Generator Divisor, Extended Control and Status
3	✓	✓	Module Revision ID and Shadow registers
4		✓	IR mode setup
5		✓	IR Control
6		✓	IR Physical Layer Configuration
7		✓	CEIR and Optical Transceiver Configuration

9.5.3 SP2 Register Map

All registers are V_{DD3} powered.

Table 94. Bank 0 Register Map

Offset	Mnemonic	Register Name	Type
00h	RXD	Receiver Data	RO
	TXD	Transmitter Data	W
01h	IER	Interrupt Enable	R/W

9.0 Legacy Functional Blocks (Continued)

Table 94. Bank 0 Register Map

Offset	Mnemonic	Register Name	Type
02h	EIR	Event Identification	R
	FCR	FIFO Control	W
03h	LCR	Link Control	W
	BSR	Bank Select	R/W
04h	MCR	Modem/Mode Control	R/W
05h	LSR	Link Status	R/W
06h	MSR	Modem Status	R
07h	SPR	Scratchpad	R/W
	ASCR	Auxiliary Status and Control	Varies per bit

Table 95. Bank Selection Encoding

BSR Bits								Bank Selected	LCR
7	6	5	4	3	2	1	0		
0	x	x	x	x	x	x	x	0	LCR Written
1	0	x	x	x	x	x	x	1	
1	1	x	x	x	x	1	x	1	
1	1	x	x	x	x	x	1	1	
1	1	1	0	0	0	0	0	2	LCR Not Written
1	1	1	0	0	1	0	0	3	
1	1	1	0	1	0	0	0	4	
1	1	1	0	1	1	0	0	5	
1	1	1	1	0	0	0	0	6	
1	1	1	1	0	1	0	0	7	
1	1	1	1	1	x	0	0	Reserved	
1	1	0	x	x	x	0	0	Reserved	

Table 96. Bank 1 Register Map

Offset	Mnemonic	Register Name	Type
00h	LBGD(L)	Legacy Baud Generator Divisor (Low Byte)	R/W
01h	LBGD(H)	Legacy Baud Generator Divisor (High Byte)	R/W
02h		Reserved	
03h	LCR/BSR	Link Control/Bank Select	R/W
04h - 07h		Reserved	

9.0 Legacy Functional Blocks (Continued)

Table 97. Bank 2 Register Map

Offset	Mnemonic	Register Name	Type
00h	BGD(L)	Baud Generator Divisor (Low Byte)	R/W
01h	BGD(H)	Baud Generator Divisor (High Byte)	R/W
02h	EXCR1	Extended Control1	R/W
03h	BSR	Bank Select	R/W
04h	EXCR2	Extended Control 2	R/W
05h		Reserved	
06h	TXFLV	TX_FIFO Level	RO
07h	RXFLV	RX_FIFO Level	RO

Table 98. Bank 3 Register Map

Offset	Mnemonic	Register Name	Type
00h	MRID	Module Identification and Revision ID	RO
01h	SH_LCR	Shadow of LCR	RO
02h	SH_FCR	Shadow of FIFO Control	RO
03h	BSR	Bank Select	R/W
04-07h		Reserved	

Table 99. Bank 4 Register Map

Offset	Mnemonic	Register Name	Type
00-01h		Reserved	
02h	**IRCR1**	IR Control 1	R/W
03h	**BSR**	Bank Select	R/W
04-07h		Reserved	

Table 100. Bank 5 Register Map

Offset	Mnemonic	Register Name	Type
00h-02h		Reserved	
03h	**BSR**	Bank Select	R/W
04h	**IRCR2**	IR Control 2	R/W
05h-07h		Reserved	

Table 101. Bank 6 Register Map

Offset	Mnemonic	Register Name	Type
00h	**IRCR3**	IR Control 3	R/W
01h		Reserved	

9.0 Legacy Functional Blocks (Continued)

Table 101. Bank 6 Register Map

Offset	Mnemonic	Register Name	Type
02h	**SIR_PW**	SIR Pulse Width Control	R/W
03h	**BSR**	Bank Select	R/W
04-07h		Reserved	

Table 102. Bank 7 Register Map

Offset	Mnemonic	Register Name	Type
00h	IRRXDC	IR Receiver Demodulator Control	R/W
01h	IRTXMC	IR Transmitter Modulator Control	R/W
02h	RCCFG	CEIR Configuration	R/W
03h	BSR	Bank Select	R/W
04h	IRCFG1	IR Interface Configuration 1	R/W
05h-06h		Reserved	
07h	IRCFG4	IR Interface Configuration 4	R/W

9.6 KEYBOARD AND MOUSE CONTROLLER (KBC)

9.6.1 General Description

The KBC is implemented physically as a single hardware module and houses two separate logical devices: a mouse controller (Logical Device 5) and a keyboard controller (Logical Device 6). The KBC is functionally equivalent to the industry standard 8042AH keyboard controller. The 8042AH datasheet can be used as a detailed technical reference for the KBC.

The hardware KBC module is integrated to provide the following pin functions: $\overline{\text{KBRST}}$ (P20), GA20 (P21), KBDAT, KBCLK, MDAT and MCLK. $\overline{\text{KBRST}}$ and GA20 are implemented as bi-directional open-drain pins with internal active pull-up. The keyboard and mouse interfaces are implemented as bi-directional open-drain pins. Their internal connections are shown in Figure 41.

Ports P10-P17 and P22-P27 of the KBC core are not available on dedicated pins; neither are T0 and T1. P10, P11, P22, P23, P26, P27, T0 and T1 are used to implement the keyboard and mouse interface.

The KBC executes a program fetched from an on-chip 2 Kbyte ROM. The code programmed in this ROM is user-customizable. The KBC has two interrupt request signals: one for the keyboard and one for the mouse. The interrupt requests are implemented using ports P24 and P25 of the KBC core. The interrupt requests are controlled exclusively by the KBC firmware, except for the IRQ type and number, which are set by configuration registers (see Section 3.2.3 on page 39).

The interrupt requests are implemented as bi-directional signals. When an I/O port is read, all unused bits return the value latched in the output registers of the ports.

For KBC firmware that implements interrupt-on-OBF schemes, the following is the recommended implementation:

1. Put the data in DBBOUT.
2. Set the appropriate port bit to issue an interrupt request.

9.0 Legacy Functional Blocks (Continued)

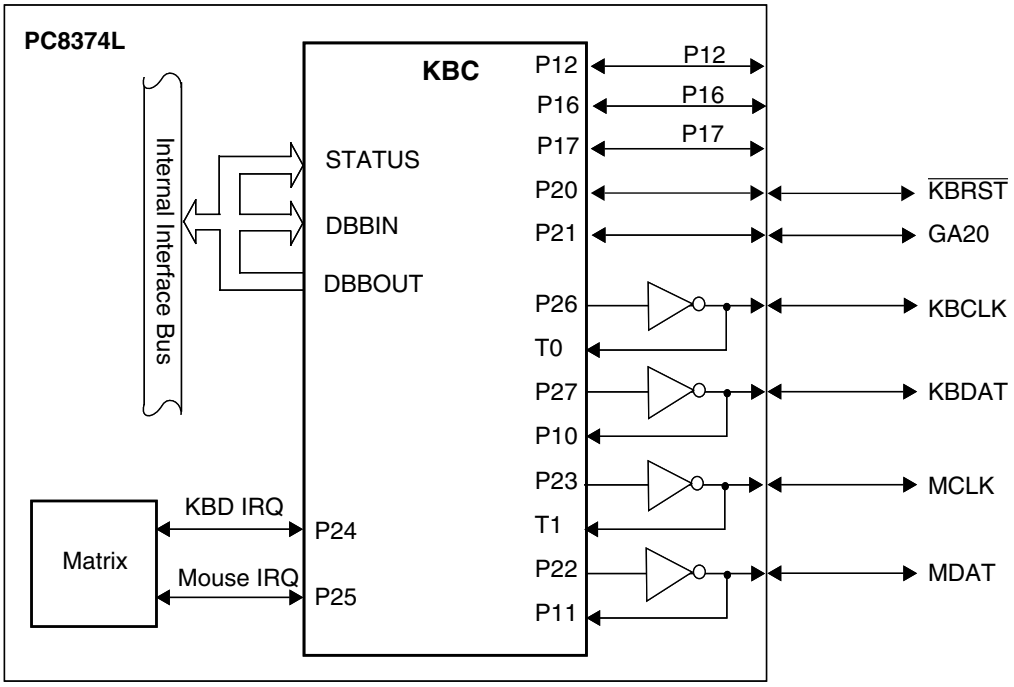


Figure 41. Keyboard and Mouse Interfaces

9.6.2 KBC Register Map

All registers are V_{DD3} powered.

Table 103. KBC Register Map

Offset	Mnemonic	Register Name	Type
00h	DBBOUT	Read KBC Data	R
	DBBIN	Write KBC Data	W
04h	STATUS	Read Status	R
	DBBIN	Write KBC Command	W

9.6.3 KBC Bitmap Summary

Table 104. KBC Bitmap Summary

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	DBBOUT	KBC Data Bits (For Read cycles)							
	DBBIN	KBC Data Bits (For Write cycles)							
04h	STATUS	General-Purpose Flags				F1	F0	IBF	OBF
	DBBIN	KBC Command Bits (For Write cycles)							

10.0 Device Characteristics

10.1 GENERAL DC ELECTRICAL CHARACTERISTICS

10.1.1 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD3}	Main 3V Supply Voltage	3.0	3.3	3.6	V
V_{SB3}	Standby 3V Supply Voltage	3.0	3.3	3.6	V
V_{BAT}	Battery Backup Supply Voltage	2.4	3.0	3.6	V
T_A	Operating Temperature	0		+70	°C

10.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur. Unless otherwise specified, all voltages are relative to ground (V_{SS}).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SUP}	Supply Voltage[1]		–0.5	+4.1	V
V_I	Input Voltage	All other pins	–0.5	5.5	V
		LAD3-0, $\overline{\text{LFRAME}}$, SERIRQ	–0.5	V_{DD3} + 0.5	V
V_O	Output Voltage	All other pins	–0.5	5.5	V
		LAD3-0, $\overline{\text{LDRQ}}$, SERIRQ	–0.5	V_{DD3} + 0.5	V
T_{STG}	Storage Temperature		–65	+165	°C
P_D	Power Dissipation			1	W
T_L	Lead Temperature Soldering (10 s)			+260	°C
	ESD Tolerance	C_{ZAP} = 100 pF R_{ZAP} = 1.5 KΩ[2]	2000		V

1. V_{SUP} is V_{DD3}, V_{SB3}.
2. Value based on test complying with RAI-5-048-RA human body model ESD testing.

10.1.3 Capacitance

Symbol	Parameter	Conditions	Min[2]	Typ[1]	Max[2]	Unit
C_{IN}	Input Pin Capacitance			4	5	pF
C_{INC}	LPC Clock Input Capacitance	PCI_CLK	5	8	12	pF
C_{PCI}	LPC Pin Capacitance	LAD3-0, $\overline{\text{LFRAME}}$, $\overline{\text{PCI\_RESET}}$, SERIRQ, $\overline{\text{LDRQ}}$		8	10	pF
C_{IO}	I/O Pin Capacitance			8	10	pF
C_O	Output Pin Capacitance			6	8	pF

1. T_A = 25°C; f = 1 MHz.
2. Not tested. Guaranteed by characterization.

10.0 Device Characteristics (Continued)

10.1.4 Power Consumption under Recommended Operating Conditions

Symbol	Parameter	Conditions[1]	Typ	Max[2]	Unit
I_{DD3}	V_{DD3} Average Supply Current	V_{IL} = 0.5V, V_{IH} = 2.4V, No Load	14	20	mA
I_{DD3LP}	V_{DD3} Quiescent Supply Current in Low Power Mode[3]	V_{IL} = V_{SS}, V_{IH} = V_{DD3}, No Load	0.5	0.8	mA
I_{SB3}	V_{SB3} Average Supply Current	V_{IL} = 0.5V, V_{IH} = 2.4V, No Load	21	30	mA
I_{SB3LP}	V_{SB3} Quiescent Supply Current in Low Power Mode[3]	V_{IL} = V_{SS}, V_{IH} = V_{SB3}, No Load	5	TBD	mA
I_{BAT}	V_{BAT} Battery Supply Current	V_{DD3}, V_{SB3} = 0V, V_{BAT} = 3V	0.2	0.4	µA

1. All parameters specified for 0°C ≤ T_A ≤ 70°C; V_{DD3} and V_{SB3} = 3.3V ±10% unless otherwise specified.
2. Not tested. Guaranteed by characterization.
3. All the modules disabled; no LPC bus activity.

10.1.5 Voltage Thresholds

Symbol	Parameter[1]	Min[2]	Typ	Max[2]	Unit
V_{DD3ON}	V_{DD3} Detected as Power-on	2.3	2.6	2.9	V
V_{DD3OFF}	V_{DD3} Detected as Power-off	2.1	2.5	2.8	V
V_{SB3ON}	V_{SB3} Detected as Power-on	2.3	2.6	2.9	V
V_{SB3OFF}	V_{SB3} Detected as Power-off	2.1	2.5	2.8	V
V_{BATLOW}	V_{BAT} Detected as “Low”			2.3	V

1. All parameters specified for 0°C ≤ T_A ≤ 70°C.
2. Not tested. Guaranteed by characterization.

10.2 DC CHARACTERISTICS OF PINS, BY I/O BUFFER TYPES

The following tables summarize the DC characteristics of all device pins described in Section 1.2 on page 15. The characteristics describe the general I/O buffer types defined in Table 1 on page 15. For exceptions, refer to Section 10.2.13 on page 217. The DC characteristics of the LPC interface meet the *PCI Local Bus Specification (Rev 2.2 December 18, 1998)* for 3.3V DC signaling.

10.2.1 Input, TTL Compatible

Symbol: IN_T

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V
I_{IL}[2]	Input Leakage Current	0 < V_{IN} < V_{SUP}[3]		±1	µA

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.
3. V_{SUP} is V_{DD3} or V_{SB3} according to the input power well.

10.0 Device Characteristics (Continued)

10.2.2 Input, TTL Compatible, with Schmitt Trigger

Symbol: IN_{TS}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V
V_{HY}	Input Hysteresis		250[2]		mV
I_{IL}[3]	Input Leakage Current	$0 < V_{IN} < V_{SUP}$[4]		±1	µA

1. Not tested. Guaranteed by design.
2. Not tested. Guaranteed by characterization.
3. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.
4. V_{SUP} is V_{DD3} or V_{SB3} according to the input power well.

10.2.3 Input, TTL Compatible, with 200 mV Schmitt Trigger

Symbol: IN_{TS2}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V
V_{HY}	Input Hysteresis		200[2]		mV
I_{IL}[3]	Input Leakage Current	$0 < V_{IN} < V_{SUP}$[4]		±1	µA

1. Not tested. Guaranteed by design.
2. Not tested. Guaranteed by characterization.
3. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.
4. V_{SUP} is V_{DD3} or V_{SB3} according to the input power well.

10.2.4 Input, TTL Compatible, with 400 mV Schmitt Trigger

Symbol: IN_{TS4}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V
V_{HY}	Input Hysteresis		400[2]		mV
I_{IL}[3]	Input Leakage Current	$0 < V_{IN} < V_{SUP}$[4]		±1	µA

1. Not tested. Guaranteed by design.
2. Not tested. Guaranteed by characterization.
3. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.
4. V_{SUP} is V_{DD3} or V_{SB3} according to the input power well.

10.0 Device Characteristics (Continued)

10.2.5 Input, PCI 3.3V Compatible

Symbol: IN_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		0.5 V_{DD}	V_{DD} + 0.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.3 V_{DD}	V
I_{IL}[2]	Input Leakage Current	0 < V_{IN} < V_{DD3}		±1	µA

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.

10.2.6 Input, SMBus Compatible

Symbol: IN_{SM}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		1.4	5.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V
I_{IL}[2]	Input Leakage Current	0 < V_{IN} < V_{SB}		±1	µA

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bidirectional buffers with TRI-STATE outputs.

10.2.7 Analog Input

Symbol: AI

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IR}	Input Voltage Range		0	5.5[1]	V
I_{IL}	Input Leakage Current	V_{IN} = V_{IR}		300	µA

1. Not tested. Guaranteed by characterization.

10.2.8 Output, TTL/CMOS Compatible, Push-Pull Buffer

Symbol: $O_{p/n}$

Output, TTL/CMOS Compatible, rail-to-rail push-pull buffer that is capable of sourcing *p* mA and sinking *n* mA

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –*p* mA	2.4		V
		I_{OH} = –50 µA	V_{SUP} – 0.2[1]		V
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V
		I_{OL} = 50 µA		0.2	V

1. V_{SUP} is V_{DD3} or V_{SB3} according to the output power well.

10.0 Device Characteristics (Continued)

10.2.9 Output, TTL/CMOS Compatible, Open-Drain Buffer

Symbol: OD_n

Output, TTL/CMOS-compatible open-drain output buffer capable of sinking *n* mA. Output from these signals is open-drain and is never forced high.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V
		I_{OL} = 50 µA		0.2	V

10.2.10 Output, PCI 3.3V Compatible

Symbol: O_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{out} = –500 µA	0.9 V_{DD3}		V
V_{OL}	Output Low Voltage	I_{out} = 1500 µA		0.1 V_{DD3}	V

10.2.11 Analog Output

Symbol: AO

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OR}	Output Voltage Range		0	5.5[1]	V
V_{OD}	Output Drive Voltage	I_{out} = –3.6 mA	V_{SUP}[2] – 150 mV		
I_{OL}	Output Leakage Current	$V_{OUT} = V_{OR}$, $V_{SUP} < V_{OUT}$		20	µA

1. Not tested. Guaranteed by characterization.
2. V_{SUP} is V_{DD3} or V_{SB3} according to the pin power well.

10.2.12 Input/Output Switch, SMBus Compatible

Symbol: SW_{SM}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRP}	Pin-to-Pin Voltage Drop	I_{SW} = ±3 mA, Switch Closed		150[1]	mV
V_{ISC}	Input Voltage for Switch Closed	I_{SW} = ±3 mA	1.5[1]		V
V_{ISO}	Input Voltage for Switch Open	I_{SW} = ±20 µA		2.25	V
I_{IL}	Input Leakage Current	$V_{ISO} < V_{IN} < 5.5V$		±20[1]	µA

1. Not tested. Guaranteed by characterization.

10.0 Device Characteristics (Continued)

10.2.13 Exceptions

1. All pins are 5V tolerant except for the output pins with PCI (O_{PCI}) buffer types.
2. All pins are back-drive protected except for the output pins with PCI (O_{PCI}) buffer types.
3. The following pins have an internal static pull-up resistor (when enabled) and therefore may have leakage current from V_{SUP} (when V_{IN} = 0): SWD, $\overline{ACK}$, $\overline{AFD\_DSTRB}$, $\overline{ERR}$, $\overline{INIT}$, PE, $\overline{SLIN\_ASTRB}$, $\overline{STB\_WRITE}$, $\overline{KBRST}$, GA20, $\overline{SIOPME}$, GPIOE00-07, GPIOE10-17, GPO11-13 PWRGD_PS, $\overline{CPU\_PRESENT}$, $\overline{PRIMARY\_HD}$, $\overline{SECONDARY\_HD}$, $\overline{SCSI}$.
4. The following pins have an internal static pull-down resistor (when enabled) and therefore may have leakage current to V_{SS} (when $V_{IN} = V_{SUP}$): BUSY_$\overline{WAIT}$, PE and SLCT, GPIOE14, GPIOE00 (on pin 118), GPIOE07 (on pin 128).
5. The following strap pins have an internal static pull-up resistor enabled during Power-Up reset and therefore may have leakage current to V_{SUP} (when V_{IN} = 0): $\overline{BADDR}$, $\overline{TRIS}$, $\overline{TEST}$, VsbStrap1, VddStrap1, VddStrap2.
6. When V_{DD3} = 0V, the following pins present a DC load to V_{SS} of 30 KΩ minimum (not tested, guaranteed by design) for a pin voltage of 0V to 3.6V: $\overline{CTS1}$, $\overline{CTS2}$, $\overline{DCD1}$, $\overline{DCD2}$, $\overline{DSR1}$, $\overline{DSR2}$, $\overline{DTR\_BOUT1}$, $\overline{DTR\_BOUT2}$, $\overline{RI1}$, $\overline{RI2}$, $\overline{RTS1}$, $\overline{RTS2}$, SIN1, SIN2, SOUT1, SOUT2.
7. Output from SLCT, BUSY_$\overline{WAIT}$ (and PE if bit 2 of PP Confg0 register is 0) is open-drain in all SPP modes except in SPP-Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is 1. Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
8. Output from $\overline{ACK}$, $\overline{ERR}$ (and PE if bit 2 of PP Confg0 register is set to 1) is open-drain in all SPP modes except in SPP-Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is set to 1. Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
9. Output from $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$ and $\overline{SLIN}$ is open-drain in all SPP modes, except in SPP-Compatible mode when the setup mode is ECP-based (FIFO). Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
10. I_{OH} is valid for a GPIO pin only when it is not configured as open-drain.
11. In XOR Tree mode, the buffer type of the input pins participating in the XOR Tree is IN_T (Input, TTL compatible), regardless of the buffer type of these pins in normal device operation mode (see Section 1.4 on page 21).

10.2.14 Terminology

Back-Drive Protection. A pin that is back-drive protected does not sink current into the supply when an input voltage higher than the supply, but below the pin's maximum input voltage, is applied to the pin. This is true even when the supply is inactive. Note that active pull-up resistors and active output buffers are typically not back-drive protected.

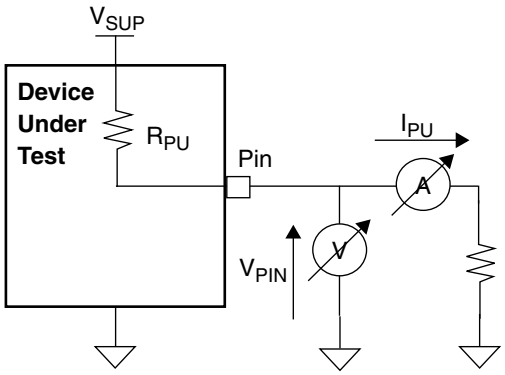
5-Volt Tolerance. An input signal that is 5V tolerant can operate with input voltage of up to 5V even though the supply to the device is only 3.3V. The actual maximum input voltage allowed to be supplied to the pin is indicated by the maximum high voltage allowed for the input buffer. Note that some pins have multiple buffers, not all of which are 5V tolerant. In such cases, there is a note that indicates at what conditions a 5V input may be applied to the pin; if there is no note, the low maximum voltage among the buffers is the maximum voltage allowed for the pin.

10.0 Device Characteristics (Continued)

10.3 INTERNAL RESISTORS

DC Test Conditions

Pull-Up Resistor Test Circuit



Pull-Down Resistor Test Circuit

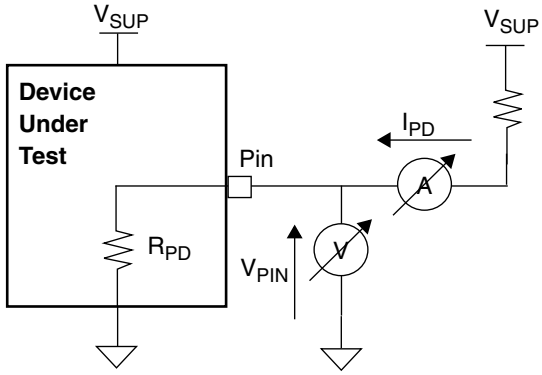


Figure 42. Internal Resistor Test Conditions, T_A = 0°C to 70°C, V_{SUP} = 3.3V

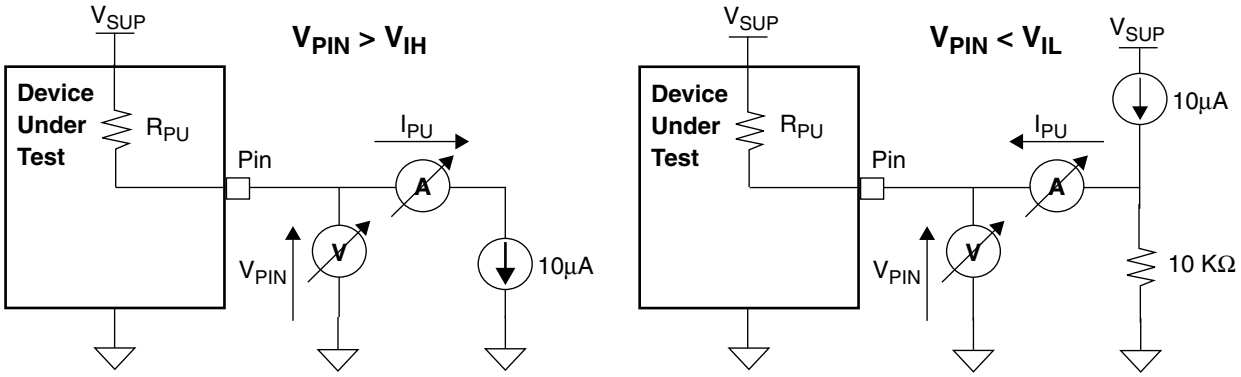


Figure 43. Internal Pull-Down Resistor for Straps, T_A = 0°C to 70°C, V_{SUP} = 3.3V

Notes for Figures 42 and 43:

1. V_{SUP} is V_{DD3} or V_{SB3} according to the pin power well.
2. The equivalent resistance of the pull-up resistor is calculated by $R_{PU} = (V_{SUP} - V_{PIN}) / I_{PU}$.
3. The equivalent resistance of the pull-down resistor is calculated by $R_{PD} = V_{PIN} / I_{PD}$.

10.3.1 Pull-Up Resistor

Symbol: PU_{nn}

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PU}	Pull-up equivalent resistance	V_{PIN} = 0V	*nn* – 30%	*nn*	*nn* + 30%	KΩ
		V_{PIN} = 0.8 V_{SUP}[3]			*nn* – 38%	KΩ
		V_{PIN} = 0.17 V_{SUP}[3]	*nn* – 35%			KΩ

1. TA = 0°C to 70°C, V_{SUP} = 3.3V.
2. Not tested. Guaranteed by characterization.
3. For strap pins only.

10.3.2 Pull-Down Resistor

Symbol: PD_{nn}

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PD}	Pull-down equivalent resistance	V_{PIN} = V_{SUP}	*nn* – 30%	*nn*	*nn* + 30%	KΩ

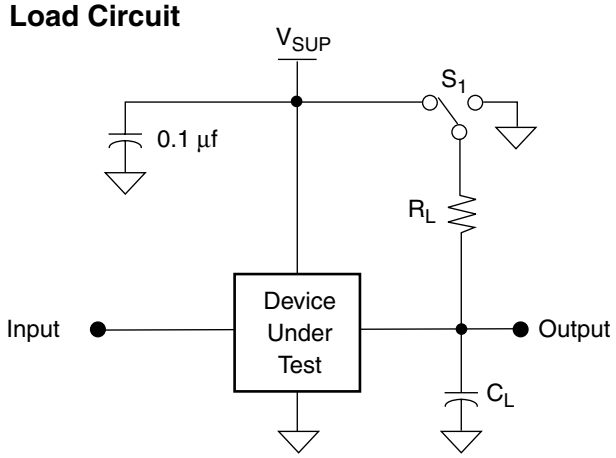
1. TA = 0°C to 70°C, V_{SUP} = 3.3V.
2. Not tested. Guaranteed by characterization.

10.0 Device Characteristics (Continued)

10.4 AC ELECTRICAL CHARACTERISTICS

10.4.1 AC Test Conditions

Load Circuit



AC Testing Input, Output Waveform

(unless otherwise specified)

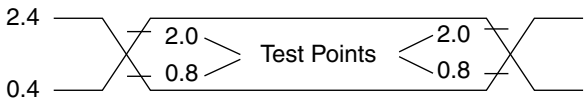


Figure 44. AC Test Conditions, T_A = 0°C to 70°C, V_{SUP} = 3.3V ±10%

Notes:

1. V_{SUP} is either V_{DD3} or V_{SB3}, according to the pin power well.
2. C_L = 50 pF for all output pins except the following pin groups:
   – C_L = 100 pF for Serial Port 1 and 2 pins (see Section 1.4.2 on page 21), Parallel Port pins (see Section 1.4.4 on page 22) and Floppy Disk Controller pins (see Section 1.4.5 on page 23).
   – C_L = 40 pF for $\overline{\text{IDE\_RSTDRV}}$ pin.
   – C_L = 400 pF for SMBus pins (see "SMBus Voltage Translation and Isolation Timing" on page 235).
   These values include both jig and oscilloscope capacitance.
3. S_1 = Open – for push-pull output pins.
   S_1 = V_{SUP} – for high impedance to active low and active low to high-impedance transition measurements.
   S_1 = GND – for high impedance to active high and active high to high-impedance transition measurements.
   R_L = 1.0 KΩ – for all the pins
4. For the FDC open-drain interface pins, S_1 = V_{DD3} and R_L = 150Ω.

10.4.2 Reset Timing

V_{SB} Power-Up Reset

Symbol	Figure	Description	Reference Conditions		Min[1]	Max[1]
t_{IRST}	45	Internal Power-Up Reset Time	V_{SB3} power-up to end of internal reset	Ended by 32 KHz Clock Domain		$t_{32KW} + t_{32KVAL}$[2] + 17 * t_{CP}
	46			Ended by $\overline{\text{PCI\_RESET}}$		t_{LRST}
t_{LRST}	46	$\overline{\text{PCI\_RESET}}$ active time	V_{SB3} power-up to end of $\overline{\text{PCI\_RESET}}$		10 ms	
t_{IPLV}	46	Internal VsbStrap1 strap pull-up resistor, valid time[3]	Before end of internal reset		t_{IRST}	
t_{EPLV}	46	External VsbStrap1 strap pull-down resistor, valid time	Before end of internal reset		t_{IRST}	

1. Not tested. Guaranteed by design.
2. t_{32KW} + t_{32KVAL} from V_{SB3} power-up to 32 KHz domain toggling; see "Low-Frequency Clock Timing" on page 223.
3. Active only during V_{SB3} Power-Up reset.

10.0 Device Characteristics (Continued)

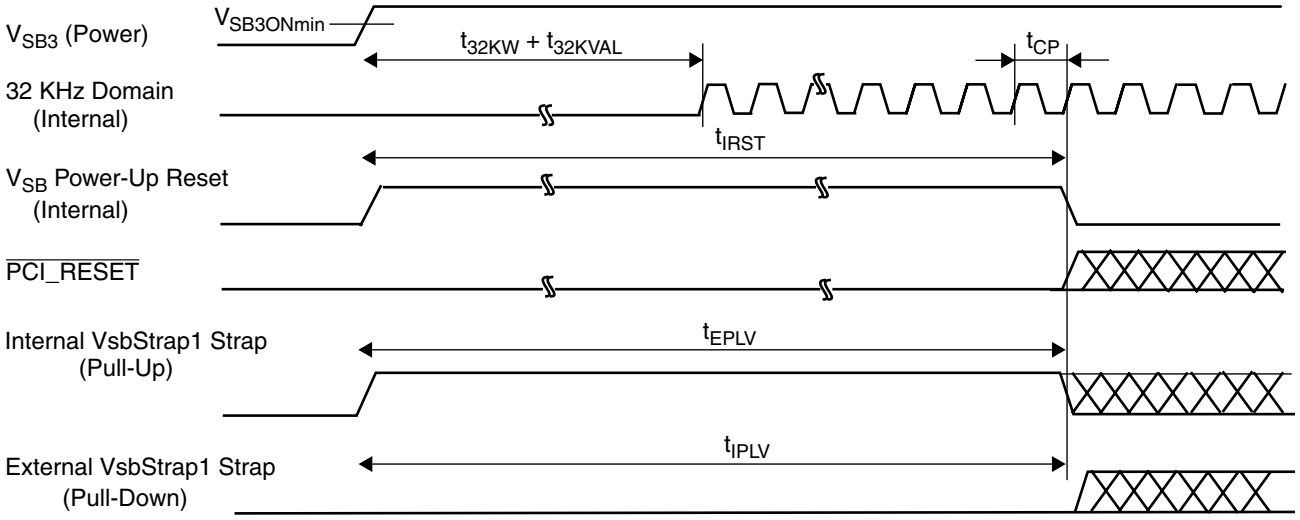


Figure 45. Internal V_{SB} Power-Up Reset - Ended by 32 KHz Clock

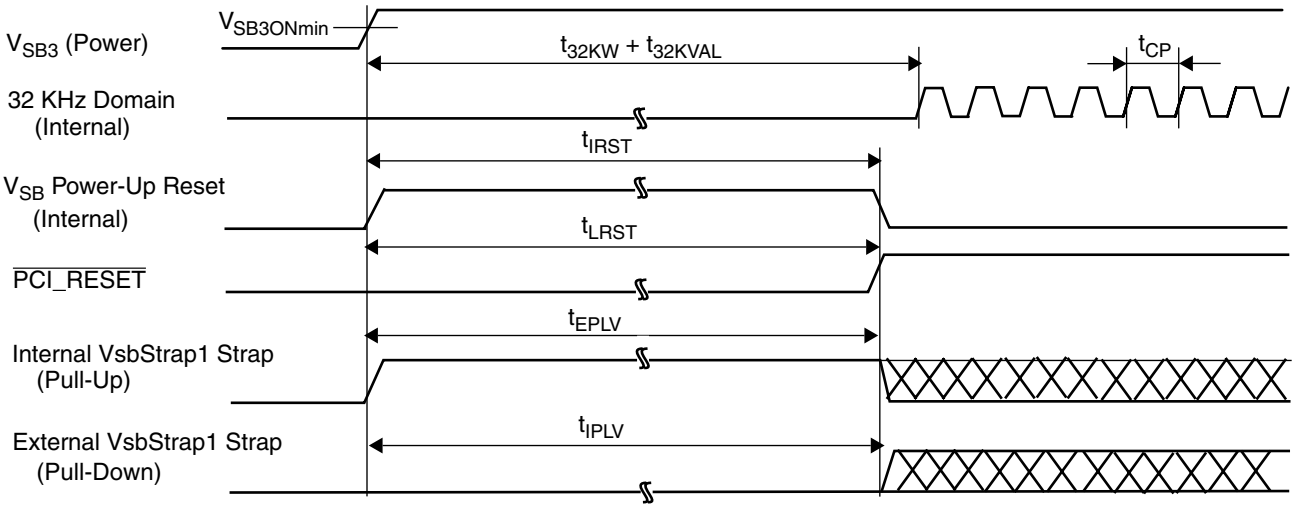


Figure 46. Internal V_{SB} Power-Up Reset - Ended by $\overline{\text{PCI\_RESET}}$

10.0 Device Characteristics (Continued)

V_{DD} Power-Up Reset

Symbol	Figure	Description	Reference Conditions	Min[1]	Max[1]
t_{IRST}	47	Internal Power-Up reset time	V_{DD3} power-up to end of internal reset		t_{LRST}
t_{LRST}	47	$\overline{PCI\_RESET}$ active time	V_{DD3} power-up to end of $\overline{PCI\_RESET}$	10 ms	2.5 s
t_{IPLV}	47	Internal strap pull-up resistor, valid time[2]	Before end of internal reset	t_{IRST}	
t_{EPLV}	47	External strap pull-down resistor, valid time	Before end of internal reset	t_{IRST}	

1. Not tested. Guaranteed by design.
2. Active only during V_{DD3} Power-Up reset.

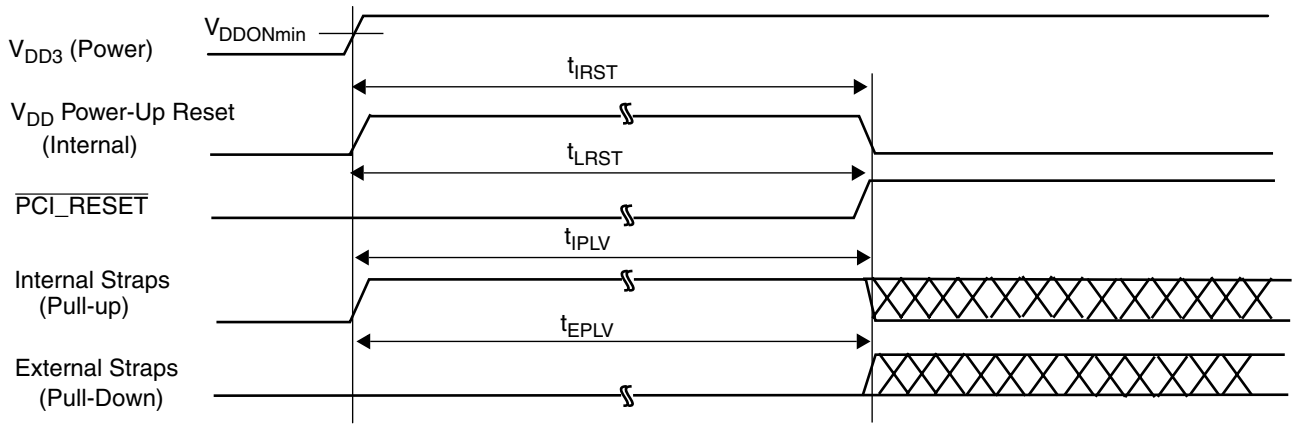


Figure 47. Internal V_{DD} Power-Up Reset

Hardware Reset

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{WRST}	48	$\overline{PCI\_RESET}$ pulse width		100 ns	

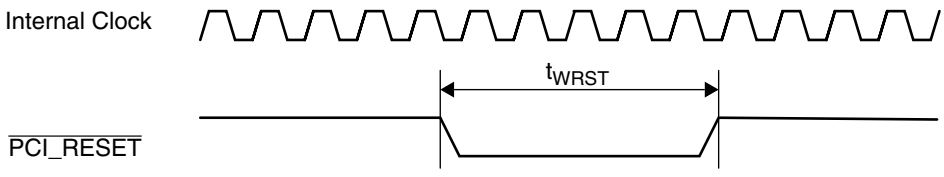


Figure 48. Hardware Reset

10.0 Device Characteristics (Continued)

10.4.3 Clock Timing

High-Frequency Clock Timing

Symbol	Figure	Clock Input Parameters	Reference Conditions	CLOCKI14			Units
				Min	Typ	Max	
t_{CH}	49	Clock High Pulse Width[1]		20			ns
t_{CL}	49	Clock Low Pulse Width[1]		20			ns
t_{CP}	49	Clock Period[1] (50%-50%)		69.14	69.84	70.54	ns
F_{CK}	–	Clock Frequency		F_{CKTYP} – 1%	14.31818	F_{CKTYP} + 1%	MHz
t_{CR}	49	Clock Rise Time[1] (V_{IL} to V_{IH})				5[2]	ns
t_{CF}	49	Clock Fall Time[1] (V_{IH} to V_{IL})				5[2]	ns
t_{CE}	50	Clock Generator Enable	RE $\overline{\text{PCI\_RESET}}$ to Clock Generator enabled			80	µs

1. Not tested. Guaranteed by design.
2. Recommended value.

Sym.	Fig.	Internal Clock Parameter	Reference Conditions	INT48M			Units
				Min	Typ	Max	
t_{CP}	49	Clock Period[1] (50%-50%)			20.83		ns
F_{CK}	–	Clock Frequency			48		MHz
t_{48MD}	50	Clock Wake-Up Time[1]	After Clock Generator enabled			500	µs

1. Not tested. Guaranteed by characterization.

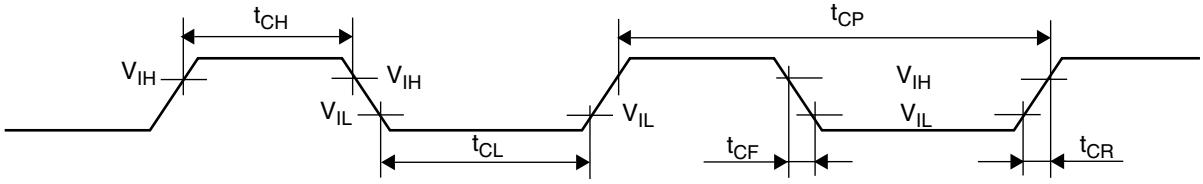


Figure 49. High-Frequency Clock Waveform Timing

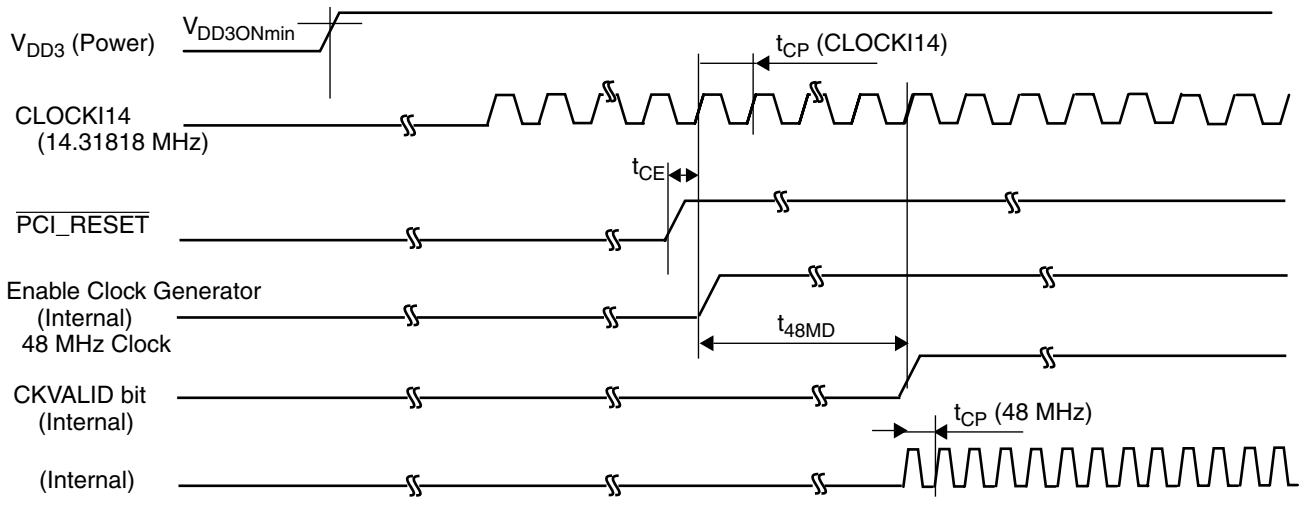


Figure 50. CLOCKI14 and Internal 48 MHz Clock Timing

10.0 Device Characteristics (Continued)

Low-Frequency Clock Timing

Symbol	Figure	Internal Clock Parameters	Reference Conditions	INT32K			Units
				Min	Typ	Max	
t_{CP}	51	Clock Period[1] (50%-50%)	After V_{SB3} power-up	21.3623	30.517578	39.6728	µs
t_{CPL}	51	Clock Period[1] (50%-50%)	After CLOCKI14 valid	30.2124	30.517578	30.8227	µs
			When V_{DD3} does not exist	27.465820	30.517578	33.569336	
F_{CK}	–	Clock Frequency	After V_{SB3} power-up	F_{32TYP} – 30%	32.768 (F_{32TYP})	F_{32TYP} + 30%	KHz
F_{CKL}		Clock Frequency	After CLOCKI14 valid	F_{32TYP} – 1%	32.768 (F_{32TYP})	F_{32TYP} + 1%	
			When V_{DD3} does not exist	F_{32TYP} – 10%	32.768 (F_{32TYP})	F_{32TYP} + 10%	
t_{32KW}	51	Clock wake-up time[1]	V_{SB3} stable to clock start toggling			5	ms
t_{32KVAL}	51	Clock valid time[1]	Clock start toggling to clock valid			1	ms

1. Not tested. Guaranteed by characterization.

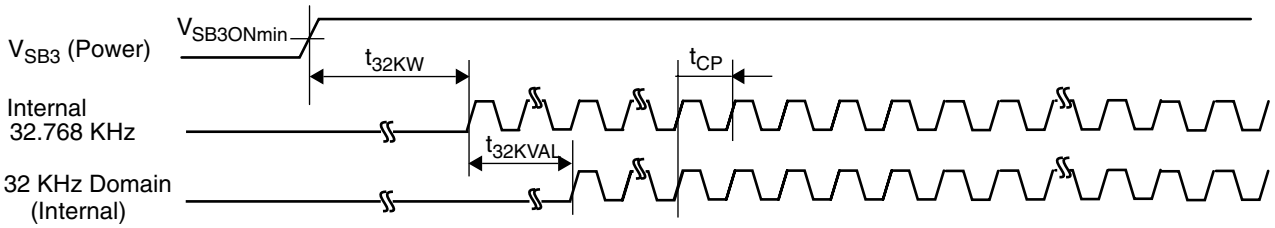


Figure 51. Internal 32 KHz (INT32K) and CLOCKO32 Timing

10.0 Device Characteristics (Continued)

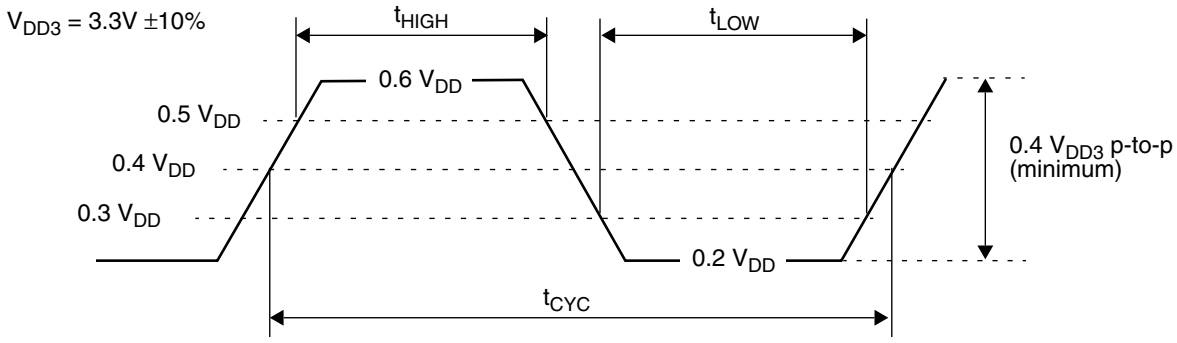
10.4.4 LPC Interface Timing

The AC characteristics of the LPC interface meet the PCI Local Bus Specification *(Rev 2.2 December 18, 1998)* for 3.3V DC signaling.

PCI_CLK and $\overline{\text{PCI\_RESET}}$

Symbol	Parameter	Min	Max	Units
t_{CYC}[1]	PCI_CLK Cycle Time	30		ns
t_{HIGH}	PCI_CLK High Time[2]	11		ns
t_{LOW}	PCI_CLK Low Time[2]	11		ns
–	PCI_CLK Slew Rate[2,3]	1	4	V/ns
–	$\overline{\text{PCI\_RESET}}$ Slew Rate[2,4]	50		mV/ns

1. The PCI may have any clock frequency between nominal DC and 33 MHz. Device operational parameters at frequencies under 16 MHz are guaranteed by design rather than by testing. The clock frequency may be changed at any time during the operation of the system as long as the clock edges remain “clean” (monotonic) and the minimum cycle high and low times are not violated. The clock may only be stopped in a low state.
2. Not tested. Guaranteed by characterization.
3. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock wavering (0.2 * V_{DD3} to 0.6 * V_{DD3}) as shown below.
4. The minimum $\overline{\text{PCI\_RESET}}$ slew rate applies only to the rising (de-assertion) edge of the reset signal and ensures that system noise cannot make an otherwise monotonic signal appear to bounce in the switching range.



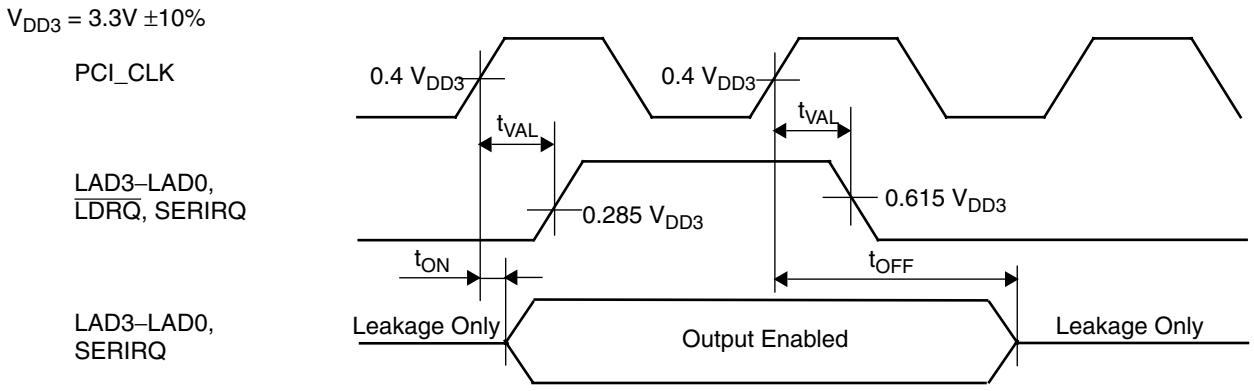
10.0 Device Characteristics (Continued)

LPC Signals

Symbol	Figure	Description	Reference Conditions	Min	Max	Unit
t_{VAL}	Outputs	Output Valid Delay	After RE of CLK	2	11	ns
t_{ON}	Outputs	Float to Active Delay	After RE of CLK	2		ns
t_{OFF}	Outputs	Active to Float Delay	After RE of CLK		28	ns
t_{SU}	Inputs	Input Setup Time	Before RE of CLK	7		ns
t_{HL}	Inputs	Input Hold Time	After RE of CLK	0		ns

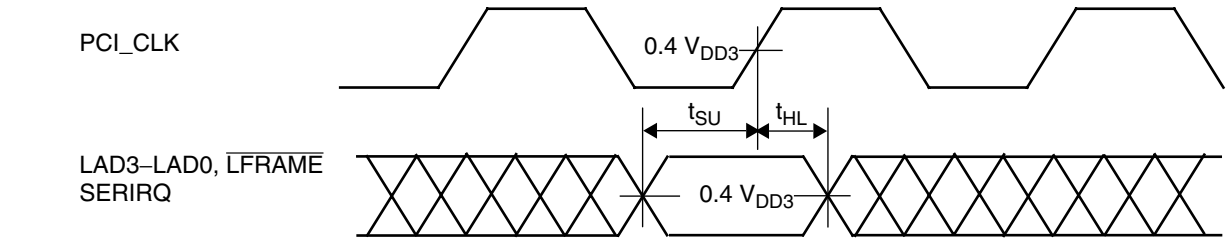
Outputs

V_{DD3} = 3.3V ±10%



Inputs

V_{DD3} = 3.3V ±10%



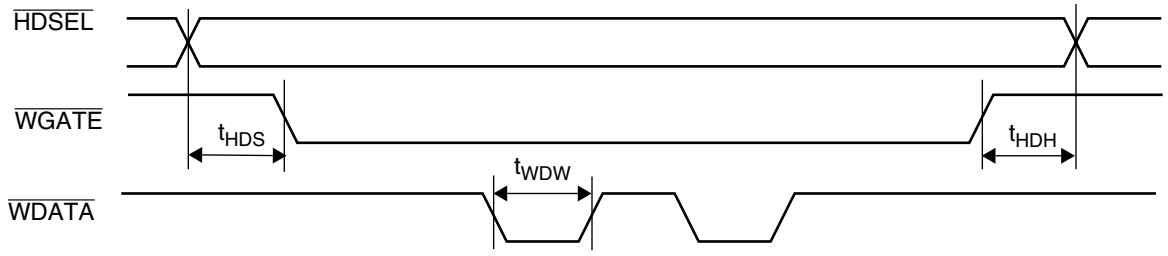
10.0 Device Characteristics (Continued)

10.4.5 FDC Timing

FDC Write Data Timing

Symbol	Parameter	Min	Max	Unit
t_{HDH}	$\overline{HDSEL}$ Hold from $\overline{WGATE}$ Inactive[1]	100		µs
t_{HDS}	$\overline{HDSEL}$ Setup to $\overline{WGATE}$ Active[1]	100		µs
t_{WDW}	Write Data Pulse Width[1]	See t_{DRP}, t_{ICP} and t_{WDW} values in table below		

1. Not tested. Guaranteed by design.



t_{DRP} t_{ICP} t_{WDW} Values

Data Rate	t_{DRP}	t_{ICP}	t_{ICP} Nominal	t_{WDW}	t_{WDW} Minimum	Unit
1 Mbps	1000	6 x t_{CP}[1]	125	2 x t_{ICP}	250	ns
500 Kbps	2000	6 x t_{CP}[1]	125	2 x t_{ICP}	250	ns
300 Kbps	3333	10 x t_{CP}[1]	208	2 x t_{ICP}	375	ns
250 Kbps	4000	12 x t_{CP}[1]	250	2 x t_{ICP}	500	ns

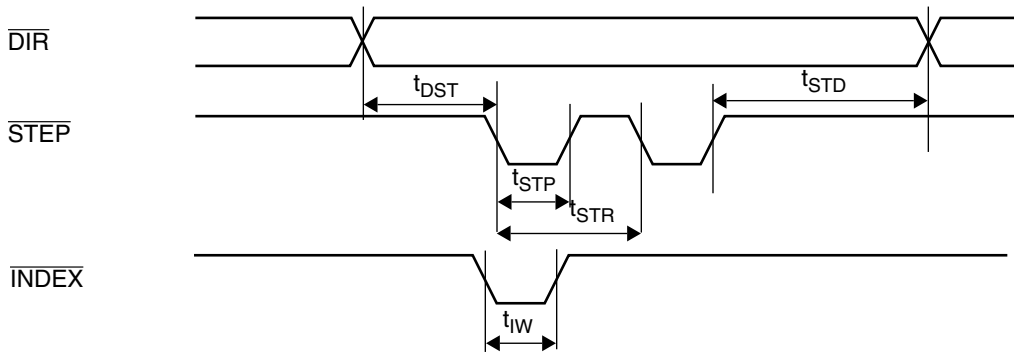
1. t_{CP} is the clock period defined for CLOCKI in “Clock Timing” on page 222.

FDC Drive Control Timing

Symbol	Parameter	Min	Max	Unit
t_{DST}	$\overline{DIR}$ Setup to $\overline{STEP}$ Active[1]	6		µs
t_{IW}	Index Pulse Width	100		ns
t_{STD}	$\overline{DIR}$ Hold from $\overline{STEP}$ Inactive	t_{STR}		ms
t_{STP}	$\overline{STEP}$ Active (Low) Pulse Width[1]	8		µs
t_{STR}	$\overline{STEP}$ Rate Time[1]	0.5		ms

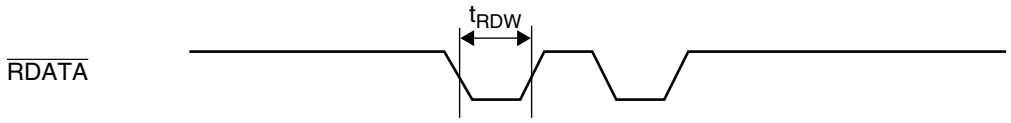
1. Not tested. Guaranteed by design.

10.0 Device Characteristics (Continued)



FDC Read Data Timing

Symbol	Parameter	Min	Max	Unit
t_{RDW}	Read Data Pulse Width	50		ns

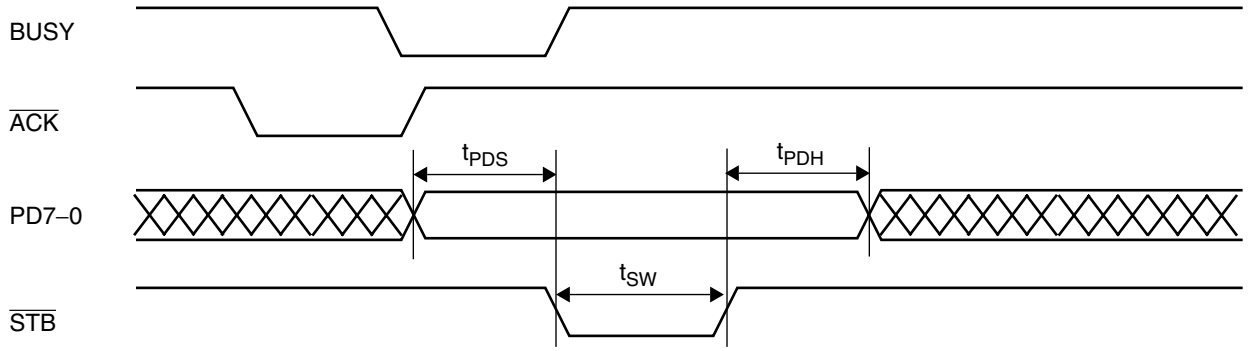


10.0 Device Characteristics (Continued)

10.4.6 Parallel Port Timing

Standard Parallel Port Timing

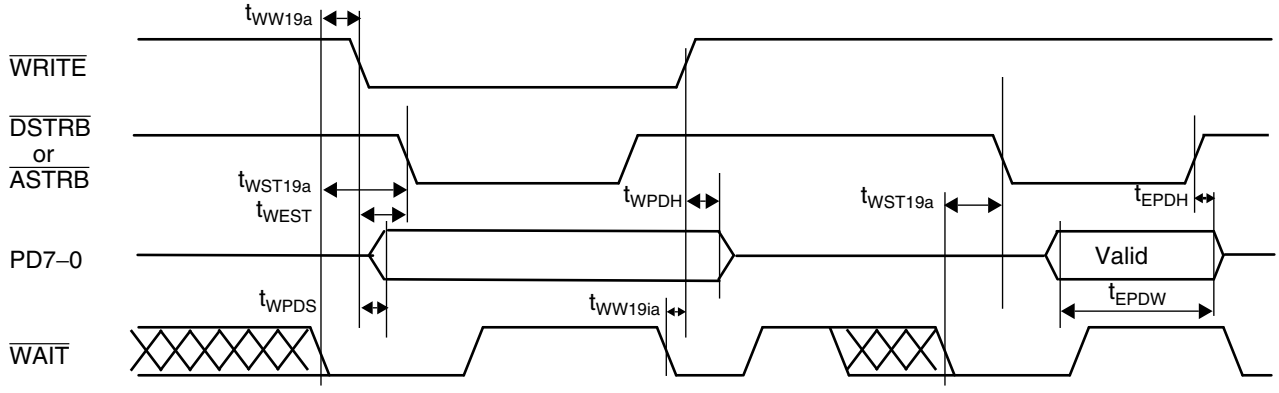
Symbol	Parameter	Conditions	Min	Max	Unit
t_{PDH}	Port Data Hold	SPP Mode 0 and Mode 1, ECP Mode 0 and Mode1: system dependent; ECP Mode 2: device dependent.	750		ns
t_{PDS}	Port Data Setup	SPP Mode 0 and Mode 1, ECP Mode 0 and Mode1: system dependent; ECP Mode 2: device dependent.	750		ns
t_{SW}	Strobe Width	SPP Mode 0 and Mode 1, ECP Mode 0 and Mode1: system dependent; ECP Mode 2: device dependent.	750		ns



Enhanced Parallel Port Timing

Symbol	Parameter	Min	Max	EPP 1.7[1]	EPP 1.9[1]	Unit
t_{WW19a}	$\overline{WRITE}$ Active from $\overline{WAIT}$ Low		45		✔	ns
t_{WW19ia}	$\overline{WRITE}$ Inactive from $\overline{WAIT}$ Low		45		✔	ns
t_{WST19a}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active from $\overline{WAIT}$ Low		65		✔	ns
t_{WEST}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active after $\overline{WRITE}$ Active	10		✔	✔	ns
t_{WPDH}	PD7–0 Hold after $\overline{WRITE}$ Inactive	0		✔	✔	ns
t_{WPDS}	PD7–0 Valid after $\overline{WRITE}$ Active		15	✔	✔	ns
t_{EPDW}	PD7–0 Valid Width	80		✔	✔	ns
t_{EPDH}	PD7–0 Hold after $\overline{DSTRB}$ or $\overline{ASTRB}$ Inactive	0		✔	✔	ns

1. Also in ECP Mode 4.



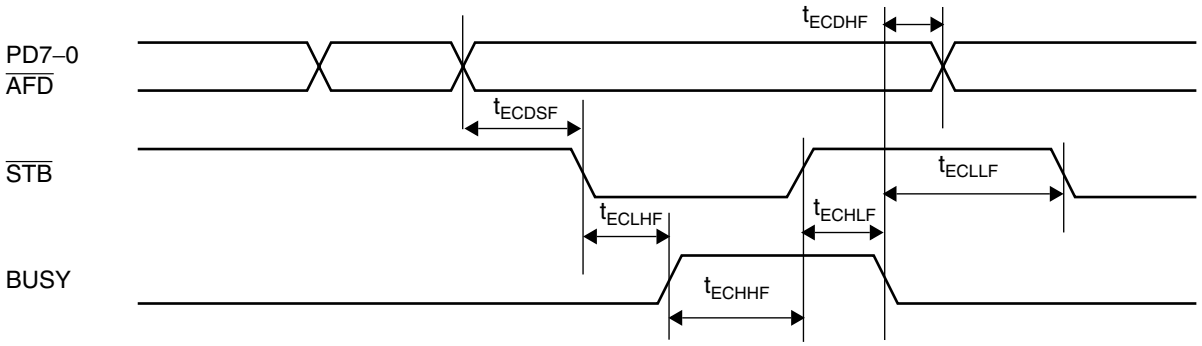
10.0 Device Characteristics (Continued)

Extended Capabilities Port (ECP) Timing

Forward Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSF}	Data Setup before $\overline{STB}$ Active	0		ns
t_{ECDHF}	Data Hold after BUSY Inactive	0		ns
t_{ECLHF}	BUSY Active after $\overline{STB}$ Active	75		ns
t_{ECHHF}	$\overline{STB}$ Inactive after BUSY Active[1]	0	1	s
t_{ECHLF}	BUSY Inactive after $\overline{STB}$ Inactive[1]	0	35	ms
t_{ECLLF}	$\overline{STB}$ Active after BUSY Inactive	0		ns

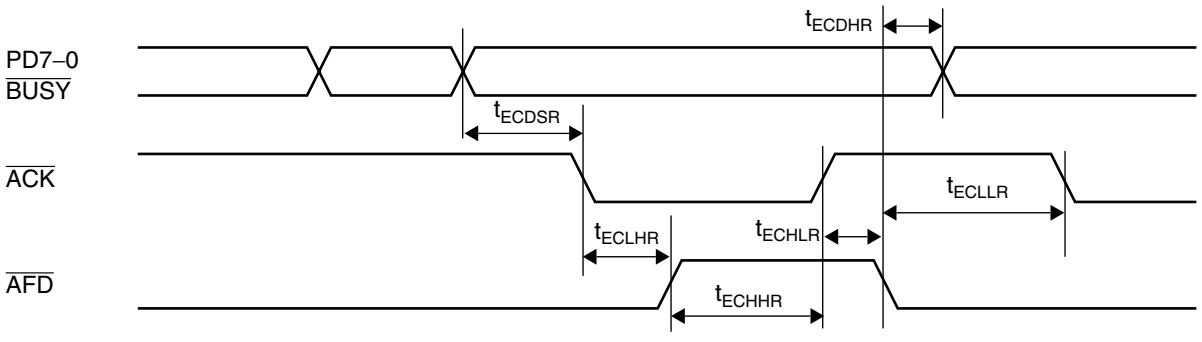
1. Not tested. Guaranteed by design.



Reverse Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSR}	Data Setup before $\overline{ACK}$ Active	0		ns
t_{ECDHR}	Data Hold after $\overline{AFD}$ Active	0		ns
t_{ECLHR}	$\overline{AFD}$ Inactive after $\overline{ACK}$ Active	75		ns
t_{ECHHR}	$\overline{ACK}$ Inactive after $\overline{AFD}$ Inactive[1]	0	35	ms
t_{ECHLR}	$\overline{AFD}$ Active after $\overline{ACK}$ Inactive[1]	0	1	s
t_{ECLLR}	$\overline{ACK}$ Active after $\overline{AFD}$ Active	0		ns

1. Not tested. Guaranteed by design.



10.0 Device Characteristics (Continued)

10.4.7 Serial Ports 1 and 2 Timing

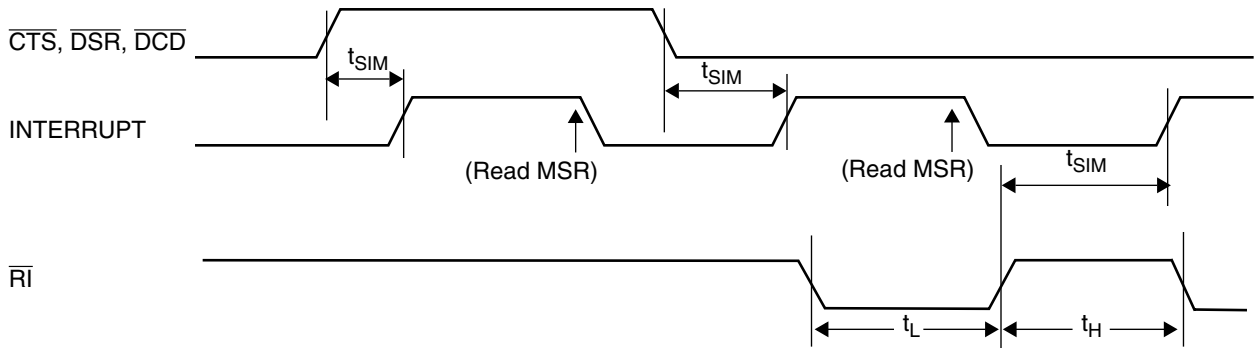
Serial Port Data Timing

See Section 10.4.8 on page 231.

Modem Control Timing

Symbol	Parameter	Min	Max	Unit
t_L	$\overline{RI1,2}$ Low Time[1,2]	10		ns
t_H	$\overline{RI1,2}$ High Time[1,2]	10		ns
t_{SIM}	Delay to Set IRQ from Modem Input		40	ns

1. Not tested. Guaranteed by characterization.
2. The value also applies to $\overline{RI1,2}$ wake-up detection in the SWC module.

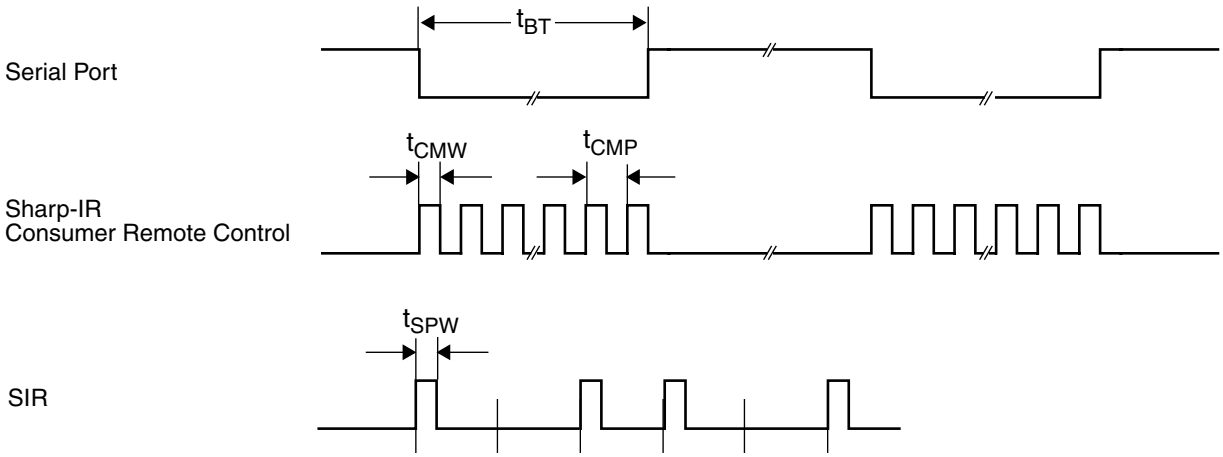


10.0 Device Characteristics (Continued)

10.4.8 Serial Port, Sharp-IR, SIR and Consumer Remote Control Timing

Symbol	Parameter	Conditions	Min[1]	Max[1]	Unit
t_{BT}	Single Bit Time in Serial Port and Sharp-IR	Transmitter	$t_{BTN} - 25$[2]	$t_{BTN} + 25$	ns
		Receiver	$t_{BTN} - 2\%$	$t_{BTN} + 2\%$	ns
t_{CMW}	Modulation Signal Pulse Width in Sharp-IR and Consumer Remote Control	Transmitter	$t_{CWN} - 25$[3]	$t_{CWN} + 25$	ns
		Receiver	500		ns
t_{CMP}	Modulation Signal Period in Sharp-IR and Consumer Remote Control	Transmitter	$t_{CPN} - 25$[4]	$t_{CPN} + 25$	ns
		Receiver	t_{MMIN}[5]	t_{MMAX}[5]	ns
t_{SPW}	SIR Signal Pulse Width	Transmitter, Variable	$(3/16) \times t_{BTN} - 15$[2]	$(3/16) \times t_{BTN} + 15$[2]	ns
		Transmitter, Fixed	1.48	1.78	µs
		Receiver	1		µs
S_{DRT}	SIR Data Rate Tolerance. % of Nominal Data Rate.	Transmitter		± 0.87%	
		Receiver		± 2.0%	
t_{SJT}	SIR Leading Edge Jitter. % of Nominal Bit Duration.	Transmitter		± 2.5%	
		Receiver		± 6.5%	

1. Not tested. Guaranteed by design.
2. t_{BTN} is the nominal bit time in Serial Port, Sharp-IR, SIR and Consumer Remote Control modes. It is determined by the setting of the Baud Generator Divisor registers.
3. t_{CWN} is the nominal pulse width of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by MCPW field (bits 7-5) of IRTXMC register and TXHSC bit (bit 2) of RCCFG register.
4. t_{CPN} is the nominal period of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by MCFR field (bits 4-0) of IRTXMC register and the TXHSC bit (bit 2) of RCCFG register.
5. t_{MMIN} and t_{MMAX} define the time range within which the period of the incoming subcarrier signal has to fall in order for the signal to be accepted by the receiver. These time values are determined by the contents of the IRRXDC register and the setting of RXHSC bit (bit 5) of RCCFG register.



10.0 Device Characteristics (Continued)

10.4.9 Glue Function Timing

Highest Active Main and Standby Supply Reference

Symbol	Figure	Description	Reference Conditions	Min	Max
Main					
t_{PD}	52	V_{DD3} to REF5V Propagation Delay[1]	V_{DD5} = 0; V_{DD3} slew rate > 10 V/ms		1 ms
Standby					
t_{PD}	52	V_{SB3} to REF5V_STBY Propagation Delay[1]	V_{SB5} = 0; V_{SB3} slew rate > 10 V/ms		1 ms

1. Not tested. Guaranteed by design.

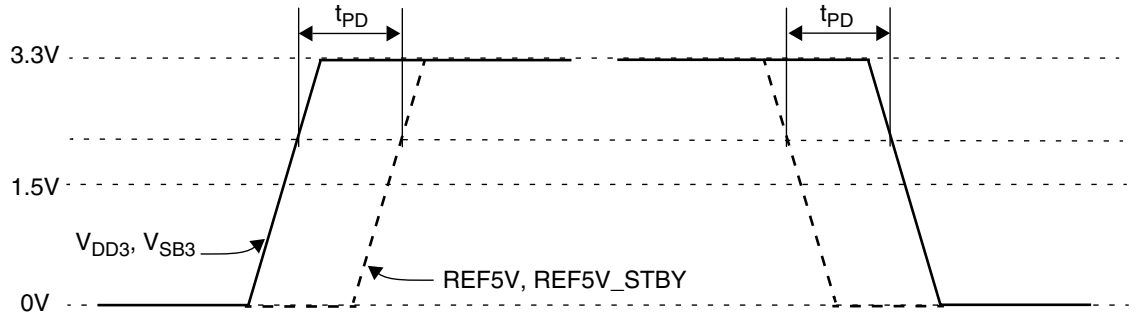


Figure 52. REF5V and REF5V_STBY (AC Characteristics)

Resume Reset

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{RD}	53	Rising Supply Delay[1] (typ. 32 ms)	$V_{SB5} > V_{TRIP}$ and $V_{SB3} > V_{SB3ON}$	20	100	ms
t_{FD5}	53	Falling V_{SB5} Supply Delay[1]	$V_{SB5} < V_{TRIP}$ and $V_{SB3} > V_{SB3ON}$		100	ns
t_{GA}	53	V_{SB5} and V_{SB3} Glitch Allowance[1]	$V_{SB5} < V_{TRIP}$ or $V_{SB3} < V_{SB3OFF}$		100	ns
t_{FD3}	53	Falling V_{SB3} Supply Delay[1]	$V_{SB3} < V_{SB3OFF}$ and $V_{SB5} > V_{TRIP}$		100	ns
t_R	53	Rise Time[2]	$V_{SB3} > V_{SB3ON}$		100	ns
t_F	53	Fall Time[2]	$V_{SB3} > V_{SB3ON}$		100	ns

1. Not tested. Guaranteed by characterization.
2. Not tested. Guaranteed by design.

10.0 Device Characteristics (Continued)

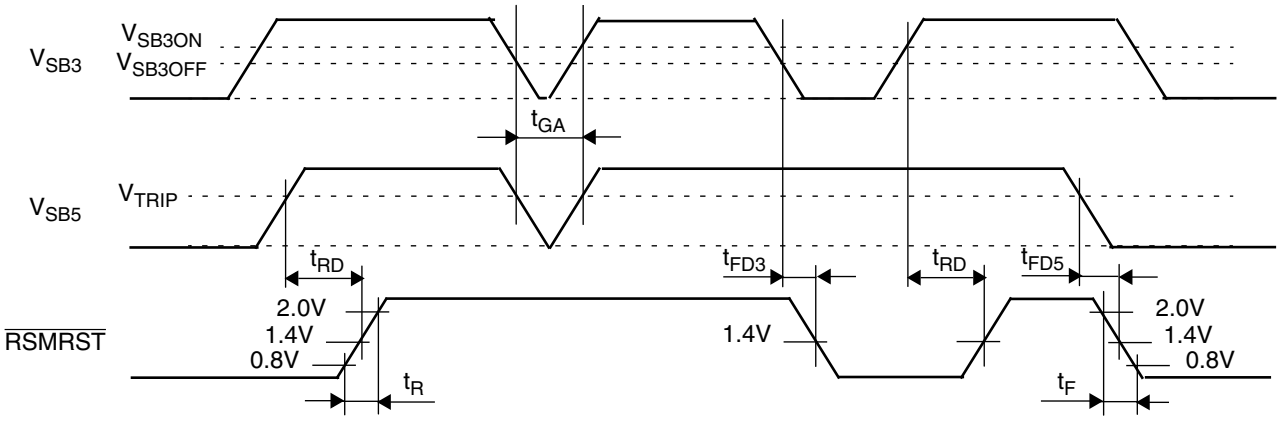


Figure 53. RSMRST (AC Characteristics)

PCI Reset Buffering

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{PDR}	54	Rise Propagation Delay	From RE of PCI_RESET to RE of PCIRST_OUT, PCIRST_OUT2		30	ns
t_R	54	Rise Time	PCIRST_OUT, PCIRST_OUT2		50	ns
t_{PDF}	54	Fall Propagation Delay	From FE of PCI_RESET to FE of IDE_RSTDRV		20	ns
t_F	54	Fall Time	IDE_RSTDRV		15	ns

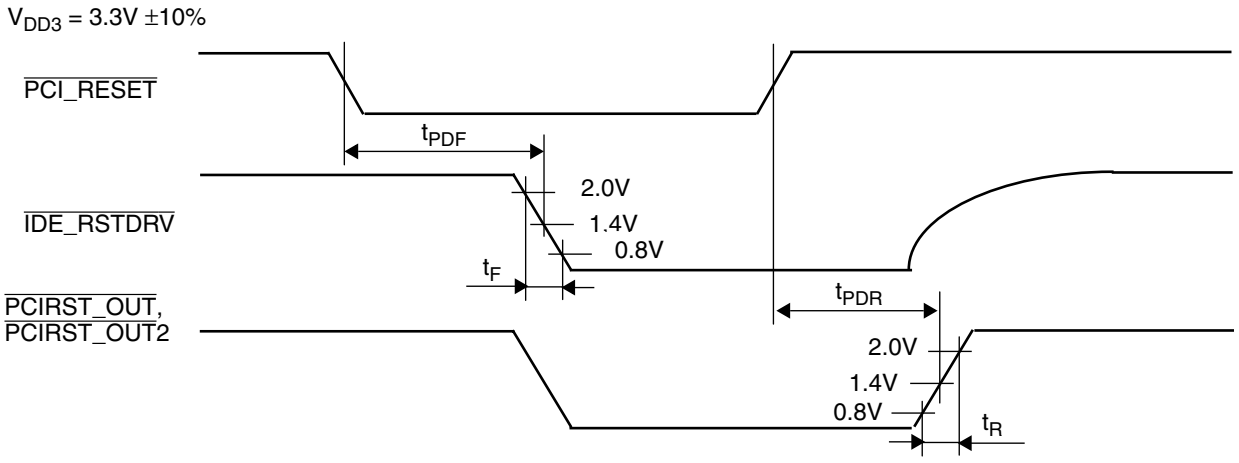


Figure 54. Reset Outputs

10.0 Device Characteristics (Continued)

Main Power Good

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{PSD}	–	Low-to-High Delay[1]	After RE of PWRGD_PS	100	120	ms
t_{S3D}	–	High-to-Low Delay[1]	After FE of $\overline{SLP\_S3}$		20	ns
t_R	–	PWRGD_3V Rise Time[1]	0.8V to 2.0V		50	ns
t_F	–	PWRGD_3V Fall Time[1]	2.0V to 0.8V		50	ns

1. Not tested. Guaranteed by design.

Power Distribution Control

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{PB}	–	$\overline{BKFD\_CUT}$ Propagation Delay[1]	PWRGD_PS or $\overline{SLP\_S3}$ to $\overline{BKFD\_CUT}$		1	µs
t_{TB}	–	$\overline{BKFD\_CUT}$ Transition Time[1]	0.8V to 2.0V		50	ns
t_{PL}	55	LATCHED_BF_CUT Propagation Delay[1]	$\overline{BKFD\_CUT}$ or $\overline{SLP\_S5}$ to LATCHED_BF_CUT		1	µs
t_{TL}	55	LATCHED_BF_CUT Transition Time[1]	0.8V to 2.0V		50	ns

1. Not tested. Guaranteed by design.

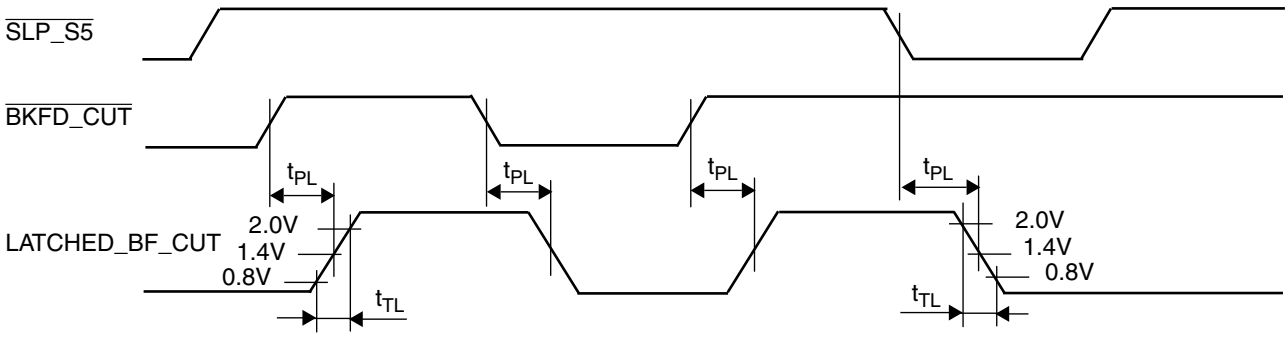


Figure 55. $\overline{BKFD\_CUT}$ and LATCHED_BF_CUT (AC Characteristics)

10.0 Device Characteristics (Continued)

Main Power Supply Control

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{PR}	–	Rise Propagation Delay[1,2]	($\overline{\text{CPU\_PRESENT}}$ = 1) or ($\overline{\text{SLP\_S3}}$ = 0) or (ETC event occurred) to RE of $\overline{\text{PS\_ON}}$		1	µs
t_{PF}	–	Fall Propagation Delay[1]	From whichever occurs last: ($\overline{\text{CPU\_PRESENT}}$ = 0), ($\overline{\text{SLP\_S3}}$ = 1), (No ETC event and RE on $\overline{\text{SLP\_S3}}$) to FE of $\overline{\text{PS\_ON}}$		1	µs
t_R	–	Rise Time[1,2]	0.8V to 2.0V		50	ns
t_F	–	Fall Time[1]	2.0V to 0.8V		50	ns

1. Not tested. Guaranteed by design.
2. Test conditions: C_L = 50 pF and 1 KΩ external resistor to V_{SB5}.

SMBus Voltage Translation and Isolation Timing

Symbol	Figure	Description	Type of Requirement[1]	Min	Max	Unit
t_{SMBR}	–	Rise Time (all signals)	Input		1000[2,3]	ns
t_{SMBF}	–	Fall Time (all signals)	Input		250[3]	ns
			Output		300[2,4]	ns
t_{SMBD}	–	Propagation Delay (each signal pair, in both directions)	Output		500[2,4]	ns

1. An “Input” type is a value the PC8374L device expects from the system; an “Output” type is a value the PC8374L device provides to the system.
2. Test conditions: R_L = 1 KΩ to V_{DD3} = 2.25V or 3.3V, or R_L = 1.5 KΩ to V_{DD5} = 5V and C_L = 400 pF to GND.
3. Not tested. Guaranteed by design.
4. Not tested. Guaranteed by characterization.

10.0 Device Characteristics (Continued)

10.4.10 SWC Timing

Wake-Up Inputs at V_{SB3} Power Switching

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{EWIV}	56	External Wake-Up Inputs Valid[1]	At V_{SB3} power on, after the 32 KHz Domain is toggling	24576 * t_{CP}[2]	32768 * t_{CP}

1. Not tested. Guaranteed by characterization.
2. t_{CP} is the cycle time of the 32 KHz clock domain (see “Low-Frequency Clock Timing” on page 223).

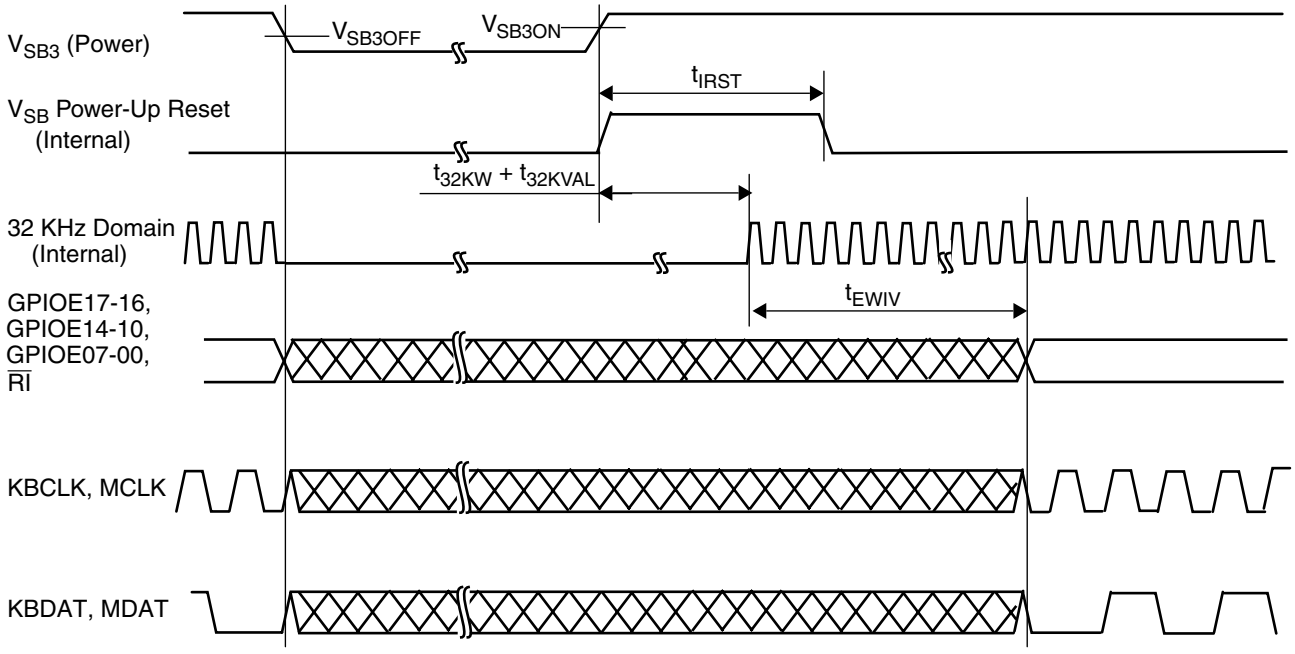


Figure 56. Inputs at V_{SB3} Power Switching

Wake-Up Inputs at V_{DD3} Power Switching

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{EWIV}	57	External Wake-Up Inputs Valid[1]	After V_{DD3} power on[2]	24576 * t_{CP}[3]	32768 * t_{CP}

1. Not tested. Guaranteed by characterization.
2. The 32 KHz clock domain is assumed to be toggling at V_{DD3} power stable.
3. t_{CP} is the cycle time of the 32 KHz clock domain (see “Low-Frequency Clock Timing” on page 223).

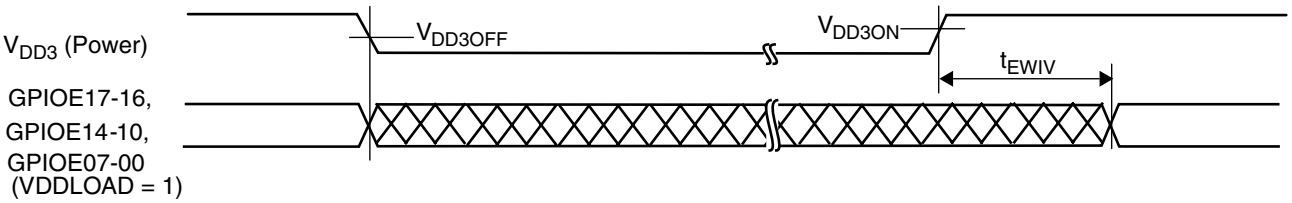


Figure 57. Wake-Up Inputs at V_{DD3} Power Switching

10.0 Device Characteristics (Continued)

10.4.11 SMBus Timing

Symbol	Figure	Description	Type of Requirement[1]	Min	Max	Unit
t_{SMBR}	58	Rise time (HMSCL and HMSDA)	Input[2]		1000[3]	ns
t_{SMBF}	58	Fall time (HMSCL and HMSDA)	Input		300[3]	ns
			Output[2]		250[4]	ns
t_{SMBCKL}	58	Clock low period (HMSCL)	Input	4.7		µs
t_{SMBCKH}	58	Clock high period (HMSCL)	Input	4		µs
t_{SMBCY}	59	Clock cycle (HMSCL)	Input	10		µs
t_{SMBDS}	59	Data setup time (before clock rising edge)	Input	250		ns
			Output[2]	250		ns
t_{SMBDH}	59	Data hold time (after clock falling edge)	Input	0		ns
			Output[2]	300		ns
t_{SMBPS}	60	Stop condition setup time (clock before data)	Input	4		µs
t_{SMBSH}	60	Start condition hold time (clock after data)	Input	4		µs
t_{SMBBUF}	60	Bus free time between Stop and Start conditions (HMSDA)	Input	4.7		µs
t_{SMBRS}	61	Restart condition setup time (clock before data)	Input	4.7		µs
t_{SMBRH}	61	Restart condition hold time (clock after data)	Input	4		µs
t_{SMBLEX}	-	Cumulative clock low extend time from Start to Stop (HMSCL)	Output		25[3]	ms
t_{SMBTO}	-	Clock low time-out (HMSCL)	Input	25[3,5]		ms
			Output		35[3,6]	ms

1. An “Input” type is a value the PC8374L expects from the system; an “Output” type is a value the PC8374L provides to the system.
2. Test conditions: R_L = 1 KΩ to V_{SB} = 3.3V, C_L = 400 pF to GND.
3. Not tested. Guaranteed by design.
4. Not tested. Guaranteed by characterization.
5. The PC8374L detects a time-out condition if HMSCL is held low for more than t_{SMBTO}.
6. On detection of a time-out condition, the PC8374L resets the SMBus Interface no later than t_{SMBTO}.

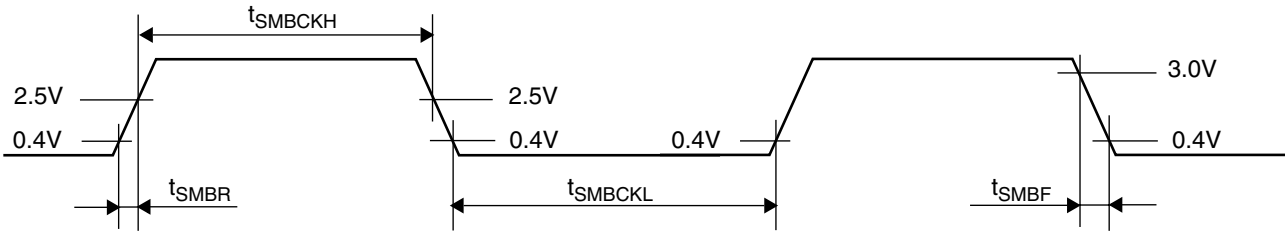


Figure 58. SMBus Signals (HMSCL and HMSDA) Rising Time and Falling Time

10.0 Device Characteristics (Continued)

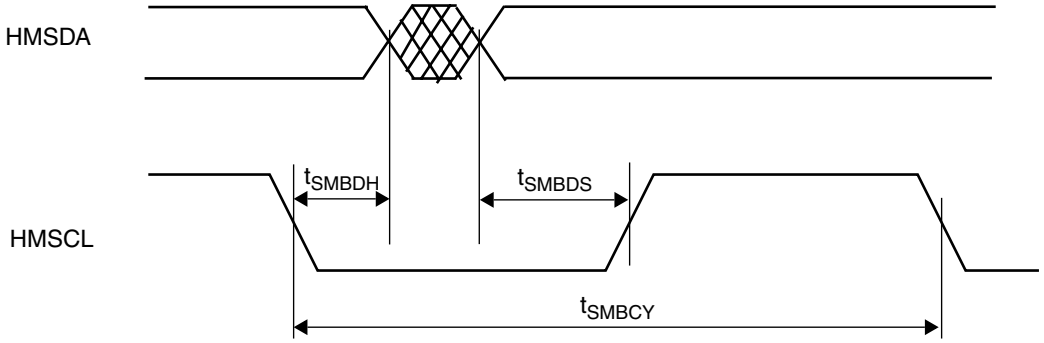


Figure 59. SMBus Data Bit Timing

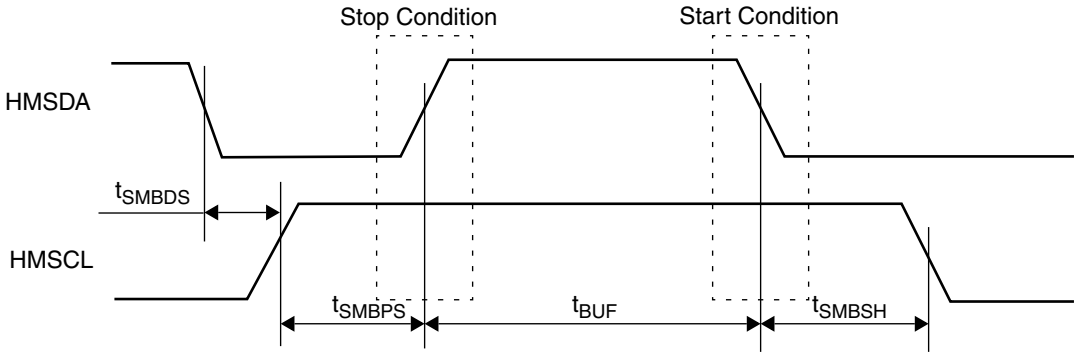


Figure 60. SMBus Start and Stop Condition Timing

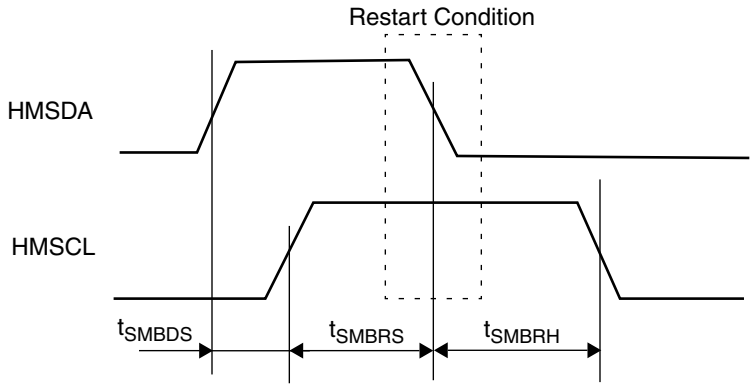


Figure 61. SMBus Restart Condition TIming

10.5 PACKAGE THERMAL INFORMATION

Thermal resistance (degrees C/W) $Theta_{JC}$ and $Theta_{JA}$ values for the PC8374L package are as follows:

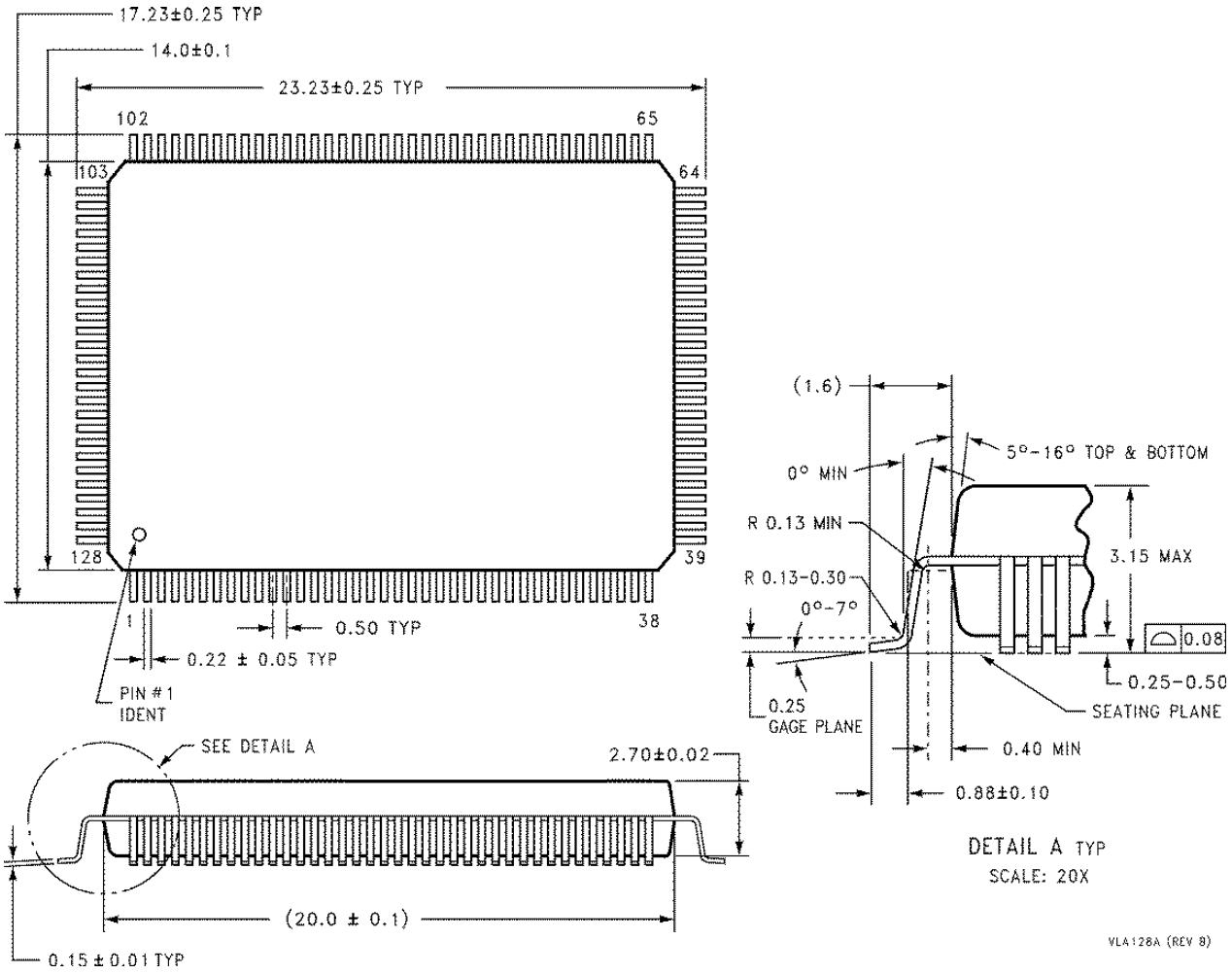
Table 105. Theta (Θ) J Values

Package Type	$Theta_{JA}$@0 lfpm	$Theta_{JA}$@225 lfpm	$Theta_{JA}$@500 lfpm	$Theta_{JA}$@900 lfpm	$Theta_{JC}$
128-PQFP	41.5	33.7	30.1	27.7	16.8

Note: Airflow for $Theta_{JA}$ values is measured in linear feet per minute (lfpm).

Physical Dimensions

All dimensions are in millimeters



Plastic Quad Flatpack (PQFP), JEDEC
Order Number PC8374L0xxx/VLA
NS Package Number VLA128A

Note: 'xxx' stands for the following Keyboard Controller Microcodes:
IBW - for AMI IBU - for Intel
IBM - for IBM ICG - for Dell
ICK - for Phoenix

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