FAIRCHILD SEMICONDUCTOR™

August 1997

NM95MS18 User's Guide

Register Summary

Following is a list of registers implemented on NM95MS18 Plug-n-Play controller. Registers located from 0x00 to 0x0F (Word address) are specific to NM95MS18 and are not part of registers defined by Plug-n-Play specification. NM95MS18 initializes itself to a specific configuration (e.g. DMA mode or Extended Interrupt mode) based on the contents of these registers. These registers are loaded from EEPROM during Power-on. Following table lists these registers along with their EPPROM address location.

Word Address	Byte Address	Register Name
0x00	0x00	I/O Decode Qualification
0x01	0x02	DMA Level Selection
0x02	0x04	Interrupt Level Selection-A
0x03	0x06	Interrupt Level Selection-B
0x04	0x08	Chip Select 0 Decode Size
0x05	0x0A	Chip Select 1 Decode Size
0x06	0x0C	Chip Select 2 Decode Size
0x07	0x0E	Reserved for Future Use
0x08	0x10	IRQ Type
0x09	0x12	Reserved for Future Use
0x0A	0x14	Reserved for Future Use
0x0B	0x16	Reserved for Future Use
0x0C	0x18	Reserved for Future Use
0x0D	0x1A	Reserved for Future Use
0x0E	0x1C	Reserved for Future Use
0x0F	0x1E	Reserved for Future Use
0x10	0x20	Vendor ID
0x11	0x22	Vendor ID
0x12	0x24	Serial Number
0x13	0x26	Serial Number
0x14 (LSB)	0x28	Checksum of (Vendor ID + Serial Number)
0x14 (MSB)	0x29	Start of PnP Resource Data Structure

Each of the above registers is explained in the next page.

Register Summary (Continued)

I/O DECODE QUALIFICATION REGISTER:

Bit Definition	Description
Bit[15]	Write-Protect bit 0 - Write protection ON for entire internal memory (PnP and Non-PnP) 1 - Write protection OFF for entire internal memory (PnP and Non-PnP)
Bit[14]	“Wire-AND” enable for IOCS2 with IOCS0 1 - Enable “Wire-AND” of IOCS2 with IOCS0 0 - Disable “Wire-AND” of IOCS2 with IOCS0
Bit[13]	“Wire-AND” enable for IOCS1 with IOCS0 1 - Enable “Wire-AND” of IOCS2 with IOCS0 0 - Disable “Wire-AND” of IOCS2 with IOCS0
Bit[12-10]	Reserved. (Must be 0)
Bit[9-8]	Mode Selection 00 - DMA Mode 01 - Extended Interrupt Mode 10 - Illegal Mode 11 - Illegal Mode
Bit[7-3]	Reserved. (Must be 0)
Bit[2]	Read-Write-Qualifier for IOCS2 signal 0 - IOCS2 signal is decoded from ISA address bus, IORD* and IOWR* 1 - IOCS2 signal is decoded from ISA address bus only.
Bit[1]	Read-Write-Qualifier for IOCS1 signal 0 - IOCS1 signal is decoded from ISA address bus, IORD* and IOWR* 1 - IOCS1 signal is decoded from ISA address bus only.
Bit[0]	Read-Write-Qualifier for IOCS0 signal 0 - IOCS0 signal is decoded from ISA address bus, IORD* and IOWR* 1 - IOCS0 signal is decoded from ISA address bus only.

DMA LEVEL SELECTION REGISTER:

Bit Definition	Description
Bit[15-8]	Reserved. (Must be 0)
Bit[7-5]	ISA DMA Channel selection for ISADRQ1 pin 000 - ISADRQ1 pin is connected to DRQ0 on the ISA bus 001 - ISADRQ1 pin is connected to DRQ1 on the ISA bus 010 - ISADRQ1 pin is connected to DRQ2 on the ISA bus 011 - ISADRQ1 pin is connected to DRQ3 on the ISA bus 100 - ISADRQ1 pin is not connected to any ISA DMA channel 101 - ISADRQ1 pin is connected to DRQ5 on the ISA bus 110 - ISADRQ1 pin is connected to DRQ6 on the ISA bus 111 - ISADRQ1 pin is connected to DRQ7 on the ISA bus
Bit[4-3]	Reserved. (Must be 0)
Bit[2-0]	ISA DMA Channel selection for ISADRQ0 pin 000 - ISADRQ0 pin is connected to DRQ0 on the ISA bus 001 - ISADRQ0 pin is connected to DRQ1 on the ISA bus 010 - ISADRQ0 pin is connected to DRQ2 on the ISA bus 011 - ISADRQ0 pin is connected to DRQ3 on the ISA bus 100 - ISADRQ0 pin is not connected to any ISA DMA channel 101 - ISADRQ0 pin is connected to DRQ5 on the ISA bus 110 - ISADRQ0 pin is connected to DRQ6 on the ISA bus 111 - ISADRQ0 pin is connected to DRQ7 on the ISA bus

Register Summary (Continued)

INTERRUPT LEVEL SELECTION REGISTER—A:

Bit Definition	Description
Bit[15-12]	ISA IRQ channel selection for IRQOUT3 pin These bits specify the ISA IRQ channel connected to ≤IRQOUT3≤ pin. Possible bit values are “0001” through “1111”. For example if the bit values are: 0100 - IRQ4 is connected to IRQOUT3 pin 1100 - IRQ12 is connected to IRQOUT3 pin Setting “0000” implies no IRQ channel is selected for this pin.
Bit[11-8]	ISA IRQ channel selection for IRQOUT2 pin Definition is similar as Bit[15-12]
Bit[7-4]	ISA IRQ channel selection for IRQOUT1 pin Definition is similar as Bit[15-12]
Bit[3-0]	ISA IRQ channel selection for IRQOUT0 pin Definition is similar as Bit[15-12]

INTERRUPT LEVEL SELECTION REGISTER—B:

Bit Definition	Description
Bit[15-12]	ISA IRQ channel selection for IRQOUT7 pin These bits specify the ISA IRQ channel connected to ≤IRQOUT3≤ pin. Possible bit values are “0001” through “1111”. For example if the bit values are: 0100 - IRQ4 is connected to IRQOUT3 pin 1100 - IRQ12 is connected to IRQOUT3 pin Setting “0000” implies no IRQ channel is selected for this pin.
Bit[11-8]	ISA IRQ channel selection for IRQOUT6 pin Definition is similar as Bit[15-12]
Bit[7-4]	ISA IRQ channel selection for IRQOUT5 pin Definition is similar as Bit[15-12]
Bit[3-0]	ISA IRQ channel selection for IRQOUT4 pin Definition is similar as Bit[15-12]

CHIP SELECT 0 DECODE SIZE REGISTER

Bit Definition	Description	
Bit[15-8]	Reserved. (Must be 0)	
Bit[7-0]	These bits should contain a value that reflects the RANGE for IOCS0 chipselect signal. For example a typical MODEM card would need ISA I/O space from 0x3f8 to 0x3ff, occupying a range of 8 bytes. In this case Bit[7-0] are set to ≤00000111≤. Following is a list of possible values:	
	Range Required	Bit[7-0] value
	1 Byte	00000000b or 00h
	2 Bytes	00000001b or 01h
	3 to 4 Bytes	00000011b or 03h
	5 to 8 Bytes	00000111b or 07h
	9 to 16 Bytes	00001111b or 0Fh
	17 to 32 Bytes	00011111b or 1Fh
	33 to 64 Bytes	00111111b or 3Fh
	65 to 128 Bytes	01111111b or 7Fh
	129 to 256 Bytes	11111111b or 7Fh

Register Summary (Continued)

CHIP SELECT 1 DECODE SIZE REGISTER

Bit Definition	Description
Bit[15-8]	Reserved. (Must be 0)
Bit[7-0]	These bits should contain a value that reflects the RANGE for IOCS1 chipselect signal. Bit definition is same as Bit[7-0] of “CHIPSELECT 0 DECODE SIZE REGISTER”

CHIP SELECT 2 DECODE SIZE REGISTER

Bit Definition	Description
Bit[15-8]	Reserved. (Must be 0)
Bit[7-0]	These bits should contain a value that reflects the RANGE for IOCS2 chipselect signal. Bit definition is same as Bit[7-0] of “CHIPSELECT 0 DECODE SIZE REGISTER”

IRQ TYPE REGISTER

Bit Definition	Description
Bit[15-8]	Reserved. (Must be 0)
Bit[7]	IRQ type selection for IRQOUT7 pin. 0 - TTL type 1 - Open-Drain type
Bit[6]	IRQ type selection for IRQOUT6 pin. 0 - TTL type 1 - Open-Drain type
Bit[5]	IRQ type selection for IRQOUT5 pin. 0 - TTL type 1 - Open-Drain type
Bit[4]	IRQ type selection for IRQOUT4 pin. 0 - TTL type 1 - Open-Drain type
Bit[3]	IRQ type selection for IRQOUT3 pin. 0 - TTL type 1 - Open-Drain type
Bit[2]	IRQ type selection for IRQOUT2 pin. 0 - TTL type 1 - Open-Drain type
Bit[1]	IRQ type selection for IRQOUT1 pin. 0 - TTL type 1 - Open-Drain type
Bit[0]	IRQ type selection for IRQOUT0 pin. 0 - TTL type 1 - Open-Drain type

Plug and Play Registers Implemented on the NM95MS18

Table A. Plug and Play Standard Registers

Name	Address Port Value	Definition
Set RD__DATA Port	0x00	Writing to this location modifies the address of the port used for reading from the Plug and Play ISA cards. Bits [7:0] become I/O read port address bits [9:2]. Reads from this register are ignored.
Serial Isolation	0x01	A read to this register causes a Plug and Play cards in the **Isolation** state to compare one bit of the boards ID. This process is fully described above. This register is read only.
Config Control	0x02	Bit[2]—Reset CSN to 0 Bit[1] Return to the **Wait for Key state** Bit[0]—Reset all logical devices and restore configuration registers to their power-up values. A write to bit[0] of this register performs a reset function on all logical devices. This resets the contents of configuration registers to their default state. All card's logical devices enter their default state and the CSN is preserved. A write to bit[I] of this register causes all cards to reset their CSN to zero. This register is write-only. The values are not sticky, that is, hardware will automatically clear them and there is no need for software to clear the bits.
Wake[CSN]	0x03	A write to this port will cause all cards that have a CSN that matches the write data [7:0] to go from the **Sleep** state to either the **Isolation** state if the write data for this command is zero or the **Config** state if the write data is not zero. Additionally, the pointer to the byte-serial device is reset. This register is write-only.
Resource Data	0x04	A read from this address reads the next byte of resource information. The Status register must be polled until bit[0] is set before this register may be read. This register is read only.
Status	0x05	Bit[0] when set indicates it is okay to read the next data byte from the Resource Data register. This register is read-only.
Card Select Number	0x06	A write to this port sets a card's CSN. The CSN is a value uniquely assigned to each ISA card after the serial identification process so that each card may be individually selected during a Wake[CSN] command. This register is read/write.
Logical Device Number	0x07	Selects the current logical device. All reads and writes of memory, I/O, interrupt and DMA configuration information access the registers of the logical device written here. In addition, the I/O Range Check and Activate commands operate only on the selected logical device. This register is read-only. It returns a value of 0x00 on Read.

Plug and Play Registers Implemented on the NM95MS18 (Continued)

Table A1. Plug & Play Logical Device Control Registers

Name	Address Port Value	Definition
Activate	0x30	For each logical device there is one activate register that controls whether or not the logical device is active on the ISA bus. Bit[0], if set, activates the logical device. Bits[7:1] are reserved and must return 0 on reads. This is a read/write register. Before a logical device is activated, I/O range check must be disabled.
I/O Range Check	0x31	This register is used to perform a conflict check on the I/O port range programmed for use by a logical device. Bit[7:2] Reserved and must return 0 on reads Bit[1] Enable I/O Range check, if set then I/O Range Check is enabled. I/O range check is only valid when the logical device is inactive. Bit[0], if set, forces the logical device to respond to I/O reads of the logical device's assigned I/O range with a 0x55 when I/O range check is in operation. If clear, the logical device drives 0xAA. This register is read/write.
I/O port base address bits [15:8] Descriptor 0	0x60	Read/write value indicating the selected I/O lower limit address bits[15:8] for I/O descriptor 0. If a logical device indicates it only uses 10 bit decoding, then bits[15:10] do not need to be supported.
I/O port base address bits [7:0] Descriptor 0	0x61	Read/write value indicating the selected I/O lower limit address bits[7:0] for I/O descriptor 0.
I/O port address descriptors [1-2]	0x62–0x65	I/O base addresses for I/O descriptors 1 and 2.

Table A2. Interrupt Configuration

Name	Register Index	Definition
Interrupt request level select 0	0x70	Read/write value indicating selected interrupt level. Bits[3:0] select which interrupt level is used for Interrupt 0. One selects IRQL 1, fifteen selects IRQL15. IRQL 0 is not a valid interrupt selection and represents no interrupt selection.
Interrupt request type select 0	0x71	Read/Write value indicating which type of interrupt is used for the Request Level selected above.
Interrupt request level select 1	0x72	Read/Write value indicating selected interrupt level. Bits[3:0] select which interrupt level is used for Interrupt 0. One selects IRQL 1, fifteen selects IRQL 15. IRQL 0 is not a valid interrupt selection and represents no interrupt selection.
Interrupt request type select 1	0x73	Read/Write value indicating which type of interrupt is used for the Request Level selected above.

Plug and Play Registers Implemented on the NM95MS18 (Continued)

Table A3. DMA Channel Configuration

Name	Register Index	Definition
DMA Channel Select 0	0x74	Read/write value indicating selected DMA channels. Bits[2:0] select which DMA channel is in use for DMA 0. Zero selects DMA channel 0, seven selects DMA channel 7. DMA channel 4, the cascade channel, is used to indicate no DMA channel is active.

Programming Interface

Table A4. Programming EEPROM Register

Name	Register Index	Definition
Status and Command Register	0xF0	Bit[I:0]—OP Code bits 10—Read operation 01—Write operation 11—Erase operation Bit[2]—GA (Go ahead bits) If set to I, the programming will continue Bit[7:3]—Reserved, should be 0
Address Register	0xF1	Address Register [A0–A7]
Data Register	0xF2	Data Byte [MSB]
Data Register	0xF3	Data Byte [LSB]
Status Register	0x05	Bit [0]—STATUS/BUSY bit during programming. “0” is busy, “1” is done.

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation
Americas
Tel. 1-888 522-5372
Fax 1-800 737-7018

www.fairchildsemi.com

Fairchild Europe
Fax: +49 (0) 1-80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

Fairchild Hong Kong Ltd.
13th Floor, Straight Block
Ocean Center, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel; (852) 2737-1600
Fax: (852) 2736-9960

NS Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179