NCT5569D

Nuvoton LPC I/O

Date: September 23rd, 2016 Revision 1.0

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1. GENERAL DESCRIPTION

The NCT5569D is a member of Nuvoton's Super I/O product line. The NCT5569D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. The NCT5569D also supports the Smart Fan control system, which makes the system more stable and user-friendly.

The NCT5569D provides one high-speed serial communication port (UART), which includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems. The NCT5569D supports keyboard and mouse interface which is 8042-based keyboard controller.

The NCT5569D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The NCT5569D supports the Intel® PECI (Platform Environment Control Interface) interface, ERP function to help customers to reduce the power consumption while in S5 state, and port 80 diagnostic messages by hardware strapping.

The configuration registers inside the NCT5569D support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows, making the allocation of the system resources more efficient than ever.

2. FEATURES

General

Meet LPC Specification 1.1
Support SERIRQ (Serialized IRQ)
Integrated hardware monitor functions
Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
Programmable configuration settings
Single 24-MHz or 48-MHz clock input
Support selective pins of 5 V tolerance

UART

One high-speed, 16550-compatible UART with 16-byte send / receive FIFO
Support RS485
--- Supports auto flow control
Fully programmable serial-interface characteristics:
--- 5, 6, 7 or 8-bit characters
--- Even, odd or no parity bit generation / detection
--- 1, 1.5 or 2 stop-bit generation
Internal diagnostic capabilities:
--- Loop-back controls for communications link fault isolation
--- Break, parity, overrun, framing error simulation
Programmable baud rate generator allows division of clock source by any value from 1 to (2^{16}-1)
Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5 M bps.

Keyboard Controller

8042-based keyboard controller
Asynchronous access to two data registers and one status register
Software-compatible with 8042
Support PS/2 mouse
Support Port 92
Support both interrupt and polling modes
Fast Gate A20 and Hardware Keyboard Reset
12MHz operating frequency

Hardware Monitor Functions

Smart Fan control system
Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in the Thermal Cruise™ mode
Support Current Mode (dual current source) temperature sensing method
Eleven voltage inputs (CPUVCORE, VIN0~4, 3VCC, AVCC, 3VSB, VTT and VBAT)
Three fan-speed monitoring inputs

Three fan-speed control outputs
Programmable hysteresis and setting points for all monitored items
Issue SMI#, OVT# (Over-temperature) to activate system protection
Nuvoton Health Manager Pro support

General Purpose I/O Ports

GPIO programmable general purpose I/O ports
Two access channels, indirect (via 2E/2F or 4E/4F) and direct (Base Address) access

ACPI Configuration

Support Glue Logic functions
Support general purpose Watch Dog Timer functions

OnNow Functions

Keyboard Wake-Up by programmable keys
Mouse Wake-Up by programmable buttons
OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

PECI Interface

Support PECI 3.0 specification
Support 2 CPU addresses and 2 domains per CPU address

AMD SB-TSI Interface

Support AMD® SB-TSI specification

Advanced Power Saving

Advanced Sleep State Control to save motherboard Stand-by power consumption

Diagnostics

Support Port80 diagnostics output via UART TX or PME# by hardware strapping
Enable Port80 to UART by Debug Port.

DDR4 Sequence

Built-in DDR4 sequence

Operation voltage

3.3 voltage

Package

64-pin LQFP

Green

3. BLOCK DIAGRAM

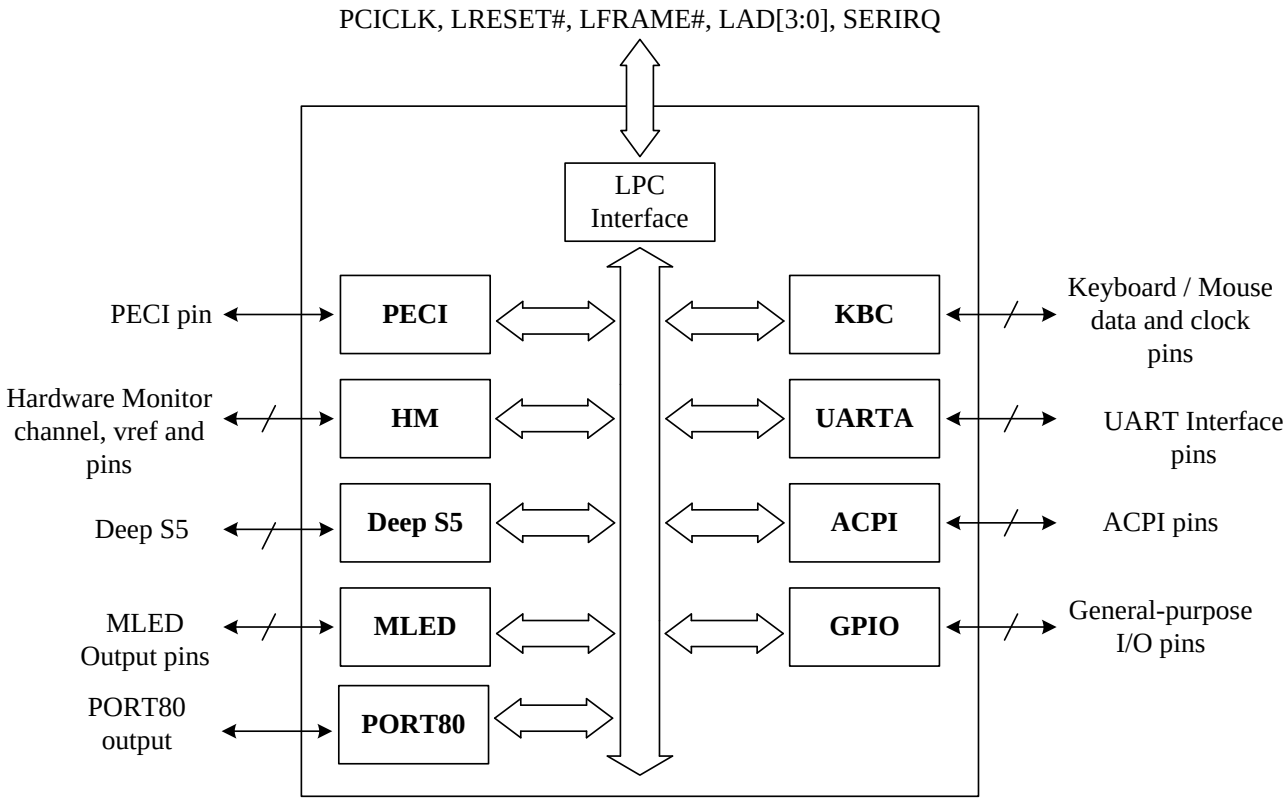


Figure 3-1 NCT5569D Block Diagram

4. PIN LAYOUT

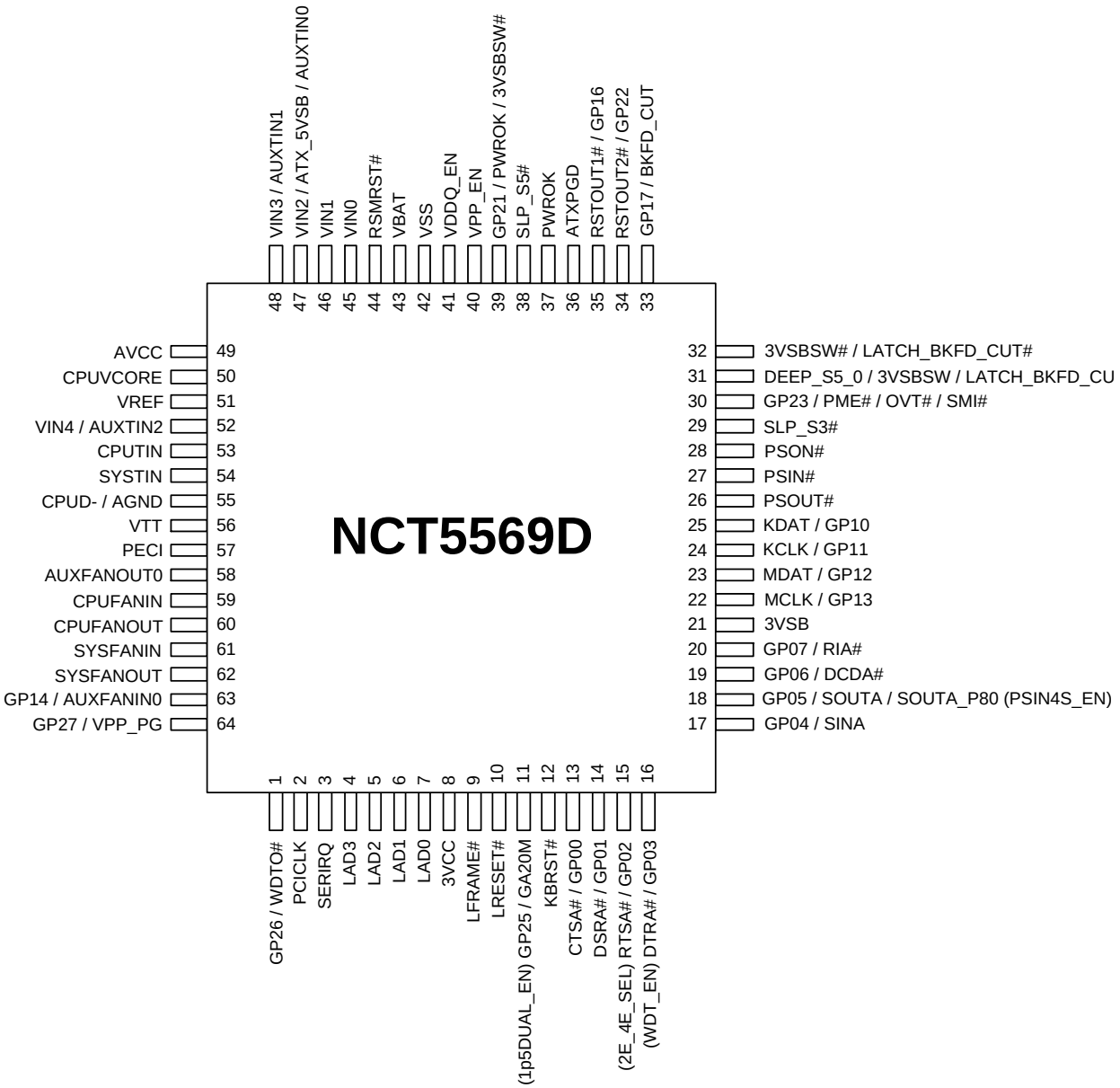


Figure 4-1 NCT5569D Pin Layout

5. PIN DESCRIPTION

AOUT - Analog output pin
AIN - Analog input pin
IN_{tp3} - 3.3V TTL-level input pin
IN_{tsp3} - 3.3V TTL-level, Schmitt-trigger input pin
IN_{gp5} - 5V GTL-level input pin
IN_{tp5} - 5V TTL-level input pin
IN_{tcup5} - 5V TTL-level, input buffer with controllable pull-up
IN_{tscup5} - 5V TTL-level, Schmitt-trigger, input buffer with controllable pull-up
IN_{tsp5} - 5V TTL-level, Schmitt-trigger input pin
IN_{tdp5} - 5V TTL-level input pin with internal pull-down resistor
IN_{tp318} - 3.3V/1.8V TTL-level input pin
IN_{sp318} - 3.3V/1.8V TTL-level, Schmitt-trigger input pin
O_8 - output pin with 8-mA source-sink capability
OD_8 - open-drain output pin with 8-mA sink capability
O_{12} - output pin with 12-mA source-sink capability
OD_{12} - open-drain output pin with 12-mA sink capability
O_{24} - output pin with 24-mA source-sink capability
OD_{24} - open-drain output pin with 24-mA sink capability
O_{48} - output pin with 48-mA source-sink capability
OD_{48} - open-drain output pin with 48-mA sink capability
I/O_{v3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O_{v4} - Bi-direction pin with source capability of 6 mA
O_{12cu} - output pin 12-mA source-sink capability with controllable pull-up
OD_{12cu} - open-drain 12-mA sink capability output pin with controllable pull-up

5.1 LPC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
2	PCICLK	I	IN_{tp5}	VCC	Low Pin Count interface clock, 19.2MHZ~33MHz.
3	SERIRQ	I/O	IN_{tp3} O_8 OD_8	VCC	Serialized IRQ input / output.
7-4	LAD[3:0]	I/O	IN_{tp3} OD_{12}	VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
9	LFRAME#	I	IN_{tp3}	VCC	Indicates the start of a new cycle or the termination of a broken cycle.
10	LRESET#	I	IN_{tsp3}	VCC	Reset signal. It can be connected to the PCIRST# signal on the host.
30	PME#	O	OD_{12}	VSB	Generated PME event.

5.2 Serial Port Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
20	RIA#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
19	DCDA#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
18	SOUTA	O	O_{12}	VSB	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
18	SOUTA_P80	O	O_{12}	VCC	PORT80 to UART Serial Output. This pin is used to transmit serial data out to the communication link.
17	SINA	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
16	DTRA#	O	O_{12}	VSB	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
15	RTSA#	O	O_{12}	VSB	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
14	DSRA#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
13	CTSA#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.

5.3 KBC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
11	GA20M	O	O_{12} OD_{12}	VSB	Gate A20 output. This pin is high after system reset. (KBC P21)
12	KBRST#	OD	O_{12} OD_{12}	VSB	Keyboard reset. This pin is high after system reset. (KBC P20)
24	KCLK	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Clock.
25	KDAT	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Data.
22	MCLK	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Clock.
23	MDAT	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Data.

5.4 Hardware Monitor Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
45	VIN0	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
46	VIN1	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
47	VIN2	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
47	ATX_5VSB	I	AIN	VRTC	Analog input for voltage measurement (Range: 0 to 2.048 V)
48	VIN3	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
52	VIN4	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
50	CPUVCORE	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
51	VREF	O	AOUT	AVCC	Reference Voltage (around 2.048 V).
47	AUXTIN0	I	AIN	AVCC	The input of temperature sensor 0. It is used for AUX0 temperature sensing.
48	AUXTIN1	I	AIN	AVCC	The input of temperature sensor 1. It is used for AUX1 temperature sensing.
52	AUXTIN2	I	AIN	AVCC	The input of temperature sensor 2. It is used for AUX2 temperature sensing.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
53	CPUTIN	I	AIN	AVCC	The input of temperature sensor 1. It is used for CPU temperature sensing.
54	SYSTIN	I	AIN	AVCC	The input of temperature sensor 1. It is used for SYS temperature sensing.
30	OVT#	O	OD_{12}	VSB	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
	SMI#	O	OD_{12}	VSB	System Management Interrupt channel output.
63	AUXFANIN0	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
58	AUXFANOUT0	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
59	CPUFANIN	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
60	CPUFANOUT	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
61	SYSFANIN	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
62	SYSFANOUT	O	O_{12} OD_{12} AOUT	VCC	PWM duty-cycle signal for fan speed control. DC voltage output for fan speed control.

5.5 Intel® PECI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
57	PECI	I/O	I/O_{V3}	Vtt	INTEL® CPU PECI interface. Connect to CPU.

5.6 Advanced Configuration & Power Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
27	PSIN#	I	IN_{tp5}	VSB	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.
26	PSOUT#	O	OD_{12}	VSB	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.
44	RSMRST#	O	OD_{8}	VRTC	Resume reset signal output.
29	SLP_S3#	I	IN_{tp318}	VSB	SLP_S3# input.
38	SLP_S5#	I	IN_{tp318}	VSB	SLP_S5# input.
28	PSON#	O	OD_{12}	VSB	Power supply on-off output.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
37	PWROK	O	O_8 OD_8	VRTC	3VCC PWROK signal.
36	ATXPGD	I	IN_{tp5}	VSB	ATX power good signal.
39	PWROK	O	OD_{12}	VSB	3VCC PWROK signal.
31	3VSBSW	O	OD_{12}	VRTC	Switch 3VSB power to memory when in S3 state.
32	3VSBSW#	O	OD_{24}	VSB	Switch 3VSB power to memory when in S3 state.
39	3VSBSW#	O	OD_{12}	VSB	Switch 3VSB power to memory when in S3 state.
35	RSTOUT1#	O	O_{24} OD_{24}	VSB	PCI Reset Buffer 1. This pin default is push-pull output and could be programmed to open-drain output by register Logic Device A, CRF7 bit6.
34	RSTOUT2#	O	O_{24} OD_{24}	VSB	PCI Reset Buffer 2. This pin default is push-pull output and could be programmed to open-drain output by register Logic Device A, CRF7 bit7.

5.7 Advanced Sleep State Control Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
31	DEEP_S5_0	O	OD_{12}	VRTC	This pin is to control system power for entering “more power saving mode”.

5.8 Port 80 Message Display

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
18	SOUTA_P80	O	O_{12}	VCC	PORT80 to UART Serial Output. This pin is used to transmit serial data out to the communication link.

5.9 Dual Voltage Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
33	BKFD_CUT	O	OD_{12}	VSB	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S3 sleep state.
32	LATCH_BKFD_CUT#	O	O_{24}	VSB	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S5 sleep state.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
31	LATCH_BKFD_CUT	O	O_{12}	VRTC	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S5 sleep state.

5.10 WatchDog

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
1	WDTO#	O	OD_{12}	VSB	Watchdog Timer output signal.

5.11 DDR4 Power Sequence

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
64	VPP_PG	I	IN_{tp5}	VSB	DDR4 VPP power on sequence ok signal
40	VPP_EN	O	OD_{12}	VSB	VPP Power Enable
41	VDDQ_EN	O	OD_{12}	VSB	VDDQ Power Enable

5.12 Power Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
21	3VSB	I			+3.3 V stand-by power supply for the digital circuits.
43	VBAT	I			+3 V on-board battery for the digital circuits.
8	VCC	I			+3.3 V power supply for driving 3 V on host interface.
49	AVCC	I			Analog +3.3 V power input. Internally supply power to all analog circuits.
55	CPUD- / AGND	I			Analog ground. The ground reference for all analog input. Internally connected to all analog circuits. This pin should be connected to ground.
42	VSS	I			Ground.
56	VTT	I			INTEL® CPU VTT power.

5.13 General Purpose I/O Port

5.13.1 GPIO-0 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
13	GP00	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 0.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
14	GP01	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 1.
15	GP02	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 2.
16	GP03	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 3.
17	GP04	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 4.
18	GP05	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 5.
19	GP06	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 6.
20	GP07	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 7.

5.13.2 GPIO-1 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
25	GP10	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 0.
24	GP11	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 1.
23	GP12	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 2.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
22	GP13	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 3.
63	GP14	I/O	IN_{tsp5} O_{12} OD_{12}	VCC	General-purpose I/O port 1 bit 4.
35	GP16	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 6.
33	GP17	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 7.

5.13.3 GPIO-2 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
39	GP21	I/O	IN_{tp5} O_{24} OD_{24}	VSB	General-purpose I/O port 2 bit 1.
34	GP22	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 2.
30	GP23	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 3.
11	GP25	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 5.
1	GP26	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 6.
64	GP27	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 7.

5.14 Strapping Pins

<table>
<tr><th>PIN</th><th>SYMBOL</th><th>I/O</th><th>BUFFER TYPE</th><th>POWER WELL</th><th>DESCRIPTION</th></tr>
<tr><td>11</td><td>1p5DUAL_
EN</td><td>I</td><td>IN_{tdp5}</td><td>VSB</td><td>Pin32 function selection.
(Strapped by VSB)

Pin32 function selection
<table>
<tr><th>1p5DUAL_EN</th><th>CR2C Bit 6-5</th><th>Pin32</th></tr>
<tr><td>1</td><td>xx</td><td>1p5VDual_EN#</td></tr>
<tr><td>0</td><td>00</td><td>3VSBSW#</td></tr>
<tr><td>0</td><td>1x</td><td>LATCH_BKFD_CUT</td></tr>
<tr><td>0</td><td>01</td><td>3VSBSW#</td></tr>
</table></td></tr>
<tr><td>15</td><td>2E_4E_SEL</td><td>I</td><td>IN_{tdp5}</td><td>VSB</td><td>SIO I/O address selection.
(Strapped by LRESET#)

Strapped to high: SIO I/O address is 4Eh/4Fh.
Strapped to low: SIO I/O address is 2Eh/2Fh.</td></tr>
<tr><td>16</td><td>WDT_EN</td><td>I</td><td>IN_{tdp5}</td><td>VSB</td><td>RESETCONO# WDT Pulse Output selection
(Strapped by VCC: internal Power OK signal without any delay.)

Strapped to high: Enable WDT5s to RESETCONO#.
Strapped to low: Disable WDT5s to RESETCONO#</td></tr>
<tr><td>18</td><td>PSIN4S_EN</td><td>I</td><td>IN_{tdp5}</td><td>VSB</td><td>Input clock rate selection
(Strapped by VCC: internal Power OK signal without any delay.)

Strapped to high: Enable PSIN# keep low over 4sec function.
Strapped to low: Enable PSIN# keep low over 4sec function.</td></tr>
</table>

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

1) VSB Strapping result can be programming by LPC, and reset by RSMRST#.
2) VCC Strapping result can be programming by LPC, and reset by PWROK.
3) LRESET# strapping (2E_4E_SEL) can be programming by LPC, and reset by LRESET#.

5.15 Internal pull-up, pull-down pins

Signal	Pin(s)	Power well	Type	Resistor	Note
Strapping Pins					
2E_4E_SEL	15	3VSB	Pull-down	47.4K	1

Signal	Pin(s)	Power well	Type	Resistor	Note
WDT_EN	16	3VSB	Pull-down	47.4K	1
PSIN4S_EN	18	3VSB	Pull-down	47.4K	1
1p5DUAL_EN	11	3VSB	Pull-down	47.4K	1
Advanced Configuration & Power Interface					
PSIN#	27	3VSB	Pull-up	47.03K	

Note1. Active only during VCC Power-up reset
Note2. Active only during VSB Power-up reset

6. GLUE LOGIC

6.1 ACPI Glue Logic

Table 6-1 Pin Description

SYMBOL	PIN	DESCRIPTION
SLP_S5#	38	SLP_S5# input.
PWROK	37	This pin generates the PWROK signals while 3VCC is present.
RSMRST#	44	The RSMRST# signal is a reset output and is used as the VSB power on reset signal for the South Bridge. When the NCT5569D detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

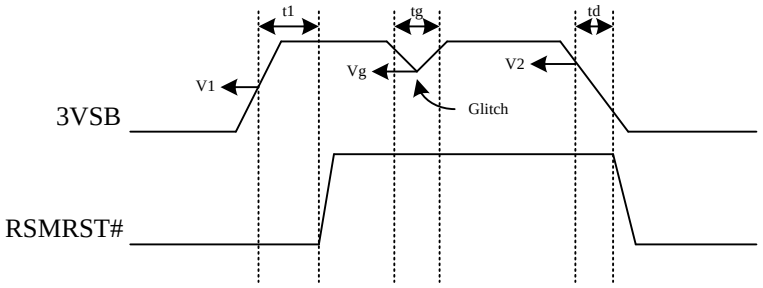


Figure 6-1 RSMRST# and VSB

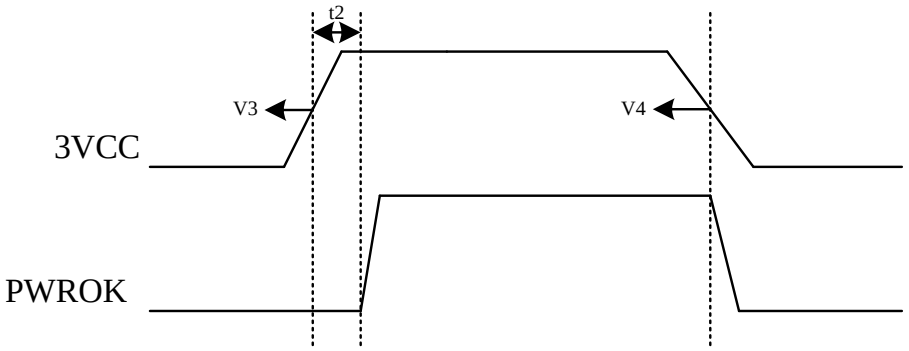


Figure 6-2 PWROK and VCC

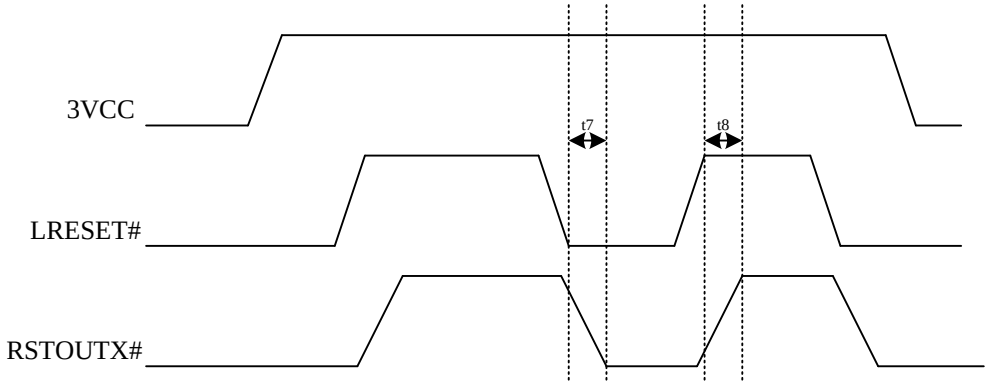


Figure 6-3 RSTOUTX# and LRESET#

TIMING	PARAMETER	MIN	MAX	UNIT
t1	Valid 3VSB to RSMRST# inactive	200	300	mS
tg	3VSB Glitch allowance		1	uS
td	Falling 3VSB supply Delay		1	uS
t2	Valid 3VCC to PWROK active	300	500	mS
t7	LRESET# active to RSTOUTx# active	0	80	nS
t8	LRESET# inactive to RSTOUTx# inactive	0	80	nS

DC	PARAMETER	MIN	MAX	UNIT
V1	3VSB Valid Voltage	2.94	3.00	Volt
V2	3VSB Ineffective Voltage	2.9	2.96	Volt
V3	3VCC Valid Voltage	-	2.75	Volt

DC	PARAMETER	MIN	MAX	UNIT
V4	3VCC Ineffective Voltage	2.40	-	Volt
Vg	3VSB drops by Power noise	2	-	Volt

Note： 1. The values above are the worst-case results of R&D simulation.

6.2 BKFD_CUT & LATCH_BKFD_CUT

NCT5569D supports BKFD_CUT & LATCH_BKFD_CUT functions, please refer the timing diagram below:

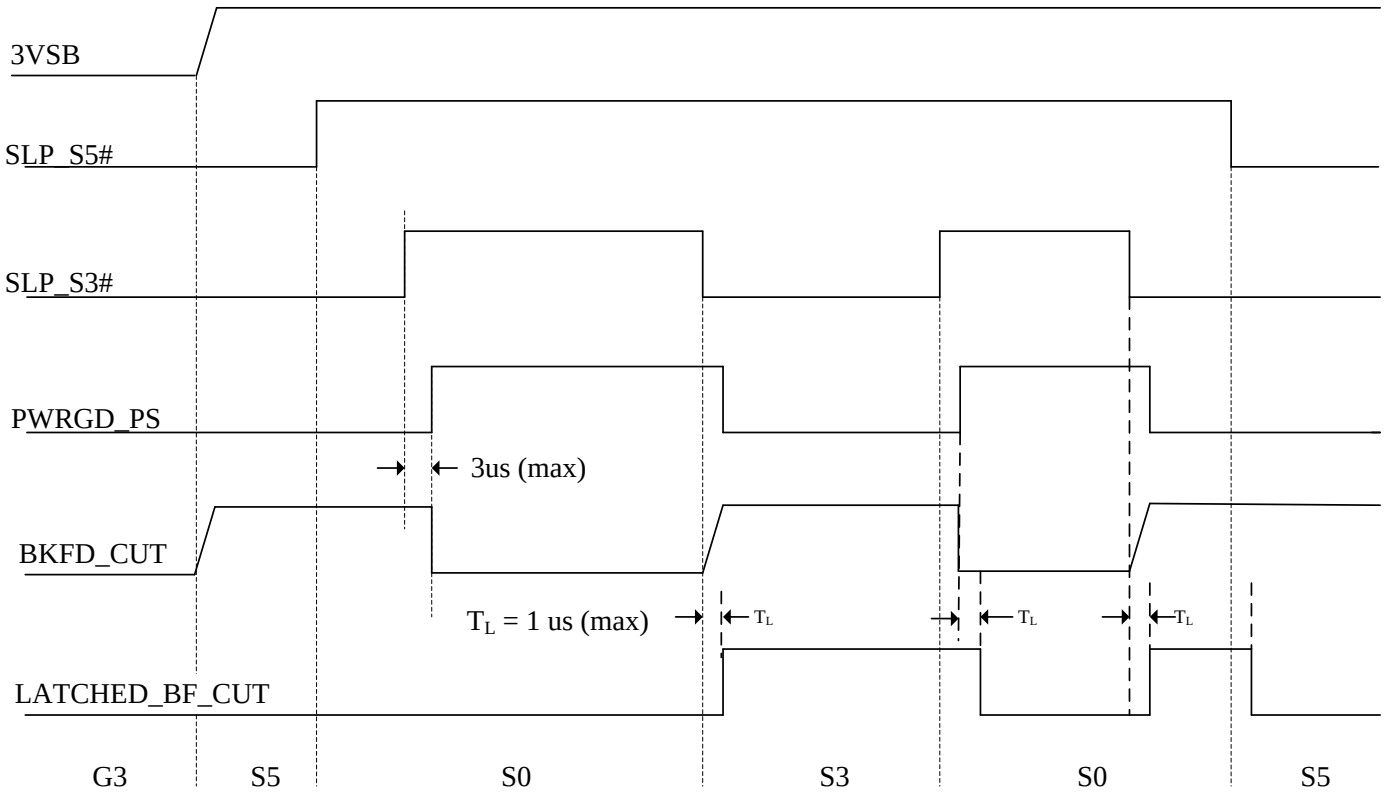


Figure 6-4 BKFD_CUT and LATCH_BKFD_CUT

BKFD_CUT (Backfeed_Cut) – When high, switches dual rails to standby power.

LATCH_BKFD_CUT (Latched_Backfeed_Cut) – When high, switches dual rails to standby power.

6.3 3VSBSW#

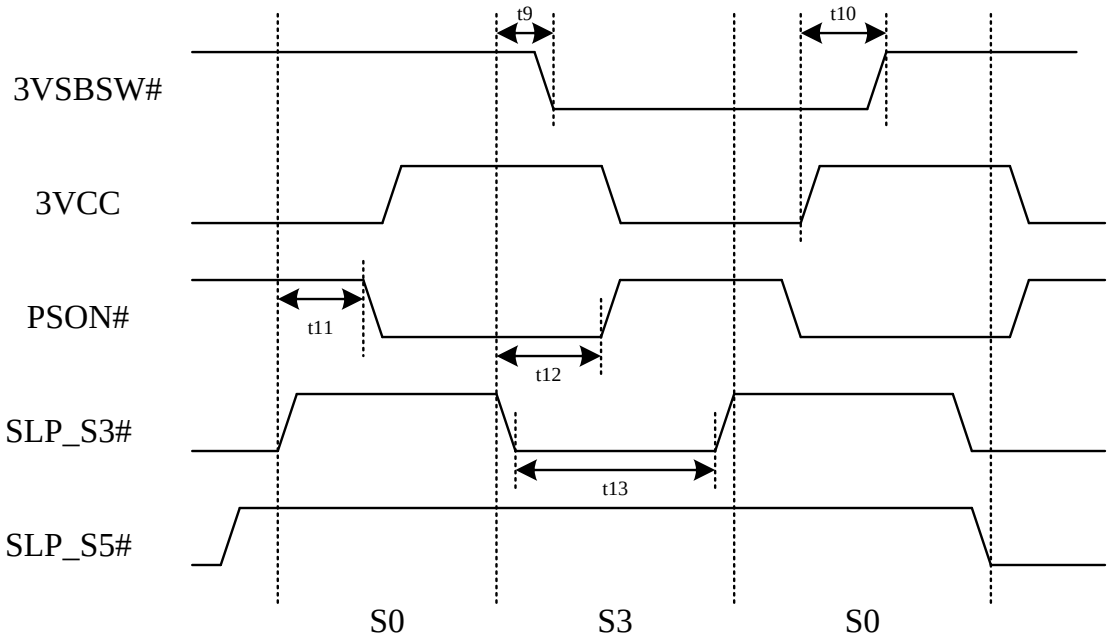


Figure 6-5 3VSBSW#

TIMING	PARAMETER	MIN	MAX	UNIT
t9	SLP_S3# active to 3VSBSW# active	0	10	mS
t10	3VCC active to 3VSBSW# inactive	120	190	mS
t11	SLP_S3# inactive to PSON# active	0	80	nS
t12	SLP_S3# active to PSON# inactive	15	45	mS
t13	SLP_S3# minimal Low Time	40	-	mS

6.4 PSON# Block Diagram

The PSON# function controls the main power on/off. The main power is turned on when PSON# is low. Please refer to the figure below.

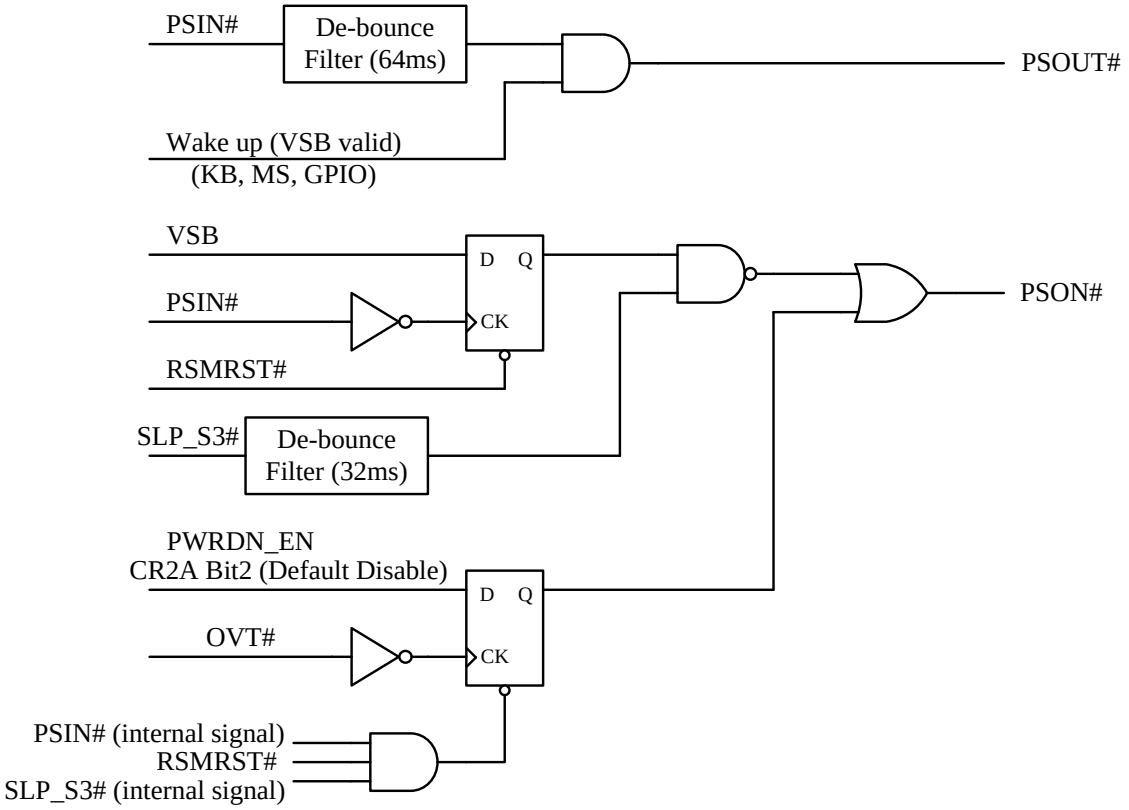
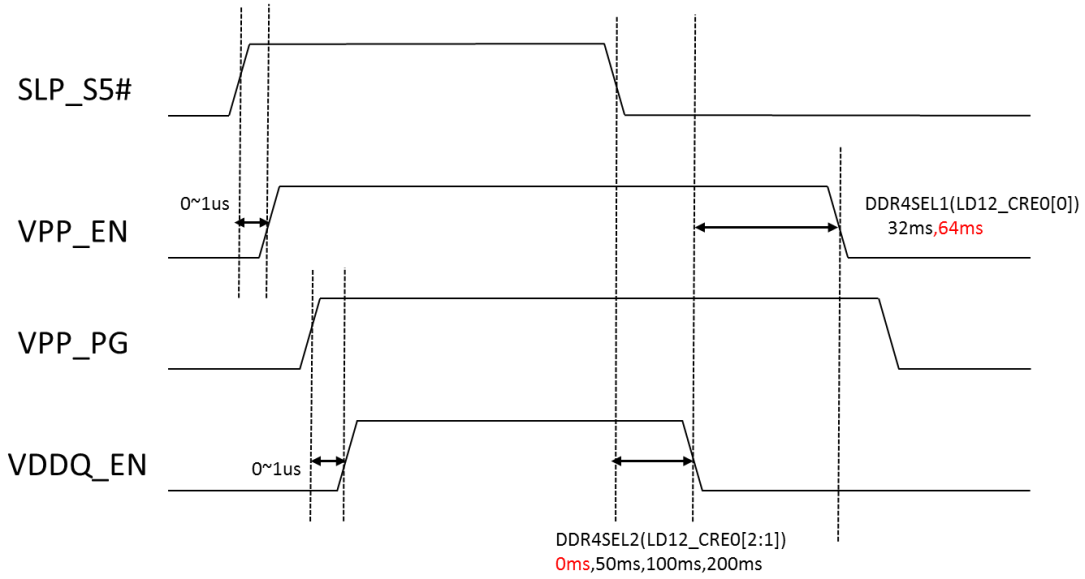


Figure 6-6 PSON# Block Diagram

6.5 DDR4 Power Sequence

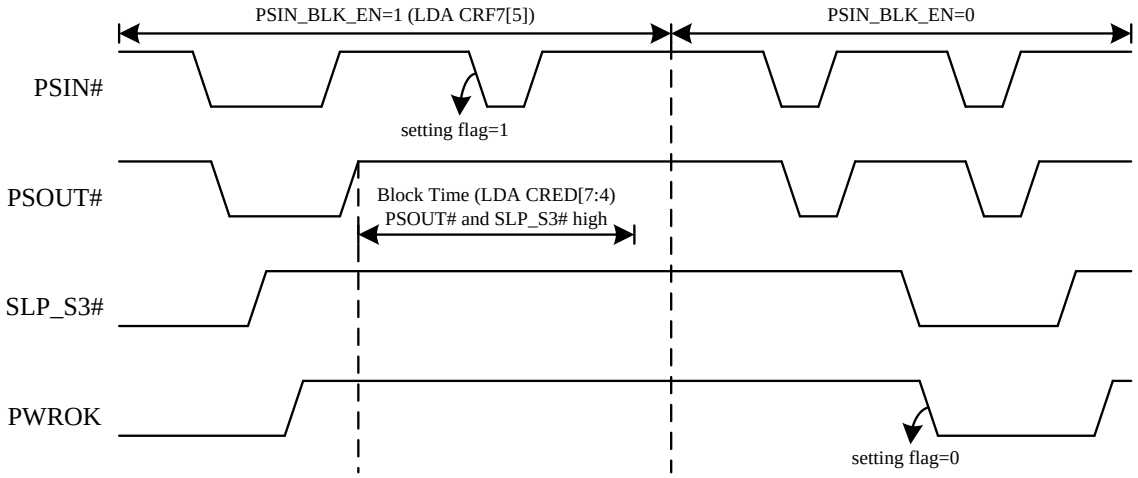
DDR4PWR is the power sequence control of DDR4 SDRAM. It is a high speed and low power platform. There are two timer register can be select in the sequence (DDR4SEL1: LDA CRE9 bit[7], DDR4SEL2: LDA CRE9 bit [6:5]).



6.6 PSIN#

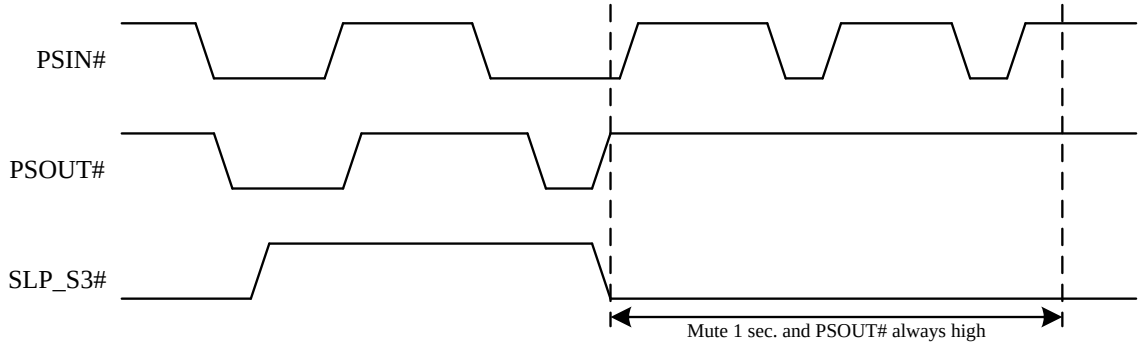
6.6.1 PSIN# Block Diagram (S5 -> S0)

When system is at S5 to S0 state, we add block time to avoid system enter S5 again by PSIN# glitch. The block time can be set by LDA_CRED[7:4] and the default is 0.5sec. If the glitch happen in the block time, the flag (LDA_CREC[2]) will set high and can be observe when user enter S0 state. The function need to set enable bit (LDA_CRF7[5]: PSIN_BLK_EN).



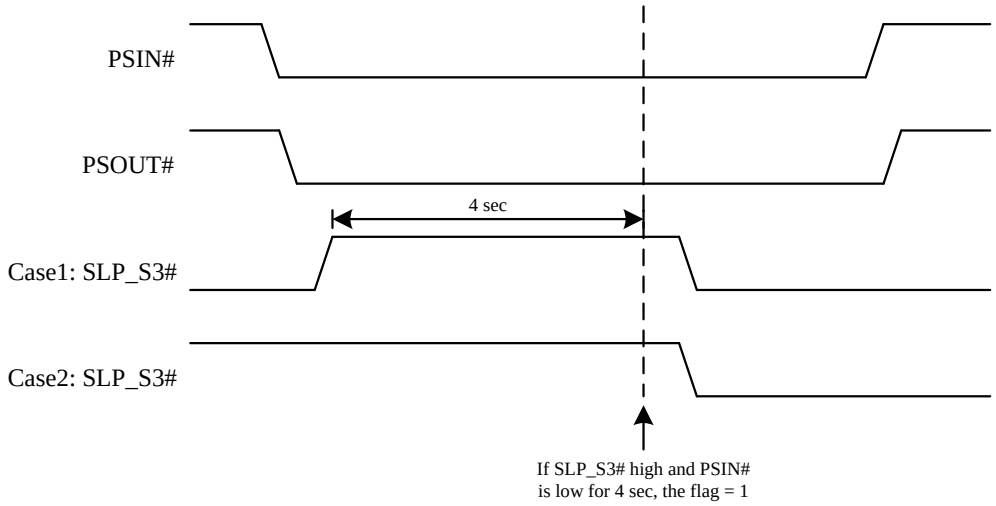
6.6.2 PSIN# Block 1sec Diagram (S0 -> S5)

When system is at S0 to S5 state, we add block 1 sec to avoid system enter S0 again by PSIN# glitch. The block time is fix and can't be set. The function need to set enable bit (LDA_CRF7[5]: PSIN_BLK_EN).



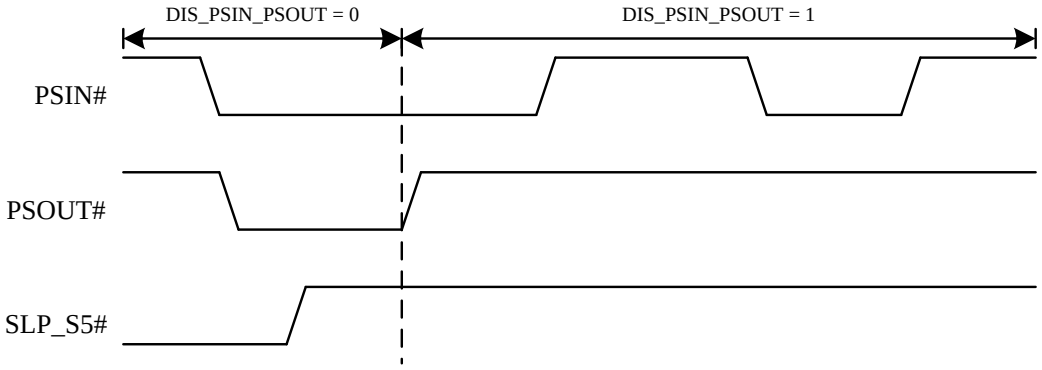
6.6.3 PSIN# 4sec Status Diagram

When user push PSIN button sustainably more than 4 sec, the system will enter S5 state and we have a flag to monitor (LDA_CREC[0]).



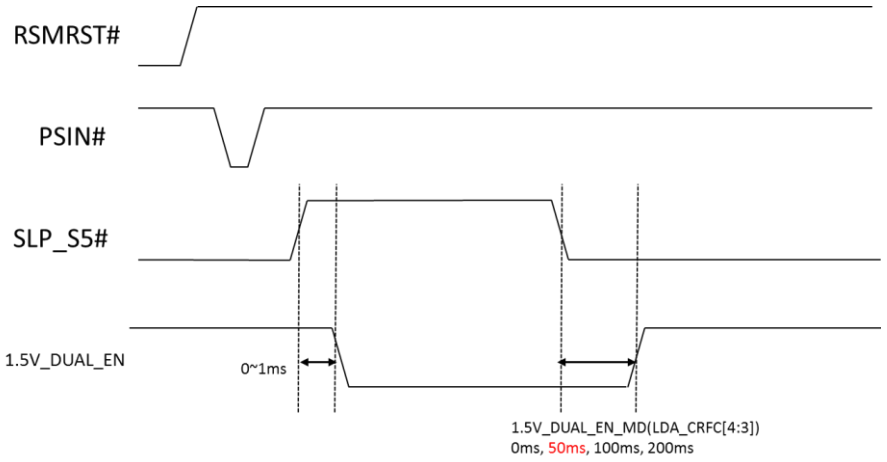
6.6.4 Disable PSIN# to PSOUT# Diagram

When system enter S0 from S5, user can monitor PSIN status by register (LDA_CREC[7]) for several application. For example, user can set DIS_PSIN_PSOUT (LDA_CREC[1]) to disconnect PSIN and PSOUT. If DIS_PSIN_PSOUT = 1, PSOUT will not follow PSIN. To avoid BIOS not clear this bit abnormally, it can be cleared automatically by PSIN rising signal to set LDA_CREC[3] = 1.



6.6.5 1.5V_Dual_En

1.5V_Dual_En is a power control to inverse SLP_S5# with a timer. As the figure below, when SLP_S5# go high, 1.5V_Dual_En will go low. when SLP_S5# go low, 1.5V_Dual_En will go high but with a distance. The timer can be control by register LDA_CRFC[4:3] and the default is 50ms.



6.7 PWROK

PWROK Signal indicates the main power (VCC Power) is valid. Besides, valid PWROK signal also requires the following conditions, as shown in the figure below.

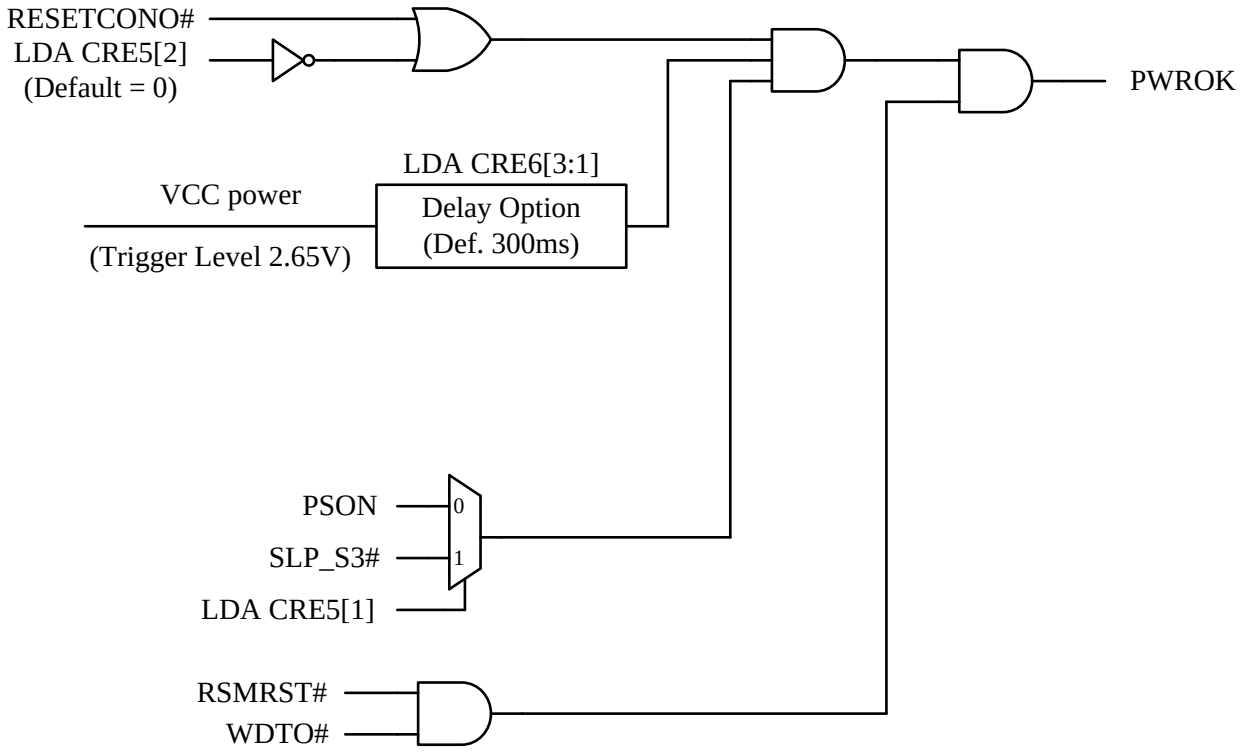


Figure 6-7 PWROK Block Diagram

6.8 Advanced Sleep State Control (ASSC) Function

Advanced Sleep State Control (ASSC) Function is used to control the system power at S3 or S5 state. The purpose of this function is to provide a method to reduce power consumption at S3 or S5 state. This function is disabled by default. When VCC power is first supplied, BIOS can program the register to enable ASSC Function. The register is powered by 3VSB_IO and some is powered by VBAT. The related registers are located at Logic Device 16 CRE0h ~ CRE3h.

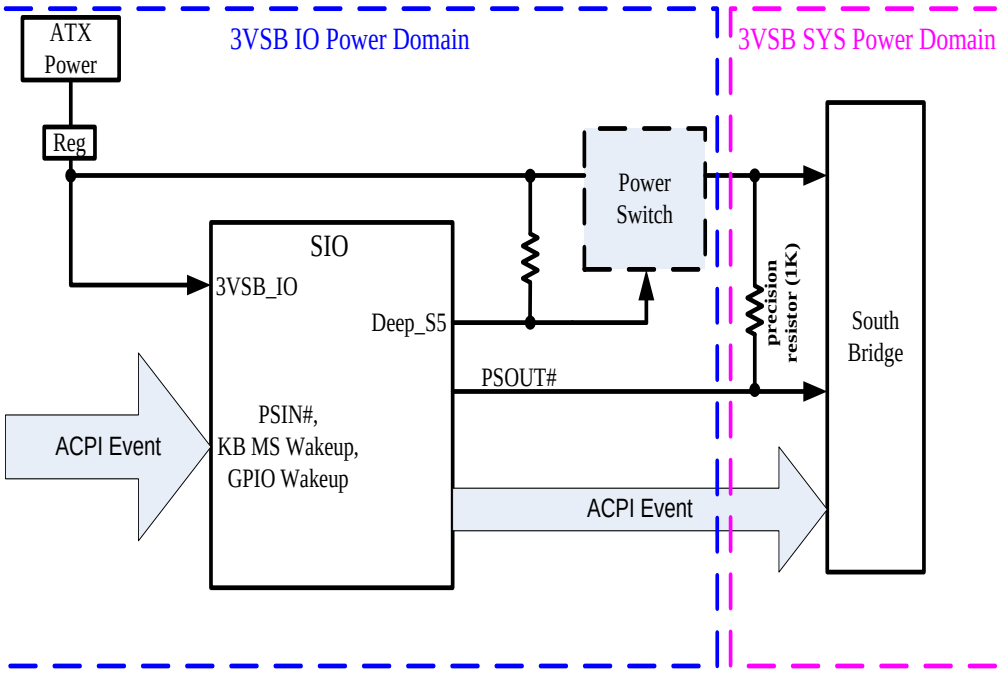
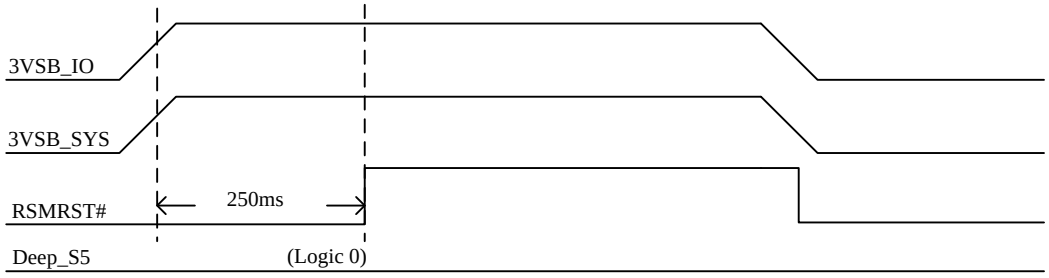


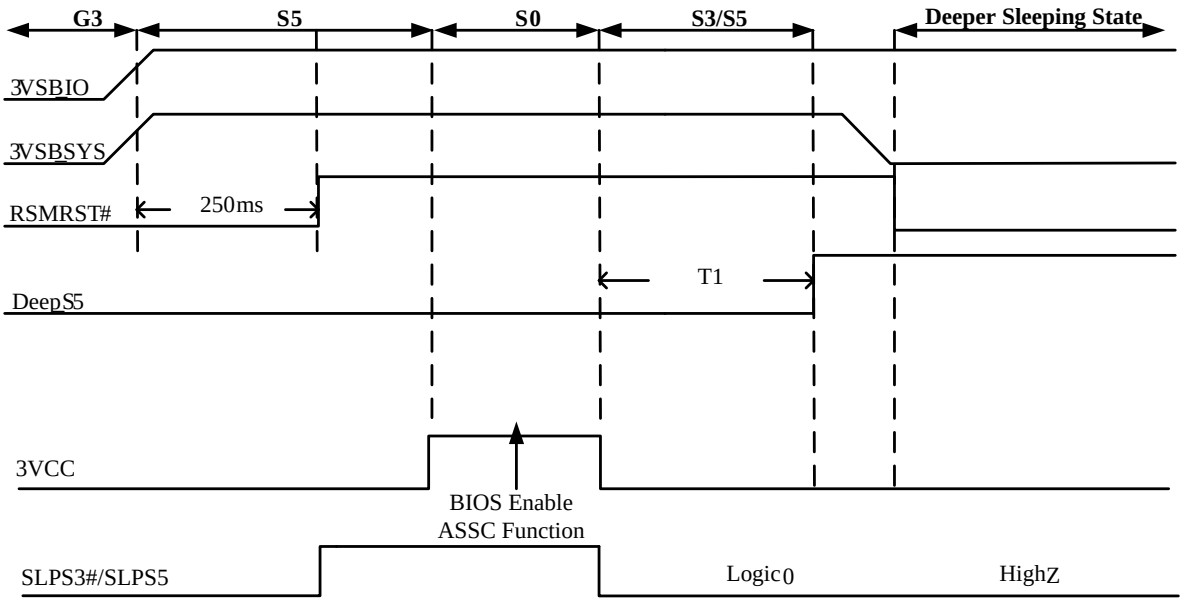
Figure 6-8 ASSC Application Diagram

6.8.1 When ASSC is disabled



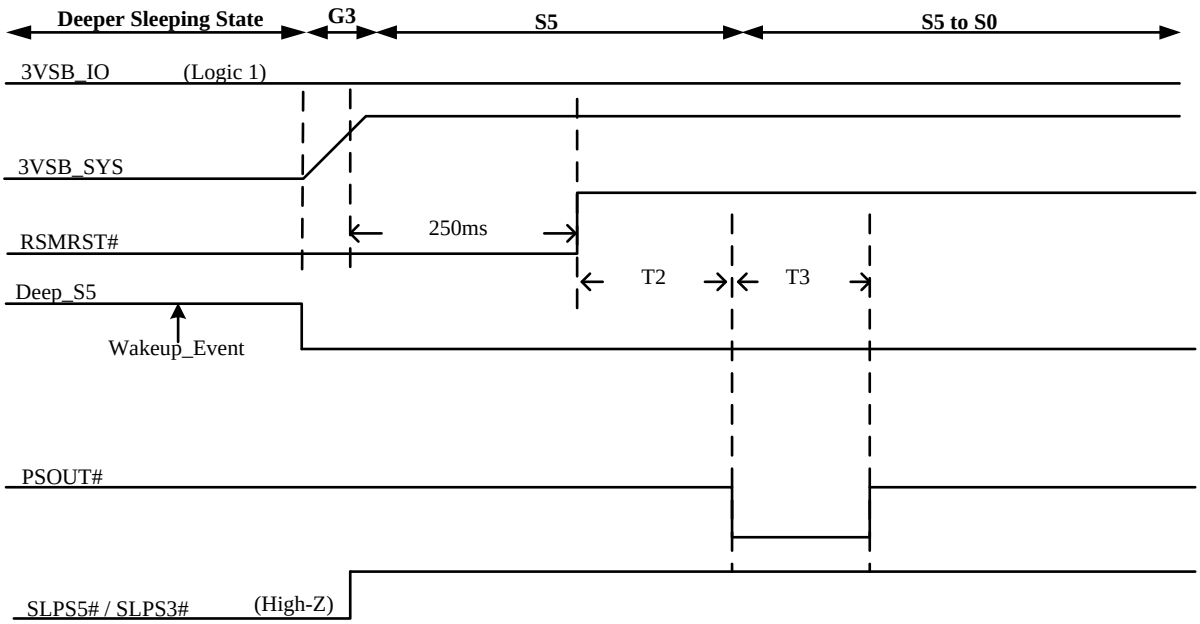
When ASSC is disabled, ACPI function is as same as the normal ACPI behavior.

6.8.2 When ASSC is enabled (Enter into Deeper Sleeping State)



When the first time AC plug in and enter into S0 State, BIOS can enable ASSC Function (DeepS3 or DeepS5), when the system enters S3/S5 state, the pin DEEP_S5 will be asserted after pre configuration delay time (power_off_dly_time, LD16 CRE2) to make the system entering the “Deeper Sleeping State (DSS)” where system’s VSB power is cut off. When pin DEEP_S5 asserts, the pin RSMRST# will de-assert by detecting PSOUT# signal (monitor 3VSB SYS Power).

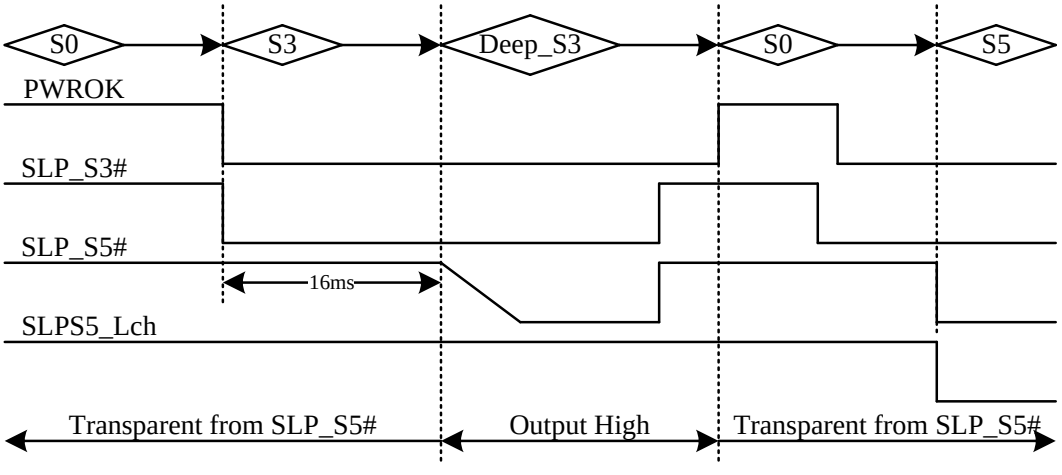
6.8.3 When ASSC is enabled (Exit Deeper Sleeping State)



When any Wakeup Event (PSIN#, KB MS Wakeup, GPIO Wakeup) happened, pin DEEP_S5 will be de-asserted to turn on the VSB power to the system. The pin RSMRST# will de-assert when 3VSB_SYS power reach valid voltage. And then the pin PSOUT# will issue a low pulse (T3) turn on the system after T2 time (wakeup delay time, LD16 CRE0). The PSOUT# low pulse is also programmable (LD16 CRE1). The T4 time is the delay from Deep_S5 ds-assert to Deeo_S5#_DELAY de-assert.

6.8.4 SLP_S5#_LATCH Control Function

SLP_S5#_LATCH control signal is similar to SLPS5# signal. When System is at S0 ~ S5 state, SLP_S5#_LATCH follows the SLPS5# signal. When system is at DeepS5 State, SLP_S5#_LATCH will keep low state till system returns to S0 state. When system is at DeepS3 State, SLP_S5#_LATCH will keep high till system returns to S0 state. Please see the following timing diagram:



7. CONFIGURATION REGISTER ACCESS PROTOCOL

The NCT5569D uses a special protocol to access configuration registers to set up different types of configurations. The NCT5569D has a total of 16 Logical Devices (from Logical Device 1 to Logical Device 16 with the exception of Logical Device 0, 1, 3, 4, 6, C, D, E, 10, 11, 12, 13, 14 & 15 for backward compatibility) corresponding to fourteen individual functions: UART A (Logical Device 2), Keyboard Controller (Logical Device 5), GPIO 7 & 8 (Logical Device 7), WDT1 & GPIO0 (Logical Device 8), GPIO 2, 3, 4, 5, 7 & 8 (Logical Device 9), ACPI (Logical Device A), Hardware Monitor & Front Panel LED (Logical Device B), GPIO (Logical Device F), and Deep Sleep (Logical Device 16).

It would require a large address space to access all of the logical device configuration registers if they were mapped into the normal PC address space. The NCT5569D, then, maps all the configuration registers through two I/O addresses (2Eh/2Fh or 4Eh/4Fh) set at power on by the strap pin 2E_4E_SEL. The two I/O addresses act as an index/data pair to read or write data to the Super I/O. One must write an index to the first I/O address which points to the register and read or write to the second address which acts as a data register.

An extra level of security is added by only allowing data updates when the Super I/O is in a special mode, called the Extended Function Mode. This mode is entered by two successive writes of 87h data to the first I/O address. This special mode ensures no false data can corrupt the Super I/O configuration during a program runaway.

There are a set of global registers located at index 0h – 2Fh, containing information and configuration for the entire chip.

The method to access the control registers of the individual logical devices is straightforward. Simply write the desired logical device number into the global register 07h. Subsequent accesses with indexes of 30h or higher are directly to the logical device registers.

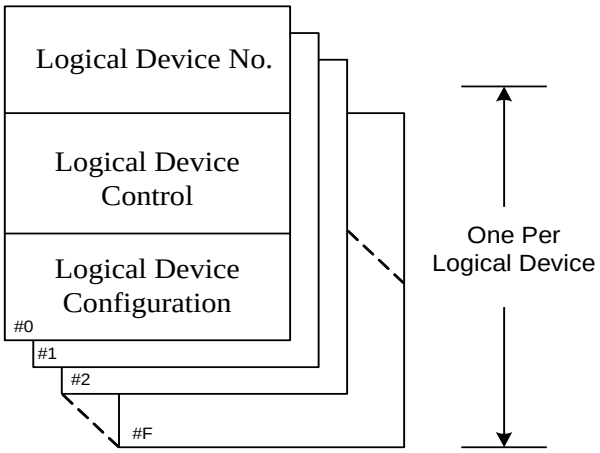


Figure 7-1 Structure of the Configuration Register

Table 7-1 Devices of I/O Base Address

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
0	Reserved	
1	Reserved	
2	UART A	100h ~ FF8h
3	Reserved	
4	Reserved	
5	Keyboard Controller	100h ~ FFFh
6	Reserved	
7	GPIO 7 & 8	Reserved
8	WDT1 ,GPIO 0	Reserved
9	GPIO 2, 3, 4, 5, 7 & 8	Reserved
A	ACPI	Reserved
B	Hardware Monitor & Front Panel LED	100h ~ FFEh
C	Reserved	
D	Reserved	
E	Reserved	
F	GPIO	Reserved
10	Reserved	
11	Reserved	
12	Reserved	
13	Reserved	
14	Reserved	
15	Reserved	
16	Deep Sleep	Reserved

7.1 Configuration Sequence

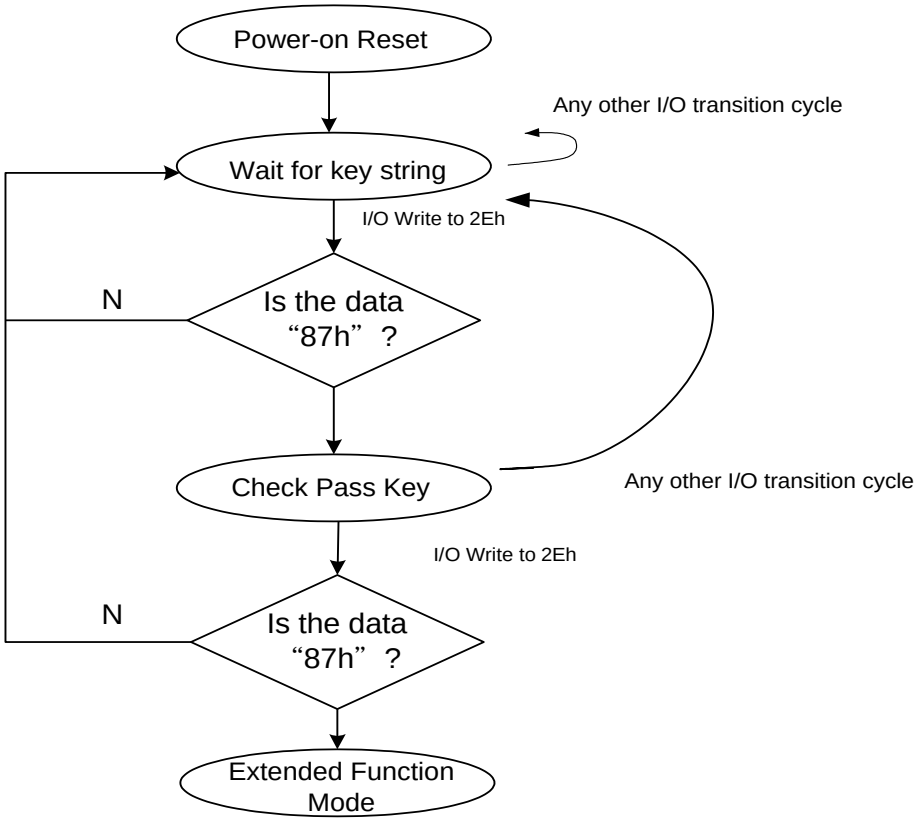


Figure 7-2 Configuration Register

To program the NCT5569D configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

(3). Exit the Extended Function Mode.

7.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

7.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

7.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

7.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR[26h] bit 6 showing the value of the strap pin at power on) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

This example programs the configuration register F0h (clock source) of logical device 1 (UART A) to the value of 3Ch (24MHz). First, one must enter the Extended Function Mode, then setting the Logical Device Number (Index 07h) to 01h. Then program index F0h to 3Ch. Finally, exit the Extended Function Mode.

```
;-----------------------------------------------------
; Enter the Extended Function Mode
;-----------------------------------------------------
MOV    DX, 2EH
MOV    AL, 87H
OUT    DX, AL
OUT    DX, AL
;--------------------------------------------------------------------------
; Configure Logical Device 1, Configuration Register CRF0
;--------------------------------------------------------------------------
MOV    DX, 2EH
MOV    AL, 07H
OUT    DX, AL          ; point to Logical Device Number Reg.
MOV    DX, 2FH
MOV    AL, 01H
OUT    DX, AL          ; select Logical Device 1
;
MOV    DX, 2EH
MOV    AL, F0H
OUT    DX, AL          ; select CRF0
MOV    DX, 2FH
MOV    AL, 3CH
OUT    DX, AL          ; update CRF0 with value 3CH
;-----------------------------------------------
; Exit the Extended Function Mode
;-----------------------------------------------
MOV    DX, 2EH
MOV    AL, AAH
OUT    DX, AL
```

8. HARDWARE MONITOR

8.1 General Description

The NCT5569D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures, all of which are very important for a high-end computer system to work stably and properly. In addition, proprietary hardware reduces the amount of programming and processor intervention to control cooling fan speeds, minimizing ambient noise and maximizing system temperature and reliability.

The NCT5569D can simultaneously monitor all of the following inputs:

- Eleven analog voltage inputs (five internal voltages VTT, VBAT, 3VSB, 3VCC and AVCC; six external voltage inputs)
- Three fan tachometer inputs
- Five remote temperatures, using either a thermistor or from the CPU thermal diode (voltage or Current Mode measurement method)

These inputs are converted to digital values using the integrated, eight-bit analog-to-digital converter (ADC).

In response to these inputs, the NCT5569D can generate the following outputs:

- Three fan outputs for the fan speed control
- SMI#
- OVT# signals for system protection events

The NCT5569D provides hardware access to all monitored parameters through the LPC interface and software access through application software, such as Nuvoton's Hardware Doctor™, or BIOS.

The rest of this section introduces the various features of the NCT5569D hardware-monitor capability. These features are divided into the following sections:

- Access Interfaces
- Analog Inputs
- TwoFan Speed Measurement and Control
- Smart Fan Control
- SMI# interrupt mode
- OVT# interrupt mode
- Registers and Value RAM

8.2 Access Interfaces

The NCT5569D provides interfaces LPC, for the microprocessor to read or write the internal registers of the hardware monitor.

8.3 LPC Interface

The internal registers of the hardware monitor block are accessible through two separate methods on the LPC bus. The first set of registers, which primarily enable the block and set its address in the CPU I/O address space are accessed by the Super I/O protocol described in Chapter 7 at address 2Eh/2Fh or 4Eh/4Fh. The bulk of the functionality and internal registers of this block are accessed form an index/data pair of CPU I/O addresses. The standard locations are usually 295h/296h and are set by CR[60h]&CR[61h] accessed using the Super I/O protocol as described in Chapter 7.

Due to the number of internal register, it is necessary to separate the register sets into "banks" specified by register 4Eh. The structure of the internal registers is shown in the following figure.

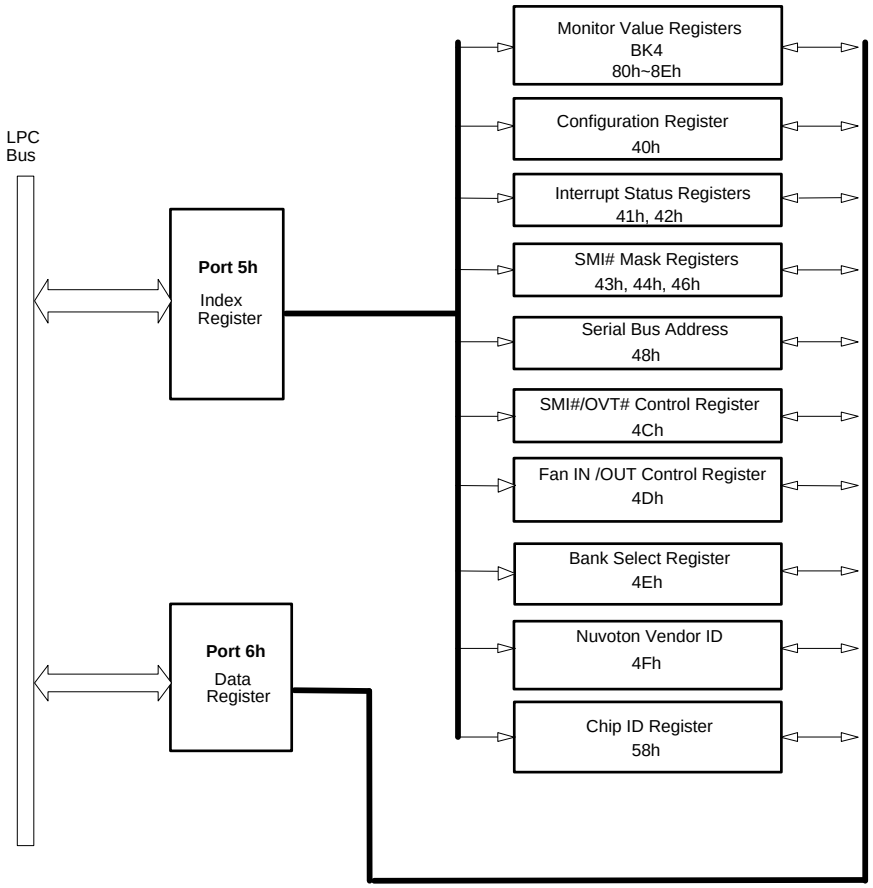


Figure 8-1 LPC Bus' Reads from / Write to Internal Registers

8.4 Analog Inputs

The analog inputs of the hardware monitor block connect to an 8-bit Analog to Digital Converter (ADC) and consist of 6 general-purpose inputs connected to external device pins and five internal signals connected to the power supplies (VTT, AVCC, VBAT, 3VSB and 3VCC). All inputs are limited to a maximum voltage of 2.048V due to an internal setting of 8mV LSB (256 steps x 8mV = 2.048V). All inputs to the ADC must limit the maximum voltage by using a voltage divider. The power supplies have internal resistors, while the external pins require outside limiting resistors as described below.

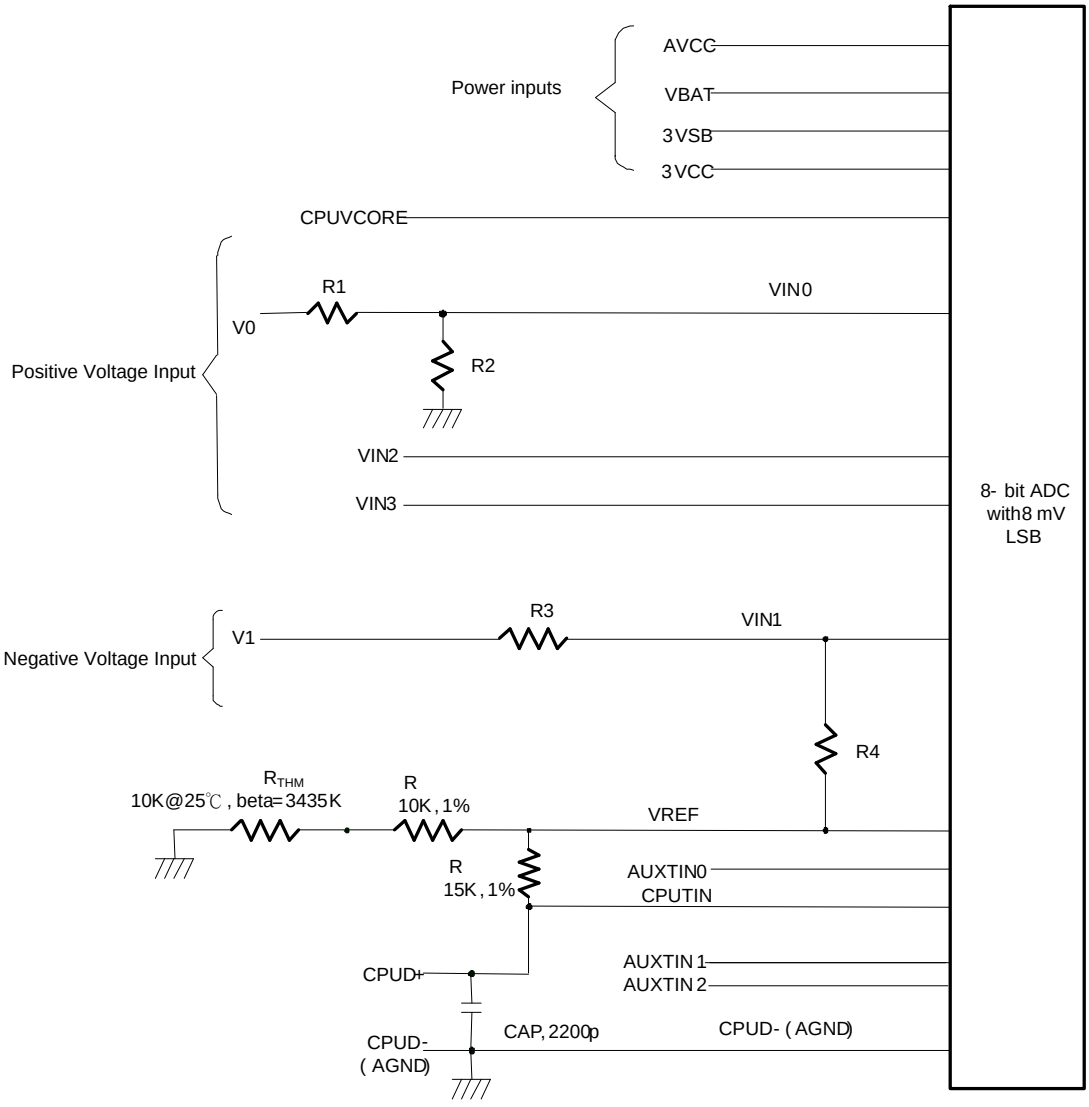


Figure 8-2 Analog Inputs and Application Circuit of the NCT5569D

As illustrated in the figure above, other connections may require some external circuits. The rest of this section provides more information about voltages outside the range of the 8-bit ADC, CPU Vcore voltage detection, and temperature sensing.

8.4.1 Voltages Over 2.048 V or Less Than 0 V

Input voltages greater than 2.048 V should be reduced by an external resistor divider to keep the input voltages in the proper range. For example, input voltage V_0 (+12 V) should be reduced before it is connected to VIN0 according to the following equation:

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

R1 and R2 can be set to 56 KΩ and 10 KΩ, respectively, to reduce V_0 from +12 V to less than 2.048 V.

All the internal inputs of the ADC, AVCC, VBAT, 3VSB and 3VCC utilize an integrated voltage divider with both resistors equal to 34KΩ, yielding a voltage one half of the power supply. Since one would expect a worst-case 10% variation or a 3.63V maximum voltage, the input to the ADC will be 1.815V, well within the maximum range.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \cong 1.65V$$, where VCC is set to 3.3V

The CPUVCORE pin feeds directly into the ADC with no voltage divider since the nominal voltage on this pin is only 1.2V.

Negative voltages are handled similarly, though the equation looks a little more complicated. For example, negative voltage V1 (-12V) can be reduced according to the following equation:

$$VIN1 = (V_1 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, where V_1 = -12$$

R3 and R4 can be set to 232 KΩ and 10 KΩ, respectively, to reduce negative input voltage V_1 from –12 V to less than 2.048 V. Note that R4 is referenced to VREF, or 2.048V instead of 0V to allow for more dynamic range. This is simply good analog practice to yield the most precise measurements.

Both of these solutions are illustrated in the figure above.

8.4.2 Voltage Data Format

The data format for voltage detection is an eight-bit value, and each unit represents an interval of 8 mV.

Detected Voltage = Reading * 0.008 V

If the source voltage was reduced by a voltage divider, the detected voltage value must be scaled accordingly.

8.4.2.1. Voltage Reading

NCT5569D has 11 voltage reading

	CPUVCORE	**VIN0**	**AVCC**	**3VCC**	**VIN1**
Voltage reading	IO_SPACE 00h	IO_SPACE 01h	IO_SPACE 02h	IO_SPACE 03h	IO_SPACE 04h
	VTT	**3VSB**	**VBAT**	**VIN4**	**VIN2**
Voltage reading	IO_SPACE 05h	IO_SPACE 06h	IO_SPACE 07h	IO_SPACE 08h	IO_SPACE 09h
	VIN3				
Voltage reading	IO_SPACE 0Ah				

8.4.3 Temperature Data Format

The data format for sensors CPUTIN and AUXTIN is 8-bit, two's-complement. This is illustrated in the table below. There are two sources of temperature data: external thermistors or thermal diodes.

Table 8-1 Temperature Data Format

TEMPERATURE	8-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX
+125°C	0111,1101	7Dh
+25°C	0001,1001	19h
+1°C	0000,0001	01h
+0.5°C	-	-
+0°C	0000,0000	00h
-0.5°C	-	-
-1°C	1111,1111	FFh
-25°C	1110,0111	E7h
-55°C	1100,1001	C9h

8.4.3.1. Monitor Temperature from Thermistor

External thermistors should have a β value of 3435K and a resistance of 10 KΩ at 25°C. As illustrated in the schematic above, the thermistor is connected in series with a 10-KΩ resistor and then connects to VREF (pin 53). The configuration registers to select a thermistor temperature sensor and the measurement method are found at Bank 0, index 5Dh.

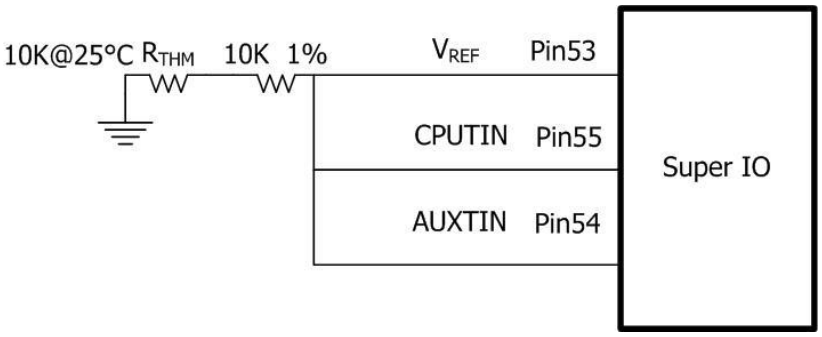


Figure 8-3 Monitoring Temperature from Thermistor

8.4.3.2. Monitor Temperature from Thermal Diode (Current Mode) mhwu

The NCT5569D can also sense the diode temperature through Current Mode and the circuit is shown in the following figure.

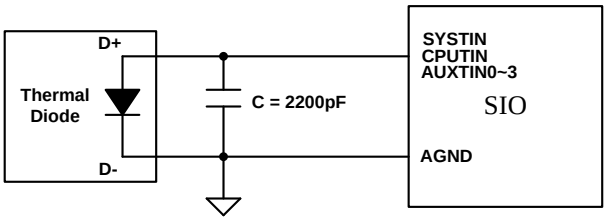


Figure 8-4 Monitoring Temperature from Thermal Diode (Current Mode)

The pin of processor D- is connected to CPUD- and the pin D+ is connected to temperature sensor pin in the NCT5569D. A bypass capacitor C=2200pF should be added to filter the high frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, index 5Dh and 5Eh.

8.4.3.3. Monitor Temperature from Thermal Diode (Voltage Mode)

The thermal diode D- pin is connected to AGND (pin 117), and the D+ pin is connected to the temperature sensor pin in the NCT5569D. A 15-KΩ resistor is connected to VREF to supply the bias current for the diode, and the 2200-pF, bypass capacitor is added to filter high-frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, index 5Dh.

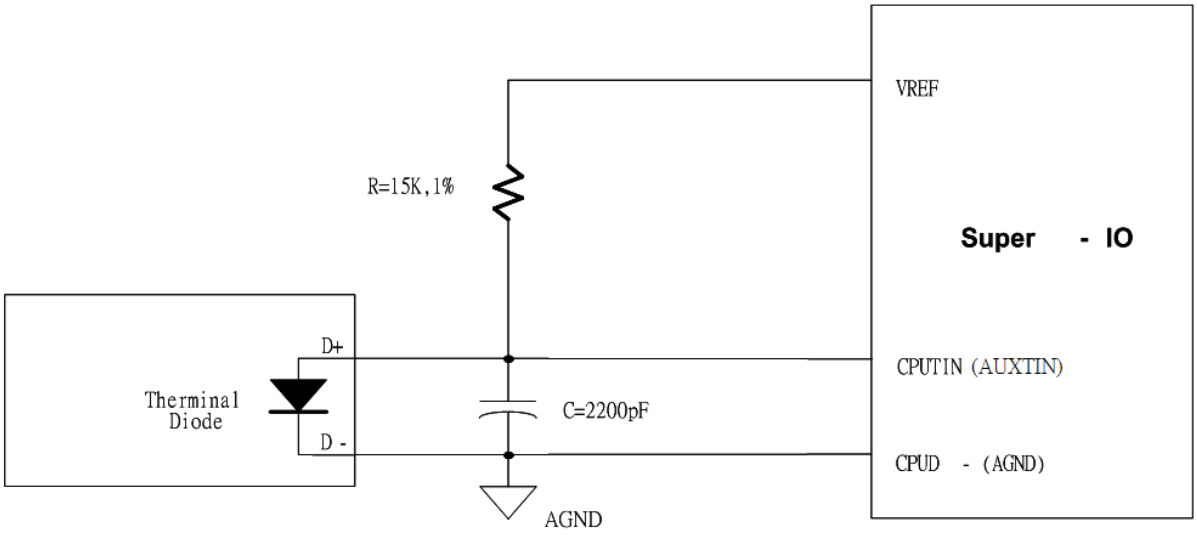


Figure 8-5 Monitoring Temperature from Thermal Diode (Voltage Mode)

8.4.3.4. Temperature Reading

NCT5569D has 2 temperature reading can monitor different temperature sources (ex. CPUTIN, AUXTIN, PECI…etc).

	SMIOVT1	**SMIOVT2**
Temperature source select	Bank6,index21 bit[2:0] default: CPUTIN	Bank6, index22 bit[2:0] default:AUXTIN
Temperature	Bank0, index27	Bank1, index50

reading		

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

8.5 PECI

PECI (Platform Environment Control Interface) is a new digital interface to read the CPU temperature of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECI uses a single wire for self-clocking and data transfer. By interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECI reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

PECI is one of the temperature sensing methods that the NCT5569D supports. The NCT5569D contains a PECI master and reads the CPU PECI temperature. The CPU is a PECI client.

The PECI temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECI temperatures. For further information, refer to the PECI specification. All references to "temperature" in this section are in "counts" instead of "°C".

Figure 8-6 PECI Temperature shows a typical fan speed (PWM duty cycle) and PECI temperature relationship.

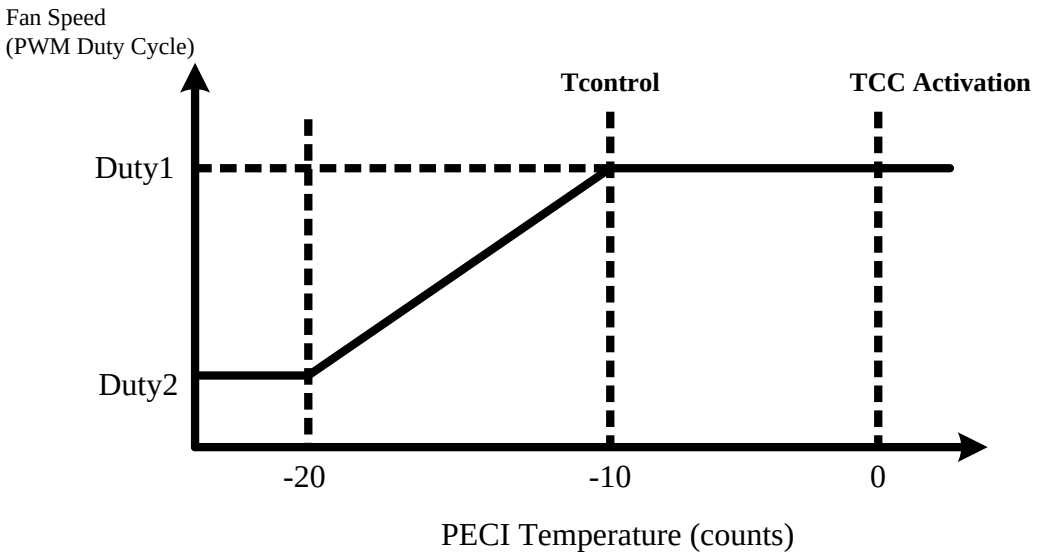


Figure 8-6 PECI Temperature

In this illustration, when PECI temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECI temperature is -10, the PWM duty cycle is at Duty1.

At Tcontrol PECI temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore Duty1 is 100% if this recommendation is followed. The value of Tcontrol can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The Tcontrol MSR address is usually in the BIOS Writer's guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, Tcontrol is -10.

When the PECI temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

The device also provides an offset register to 'shift' the negative PECI readings to positive values. The offset registers are called "Tbase", which are located at Bank7 Index 09h for Agent0 and Bank7 Index 0Ah for Agent1. All default values of these Tbase registers are 8'h00. The unit of the Tbase register contents is "count" to match that of PECI values. The resultant value (Tbase + PECI) should not be interpreted as the "temperature" (whether in count or °C) of the PECI client (CPU).

The Figure 8-7 Temperature and Fan Speed Relation after Tbase Offsets, shows the temperature and fan-speed relationship after Tbase offset is applied (based on Figure 8-6 PECI Temperature). This view is from the perspective of the NCT5569D fan control circuit.

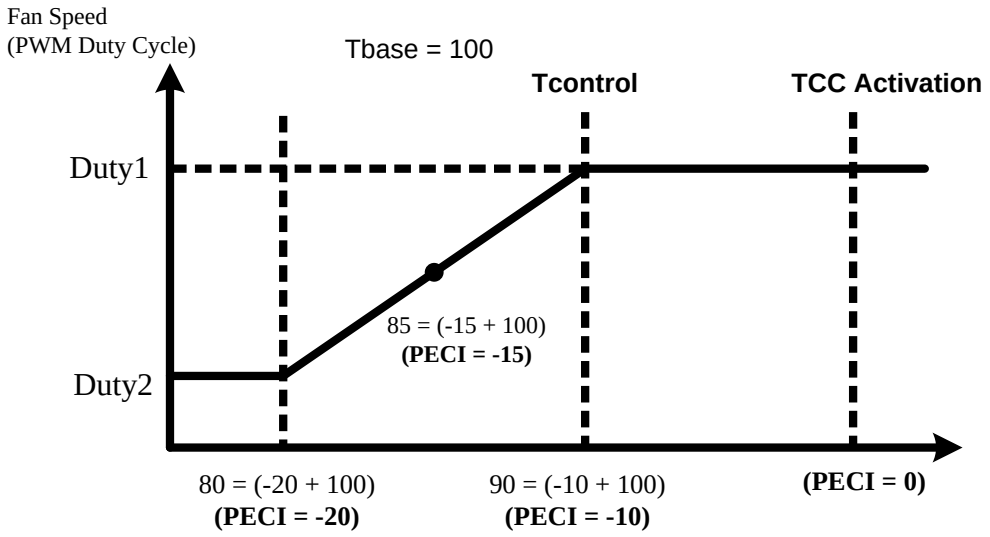


Figure 8-7 Temperature and Fan Speed Relation after Tbase Offsets

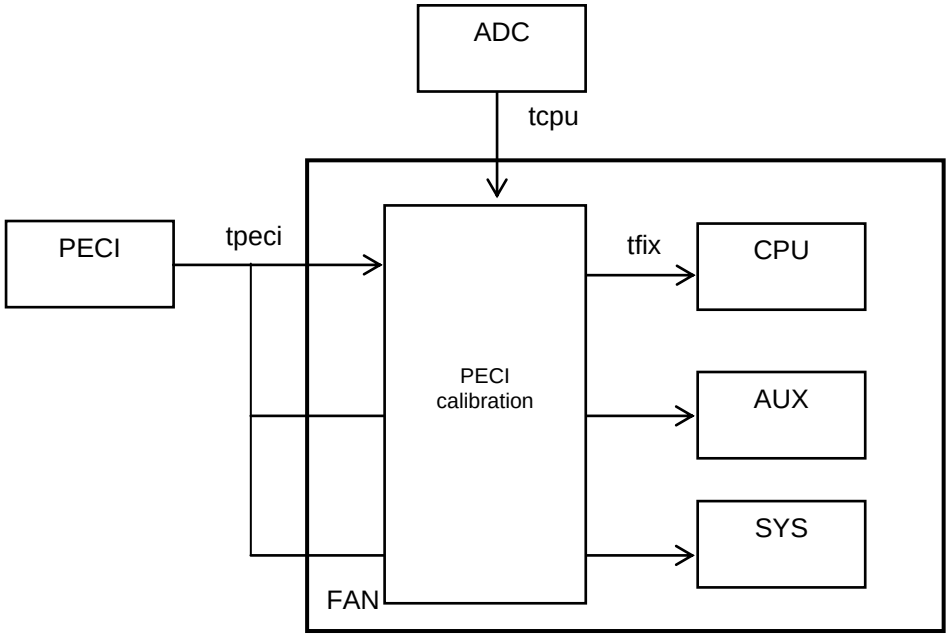
Assuming Tbase is set to 100 and the PECI temperature is -15 , the real-time temperature value to the fan control circuit will be 85 (-15 + 100). The value of 55 (hex) will appear in the relevant real-time temperature register.

While using Smart Fan control function of NCT5569D, BIOS/software can include Tbase in determining the thresholds (limits). In this example, assuming Tcontrol is -10 and Tbase is set to 100 (1), the threshold temperature value corresponding to the "100% fan duty-cycle" event is 90 (-10+100). The value of 5A (hex) should be written to the relevant threshold register.

Tcontrol is typically -10 to -20 for PECI-enabled CPUs. Base on that, a value of 85 ~100 for Tbase could be set for proper operation of the fan control circuit. This recommendation is applicable for most designs. In general, the concept presented in this section could be used to determine the optimum value of Tcontrol to match the specific application.

8.5.1 PECI Calibration

NCT5569D support PECI calibration to adjust the temperature read from CPU to thermistor because the source of thermistor is more accurate than PECI. We have several register for user to set. Bank4 Index FAh[0] is the enable bit for two agents. If user disable the function, the output will be the original source of PECI. Index FAh[7:4] is interval time for each calibrate, for example, every 0.1 sec (default) will calibrate again. Index F8h[7:3] is the max number of update times, number = 0 means only update 1 times. Index F8h[2:0] is the unit step, unit = 0 means 1 degree. We have the overflow and underflow mechanism to protect the system.



8.6 Fan Speed Measurement and Control

This section is divided into two parts, one to measure the speed and one to control the speed.

8.6.1 Fan Speed Reading

The fan speed reading at:

	FAN COUNT READING		FAN RPM READING	
	13-bit		16-bit	
	[12:5]	[4:0]	[15:8]	[7:0]
SYSFANIN	IO space, index 2E	IO space, index 2F	IO space, index3A	IO space, index 3B
CPUFANIN	IO space, index 30	IO space, index 31	IO space, index 3C	IO space, index 3D
AUXFANIN0	IO space, index 32	IO space, index 33	IO space, index 3E	IO space, index 3F

8.6.2 Fan Speed Calculation by Fan Count Reading

In 13-bit fan count reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count}$$

8.6.3 Fan Speed Calculation by Fan RPM Reading

In 16-bit fan RPM reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by translating 16-bit RPM reading from hexadecimal to decimal.

Register reading 0x09C4h = 2500 RPM

8.6.4 Fan Speed Control

The NCT5569D has three output pins for fan control.

	SYSFANOUT	CPUFANOUT	AUXFANOUT0
Output Type Select (in PWM output)	CR24 bit[4] 0: open-drain (default) 1: push-pull	CR24 bit[3] 0: open-drain (default) 1: push-pull	CR24 bit[5] 0: open-drain (default) 1: push-pull
PWM Output Freqency	Bank0, index00	Bank0, index02	Bank0, index10
Fan Control Mode Select	Bank1, index02, bit[7:4] 0h: Manual mode (def.) 4h: SMART FAN IV	Bank2, index02, bit[7:4] 0h: Manual mode(def.) 4h: SMART FAN IV	Bank3, index02, bit[7:4] 0h: Manual mode (def.) 4h: SMART FAN IV
Output Value (write)	Bank1, index09 bit[7:0]	Bank2, index09 bit[7:0]	Bank3, index09 bit[7:0]
Current Output Value (read only)	IO space, index 4C	IO space, index 4D	IO space, index 4E

For PWM, the duty cycle is programmed by eight-bit registers at Bank1 Index 09h for SYSFANOUT, Bank2 Index

09h for CPUFANOUT, Bank3 Index 09h for AUXFANOUT0, The duty cycle can be calculated using the following equation:

$$\text{Duty cycle}(\%) = \frac{\text{Programmed 8-bit Register Value}}{255} \times 100\%$$

The default duty cycle is 7Fh, or 50% for SYSFANOUT and CPUFANOUT, duty cycle is FFh, or 100% for AUXFANOUT0.

Note.The default speed of fan output is specified in registers CR[E0h] to CR[E2h] of Logical Device B.

The PWM clock frequency is programmed at Bank0 Index 00h, Index 02h, Index 10.

8.6.5 SMART FAN™ Control

The NCT5569D supports various different fan control features:

- SMART FAN™ IV
- SMART FAN™ IV Close-Loop Fan Control RPM mode

	SYSFANOUT	CPUFANOUT	AUXFANOUT0
Fan Control Mode Select	Bank1, index02, bit[7:4] 0h: Manual mode (def.) 4h: SMART FAN IV	Bank2, index02, bit[7:4] 0h: Manual mode(def.) 4h: SMART FAN IV	Bank3, index02, bit[7:4] 0h: Manual mode (def.) 4h: SMART FAN IV

8.6.6 Temperature Source & Reading for Fan Control

Select temperature source for each fan control output:

	SYSFANOUT	CPUFANOUT	AUXFANOUT0
Fan Control Temperature Source Select	Bank1, index00 bit[4:0] Default: CPUTIN	Bank2, index00 bit[4:0] Default: AUXTIN	Bank3, index00 bit[4:0] Default: CPUTIN
Fan Control Temperature Reading	IO space, index 19	IO space, index 1A	IO space, index 1B

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

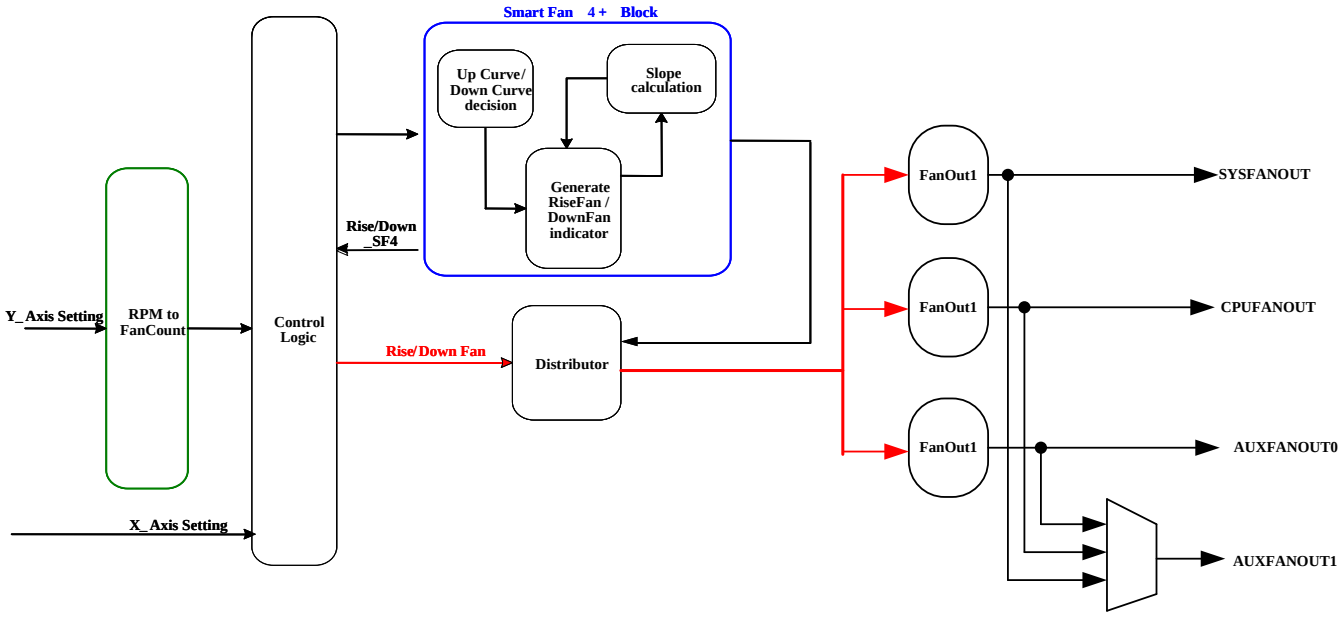


Figure 8-8 SMART FAN™ Function Block Diagram

8.7 SMART FAN™ IV & Close Loop Fan Control Mode

SMART FAN™ IV and Close Loop Fan Control Mode offer 3 slopes to control the fan speed.

Set **Critical Temperature, Bank1 Index 35_{HEX} , Bank2 Index 35_{HEX} , Bank3 Index 35_{HEX}.**

- Set the **Relative Register-at SMART FAN™ IV Control Mode Table**
  If fan control mode is set as Close Loop Fan Control, the unit step is 50RPM. So the maximum controllable RPM is 50*255=12,750RPM.
- Set Tolerance **of Target Temperature, Bank1 Index 02_{HEX} bit[2:0] . Bank2 Index 02_{HEX} bit[2:0]. Bank3 Index 02_{HEX} bit[2:0].**

The 3 slopes can be obtained by setting FanDuty1/RPM1~FanDuty4/RPM4 and T1~T4 through the registers. When the temperature rises, FAN Output will calculate the target FanDuty/RPM based on the current slope. For example, assuming Tx is the current temperature and Ty is the target, then

The slope:

$$X2 = \frac{(FanDuty3/RPM3) - (FanDuty2/RPM2)}{(T3 - T2)}$$

Fan Output:

$$Target\ FanDuty\ or\ RPM = (FanDuty2\ or\ RPM2) + (Tx - T2) \cdot X2$$

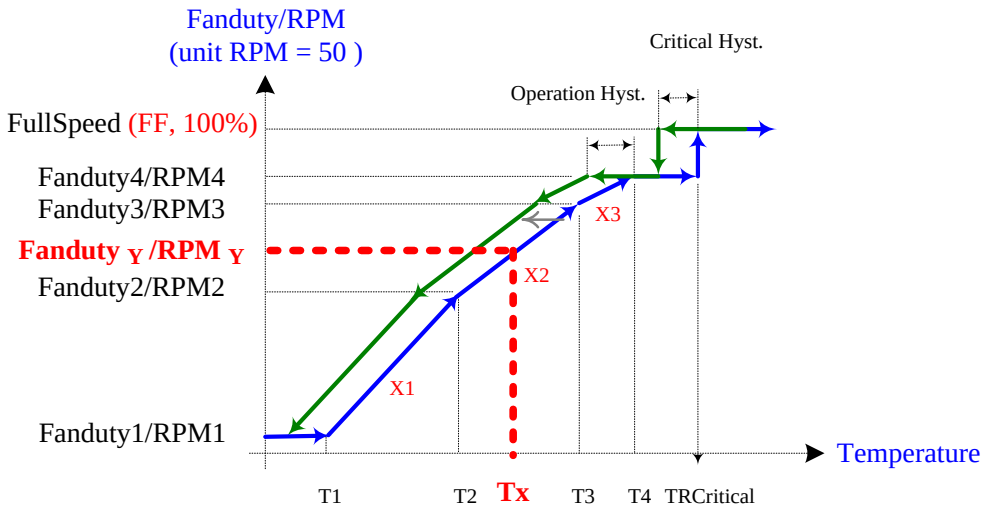


Figure 8-9 SMART FAN™ IV & Close Loop Fan Control Mechanism

Table 8-2 Relative Register-at SMART FAN™ IV Control Mode

DESCRIPTION	T1	T2	T3	T4
SYSFANOUT	Bank 1, Index 21h	Bank 1, Index 22h	Bank 1, Index 23h	Bank 1, Index 24h
CPUFANOUT	Bank 2, Index 21h	Bank 2, Index 22h	Bank 2, Index 23h	Bank 2, Index 24h
AUXFANOUT0	Bank 3, Index 21h	Bank 3, Index 22h	Bank 3, Index 23h	Bank 3, Index 24h
DESCRIPTION	**FD1/PWM1**	**FD2/PWM2**	**FD3/PWM3**	**FD4/PWM4**
SYSFANOUT	Bank 1, Index 27h	Bank 1, Index 28h	Bank 1, Index 29h	Bank 1, Index 2Ah
CPUFANOUT	Bank 2, Index 27h	Bank 2, Index 28h	Bank 2, Index 29h	Bank 2, Index 2Ah

DESCRIPTION	STEP- UP TIME	STEP-DOWN TIME	Enable SMART FAN IV	ENABLE CRITICAL DUTY	CRITICAL DUTY
SYSFANOUT	Bank 1, index 03h	Bank 1, index 04h	Bank 1, Index 02h bit[7:4] = 04h	Bank 1, Index 36h, Bit0	Bank 1, index 37h
CPUFANOUT	Bank 2, index 03h	Bank 2, index 04h	Bank 2, Index 02h bit[7:4] = 04h	Bank 2, Index 36h, Bit0	Bank 2, index 37h
AUXFANOUT0	Bank 3, index 03h	Bank 3, index 04h	Bank 3, Index 02h bit[7:4] = 04h	Bank 3, Index 36h, Bit0	Bank 3, index 37h

DESCRIPTION	T1	T2	T3	T4
AUXFANOUT0	Bank 3, Index 27h	Bank 3, Index 28h	Bank 3, Index 29h	Bank 3, Index 2Ah

DESCRIPTION	CRITICAL TEMPERATURE	CRITICAL TOLERANCE	TEMPERATURE TOLERANCE	STEP DOWN VALUE	ENABLE RPM MODE	RPM TOLERANCE	ENABLE RPM HIGH MODE
SYSFANOUT	Bank 1, Index 35h	Bank 1, Index 38h, bit[2:0]	Bank 1, Index 02h, bit[2:0]	Bank1, index66 Bit[3:0]	Bank 6, Index 00h, Bit0	Bank 6, index 01h	Bank 6, Index 06h, Bit0
CPUFANOUT	Bank 2, Index 35h	Bank 2, Index 38h, bit[2:0]	Bank 2, Index 02h, bit[2:0]	Bank2, index66 Bit[3:0]	Bank 6, Index 00h, Bit1	Bank 6, index 02h	Bank 6, Index 06h, Bit1
AUXFANOUT0	Bank 3, Index 35h	Bank 3, Index 38h, bit[2:0]	Bank 3, Index 02h, bit[2:0]	Bank3, index66 Bit[3:0]	Bank 6, Index 00h, Bit2	Bank 6, index 03h	Bank 6, Index 06h, Bit2

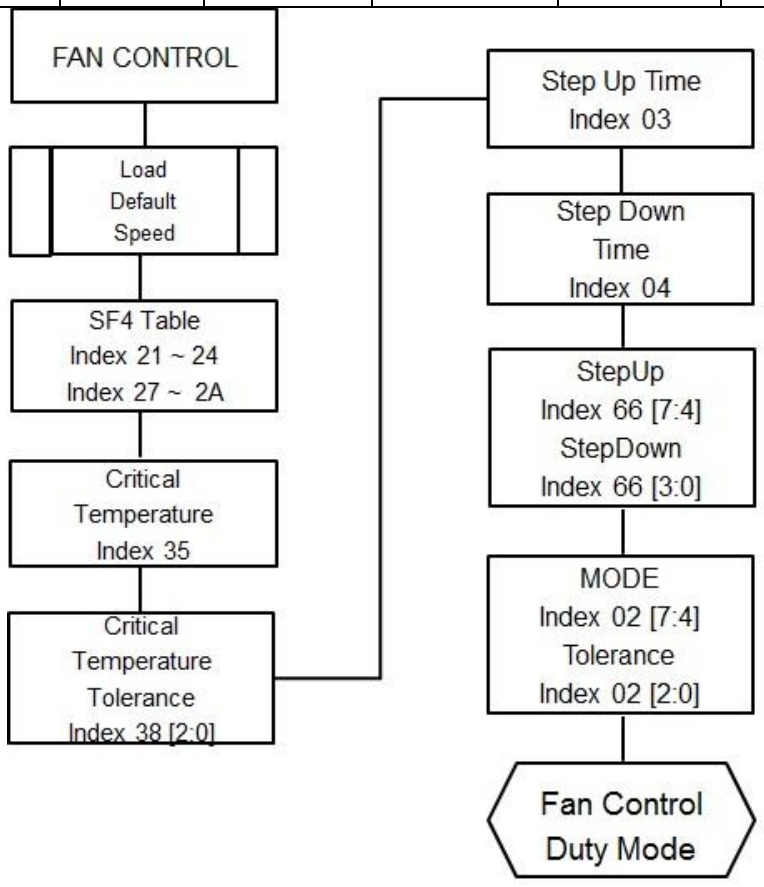


Figure 8-10 Fan Control Duty Mode Programming Flow

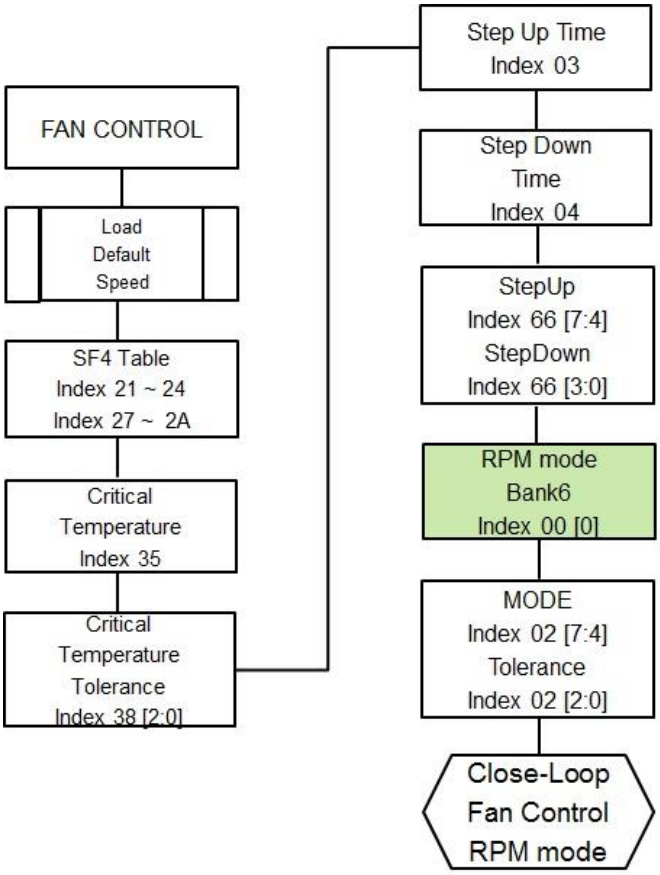


Figure 8-11 Close-Loop Fan Control RPM mode Programming Flow

8.7.1 Step Up Time / Step Down Time

SMART FAN™ IV is designed for the smooth operation of the fan. The Up Time / Down Time register defines the time interval between successive duty increases or decreases. If this value is set too small, the fan will not have enough time to speed up after tuning the duty and sometimes may result in unstable fan speed. On the other hand, if Up Time / Down Time is set too large, the fan may not work fast enough to dissipate the heat.

8.7.2 Fan Output Step

The “Fanout Step” itself is separately specified in Bank1 Index66h for SYSFANOUT, Bank2 Index66h for CPUFANOUT, Bank3 Index66h for AUXFANOUT0.

This example for Fanout Step exposition:

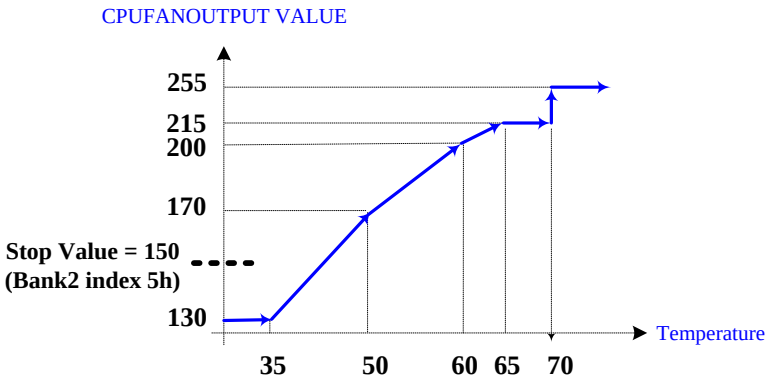


Figure 8-12 CPUFAN SMART FAN™ IV Table Parameters Figure

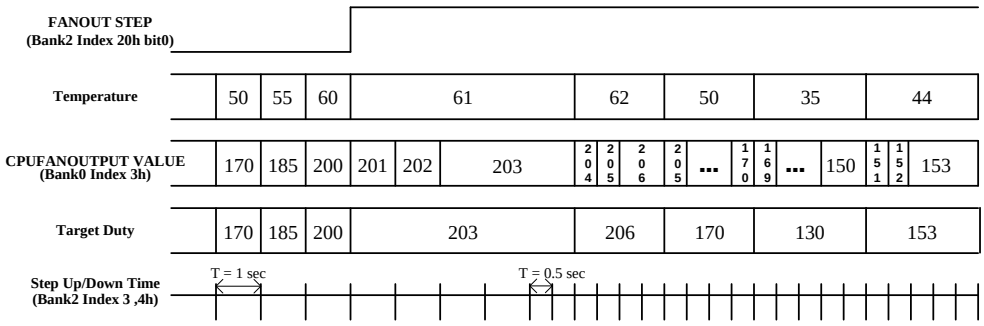


Figure 8-13 Fanout Step Relation of CPUFANOUT

8.7.3 Revolution Pulse Selection

The NCT5569D supports four RPM output of the pulses selection function for different type of FAN which has the character of different pulses per revolution.The others could be set by HM register at Bank6, Index44, Bit1-0 for SYSFANIN; Index45, Bit1-0 for CPUFANIN; Index46, Bit1-0 for AUXFANIN0. All default value of pulse selection registers are 2 pulses of one revolution.

Setting description for “Pulse Selections Bits”:

00: 4 pulses per revolution
01: 1 pulse per revolution
10: 2 pulses per revolution (default)
11: 3 pulses per revolution

8.7.4 Weight Value Control

The NCT5569D supports weight value control for fan duty output. By register configuration, the results of weight value circuit can be added to the fan duty of SMART FAN™ IV and output to the fan. Take CPUFANOUT for example, if SMART FAN™ IV is selected, CPUTIN is the temperature source, and weight value control is enabled, SMART FAN™ IV will calculate the output duty, and weight value circuit will calculate the corresponding weight value based on CPUTIN. As the CPUTIN temperature rises, its corresponding weight value increases. Then, the two values will be summed up and output to CPU fan. In other words, the CPU fan duty is affected not only by the CPUTIN but also the CPUTIN temperature.

Figure 8-14 SYS TEMP and Weight Value Relations shows the relation between the CPUTIN temperature and the weight value. Tolerance setup is offered on each change point to avoid weight value fluctuation resulted from CPUTIN temperature change. The weight value will increase by one weight value step only when the CPUTIN temperature is higher than the point value plus tolerance. Likewise, the weight value decreases by one weight value step only when the CPUTIN temperature is lower than the point value minus tolerance.

Nots：This relative register should not be zero and not support negative temperature.

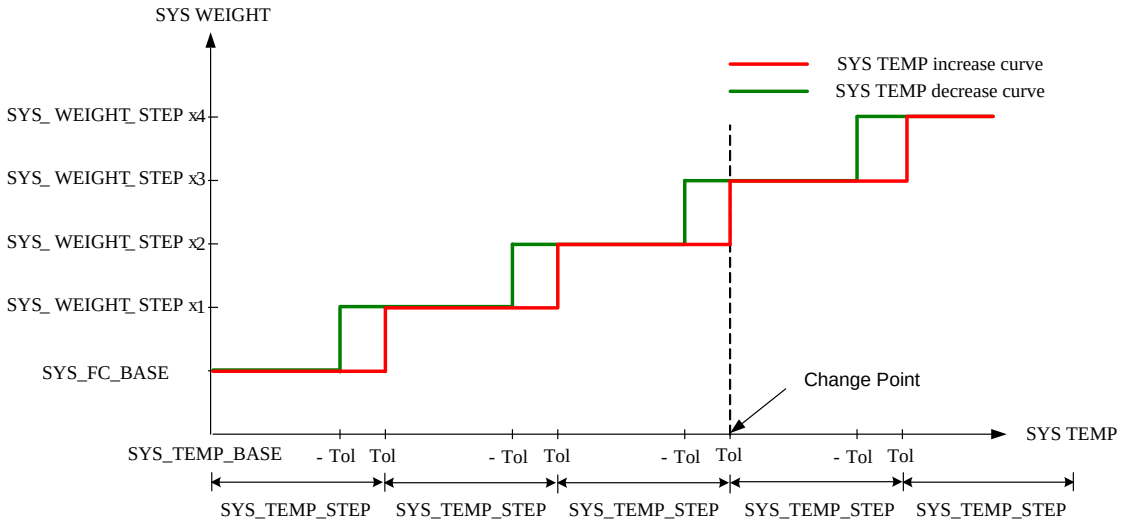


Figure 8-14 SYS TEMP and Weight Value Relations

Table 8-3 Relative Register-at Weight Value Control

DESCRIPTION	ENABLE WEIGHT MODE	WEIGHT TEMPERATURE SOURCE SELECT
CPUFANOUT	Bank 2, Index 39h, bit7	Bank 2, Index 39h, bit[1:0]

DESCRIPTION	TEMP BASE	DUTY BASE	TEMP STEP	TEMP STEP TOLERANCE	WEIGHT STEP
CPUFANOUT	Bank 2, Index 3Dh	Bank 2, Index 3Eh	Bank 2, Index 3Ah	Bank 2, Index 3Bh	Bank 2, Index 3Ch

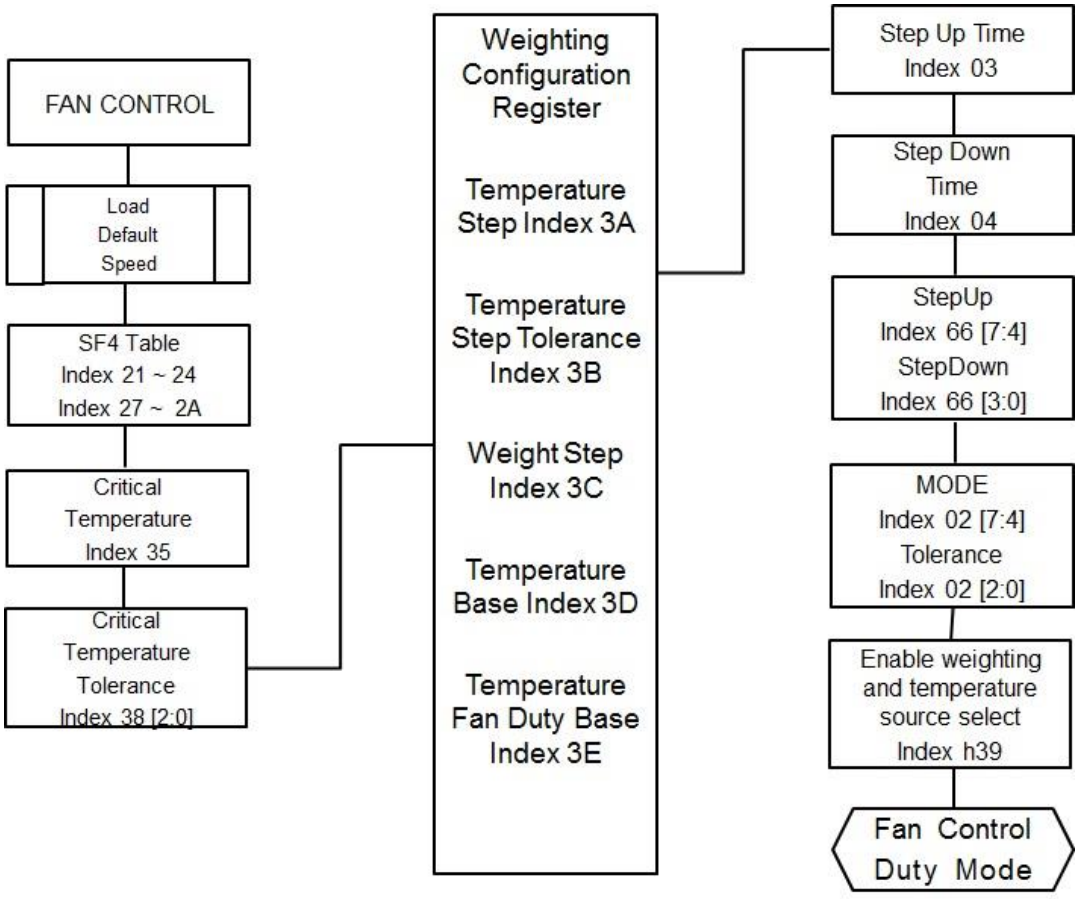


Figure 8-15 Fan Control Weighting Duty Mode Programming Flow

8.8 Alert and Interrupt

NCT5569D supports 2 Temperature Sensors for interrupt detection depending on selective monitor temperature source.

	SMIOVT1	**SMIOVT2**
Temperature source select	Bank6, index21 bit[2:0] default: CPUTIN	Bank6, index22 bit[2:0] default: AUXTIN2
Temperature reading (2's complement)	Bank0, index27	Bank1, index50
Temperature High Limit	Bank6, index50	Bank6, index52
Temperature Low Limit	Bank6, index51	Bank6, index53

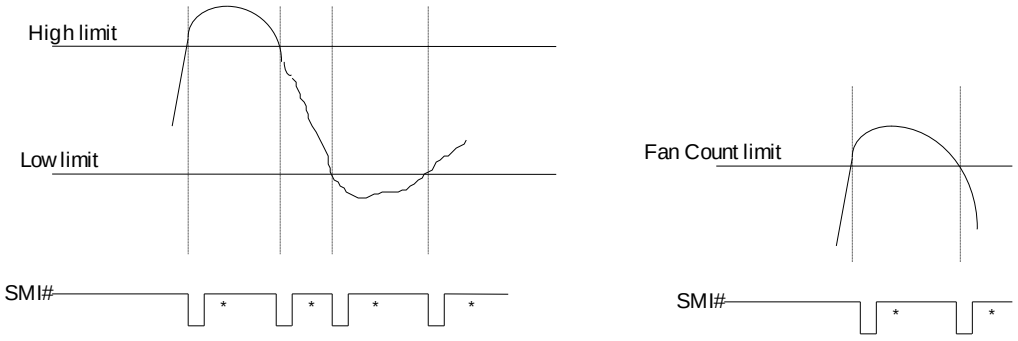
SMIOVT Relative Temperature Registers

8.8.1 SMI# Interrupt

HM_SMI# can be routed to RESETCONI# pin by setting Configuration Register CR1Ah, bit 7 & bit 6 or routed to gpio bit 1 by setting Logic Device 9 CRE3 bit 1 to high. It can monitor voltages, fan counts, or temperatures.

8.8.2 Voltage SMI# Mode

The HM_SMI# signal can create an interrupt if a voltage exceeds a specified high limit or falls below a specified low limit. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

Figure 8-16 SMI Mode of Voltage and Fan Inputs

8.8.3 Fan SMI# Mode

The HM_SMI# signal can create an interrupt if a fan count crosses a specified fan limit (rises above it or falls below it). This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the figure above.

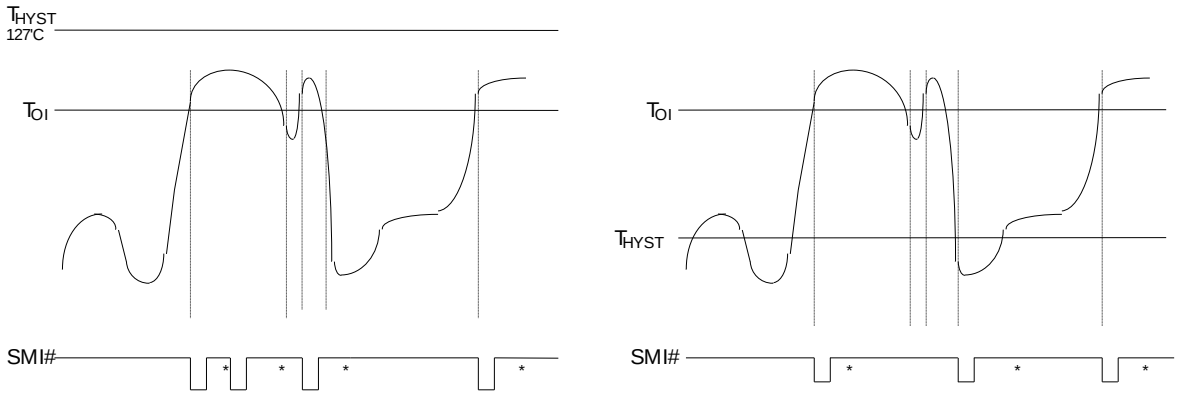
8.8.4 Temperature SMI# Mode

The HM_SMI# signal can create interrupts that depend on the temperatures measured by CPUTIN, and AUXTIN. There are three intertupt mode of SMI# for temperature in this chip.

(1) Comparator Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) to 127°C.

In this mode, the SMI# pin can create an interrupt as long as the current temperature exceeds T_O (Over Temperature). This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. If the interrupt is reset, the SMI# pin continues to create interrupts until the temperature goes below T_O. This is illustrated in the figure below.



*Interrupt Reset when Interrupt Status Registers are read

Comparator Interrupt Mode Two-Times Interrupt Mode

Figure 8-17 Comparator & Two Time SMI Mode

(2) Two-Times Interrupt Mode

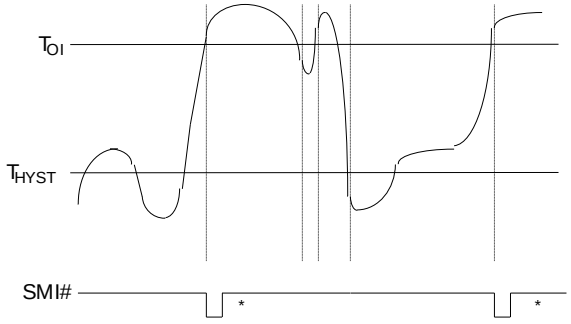
This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index 40h, bit 4 to zero for sensor 1 and bit 5 to zero for sensor 2.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

(3) One-Time Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index 40h, bit 4 to one for sensor 1 and bit 5 to one for sensor 2.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. Another interrupt is generated again after tmeperatute should falls below T_{HYST} once. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

One-Time Interrupt Mode

Figure 8-18 One-Time SMI Mode

Table 8-4 Relative Register of OVT functions

SMIOVT1	SMIOVT2
Bank0,Index18_Bit6 **0:** Enable SMIOVT1 output **1:** Disable SMIOVT1 output **Bank0, Index18_Bit0** **0:** Start to monitor the source of SMIOVT1 temperature. **1:** Stop monitoring the source of SMIOVT1 temperature. **Bank0,Index18_Bit4** **0:** Comparator Mode (def.) **1:** Interrupt Mode	**Bank 0, Inedex4C_Bit 3** **0:** Enable SMIOVT2 output **1:** Disable SMIOVT2 output **Bank1, Index52_Bit0** **0:** Start to monitor the source of SMIOVT2 temperature. **1:** Stop monitoring the source of SMIOVT2 temperature. **Bank 1, Index52_Bit 1** **0:** Comparator Mode(def.) **1:** Interrupt Mode

8.8.5 OVT# Interrupt

OVT# Interrupt can monitor temperatures. It is enabled to give output by Bank0 Index 18h, bit 6 for Temperature Sensor 1(default: CPUTIN); Bank1 Index 4Ch, bit 3 for Temperature Sensor 2(default: AUXTIN). It can be routed to RESETCONI# pin by setting Configuration Register CR1Ah, bit 7 & bit 6 or routed to gpio bit 6 by setting Logic Device 9 CRE3 bit 6 to high.

The OVT# singal has two interrupt modes, comparator and interrupt. The modes are illustrated in this figure.

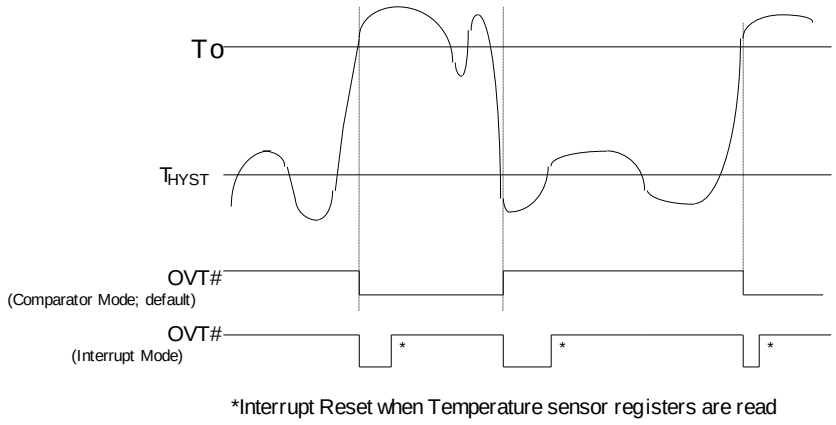


Figure 8-19 OVT# Modes of Temperature Inputs

If Bank0 Index 18h, bit 4, is set to zero for Tempaerature Sensor1 or Bank1 Index 52h, bit 1, is set to zero for Tempaerature Sensor2, the OVT# signal is in comparator mode. In comparator mode, the OVT# pin can create

an interrupt once the current temperature exceeds T_O and continues to create interrupts until the temperature falls below T_{HYST}. The OVT# signal is asserted once the temperature has exceeded T_O and has not yet fallen below T_{HYST}.

If Bank0 Index 18h, bit 4, is set to one for Tempaerature Sensor1 or Bank1 Index 52h, bit 1, is set to one for Tempaerature Sensor2, the OVT# signal is in interrupt mode. In interrupt mode, the OVT# pin can create an interrupt once the current temperature rises above T_O or when the temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers. The OVT# signal is asserted when an interrupt is generated and remains asserted until the interrupt is reset.

9. HARDWARE MONITOR REGISTER SET

The base address of the Address Port and Data Port is specified in registers CR[60h] and CR[61h] of Logical Device B, the hardware monitor device. CR[60h] is the high byte, and CR[61h] is the low byte. The Address Port and Data Port are located at the base address, plus 5h and 6h, respectively. For example, if CR[60h] is 02h and CR[61h] is 90h, the Address Port is at 0x295h, and the Data Port is at 0x296h.

Remember that this access is from the host CPU I/O address range. To conserve space in the crowded CPU I/O addresses, many of the hardware monitor registers are “banked” with the bank number located at Bank0, index 04Eh.

9.1 Address Port (Port x5h)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RESERVED.**
7-0	**READ/WRITE.**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Address Pointer (Power On default 00h)							
A7	A6	A5	A4	A3	A2	A1	A0

9.2 Data Port (Port x6h)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Data to be read from or to be written to Value RAM and Register.

9.3 SYSFANOUT PWM Output Frequency Configuration Register – Index 00h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL1	PWM_SCALE1						
DEFAULT	0	0	0	0	0	0	1	1

The register is meaningful only when SYSFANOUT is progarmmed for PWM output (i.e., Bank0, Index 04h, bit 0 is 0).

BIT	DESCRIPTION
7	**PWM_CLK_SEL1. SYSFANOUT PWM Input Clock Source Select.** This bit selects the clock source for PWM output frequency. Refer the Divisor table.
6-0	**PWM_SCALE1. SYSFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.4 CPUFANOUT PWM Output Frequency Configuration Register – Index 02h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL2	PWM_SCALE2						
DEFAULT	0	0	0	0	0	0	1	1

The register is meaningful only when CPUFANOUT is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL2. CPUFANOUT PWM Input Clock Source Select.** This bit selects the clock source for the PWM output. Refer the Divisor table.
6-0	**PWM_SCALE2. CPUFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.5 AUXFANOUT0 PWM Output Frequency Configuration Register – Index 10h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL3	PWM_SCALE3						
DEFAULT	0	0	0	0	0	0	1	1

This register is only meaningful when AUXFANOUT0 is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL3. AUXFANOUT0 PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE3. AUXFANOUT0 PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.6 OVT# Configuration Register – Index 18h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

BIT	RESERVED	DIS_OVT1	RESERVED	OVTMOD1	RESERVED			STOPOVT1
DEFAULT	0	1	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**DIS_OVT1.** 0: Enable SMIOVT1 OVT# output. 1: Disable temperature sensor SMIOVT1 over-temperature (OVT#) output. (Default)
5	**Reserved.**
4	**OVTMOD1. Temperature 1 OVT Mode Select.** 0 : Compare Mode. (Default) 1 : Interrupt Mode.
3-1	**Reserved.**
0	**STOPOVT1.** **0: Monitor SMIOVT1 temperature source.** **1: Stop monitoring SMIOVT1 temperature source.**

9.7 Value RAM — Index 27h ~ 3Fh (Bank 0)

ADDRESS A6-A0	DESCRIPTION
27h	SMIOVT1 temperature source reading.
2Bh	CPUVCORE High Limit
2Ch	CPUVCORE Low Limit
2Dh	VIN0 High Limit
2Eh	VIN0 Low Limit
2Fh	AVCC High Limit
30h	AVCC Low Limit
31h	3VCC High Limit
32h	3VCC Low Limit
33h	VIN1 High Limit
34h	VIN1 Low Limit
35h	VTT High Limit
36h	VTT Low Limit
37h	3VSB High Limit
38h	3VSB Low Limit

9.8 Configuration Register – Index 40h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	INITIALIZATION	RESERVED	EN_WS1	EN_WS	INT_CLEAR	RESERVED	SMI#ENABLE	START
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Initialization.** A one restores the power-on default values to some registers. This bit clears itself since the power-on default of this bit is zero.
6	**RESERVED**
5	**Output type of SMIOVT2:** 1: SMI# output type of SMIOVT Source2 temperature (Default: AUXTIN) is one-time Interrupt Mode. 0: SMI# output type of SMIOVT Source2 temperature (Default: AUXTIN) is two-time Interrupt Mode.
4	**Output type of SMIOVT1** 1: SMI# output type of SMIOVT Source1 temperature (Default: CPUTIN) is one-time Interrupt Mode. 0: SMI# output type of SMIOVT Source1 temperature (Default: CPUTIN) is two-time Interrupt Mode.
3	**INT_Clear.** A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
2	**Reserved.**
1	**SMI# Enable.** A one enables the SMI# Interrupt output. 1: Enable SMI# function (Deafult) 0: Disable SMI# function
0	**Start.** A one enables startup of monitoring operations. A zero puts the part in standby mode. **Note:** Unlike the "INT_Clear" bit, the outputs of interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred.

9.9 Interrupt Status Register 1 – Index 41h (Bank 0)

Attribute: Read Clear

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	STS_CPU FANIN	STS_SYSF ANIN	Reserved		STS_3VCC	STS_AVC C	STS_VIN0	STS_CPUV CORE
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**STS_CPUFANIN.** A one indicates the fan count limit of CPUFANIN has been exceeded.
6	**STS_SYSFANIN.** A one indicates the fan count limit of SYSFANIN has been exceeded.
2	**Reserved.**
3	**STS_3VCC.** A one indicates the high or low limit of 3VCC has been exceeded.
2	**STS_AVCC (Pin 51).** A one indicates the high or low limit of AVCC has been exceeded.
1	**STS_VIN0.** A one indicates the high or low limit of VIN0 has been exceeded.
0	**STS_CPUVCORE.** A one indicates the high or low limit of CPUVCORE has been

BIT	DESCRIPTION
	exceeded.

9.10 Interrupt Status Register 2 – Index 42h (Bank 0)

Attribute: Read Clear

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	CASEOPEN1	Reserved.	Reserved	AUXFANIN0	STS_3VSB	STS_VTT	STS_VIN1
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**STS_CASEOPEN1.** A one indicates the case has been opened.
5	**Reserved.**
4	**Reserved.**
3	**STS_AUXFANIN0.** A one indicates the fan count limit of AUXFANIN0 has been exceeded.
2	**STS_3VSB.** A one indicates the high or low limit of VCOREREFIN has been exceeded.
1	**STS_VTT.** A one indicates the high or low limit of VTT has been exceeded.
0	**STS_VIN1.** A one indicates the high or low limit of VIN1 has been exceeded.

9.11 SMI# Mask Register 1 – Index 43h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MSK_CPUFANIN	MSK_SYSFANIN	Reserved		MSK_3VCC	MSK_AVCC	MSK_VIN0	MSK_CPUVCORE
DEFAULT	1	1	0	0	1	1	1	1

BIT	DESCRIPTION	
7	**MSK_CPUFANIN.**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 1 – Index 41h (Bank0))
6	**MSK_SYSFANIN.**	
5-4	**Reserved.**	
3	**MSK_3VCC.**	
2	**MSK_AVCC.**	
1	**MSK_VIN0.**	
0	**MSK_CPUVCORE.**	

9.12 SMI# Mask Register 2 – Index 44h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MSK_TAR2	MSK_TAR1	RESERVED	RESERVED	MSK_AUXFANIN0	MSK_3VSB	MSK_VTT	MSK_VIN1
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	**MSK_TAR2.**	A one disables the corresponding interrupt status bit for the interrupt. (See Interrupt Status Register 2 – Index 42h (*Bank 0*))

9.13 Interrupt Status Register 4 – Index 45h (Bank 0)

Attribute: Read Clear

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		AUX FANOUT0	CPU FANOUT	SYS FANOUT	RESERVED	STS_TEMP2	STS_TEMP1
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RESERVED**
6	**RESERVED**
5	**AUXFANOUT0.** “1” indicates that AUXFANOUT0 works for three minutes at the full fan speed.
4	**CPUFANOUT.** “1” indicates that CPUFANOUT works for three minutes at the full fan speed.
3	**SYSFANOUT.** “1” indicates that SYSFANOUT works for three minutes at the full fan speed.
2	**RESERVED**
1	**STS_TEMP2.** “1” indicates the SMI# Interrupt of SMIOVT temperature set 2 has occurred. (AUXTIN is default temperature)
0	**STS_TEMP1.** “1” indicates the SMI# Interrupt of SMIOVT temperature set 1 has occurred. (CPUTIN is default temperature)

9.14 SMI# Mask Register 3 – Index 46h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	CASEOPEN1 CLEAR	Reserved	MSK_TEMP2	MSK_TEMP1	Reserved	AUXFANIN1	CASEOPEN1
DEFAULT	0	0	0	1	1	0	1	1

BIT	DESCRIPTION

BIT	DESCRIPTION	
7	**RESERVED**	
6	**CASEOPEN1 Clear Control.** Writing 1 to this bit will clear CASEOPEN status. This bit will be cleared itself. The function is the same as LDA, CR[EEh], bit 0..	
5	**RESERVED**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt. (See Interrupt Status Register 4 – Index 45h (Bank 0)).
4	**MSK_TEMP2**	
3	**MSK_TEMP1**	
2	**AUXFANIN2**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt.
1	**AUXFANIN1**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt
0	**CASEOPEN1**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt.

9.15 SMI/OVT Control Register1 – Index 4Ch (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	T2ToT6_INT MODE	EN_T1 _ONE	RESERVED	DIS_ OVT2	OVTPOL	RESERVED	
DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION
7-4	**Reserved**
3	**DIS_OVT2.** 1: Disable SMIOVT Source2 temperature sensor (Default: AUXTIN) over-temperature (OVT) output. (Default) 0: Enable SMIOVT Source2 temperature OVT output through pin OVT#.
2	**OVTPOL (Over-temperature polarity).** 1: OVT# is active high. 0: OVT# is active low (Default).
1-0	**Reserved.**

9.16 FAN IN/OUT Control Register – Index 4Dh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANOPV4	FANINC4	FANOPV3	FANINC3	FANOPV2	FANINC2	FANOPV1	FANINC1
DEFAULT	0	1	0	1	0	1	0	1

BIT	DESCRIPTION
7	**FANOPV4. AUXFANIN1 output value**, only if bit 2 is set to zero. 1: Pin 61 (CPUFANIN) generates a logic-high signal. 0: Pin 61 generates a logic-low signal. (Default)
6	**FANINC4. AUXFANIN1 Input Control.** 1: Pin 63 (SYSFANIN) acts as a fan tachometer input. (Default) 0: Pin 63 acts as a fan control signal, and the output value is set by bit 1.
5	**FANOPV3. AUXFANIN0 output value**, only if bit 2 is set to zero. 1: Pin 61 (CPUFANIN) generates a logic-high signal. 0: Pin 61 generates a logic-low signal. (Default)
4	**FANINC3. AUXFANIN0 Input Control.** 1: Pin 63 (SYSFANIN) acts as a fan tachometer input. (Default) 0: Pin 63 acts as a fan control signal, and the output value is set by bit 1.
3	**FANOPV2. CPUFANIN output value**, only if bit 2 is set to zero. 1: Pin 61 (CPUFANIN) generates a logic-high signal. 0: Pin 61 generates a logic-low signal. (Default)
2	**FANINC2. CPUFANIN Input Control.** 1: Pin 61 (CPUFANIN) acts as a fan tachometer input. (Default) 0: Pin 61 acts as a fan control signal, and the output value is set by bit 3.
1	**FANOPV1. SYSFANIN output value**, only if bit 0 is set to zero. 1: Pin 63 (SYSFANIN) generates a logic-high signal. 0: Pin 63 generates a logic-low signal. (Default)
0	**FANINC1. SYSFANIN Input Control.** 1: Pin 63 (SYSFANIN) acts as a fan tachometer input. (Default) 0: Pin 63 acts as a fan control signal, and the output value is set by bit 1.

9.17 Bank Select Register – Index 4Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	HBACS	Reserved.			BANK SEL3	BANK SEL2	BANK SEL1	BANK SEL0
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**HBACS. HBACS – High Byte Access.** 1: Access Index 4Fh high-byte register. (Default) 0: Access Index 4Fh low-byte register.	
6-4	**Reserved.**	
3-0	**BANKSEL3.**	Bank Select for Bank0 to Bank7. The Three-bit binary value corresponds to the bank number. For example, "0010" selects bank2.

9.18 Nuvoton Vendor ID Register – Index 4Fh (Bank 0)

Attribute: Read Only
Size: 16 bits

BIT	15	14	13	12	11	10	9	8
NAME	VIDH							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDL							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	**Vendor ID High-Byte**, if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	**Vendor ID Low-Byte**, if Index 4Eh, bit 7 is 0. Default A3h.

9.19 Chip ID – Index 58h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CHIPID							
DEFAULT	1	1	0	0	0	0	0	1

BIT	DESCRIPTION
7-0	Nuvoton Chip ID number. Default C1h.

9.20 VBAT Monitor Control Register – Index 5Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		DIODES5	DIODES4	DIODES3	DIODES2	DIODES1	EN_VBAT_MNT
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Reserved**
5	**DIODES 5. Sensor type selection for SYSTIN.** 1: Diode sensor. 0: Thermistor sensor.
4	**DIODES 4. Sensor type selection for AUXTIN1.**

BIT	DESCRIPTION
	1: Diode sensor. 0: Thermistor sensor.
3	**DIODES 3. Sensor type selection for AUXTIN0.** 1: Diode sensor. 0: Thermistor sensor.
2	**DIODES 2. Sensor type selection for AUXTIN2.** 1: Diode sensor. 0: Thermistor sensor. (default)
1	**DIODES 1. Sensor type selection for CPUTIN.** 1: Diode sensor. 0: Thermistor sensor. (default)
0	**EN_VBAT_MNT.** 1: Enable battery voltage monitor. When this bit changes from zero to one, it takes one monitor cycle time to update the VBAT reading value register. 0: Disable battery voltage monitor.

9.21 Current Mode Enable Register – Index 5Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		EN_ SYSTIN CURRENT MODE	EN_ AUXTIN1 CURRENT MODE	EN_ AUXTIN0 CURRENT MODE	EN_ AUXTIN2 CURRENT MODE	EN_ CPUTIN CURRENT MODE	Reserved
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7 -6	**Reserved**
5	**Enable** SYSTIN **Current Mode**. With SYSTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 3 = 1). 1: Temperature sensing of SYSTIN by Current Mode. 0: Temperature sensing of SYSTIN depends on the setting of Index 5Dh. **(Default)**
4	**Enable AUXTIN1 Current Mode**. With AUXTIN1 is selected to Diode sensor (Bank0, Index 5Dh, Bit 3 = 1). 1: Temperature sensing of AUXTIN1 by Current Mode. 0: Temperature sensing of AUXTIN1 depends on the setting of Index 5Dh. **(Default)**
3	**Enable AUXTIN0 Current Mode**. With AUXTIN0 is selected to Diode sensor (Bank0, Index 5Dh, Bit 3 = 1). 1: Temperature sensing of AUXTIN0 by Current Mode. 0: Temperature sensing of AUXTIN0 depends on the setting of Index 5Dh. **(Default)**
2	**Enable AUXTIN2 Current Mode.** With AUXTIN2 is selected to Diode sensor (Bank0, Index 5Dh, Bit 2 = 1). 1: Temperature sensing of AUXTIN2 by Current mode. 0: Temperature sensing of AUXTIN2 depends on the setting of Index 5Dh. **(Default)**
1	**Enable CPUTIN Current Mode.** With CPUTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 1 = 1).

BIT	DESCRIPTION
	1: Temperature sensing of CPUTIN by Current Mode. 0: Temperature sensing of CPUTIN depends on the setting of Index 5Dh. **(Default)**
0	**Reserved**

9.22 Reserved Register – Index 61h~ADh (Bank 0)

9.23 PECI Temperature Reading Enable for SMIOVT and SMART FAN Control Register – Index AEh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_PECI1	EN_PECI0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**Reserved.**
1	**Enable PECI Agent1**
0	**Enable PECI Agent0**

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.24 BEEP Control Register 1 – Index B2h (Bank0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EnVBAT_BP	En3VSB_BP	EnVTT_BP	EnVIN1_BP	En3VCC_BP	EnAVCC_BP	EnVIN0_BP	EnCPUVCORE_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**EnVBAT_BP** **1 : Enable VBAT Beep function** **0 : Disable VBAT Beep fuction**
6	**En3VSB_BP** **1 : Enable 3VSB Beep function** **0 : Disable 3VSB Beep fuction**
5	**EnVTT_BP** **1 : Enable VTT Beep function** **0 : Disable VTT Beep fuction**
4	**EnVIN1_BP** **1 : Enable VIN1 Beep function**

BIT	DESCRIPTION
	0 : Disable VIN1 Beep fuction
3	**En3VCC_BP** **1 : Enable 3VCC Beep function** **0 : Disable 3VCC Beep fuction**
2	**EnAVCC_BP** **1 : Enable AVCC Beep function** **0 : Disable AVCC Beep fuction**
1	**EnVIN0_BP** **1 : Enable VIN0 Beep function** **0 : Disable VIN0 Beep fuction**
0	**EnCPUVCORE_BP** **1 : Enable CPUVCORE Beep function** **0 : Disable CPUVCORE Beep fuction**

9.25 BEEP Control Register 2 – Index B3h (Bank0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					EnVIN3_BP	EnVIN2_BP	EnVIN4_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**Reserved.**
2	**EnVIN3_BP** **1 : Enable VIN3 Beep function** **0 : Disable VIN3 Beep fuction**
1	**EnVIN2_BP** **1 : Enable VIN2 Beep function** **0 : Disable VIN2 Beep fuction**
0	**EnVIN4_BP** **1 : Enable VIN4 Beep function** **0 : Disable VIN4 Beep fuction**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.26 BEEP Control Register 3 – Index B4h (Bank0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	User Mode	Reserved					EnT2	EnT1

							_BP	_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**User control for Beep alarm** **1 : Enable** **0 : Disable**
6-2	**Reserved.**
1	**EnT2_BP** **1 : Enable Temperature 2 Beep function** **0 : Disable Temperatre 2 Beep fuction**
0	**EnT1_BP** **1 : Enable Temperature 1 Beep function** **0 : Disable Temperatre 1 Beep fuction**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.27 SYSFAN Virtual Temperature 1 Register – Index EAh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**SYSFAN Virtual Temperature**							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SYSFAN Virtual TEMP 1

9.28 BEEP Control Register 4 – Index B5h (Bank0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**En Caseopen1_BP**	**Reserved**	**Reserved**	**En AUXFANIN1 _BP**	**En AUXFANIN0 _BP**	**En CPUFANIN _BP**	**En SYSFANIN _BP**	**En_Beep**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En Caseopen1_BP** **1 : Enable Caseopen1 Beep function** **0 : Disable Caseopen1 Beep fuction**
6	**Reserved.**
5	**Reserved.**
4	**En AUXFANIN1_BP**

BIT	DESCRIPTION
	1 : Enable AUXFANIN1 Beep function **0 : Disable AUXFANIN1 Beep fuction**
3	**En AUXFANIN0_BP** **1 : Enable AUXFANIN0 Beep function** **0 : Disable AUXFANIN0 Beep fuction**
2	**En CPUFANIN _BP** **1 : Enable CPUFANIN Beep function** **0 : Disable CPUFANIN Beep fuction**
1	**En SYSFANIN _BP** **1 : Enable SYSFANIN Beep function** **0 : Disable SYSFANIN Beep fuction**
0	**Enable Beep Function:** **1 : Enable Beep Function** **0 : Disable Beep Fuction**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.29 CPUFAN Virtual Temperature 2 Register – Index EBh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Virtual Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN Virtual TEMP 2

9.30 AUX0FAN Virtual Temperature 3 Register – Index ECh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUX0FAN Virtual Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUX0FAN Virtual TEMP 3

9.31 SYSFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				SYSFAN SOURCE			
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-4	**Reserved**
3-0	**SYSFAN Temperature Source Select**: 0 0 0 0: Select **Local Temp** as SYSFAN monitoring source. 0 0 0 1: Select **CPUTIN** as SYSFAN monitoring source. (Default) 0 0 1 0: Select **AUXTIN2** as SYSFAN monitoring source. 0 0 1 1: Select **AUXTIN0** as SYSFAN monitoring source. 0 1 0 0: Select **AUXTIN1** as SYSFAN monitoring source. 0 1 0 1: Select **PECI Agent 0** Calibration as SYSFAN monitoring source. 0 1 1 0: Select **PECI Agent 1** Calibration as SYSFAN monitoring source. 0 1 1 1: Select **Virtual Temp 1** as SYSFAN monitoring source. 1 0 0 0: Select **SYSTIN** as SYSFAN monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.32 SYSFAN MODE Register / SYSFAN TOLERRANCE Register – Index 02h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN MODE				Reserved	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**SYSFANOUT Mode Select.** 0000: SYSFANOUT is in Manual Mode. **(Default)** 0100: SYSFANOUT is in SMART FAN IV Mode.
3	**Reserved**
2-0	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L.

9.33 SYSFANOUT Step Up Time Register – Index 03h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Step Up Time							

DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.05 second. The default time is 0.5 second.

9.34 SYSFANOUT Step Down Time Register – Index 04h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.05 second. The default time is 0.5 second.

9.35 SYSFANOUT Output Value Select Register – Index 09h (Bank 1)

Attribute: Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	0	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E2h] of Logical Device B, CR[E0h] is the Default Speed Configuration Register of SYSFANOUT.

Read from I/O space address.

9.36 SYSFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.37 SYSFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.38 SYSFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.39 SYSFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.40 SYSFAN (SMART FAN™ IV) PWM 1 Register – Index 27h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 1 Register.

9.41 SYSFAN (SMART FAN™ IV) PWM 2 Register – Index 28h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 2 Register.

9.42 SYSFAN (SMART FAN™ IV) PWM 3 Register – Index 29h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 3 Register.

9.43 SYSFAN (SMART FAN™ IV) PWM 4 Register – Index 2Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 4 Register.

9.44 SYSFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Critical Temperature Register.

9.45 SYSFAN Enable Critical Duty – Index 36h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_SYS_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_SYS_CRITICAL_DUTY** 0: Load default Full Speed 8'hFF for SYSFANOUT. 1: Used Index 37 CRITICAL_DUTY Value for SYSFANOUT.

9.46 SYSFAN Critical Duty Register – Index 37h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	SYSFAN Critical Duty.

9.47 SYSFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					SYSFANOUT Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	SYSFANOUT Critical Temperature Tolerance

9.48 SYSFAN PECIERR DUTY Enable Register – Index 3Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_SYS_PECIERR_DUTY	

DEFAULT	0	0	0

BIT	DESCRIPTION
7-2	**Reserved**
1-0	**EN_SYS_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_SYSOUT** Value for SYSFANOUT. 10,11: Keep Full Speed

9.49 SYSFANOUT Pre-Configured Register For PECI Error – Index 41h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT pre-configured register for PECI error (PECI_ERR_SYSOUT)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SYSFANOUT pre-configured register for PECI error.**

9.50 SMIOVT2 Temperature Source (High Byte) Register – Index 50h (Bank 1)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<7:0>							

BIT	DESCRIPTION
7-0	**Temperature <7:0> (default: AUXTIN2 temperature source).** The 8-bit value is in units of 1℃.

9.51 SMIOVT2 Temperature Source Configuration Register – Index 52h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					RESERVED	OVTMOD2	STOPOVT2
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**Reserved.**
1	**OVTMOD2. Tempaerature 2 OVT Mode Select.** 0 : Compare Mode. (Default)

BIT	DESCRIPTION
	1: Interrupt Mode.
0	**STOPOVT2.** 0: Monitor SMIOVT2 temperature source. 1: Stop monitoring SMIOVT2 temperature source.

9.52 FAN COUNT STEP Register – Index 66h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	FAN count UP unit.
3-0	FAN count DOWN unit.

9.53 T1 Delay Time Register – Index 67h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.54 CPUFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				CPUFAN SOURCE			
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**CPUFAN Temperature Source Select**:

BIT	DESCRIPTION
	0 0 0 0: Select **Local Temp** as CPUFAN monitoring source. 0 0 0 1: Select **CPUTIN** as CPUFAN monitoring source. 0 0 1 0: Select **AUXTIN2** as CPUFAN monitoring source. (Default) 0 0 1 1: Select **AUXTIN0** as CPUFAN monitoring source. 0 1 0 0: Select **AUXTIN1** as CPUFAN monitoring source. 0 1 0 1: Select **PECI Agent 0** Calibration as CPUFAN monitoring source. 0 1 1 0: Select **PECI Agent 1** Calibration as CPUFAN monitoring source. 0 1 1 1: Select **Virtual Temp 2** as CPUFAN monitoring source. 1 0 0 0: Select **SYSTIN** as CPUFAN monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.55 CPUFAN MODE Register / CPUFAN TOLERRANCE Register – Index 02h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN MODE				Reserved	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L		
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-4	**CPUFANOUT Mode Select.** 0000: CPUFANOUT is in Manual Mode. (Default) 0100: CPUFANOUT is in SMART FAN IV Mode.
3	**Reserved**
2-0	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L.

9.56 CPUFANOUT Step Up Time Register – Index 03h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.05 second. The default time is 0.5 second.

9.57 CPUFANOUT Step Down Time Register – Index 04h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.05 second. The default time is 0.5 second.

9.58 CPUFANOUT Output Value Select Register – Index 09h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value							
DEFAULT	0	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E1h] is the Default Speed Configuration Register of CPUFANOUT.

Read from I/O space address.

9.59 Reserved Register – Index 0Ah (Bank 2)

9.60 CPUFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.61 CPUFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	CPUFAN (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.62 CPUFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.63 CPUFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 4							
DEFAULT	0	1	0	0	0	1	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.64 CPUFAN (SMART FAN™ IV) PWM1 Register – Index 27h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM1 Register.

9.65 CPUFAN (SMART FAN™ IV) PWM2 Register – Index 28h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM2 Register.

9.66 CPUFAN (SMART FAN™ IV) PWM3 Register – Index 29h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM3 Register.

9.67 CPUFAN (SMART FAN™ IV) PWM4 Register – Index 2Ah (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM4 Register.

9.68 CPUFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Critical Temperature Register.

9.69 CPUFAN Enable Critical Duty – Index 36h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_CPU_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_CPU_CRITICAL_DUTY** 0: Load default Full Speed 8'hFF for CPUFANOUT. 1: Used Index 37 CRITICAL_DUTY Value for CPUFANOUT.

9.70 CPUFAN Critical Duty Register – Index 37h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	CPUFAN Critical Duty.

9.71 CPUFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					CPUFANOUT Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**CPUFANOUT Critical Temperature Tolerance**

9.72 Weight value Configuration Register – Index 39h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_CPUFAN_	Reserved				CPU_WEIGHT_SEL		

	WEIGHT							
DEFAULT	0	0		0	0	0	0	0

BIT	DESCRIPTION
7	**EN_CPUFAN_WEIGHT.** 0: Disable Weight Value Control for CPUFAN. 1: Enable Weight Value Control for CPUFAN.
6-3	**Reserved**
2-0	**CPUFAN Weighting Temperature Source Select**: 0 0 0: Select **CPUTIN** as CPUFAN monitoring source. (Default) 0 0 1: Select **AUXTIN2** as CPUFAN monitoring source. 0 1 0: Select **AUXTIN0** as CPUFAN monitoring source. 0 1 1: Select **AUXTIN1** as CPUFAN monitoring source. 1 0 0: Select **PECI Agent 0** Calibration as CPUFAN monitoring source. 1 0 1: Select **PECI Agent 1** Calibration as CPUFAN monitoring source.

9.73 CPUFANOUT Temperature Step Register – Index 3Ah (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Temperature Step (CPU_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Step**

9.74 CPUFANOUT Temperature Step Tolerance Register – Index 3Bh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Temperature Step Tolerance (CPU_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Step Tolerance**

9.75 CPUFANOUT Weight Step Register – Index 3Ch (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Weight Step (CPU_WEIGHT_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Weight Step**

9.76 CPUFANOUT Temperature Base Register – Index 3Dh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_TEMP_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Base**

9.77 CPUFANOUT Temperature Fan Duty Base Register – Index 3Eh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_FC_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Start point of Fan Duty increasing**

9.78 CPUFAN PECIERR DUTY Enable Register – Index 3Fh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_CPU_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	**Reserved**
1-0	**EN_CPU_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_CPUOUT** Value for CPUFANOUT.

	10,11: Keep Full Speed

9.79 CPUFANOUT Pre-Configured Register For PECI Error – Index 41h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT pre-configured register for PECI error (PECI_ERR_CPUOUT)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**CPUFANOUT pre-configured register for PECI error.**

9.80 FAN COUNT STEP Register – Index 66h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	FAN count UP unit.
3-0	FAN count DOWN unit.

9.81 T1 Delay Time Register – Index 67h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.82 AUXFAN0 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				AUXFAN0 SOURCE			
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-4	**Reserved**
3-0	**AUXFAN0 Temperature Source Select**: 0 0 0 0: Select **Local Temp** as AUXFAN0 monitoring source. 0 0 0 1: Select **CPUTIN** as AUXFAN0 monitoring source. (Default) 0 0 1 0: Select **AUXTIN2** as AUXFAN0 monitoring source. 0 0 1 1: Select **AUXTIN0** as AUXFAN0 monitoring source. 0 1 0 0: Select **AUXTIN1** as AUXFAN0 monitoring source. 0 1 0 1: Select **PECI Agent 0** Calibration as AUXFAN0 monitoring source. 0 1 1 0: Select **PECI Agent 1** Calibration as AUXFAN0 monitoring source. 0 1 1 1: Select **Virtual Temp 3** as AUXFAN0 monitoring source. 1 0 0 0: Select **SYSTIN** as AUXFAN0 monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.83 AUXFAN0 MODE Register / AUXFAN0 TOLERRANCE Register – Index 02h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 MODE				Reseved	Tolerance of AUXFAN0 Target Temperature or AUXFANIN0 Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**AUXFANOUT0 Mode Select.** 0000: **AUXFANOUT0** is in Manual Mode. **(Default)** 0100: **AUXFANOUT0** is in SMART FAN IV Mode.
3	**Reseved**
2-0	Tolerance of AUXFAN0 Target Temperature or AUXFANIN0 Target Speed_L.

9.84 AUXFANOUT0 Step Up Time Register – Index 03h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Value Step Up Time							

DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT0 takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.05 second. The default time is 0.5 second.

9.85 AUXFANOUT0 Step Down Time Register – Index 04h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT0 takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.05 second. The default time is 0.5 second.

9.86 AUXFANOUT0 Output Value Select Register – Index 09h (Bank 3)

Attribute: Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Value							
DEFAULT	1	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E2h] is the Default Speed Configuration Register of AUXFANOUT0.

Read from I/O space address.

9.87 AUXFAN0 (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 1 Register (T1).

9.88 AUXFAN0 (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 2 Register (T2).

9.89 AUXFAN0 (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 3 Register (T3).

9.90 AUXFAN0 (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 4 Register (T4).

9.91 AUXFAN0 (SMART FAN™ IV) PWM 1 Register – Index 27h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) PWM 1 Register.

9.92 AUXFAN0 (SMART FAN™ IV) PWM 2 Register – Index 28h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) PWM 2 Register.

9.93 AUXFAN0 (SMART FAN™ IV) PWM 3 Register – Index 29h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) PWM 3 Register.

9.94 AUXFAN0 (SMART FAN™ IV) PWM 4 Register – Index 2Ah (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) PWM 4 Register.

9.95 AUXFAN0 (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Critical Temperature Register

9.96 AUXFAN0 Enable Critical Duty – Index 36h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX0_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUX0_CRITICAL_DUTY** 0: Load default Full Speed 8'hFF for AUXFANOUT0. 1: Used Index 37 CRITICAL_DUTY Value for AUXFANOUT0.

9.97 AUXFAN0 Critical Duty Register – Index 37h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	AUXFAN0 Critical Duty.

9.98 AUXFANOUT0 Critical Temperature Tolerance Register – Index 38h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT0 Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**AUXFANOUT0 Critical Temperature Tolerance**

9.99 AUXFAN0 PECIERR DUTY Enable Register – Index 3Fh (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_AUX0_PECIERR_DUTY	

DEFAULT	0	0	0

BIT	DESCRIPTION
7-2	**Reserved**
1-0	**EN_AUX0_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_AUXOUT0** Value for AUXFANOUT0. 10,11: Keep Full Speed

9.100 AUXFANOUT0 Pre-Configured Register For PECI Error – Index 41h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 pre-configured register for PECI error (PECI_ERR_AUXOUT0)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**AUXFANOUT0 pre-configured register for PECI error.**

9.101 FAN COUNT STEP Register – Index 66h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	FAN count UP unit.
3-0	FAN count DOWN unit.

9.102 T1 Delay Time Register – Index 67h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.103 Reserved Register – Index 29h (Bank 4)

9.104 Reserved Register – Index 43h (Bank 4)

9.105 AUXTIN1 Temperature Sensor Offset Register – Index 4Ah (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN1 Temperature Offset Value.** The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.106 Interrupt Status Register 3 – Index 50h (Bank 4)

Attribute: Read Clear
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSTIN Temperature Offset Value.** The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.107 SMI# Mask Register 4 – Index 51h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			TAR3	Reserved		SMSKVIN2	SMSKVBAT
DEFAULT	0	0	0	1	0	0	1	1

BIT	DESCRIPTION
7-5	**Reserved.**
4	**TAR3.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 45h (Bank 0))
3-2	**Reserved.**

BIT	DESCRIPTION
1	**SMSKVIN2.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
0	**SMSKVBAT.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))

9.108 CPUTIN Temperature Sensor Offset Register – Index 54h (Bank 4)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUTIN Temperature Offset Value.** The value in this register will be added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.109 AUXTIN2 Temperature Sensor Offset Register – Index 55h (Bank 4)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN2 Temperature Offset Value.** The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.110 AUXTIN0 Temperature Sensor Offset Register – Index 56h (Bank 4)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN0 Temperature Offset Value.** The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset

BIT	DESCRIPTION
	value.

9.111 Real Time Hardware Status Register I – Index 59h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN _STS	SYSFANIN _STS	Reserved		3VCC _STS	AVCC _STS	VIN0 _STS	CPUVCORE _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN_STS. CPUFANIN Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
6	**SYSFANIN_STS. SYSFANIN Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
5-4	**Reserved.**
3	**3VCC_STS. 3VCC Voltage Status.** 1: 3VCC voltage is over or under the allowed range. 0: 3VCC voltage is in the allowed range.
2	**AVCC_STS. AVCC Voltage Status.** 1: AVCC voltage is over or under the allowed range. 0: AVCC voltage is in the allowed range.
1	**VIN0_STS. VIN1 Voltage Status.** 1: VIN0 voltage is over or under the allowed range. 0: VIN0 voltage is in the allowed range.
0	**CPUVCORE_STS. CPUVCORE Voltage Status.** 1: CPUVCORE voltage is over or under the allowed range. 0: CPUVCORE voltage is in the allowed range.

9.112 Real Time Hardware Status Register II – Index 5Ah (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2 _STS	TAR1 _STS	Reserved	Reserved	AUXFANIN0 _STS	AUXFANIN1 _STS	CASEOPEN1 _Real	VIN1 _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TAR2_STS. Smart Fan of CPUFANIN Warning Status.** 1: Selected temperature has been over the target temperature for three minutes at full fan

BIT	DESCRIPTION
	speed in SMART FAN™ IV. 0: Selected temperature has not reached the warning range.
6	**TAR1_STS. Smart Fan of SYSFANIN Warning Status.** 1: AUXTIN temperature has been over the target temperature for three minutes at full fan speed in SMART FAN™ IV. 0: AUXTIN temperature has not reached the warning range.
5	**Reserved.**
4	**Reserved.**
3	**AUXFANIN0_STS. AUXFANIN0 Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
2	**AUXFANIN1_STS. AUXFANIN1 Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
1	**CASEOPEN1_Real.** CaseOpen1 Pin Status.
0	**VIN1_STS. VIN0 Voltage Status.** 1: VIN1 voltage is over or under the allowed range. 0: VIN1 voltage is in the allowed range.

9.113 Real Time Hardware Status Register III – Index 5Bh (Bank 4)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		VTT _STS	3VSB _STS	TAR4 _STS	TAR3 _STS	VIN2 _STS	VBAT _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Reserved.**
5	**VTT_STS. VTT Voltage Status.** 1: VTT Voltage is over or under the allowed range. 0: VTT Voltage is in the allowed range.
4	**3VSB_STS. 3VSB Voltage Status.** 1: 3VSB voltage is over or under the allowed range. 0: 3VSB voltage is in the allowed range.
3	**Reserved.**
2	**TAR3_STS. Smart Fan of AUXFANIN0 Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in SMART FAN™ IV. 0: The selected temperature has not reached the warning range.
1	**VIN2_STS. VIN2 Voltage Status.** 1: The VBAT voltage is over or under the allowed range.

BIT	DESCRIPTION
	0: The VBAT voltage is in the allowed range.
0	**VBAT_STS. VBAT Voltage Status.** 1: The 3VSB voltage is over or under the allowed range. 0: The 3VSB voltage is in the allowed range.

9.114 PECI Agent Calibration Control Register – Index F8h (Bank 4)

Attribute: Read / Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	UP or Down Times					Adjust unit		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**UP or Down Times For PECI Agent Calibration**
2-0	**Adjust unit for PECI Agent Calibration**

9.115 PECI Agent Calibration Control Register – Index FAh (Bank 4)

Attribute: Read / Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Update Time					Reserved		Enable
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**Update Times For PECI Agent Calibration (0.1~3.2sec)**
2-1	**Reserved**
0	**Function Enable for PECI Agent Calibration**

9.116 Reserved Register – Index FBh ~ FFh (Bank 4)

9.117 Reserved Register – Index 00h ~ 53h (Bank 5)

9.118 Value RAM 2 — Index 50h-5Fh (Bank 5)

ADDRESS A6-A0	DESCRIPTION
54h	**VBAT High Limit**
55h	**VBAT Low Limit**

ADDRESS A6-A0	DESCRIPTION
56h	**VIN4 High Limit**
57h	**VIN4 Low Limit**
58h	**VIN2 High Limit**
59h	**VIN2 Low Limit**
5Ah	**VIN3 High Limit**
5Bh	**VIN3 Low Limit**

9.119 Close-Loop Fan Control RPM mode Register – Index 00 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					En_AUX0_RPM	En_CPU_RPM	En_SYS_RPM
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**RESERVED**
2	**En_AUX0_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.
1	**En_CPU_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.
0	**En_SYS_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.

9.120 SYSFAN RPM Mode Tolerance Register – Index 01 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ SYS_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit0）, unit is 100 RPM.

9.121 CPUFAN RPM Mode Tolerance Register – Index 02 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ CPU_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit1）, unit is 100 RPM.

9.122 AUXFAN0 RPM Mode Tolerance Register – Index 03 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ AUX0_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit2）, unit is 100 RPM.

9.123 Enable RPM High Mode Register – Index 06 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7-3	2	1	0
NAME	RESERVED	En_AUX0_RPM_HIGH	En_CPU_RPM_HIGH	En_SYS_RPM_HIGH
DEFAULT	0	0	0	0

BIT	DESCRIPTION
7-3	**RESERVED**
2	**En_AUX0_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable

1	**En_CPU_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
0	**En_SYS_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable

9.124 SMIOVT1 Temperature Source Select Register – Index 21 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					SMIOVT_SRC1		
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-3	**RESERVED**
2-0	**SMIOVT1 Temperature selection.** 0 0 0: Select **Local Temp** as Temperature 1 monitoring source. 0 0 1: Select **CPUTIN** as Temperature 1 monitoring source. (Default) 0 1 0: Select **AUXTIN2** as Temperature 1 monitoring source. 0 1 1: Select **AUXTIN0** as Temperature 1 monitoring source. 1 0 0: Select **AUXTIN1** as Temperature 1 monitoring source. 1 0 1: Select **PECI Agent 0** Calibration as Temperature 1 monitoring source. 1 1 0: Select **PECI Agent 1** Calibration as Temperature 1 monitoring source. 1 1 1: Select **SYSTIN** as Temperature 1 monitoring source.

9.125 SMIOVT2 Temperature Source Select Register – Index 22 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					SMIOVT_SRC2		
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-3	**RESERVED**
2-0	**SMIOVT2 Temperature selection.**

	0 0 0: Select **Local Temp** as Temperature 2 monitoring source. 0 0 1: Select **CPUTIN** as Temperature 2 monitoring source. 0 1 0: Select **AUXTIN2** as Temperature 2 monitoring source. (Default) 0 1 1: Select **AUXTIN0** as Temperature 2 monitoring source. 1 0 0: Select **AUXTIN1** as Temperature 2 monitoring source. 1 0 1: Select **PECI Agent 0** Calibration as Temperature 2 monitoring source. 1 1 0: Select **PECI Agent 1** Calibration as Temperature 2 monitoring source. 1 1 1: Select **SYSTIN** as Temperature 2 monitoring source.

9.126 (SYSFANIN) Fan Count Limit High-byte Register – Index 3Ah (Bank 6)

Attribute: Read /Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN1_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN1_HL:** 13-bit SYSFANIN Fan Count Limit, High Byte

9.127 (SYSFANIN) Fan Count Limit Low-byte Register – Index 3Bh (Bank 6)

Attribute: Read /Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN1_HL [4:0]				
DEFAULT	0			1	1	1	1	1

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN1_HL:** 13-bit SYSFANIN Fan Count Limit, Low Byte

9.128 (CPUFANIN) Fan Count Limit High-byte Register – Index 3Ch (Bank 6)

Attribute: Read /Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN2_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN2_HL:** 13-bit CPUFANIN Fan Count Limit, High Byte

9.129 (CPUFANIN) Fan Count Limit Low-byte Register – Index 3Dh (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN2_HL [4:0]				
DEFAULT	0			1	1	1	1	1

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN2_HL:** 13-bit CPUFANIN Fan Count Limit, Low Byte

9.130 (AUXFANIN0) Fan Count Limit High-byte Register – Index 3Eh (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN3_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN3_HL:** 13-bit AUXFANIN0 Fan Count Limit, High Byte

9.131 (AUXFANIN0) Fan Count Limit Low-byte Register – Index 3Fh (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN3_HL [4:0]				
DEFAULT	0			1	1	1	1	1

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN3_HL:** 13-bit AUXFANIN0 Fan Count Limit, Low Byte

9.132 (AUXFANIN1) Fan Count Limit High-byte Register – Index 40h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN4_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN4_HL:** 13-bit AUXFANIN1 Fan Count Limit, High Byte

9.133 (AUXFANIN1) Fan Count Limit Low-byte Register – Index 41h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN4_HL [4:0]				
DEFAULT	0			1	1	1	1	1

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN4_HL:** 13-bit AUXFANIN1 Fan Count Limit, Low Byte

9.134 SYSFANIN Revolution Pulses Selection Register – Index 44h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan1_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**SYSFANIN Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.135 CPUFANIN Revolution Pulses Selection Register – Index 45h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan2_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**CPUFANIN Revolution Pulses Selection**

	= 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.136 AUXFANIN0 Revolution Pulses Selection Register – Index 46h (Bank 6)

Attribute: Read /Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan3_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**AUXFANIN0 Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.137 AUXFANIN1 Revolution Pulses Selection Register – Index 47h (Bank 6)

Attribute: Read /Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan4_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**AUXFANIN1 Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.138 SMIOVT1 Temperature 1 Ctritical Limit Register – Index 50h (Bank6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT1_CT<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMIOVT1_CT<7:0>.** Temperature 1 high limit bits 7-0. The 8-bit value is in units of 1°C, and the default is 0°C.

9.139 SMIOVT1 Temperature 1 Ctritical Limit Hysteresis Register – Index 51h (Bank6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT1_CTH<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMIOVT1_CTH<7:0>.** Temperature 1 hysterisis limit bits 7-0. The 8-bit value is in units of 1°C, and the default is 0°C.

9.140 SMIOVT2 Temperature 2 Ctritical Limit Register – Index 52h (Bank6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT2_CT<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMIOVT2_CT<7:0>.** Temperature 1 high limit bits 7-0. The 8-bit value is in units of 1°C, and the default is 0°C.

9.141 SMIOVT2 Temperature 2 Ctritical Limit Hysteresis Register – Index 53h (Bank6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT2_CTH<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMIOVT2_CTH<7:0>.** Temperature 2 hysterisis limit bits 7-0. The 8-bit value is in units of 1°C, and the default is 0°C.

9.142 PECI Function Control Registers – Index 01 ~ 04h (Bank 7)

9.143 PECI Enable Function Register – Index 01h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI_En	Reserved					Manual_En	Routine_En
DEFAULT	0	0	0	1	0	0	0	0

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable PECI Function. (**PECI_En**)
6 ~ 2	R / W	Reserved
1	R / W	Enable PECI 3.0 Manual Function (**Manual_En**) (**One-shot clear**)
0	R / W	Enable PECI 3.0 Routine Function (**Routine_En**)

9.144 PECI Timing Config Register – Index 02h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		TN_Extend		Adj[2:0]			PECI_DC
DEFAULT	0	0	0	0	0	0	1	0

BIT	READ / WRITE	DESCRIPTION
7 ~ 6	R / W	Reserve
5	R / W	**TN_Extend[1:0]** Adjust Transaction Rate. 00_{BIN} = 1.5 MHz (Default) 01_{BIN} = 750 KHz 10_{BIN} = 375 KHz 11_{BIN} = 187.5 KHz
4	R / W	
3	R / W	**Adj[2:0]** Compensate the effect of rising time on physical bus Default Value = 001
2	R / W	
1	R / W	
0	R / W	Adjust PECI Tbit Duty cycle selection. **(PECI_DC)** 0 = 75% Tbit high duty cycle time. (Default) 1 = 68% Tbit high duty cycle time.

9.145 PECI Temperature Config Register – Index 04h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	En_Agt[1:0]		Domain1_Agt1	Domain1_Agt0	Clamp	RtDmn_Agt[1:0]		RtHigher
DEFAULT	0	0	0	0	0	0	0	0

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	**En_Agt[1:0] Enable Agent** 00 = Disable Agent. 01= Enable Agent0. 10 = Reserved. 11 = Enable Agent0 and Agent1.
5	R / W	Enable domain 1 for Agent1 0 = Agent1 without domain1 1 = Agent1 with domain 1
4	R / W	Enable domain 1 for Agent0 0 = Agent0 without domain 1 1 = Agent0 with domain 1
3	R / W	When temperature data reading is positive or less than -128, can enable this function to clamp temperature data.(**Clamp**)
2	R / W	**RtDmn_Agt[1:0]** Agent 1 – Agent 0 always return the relative domain Temperature. 0 = Agent always returns the relative temperature from domain 0. 1 = Agent always returns the relative temperature from domain 1.
1	R / W	
0	R / W	Return High Temperature of doamin0 or domain1.(**RtHigher**) 0 = The temperature of each agent is returned from domain 0 or domain 1, which is controlled by (CR 04_{HEX}) 1 = Return the highest temperature in domain 0 and domain 1 of individual Agent.

9.146 PECI Command Write Data Registers – Index 08 ~ 1Eh (Bank 7)

9.147 PECI Command Code Register – Index 08h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			PECI Command Code				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~5	RESERVED
4~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.148 PECI Command Tbase0 Register – Index 09h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Tbase 0						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.149 PECI Command Tbase1 Register – Index 0Ah (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Tbase 1						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.150 PECI Command Write Data 1 Register – Index 0Bh (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.151 PECI Command Write Data 2 Register – Index 0Ch (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.152 PECI Command Write Data 3 Register – Index 0Dh (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.153 PECI Command Write Data 4 Register – Index 0Eh (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.154 PECI Command Write Data 5 Register – Index 0Fh (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.155 PECI Command Write Data 6 Register – Index 10h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	PECI Write Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.156 PECI Command Write Data 7 Register – Index 11h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 7							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.157 PECI Command Write Data 8 Register – Index 12h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.158 PECI Command Write Data 9 Register – Index 13h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.159 PECI Command Write Data 10 Register – Index 14h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 10							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.160 PECI Command Write Data 11 Register – Index 15h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 11							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.161 PECI Command Write Data 12 Register – Index 16h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 12							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.162 PECI Agent Relative Temperature Register (ARTR) – Index 17h-1Eh (Bank 7)

These registers return the **"raw data"** retrieved from PECI GetTemp() command. These data could be the error codes (range: 8000H~81FFH) or relative temperatures to process the defined Tbase. The error code will only be update in **ARTR**; while "Temperature Reading Register", Bank7 Index 20h and 21h, will not be updated when the error code is received. If the **RtHigher** mechanism is activated, the normal temperature will always be returned first. In case both 2 domains return errors, the return priority will be Overflow Error > Underflow Error > Missing Diode > General Error. The reset value is $8001_{HEX,}$ in that PECI is defaulted to be off. In PECI, 8001_{HEX} means the diode is missing.

Attribute: Read

ADDRESS 17-1E	DESCRIPTION
17h[15:8],18h[7:0]	Domain0 Relative Temperature Agent0 [15:0]
19h[15:8],1Ah[7:0]	Domain1 Relative Temperature Agent0 [15:0]
1Bh[15:8],1Ch[7:0]	Domain0 Relative Temperature Agent1 [15:0]
1Dh[15:8],1Eh[7:0]	Domain1 Relative Temperature Agent1 [15:0]

GetTemp() PECI Temperature format:

BIT	DESCRIPTION
15	Sign Bit. **(Sign)** In PECI Protocol, this bit should always be 1 to represent a negative temperature.
14-6	The integer part of the relative temperature. (**Temperature[8:0]**)
5	**TEMP_2**. 0.5℃ unit.
4	**TEMP_4**. 0.25℃ unit.
3	**TEMP_8**. 0.125℃ unit.
2	**TEMP_16**. 0.0625℃ unit.
1	**TEMP_32**. 0.03125℃ unit.
0	**TEMP_64**. 0.015625℃ unit.

GetTemp() Response Definition:

RESPONSE	MEANING
General Sensor Error (GSE)	Thermal scan did not complete in time. Retry is appropriate.
0x0000	Processor is running at its maximum temperature or is currently being reset.
All other data	Valid temperature reading, reported as a negative offset from the TCC activation temperature. The valide temperature reading is referred to GetTemp() PECI Temperature format

Error Code	Description	Host operation
8000_{HEX}	General Sensor Error	No further processing.
8001_{HEX}	Sensing Device Missing	

8002_{HEX}	Operational, but the temperature is lower than the sensor operation range.	Compulsorily write 0℃ back to the temperature readouts.
8003_{HEX}	Operational, but the temperature is higher than the sensor operation range.	Compulsorily write 127℃ back to the temperature readouts.
8004_{HEX} ~ $81FF_{HEX}$	Reserved.	No further operation.

9.163 PECI Command Read Data Registers – Index 20 ~ 32h (Bank 7)

9.164 PECI Temperature Reading Register (Integer) – Index 20h (Bank 7)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Temperature Reading---Integer [9:2]							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION
7~0	**Temperature value [9] (Sign bit)** **Temperature value [8:2] (Integer bits)** Temperature value [1:0] (Fraction bits)

Note. Temperature reading register is count from raw data and Tbase, for example:

Raw data	+	*Tbase*	=	*Temp Reading*
Bank7, Index [17][18]	+	**Bank7, Index [09]**	=	**Bank7, Index [20][21]**

9.165 PECI Temperature Reading Register (Fraction) – Index 21h (Bank 7)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECI Temperature Vaule[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Temperature value [9] (Sign bit) Temperature value [8:2] (Integer bits)

BIT	DESCRIPTION
	Temperature value [1:0] (Fraction bits)

9.166 PECI Command TN Count Value Register – Index 22h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Timing Negotiation count Value[7:0]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.167 PECI Command TN Count Value Register – Index 23h (Bank 7)

Attribute: Read only
Size: 8 bits
Record which agentis able to respond to Ping().**Default value is 00_{HEX}.**
1: agent is able to respond to Ping() command. Agent alive
0: agent isn't able to respond to Ping() command. Agent is not alive

BIT	7	6	5	4	3	2	1	0
NAME	Alert Value[1:0]		PECI Alive Agent		PECI Timing Negotiation count Value[11:8]			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~6	**Agent Alert Bit** (Default value is 0) 0: Agent has valid FCS. 1: Agent has invalid FCS in the previous 3 transactions. DEFAULT VALUE IS 00_{HEX}.
5	1: agent1 is able to respond to Ping() command. Agent alive 0: agent1 isn't able to respond to Ping() command. Agent is not alive
4	1: agent0 is able to respond to Ping() command. Agent alive 0: agent0 isn't able to respond to Ping() command. Agent is not alive
3~0	The data would be get from client. **Default value is 00_{HEX}.**

9.168 PECI Command FCS Data Register – Index 25h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserve		Warning	CC_Fail	ZeroWFCS	AbortWFCS	BadRFCS	BadWFCS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
5~0	Retrieve PECI related data from client and host. **Default value is 00_{HEX}.**

9.169 PECI Command Read Data 1 Register – Index 2Ah (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.170 PECI Command Read Data 2 Register – Index 2Bh (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.171 PECI Command Read Data 3 Register – Index 2Ch (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.172 PECI Command Read Data 4 Register – Index 2Dh (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.173 PECI Command Read Data 5 Register – Index 2Eh (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.174 PECI Command Read Data 6 Register – Index 2Fh (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.175 PECI Command Read Data 7 Register – Index 30h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 7							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.176 PECI Command Read Data 8 Register – Index 31h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.177 PECI Command Read Data 9 Register – Index 32h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

PECI Manual Command Address Table

Command Bank 7	Address	WriteLength	Read Length	Command	CR 08_{HEX}
Ping()	30/31	00	00	00	5'bx_x000
GetDIB()		01	08	F7	5'bx_x001
GetTemp()		01	02	01/02	5'bx_x010

RdPkgConfig()		**05**	**05**	**A1/A2**	**5'bx_x100**
WrPkgConfig()		**0A**	**01**	**A5/A6**	**5'bx_x101**
RdIAMSR()		**05**	**09**	**B1/B2**	**5'bx_x011**

CR08[4]: 0，Address = 30。

CR08[4]: 1，Address = 31。

CR08[3]: 0，Command = 01/A1/A5/B1。

CR08[3]: 1，Command = 02/A2/A6/B2。

PECI Manual Command Read Data Table

Command	**RdPkgConfig()**	**WrPkgConfig()**	**RdIAMSR()**	**GetDIB()**	**GetTemp()**
Command Code	**A1**	**A5**	**B1**	**F7**	**01**
RdData 1 CR 2A$_{HEX}$	Ccode	Ccode	Ccode	X	X
RdData 2 CR 2B$_{HEX}$	X	X	Data LSB_1	Device Info	X
RdData 3 CR 2C$_{HEX}$	X	X	Data LSB_2	Revision Number	X
RdData 4 CR 2D$_{HEX}$	X	X	Data LSB_3	Reserved 1	X
RdData 5 CR 2E$_{HEX}$	X	X	Data LSB_4	Reserved 2	X
RdData 6 CR 2F$_{HEX}$	Data LSB_1	X	Data LSB_5	Reserved 3	X
RdData 7 CR 30$_{HEX}$	Data LSB_2	X	Data LSB_6	Reserved 4	X
RdData 8 CR 31$_{HEX}$	Data LSB_3	X	Data LSB_7	Reserved 5	Temp_LB
RdData 9 CR 32$_{HEX}$	Data MSB	X	Data MSB	Reserved 6	Temp_HB

PECI Manual Command Write Data Table

Command	**RdPkgConfig()**	**WrPkgConfig()**	**RdIAMSR()**
Command Code	**A1**	**A5**	**B1**
WrData 1 CR 0B$_{HEX}$	Host ID	Host ID	Host ID
WrData 2 CR 0C$_{HEX}$	Index	Index	Processor ID
WrData 3	Param	Param	Addr

CR 0D$_{HEX}$	LSB	LSB	LSB
WrData 4 **CR 0E$_{HEX}$**	Param MSB	Param MSB	Addr MSB
WrData 5 **CR 0F$_{HEX}$**	X	Data LSB_1	X
WrData 6 **CR 10$_{HEX}$**	X	Data LSB_2	X
WrData 7 **CR 11$_{HEX}$**	X	Data LSB_3	X
WrData 8 **CR 12$_{HEX}$**	X	Data MSB	X
WrData 9 **CR 13$_{HEX}$**	X	X	X
WrData10 **CR 14$_{HEX}$**	X	X	X
WrData11 **CR 15$_{HEX}$**	X	X	X
WrData12 **CR 16$_{HEX}$**	X	X	X

9.178 Fast Access IO Space register

Some hardware monitor registers are served as fast access register for LPC via second hardware monitor I/O port. The related I/O base address is set by hardware monitor CR64 & CR65. The registers are list below:

Base Address +	Name	Attr	7	6	5	4	3	2	1	0
0	Voltage CPUVCORE ReadOut	R	CPUVCORE reading							
1	Voltage VIN0 ReadOut	R	VIN0 reading							
2	Voltage AVCC ReadOut	R	AVCC reading							
3	Voltage 3VCC Readout	R	3VCC reading							
4	Voltage VIN1 Readout	R	VIN1 reading							
5	Voltage VTT Readout	R	VTT reading							
6	Voltage VSB3V Readout	R	VSB3V reading							
7	Voltage VBAT Readout	R	VBAT reading							
8	Voltage VIN4 Readout	R	VIN4 reading.							
9	Voltage VIN2 Readout	R	VIN2 reading.							
A	Voltage VIN3 Readout	R	VIN3 reading.							
10	CUPTIN Byte	R	MNTRTD1							
11	AUXTIN2 Byte	R	MNTRTD2							
12	AUXTIN0 Byte	R	MNTRTD3							

13	AUXTIN1 Byte	R	MNTRTD4
14	SYSTIN Byte	R	MNTRTD5
15	LTD Byte	R	MNTLTD
19	Fan Control Temp high temp SYS	R	FanControlTemp_SYS
1A	Fan Control Temp high temp	R	FanControlTemp_CPU
1B	Fan Control Temp high temp AUX0	R	FanControlTemp_AUX0
1C	SMIOVT_Temp1	R	FanControlTemp_AUX1
1D	SMIOVT_Temp2	R	FanControlTemp_AUX2
21	Weighting Temp CPU	R	CPU_WT_Temp
23	FAN Target CPU	R	FanTarget_CPU
24	FAN Target AUX0	R	FanTarget_AUX0
25	Fan Target AUX1	R	FanTarget_AUX1
28	Rpm Target SYS	R	RpmTarget_SYS
29	Rpm Target CPU	R	RpmTarget_CPU
2A	Rpm Target AUX0	R	RpmTarget_AUX0
2E	(SYSFANIN) FANCNT1 High-byte	R	FANCNT1 [12:5]
2F	(SYSFANIN) FANCNT1 Low-byte	R	FANCNT1 [4:0]
30	(CPUFANIN) FANCNT2 High-byte	R	FANCNT2 [12:5]
31	(CPUFANIN) FANCNT2 Low-byte	R	FANCNT2 [4:0]
32	(AUXFANIN0) FANCNT3 High-byte	R	FANCNT3 [12:5]
33	(AUXFANIN0) FANCNT3 Low-byte	R	FANCNT3 [4:0]
34	(AUXFANIN1) FANCNT4 High-byte	R	FANCNT4 [12:5]
35	(AUXFANIN1) FANCNT4 Low-byte	R	FANCNT4 [4:0]
3A	MNTVAL SYSRPM High Byte	R	MNTVAL_RPM1[15:8]
3B	MNTVAL SYSRPM Low Byte	R	MNTVAL_RPM1[7:0]
3C	MNTVAL CPURPM High Byte	R	MNTVAL_RPM2[15:8]
3D	MNTVAL CPURPM Low Byte	R	MNTVAL_RPM2[7:0]
3E	MNTVAL AUX0RPM High Byte	R	MNTVAL_RPM3[15:8]
3F	MNTVAL AUX0RPM Low Byte	R	MNTVAL_RPM3[7:0]
40	MNTVAL AUX1RPM High Byte	R	MNTVAL_RPM4[15:8]
41	MNTVAL AUX1RPM Low Byte	R	MNTVAL_RPM4[7:0]
46	MAX RPM SYS high byte	R	MAX_RPM_SYS[15:8]
47	MAX RPM SYS low byte	R	MAX_RPM_SYS[7:0]
48	MAX RPM CPU high byte	R	MAX_RPM_CPU[15:8]
49	MAX RPM CPU low byte	R	MAX_RPM_CPU[7:0]
4A	MAX RPM AUX0 high byte	R	MAX_RPM_AUX0[15:8]
4B	MAX RPM AUX0 low byte	R	MAX_RPM_AUX0[7:0]

4C	SYSFANOUT Output Value Select	R	MUX_Duty_1
4D	CPUFANOUT Output Value Select	R	MUX_Duty_2
4E	AUXFANOUT Output Value Select	R	MUX_Duty_3
52	PECI Agent0 temperature	R	MNTPECI0
54	PECI Agent1 temperature	R	MNTPECI1
71	PECI Cali0	R	PECI Agent0 Calibration
72	PECI Cali1	R	PECI Agent1 Calibration

10. UART PORT

10.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.

BIT	7	6	5	4	3	2	1	0
NAME	BDLAB	SSE	PBFE	EPE	PBE	MSBE	DLS1	DLS0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**BDLAB (Baud Rate Divisor Latch Access Bit).** When this bit is set to logic 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logic 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.
6	**SSE (Set Silence Enable).** A logic 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.
5	**PBFE (Parity Bit Fixed Enable).** When PBE and PBFE of UCR are both set to logic 1, (1) if EPE is logic 1, the parity bit is logical 0 when transmitting and checking; (2) if EPE is logic 0, the parity bit is logical 1 when transmitting and checking.
4	**EPE (Even Parity Enable).** When PBE is set to logic 1, this bit counts the number of logic 1's in the data word bits and determines the parity bit. When this bit is set to logic 1, the parity bit is set to logic 1 if an even number of logic 1's are sent or checked. When the bit is set to logic 0, the parity bit is logic 1, if an odd number of logic 1's are sent or checked.
3	**PBE (Parity Bit Enable).** When this bit is set to logic 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.
2	**MSBE (Multiple Stop Bit Enable).** Defines the number of stop bits in each serial character that is transmitted or received. (1) If MSBE is set to logic 0, one stop bit is sent and checked. (2) If MSBE is set to logic 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked. (3) If MSBE is set to logic 1 and the data length is 6, 7, or 8 bits, two stop bits are sent and checked.
1	**DLS1 (Data Length Select Bit 1).** Defines the number of data bits that are sent or checked in each serial character.
0	**DLS0 (Data Length Select Bit 0).** Defines the number of data bits that are sent or checked in each serial character.

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits

DLS1	DLS0	DATA LENGTH
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Table 10-1 Register Summary for UART

Bit Number										
Register Address Base			**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 Mode.

10.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.

BIT	7	6	5	4	3	2	1	0
NAME	RF EI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
DEFAULT	0	1	1	0	0	0	0	0

BIT	DESCRIPTION
7	**RF EI (RX FIFO Error Indication).** In 16450 mode, this bit is always set to logical 0. in 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop0bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.
6	**TSRE (Transmitter Shift Register Empty).** In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.
5	**TBRE (Transmitter Buffer Register Empty).** In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI of ICR is high, and interrupt is generated to notify the CPU to write next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.
4	**SBD (Silent Byte Detected).** This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
3	**NSER (No Stop Bit Error).** This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
2	**PBER (Parity Bit Error).** This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
1	**OER (Overrun Error).** This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.
0	**RDR (RBR Data Ready).** This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

10.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			INTERNAL LOOPBACK ENABLE	IRQ ENABLE	LOOPBACK RI INPUT	RTS	DTR
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.**
4	**Internal Loopback Enable.** When this bit is set to logic 1, the UART enters diagnostic mode, as follows: (1) SOUT is forced to logic 1, and SIN is isolated from the communication link. (2) The modem output pins are set to their inactive state. (3) The modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) →DSR#, RTS (bit 1 of HCR) →CTS#, Loopback RI input (bit 2 of HCR) → RI# and IRQ enable (bit 3 of HCR) →DCD#. Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.
3	**IRQ Enable.** The UART interrupt output is enabled by setting this bit to logic 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.
2	**Loopback RI Input.** This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.
1	**RTS (Request to Send).** This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.
0	**DTR (Data Terminal Ready).** This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

10.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins used with handshake peripherals such as modems and records changes on these pins.

BIT	7	6	5	4	3	2	1	0
NAME	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
DEFAULT	NA	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DCD (Data Carrier Detect).** This bit is the inverse of the DCD# input and is equivalent to bit 3 of HCR in Loopback mode.
6	**RI (Ring Indicator).** This bit is the inverse of the RI# input and is equivalent to bit 2 of HCR in Loopback mode.
5	**DSR (Data Set Ready).** This bit is the inverse of the DSR# input and is equivalent to bit 0 of HCR in Loopback mode.
4	**CTS (Clear to Send).** This bit is the inverse of the CTS# input and is equivalent to bit 1 of HCR in Loopback mode.
3	**TDCD (DCD# Toggling).** This bit indicates that the state of the DCD# pin has changed after HSR is read by the CPU.
2	**FERI (RI Falling Edge).** This bit indicates that the RI# pin has changed from low to high after HSR is read by the CPU.
1	**TDSR (DSR# Toggling).** This bit indicates that the state of the DSR# pin has changed after HSR is read by the CPU.
0	**TCTS (CTS# Toggling).** This bit indicates that the state of the CTS# pin has changed after HSR is read by the CPU.

10.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	MSB	LSB	RESERVED		DMA MODE SELECT	TRANSMITTER FIFO RESET	RECEIVER FIFO RESET	FIFO ENABLE
DEFAULT	0	0	NA	NA	0	0	0	0

BIT	DESCRIPTION	
7	**MSB (RX Interrupt Active Level).**	These two bits are used to set the active level of the receiver FIFO interrupt. The active level is the number of bytes that must be in the receiver FIFO to generate an interrupt.
6	**LSB (RX Interrupt Active Level).**	
5-4	**RESERVED.**	
3	**DMS MODE SELECT.** When this bit is set to logic 1, DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.	
2	**TRANSMITTER FIFO RESET.** Setting this bit to logic 1 resets the TX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
1	**RECEIVER FIFO RESET.** Setting this bit to logic 1 resets the RX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
0	**FIFO ENABLE.** This bit enables 16550 (FIFO) mode. This bit should be set to logic 1 before other UFR bits are programmed.	

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

10.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status.

BIT	7	6	5	4	3	2	1	0
NAME	FIFOS ENABLED		RESERVED		INTERRUPT STATUS BIT 2	INTERRUPT STATUS BIT 1	INTERRUPT STATUS BIT 0	0 IF INTERRUPT PENDING
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	**FIFOS ENABLED.** Set to logical 1 when UFR, bit 0 = 1.
5-4	**RESERVED.**

3	**INTERRUPT STATUS BIT 2.** In 16450 mode, this bit is logical 0. In 16550 mode, bits 3 and 2 are set to logical 1 when a time-out interrupt is pending. Please see the table below.	
2	**INTERRUPT STATUS BIT 1.**	These two bits identify the priority level of the pending interrupt, as shown in the table below.
1	**INTERRUPT STATUS BIT 0.**	
0	**0 IF INTERRUPT PENDING.** This bit is logic 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.	

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

10.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.

BIT	7	6	5	4	3	2	1	0
NAME	En_address_byte	RX_ctrl	RESERVED		EHSRI	EUSRI	ETBREI	ERDRI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En_address_byte.** 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	**RX_ctrl.** 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)
5-4	**RESERVED.**
3	**EHSRI (Handshake Status Interrupt Enable).** Set this bit to logical 1 to enable the

BIT	DESCRIPTION
	handshake status register interrupt.
2	**EUSRI (UART Receive Status Interrupt Enable).** Set this bit to logical 1 to enable the UART status register interrupt.
1	**ETBREI (TBR Empty Interrupt Enable).** Set this bit to logical 1 to enable the TBR empty interrupt.
0	**ERDRI (RBR Data Ready Interrupt Enable).** Set this bit to logical 1 to enable the RBR data ready interrupt.

10.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divide it by a divisor from 1 to (2^{16} –1). The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (CRF0, bits 1 and 0), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. As a result, in high-speed mode, the data transmission rate can be as high as 1.5M bps.

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
PRE-DIV: 13 1.8461M HZ	**PRE-DIV:1.625 14.769M HZ**	**PRE-DIV: 1.0 24M HZ**	**DECIMAL DIVISOR USED TO GENERATE 16X CLOCK**	**ERROR PERCENTAGE**
50	400	650	2304	**
75	600	975	1536	**
110	880	1430	1047	0.18%
134.5	1076	1478.5	857	0.099%
150	1200	1950	768	**
300	2400	3900	384	**
600	4800	7800	192	**
1200	9600	15600	96	**
1800	14400	23400	64	**
2000	16000	26000	58	0.53%
2400	19200	31200	48	**
3600	28800	46800	32	**
4800	38400	62400	24	**
7200	57600	93600	16	**
9600	76800	124800	12	**
19200	153600	249600	6	**
38400	307200	499200	3	**
57600	460800	748800	2	**
115200	921600	1497600	1	**

** Unless specified, the error percentage for all of the baud rates is 0.16%.

Note: Pre-Divisor is determined by CRF0 of UART A and B.

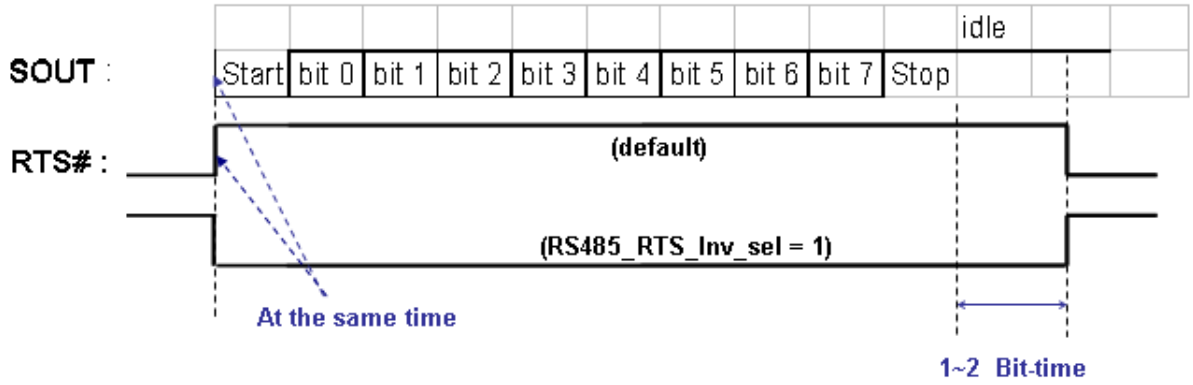
10.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

10.10 UART RS485 Auto Flow Control

NCT5569D supports RS485 auto flow control function for UARTA. When enabling the RS485 auto control function, it will automatically drive RTS# pin to logic high or low for UARTA when UART TX block transmits the data.

The diagram shown below illustrates the RS485 auto flow control function for UARTA.



The default behavior of RTS# pin will drive logic high the time edge between **Start bit** and **bit0** when the UART TX Block start to transmits the data on SOUT pin. Then the RTS# pin will drive logic low later than **Stop bit** about 1~2 x Bit-time when UART TX Block completes the data transmission. The driving behavior of RTS# will be inverted when we set RS485_RTS_inv_sel bit = 1'b1. (Bit-time: Depends on the baud rate of transmission)

The bellowing control register table relates to the RS485 auto flow control function for UARTA.

	UARTA
RTS485_enable	Logic Device 2, CRF2_Bit7
RTS485_inv_sel	Logic Device 2, CRF2_Bit6

11. KEYBOARD CONTROLLER

The NCT5569D KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.

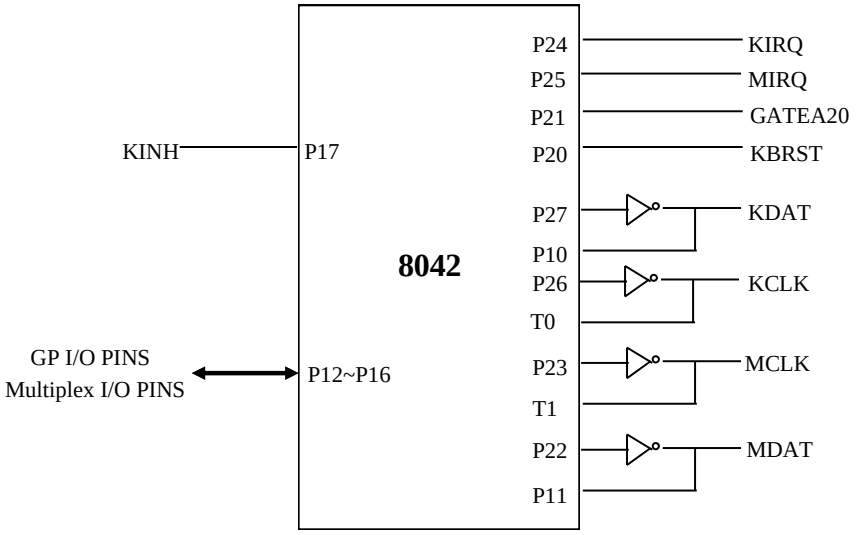


Figure 11-1 Keyboard and Mouse Interface

11.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60H (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

11.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

11.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64h (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

Table 11-1 Bit Map of Status Register

BIT	BUT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

11.4 Commands

Table 11-2 KBC Command Sets

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte of Keyboard Controller</td></tr>
<tr><td>60h</td><td>Write Command Byte of Keyboard Controller
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>7</td><td>Reserved</td></tr>
<tr><td>6</td><td>IBM Keyboard Translate Mode</td></tr>
<tr><td>5</td><td>Disable Auxiliary Device</td></tr>
<tr><td>4</td><td>Disable Keyboard</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>2</td><td>System Flag</td></tr>
<tr><td>1</td><td>Enable Auxiliary Interrupt</td></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
</table></td></tr>
<tr><td>A4h</td><td>Test Password
Returns 0Fah if Password is loaded
Returns 0F1h if Password is not loaded</td></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a logical 0 is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>Aah</td><td>Self-test
Returns 055h if self-test succeeds</td></tr>
<tr><td>Abh</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Keyboard "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Keyboard "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Keyboard "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Keyboard "Data" line is stuck high</td></tr>
</table></td></tr>
</table>

COMMAND	FUNCTION
Adh	Disable Keyboard Interface
Aeh	Enable Keyboard Interface
C0h	Read Input Port (P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into the STATUS register
C2h	Continuously puts the upper four bits of Port1 into the STATUS register
D0h	Send Port 2 value to the system
D1h	Only set / reset GateA20 line based on system data bit 1
D2h	Send data back to the system as if it came from the Keyboard
D3h	Send data back to the system as if it came from Auxiliary Device
D4h	Output next received byte of data from system to Auxiliary Device
E0h	Reports the status of the test inputs
FXh	Pulse only RC (the reset line) low for 6μs if the Command byte is even

11.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

11.5.1 KB Control Register (Logic Device 5, CR-F0)

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	RESERVED			P92EN	HGA20	HKBRST#
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**KCLKS1.**	Select the KBC clock rate. **Bits** **7 6** 0 0: Reserved 0 1: Reserved 1 0: KBC clock input is 12 MHz. 1 1: Reserved
6	**KCLKS0.**	
5-3	**RESERVED.**	
2	**P92EN (Port 92 Enable).** 1: Enables Port 92 to control GATEA20 and KBRESET. 0: Disables Port 92 functions.	
1	**HGA20 (Hardware GATEA 20).** 1: Selects hardware GATE A20 control logic to control GATE A20 signal. 0: Disables GATEA20 control logic functions.	
0	**HKBRST# (Hardware Keyboard Reset).** 1: Selects hardware KB RESET control logic to control KBRESET signal. 0: Disables hardware KB RESET control logic function.	

When the KBC receives data that follows a “D1” command, the hardware control logic sets or clears GATE A20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an “FE” command, the KBRESET is pulse low for 6 μs (Min.) with a 14 μs (Min.) delay.

GATE A20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATE A20 and KBRESET are merged with Port92 when the P92EN bit is set.

11.5.2 Port 92 Control Register (Default Value = 0x24)

BIT	7	6	5	4	3	2	1	0
NAME	RES. (0)		RES. (1)	RES. (0)		RES. (1)	SGA20	PLKBRST#
DEFAULT	0	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-6	**RES. (0)**
5	**RES. (1)**
4-3	**RES. (0)**
2	**RES. (1)**
1	**SGA20 (Special GATE A20 Control)** 1: Drives GATE A20 signal to high. 0: Drives GATE A20 signal to low.
0	**PLKBRST# (Pulled-low KBRESET).** A logical 1 on this bit causes KBRESET to drive low for 6 µS(Min.) with a 14 µS(Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

12. POWER MANAGEMENT EVENT

The PME# signal is connected to the South Bridge and is used to wake up the system from S1 ~ S5 sleeping states.

One control bit and four registers in the NCT5569D are associated with the PME function. The control bit is at Logical Device A, CR[F2h], bit[0] and is for enabling or disabling the PME function. If this bit is set to "0", the NCT5569D won't output any PME signal when any of the wake-up events has occurred and is enabled. The four registers are divided into PME status registers and PME interrupt registers of wake-up events Note.1.

1) The PME status registers of wake-up event:
   - At Logical Device A, CR[F3h] and CR[F4h]
   - Each wake-up event has its own status
   - The PME status should be cleared by writing a "1" before enabling its corresponding bit in the PME interrupt registers
2) The PME interrupt registers of wake-up event:
   - At Logical Device A, CR[F6h] and CR[F7h]
   - Each wake-up event can be enabled / disabled individually to generate a PME# signal

Note.1 PME wake-up events that the NCT5569D supports include:

- Mouse event*
- Keyboard event*
- UART A IRQ event
- Hardware Monitor IRQ event
- WDT1 event
- RIA (UARTA Ring Indicator) event

Note.2 All the above support both S0 and S1 states. Events with the "*" mark also support S3 ~ S5 states.

12.1 Power Control Logic

This chapter describes how the NCT5569D implements its ACPI function via these power control pins: PSIN#, PSOUT#, SLP_S3# and PSON#. The following figure illustrates the relationships.

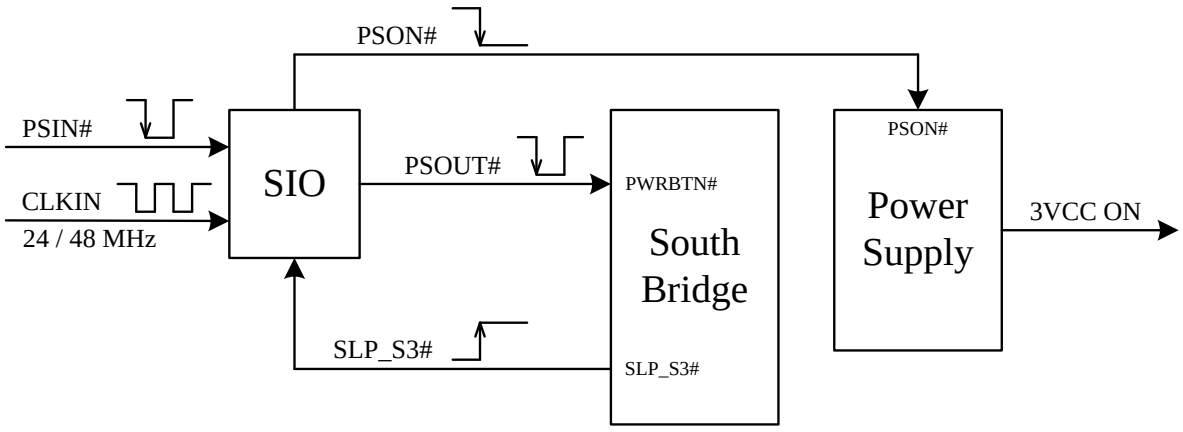


Figure 12-1 Power Control Mechanism

12.1.1 PSON# Logic

12.1.1.1. Normal Operation

The PSOUT# signal will be asserted low if the PSIN# signal is asserted low. The PSOUT# signal is held low for as long as the PSIN# is held low. The South Bridge controls the SLP_S3# signal through the PSOUT# signal. The PSON# is directly connected to the power supply to turn on or off the power.

Figure 15-2 shows the power on and off sequences.

The ACPI state changes from S5 to S0, then to S5

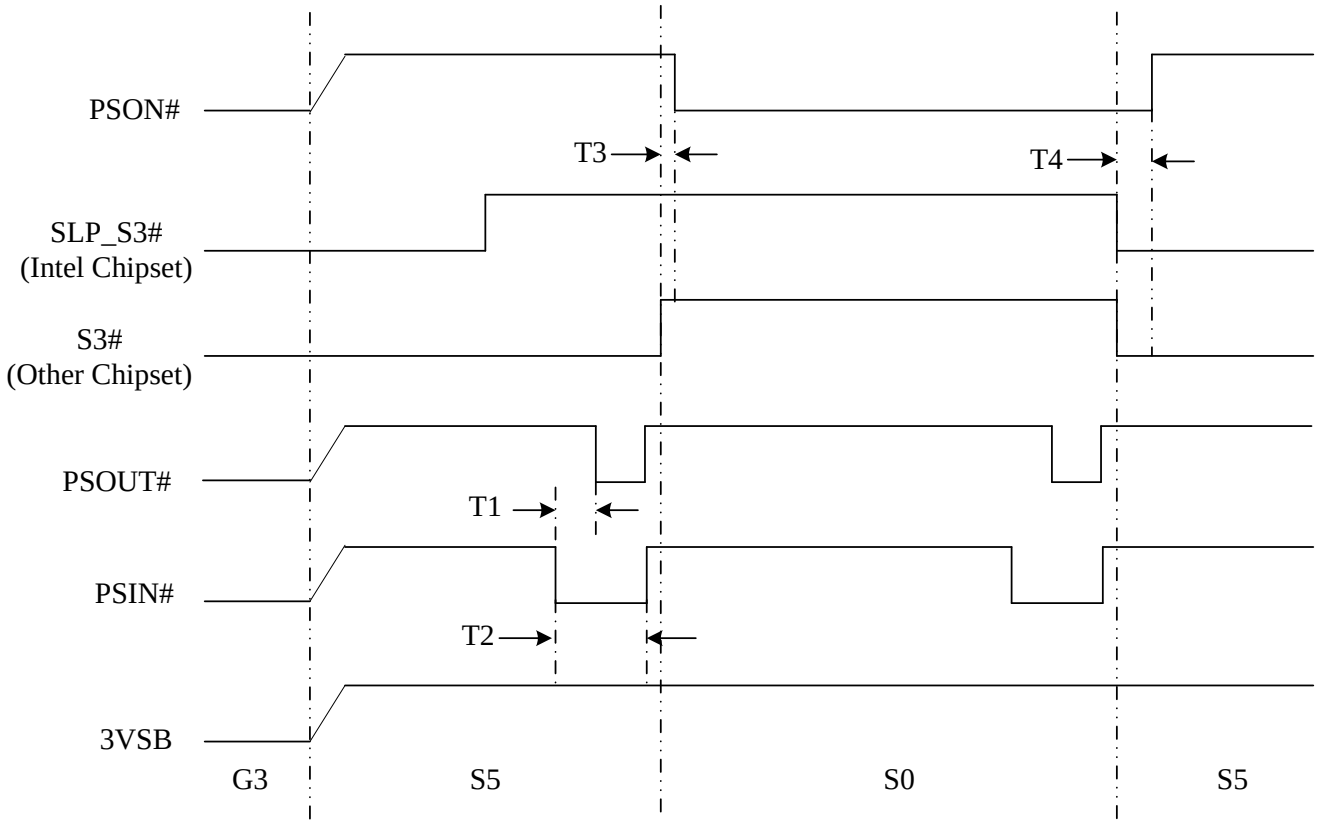


Figure 12-2 Power Sequence from S5 to S0, then Back to S5

12.1.2 AC Power Failure Resume

By definition, AC power failure means that the standby power is removed. The power failure resume control logic of the NCT5569D is used to recover the system to a pre-defined state after AC power failure. Two control bits at Logical Device A, CR[E4h], bits[6:5] indicate the pre-defined state. The definition of these two bits is listed in the following table:

Table 12-1 Bit Map of Logical Device A, CR[E4h], Bits[6:5]

LOGICAL DEVICE A, CR[E4H], BITS[6 :5]	DEFINITION
00	System always turns off when it returns from AC power failure
01	System always turns on when it returns from AC power failure
10	System turns off / on when it returns from power failure depending on the state before the power failure. (Please see Note 1)
11	User defines the state before the power failure. (The previous state is set at CRE6[4]. Please see Note 2)

Note1. The NCT5569D detects the state before power failure (on or off) through the SLP_S3# signal and the 3VCC power. The relation is illustrated in the following two figures.

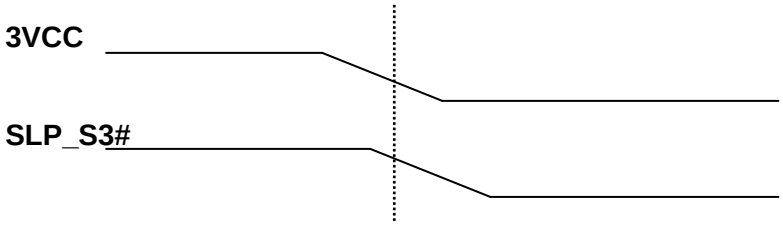


Figure 12-3 The previous state is “on”

3VCC falls to 2.6V and SLP_S3# keeps at 2.0V.

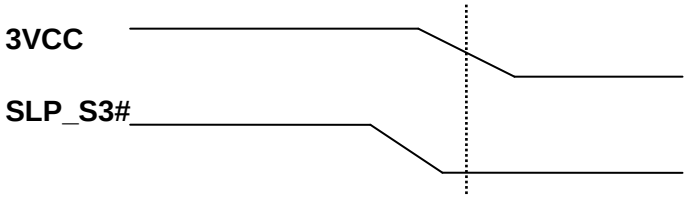


Figure 12-4 The previous state is “off”

3VCC falls to 2.6V and SLP_S3# keeps at 0.8V.

Note 2.

Logical Device A, CR[E6h] bit [4]	Definition
0	User defines the state to be “on”
1	User defines the state to be “off”

To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT5569D adds the option of “user define mode” for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be “On” or “Off”. According to this setting, the system is returned to the pre-defined state after the AC power recovery.

12.2 Wake Up the System by Keyboard and Mouse

The NCT5569D generates a low pulse through the PSOUT# pin to wake up the system when it detects a key code pressed or mouse button clicked. The following sections describe how the NCT5569D works.

12.2.1 Waken up by Keyboard events

The keyboard Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 6 to "1".

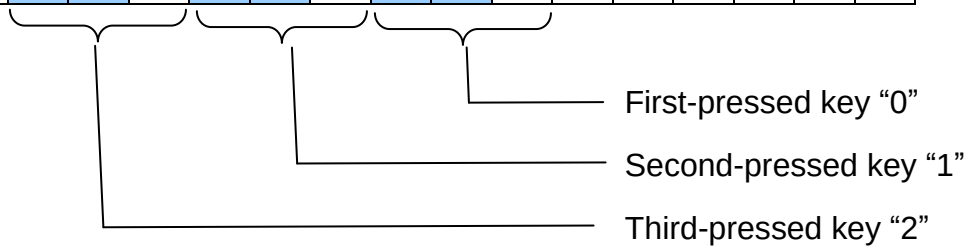
There are two keyboard events can be used for the wake-up

1) Any key – Set bit 0 at Logical Device A, CR[E0h] to "1" (Default).
2) Specific keys (Password) – Set bit 0 at Logical Device A, CR[E0h] to "0".

One set of specific key combinations are stored at Logical Device A. CR[E1h] is an index register to indicate which byte of key code storage (0x00h ~ 0x0Eh) is going to be read or written through CR[E2h]. According to IBM 101/102 keyboard specification, a complete key code contains a 1-byte make code and a 2-byte break code. For example, the make code of "0" is 0x45h, and the corresponding break code is 0xF0h, 0x45h.

The approach to implement Keyboard Password Wake-Up Function is to fill key codes into the password storage. Assume that we want to set "012" as the password. The storage should be filled as below. Please note that index 0x09h ~ 0x0Eh must be filled as 0x00h since the password has only three numbers.

Index(CRE1)→	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Data(CRE2)→	1E	F0	1E	16	F0	16	45	F0	45	00	00	00	00	00	00



12.2.2 Waken up by Mouse events

The mouse Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 5 to "1".

The following specific mouse events can be used for the wake-up:

- Any button clicked or any movement
- One click of the left or the right button
- One click of the left button
- One click of the right button
- Two clicks of the left button
- Two clicks of the right button.

Three control bits (ENMDAT_UP, MSRKEY, MSXKEY) define the combinations of the mouse wake-up events. Please see the following table for the details.

Table 12-2 Definitions of Mouse Wake-Up Events

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
1	x	1	Any button clicked or any

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
			movement.
1	x	0	One click of the left or right button.
0	0	1	One click of the left button.
0	1	1	One click of the right button.
0	0	0	Two clicks of the left button.
0	1	0	Two clicks of the right button.

12.3 Resume Reset Logic

The RSMRST# signal is a reset output and is used as the VSB power on reset signal for the South Bridge.

When the NCT5569D detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

Timing and voltage parameters are shown in Figure 15-5 and Table 15-3.

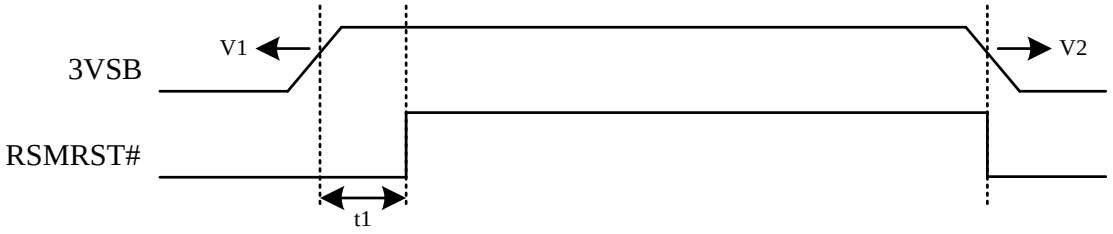


Figure 12-5 Mechanism of Resume Reset Logic

Table 12-3 Timing and Voltage Parameters of RSMRST#

NAME	PARAMETER	MIN.	MAX.	UNIT
V1	3VSB Valid Voltage	-	3.033	V
V2	3VSB Ineffective Voltage	2.882	-	V
t1	Valid 3VSB to RSMRST# inactive	200	300	mS

13. SERIALIZED IRQ

The NCT5569D supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

13.1 Start Frame

There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the NCT5569D drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the NCT5569D from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.

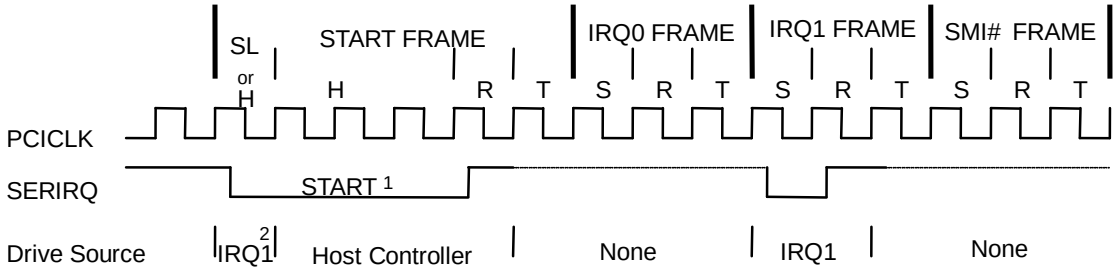


Figure 13-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1

H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the NCT5569D because IRQ1 of the NCT5569D needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

13.2 IRQ/Data Frame

Once the Start Frame has been initiated, the NCT5569D must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the NCT5569D drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the NCT5569D device drives the SERIRQ high. During the Turn-around phase, the NCT5569D device leaves the SERIRQ tri-stated. The NCT5569D starts to drive the SERIRQ line from the beginning of "IRQ0 FRAME" based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 13-1.

Table 13-1 SERIRQ Sampling Periods

SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	**SIGNAL SAMPLED**	**# OF CLOCKS PAST START**	**EMPLOYED BY**
1	IRQ0	2	Reserved
2	IRQ1	5	Keyboard
3	SMI#	8	H/W Monitor & SMI
4	IRQ3	11	Reserved
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	Reserved
8	IRQ7	23	Reserved
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	Reserved
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

13.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminates SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.

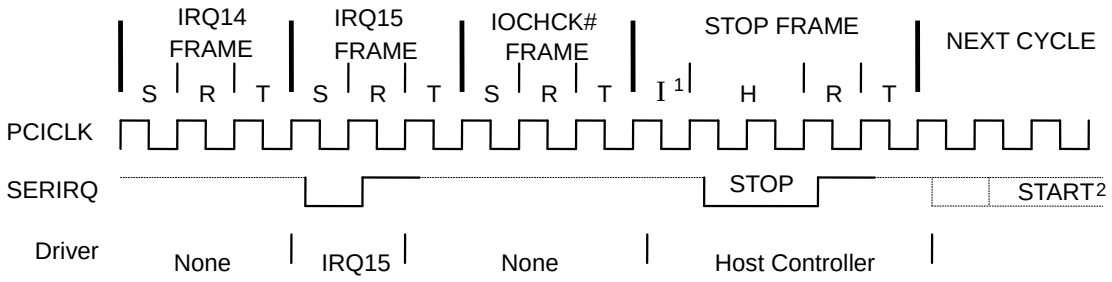


Figure 13-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period

H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

14. WATCHDOG TIMER

The Watchdog Timer 1 of the NCT5569D consists of an 8-bit programmable time-out counter and a control and status register. GPIO provides an alternative WDT1 function. This function can be configured by the relative GPIO control register. The units of Watchdog Timer counter can be selected at Logical Device 8, CR[F5h], bit[3]. The time-out value is set at Logical Device 8, CR[F6h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

When Watchdog Timer 1 time-out event is occurring, GPIO bit[0],[3], PWROK and RESETCONO# will trigger a low pulse apporx 100mS or low level by Logical Device 8 CR[F5h], bit[0] and RSMRST# will trigger a low pulse approx 250ms. The PWROK, SLP_S3# and RSMRST# event also relate to acpi sequence, that can be control by Logical Device D, CR[F0h], bit[7] and bit[0], Logical Device D, CR[F0h], bit[7] and bit[0] as 2'b00 is normal acpi function, others timing illustrations are define in Figure 14-1 to Figure 14-3 In other words, when the value is counted down to zero, the timer stops, and the NCT5569D sets the WDT1 status bit in Logical Device 8, CR[F7h], bit[4]. Writing a zero will clear the status bit. it. This bit will also be cleared if LRESET# or PWROK signal is asserted.

The Watchdog Timer 2 of the NCT5569D consists of an 8-bit programmable time-out counter register (Logic Device D, CR[EBh]) and status register (Logic Device D, CR[F3h] bit[7]). The timeout event will trigger PWROK pin to gerenate a pulse when EN_AS set to oen. CR[2Fh], bit[2] is EN_AS enable bit, and Logic Device D, CR[EDh], bit[0] is timer count down start bit. When Logic Device D, CR[EDh], bit[0] set to one or LRESET# is low more than 5 secend, the timer will start count down, until this bit is written to zero.

The Watchdog Timer 3 of the NCT5569D consists of an 8-bit programmable time-out counter and a control and status register. The units of Watchdog Timer counter can be selected at Logical Device 8, CR[F8h], bit[3]. The time-out value is set at Logical Device 8, CR[F9h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

When Watchdog Timer 3 time-out event is occurring, PWROK and RESETCONO# will trigger a low pluse apporx 100mS or low level by Logical Device 8 CR[F8h], bit[0]. In other words, when the value is counted down to zero, the timer stops, and the NCT5569D sets the WDT3 status bit in Logical Device 8, CR[FAh], bit[4]. Writing a zero will clear the status bit. it. This bit will also be cleared if LRESET# or PWROK signal is asserted.

The Watchdog Timer 4 of the NCT5569D consists of an status register (Logic Device A, CR[F3h] bit[6]). The timeout event will trigger RESETCONO pin to gerenate a pulse when WDTRST_EN set to oen. CR[2Fh], bit[0] is WDTRST_EN enable bit. When WDTRST_EN set to one, if VCC3V is good, the timer will start count down, after 5 second, the timer time-out and to issue about 100ms low pulse to trigger pin.

Watchdog Timer Time-Out Trigger Event	Watchdog Timer 1	Watchdog Timer 2	Watchdog Timer 3	Watchdog Timer 4
		EN_AS enable, 5 sec to issue PWROK if LRESET# is Low		WDTRST_EN strapping, 5 sec to issue RESETCON# if VCC3V is High
KBRST#	✓	×	×	×
PWROK	×	✓	✓	×
GPIO Pin	✓	×	×	×
RESETCONO# Pin	✓	×	✓	✓
RSMRST# Event	✓	×	×	×
PWROK Event Then Into Deep S5	✓	×	×	×
Internal SLP_S3# Event Then Into Deep S5	✓	×	×	×

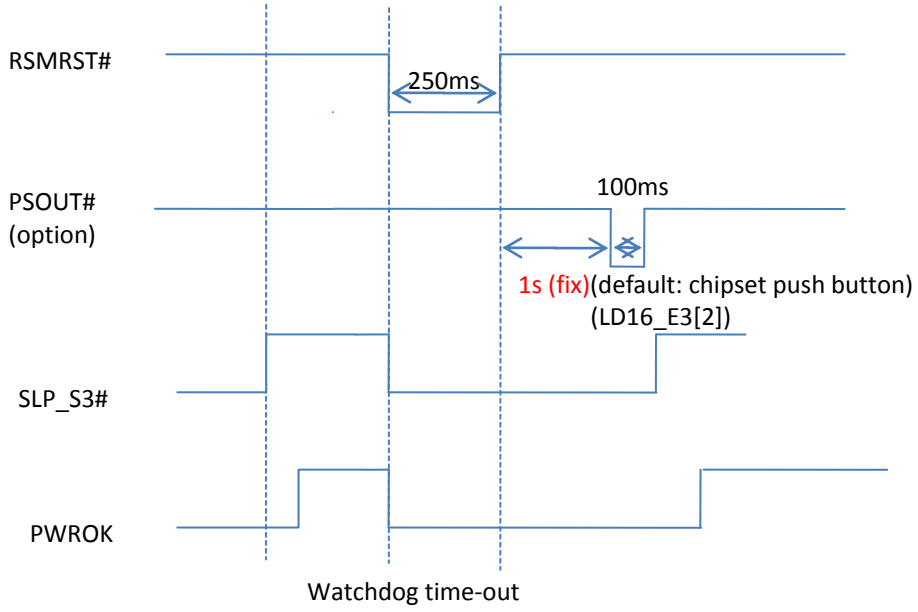


Figure 14-1 RSMRST# Event When Logical Device D CR[F0h], Bit[7] and Bit[0] as 2’b01

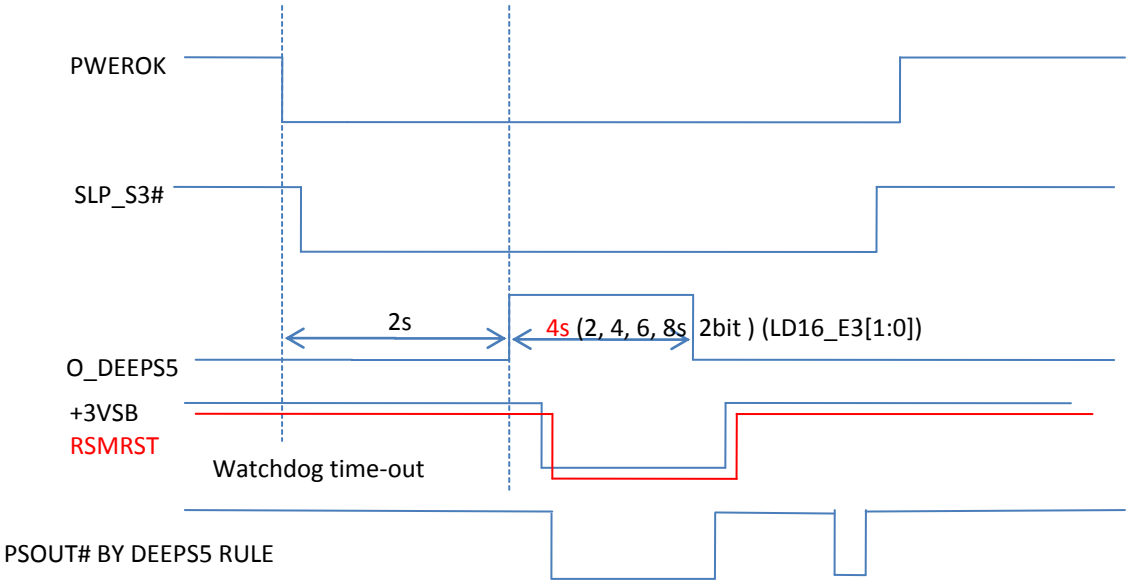


Figure 14-2 PWROK Event When Logical Device D CR[F0h], Bit[7] and Bit[0] as 2'b10

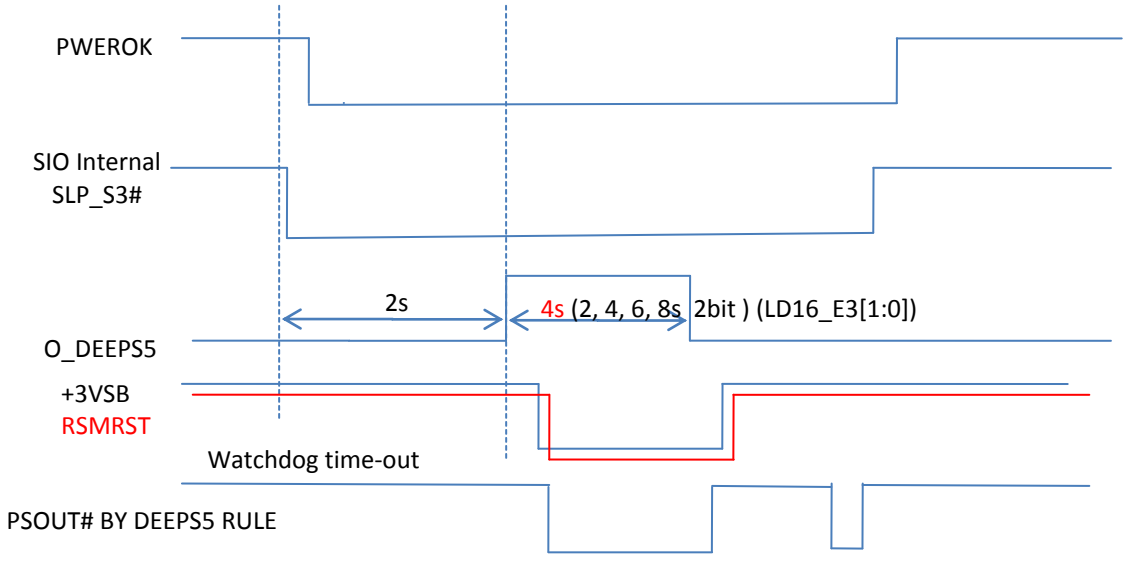


Figure 14-3 SLP_S3# Event When Logical Device D CR[F0h], Bit[7] and Bit[0] as 2'b11

15. GENERAL PURPOSE I/O

15.1 GPIO ARCHITECTURE

The NCT5569D provides three group input/output ports that can be configured to perform a simple basic I/O function or alternative, pre-defined function. The three groups can be select by logical device 9 CRF5 bit[2:0] and only one can be access at the same time. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 = output, 1 = input). Invert port value by setting inversion register (0 = non–inverse, 1 = inverse). Port value is read/write through data register.

In addition, only **GP23** is designed to be able to assert **PSOUT#** signal to wake up the system if it has falling transitions. Only falling, to perform the wake-up function. The following table gives more detailed register map on GP23.

Table 15-1 Relative Control Registers of GP23 that Support Wake-Up Function

	EVENTROUTE (PSOUT#) **0 : DISABLE** **1 : ENABLE**	**STATUS (PSOUT#)**	**MODE SELECT (PSOUT#)**
GP23	LDA, CR[FEh] bit5	LD15 CR[E1] bit5	LD15 CR[E2] bit0

Table 15-2 GPIO Group Programming Table

Equips maximum 8-pin GPIOs.

GPIO0 Group

Group Select: Logic Device 9 CRE5[2:0] = 3'b001
Enable: Logic Device 9, CR30[0]
Data: Logic Device 9, E0~E2
Multi-function: WDTO, SMI, BEEP, MLED, OVT, SLPS5_LCH (Logic Device9, CRE3[0~7])
Reset: Logic Device A, CRE9[2]
OD/PP: Logic Device 9, CRE4

Name	**Pin**	**Default function**	**Default type**	**GPIO power plane**	**Switch default function to GPIO**
GP00	13	GP00	Input	3VSB	
GP01	14	GP01	Input	3VSB	
GP02	15	GP02	Input	3VSB	
GP03	16	GP03	Input	3VSB	
GP04	17	GP04	Input	3VSB	
GP05	18	GP05	Input	3VSB	
GP06	19	GP06	Input	3VSB	
GP07	20	GP07	Input	3VSB	

GPIO1 Group

Group Select: Logic Device 9 CRE5[2:0] = 3'b010
Enable: Logic Device 9, CR30[1]
Data: Logic Device 9, E0~E2
Multi-function: WDTO, SMI, BEEP, MLED, OVT, SLPS5_LCH (Logic Device9, CRE3[0~7])
Reset: Logic Device A, CRE9[2]
OD/PP: Logic Device 9, CRE4

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP10	25	KDAT	Bi-direction	3VSB	CR2A[0]=1
GP11	24	KCLK	Bi-direction	3VSB	
GP12	23	MDAT	Bi-direction	3VSB	CR2A[1]=1
GP13	22	MCLK	Bi-direction	3VSB	
GP14	63	AUXFANIN0	Input	3VSB	CR1C[5]=1, Pad is VCC domain
GP16	35	RSTOUT1#	Output	3VSB	CR2B[6]=1
GP17	33	GP17	Input	3VSB	

GPIO2 Group

Group Select: Logic Device 9 CRE5[2:0] = 3'b100
Enable: Logic Device 9, CR30[2]
Data: Logic Device 9, E0~E2
Multi-function: WDTO, SMI, BEEP,MLED(Logic Device9, CRE3[0~5])
Reset: Logic Device A, CRE9[2]
OD/PP: Logic Device 9, CRE4

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP21	39	GP21	Input	3VSB	
GP22	34	RSTOUT2#	Output	3VSB	CR2B[7]=1
GP23	30	GP23	Input	3VSB	
GP25	11	GA20M	Output	3VSB	CR1B[6]=1
GP26	1	WDTO#	Output(OD)	3VSB	CR1B[3]=1

15.2 ACCESS CHANNELS

There are two different channels to set up/access the GPIO ports. The first one is the indirect access via register 2E/2F (4E/4F, it depends by HEFRAS trapping). The registers can be read / written only when the respective logical device ID and port number are selected.

The other is the direct access through GPIO register table that can be configured by {CR61, CR60} of logic device 8. The mapped 6 registers are defined in table 18-2. Base address plus 0 to 3 are GPIO registers, base address plus 5 and 6 are watchdog registers.Since the base address is set, and the I/O register, the Data register and the Inversion register are mapped to addresses Base+1, Base+2 and Base+3 respectively. Only one GPIO can be accessed at one time.

Table 15-3 GPIO Register Addresses

ADDRESS	ABBR	BIT NUMBER							
		7	6	5	4	3	2	1	0
Base + 1	IOR	GPIO I/O Register							
Base + 2	DAT	GPIO Data Register							
Base + 3	INV	GPIO Inversion Register							
Base + 5	Wdtmod	Watchdog Timer I (WDT1) and KBC P20 Control Mode Register							
Base + 6	Wdttim	Watchdog Timer I (WDT1) Control Register							

16. CONFIGURATION REGISTER

16.1 Chip (Global) Control Register

Default Value of Global Control Register:

Register	Default	Register	Default	Register	Default
CR 07h	00h	CR 20h	53h (ID_H)	CR 2Bh	00h
CR 10h	FFh	CR 21h	91h (ID_L)	CR 2Ch	01h
CR 11h	FFh	CR 22h	FFh	CR 2Fh	0ss0ssssb
CR 13h	00h	CR 24h	04h		
CR 14h	00h	CR 25h	00h		
CR 1Ah	30h	CR 26h	0s000000b		
CR 1Bh	70h	CR 27h	00h		
CR 1Ch	00h	CR 28h	00h		
CR 1Dh	00h	CR 2Ah	80h		

Note. The value of “s” means hardware strapping result: strapping high will report 1; strapping low will report 0.
In addition, BIOS can write the value of strapping result after hardware strapping.

Note. The CR21h is low-byte of the Chip-ID; the “X” means IC version. EX. 61=A version, 62=B version, 63=C version.

Reserved Registers of Global Control Register:

Register	Default	Register	Default
CR 02h	00h	CR 1Eh	FFh
CR 12h	FFh	CR 1Fh	FFh
CR 15h	FFh	CR 23h	00h
CR 16h	FFh	CR 29h	FFh
CR 17h	FFh	CR 2Dh	FFh
CR 18h	FFh	CR 2Eh	00h
CR 19h	FFh		

Note. All reserved registers must keep default value.

Note. Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 07h. Logical Device Selection

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Logical Device Number.

CR 10h. Device IRQ TYPE Selection

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	UARTA IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4	Reserved.	
3	R / W	KBC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
2	R / W	MOUSE IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
1-0	Reserved.	

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 11h. Device IRQ TYPE Selection
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	R / W	HM IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
6	R / W	WDTO IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5-2	Reserved.	
1	R / W	SMI IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	Reserved.	

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 13h. Device IRQ Polarity Selection
Attribute: Read/Write
Power Well: VCC

Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<15:8> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 14h. Device IRQ Polarity Selection
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<7:0> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 1Ah. Multi Function Selection
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 21h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-5</td><td colspan="2">Reserved</td></tr>
<tr><td>4-3</td><td>R / W</td><td>Pin33 GP17/MLED/GPIOE#/BKFD_CUT function select
<table>
<tr><td></td><td>GPIOE_SEL</td></tr>
<tr><td>GP17</td><td>00 (Default)</td></tr>
<tr><td>MLED</td><td>01</td></tr>
<tr><td>GPIOE#</td><td>10</td></tr>
<tr><td>BKFD_CUT</td><td>11</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin11 GATEA20 OD select Control
0: Push Pull (Default)
1: OD</td></tr>
<tr><td>1</td><td colspan="2">Reserved</td></tr>
<tr><td>0</td><td>R / W</td><td>Pin12 (KBRST#) output type selection
0: push pull
1: OD (Default)</td></tr>
</table>

CR 1Bh. Multi Function Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 70h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td colspan="2">Reserved</td></tr>
<tr><td>6</td><td>R / W</td><td>Pin11 GP25/GATEA20 function select
<table>
<tr><td>CR1B[Bit6]</td><td>Pin11</td></tr>
<tr><td>0</td><td>GATEA20 (Default)</td></tr>
<tr><td>1</td><td>GP25</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>R / W</td><td>Pin30 GP23/PME#/OVT#/SMI# function select
<table>
<tr><td></td><td>GP23_SEL</td></tr>
<tr><td>GP23</td><td>00 (Default)</td></tr>
<tr><td>PME#</td><td>01</td></tr>
<tr><td>OVT#</td><td>10</td></tr>
<tr><td>SMI#</td><td>11</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Pin1 Function Select
<table>
<tr><td></td><td>CR1B[3]</td></tr>
<tr><td>GP26</td><td>1</td></tr>
<tr><td>WDTO#</td><td>0(Default)</td></tr>
</table></td></tr>
<tr><td>2-0</td><td colspan="2">Reserved.</td></tr>
</table>

CR 1Ch. Multi Function Selection

Attribute: Read/Write
Power Well: VSB
Reset by: PWROK
Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-6</td><td colspan="2">Reserved.</td></tr>
<tr><td>5</td><td>R / W</td><td>Pin63 function selection
<table>
<tr><td>CR1C [Bit5]</td><td>Pin63</td></tr>
<tr><td>0</td><td>AUXFANIN0</td></tr>
<tr><td>1</td><td>GP14</td></tr>
</table></td></tr>
<tr><td>4-0</td><td colspan="2">Reserved.</td></tr>
</table>

CR 1Dh. Multi Function Selection

Attribute: Read/Write

Power Well: VSB
Reset by: PWROK(Bit7-5, 0), RSMRST#(Bit4-3), RSMRST#&5VUSB_DETECT(Bit2-0)
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIOE# is inactive. 1: GPIOE# is active.
6	R / W	Issue GPIOE# to RESETCONO#. 0: Disable 1: Enable
5	R / W	Issue GPIOE# to PWROK. 0: Disable 1: Enable
4	R / W	0: Disable ANTISURGE event route to KBRST# 1: Enable ANTISURGE event route to KBRST#
3-1	R / W	**Pin39** function selection CR1D [Bit3] / CR1D [Bit2-1] / Pin39: 0 / xx / GP21 1 / 00 / Tri-state 1 / 01 / 3VSBSW# 1 / 10 / PWROK 1 / 11 / Tri-state
0	R / W	**Pin18** Enable Port80 to SOUTA Function 0: Disable 1: Enable

CR 20h. Chip ID (High Byte)
Attribute: Read Only
Power Well: VCC
Reset by: None
Default : 51h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = D1h (high byte).

CR 21h. Chip ID (Low Byte)
Attribute: Read Only
Power Well: VCC
Reset by: None
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = 62h (low byte)

CR 22h. Device Power Down

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	UARTA Power Down. 0: Powered down. 1: Not powered down.
3-0	Reserved.	

CR 24h. Global Option

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	Select output type of AUXFANOUT0 =0 AUXFANOUT0 is Open-drain. =1 AUXFANOUT0 is Push-pull.
4	R / W	Select output type of SYSFANOUT =0 SYSFANOUT is Open-drain. =1 SYSFANOUT is Push-pull.
3	R / W	Select output type of CPUFANOUT =0 CPUFANOUT is Open-drain. =1 CPUFANOUT is Push-pull.
2-1	Reserved.	
0	R / W	PNPCVS => = 0 The compatible PNP address-select registers have default values. = 1 The compatible PNP address-select registers have no default values.

CR 25h. Interface Tri-state Enable

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved.	
2	R / W	UARTATRI
1-0	Reserved.	

CR 26h. Global Option s: value by strapping
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 0s000000b

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA#.
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4-2	Reserved.	
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
0	Reserved.	

CR 2Ah. Multi Function Selection
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#, RST_KM (bit1-0) (reference LDB CRE6[bit7])
Default : 80h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**Pin13** function selection

CR2A [Bit7]	Pin13
0	CTSA#
1	GP00

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>
Pin14 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin14</td></tr>
<tr><td>0</td><td>DSRA#</td></tr>
<tr><td>1</td><td>GP01</td></tr>
</table>
Pin15 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin15</td></tr>
<tr><td>0</td><td>RTSA#</td></tr>
<tr><td>1</td><td>GP02</td></tr>
</table>
Pin16 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin16</td></tr>
<tr><td>0</td><td>DTRA#</td></tr>
<tr><td>1</td><td>GP03</td></tr>
</table>
Pin17 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin17</td></tr>
<tr><td>0</td><td>SINA</td></tr>
<tr><td>1</td><td>GP04</td></tr>
</table>
Pin18 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>SOUTA_P80_EN</td><td>Pin18</td></tr>
<tr><td>0</td><td>0</td><td>SOUTA</td></tr>
<tr><td>1</td><td>0</td><td>GP05</td></tr>
<tr><td>x</td><td>1</td><td>SOUTA_P80</td></tr>
</table>
Pin19 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin19</td></tr>
<tr><td>0</td><td>DCDA#</td></tr>
<tr><td>1</td><td>GP06</td></tr>
</table>
Pin20 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin20</td></tr>
<tr><td>0</td><td>RIA#</td></tr>
<tr><td>1</td><td>GP07</td></tr>
</table>
</td></tr>
<tr><td>6-3</td><td colspan="2">Reserved.</td></tr>
<tr><td>2</td><td>R/W</td><td>Enable Over Temperature shutdown Protection (OVT#)
= 0 The thermal shutdown function is disabled. (Default)
= 1 Enable thermal shutdown function.
(If set this bit to 1, the relative registers of OVT# event are:
Bank0, Index18 ,Bit6 → SMIOVT1 OVT# (Default CPUTIN)
Bank0, Index4C ,Bit3 → SMIOVT2 OVT# (Default AUXTIN)
If current temperature exceeds high-limit setting, OVT# event will be triggered and PSON# will inactive immediately.)</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>R / W</td><td>Pin22 function selection
<table>
<tr><td>CR2A [Bit1]</td><td>Pin22</td></tr>
<tr><td>0</td><td>MCLK</td></tr>
<tr><td>1</td><td>GP13</td></tr>
</table>
Pin23 function selection
<table>
<tr><td>CR2A [Bi 1]</td><td>Pin23</td></tr>
<tr><td>0</td><td>MDAT</td></tr>
<tr><td>1</td><td>GP12</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin24 function selection
<table>
<tr><td>CR2A [Bit0]</td><td>Pin24</td></tr>
<tr><td>0</td><td>KCLK</td></tr>
<tr><td>1</td><td>GP11</td></tr>
</table>
Pin25 function selection
<table>
<tr><td>CR2A [Bit0]</td><td>Pin25</td></tr>
<tr><td>0</td><td>KDAT</td></tr>
<tr><td>1</td><td>GP10</td></tr>
</table></td></tr>
</table>

CR 2Bh. Multi Function Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin34 function selection
<table>
<tr><td>CR2B [Bit6]</td><td>Pin34</td></tr>
<tr><td>0</td><td>RSTOUT2#</td></tr>
<tr><td>1</td><td>GP22</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin35 function selection
<table>
<tr><td>CR2B [Bit5]</td><td>Pin35</td></tr>
<tr><td>0</td><td>RSTOUT1#</td></tr>
<tr><td>1</td><td>GP16</td></tr>
</table></td></tr>
<tr><td>4-0</td><td colspan="2">Reserved.</td></tr>
</table>

CR 2Ch. Multi Function Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td colspan="2">Reserved.</td></tr>
<tr><td>6-5</td><td>R / W</td><td>Pin32 3VSBSW#/LATCH_BKFD_CUT#/1.5V_DUAL_EN function selection
<table>
<tr><th>CR2C [Bit6-5]</th><th>1p5DUAL_EN</th><th>Pin32</th></tr>
<tr><td>00</td><td>0</td><td>3VSBSW#(OD)</td></tr>
<tr><td>1x</td><td>0</td><td>LATCH_BKFD_CUT#</td></tr>
<tr><td>01</td><td>0</td><td>3VSBSW#(PP)</td></tr>
<tr><td>xx</td><td>1</td><td>1.5V_DUAL_EN (OD)</td></tr>
</table></td></tr>
<tr><td>4-0</td><td colspan="2">Reserved</td></tr>
</table>

CR 2Fh. Strapping Function Result

Location: Address 2Fh

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#(Bit5-2), PWROK(Bit7, 0), LRESET#(Bit6, 1)

Default : by 0ss0_ssss

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	Enable RSMWDT# Function. RSMWDT# Strapping result.
5	R / W	Enable LNV Function. OTP Strapping result.
4	Reserved.	
3	R / W	Enable 1p5DUAL_EN Function, 1p5DUAL_EN Strapping result.
2-1	Reserved.	
0	R / W	PSIN4S_EN Strapping result reading

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

4) VSB Strapping result can be programming by LPC, and reset by RSMRST#
5) VCC Strapping result can be programming by LPC, and reset by PWROK
6) LRESET Strapping (2E_4E_SEL) : No change

16.2 Logical Device 2 (UART A)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, F8h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 1 I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 1.

CR F0h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.

BIT	READ / WRITE	DESCRIPTION
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART A clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART A clock source is 2 MHz (24 MHz / 12). 1 0: UART A clock source is 24 MHz (24 MHz / 1). 1 1: IR clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**UARTA_RS485_enable** 0: Disable RS485 auto flow control function for UARTA 1: Enable RS485 auto flow control function for UARTA
6	R / W	**UARTA_RS485_inv_sel** (Available only when CRF2_Bit7=1) 0: Do not invert the behavior of RTSA# pin for RS485 auto flow control. 1: Invert the behavior of RTSA# pin for RS485 auto flow control.
5-0	Reserved.	

16.3 Logical Device 5 (Keyboard Controller)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the first KBC I/O base address <100h: FFFh> on 1-byte boundary.

CR 62h, 63h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the second KBC I/O base address <100h: FFFh> on 1 byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h.

Attribute: Read/Write
Power Well: VCC

Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 83h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	KBC clock rate selection **Bits** **7 6** 0 0: Reserved 0 1: Reserved 1 0: 12MHz 1 1: Reserved
5-3	Reserved.	
2	R / W	0: Port 92 disabled. 1: Port 92 enabled.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST# software control. 1: KBRST# hardware speed up.

16.4 Logical Device 8 (WDT1, WDT3, GPIO)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	0: WDT3 is inactive. 1: WDT3 is active.
3	R / W	0: GPIO Base Address mode is inactive 1: GPIO Base Address mode is active
2-1	Reserved.	
0	R / W	0: WDT1 is inactive. 1: WDT1 is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select GPIO Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR F5h. Watchdog Timer I(WDT1) and KBC P20 Control Mode Register

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET# or PWROK(see LDA E7[3])
Default : 00hf

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W Write “1” Only	Disable / Enable RESETCONO# One Shooting bit. This bit is self-clearing. 0: Disable 1: Enable
4	R / W	Watchdog Timer I count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is 0, the count mode is 1/1000 seconds mode.) (If bit-3 is 1, the count mode is 1/1000 minutes mode.)

BIT	READ / WRITE	DESCRIPTION
3	R / W	Select Watchdog Timer I count mode. 0: Second Mode. 1: Minute Mode. The unit of time divide by 24MHz.
2	R / W	Enable the rising edge of a KBC reset (P20) to issue a time-out event. 0: Disable. 1: Enable.
1	R / W	Disable / Enable the Watchdog Timer I output low pulse to the KBRST# pin 0: Disable. 1: Enable.
0	R / W	Pulse or Level mode select 0: Pulse mode 1: Level mode

CR F6h. Watchdog Timer I(WDT1) Counter Register

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET# or PWROK(see LDA E7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Watch Dog Timer I Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watch Dog Counter and start counting down. The accuracy of watchgdog timer 1 about oen cycle tolerance. If CR F7h, bits 7 and 6 are set, any Mouse Interrupt or Keyboard Interrupt event causes the previously-loaded, non-zero value to be reloaded to the Watch Dog Counter and the count down resumes. Reading this register returns the current value in the Watch Dog Counter, not the Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after one cycle time, the cycle time is base on LD8 CRF5, bit[3], by analogy.

CR F7h. Watchdog Timer I(WDT1) Control & Status Register

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET# or PWROK(see LDA E7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mouse interrupt reset enables watch-dog timer reload 0: Watchdog Timer I is not affected by mouse interrupt. 1: Watchdog Timer I is reset by mouse interrupt.

BIT	READ / WRITE	DESCRIPTION
6	R / W	Keyboard interrupt reset enables watch-dog timer reload 0: Watchdog Timer I is not affected by keyboard interrupt. 1: Watchdog Timer I is reset by keyboard interrupt.
5	Write “1” Only	Trigger Watchdog Timer I event. This bit is self-clearing.
4	R / W Write “0” Clear	Watchdog Timer I status bit 0: Watchdog Timer I is running. 1: Watchdog Timer I issues time-out event.
3-0	R / W	These bits select the IRQ resource for the Watchdog Timer I

CR F8h. Watchdog Timer III(WDT3) Control Mode Register

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET# or PWROK(see LDA EE[2])
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	Watchdog Timer III count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is 0, the count mode is 1/1000 seconds mode.) (If bit-3 is 1, the count mode is 1/1000 minutes mode.)
3	R / W	Select Watchdog Timer III count mode. 0: Second Mode. 1: Minute Mode. The unit of time divide by 24MHz.
2-1	Reserved.	
0	R / W	Pulse or Level mode select 0: Pulse mode 1: Level mode

CR F9h. Watchdog Timer III(WDT3) Counter Register

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET# or PWROK(see LDA EE[1])
Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Watch Dog Timer III Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watch Dog Counter and start counting down. The accuracy of watchgdog timer 3 about oen cycle tolerance. Reading this register returns the current value in the Watch Dog Counter, not the Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after one cycle time, the cycle time is base on LD8 CRF8, bit[3], by analogy.

CR FAh. Watchdog Timer III(WDT3) Control & Status Register

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET# or PWROK(see LDA EE[1])
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W Write “1” Only	Trigger Watchdog Timer III event. This bit is self-clearing.
4	R / W Write “0” Clear	Watchdog Timer III status bit 0: Watchdog Timer III is running. 1: Watchdog Timer III issues time-out event.
3-0	R / W	These bits select the IRQ resource for Watchdog Timer III

CR FEh. Watchdog Timer I(WDT1) Timeout Counter Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W Write “1” Clear	Watchdog Timer I Timeout Counter.

CR FFh. Watchdog Timer III(WDT_MEM) Timeout Counter Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W Write “1” Clear	Watchdog Timer III Timeout Counter.

16.5 Logical Device 9 (GPIO)

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION	
7-3	Reserved		
2	R / W	0: GPIO2 is inactive.	1: GPIO2 is active
1	R / W	0: GPIO1 is inactive.	1: GPIO1 is active.
0	R / W	0: GPIO0 is inactive.	1: GPIO0 is active.

CR E0h. GPIO I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GPX_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO I/O register 0: The respective GPIO PIN is programmed as an output port 1: The respective GPIO PIN is programmed as an input port.

CR E1h. GPIO Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GPX_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR E2h. GPIO Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GPX_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E3h. GPIO Multi-function Select Register

Attribute: Read Only

Power Well: VSB

Reset by: GPX_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIOx7 1: GPIOx7 → WDTO (Please also set this GPIO to “output” type.)
6	R / W	0: GPIOx6 1: GPIOx6 → BEEP (Please also set this GPIO to “output” type.)
5	R / W	0: GPIOx5 1: GPIOx5 → SMI (Please also set this GPIO to “output” type.)
4	R / W	0: GPIOx4 1: GPIOx4 → WDTO (Please also set this GPIO to “output” type.)
3	R / W	0: GPIOx3 1: GPIOx3 → MLED (Please also set this GPIO to “output” type.)
2	R / W	0: GPIOx2 1: GPIOx2 → BEEP (Please also set this GPIO to “output” type.)
1	R / W	0: GPIOx1 1: GPIOx1 → OVT (Please also set this GPIO to “output” type.)
0	R / W	0: GPIOx0 1: GPIOx0 → WDTO (Please also set this GPIO to “output” type.)

Note: x indicated GPIO group which is select by CRE5 bit[2:0]

CR E4h. GPIO Push-Pull/Open-Drain Register

Attribute: Read/Write

Power Well: VSB

Reset by: GPX_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E5h. GPIO Group Select and De-bounce Register

Attribute: Read/Write

Power Well: VSB
Reset by: GPX_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2-0	R / W	GPIO Group Select register 3'b001 : GPIO Group 0 3'b010 : GPIO Group 1 3'b100 : GPIO Group 2

16.6 Logical Device A (ACPI)

CR E0h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 01h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>DIS_PSIN => Disable the panel switch input to turn on the system power supply.
0: PSIN is wire-AND and connected to PSOUT#.
1: PSIN is blocked and cannot affect PSOUT#.</td></tr>
<tr><td>6</td><td>R / W</td><td>Enable KBC wake-up
0: Disable keyboard wake-up function via PSOUT#.
1: Enable keyboard wake-up function via PSOUT#.</td></tr>
<tr><td>5</td><td>R / W</td><td>Enable Mouse wake-up
0: Disable mouse wake-up function via PSOUT#.
1: Enable mouse wake-up function via PSOUT#.</td></tr>
<tr><td>4</td><td>R / W</td><td>MSRKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the following table for the details.
<table>
<tr><th>ENMDAT_UP</th><th>MSRKEY</th><th>MSXKEY</th><th>Wake-up event</th></tr>
<tr><td>1</td><td>x</td><td>1</td><td>Any button clicked or any movement.</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>One click of left or right button.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One click of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>One click of the right button.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Two clicks of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two clicks of the right button.</td></tr>
</table></td></tr>
<tr><td>3</td><td colspan="2">Reserved.</td></tr>
<tr><td>2</td><td>R / W</td><td>Keyboard / Mouse swap enable
0: Normal mode.
1: Keyboard / Mouse ports are swapped.</td></tr>
<tr><td>1</td><td>R / W</td><td>MSXKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.</td></tr>
<tr><td>0</td><td>R / W</td><td>KBXKEY =>
0: Only the pre-determined key combination in sequence can wake up the system.
1: Any character received from the keyboard can wake up the system.</td></tr>
</table>

CR E1h. KBC Wake-Up Index Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up index register. This is the index register of CRE2, which is the access window for the keyboard's pre-determined key key-combination characters. The first set of wake-up keys is in of 0x00 – 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combinations can be read through 0x10 – 0x1E.

CR E2h. KBC Wake-Up Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up data register. This is the data register for the keyboard's pre-determined key-combination characters, which is indexed by CRE1.

CR E3h. Event Status Register

Attribute: Read Only
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	Read Only Read-Clear	This status flag indicates VSB power off/on.
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event issued. 1: Thermal shutdown event issued.
2	Read Only Read-Clear	PSIN_STS 0: No PSIN event issued. 1: PSIN event issued.
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event issued. 1: Mouse wake-up event issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event issued. 1: Keyboard wake-up event issued.

CR E4h.

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset, PWROK(Bit4), LRESET#(Bit3-2)
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-5	R / W	Power-loss control [Note] (These two bits will determine the system turn on or off after AC resume, from G3 to S5 state.) **Bits** **6 5** 0 0: Always turn off. 0 1: Always turn on. (PSON# will active when S3# is high.) 1 0: Pre-state. (System turns On or Off which depends on the state before the power loss.) 1 1: User defined mode for power loss last-state. (The last-state flag is located on "CRE6h, bit4.")
4	R / W	3VSBSW# enable bit 0: Disable. 1: Enable.
3	R / W	Keyboard wake-up options. 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2	R / W	Enable the hunting mode for wake-up events set in CRE0. This bit is cleared when any wake-up event is captured. (Note. This bit is use for KB and MS to generate PSOUT# while VCC valid, for example, wake-up from S1 to S0 via PSOUT#.) 0: Disable.(Default) 1: Enable.
1-0	Reserved.	

Note. Whether "Always turn on", "Pre-state" or "User defined mode", the PSON#'s active condition for system to turn-on is S3# goes high. For south-bridge which S3# default is low while AC resume, please refer "CRE7h, bit4" to achieve the power-loss control application.

CR E5h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 02h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved.	
2	R / W	RESETCONO# signal to control PWROK 0: Disable (Default) 1: Enable
1	R / W	Route to PWROK source selection. 0: PSON#. 1: SLP_S3#. (Default)

BIT	READ / WRITE	DESCRIPTION
0	R / W	ATXPGD Control 0: Enable ATXPGD 1: Disable ATXPGD

CR E6h.

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#(Bit7, Bit5, Bit3-1), Battery reset(Bit6, Bit4), PWROK(Bit0)

Default : 1Ah

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the table in CRE0, bit 4 for the details.
6	Read Only	SKTOCC Status. This bit is '1' when SKTOCC# = 1.
5	R / W	CASEOPEN0 Clear Control. Write 1 to this bit to clear CASEOPEN0 status. This bit will clear the status itself.
4	R / W	Power-loss Last State Flag. 0: ON 1: OFF. (Default)
3-1	R / W	PWROK_DEL Set the delay time when rising from 3VCC to PWROK **Bits** **3 2 1** 0 0 0: 50mS 0 0 1: 100mS 0 1 0: 150mS 0 1 1: 200mS 1 0 0: 250mS 1 0 1: 300mS (Default) 1 1 0: 500mS 1 1 1: 700mS
0	R / W	PWROK_TRIG => 0: PWROK work normally. (Default) 1: Write 1 will let internal PWROK keep low or from high to low immediately.

CR E7h.

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#(Bit3), Battery reset(Bit4, Bit0)

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	EN_ONPSOUT **(VBAT)** Disable/Enable to issue a 0.5s delay PSOUT# level when system returns from power loss state and is supposed to be on as described in CRE4[6:5], logic device A. (For southbridge which S3# default is low when AC resume, like VIA, AMD…etc.) 0: Disable. (Default) 1: Enable.
3	R / W	Select WDT1 reset source 0: Watchdog timer is reset by LRESET#. 1: Watchdog timer is reset by PWROK.
2-1	Reserved.	
0	R / W	Hardware Monitor RESET source select 0: PWROK. (Default) 1: LRESET#.

CR E9h. DDR4 and GPIOs Reset Source Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	DDR4SEL1 When S0 → S5 state, the delay timer of VDDQ_EN to VPP_EN. 0: 64ms 1: 32ms
6-5	R / W	DDR4SEL2 When S0 → S5 state, the delay timer of SLP_S5# to VDDQ_EN. 00: 0ms 01: 50ms 10: 100ms 11: 200ms
4-3	Reserved.	
2	R / W	GPX_MRST 0: GPX reset by RSMRST#. 1: GPX reset by SLPS5.
1-0	Reserved	

CR ECh. ACPI Control and Status Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R	PSIN real time Status
6-4	Reserved.	
3	R / W	Auto clear PSOUT# to disconnect to PSIN# function select 0: Disable. Clear by RSMRST 1: Enable. Clear by PSIN rising and RSMRST
2	Reserved.	
1	R / W	Enable to disconnect PSIN to PSOUT 0: Disable , PSOUT will bypass PSIN. 1: Enable.
0	Reserved.	

CR EDh.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	PSIN# blocking time register from S5 to S0. 1bit for 0.5sec.. Min: 0.5sec Max: 8sec
3	R / W	Hardware monitor reset source select. 0: VDD3VOK. 1: PWROK.
2-1	Reserved	
0	R / W	RSMRST reset source select. 0: VSB and PSOUT/PCHVSB 1: VSB and PSOUT/PCHVSB and Deep_S5_Ctrl

CR EEh.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	RESCON Reset source selection. 0: LRESET_L 1: PWROK
6	R / W	RIA Wakeup Enable 0: Disable GPIO event route to PSOUT#. 1: Enable GPIO event route to PSOUT#.
5-3	Reserved.	

BIT	READ / WRITE	DESCRIPTION
2	R / W	WDT3 reset source selection 0: Watchdog timer is reset by LRESET#. 1: Watchdog timer is reset by PWROK.
1	R / W	CASEOPEN polarity 0: None inverse CASEOPEN0/1 INPUT 1: Inverse CASEOPEN0/1 INPUT
0	R / W	CASEOPEN1 Clear Control. Write 1 to this bit to clear CASEOPEN1 status. This bit will clear the status itself.

CR F0h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 08h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-5</td><td>R / W</td><td>Pin31 function selection
<table>
<tr><th>LDA CRF0 [Bit7-5]</th><th>Pin31</th></tr>
<tr><td>000</td><td>Deep_S5_0</td></tr>
<tr><td>001</td><td>3VSBSW</td></tr>
<tr><td>010</td><td>LATCH_BKFD_CUT</td></tr>
<tr><td>011</td><td>Deep_S5_0</td></tr>
<tr><td>1xx</td><td>PWROK</td></tr>
</table></td></tr>
<tr><td>4-2</td><td colspan="2">Reserved</td></tr>
<tr><td>1</td><td>R / W</td><td>PSIN de-bounce
0: 62.4ms
1: 206ms</td></tr>
<tr><td>0</td><td>R / W</td><td>Keyboard Auto-swap Enable.
0: Disable
1: Enable</td></tr>
</table>

CR F2h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 58h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	

BIT	READ / WRITE	DESCRIPTION
5	R / W	Block SLP_S3# to PSON# 0: Disable 1: Enable
4	R / W	Enable RSTOUT2# function. 0: Disable RSTOUT2#. 1: Enable RSTOUT2#. (Default)
3	R / W	Enable RSTOUT1# function. 0: Disable RSTOUT1#. 1: Enable RSTOUT1#. (Default)
2-1	Reserved	
0	R / W	EN_PME 0 : Disable PME. (Default) 1 : Enable PME.

CR F3h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W-Clear	Status of the WDT4 event. Write 1 to clear this status.
5	R / W-Clear	PME status of the Mouse event. Write 1 to clear this status.
4	R / W-Clear	PME status of the KBC event. Write 1 to clear this status.
3-2	Reserved.	
1	R / W-Clear	PME status of the URA IRQ event. Write 1 to clear this status.
0	Reserved	

CR F4h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	

BIT	READ / WRITE	DESCRIPTION
3	R / W-Clear	PME status of the HM IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the WDT1 event. Write 1 to clear this status.
1	R / W-Clear	PME status of the RIA event. Write 1 to clear this status.
0	Reserved	

CR F6h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#(Bit7), RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable KB, MS interrupt of the KBC password event. 1: Enable KB, MS interrupt of the KBC password event.
6	Reserved.	
5	R / W	0: Disable PME interrupt of the Mouse event. 1: Enable PME interrupt of the Mouse event.
4	R / W	0: Disable PME interrupt of the KBC event. 1: Enable PME interrupt of the KBC event.
3-2	Reserved.	
1	R / W	0: Disable PME interrupt of the URA IRQ event. 1: Enable PME interrupt of the URA IRQ event.
0	Reserved	

CR F7h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : C0h

BIT	READ / WRITE	DESCRIPTION
7	R / W	RSTOUT2# Push-Pull/OD select 0: Open Drain 1: Push-Pull (Default)
6	R / W	RSTOUT1# Push-Pull/OD select 0: Open Drain 1: Push-Pull (Default)

BIT	READ / WRITE	DESCRIPTION
5	R / W	PSIN_BLK_EN. When S5->S0 or S0->S5, SIO will filter PSIN# a specific time. 0: Disable 1: Enable
4	Reserved	
3	R / W	0: Disable PME interrupt of the HM IRQ event. 1: Enable PME interrupt of the HM IRQ event.
2	R / W	0: Disable PME interrupt of the WDT1 event. 1: Enable PME interrupt of the WDT1 event.
1	R / W	0: Disable PME interrupt of the RIA event. 1: Enable PME interrupt of the RIA event.
0	Reserved	

CR FCh.

Attribute: Read/Write

Power Well: VSB

Reset by: Bit[7] reset by RSMRST ; Bit[4:0]: Rset by Battery reset

Default : 88h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4-3	R / W	1.5V_DUAL_EN_MD. Timer to control SLP_S5# to 1.5V_DUAL_EN. When SLP_S5# go low, 1.5V_DUAL_EN will go high with a timer. 00: 0ms 01: 50ms (default) 10: 100ms 11: 200ms
2-0	R / W	RSMRST# V1/V2 adjust register 000: normal V1/V2 001: -3% ~ -6% of normal 011: -6% ~ -9% of normal 111: -9% ~ -12% of normal

CR FEh.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	ATX5VSB_EN Reset source select (For Test) 0: VPS (Default) 1: RSMRST

BIT	READ / WRITE	DESCRIPTION
6	Reserved	
5	R / W	GPIO Wakeup Enable 0: Disable GPIO event route to PSOUT#. 1: Enable GPIO event route to PSOUT#.
4-1	Reserved	
0	R / W	Enable ATX5VSB to effect RSMRST 0: Disable .(Default) 1: Enable.

16.7 Logical Device B (Hardware Monitor, Front Panel LED)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: Hardware Monitor device is inactive. 1: Hardware Monitor device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the HM base address <100h : FFEh> along a two-byte boundary.

CR 64h, 65h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the I/O base address <100h : FFEh> along a two-byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select the IRQ resource for HM.

CR E0h. SYSFAN Duty Cycle Register

Attribute: Read/Write
Power Well: VSB

Reset by: RSMRST#
Default : 7Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	SYSFAN Duty Cycle Register

CR E1h. CPUFAN Duty Cycle Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 7Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	CPUFAN Duty Cycle Register

CR E2h. AUXFAN0 Duty Cycle Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN0 Duty Cycle Register

CR E5h. ANTISURGE Voltage Channel Confiugration Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : A8h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	AVCC high / low limit voltage setting 00: UV -10%, OV +9.8% 01: UV -15%, OV +14.8% 10: UV -19.9%, OV +19.8% 11: UV -24.9%, OV + 24.1%
5-4	R / W	VIN1 high / low limit voltage setting 00: UV -9.9%, OV +9.6% 01: UV -15%, OV +14.7% 10: UV -20.1%, OV +19.8% 11: UV -25.2%, OV + 24.9%
3-2	R / W	VIN0 high / low limit voltage setting 00: UV -9.9%, OV +9.6% 01: UV -15%, OV +14.7% 10: UV -20.1%, OV +19.8% 11: UV -25.2%, OV + 24.9%

BIT	READ / WRITE	DESCRIPTION
1-0	Reserved.	

CR E6h. Configuration Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#(Bit7), WDT&PWROK(Bit6)
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	CR2A Bit1-0 reset source selection 0: WDT & PWROK 1: RSMRST#
6	R / W	RESETCONI# and PSIN# input block 0: Enable 1: Disable
5-1	Reserved.	
0	R / W	Block OVP/UVP detect signal by VCC & S3#. 0: SLP_S3 and VCC effect UVP function. (Default) 1: VCC effect UVP function.

CR F0h. FANIN De-bouncer Register

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#, RSMRST# (only bit[0])
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	1: Enable AUXFANIN1 input de-bouncer. 0: Disable AUXFANIN1 input de-bouncer.
3	R / W	1: Enable AUXFANIN0 input de-bouncer. 0: Disable AUXFANIN0 input de-bouncer.
2	R / W	1: Enable CPUFANIN input de-bouncer. 0: Disable CPUFANIN input de-bouncer.
1	R / W	1: Enable SYSFANIN input de-bouncer. 0: Disable SYSFANIN input de-bouncer.
0	R / W	1: Enable debug port. 0: Disable debug port.

CR F1h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	SMI IRQ Enable.
6-2	Reserved.	
1-0	R / W	AUXFANOUT1 output selection 00: CPUFANOUT. (default) 01: SYSFANOUT. 10: AUXFANOUT0. 11: CPUFANOUT.

CR F5h. MLED Freqency select Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	MLED Frequency 0000: always high 0001: always low 0010: 4 Hz 0011: 2 Hz 0100: 1 Hz 0101: 1/2 Hz 0110: 1/4 Hz 0111: 1/8 Hz 1000: 1/16Hz 1001: Fading Led
3-0	Reserved.	

CR FAh.RESETCONO# and PWROK active Pulse width selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	ATXPGD Debounce Control (For Test) 0: Enable Debounce(Default) 1: Disable Debounce
6	R / W	Enable PIN51 5V_dect_VSB OV output delay 100ms 0: Disable (Default) 1: Enable

BIT	READ / WRITE	DESCRIPTION
5	R / W	Enable PIN51 5V_dect_VSB UV. 0: Disable (Default) 1: Enable
4	R / W	Enable PIN51 5V_dect_VSB OV. 0: Disable (Default) 1: Enable
3-2	R / W	RESETCONO# and PWROK active Pulse width selection 00:50ms ~ 60ms 01:100ms ~ 130ms 10:200ms ~ 260ms 11:200ms ~ 260ms
1-0	Reserved.	

16.8 Logical Device D (WDT2)

CR E0h. KBC Short Detection Register

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	KBC Short Detection Enable. 0: Disable KBC Short Detection. 1: Enable KBC Short Detection.

CR E7h. Watchgod Timer II(WDT2) Control Register

Location: Address E7h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3~2	R / W	Clock select of 5 second Watchdog Timer II **Bits** **3 2** **=** 0 0, clock rate 4Hz = 0 1, clock rate 1Hz = 1 0, cloak rate 1/2Hz = 1 1, clock rate 1MHz
1~0	R / W	Clock select of 100ms Watchdog Timer II **Bits** **1 0** = 0 0, clock rate 512Hz, WDT will generate 100mS low pulse after 5S = 0 1, clock rate 256Hz, WDT will generate 200mS low pulse after 5S = 1 0, clock rate 1KHz, WDT will generate 50mS low pulse after 5S = 1 1, clock rate 1MHz, WDT will generate 50uS low pulse after 5S

CR E8h. Watchdog Timer II 100ms Counter Register

Location: Address E8h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST# & TIMEOUT_EVENT(Internal)
Default : 32h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Setting of 100ms watch dog time out counter. Default is 8'h32. **Note. If CRE7[1:0] is 2'b00, then Watchdog Timer II 100ms counter will be 1.95ms(512Hz) * 50(8'h32) = 100m sec**

CR EBh. Watchdog Timer II 5s Counter Register

Location: Address EBh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 14h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Setting of 5 second watch dog time out counter. Default is 8'h14. The accuracy of watchgdog timer 2 about oen cycle tolerance. **Note. If CRE7[3:2] is 2'b00, then Watchdog Timer II counter will be 0.25s(4Hz) * 20(8'h14) = 5 sec**

CR EDh. Watchdog Timer II Software Reset Register

Location: Address EDh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
5	R / W	EN_5V_test 0: From Analog macro 1: From LDD_CRED[3] or LDD_CRED[4]
4	R / W	V5DET_UV_test
3	R / W	V5DET_OV_test
2-1	Reserved.	
0	R / W	This bit is used to start Watchdog Timer II counter 0: Disable 1: Start the counter. When the time is up, it will clear itself to 0.

CR F0h. Watchdog Timer Mask Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mask Watchdog Timer I to affect PWROK 0: Mask enable. (WDT1 not affect PWROK) 1: Mask disable. (WDT1 default affect PWROK)
6	R / W	Mask Watchdog Timer I to affect RESETCONO# 0: Mask enable. (WDT1 not affect RESETCONO#) 1: Mask disable. (WDT1 default affect RESETCONO#)
5	Reserved.	
4	R / W	Mask Watchdog Timer III to affect PWROK 0: Mask enable. (WDT_MEM not affect PWROK) 1: Mask disable. (WDT_MEM default affect PWROK)
3	R / W	Mask Watchdog Timer III to affect RESETCONO# 0: Mask enable. (WDT_MEM not affect RESETCONO#) 1: Mask disable. (WDT_MEM default affect RESETCONO#)
2-1	Reserved.	
0	R / W	Mask Watchdog Timer I to affect RSMRST# 0: Mask enable. (WDT1 not affect RSMRST #) 1: Mask disable. (WDT1 default affect RSMRST#)

CR F3h. Watchdog Timer II Status Register

Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	Watchdog Timer II status. When this bit is set to 1, it means timeout event occurs.
6~3	Reversed	
2	R Write “1” Clear	KBC Auto Swap Keyboard BAT Timeout Status
1		
0	R	KBC Auto-Swap Status. 0: Keyboard 1: MOUSE

CR F4h. KBC Auto Swap BAT Timeout Register

Location: Address F4h
Attribute: Read/Write
Power Well: VSB

Reset by: RSMRST#
Default : 40h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	When Keyboard complete BAT test, 0xAA indicate the BAT successful; When Mouse complete BAT test, folloeing the BAT completion code (0xAA), the mouse sends its device ID. These register is the time interval between BAT completion code and mouse device ID. Defualt interval time is 2ms (0.03125us*64)

16.9 Logical Device 14 (PORT80 UART)

CR E0h. PORT80 UART Control Register

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 80h

BIT	READ / WRITE	DESCRIPTION
7	R / W	TxEN (Transmit enable)
6-5	Reserved	
4	R / W	PARE (Parity enable)
3	R / W	PARS (Parity Selection) 0: odd parity 1: even parity
2	R / W	STPS (Stop bit length selection) 0: 1 stop bit 1: 2 stop bits
1	R / W	CHAS (Character length selection) 0: 8 bits 1: 7bits
0	Reserved	

CR E1h. PORT80 UART Status Register

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R	TD (Transmit done status) When UART finish transmit, it would be 1 and auto clear by hardware
0	R	TBF (Transmit buffer full flag) 0: UART is idle 1: UART is transmitting

CR E2h. PORT80 UART Baud Rate Generator High Byte

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator high byte)

CR E3h. PORT80 UART Baud Rate Generator Low Byte

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator low byte) Baud Rate = 2MHz / ({BRGH, BRGL} + 1)

CR E4h. PORT80 UART Transmit Buffer

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	UARTBUF (UART Transmit buffer)

16.10 Logical Device 15

CR E1h. GPIO, RI PSOUT Wake-Up Status Register

Attribute: Read/Write
Power Well: VRTC
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W-Clear	PSOUT status of the GP23 event. Write 1 to clear this status.
4	Reserved	
3	R / W-Clear	PSOUT status of the RIA event. Write 1 to clear this status.
2-0	Reserved.	

CR E2h. GPIO, RI PSOUT Wake-Up Control Register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R / W	GPIO and RI PSOUT Wake-Up Group Select. 0: GPIO 1: GPIO+RI
0	R / W	GPIO and RI PSOUT Wake-Up Mode Select 0: Sleep 1: Sleep+Deep

CR F8h. PLL Control Register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 60h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	EN_PLL 0: Disable Oscillator free 1: Enable Oscillator free
4-0	Reserved	

16.11 Logical Device 16 (Deep Sleep)

CR 30h. Deep Sleep configuration register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 20h

BIT	READ / WRITE	DESCRIPTION
7-2	R / W	Reserved.
1	R / W	Deep S3 Enable 0: If SLP_S3# state will not enter Deep S3 state. 1: If SLP_S3# state will enter Deep S3 state.
0	R / W	Deep S5 Enable 0: Disable Deep S5 function when into S5 state (SLP_S5#). 1: Enable Deep S5 function when into S5 state (SLP_S5#).

CR E0h. Deep Sleep wake up PSOUT# delay time

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : **20h** (Default: 512ms)

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5-0	R / W	Deep Sleep wake up PSOUT# delay time. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT# after SYS_3VSB and wait a delay time. DELAY TIME = (Setting Value) * 16ms Example : maximum delay time = $(3F)_{hex}$ * 16ms = 1008ms

CR E1h. Deep Sleep wake up PSOUT# pulse width

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : **04h** (Default: 128 ms)

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	Deep Sleep wake up PSOUT# pulse width. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT#.. Pulse Width = (Setting Value) * **32ms** Example : maximum pulse width = $(F)_{hex}$ * **32ms** = 480ms

CR E2h. Deep Sleep Delay Time Control

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 05h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: The unit of deep sleep delay time is second. 1: The unit of deep sleep delay time is Minute.
6-0	R / W	Deep Sleep Delay Time Control. When system leaves S0 State, IO will wait a delay time before entering into Deep Sleep State. Example: maximum delay time = 127 second/minute

CR FAh. Calibrated Clock control register

Location: Address FAh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 80h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	LCLK_FRQ[7:0] LCLK / (31.25KHz * 2) = LCLK_FRQ Example: 33MHz / (31.25KHz *2) = 11'h210 = 11'd528 24MHz / (31.25KHz *2) = 11'h180 = 11'd384

CR FBh. Calibrated Clock control register

Location: Address FBh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4	R / W	EN_CALI 0: Disable Oscillator free calibrate 1: Enable Oscillator free calibrate
3	Reserved	

BIT	READ / WRITE	DESCRIPTION
2-0	R / W	LCLK_FRQ[10:8] LCLK / (31.25KHz * 2) = LCLK_FRQ Example: 33MHz / (31.25KHz *2) = 11'h210 = 11'd528 24MHz / (31.25KHz *2) = 11'h180 = 11'd384

17. SPECIFICATIONS

17.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	-0.3 to 3.6	V
VI	Input Voltage	-0.3 to 3VCC+0.3	V
	Input Voltage (5V tolerance)	-0.3 to 5.5	V
TA	Operating Temperature	0 to +70	°C
TSTG	Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

17.2 DC CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V)

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Battery Quiescent Current	IBAT			2.4	μA	VBAT = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	IVSB			8.0	mA	VSB = 3.3 V, All ACPI pins are not connected.
VCC Quiescent Current	IVCC			25	mA	VSB = 3.3 V VCC (AVCC)= 3.3 V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
Vtt Quiescent Current	IVTT			1	mA	VSB = 3.3 V VCC (AVCC)= 3.3 V VTT = 1.0V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
AIN – Analog input						
AOUT – Analog output						

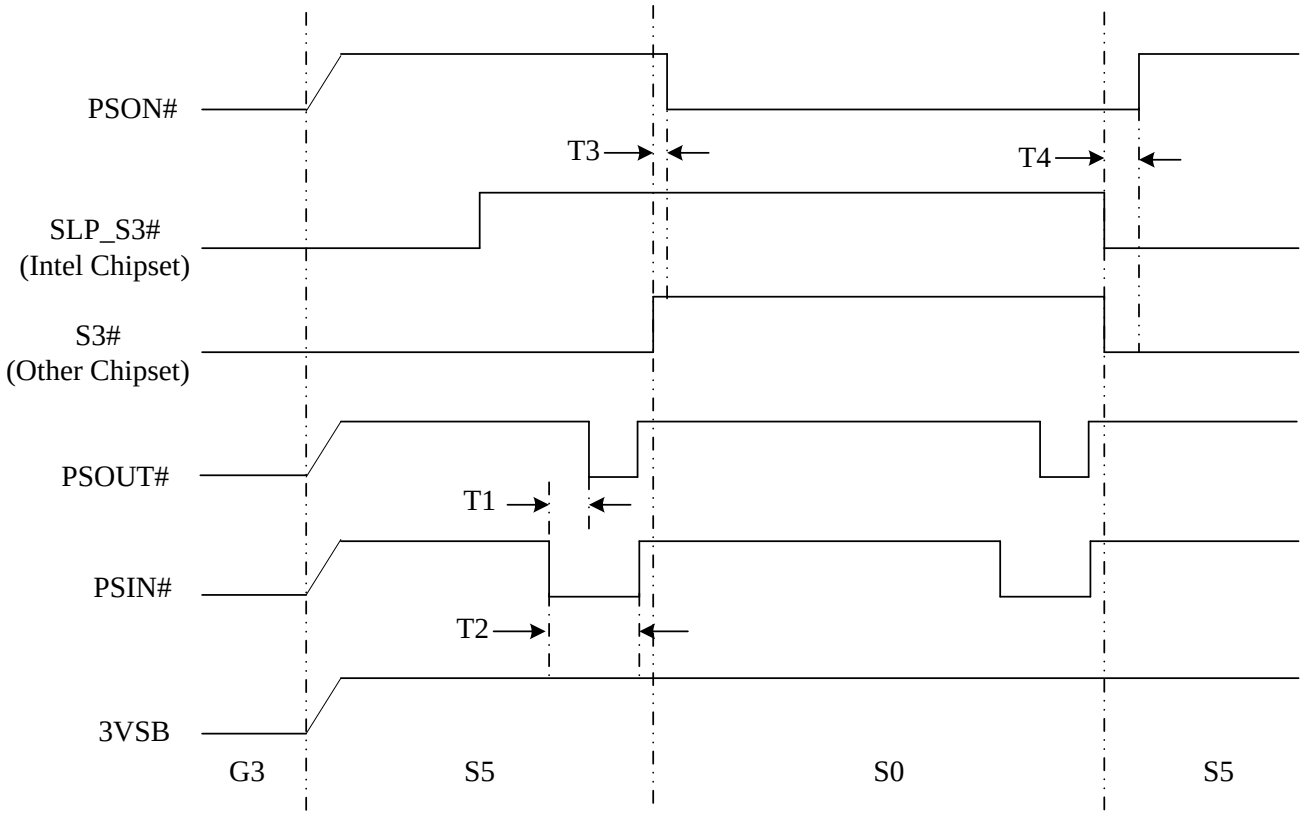
PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
IN_{tp3} – 3.3V TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tsp3} – 3.3V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{gp5} – 5V GTL-level input pin						
Input Low Voltage	V_{IL}		0.72		V	
Input High Voltage	V_{IH}		0.72		V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tp5} – 5V TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tscup5} – 5V TTL-level, Schmitt-trigger input buffer with controllable pull-up						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tsp5} – 5V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tdp5} – 5V TTL-level input pin with internal pull-down resistor						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
O_8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
OD_8 – Open-drain output pin with 8mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
O_{12} – Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_{12} – Open-drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
O_{24} – Output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
OD_{24} – Open-drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
O_{48} – Output pin with 48mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -48 mA
OD_{48} – Open-drain output pin with 48mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
I/O_{V3} – Bi-direction pin with source capability of 6 mA for INTEL® PECI						
Input Low Voltage	V_{IL}	0.275*V_{tt}		0.5*V_{tt}	V	
Input High Voltage	V_{IH}	0.55*V_{tt}		0.725*V_{tt}	V	
Output Low Voltage	V_{OL}			0.25*V_{tt}	V	
Output High Voltage	V_{OH}	0.75*V_{tt}			V	
Hysterisis	V_{Hys}	0.1*V_{tt}			V	
Sink	I_{Sink}	0.5mA		1mA		
O_{12cu} – Output pin 12mA source-sink capability with controllable pull-up						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
OD12cu – Open-drain 12mA sink capability output pin with controllable pull-up						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA

18. AC CHARACTERISTICS

18.1 Power On / Off Timing

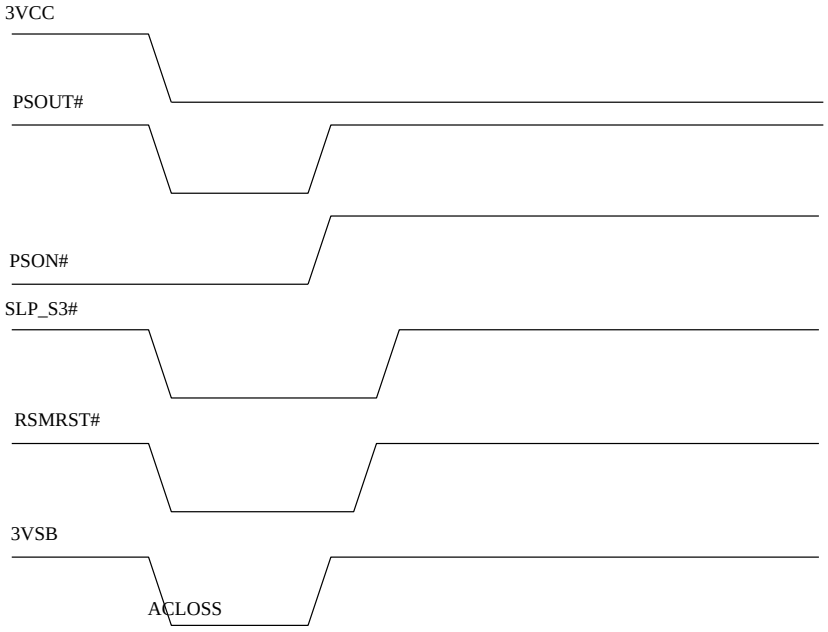


	T1	T2	T3	T4
IDEAL TIMING	48ms~66ms	Over 64ms at least	< 10ns	15ms~32ms

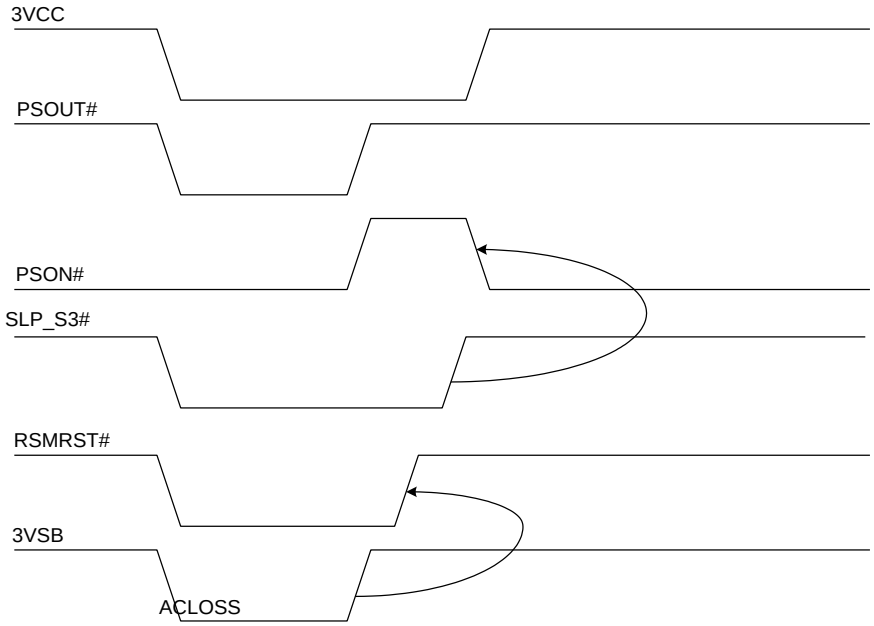
18.2 AC Power Failure Resume Timing

(1) Logical Device A, CR [E4h] bits [6:5] =00 means “OFF” state

(“OFF” means the system is always turned off after the AC power loss recovered.)



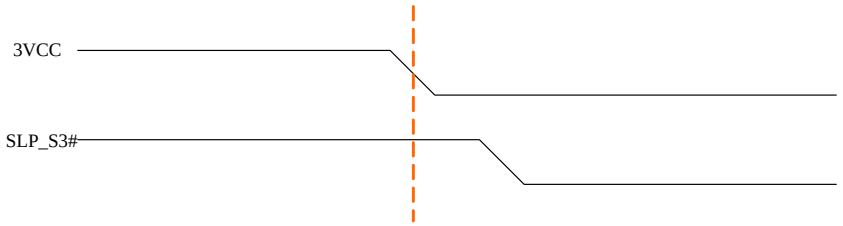
(2) Logical Device A, CR [E4h] bits [6:5]=01 means “ON” state.
(“ON” means the system is always turned on after AC power loss recovered.)



**** What's the definition of former state at AC power failure?**

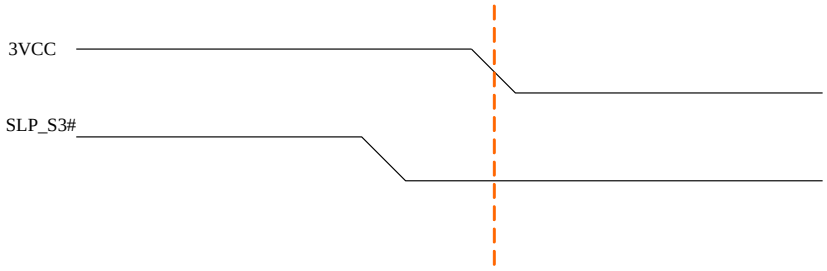
1) The previous state is "ON"

VCC falls to 2.6V and SLP_S3# keeps at VIH 2.0V



2) The previous state is "OFF"

VCC fall to 2.6V and SLP_S3# keeps at VIL 0.8V



To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT5569D adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state for the system to be "On" or "Off". According to this setting, the system chooses the state after the AC power recovery.

Please refer to the descriptions of bit 6~5 of CR E4h and bit 4 of CR E6h in Logical Device A.

CR E4h

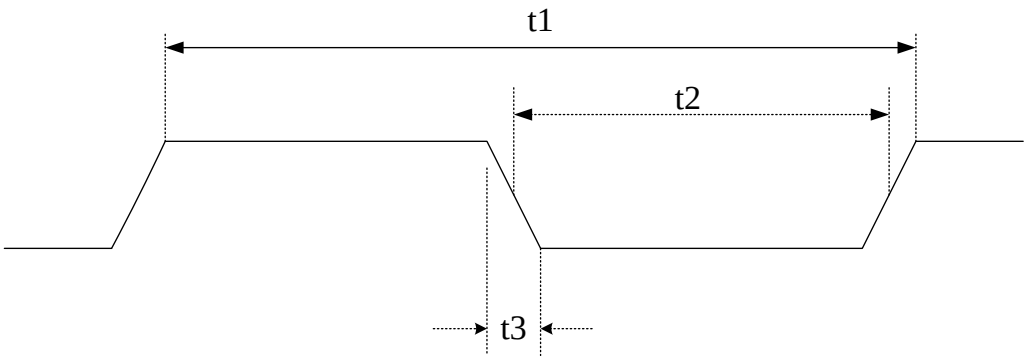
BIT	READ/WRITE	DESCRIPTION
6~5	R / W	Power-loss control bits => (VBAT) 0 0: System always turns off when it returns from power-loss state. 0 1: System always turns on when it returns from power-loss state. 1 0: System turns off / on when it returns from power-loss state depending on the state before the power loss. 1 1: User defines the resuming state before power loss.(refer to Logic Device A, CRE6[4])

CR E6h

BIT	READ/WRITE	DESCRIPTION
4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF

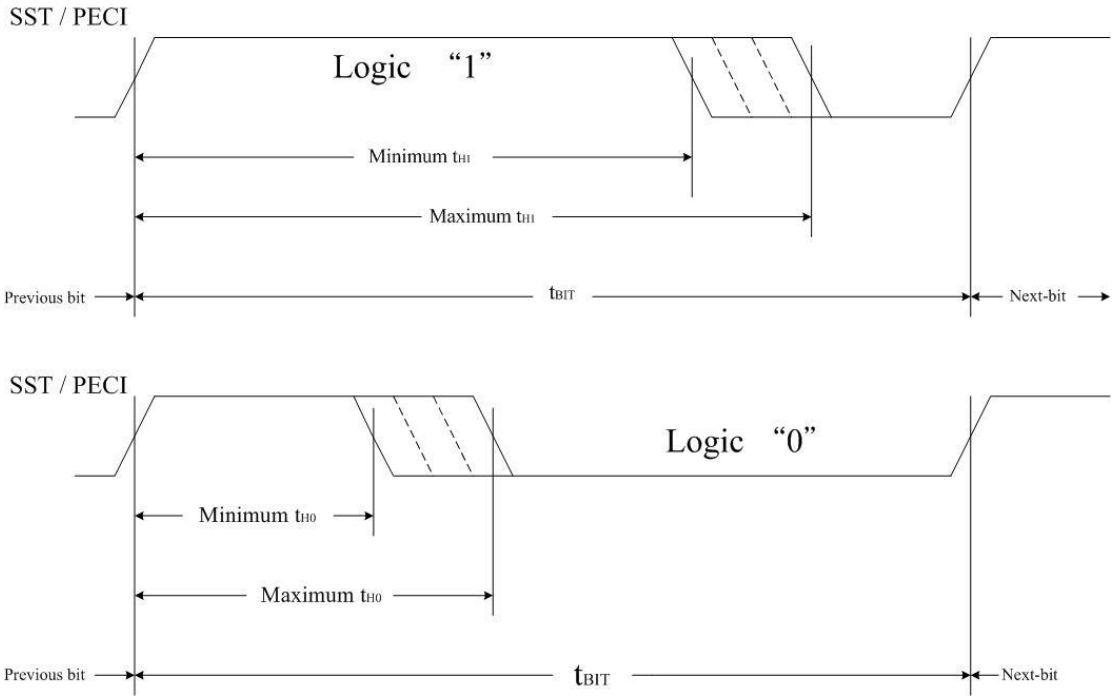
18.3 Clock Input Timing

PARAMETER	PCICLK		UNIT
	MIN	MAX	
Cycle to cycle jitter		300/500	ps
Duty cycle	45	55	%



PARAMETER	DESCRIPTION	PCICLK			UNIT
		MIN	TYP	MAX	
t1	Clock cycle time		30		ns
t2	Clock high time/low time	11	12		ns
t3	Clock rising time/falling time (0.4V~2.4V)	1		4	ns

18.4 PECI Timing

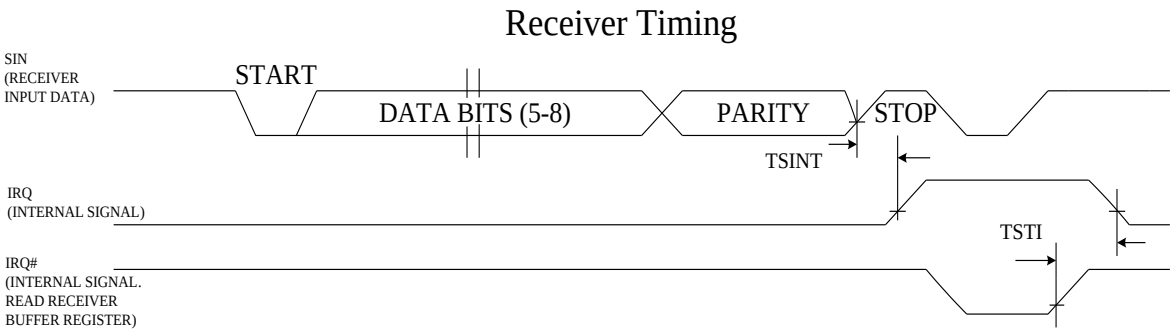


SYMBOL		MIN	TYP	MAX	UNITS
t_{BIT}	Client	0.495		500	μs
	Originator	0.495		250	
t_{H1}		0.6	3/4	0.8	× t_{BIT}
t_{H0}		0.2	1/4	0.4	× t_{BIT}

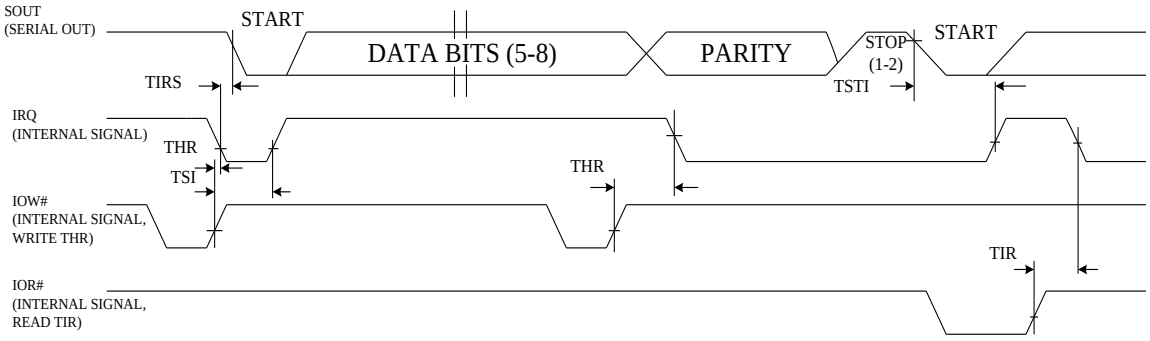
18.5 UART Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	TRINT		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR			175	nS
Delay from Initial $\overline{IOW}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			8/16	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	TIR		8	250	nS
Delay from $\overline{IOR}$ to Output	TMWO		6	200	nS
Set Interrupt Delay from Modem Input	TSIM		18	250	nS
Reset Interrupt Delay from $\overline{IOR}$	TRIM		9	250	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

UART Receiver Timing

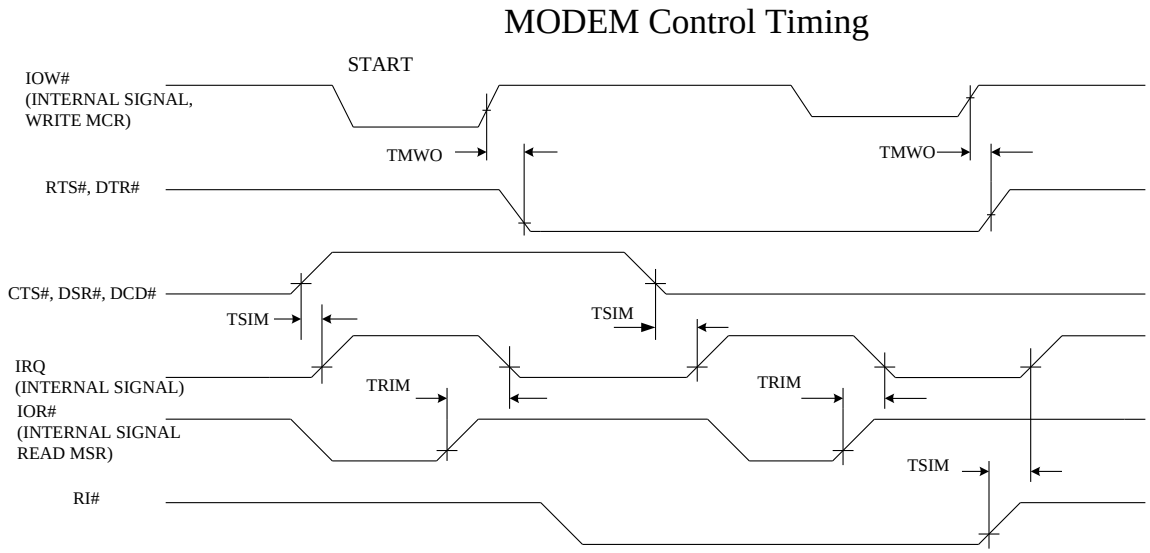


UART Transmitter Timing



18.6 Modem Control Timing

Modem Control Timing



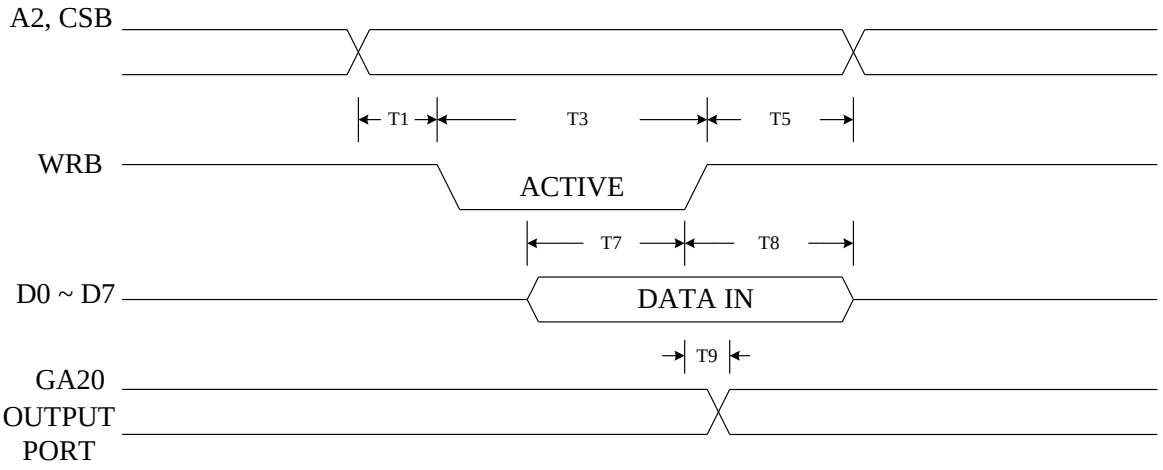
18.7 KBC Timing Parameters

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	µS
T13	K/B Clock Period	20		µS
T14	K/B Clock Pulse Width	10		µS
T15	Data Valid Before Clock Falling (RECEIVE)	4		µS
T16	K/B ACK After Finish Receiving	20		µS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		µS
T21	Input Clock Period (6–16 Mhz)	63	167	nS
T22	Duration of CLK inactive	30	50	µS
T23	Duration of CLK active	30	50	µS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	µS
T25	Time of inhibit mode	100	300	µS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	µS
T27	Duration of CLK inactive	30	50	µS
T28	Duration of CLK active	30	50	µS
T29	Time from DATA transition to falling edge of CLK	5	25	µS

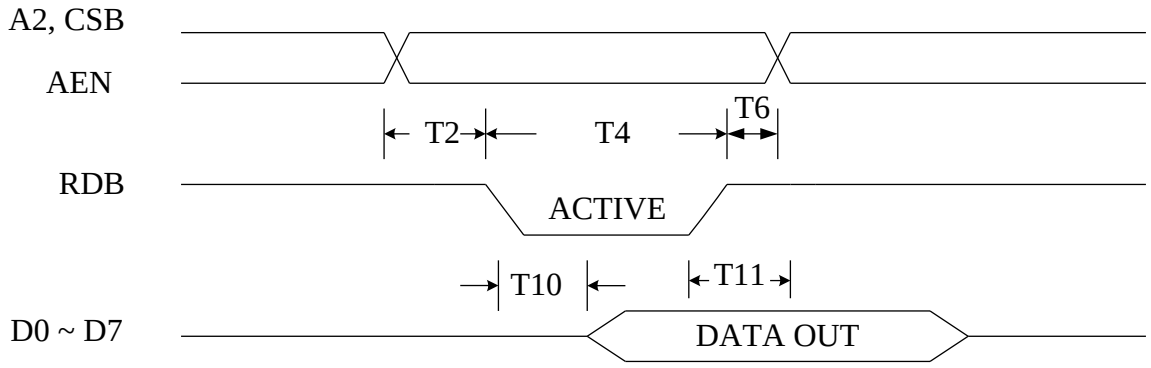
18.7.1 Writing Cycle Timing

Write Cycle Timing


A2, CSB
T1
T3
T5
WRB
ACTIVE
T7
T8
D0 ~ D7
DATA IN
T9
GA20
OUTPUT
PORT

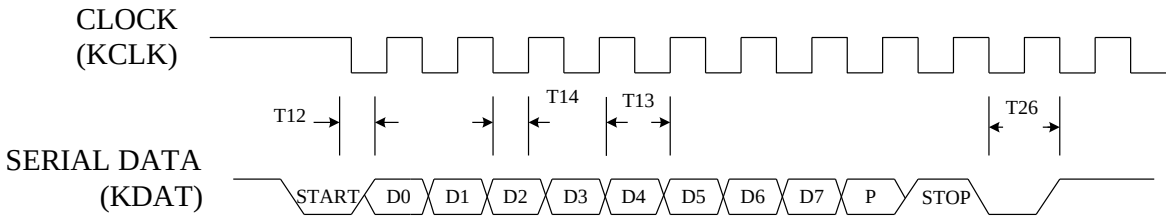
18.7.2 Read Cycle Timing

Read Cycle



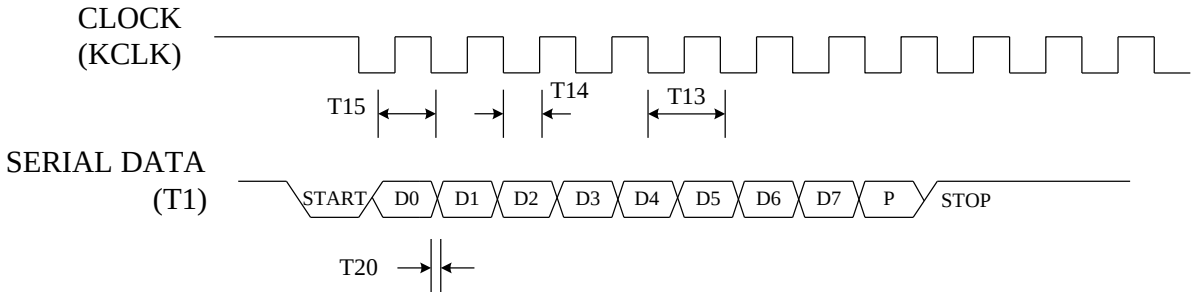
18.7.3 Send Data to K/B

Send Data to K/B



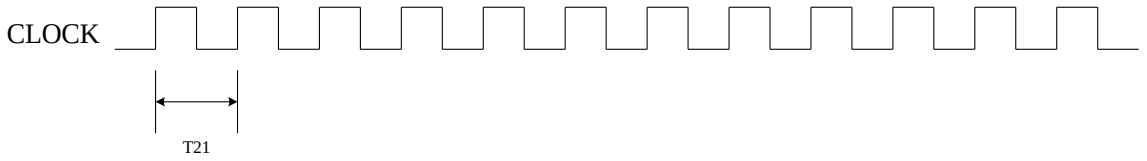
18.7.4 Receive Data from K/B

Receive Data from K/B



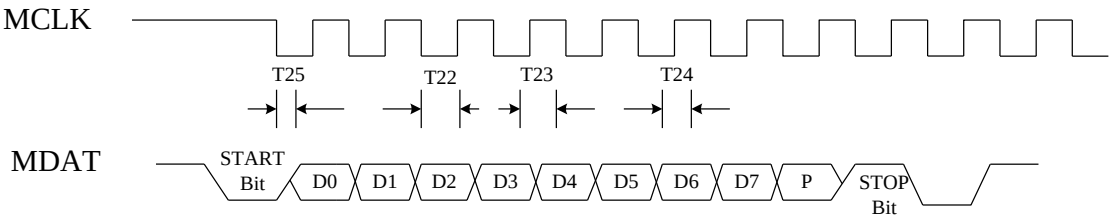
18.7.5 Input Clock

Input Clock



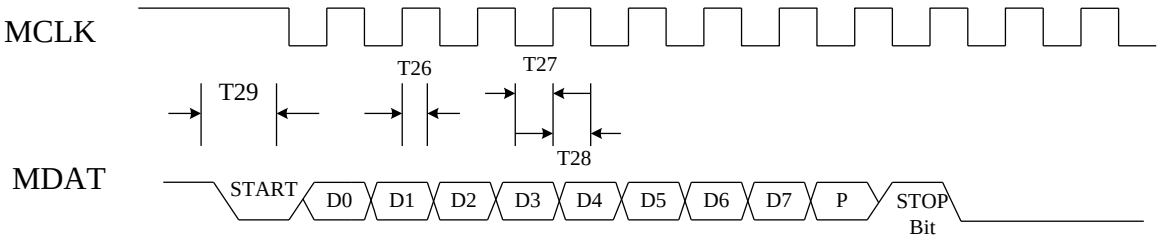
18.7.6 Send Data to Mouse

Send Data to Mouse



18.7.7 Receive Data from Mouse

Receive Data from Mouse



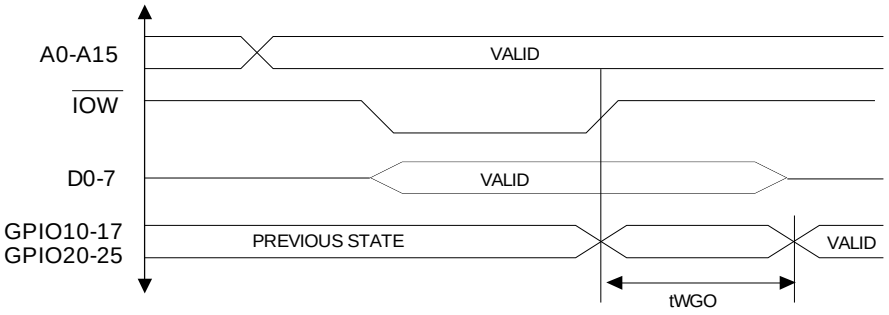
18.8 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300(Note 1)	ns

Note: Refer to Microprocessor Interface Timing for Read Timing.

18.8.1 GPIO Write Timing

GPIO Write Timing diagram



19. DEBUG PORT

NCT5569D provided debug port to output 80 port data. First, it need set debug port active. Second we input the serial keys (2^16 bits) and select command (2 bits) to DB_SI, then restart thh computer. It will output 80 port data on SOUTA_P80 (pin: SOUTA) or SOUTB_P80 (pin: SOUTC). It depends on select command.

Refer to logical device 14 to set the uart_tx.

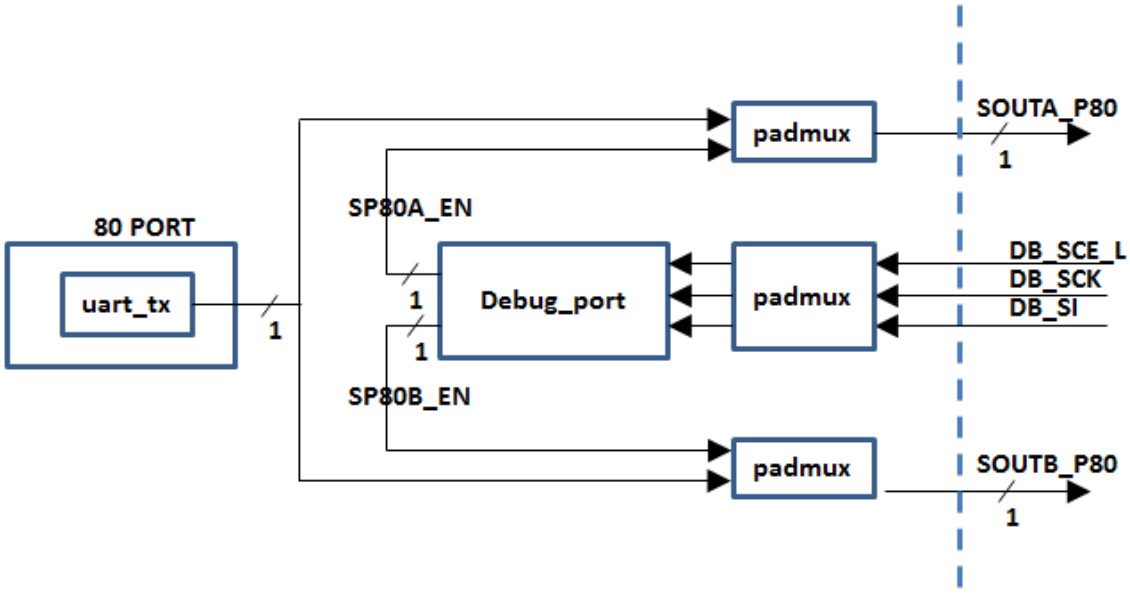


Figure 20-1 Degug port block diagram

Table 20-1 Debug port data output selection.

SELECT COMMAND	SP80A_EN	SP80B_EN
select command = 1	1	0
select command = 2	0	1
select command = 3	1	1

20. TOP MARKING SPECIFICATIONS

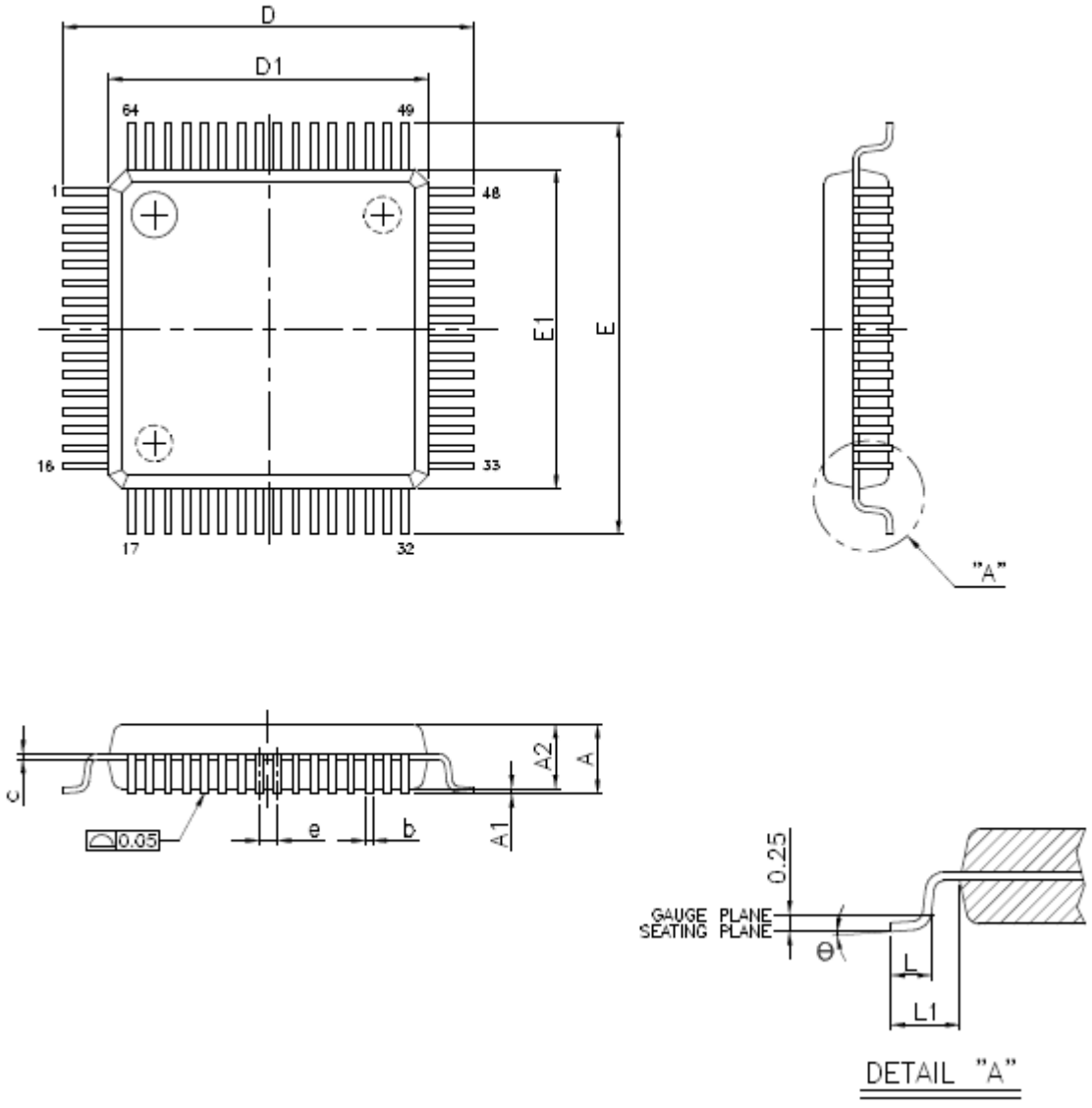
1st line: Nuvoton logo
2nd line: part number: NCT5569D (Green package)
3rd line: wafer production series lot number: **28201234**
4th line: tracking code 634G7AFA

634: packages made in 2016, week 34
G: assembly house ID; G means GR, A means ASE, etc
7: code version; 7 means code 007
A: IC revision; A means version A; B means version B, and C means version C
FA: Nuvoton internal use

21. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
NCT5569D	64Pin LQFP (Green package)	Commercial, 0°C to +70°C

22. PACKAGE SPECIFICATION



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

64-pin (LQFP, 7x7x1.4mm)

23. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.1	04/18/2016	N.A.	Draft datasheet to define features and pin configuration
0.2	04/26/2016	N.A.	Re-define the pin configuration; remove AMD power sequence, AMD TSI, SMBus and CIR functions
0.3	06/16/2016	N.A.	Correct SYSTIN & CPUTIN pin configuration
1.0	09/23/2016	N.A.	Complete datasheet release to public

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Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.