MachOne™

82C935

Integrated PCI Audio Processor

Data Book

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Integrated PCI Audio Processor

1.0 Overview

The OPTi MachOne™ is a single chip PCI audio processor that taps the power and performance of the 132MB/sec PCI bus without sacrificing essential legacy support for the huge installed base of Sound Blaster™ compatible applications. With strict adherence to ISA 1.0 and PCI 2.1 PnP standards, the MachOne delivers the highest assurance of system and operating system compatibility. The MachOne is ideal for desktop, notebook, mobile, and embedded applications requiring a high level of integration and uncompromising sound quality.

The MachOne's PCI bus master interface ensures extremely low system overhead for audio data transfers, freeing the use of system memory for downloadable MIDI patchsets or Microsoft DirectMusic™ samples. By utilizing both 3V and 5V, the MachOne delivers the optimal balance between power consumption and performance.

Hi-Fidelity

OPTi's third-generation 16-bit Sigma-Delta codec provides high quality analog-to-digital and digital-to-analog conversions. The Sigma Delta codec is integrated with a low distortion complex mixer and a 3D stereo expander which dramatically enhances the audio experience with only standard speakers. Digital audio output provides support for digital speakers or external mixers, and a General Purpose I/O port is provided for external audio controllers.

In addition to the 20 OPTiFM™ voices, the MachOne architecture provides powerful audio software enhancements, including wavetable, and 3D positioning acceleration—making the MachOne an ideal gaming platform. The Digital Game Port Timer improves overall system performance by offloading from the CPU.

Expandability

The MachOne is an ideal building block for advanced audio solutions. The MPU-401 port supports external MIDI devices, such as keyboards. Two sets of asynchronous I/O ports support Zoom Video, hardware wavetable, speaker phone, Digital CD-In, DSP data and more.

Mobile Application

The MachOne supports both ACPI and APM which makes it an ideal audio solution for mobile applications. The MachOne supports the industry-standard AC-LINK; an ideal docking station interface. The small audio footprint of the MachOne 128-pin LQFP package saves valuable real estate which is prized in space constrained notebook designs.

Integration

The high level of integration of the MachOne eliminates the requirement for additional memory, codecs, 3D, and other discrete components. This minimizes the design effort as well as the total cost of design implementation.

The combination of PCI, outstanding legacy SB Pro Compatibility, smallest audio footprint, and Notebook optimization extensions make the MachOne the ideal audio solution for desktop, notebook, mobile, and embedded applications requiring a high level of integration and uncompromising sound quality.

2.0 Features

- 32-bit PCI Bus Master, PCI 2.1 compliant.
- Integrated sound controller compatible with Sound Blaster (SB) Pro, Ad Lib, and Microsoft Windows Sound System (WSS).
- SB Pro/ WSS Compatibility
  - Support distributed DMA, virtual DMA with stream scatter/gather buffer control.
  - Support Serial IRQ and Drive-back IRQ.
- Support stream scatter/gather buffer to improve PCI bus bandwidth.
- ISA 1.0 and PCI 2.1 Plug and Play compatible.
- Built-in AC-97 compatible Codec.
- Supports optional external AC-97 Codec through AC-LINK.
- Full duplex operation: Record and playback simultaneously.
- Support IMA ADPCM, μ-Law, A-Law decompression.
- High-quality 20-voice, 52-operator, enhanced OPTiFM music synthesizer.
- Built-in 16-bit Sigma-Delta Stereo codec.
- Built-in 7-channel mixer: 5 stereo channels and 2 mono channels.
- 64-step master volume control.
- QSound 3D Sound Enhancement.
- Integrated MIDI UART with FIFO for both input and output with MPU-401 interface.
- Integrated dual game port with Digital Game Port Interface.

- Push Button Volume Control interface.
- Programmable Serial Port interface for:
  - External DSP for sound effect.
  - Telephony Codec support.
  - External Wave Table digital Interface.
  - Zoom Video port.
- Four programmable I/O pins.
- 5V voltage supply.
- Support ACPI power-down mode.
- Digital PC Speaker support.
- 20-bit 1µs resolution DirectX timer.
- 128-pin LQFP package or 128-pin PQFP package.

Figure 2-1 System Block Diagram

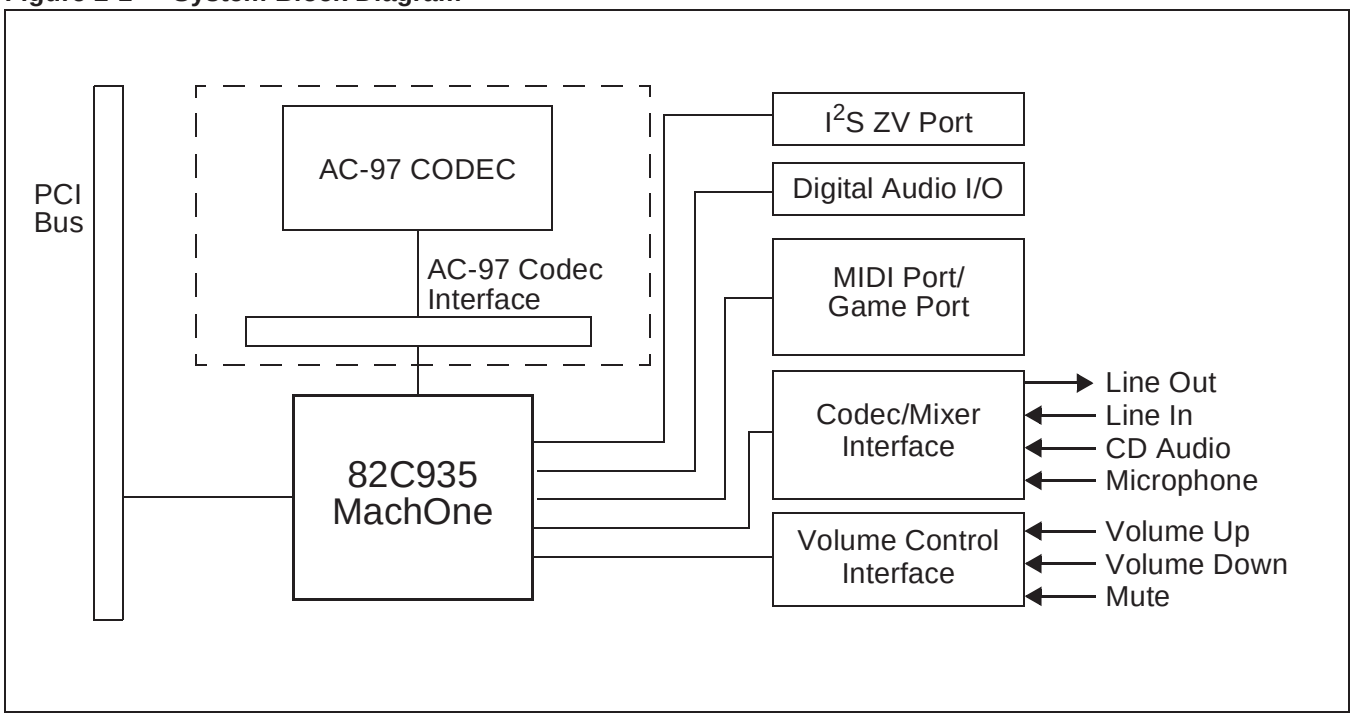
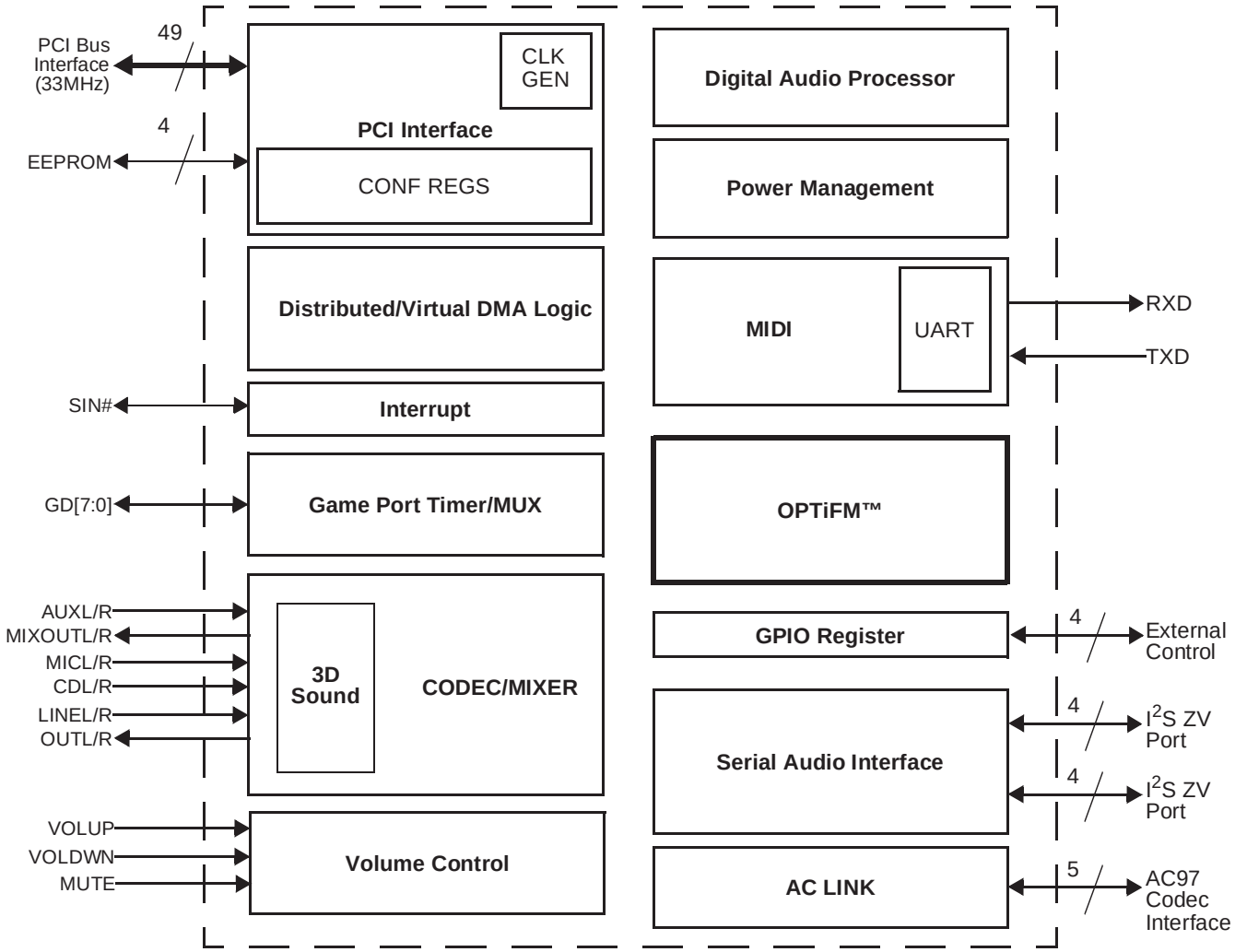


Figure 2-2 Simplified Functional Block Diagram



3.0 Signal Definitions

Figure 3-1 128-Pin PQFP/LQFP Pin Diagram

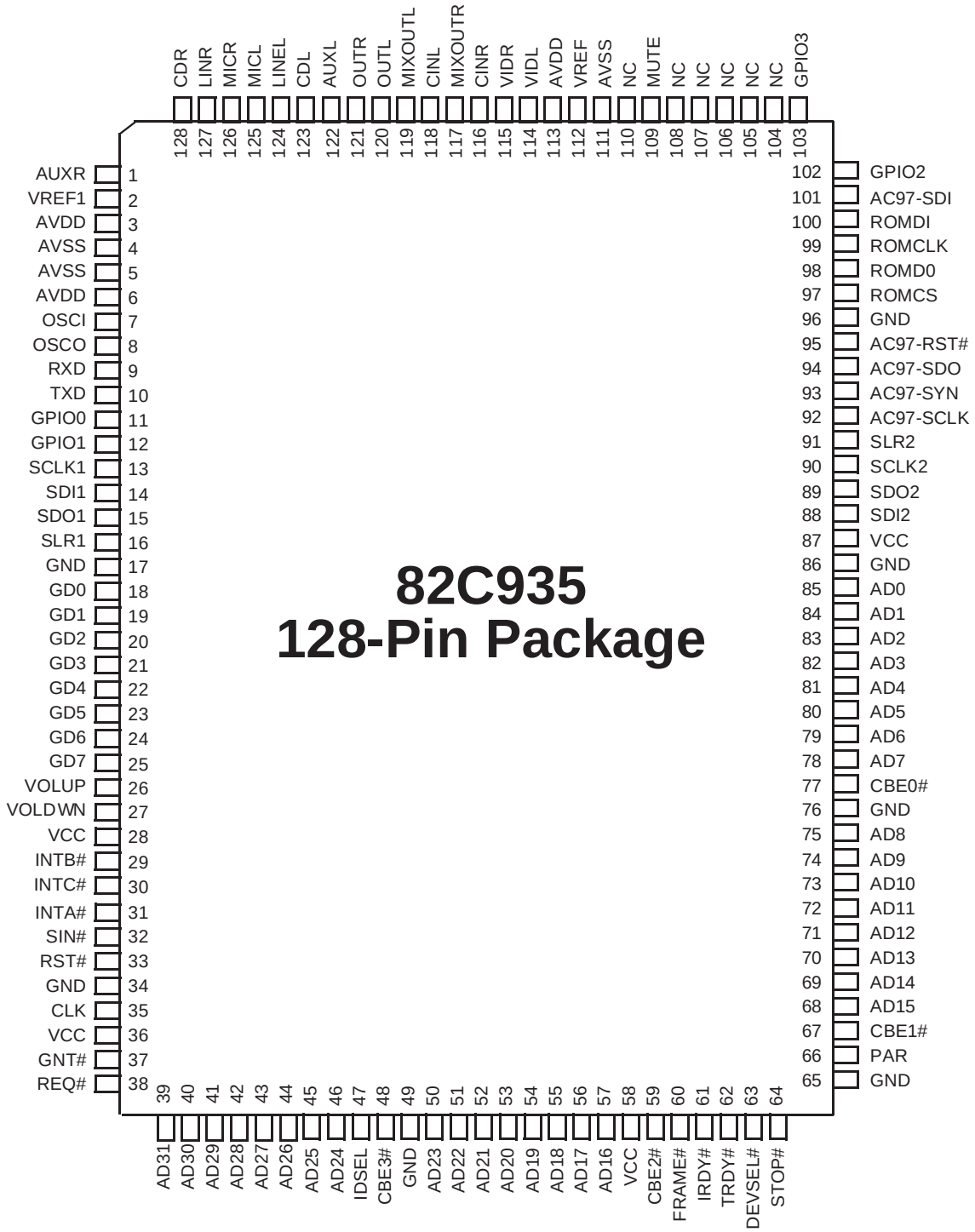


Table 3-1 128-Pin Package Pin Listing - Alphabetical Cross-Reference

Signal Name	Pin
AC97-RST#	95
AC97-SCLK	92
AC97-SDI	101
AC97-SDO	94
AC97-SYN	93
AD0	85
AD1	84
AD2	83
AD3	82
AD4	81
AD5	80
AD6	79
AD7	78
AD8	75
AD9	74
AD10	73
AD11	72
AD12	71
AD13	70
AD14	69
AD15	68
AD16	57
AD17	56
AD18	55
AD19	54
AD20	53
AD21	52
AD22	51
AD23	50
AD24	46
AD25	45
AD26	44
AD27	43
AD28	42
AD29	41
AD30	40
AD31	39
AUXL	122
AUXR	1
AVDD	3
AVDD	6
AVDD	113
AVSS	4
AVSS	5
AVSS	111
CBE0#	77
CBE1#	67
CBE2#	59
CBE3#	48
CDL	123
CDR	128
CINL	118
CINR	116
CLK	35
DEVSEL#	63
FRAME#	60
GD0	18
GD1	19
GD2	20
GD3	21
GD4	22
GD5	23
GD6	24
GD7	25
GND	17
GND	34
GND	49
GND	65
GND	76
GND	86
GND	96
GNT#	37
GPIO0	11
GPIO1	12
GPIO2	102
GPIO3	103
IDSEL	47
INTA#	31
INTB#	29
INTC#	30
IRDY#	61
LINEL	124
LINER	127
MICL	125
MICR	126
MIXOUTL	119
MIXOUTR	117
MUTE	109
NC	104
NC	105
NC	106
NC	107
NC	108
NC	110
OSCI	7
OSCO	8
OUTL	120
OUTR	121
PAR	66
REQ#‘	38
ROMCLK	99
ROMCS	97
ROMDI	100
ROMDO	98
RST#	33
RXD	9
SCLK1	13
SCLK2	90
SDI1	14
SDI2	88
SDO1	15
SDO2	89
SIN#	32
SLR1	16
SLR2	91
STOP#	64
TRDY#	62
TXD	10
VIDL	114
VIDR	115
VCC	28
VCC	36
VCC	58
VCC	87
VOLDWN	27
VOLUP	26
VREF	112
VREFI	2

Table 3-2 Signal Descriptions

Signal Name	Pin No.	Pin Type	I/O Type	Signal Description	To/From
PCI Bus Signals					
AD[31:0]	39-46, 50-57, 68-75, 78-85	I/O	TTL	Address and Data	PCI Bus
C/BE#[3:0]	48, 59, 67, 77	I/O	TTL-SMT	Bus Command and Bus Enable	PCI Bus
PAR	66	I/O	TTL-SMT	Parity	PCI Bus
FRAME#	60	I/O	TTL-SMT, pull-up	Frame, bus cycle start	PCI Bus
IRDY#	61	I/O	TTL-SMT, pull-up	Initiator Ready	PCI Bus
TRDY#	62	I/O	TTL-SMT, pull-up	Target Ready	PCI Bus
DEVSEL#	63	I/O	TTL-SMT, pull-up	Device Select	PCI Bus
STOP#	64	I/O	TTL-SMT, pull-up	Stop cycle	PCI Bus
IDSEL	47	I	TTL-SMT	Initialization Device Select	PCI Bus
RST#	33	I	TTL-SMT	Reset	PCI Bus
REQ#	38	O-T	TTL	Bus Request	PCI Bus
GNT#	37	I-T	TTL-SMT	Bus Grant	PCI Bus
INTA# INTB# INTC#	31, 29, 30	OD	TTL	Interrupt Request	PCI Bus
CLK	35	I	TTL	33MHz Clock	PCI Bus
Game Port					
GD7	31	I/O	CMOS-SMT 8mA	Game Port Data	Gport/ External CS
GD6	30				
GD5	29				
GD4	28				
GD3	26		CMOS-SMT 16mA		
GD2	25				
GD1	24				
GD0	23				
Serial IRQ					
SIN#	32	I/O	TTL	Serial In/Out	
Serial Audio Interface 1					
SCLK1	13	I/O	TTL	Serial Clock	SAP
SDI1	14	I	TTL	Serial Data In	SAP
SDO1	15	O	TTL	Serial Data Out	SAP

Signal Name	Pin No.	Pin Type	I/O Type	Signal Description	To/From
SLR1	16	O	TTL	Sample Clock	SAP
Serial Audio Interface 2					
SCLK2	90	I/O	TTL	Serial Clock	SAP
SDI2	88	I	TTL	Serial Data In	SAP
SDO2	89	O	TTL	Serial Data Out	SAP
SLR2	91	O	TTL	Sample Clock	SAP
EEPROM Interface					
ROMCS	97	O	TTL	ROM Chip Select	
ROMCLK	99	O	TTL	ROM Clock	
ROMDO	98	O	TTL	ROM Data Out	
ROMDI	100	I	TTL	ROM Data In	
AC LINK Interface					
AC97-RST#	95	O	TTL	AC97 Reset	
AC97-SCLK	92	I	TTL	AC97 System Clock	
AC97-SYN	93	O	TTL	AC97 SYN	
AC97-SDO	94	O	TTL	AC97 Serial Data Out	
AC97-SDI	101	I	TTL	AC97 Serial Data In	
General Purpose Bit I/O					
GPIO[3:0]	103, 102, 12, 11	I/O	TTL	General Purpose Bit I/O	
Volume Control					
VOLUP	26	I	TTL	Volume Up	
VOLDWN	27	I	TTL	Volume Down	
MUTE	109	I	TTL	Volume Mute	
MIDI Interface Signal					
RXD	9	I	TTL-SMT	Receive Data	MIDI Port
TXD	10	O	TTL, 20mA	Transmit Data	MIDI Port
Codec/Mixer Interface Signal					
MICL MICR	125 126	I	Analog	Microphone Input Left/Right	ANALOG
LINEL LINER	124 127	I	Analog	Line Input Left/Right	ANALOG
CDL CDR	123 128	I	Analog	CD Input Left/Right	ANALOG

Signal Name	Pin No.	Pin Type	I/O Type	Signal Description	To/From
AUXL AUXR	122 1	I	Analog	Auxiliary Input Left/Right	ANALOG
VIDL VIDR	114 115	I	Analog	Video Input Left/Right	ANALOG
OUTL OUTR	120 121	O	Analog 10KΩ, 25pF drive	Output Left/Right	ANALOG
MIXOUTL MIXOUTR	119 117	O	Analog	Mixer Output Left/Right	ANALOG
CINL CINR	118 116	I	Analog	Analog-Digital Convertor Filter Left/ Right	ANALOG
VREFI	2	O	Analog	Analog Reference	ANALOG
VREF	112	O	Analog	Voltage Reference	ANALOG
OSCI	7	I	Analog	Oscillator Input	
OSCO	8	O	Analog	Oscillator Output	
Power, Ground, No Connect (NC) Pins					
VCC	28, 36, 58, 87	I	PWR	Power Connection	
GND	17, 34, 49, 65, 76, 86, 96	I	GND	Ground Connection	
AVDD	3, 6, 113	I	PWR	Analog Power Connections	
AVSS	4, 5, 111	I	GND	Analog Ground Connections	
NC	104-108 110			No Connect	

4.0 Functional Description

The 82C935 is an optimized single chip solution with built-in Plug-and-Play functions, built-in 3D sound enhancement processor, built-in FM synthesizer and 16-bit Sigma-Delta Codec to provide all of the features needed to create the following sound characteristics and applications:

- 16-bit sound quality Sound Blaster Pro and Windows Sound System compatible card
- 3D spatial widened stereo
- 22 voice FM synthesis
- 16-bit CD-quality digital wave audio up to 44.1KHz stereo
- Game port
- MPU-401 MIDI interface
- Wavetable synthesis upgrade

The following sub-sections will discuss these built-in functions in detail.

4.1 AC-LINK

The 82C935 supports an external AC-LINK codec (AC97).

AC-LINK	Type	Set 1 (128-Pin)
AC97-RST#	O	GPIO1 (pin 95)
AC97-SYN	O	INTC# (pin 93)
AC97-SCLK	I	SIN# (pin 92)
AC97-SDO	O	VOLUP (pin 94)
AC97-SDI	I	VOLDWN (pin 101)

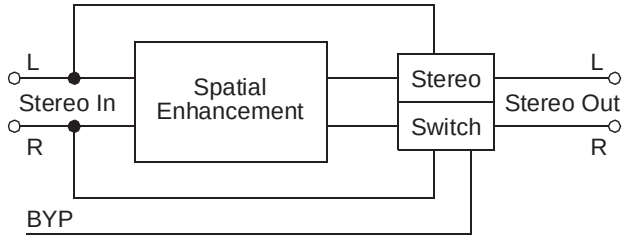
4.2 Serial IRQ

The 82C935 supports serial IRQ. The IRQ signal is transmitted through pin 32. The SIRQ is enabled at bit 0 of PCI Extended Register PCICFG 62h.

4.3 3D Sound Enhancement Processor

The 82C935 includes the 3D sound enhancement processor from QSound Labs Inc. The 3D audio enhancement is achieved while using normal left-and-right channel stereo speakers.

The following block diagram shows the functional element of the 3D sound enhance processor in the 82C935.



4.4 16-Bit Type F DMA Playback

The 82C935 supports the Type F DMA playback.

4.5 Push Button Volume Control

In silicon revision 1.0, three pins are used as volume control push-buttons (pin 27 as volume down, pin 26 as volume up, and pin 109 as mute) so that the speaker volume can be controlled through front panel buttons in desktop or notebook PCs. Appropriate software drivers are needed to enable this feature.

These three pins are active-low, edge-triggering and pulled up internally. When the button is pressed and the corresponding pin is activated, the register bits MCIR16[5:3] are set accordingly. The software drivers poll these three bits periodically. The scheme is as follows:

Buttons	MCIR16[5:3] (BUTUP:BUTDN)	Action required for the driver
Press UP button	100	increase the volume by one step
Press Down button	010	decrease the volume by one step
Press Mute button	001	mute

The register bits MCIR16[5:3] will be cleared automatically after they are read by the driver.

4.6 16-Bit Codec/Mixer

4.6.1 Codec

Features of the built-in 16-bit stereo sigma-delta codec include:

- Sigma-delta stereo ADC with 128X over-sampling
- Sigma-delta stereo DAC with 128X over-sampling
- On-chip 8X Interpolation Filter
- On-chip analog post filter
- Single-ended input and output
- Sampling rate of 5KHz to 48KHz

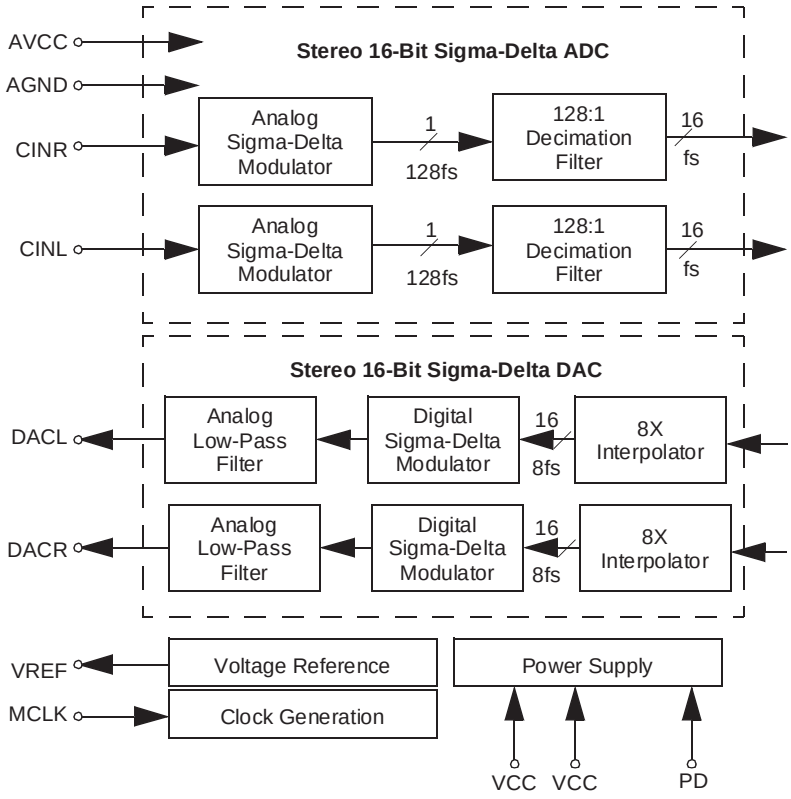
The codec serial interface provides a means to read and write 16-bit stereo data from the ADC or to the DAC respectively. The interface (as shown in Figure 4-1) consists of the following lines:

- DAC[15:0] - to write to the DAC 16-bit input
- ADC[15:0] - to read the ADC 16-bit output
- L/R - to select between the left and right channels for both the ADC and DAC data.
- MCLK - This internal master clock signal is synthesized by the frequency synthesizer from the crystal reference of 14.318MHz. One of 236 frequencies may be selected through the 8-bit FSEL line. MCLK is not active when the frequency synthesizer is powered down. The frequency of MCLK is 256 times the sampling frequency.

The DAC left/right 16-bit input data are multiplexed onto DAC[15:0] and fed into the codec. The L/R signal qualifies the data. The period of L/R is equal to that of the codec sampling frequency. One set of left/right 16-bit input data to the DAC is sent every L/R cycle. When L/R is low, the data on DAC[15:0] is meant for the left channel; when L/R is high, the data is meant for the right channel. This means that the DAC treats data packets L1 and R1 as belonging to the same sampling instance; while L2 and R2 are data for the next sampling instance.

The ADC left/right 16-bit output data are similarly multiplexed onto the ADC[15:0] bus.

Figure 4-1 Functional Block Diagram

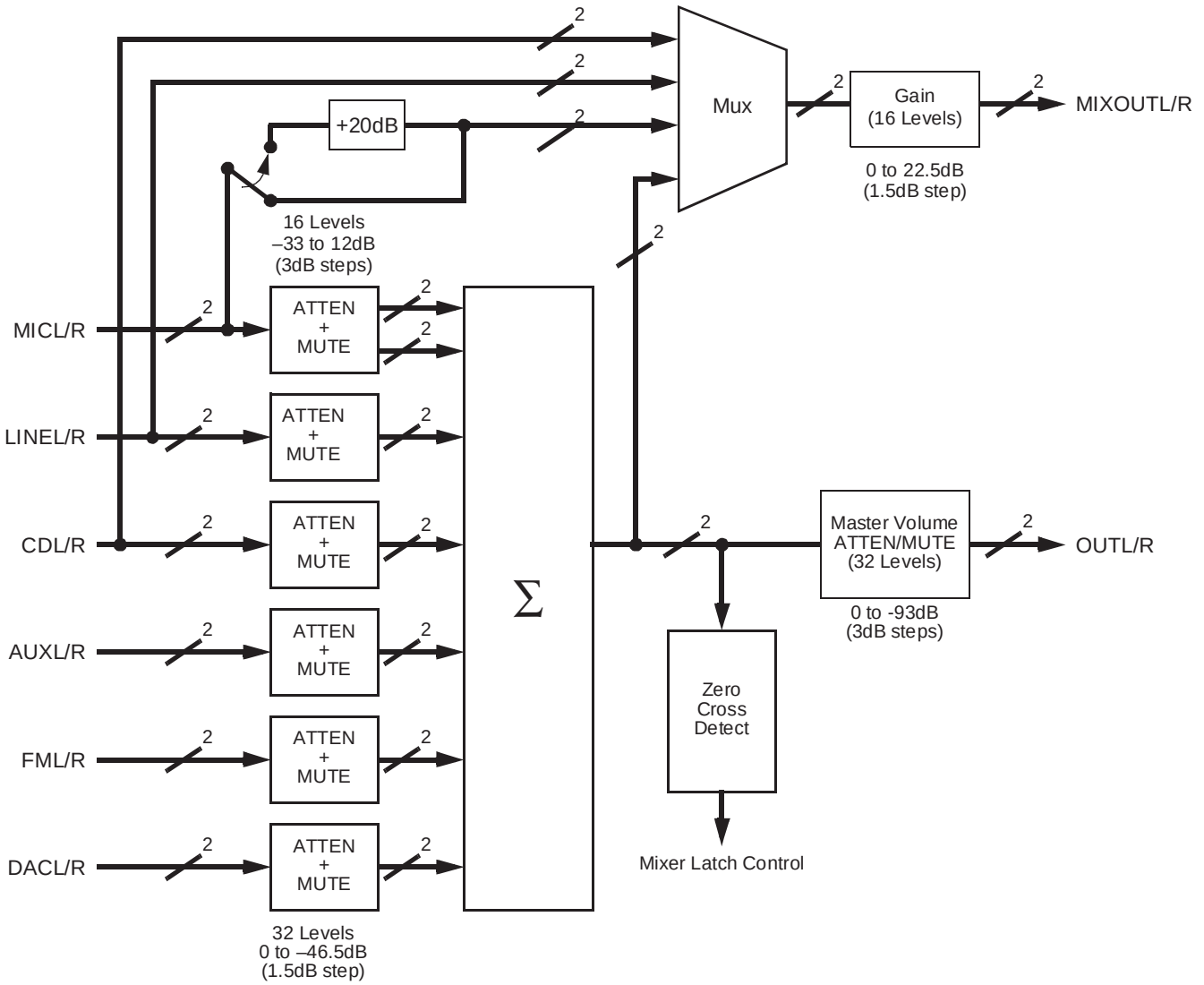


4.6.2 Mixer

The built-in mixer mixes two mono microphone level inputs (MICL/R) and five stereo analog line level input sources (LINEL/R, CDL/R, AUXL/R, FML/R, and DACL/R) with individual mixer programmable gain and mute control. The DACL/R stereo analog inputs are routed to a programmable circuit with 1.5dB steps (total of 32 levels). Internal amplifiers with a programmable 20dB gain block are provided for the MIC input (only). The remaining stereo analog inputs are routed to a programmable gain circuit which can be programmed in 3dB steps (total of 16 levels). Also, internal amplifiers with a programmable 20dB gain block are provided. Level changes only take effect on zero crossings to minimize audible artifacts. AC coupling is mandatory for these inputs since any DC offset on the input will be amplified.

MIXOUTL (mixer record output left) must be connected to CINL (codec analog input left) with a ceramic capacitor. MIXOUTR (mixer record output right) must be connected to CINR (codec analog input right) with a ceramic capacitor. MIXOUT/R are routed via gain control (1.5dB steps: total of 16 levels). Analog output OUTL/R are routed via a master volume control which provides 0db to 94.5db of attenuation, adjustable in 3dB steps. The Codec Indirect Registers used for programming the various functions/gain levels for the mixer. For details regarding these registers, refer to Table 5-10 in the Register Section. Figure 4-2 shows a functional block diagram of the mixer.

Figure 4-2 Mixer Block Diagram



4.7 External Serial EEPROM

The 82C935 has the resource data and serial identifier required by the PnP specification stored internally. If an OEM customer wants to use a different resource data and serial identifier to customize their application, an external EEPROM can be used. To use an external EEPROM, pin 97 (ROMCS) must be pulled low. This enables the resource data and serial identifier to be read from the external EEPROM instead of the 82C935's internal storage.

The 82C935 provides a serial EEPROM interface that is compatible with devices from a number of vendors. Pin 99 of the 82C935 provides the data clock for the EEPROM. Pin 98 provides data to the EEPROM, while pin 100 gets input from the EEPROM.

4.8 Serial Audio Interface

The 82C935 supports two sets of serial audio interface.

	Set 1	Set 2
SCLK	Pin 13	Pin 90
SDI	Pin 14	Pin 88
SDO	Pin 15	Pin 89
SLR	Pin 16	Pin 91

The 82C935's serial audio interface supports the following formats:

- I^2S-justified format (ZV port) and its variations.
- Sony format (short right-justified format, used by OPTi's wavetable chip and the Philips TDA1311AT DAC).
- AT&T PCM codec T7525 compatible16-bit mono format.

Please refer to sections 4.8.6, *ZV-Port I2S*, 4.8.7, *Advanced Precision General Purpose Serial Port*, 4.8.8, *TDA1311 Stereo Continuous Calibration*, for the respective timing diagrams.

4.8.1 I^2S-justified format and its variations

In the I^2S-justified format (ZV-port), LRCLK is low for the left channel, and high for the right channel. The left-channel MSB is left-justified to the high-to-low LRCLK transition with a single SCLK delay. SDATA could be SADI when the 935 is in receive mode, and SADO when the 935 is in transmit mode. The LRCLK period is programmable with a minimum of 32 SCLKs (MC22[4]). The following example assumes LRCLK period is greater than 32 SCLKs. Please note that in ZV port, there is one more signal MCLK defined but this is not needed for the 935.

To program the 935 in the I^2S-justified mode, the MC22 and MC21 registers need to be set. The relevant MC22 and MC21 bit definitions are shown below for reference.

I^2S-justified mode (ZV-port):
MC22[7:0] = "00110001" (31H).
MC21[7:0] = "10000010" (82H).

There are other I^2S variations: left-justified and right-justified.

For the left-justified, LRCLK is high for the left channel, and low for the right channel. The MSB is left-justified to an LRCLK transition, with zero SCLK delay.
MC22[7:0] = "00110100" (34H).
MC21[7:0] = "10000010" (82H).

For the right-justified, LRCLK is high for the left channel, and low for the right channel. The MSB is delayed from an LRCLK transition, the LSB will be right-justified to the next LRCLK transition.
MC22[7:0] = "00010100" (14H).
MC21[7:0] = "10000010" (82H).

4.8.2 Sony format[1]

This data format is essentially the same as the I^2S right-justified format. Normally there are only 32 SCLKs in a LRCLK period. The LRCLK is high for the left channel, and low for the right channel. The MSB comes in first. To set up the 935 in Sony format:
MC22[7:0] = “00000100” (04H).
MC21[7:0] = “10000010” (82H).

4.8.3 AT&T PCM codec T7525 compatible 16-bit mono format

The 935 supports the T7525 receive timing - word format with positive FSYNC. The benefit is that the 935's secondary DAC could be used to save a T7525 as the voice codec in modem/audio combo solution. To program the 935 in T7525 mode:
MC22[7:0] = “00110010” (32H)
MC21[7:0] = “10000010” (82H)

In short summary:

	I^2S-justified	left-justified	right-justified	Sony format	T7525 format
MC22[7:0]	31H*	34H*	14H*	04H*	32H
MC22[7:0]	82H				

* The MC22[4] bit setting may vary, depending on the LRCLK period (32 SCLK or more).

1. Short right-justified format, used by OPTi's wavetable chip and the Philips TDA1311AT DAC.

4.8.4 Testing I^2S format (ZV port) with Audio Precision machine

The Audio Precision machine system two 2322 has a serial audio data port that can generate a test tone in the I^2S format with programmable FSYNC, ranging from 24KHz to 48KHz. The 935 was tested with AP machine in various test tones: 256Hz, 1KHz and 3KHz in both sine wave and square wave with FSYNC = 48KHz.

To test out the feature, the AP machine is hooked up with the 935 with appropriate connections (AP's pin#6, 12, 14 are SDATA, SCLK and FSYNC, respectively). The next step is to setup the MC22 to “31H” and MC21 to “82H”. Then the test tone could be heard from the speaker connected to the 935. Please note that there might be some noise in the speaker. This is due to unshielded cable used to connect the serial audio interface. Shielding the cable would help improve the audio quality.

4.8.5 Relevant MC register settings

MC22 Serial Audio format control register (R/W)							**Default: 00h**
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
Reset ASIO	ASIO test enable	**First16-bit**	**CLK32**	**SCLK Polarity**	**FSYNC Polarity**	**Pulse Mode**	**I^2S Mode**

Bit 5 First16-bit: Specifies where the data is located in the LRCLK period
- 0: data located at the last 16 bits of the left/right channel in an LRCLK period
- 1: data located at the first 16 (or 17) bit of the left/right channel in an LRCLK period

Bit 4 CLK32: Specifies the number of SCLKs per LRCLK period, used only in delay-mode or pulse-mode ASIO
- 0: 32 SCLK per LRCLK period
- 1: more than 32 SCLK per LRCLK period

Bit 3 SCLK polarity:
- 0: SDATA and LRCLK change at the rising edge of SCLK
- 1: SDATA and LRCLK change at the falling edge of SCLK

Bit 2 FSYNC (LRCLK) polarity:
- 0: LRCLK is LOW for the left channel, HIGH for the right channel
- 1: LRCLK is HIGH for the left channel, LOW for the right channel

Bit 1 Pulse mode: Used for AT&T T7525 codec or CS8412 DSP data format
- 0: Pulse mode disabled
- 1: Pulse mode enabled, used for AT&T T7525 or CS8412 data format

Bit 0 I^2S mode: MSB delay mode
- 0: Zero SCLK delay from an LRCLK transition to MSB data
- 1: One SCLK delay from an LRCLK transition to MSB data

MC21 Serial Audio selection control register (R/W)							**Default: 00h**
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
CTL_SEL[1:0]		P2S_SEL[1:0]		SPCDSEL	ADCSEL	**FDACSEL**	DACSEL

bit [7:6] CTL_SEL[1:0]: ASIO shift clock selection
- 00/11: Use the shift clock from internal FS
- 01: Use FM timing
- 10: Use external SCLK

bit 1 FDACSEL: selects the data source to the FDAC
- 0: FDAC takes FM data
- 1: FDAC takes SADI (if SPCDSEL=0) or second DMA playback data (if SPCDSEL=1)

4.8.6 ZV-Port I²S

4.8.6.1 LRCLK

This signal determines which audio channel (left/right) is currently being input on the audio Serial Data input line. LRCLK is low to indicate the left channel and high to indicate the right channel. Typical frequency values for this signal are 48KHz, 44.1KHz, 32KHz, and 22KHz.

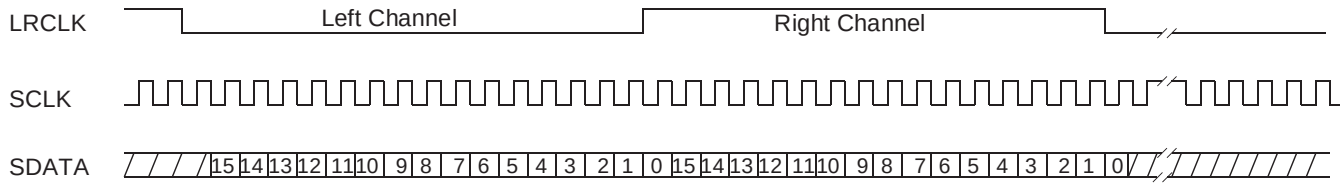
4.8.6.2 SDATA

This signal is the digital PCM signal that carries the audio information. Digital audio data is transferred using the I²S format.

I²S Format

The I²S format is shown below. The digital audio data is left channel-MSB justified to the high-to-low going edge of the LRCLK plus one SCLK delay.

Figure 4-3 I²S Format



4.8.6.3 SCLK

This signal is the serial digital audio PCM clock.

4.8.6.4 MCLK

This signal is the Master clock for the digital audio. MCLK is asynchronous to LRCLK, SDATA and SCLK.

The MCLK must be either 256x or 384x the desired Input Word Rate (IWR). IWR is the frequency at which words for each channel are input to the DAC and is equal to the LRCLK frequency. The following table illustrates several standard audio word rates and the required MCLK and LRCLK frequencies. Typically, most devices operate with 384fx master clock.

The ZV Port audio DAC should support an MCLK frequency of 384fs. This results in the frequencies shown below.

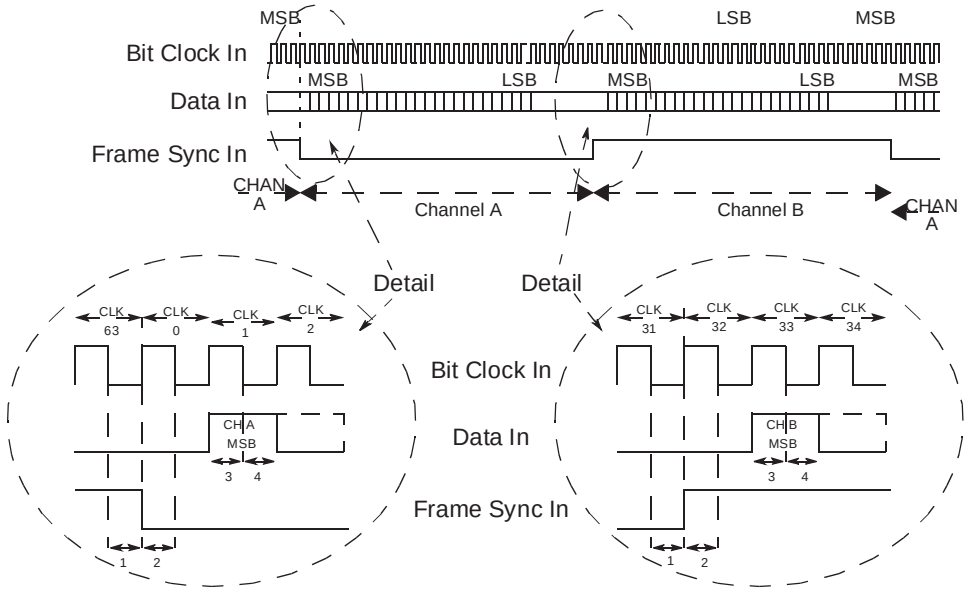
LRCLK (KHz) Sample Frequency	SCLK (MHz) 32xfs	MCLK (MHz) 384x
22	0.704	8.448
32	1.0240	12.2880
44.1	1.4112	16.9344
48	1.5360	18.4320

4.8.7 Advanced Precision General Purpose Serial Port

The 15-pin "D-sub" connector on the rear panel provides all input and output signals for a general purpose serial input.output port, plus DSP-program specific input and output pins which may be used in certain DSP (.AZ2) programs. The pinout of the connector is detailed below. All inputs are TTL level compatible CMOS. All outputs are CMOS isolated by 50Ω series resistors and rise time limiting networks.

Pin	Function	Pin	Function
1	Ground	9	Serial Input Master Clock (input)
2	+5V (tied to unused inputs high)	10	Serial Input Bit Clock (input)
3	Auxiliary Input (DSP program specific)	11	Auxiliary Output (DSP program specific)
4	Ground	12	Serial Output Bit Clock (output)
5	Ground	13	Serial Input Data (input)
6	Serial Output Data (output)	14	Serial Output Frame Sync (output)
7	Ground	15	Serial Input Frame Sync (input)
8	Ground		

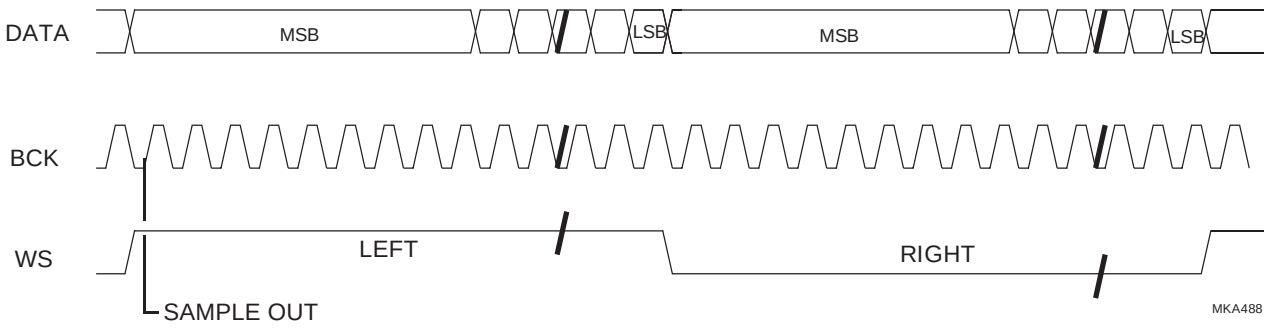
Figure 4-4 General Purpose Serial Port, Timing Relationships



1. FRAME SYNC INPUT SETUP TIME (from falling edge, las bit clock previous subframe) 30nS minimum
2. FRAME SYNC INPUT SETUP TIME (to falling edge, first bit clock of present subframe) 30nS minimum
3. DATA INPUT SETUP TIME (to bit clock falling edge) 30nS minimum
4. DATA INPUT HOLD TIME (from bit clock falling edge) 45nS minimum

4.8.8 TDA1311 Stereo Continuous Calibration

Figure 4-5 Format of Input Signals



5.0 Register Set

The 82C935 register set comprises three Control Register groups:

- PCI Configuration Registers - PCICFG Audio
- Legacy Register
- Extended MC Registers - MCIdx

Table 5-1 Register Map

PCI Configuration Registers				
PCI Base Register Group: PCICFG 00h-3Fh				
Device ID		Vendor ID		00h
PCI Status		Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Latency Timer	Reserved	0Ch
(SB-compatible Base Address)				10h
(WSS-compatible Base Address)				14h
(FM Synthesis Base Address)				18h
(MIDI Base Address)				1Ch
(Game Port Base Address)				20h
(MC Base Address)				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Reserved				30h
Reserved			Cap_Ptr	34h
Reserved				38h
Max_lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
PCI Extended Mode Register Group: PCICFG 40h-FFh				
Power Control Latch Registers (1-4)				40h
DMA Channel Selector Registers (1-4)				44h
IRQ Channel Selector Registers (1-4)				48h
Reserved		IRQ Channel Selector Registers (5-6)		4Ch
SMU Status	Feature Control	ISA Control	Hot Docking Control	50h
IRQ Driveback Protocol Address				54h
DRQ Remap Base Address				58h
Write Posting Status	Write Posting Control	ISA Slot Control (1-2)		5Ch
Reserved	SIRQ Control	DMA Feature Control		60h
Reserved				64h-DBh
Power Management Capabilities		Reserved		DCh
Reserved	Reserved	Power Management Control Status		E0h
Reserved				E4h-FFh
Legacy Register				
MCBase Register (Set by PCICFG 24h)				
Base/Type Configuration				MCIR1
BUAD 96				MCIR2
Sound Blaster/Windows Sound System Configuration				MCIR3
User Programmable General Purpose				MCIR4

Table 5-1 Register Map (cont.)

Option		MCIR5
MIDI Interface		MCIR6
Semaphore Software Register		MCIR7
Reserved		MCIR8
Test Control		MCIR9
Test Control		MCIR10
Status		MCIR11
Test		MCIR12
PNP Status		MCIR13
PNP CSN		MCIR14
PNP Read Port		MCIR15
Volume Control		MCIR16
Serial EEPROM Control		MCIR17
CONFIG Status		MCIR18
FM Control		MCIR19
GPIO Control 0		MCIR20
Serial Audio Control 0		MCIR21
Serial Audio Control 1		MCIR22
Serial Audio Clock/Output Control		MCIR23
Game Port Counter Setup and Status		MCIR24
Game Port Counter Values		MCIR25
FDAC Data Control		MCIR26
Reserved		MCIR27-31
Extended MC Register Group		
AC-LINK Index		MCRI32
AC-LINK Data		MCIR33
AC-LINK Control		MCIR34
Extended Digital Power Management		MCIR35
Extended Analog Power Management		MCIR36
Miscellaneous Control Register		MCIR37
Functional Interrupt Status Register		MCIR38
Timer [7:0]		MCIR39
Timer [15:8]		MCIR40
Timer Control	Timer [19:16]	MCIR41
Test		MCIR42
Pin Configuration		MCIR43
AC97 Reset		MCIR44
Reserved		MCIR45-63
SBBase Register (Set by PCICFG 10h)		
Left FM Status Port (RO)		SBBase+00h (ALBase+00h)
Left FM Register Address Port (WO)		SBBase+00h (ALBase+00h)
Left FM Data Port (WO)		SBBase+01h (ALBase+01h)
Right FM Register Address Port (WO)		SBBase+02h (ALBase+02h)

Table 5-1 Register Map (cont.)

Right FM Data Port (WO)	SBBase+03h (ALBase+03h)
Mixer Address Port (WO)	SBBase+04h
Mixer Data Port (R/W)	SBBase+05h
DAP Reset (WO)	SBBase+06h
FM Status Port (RO)	SBBase+08h
FM Register Address Port (WO)	SBBase+08h
FM Data Port (WO)	SBBase+09h
DAP Read Data (RO)	SBBase+0Ah
DAP Write Data/Cmd (WO)	SBBase+0Ch
DAP Write Buffer Status (RO)	SBBase+0Ch
DAP Output Buffer Status (RO)	SBBase+0Eh
WSBase Register	
Configuration (WO)	WSBase+ 00h-03h
Version (RO)	WSBase+ 00h-03h
Codec Index (R/W, exists in Codec and shadowed in 82C935)	WSBase+04h
Codec Indexed Data (R/W, exists in Codec only)	WSBase+05h
Codec Status (R/W, exists in Codec only)	WSBase+06h
Codec Direct Data (R/W, exists in Codec only)	WSBase+07h
Codec Indirect Registers	
MIXOUTL Output Control	CIR0
MIXOUTR Output Control	CIR1
CDL Input Control	CIR2
CDR Input Control	CIR3
FML Input Control	CIR4
FMR Input Control	CIR5
DACL Input Control	CIR6
DACR Input Control	CIR7
Fs and Playback Data Format Register	CIR8
Interface Configuration	CIR9
Pin Control	CIR10
Error Status and Initialization	CIR11
ID Register	CIR12
Reserved	CIR13
Playback Upper Base Count	CIR14
Playback Lower Base Count	CIR15
Expanded Mode CIR	
AUXL Input Control	CIR16
AUXR Input Control	CIR17
LINEL Input Control	CIR18
LINER Input Control	CIR19
MICL Input Control	CIR20
MICR Input Control	CIR21
OUTL Output Control	CIR22

Table 5-1 Register Map (cont.)

OUTR Output Control	CIR23
Reserved	CIR24-27
Capture Data Format	CIR28
Reserved	CIR29
Capture Upper Base Count	CIR30
Capture Lower Base Count	CIR31

5.1 PCI Configuration Registers

Table 5-2 PCI Base Register Group: PCICFG 00h-3Fh

7	6	5	4	3	2	1	0
PCICFG 00h			**Vendor Identification Register (RO) - Byte 0: Bits [7:0]**				**Default = 45h**
PCICFG 01h			**Vendor Identification Register (RO) - Byte 1: Bits [15:8]**				**Default = 10h**
PCICFG 02h			**Device ID (RO) - Byte 0: Bits [7:0]**				**Default = 35h**
PCICFG 03h			**Device ID (RO) - Byte 1: Bits [15:8]**				**Default = C9h**
PCICFG 04h			**PCI Command Register - Byte 0: Bits [7:0]**				**Default = 00h**
Reserved: Write bits as read.	PCE - Parity Checking Enabled 0 = Disable 1 = Enable	Reserved: Write bits as read.			BME - Bus Master Operation Enable 0 = Disable 1 = Enable	Reserved	IO - Enable Response to IO
PCICFG 05h			**PCI Command Register - Byte 1: Bits [15:8]**				**Default = 00h**
Reserved: Write bits as read.							
PCICFG 06h			**PCI Status Register - Byte 0: Bits [7:0]**				**Default = 00h**
Reserved	UDF - User Definable Features 0 = Disable 1 = Enable	Reserved	CL - Capabilities List 0 = Disable 1= Enable	Reserved: Write bits as read.			
PCICFG 07h			**PCI Status Register - Byte 1: Bits [15:8]**				**Default = 02h**
Parity error: 0 = No 1 = Yes Write 1 to clear	Reserved	Received master abort: 0 = No 1 = Yes Write 1 to clear	Received target abort: 0 = No 1 = Yes Write 1 to clear	Signalled target abort: 0 = No 1 = Yes Write 1 to clear	DEVSEL# timing (RO): 00 = Fast 01 = Medium 10 = Slow 11 = Reserved		Reserved: Write bits as read.
PCICFG 08h			**Class Code/Revision ID Register (RO) - Byte 0: Bits [7:0]**				**Default = 00h**
Revision ID							
PCICFG 09h			**Class Code/Revision ID Register (RO) - Byte 1: Bits [15:8]**				**Default = 00h**
Reserved Write bits as read.							
PCICFG 0Ah			**Class Code/Revision ID Register (RO) - Byte 2: Bits [23:16]**				**Default = 01h**

Table 5-2 PCI Base Register Group: PCICFG 00h-3Fh (cont.)

7	6	5	4	3	2	1	0
BCC/SCC - Base Class Code and Sub-Class Code							
PCICFG 0Bh			**Class Code/Revision ID Register (RO) - Byte 3: Bits [31:24]**				**Default = 04h**
BCC/SCC - Base Class Code and Sub-Class Code							
PCICFG 0Ch			**Cache Line Size Register** Not implemented				**Default = 00h**
PCICFG 0Dh			**Latency Timer Register**				**Default = 00h**
LT- Latency Timer					Reserved: Write bits to read		
PCICFG 0Eh			**Header Type Register (RO)**				**Default = 00h**
Multi-function device (RO): 0 = No 1 = Yes	HT - Header type						
PCICFG 0Fh			**BIST Register** Not implemented				**Default = 00h**
PCICFG 10h			**SB-Compatible Base Address - Byte 0: Bits [7:0]**				**Default = 01h**
SBA - SB-Compatible Base Address (RW)				Indicates the requirement of 16 IO spaces			Indicates IO Space Requirement Always = 1
PCICFG 11h			**SB-Compatible Base Address - Byte 1: Bits [15:8]**				**Default = 00h**
SBA - SB-Compatible Base Address (RO)				SBA - SB-Compatible Base Address (RW)			
PCICFG 12h			**SB-Compatible Base Address Byte 2: Bits [23:16]**				**Default = 00h**
SBA - SB-Compatible Base Address (RO)							
PCICFG 13h			**SB-Compatible Base Address Byte 3: Bits [31:24]**				**Default = 00h**
SBA - SB-Compatible Base Address (RO)							
PCICFG 14h			**WSS-Compatible Base Address - Byte 0: Bits [7:0]**				**Default = 01h**
WSSA - WSS-Compatible Base Address (RW)					Indicates the requirement of 8 IO spaces		Indicates IO Space Requirement Always = 1
PCICFG 15h			**WSS-Compatible Base Address - Byte 1: Bits [15:8]**				**Default = 00h**
WSSA - WSS-Compatible Base Address (RO)				WSSA - WSS-Compatible Base Address (RW)			
PCICFG 16h			**WSS-Compatible Base Address Byte 2: Bits [23:16]**				**Default = 00h**
WSSA - WSS-Compatible Base Address (RO)							
PCICFG 17h			**WSS-Compatible Base Address Byte 3: Bits [31:24]**				**Default = 00h**
WSSA - WSS-Compatible Base Address (RO)							
PCICFG 18h			**FM Synthesis Base Address - Byte 0: Bits [7:0]**				**Default = 01h**

Table 5-2 PCI Base Register Group: PCICFG 00h-3Fh (cont.)

7	6	5	4	3	2	1	0
FMA - FM Synthesis Base Address (RW)						Indicates the requirement of 4 IO spaces	Indicates IO Space Requirement Always = 1
PCICFG 19h			**FM Synthesis Base Address - Byte 1: Bits [15:8]**				**Default = 00h**
FMA - FM Synthesis Base Address (RO)				FMA - FM Synthesis Base Address (RW)			
PCICFG 1Ah			**FM Synthesis Base Address Byte 2: Bits [23:16]**				**Default = 00h**
FMA - FM Synthesis Base Address (RO)							
PCICFG 1Bh			**FM Synthesis Base Address Byte 3: Bits [31:24]**				**Default = 00h**
FMA - FM Synthesis Base Address (RO)							
PCICFG 1Ch			**MIDI Base Address - Byte 0: Bits [7:0]**				**Default = 01h**
MIDIA - MIDI Base Address (RW)						Indicates the requirement of 4 IO spaces	Indicates IO Space Requirement Always = 1
PCICFG 1Dh			**MIDI Base Address - Byte 1: Bits [15:8]**				**Default = 00h**
MIDIA - MIDI Base Address (RO)				MIDIA - MIDI Base Address (RW)			
PCICFG 1Eh			**MIDI Base Address Byte 2: Bits [23:16]**				**Default = 00h**
MIDIA - MIDI Base Address (RO)							
PCICFG 1Fh			**MIDI Base Address Byte 3: Bits [31:24]**				**Default = 00h**
MIDIA - MIDI Base Address (RO)							
PCICFG 20h			**Game Port Compatible Base Address - Byte 0: Bits [7:0]**				**Default = 01h**
GPA - Game Port Compatible Base Address (RW)				Indicates the requirement of 8 IO spaces			Indicates IO Space Requirement Always = 1
PCICFG 21h			**Game Port Compatible Base Address - Byte 1: Bits [15:8]**				**Default = 00h**
GPA - Game Port Compatible Base Address (RO)				GPA - Game Port Compatible Base Address (RW)			
PCICFG 22h			**Game Port Compatible Base Address Byte 2: Bits [23:16]**				**Default = 00h**
GPA - Game Port Compatible Base Address (RO)							
PCICFG 23h			**Game Port Compatible Base Address Byte 3: Bits [31:24]**				**Default = 00h**
GPA - Game Port Compatible Base Address (RO)							
PCICFG 24h			**MC Base Address - Byte 0: Bits [7:0]**				**Default = 01h**
MCA - MC Base Address (RW)						Indicates the requirement of 4 IO spaces	Indicates IO Space Requirement Always = 1
PCICFG 25h			**MC Base Address - Byte 1: Bits [15:8]**				**Default = 00h**
MCA - MC Base Address (RO)				MCA - MC Base Address (RW)			
PCICFG 26h			**MC Base Address Byte 2: Bits [23:16]**				**Default = 00h**
MCA - MC Base Address (RO)							

Table 5-2 PCI Base Register Group: PCICFG 00h-3Fh (cont.)

7	6	5	4	3	2	1	0
PCICFG 27h			**MC Base Address Byte 3: Bits [31:24]**				**Default = 00h**
GPA - Game Port Compatible Base Address (RO)							
PCICFG 28h-2Bh			**Reserved**				**Default = 00h**
PCICFG 2Ch			**Subsystem Vendor Register (RO) - Byte 0: Bits [7:0]**				**Default = 00h**
Subsystem Vendor Bits: - The information must be stored in the external EEPROM (if available) or in the BIOS for motherboard implementations. The BIOS is responsible for writing the subvendor ID information to PCICFG[3Ch] during initialization.							
PCICFG 2Dh			**Subsystem Vendor Register (RO) - Byte 1: Bits [15:8]**				**Default = 00h**
PCICFG 2Eh			**Subsystem ID Register (RO) - Byte 0: Bits [7:0]**				**Default = 00h**
PCICFG 2Fh			**Subsystem ID Register (RO) - Byte 1: Bits [15:8]**				**Default = 00h**
PCICFG 30h-33h			**Reserved**				**Default = 00h**
PCICFG 34h			**Capability Pointer (RO)**				**Default = DCh**
Pointer to a linked list of additional Capabilities List.							
PCICFG 35h-3Bh			**Reserved**				**Default = 00h**
PCICFG 3Ch			**Interrupt Line Register**				**Default = FFh**
Power-On-Self Test (POST) software will write the routing information into this register.							
PCICFG 3Dh			**Interrupt Pin Register**				**Default = 01h**
Default indicates INTA pin is used.							
PCICFG 3Eh			**Minimum Grant Register (RO)**				**Default = 00h**
Specifies the maximum potential length of burst sequences, in units of 250ns. Default indicates no major requirement.							
PCICFG 3Fh			**Maximum Latency Register (RO)**				**Default = 00h**
Specifies the maximum latency, in units of 250ns. Default indicates no major requirement.							

Table 5-3 PCI Extended Mode Register Group: PCICFG 40h-FFh

7	6	5	4	3	2	1	0
PCICFG 40h			**Power Control Latch Register 1 (WO)**				**Default = xxh**
Pin setting: 0 = Low 1 = High	Reserved			PWRx pin to set or clear PPWR0-PPWR15: - PPWR1-4 may be used as RSTDRV1-4 - PPWR0-7 default to high at reset - PPWR8-15 default to low at reset			
PCICFG 41h			**Power Control Latch Register 2**				**Default = xxh**
Reserved							
PCICFG 42h			**Power Control Latch Register 3 (RO)**				**Default = xxh**
PPWR7 writes: 0 = Disable 1 = Enable	PPWR6 value: 0 = Low 1 = High	PPWR5 value: 0 = Low 1 = High	PPWR4 value: 0 = Low 1 = High	PPWR3 value: 0 = Low 1 = High	PPWR2 value: 0 = Low 1 = High	PPWR1 value: 0 = Low 1 = High	PPWR0 value: 0 = Low 1 = High
PCICFG 43h			**Power Control Latch Register 4 (RO)**				**Default = xxh**
PPWR15 value: 0 = Low 1 = High	PPWR14 value: 0 = Low 1 = High	PPWR13 value: 0 = Low 1 = High	PPWR12 value: 0 = Low 1 = High	PPWR11 value: 0 = Low 1 = High	PPWR10 value: 0 = Low 1 = High	PPWR9 value: 0 = Low 1 = High	PPWR8 value: 0 = Low 1 = High
PCICFG 44h			**DMA Channel Selector Register 1**				**Default = 98h**
Channel 1: 0 = Not claimed 1 = On docking ISA	DRQ1/DACK1# pin: 000 = Channel 0 001 = Channel 1 (Default) 010 = Channel 2 011 = Channel 3		100 = Reserved 101 = Channel 5 110 = Channel 6 111 = Channel 7	Channel 0: 0 = Not claimed 1 = On docking ISA	DRQ0/DACK0# pin: 000 = Channel 0 (Default) 001 = Channel 1 010 = Channel 2 011 = Channel 3		100 = Reserved 101 = Channel 5 110 = Channel 6 111 = Channel 7
PCICFG 45h			**DMA Channel Selector Register 2**				**Default = BAh**
Channel 3: 0 = Not claimed 1 = On docking ISA	DRQ3/DACK3# pin: 000 = Channel 0 001 = Channel 1 010 = Channel 2 011 = Channel 3 (Default)		100 = Reserved 101 = Channel 5 110 = Channel 6 111 = Channel 7	Channel 2: 0 = Not claimed 1 = On docking ISA	DRQ2/DACK2# pin: 000 = Channel 0 001 = Channel 1 010 = Channel 2 (Default) 011 = Channel 3		100 = Reserved 101 = Channel 5 110 = Channel 6 111 = Channel 7
PCICFG 46h			**DMA Channel Selector Register 3**				**Default = EDh**
Channel 6: 0 = Not claimed 1 = On docking ISA	DRQ6/DACK6# pin: 000 = Channel 0 001 = Channel 1 010 = Channel 2 011 = Channel 3		100 = Reserved 101 = Channel 5 110 = Channel 6 (Default) 111 = Channel 7	Channel 5: 0 = Not claimed 1 = On docking ISA	DRQ5/DACK5# pin: 000 = Channel 0 001 = Channel 1 010 = Channel 2 011 = Channel 3		100 = Reserved 101 = Channel 5 (Default) 110 = Channel 6 111 = Channel 7
PCICFG 47h			**DMA Channel Selector Register 4**				**Default = 0Fh**
Reserved				Channel 7: 0 = Not claimed 1 = On docking ISA	DRQ7/DACK7# pin: 000 = Channel 0 001 = Channel 1 010 = Channel 2 011 = Channel 3		100 = Reserved 101 = Channel 5 110 = Channel 6 111 = Channel 7 (Default)

Table 5-3 PCI Extended Mode Register Group: PCICFG 40h-FFh (cont.)

7	6	5	4	3	2	1	0
PCICFG 48h			**IRQ Channel Selector Register 1**				**Default = 43h**
IRQ4 pin (Default = IRQ4):				IRQ3 pin (Default = IRQ3):			
0000 = IRQ0	0100 = IRQ4	1000 = IRQ8#	1100 = IRQ12	0000 = IRQ0	0100 = IRQ4	1000 = IRQ8#	1100 = IRQ12
0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = NMI	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = NMI
0010 = SMI#	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14	0010 = SMI#	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
PCICFG 49h			**IRQ Channel Selector Register 2**				**Default = 65h**
IRQ6 pin (Default = IRQ6):				IRQ5 pin (Default = IRQ5):			
0000 = IRQ0	0100 = IRQ4	1000 = IRQ8#	1100 = IRQ12	0000 = IRQ0	0100 = IRQ4	1000 = IRQ8#	1100 = IRQ12
0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = NMI	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = NMI
0010 = SMI#	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14	0010 = SMI#	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
PCICFG 4Ah			**IRQ Channel Selector Register 3**				**Default = 97h**
IRQ9 pin (Default = IRQ9):				IRQ7 pin (Default = IRQ7):			
0000 = IRQ0	0100 = IRQ4	1000 = IRQ8#	1100 = IRQ12	0000 = IRQ0	0100 = IRQ4	1000 = IRQ8#	1100 = IRQ12
0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = NMI	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = NMI
0010 = SMI#	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14	0010 = SMI#	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
PCICFG 4Bh			**IRQ Channel Selector Register 4**				**Default = BAh**
IRQ11 pin (Default = IRQ11):				IRQ10 pin (Default = IRQ10):			
0000 = IRQ0	0100 = IRQ4	1000 = IRQ8#	1100 = IRQ12	0000 = IRQ0	0100 = IRQ4	1000 = IRQ8#	1100 = IRQ12
0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = NMI	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = NMI
0010 = SMI#	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14	0010 = SMI#	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
PCICFG 4Ch			**IRQ Channel Selector Register 5**				**Default = ECh**
IRQ14 pin (Default = IRQ14):				IRQ12 pin (Default = IRQ12):			
0000 = IRQ0	0100 = IRQ4	1000 = IRQ8#	1100 = IRQ12	0000 = IRQ0	0100 = IRQ4	1000 = IRQ8#	1100 = IRQ12
0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = NMI	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = NMI
0010 = SMI#	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14	0010 = SMI#	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
PCICFG 4Dh			**IRQ Channel Selector Register 6**				**Default = DFh**
HDI pin (Default = NMI):				IRQ15 pin (Default = IRQ15):			
0000 = IRQ0	0100 = IRQ4	1000 = IRQ8#	1100 = IRQ12	0000 = IRQ0	0100 = IRQ4	1000 = IRQ8#	1100 = IRQ12
0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = NMI	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = NMI
0010 = SMI#	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14	0010 = SMI#	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
PCICFG 4Eh-4Fh			**Reserved**				**Default = 00h**

Table 5-3 PCI Extended Mode Register Group: PCICFG 40h-FFh (cont.)

7	6	5	4	3	2	1	0
PCICFG 50h			**Hot Docking Control Register**				**Default = xxh**
Reserved	HDI# pin has made low-to-high transition? 0 = No 1 = Yes Write 1 to clear	HDI# pin has made high-to-low transition? 0 = No 1 = Yes Write 1 to clear	Hot insertion attempt failed? 0 = No 1 = Yes Write 1 to clear	Hot IDE insertion failure determination: Selects number of stabilization checks to be performed before hot insertion success is determined. 00 = No retry attempts 01 = 16 attempts 10 = 256 attempts 11 = 1024 attempts		HDI# input stabilization check: Selects duration of sample period during which HDI# must remain stable to be considered a successful check. 00 = 1ms 01 = 10ms 10 = 100ms 11 = 1s	
PCICFG 51h			**ISA Control Register**				**Default = 00h**
Reserved		ISA refresh: 0 = Disable 1 = Enable	PCI SERR# generates NMI? 0 = No 1 = Yes	Reserved	ISA CHCK# NMI: 0 = Disable 1 = Enable	ATCLK source: 00 = 14MHz/2 (Default) 01 = PCICLK/3 10 = PCICLK/4 11 = PCICLK/5	
PCICFG 52h			**Feature Control Register**				**Default = 21h**
PPWRL function on RSTDRV: 0 = Disable (use pin only as RSTDRV) 1 = Enable PPWRL	Individual AEN interface: 0 = Disable 1 = Enable (DACK-MUX strap option required)	IDE controller interface: 0 = Disable (PCIIDE function will not respond) 1 = Enable (Default)	IDE control pin function select: 0 = DRD#, DWR# 1 = DBE0#, DBE1#	CHCK# pin active halts ISA bus: 0 = No (normal CHCK#) 1 = Yes (HDI# function)	Flash EEPROM writes: 0 = Disable (SMWR# is blocked also) 1 = Enable	IRQ8# active level: 0 = Low 1 = High	DMA register access: 0 = ISA mapping 1 = Distributed DMA mapping (Default)
PCICFG 53h			**SMI Status Register**				**Default = 00h**
ROMCS# pin status during reset: 0 = Low 1 = High	DRD# pin status during reset: 0 = Low 1 = High	DWR# pin status during reset: 0 = Low 1 = High	Reserved			PPWR cycle status: 0 = Complete 1 = Pending	IRQ pin generated SMI? 0 = No 1 = Yes Write 1 to clear
PCICFG 54h			**IRQ Driveback Protocol Address Register - Byte 0: Address Bits [7:0]**				**Default = 33h**
IRQ Driveback Protocol Address: - When the 82C935 logic must generate an interrupt from any source, it follows the IRQ Driveback Protocol and toggles the REQ# line to the host. Once it has the bus, it writes the changed IRQ information to the 32-bit I/O address specified in this register. The host interrupt controller claims this cycle and latches the new IRQ values. - This register defaults to a value of 0h, which disables the IRQ driveback scheme.							
PCICFG 55h			**IRQ Driveback Protocol Address Register - Byte 1: Address Bits [15:8]**				**Default = 33h**
PCICFG 56h			**IRQ Driveback Protocol Address Register - Byte 2: Address Bits [23:16]**				**Default = 33h**
PCICFG 57h			**IRQ Driveback Protocol Address Register - Byte 3: Address Bits [31:24]**				**Default = 33h**

Table 5-3 PCI Extended Mode Register Group: PCICFG 40h-FFh (cont.)

7	6	5	4	3	2	1	0
PCICFG 58h			**DRQ Remap Base Address Register - Byte 0: Address Bits [7:0]**				**Default = 00h**
IRQ Remap Base Address: - The distributed DMA protocol requires DMA controller registers for each DMA channel to be individually mapped into I/O space outside the range claimed by ISA devices. Bits A[31:0] of this register specify that base. The 82C935 logic uses this base address to claim accesses to an ISA DMA controller channel.							
PCICFG 59h			**DRQ Remap Base Address Register - Byte 1: Address Bits [15:8]**				**Default = 00h**
PCICFG 5Ah			**DRQ Remap Base Address Register - Byte 2: Address Bits [23:16]**				**Default = 00h**
PCICFG 5Bh			**DRQ Remap Base Address Register - Byte 3: Address Bits [31:24]**				**Default = 00h**
PCICFG 5Ch			**ISA Slot Control Register 1**				**Default = 00h**
AEN2 high for x000-x3F8h: 0 = No 1 = Yes	AEN2 enabled (low) for I/O range: 000 = 0000-FFFFh (normal AEN) 001 = 1000-1FFFh 010 = 2000-2FFFh 011 = 3000-3FFFh 100 = 4000-4FFFh 101 = 5000-5FFFh 110 = 6000-6FFFh 111 = 7000-7FFFh			AEN1 high for x000-x3F8h: 0 = No 1 = Yes	AEN1 enabled (low) for I/O range: 000 = 0000-FFFFh (normal AEN) 001 = 1000-1FFFh 010 = 2000-2FFFh 011 = 3000-3FFFh 100 = 4000-4FFFh 101 = 5000-5FFFh 110 = 6000-6FFFh 111 = 7000-7FFFh		
PCICFG 5Dh			**ISA Slot Control Register 2**				**Default = 00h**
Reserved				AEN3 high for x000-x3F8h: 0 = No 1 = Yes	AEN3 enabled (low) for I/O range: 000 = 0000-FFFFh (normal AEN) 001 = 1000-1FFFh 010 = 2000-2FFFh 011 = 3000-3FFFh 100 = 4000-4FFFh 101 = 5000-5FFFh 110 = 6000-6FFFh 111 = 7000-7FFFh		
PCICFG 5Eh			**Write Posting Control Register**				**Default = 00h**
Reserved: Write as read.				Reserved	Retry Attempts on Posted Writes: These bits relate to the number of retries allowed to deliver posted data before SERR# is generated on the initiator side. 000 = 2^8 101 = 2^{20} 001 = 2^{10} 100 = 2^{16} 010 = 2^{12} 110 = 2^{24} 011 = 2^{14} 111 = Infinite retries		
PCICFG 5Fh			**Write Posting Status Register (RO)**				**Default = 00h**
This register returns the number of retry attempts made to write posted data to the target. More than 256 retries are indicated by FFh. Used for diagnostic purposes.							

Table 5-3 PCI Extended Mode Register Group: PCICFG 40h-FFh (cont.)

7	6	5	4	3	2	1	0
PCICFG 60h			**DMA Feature Control Byte - Byte 0: [7:0]**				**Default = 40h**
DMA IOR Cycle Claiming 0 = Disable 1 = Enable	DMA IOW cycle snooping 0 = Disable 1 = Enable	TC Self-Clear 0 = Disable 1 = Enable	TC Update Selection 0 = By address 1 = By status bit	Host DMAC address update 0 = Disable 1 = Enable	VDMA Enable 0 = Disable 1 = Enable	Update Frequency: Define how often DMAC is updated 00 = every 8 DACK# rising 01 = every 4 DACK# rising 10 = every 2 DACK# rising 11 = every 1 DACK# rising	
PCICFG 61h			**DMA Feature Control Byte - Byte 1: [15:8]**				**Default = 04h**
PCI PnP Register Select	General Purpose Chip Select	Reserved			DMA Buffer Enable	Timer IOW snooping 0 = Disable 1 = Enable	PnP IOW snooping 0 = Disable 1 = Enable
PCICFG 62h			**SIRQ Control (R/W)**				**Default = 00h**
DMA Arbiter Enable	PC Speaker Emulation: 0 = Disable 1 = Enable	DMA Control Register Priority			Reserved		SIRQ Enable (Compaq version) 0 = Disable 1 = Enable
PCICFG 63h			**Reserved**				**Default = 00h**
PCICFG 64h-DDh			**Reserved**				**Default = 00h**
PCICFG DEh			**Power Management Capabilities - Byte 0: Bits [7:0] (RO)**				**Default = 00h**
Reserved		DynClk - This field is used by a bridge to inform the system of its clock generation capabilities. 00 = Not a bridge		Battery 0 = No battery support	Version 01 = 4 bytes of general purpose Power Management Registers		
PCICFG DFh			**Power Management Capabilities - Byte 1: Bits [15:8] (RO)**				**Default = C0h**
StatChg - This two bit field indicates the lowest power state from which the device is able to indicate a power status change interrupt event. 00 = No change events 01 = Reserved 10 = StatChg events possible from any supported state except 3D 11 = StatChg event possible from any supported state		Wave_St - Indicates the lowest power state from which the device is able to indicate a wake up event 00 = No wake up events 01 = From D1 10 = From D1 and D2 11 = From D1, D2 and D3		Reserved	D2 State 1 = Supported	D1 State 1 = Supported	FullClk 1 = This function requires a full speed clock at all times when in D0 state.

Table 5-3 PCI Extended Mode Register Group: PCICFG 40h-FFh (cont.)

7	6	5	4	3	2	1	0
PCICFG E0h			**Power Management Control Status - Byte 0: Bits [7:0]**				**Default = 00h**
Reserved	CynClk_En 0 = Non-bridge function	Int_Mask 2 = Mask the function's standard interrupt	StatChg_En 1 = Power Status Change Enable	Wake_En 1 = Wake Up Condition Enable	DeviceRdy 1 = Function is in transition to new power state	PowerState - This field is used to determine the current power state and to set the function into a new power state 00 = D0 01 = D1 10 = D2 11 = D3	
PCICFG E1h			**Power Management Control Status - Byte 1: Bits [15:8]**				**Default = 00h**
Reserved		Func_Int Indicates the current state of the function's standard interrupt. (RO)	StatChg_Int Indicate a status change interrupt. Independent of the state of StatChg_En bit. Writing a 1 will clear it and cause the function to stop asserting a status change interrupt. Writing a 0 has not effect.	Wake_Int Indicates a wake up interrupt. Independent of the state of Wake_En bit. Writing a 1 will clear it and cause the function to stop asserting a wakeup interrupt.	Reserved		
PCICFG E2h			**Reserved**				**Default = 00h**
PCICFG E3h			**Reserved**				**Default = 00h**
PCICFG E4h-FFh			**Reserved**				**Default = 00h**

5.2 Legacy Register

5.2.1 MCBase Register

MCBase is set by register PCICFG 24h. MCIndirect and MCData registers are shown in the following tables.

Table 5-4 MCIdx and MCData Registers

7	6	5	4	3	2	1	0
MCIdx							
0	0	0	Specifies which MCIR register is to be accessed. 00000 = Disable 00001 = MCIR1:Base/Type Configuration 00010 = MCIR2: Reserved 00011 = MCIR3: SB/WSS Configuration 00100 = MCIR4: User Programmable GP 00101 = MCIR5: Option 00110 = MCIR6: MIDI Interface 00111 = MCIR7: Semaphore Software 01000 = MCIR8: Reserved 01001 = MCIR9: Test Control 01010 = MCIR10: Test Control 01011 = MCIR11: Status 01100 = MCIR12: Test		01101 = MCIR13: PNP Status 01110 = MCIR14: PNP CSN 01111 = MCIR15: PNP READ_DATA 10000 = MCIR16: Volume Control 10001 = MCIR17: Serial EEPROM 10010 = MCIR18: CONFIG Status 10011 = MCIR19: FM Control 10100 = MCIR20: GPIO Control 10101 = MCIR21: Serial Audio Control 10110 = MCIR22: Serial Audio Control 10111 = MCIR23: Reserved Remaining combinations = Reserved		
MCData (refer to Table 5-5)							

Table 5-5 MC Indirect Registers

7	6	5	4	3	2	1	0
MCIR1			**Base/Type Configuration Register**				**Default = 06h**
Sound Blaster I/O base address (SBBase): 0 = 220 1 = 240	Reserved	Windows Sound System I/O base address (WSBase): 00 = 530 10 = F40 01 = E80 11 = 640		CD-ROM interface: The sense of these bits is reversed during writes. To disable CD, write b'011'. 000 = Disabled 100 = Secondary IDE All others = Reserved			Game port: 0 = Disable 1 = Enable
MCIR2			**BAUD 96 register**				**Default = 00h**
Reserved Set to 0.				BAUD96: This bit could be used by PDA devices to communicate with other devices 0 = Disabled, normal MIDI UART in RXD pin. 1 = Enabled, 9600 baud rate UART in RXD pin	Reserved Set to 0.		

Table 5-5 MC Indirect Registers (cont.)

7	6	5	4	3	2	1	0
MCIR3		**Sound Blaster/Windows Sound System Configuration Register**					**Default = 00h**
Reserved: Must be set to 0.	Reserved: Must be set to 0 for normal operation in WSS.	DAP IRQ select: 000 = Disable 001 = IRQ7 010 = IRQ9 011 = IRQ10 100 = IRQ11 101 = IRQ5 110 = Reserved 111 = Reserved			DAP DMA select: 000 = Disabled 001 = DRQ0 010 = DRQ1 011 = DRQ3 100 = Disable 101 = DRQ0 110 = DRQ1 111 = DRQ3 DRQ1(1) DRQ1(1) DRQ0(1) DRQ0(1)		
(1) If CIR9[2] = 0 (Codec Indirect Register 9, bit 2), then DAP DMA[4:7] can be selected							
MCIR4		**User Programmable General Purpose Register**					**Default = 10h**
Playback FIFO flow control: 00 = Empty 01 = Full-2 10 = Full-4 11 = Not full		OPL select: 00 = OPL2 01 = OPL3 10 = OPL4 11 = OPL5		Digital-Analog controller zero: 0 = Hold 1 = Clear	Audio:(1) 0 = Disable 1 = Enable	Sound Blaster version: 00 = 2.1 01 = 1.5 10 = 3.2 11 = 4.4	
(1) Bit 2 can also accessed through the MC register or through PNP logic.							
MCIR5			**Option Register**				**Default = 00h**
Reserved		Codec Expanded Mode:(1) 0 = Disable 1 = Enable	Sound Blaster ADPCM: 0 = Disable 1 = Enable	Command FIFO in Sound Blaster mode: 0 = Disable 1 = Enable	Volume effect for Sound Blaster Pro mixer voice volume emulation: 0 = Disable 1 = Enable	DMA watch dog timer: 0 = Disable 1 = Enable When enabled, the 82C935 will generate internal DACK after the DRQ pending time-up.	Reserved
(1) Bit 5 must be set in order to access the CIR16-31, the Expanded Mode of the Codec Indirect Registers. Refer to Table 5-9 and Table 5-11.							
MCIR6			**MIDI Interface Register (WO)**				**Default = 00h**
MPU-401: 0 = Disable 1 = Enable	MPU-401 base address select: 00 = 330 01 = 320 10 = 310 11 = 300		MPU-401 interrupt select: 00 = IRQ9 01 = IRQ10 10 = IRQ5 11 = IRQ7		Reserved	Windows sound system mode: 0 = Disable 1 = Enable	Sound Blaster mode: 0 = Disable 1 = Enable
MCIR7			**Semaphore Software Register (Software use only)**				**Default = 00h**
D7	D6	D5	D4	D3	D2	D1	D0
MCIR8			**Reserved Register**				**Default = 00h**
MCIR9			**Test Control Register**				**Default = 00h**
Digital power-down: 0 = Normal 1 = Power-down	Analog power-down: 0 = Normal 1 = Power-down	Reserved				Software reset: 0 = Disable 1 = Enable	

Table 5-5 MC Indirect Registers (cont.)

7	6	5	4	3	2	1	0
MCIR10			**Test Control Register**				**Default = 00h**
Playback reset: 0 = Normal 1 = Reset (playback data path clear, active high)	Capture reset: 0 = Normal 1 = Reset (capture data path clear, active high)	PNP test mode: 0 = Normal 1 = Test (PNP logic is set to Sleep mode)	Reserved				
MCIR11			**Status Register (RO)**				**Default = 00h**
Playback DMA pending? 0 = No 1 = Yes	Capture DMA pending? 0 = No 1 = Yes	MPU interrupt pending? 0 = No 1 = Yes	CD interrupt pending? 0 = No 1 = Yes	Capture interrupt pending? 0 = No 1 = Yes	Playback interrupt pending? 0 = No 1 = Yes	Playback FIFO empty? 0 = No 1 = Yes	Capture FIFO empty? 0 = No 1 = Yes
MCIR12			**Test Register**				**Default = 00h**
Reserved			Digital test mode output high/low byte select (WO)	Digital test mode output select (WO)			
MCIR13			**PNP Status Register (RO)**				**Default = 01h**
CSN not zero - active high: 1 = PNP configuration manager assigned a CSN to 82C935.(1)	Modem interface logical device: 0 = Disable 1 = Enable	IDE logic device: 0 = Disable 1 = Enable	MC logical device: 0 = Disable 1 = Enable	CONFIG mode: 1 = 82C935's PNP logic is in the CONFIG mode	ISOLATE mode: 1 = 82C935's PNP logic is in the ISOLATE mode	SLEEP mode: 1 = 82C935's PNP logic is in the SLEEP mode	WAIT4KEY mode: 1 = 82C935's PNP logic is in the WAIT4KEY mode
(1) When a CSN is assigned to the 82C935, it switches to the PNP mode and the resource configuration is controlled through the PNP registers.							
MCIR14			**PNP CSN Register (RO)**				**Default = 00h**
PNP card select number: This registers shows the CSN assigned to the 82C935 by the PNP configuration manager.							
MCIR15			**PNP Read Port Address Register (RO)**				**Default = 00h**
PNP READ_DATA port: This registers shows the READ_DATA port assigned by the PNP configuration manager.							
MCIR16			**Volume Control Register**				**Default = 00h**
Reserved	Push-button volume control interrupt enable	UP button is pushed? 0 = No 1 = Yes This bit is cleared after a read.	DOWN button is pushed? 0 = No 1 = Yes This bit is cleared after a read.	Master volume mute control (active high)	Push-button volume control interrupt status (RO) This bit is cleared after a read.	Volume control interrupt select: 00 = Disable 01 = IRQ5 10 = IRQ10 11 = IRQ11	

Table 5-5 MC Indirect Registers (cont.)

7	6	5	4	3	2	1	0
MCIR17			**Serial EEPROM Control Register**				**Default = 00h**
Write to external serial EEPROM: 0 = Disable 1 = Enable	External serial EEPROM chip select: 0 = Disable 1 = Enable	External serial EEPROM clock: 0 = Disable 1 = Enable	External serial EEPROM data out: 0 = Disable 1 = Enable Connected to DIN of external EEPROM	External serial EEPROM data out: 0 = Disable 1 = Enable Connected to DIN of external EEPROM	External serial EEPROM capability (R/W) When read for status: 0 = Disable 1 = Enable When write to change: 0 = Enable 1 = Disable Note: read polarity is the opposite of write's.	PNP setting (R/W): **Read:** 0 = enabled 1 = disabled **Write:** 0 = disabled 1 = enabled Note: The polarity of the read is the opposite of the write.	Reserved
MCIR18			**CONFIG Status Register**				**Default = 09h**
Reserved	ASIO function: 0 = Disable 1 = Enable	Reserved 0 = Default	Reserved Always = 0	Chip revision ID (RO) = 0x9			
MCIR19			**FM Control Register**				**Default = xxh**
Reserved	Reserved	Reserved	Reserved		MEGA bass: 0 = Disable 1 = Enable	OPTi mode for enhanced FM features: 0 = Disable 1 = Enable	External FM select: 0 = Disable 1 = Enable
MCIR20			**GPIO Control Register 0**				**Default = 00h**
GPIO3 Output Values at Pin 103	GPIO3 pin type: 0 = Input 1 = Output	GPIO2 Output Values at Pin 102	GPIO2 pin type: 0 = Input 1 = Output	GPIO1 Output Values at Pin 12	GPIO1 pin type: 0 = Input 1 = Output	GPIO3 Output Values at Pin 11	GPIO0 pin type: 0 = Input 1 = Output
Note: GPIO function is available only when the specified pin is not being used for another function.							
MCIR21			**Serial Audio Control Register 0**				**Default = 00h**
CTL_SEL[1:0] ASIO shift clock selection 00/11 = Use the shift clock from internal FS 01 = Use FM timing 10 = Use external SCLK		P2S_SEL[1:0] SAO data source selection 00/11 = From DMA Playback 01 = From FM 10 = From ADC, captured from analog section		SPCDSEL Enables dual playback 0 = 2nd DMA channel is used for DMA capture 1 = 2nd DMA is used with 1st DMA channel for DMA playback	ADCSEL Selects DMA data capture source 0 = ADC data (from analog section) 1 = SAI data	FDACSEL Selects FDAC data source 0 = FDAC takes FM data 1 = FDAC takes SADI (if SPCDSEL=0), 2nd DMA playback data (if SPCDSEL=1)	DACSEL Selects DAC data source 0 = DMA playback 1 = SAI

Table 5-5 MC Indirect Registers (cont.)

7	6	5	4	3	2	1	0
MCIR22			**Serial Audio Control Register 1**				**Default = 00h**
Reset ASIO: 0 = Normal 1 = Reset	ASIO test mode: 0 = Normal 1 = Test	F16 Specify ASIO sample period data location: 0 = Last 16 bits of the L/R half sample period 1 = First 16/17 bits of L/R half sample period	CLK32 Number of SCLKs in a sample period (delay-mode or pulse-mode ASIO only) 0 = 32 1 = >32	SCLK polarity: 0 = Reverse 1 = No changed	FSYNC polarity: 0 = Reverse 1 = No changed	PULSE Pulse mode type of serial data (AT&T7525 comp or CS8412 DSP) 0 = Not activated 1 = Activated	
MCIR23			**Serial Audio Clock/Output Control Register**				**Default = 00h**
ASDOOE ADO direction control 0 = Input 1 = Output	SCLKOE SCLK direction control 0 = Input 1 = Output	FSYNCOE FSYNC direction control 0 = Input 1 = Output	MCLKEN External MCLK enable (fed through ASDO) 0 = Disabled 1 = Enabled	MCLKSEL[1:0] Master clock divider selection 00 = asdo_clk/8 01 = asdo_clk/4 10 = asdo_clk/2 11 = asdo_clk/1		CLKSEL[1:0] Selects shift clock for serial audio data output (sclk_out) 00 = mclk/8 01 = mclk/4 10 = mclk/2 11 = mclk/1	
MCIR24			**Game Port Counter Setup and Status Register**				**Default = 00h**
JRDY/Game Port IRQ Readback of '1' indicates the game port counters are stopped and the interrupt is generated. The IRQ is cleared by writing a '1' to this location.	SOUNDIRQ Shows the status of the audio IRQ, a '1' indicates there is a sound IRQ	GPIRQEN IRQ generation when the game port counter is finish counting 0 = Disabled 1 = Enabled	GPWPEN Auto game port trigger (20x write) 0 = Disabled 1 = Enabled	ACTBY By axis counter enable 0 = Disabled 1 = Enabled	ACTBX Bx axis counter enable 0 = Disabled 1 = Enabled	ACTAY Ay axis counter enable 0 = Disabled 1 = Enabled	ACTAX Ax axis counter enable 0 = Disabled 1 = Enabled
MCIR25			**Game Port Counter Values Register**				**Default = xxh**
GPCOUNT[7:0] Hardware counter values in H-byte L-byte fashion (16-bit). The sequence will be: Joystick A-X axis Joystick A-Y axis Joystick B-X axis Joystick B-Y axis The count value will be changed automatically upon each read of this register. If that particular joystick axis is masked (disabled), the count will skip accordingly.							

Table 5-5 MC Indirect Registers (cont.)

7	6	5	4	3	2	1	0
MCIR26			**FDAC Data Control Register**				**Default = 00h**
JPTSTEN Game port counter test mode, counter toggled by 14.318MHz (default=1MHz) 0 = Disabled 1 = Enabled	Reserved	VCPIN Special volume control pins move the pins to up/down=GD5/4 (normal: up/down = GD7/6 0 = Disabled 1 = Enabled	ASWTST FDAC data auto-switching timer test mode, TxD timer toggled by 14.318MHz (default = 31KHz) 0 = Disabled 1 = Enabled	FDACMUL Multiply FDAC data by 2 0 = Disabled 1 = Enabled	FMMUL Multiply FM data by 2 0 = Disabled 1 = Enabled	FMDIV Divide FM data by 2 0 = Disabled 1 = Enabled	AUTOSW Auto-detect of TxD activity to switch the FDAC data between FM and serial audio (which comes from TxD 0 = Disabled 1 = Enabled
MCIR27-31			**Reserved**				**Default = 00h**

5.2.2 Extended MC Register

Table 5-6 Extended MC Register Group: MCIdx 20h-2Fh

7	6	5	4	3	2	1	0
MCIR32			**AC-LINK Index Register (R/W)**				**Default = 00h**
Always = 0	AC97 Mixer Index Register						
MCIR33			**AC-LINK Data Register (R/W)**				**Default = 00h**
AC97 Mixer Data Register Data toggle between low byte and high byte. Toggle register is reset after a write to MC Index register. Program procedure: 1. Index Write 2. Low Byte Access 3. High Byte Access							
MCIR34			**AC-LINK Control Register (R/W)**				**Default = 00h**
Reserved		Internal Codec Enable 0 = External AC97 Codec 1 = Internal	Internal CD Enable 0 = Internal 1 = Enable ADC output to transfer to external AC97 codec	Match - When set, Mixer Ready will be set only when the received mixer index matches with the AC-LINK register	Mixer Ready (Read Only)	Mixer Read	Mixer Write
MCIR35			**Extended Digital Power Management Register (R/W)**				**Default = 00h**
Reserved			Bus Interface 1 = Enable power down	Digital Audio Processor	Game Port Power Down	MPU401 Power Down	FM Music Synthesis Power Down

Table 5-6 Extended MC Register Group: MCIdx 20h-2Fh (cont.)

7	6	5	4	3	2	1	0
MCIR36			**Extended Analog Power Management Register (R/W)**				**Default = 00h**
Reserved				FS 1 = Enable power down	MIX Power Down	DAC Power Down	ADC Power Down
MCIR37			**Miscellaneous Control Register (R/W)**				**Default = 00h**
Reserved	SCLK2 Output Enable	SDO2 Output Enable	SDI2 Output Enable	SLR2 Output Enable	ASIO2Select 1 = Select 2nd ASIO output	3D Space Control 00 = Bypass 01 = QX1 (MIN.) 10 = QX2 11 = QX3 (MAX.)	
MCIR38			**Functional Interrupt Status Register (RO)**				**Default = 00h**
Reserved		GPI - Game Port Interrupt	TMI - Timer Interrupt	VCI - Volume Control Interrupt	MPU - MPU401 Interrupt	DAPCI - DAP Capture Interrupt	DAPPIDAP - Playback Interrupt
MCIR39			**Timer Register 0 - Byte 0: Bits [7:0] (R/W)**				**Default = FFh**
MCIR40			**Timer Register 1 - Byte 1: Bits [15:8] (R/W)**				**Default = FFh**
MCIR41			**Timer Register 2 (R/W)**				**Default = 0Fh**
Reserved		Timer Interrupt Status Write 0 to clear	Timer Enable	Timer Bits [19:16]			
MCIR42			**Test Probe Register (R/W)**				**Default = 00h**
Test Probe Status							
MCIR43			**Pin Configuration Register (R/W)**				**Default = 02h**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved Must be set to 1	AC-LINK Enable
MCIR44			**AC97 Reset Register (R/W)**				**Default = 02h**
Reserved			Reserved			AC97 Reset 0 = Enabled 1 = Disabled	Reserved
MCIR45-63			**Reserved**				**Default = 00h**

5.2.3 SBBase Register

SBBase is mainly used to access the Digital Audio Processor (DAP) registers, however, as shown in Table 5-7 other types of registers are also accessible through SBBase. The indexing scheme is the same as when accessing MCBase registers (CPU Direct I/O R/W). Note that in Table 5-7, which gives the SBBase register bit formats, some registers may also be accessed through ALBase. However, use only one Base register for accessing.

SBBase is set by PCICFG 10h.

Table 5-7 SBBase Registers for FM and DAP Applications

7	6	5	4	3	2	1	0
SBBase+00h (or ALBase+00h)			**Left FM Status Register (RO)**				
SBBase+00h (or ALBase+00h)			**Left FM Address Port Register (WO)**				
SBBase+01h (or ALBase+01h)			**Left FM Data Port Register (WO)**				
SBBase+02h (or ALBase+02h)			**Right FM Address Port Register (WO)**				
SBBase+03h (or ALBase+03h)			**Right FM Data Port Register (WO)**				
SBBase+04h			**Mixer Address Port Register (WO)**				
SBBase+05h			**Mixer Data Port Register (WO)**				
SBBase+06h			**DAP Reset Register**				
			Don't care				DAP software reset at end of the I/O write command: 0 = Disable 1 = Enable(1)
(1) When bit 0 is enabled, it sets a software reset flag. This software reset is terminated by performing another write at this location with bit 0 = 0. A system reset will reset the software reset flag, thus terminating the software reset							
SBBase+08h			**FM Status Port Register (RO)**				
SBBase+08h			**FM Address Port Register (WO)**				
SBBase+09h			**FM Data Port Register (WO)**				
SBBase+0Ah			**DAP Read Data Register (RO)**				
SBBase+0Ch			**DAP Data/Command Register (WO)**				
SBBase+0Ch			**DAP Write Buffer Status Register (RO)**				
DAP Input buffer full:(1) 0 = Empty 1 = Full	SBBase+A[6:0]						
(1) This flag is set when the host CPU writes data in the input data bus buffer and cleared when the data is read by the internal DAP.							

Table 5-7 SBBase Registers for FM and DAP Applications (cont.)

7	6	5	4	3	2	1	0
SBBase+0Eh			**DAP Output Buffer Status Register (RO**				
DAP output buffer is full:(1) 0 = Empty 1 = Full	Output Buffer						

(1) This flag is set in the DAP when data is written in the output data bus buffer and cleared when the host CPU or the DMA controller reads the data in the output data bus buffer.

Note: Reading this register will also clear the Digital Audio Processor interrupt request.

5.2.4 WSBase Register

Two types of registers can be accessed through WSBase:

- Windows Sound System (WSS) and Codec registers

These registers are accessed through the WSBase register and use the same type of indexing scheme as MCBase (CPU Direct I/O R/W). The bit formats for WSS-related registers are given in Table 5-8 and Table 5-9 shows the Codec-related registers.

WSBase is set by PCICFG 14h.

Table 5-8 WSBase Registers for Windows Sound System Applications

7	6	5	4	3	2	1	0
WSBase+00h-03h			**WSS Configuration Register (W0)**				**Default = 00h**
Reserved	IRQ sense source: 0 = Normal 1 = auto-interrupt selection	WSS IRQ select: 000 = Disable 001 = IRQ7 010 = IRQ9 011 = IRQ10 100 = IRQ11 101 = IRQ5 110 = Reserved 111 = Reserved			WSS DRQ select: **Playback** / **Capture** 000 = Disable / Disable 001 = DRQ0 / Disable 010 = DRQ1 / Disable 011 = DRQ3 / Disable 100 = Disabled / DRQ1 101 = DRQ0 / DRQ1 110 = DRQ1 / DRQ0 111 = DRQ3 / DRQ0		
WSBase+00h-03h			**WSS Version Register (R0)**				**Default = 00h**
Channel available: 0 = DRQ0/1/3 and IRQ7/9/10/11 available 1 = DRQ1/3 and IRQ7/9 available	IRQ sense: 0 = No interrupt 1 = WSS interrupt active	Version: 04h					

Note that at the Codec Index Address Register (WSBase+04h), bits 4 through 0 are used as the index address for accessing the Codec Indirect Registers (CIR). A write to or a read from the Codec Indexed Data Register (WSBase+05h) will access the Indirect Register which is indexed by the value most recently written to the Codec Index Address Register.

There are 31 Codec Indirect Registers, CIR0-CIR15 are accessed normally. To access CIR16 through CIR31, Expanded Mode registers, MCIR12[5] = 1 (MCBase Indirect

Register, bit 5). Table 5-10 gives the bit formats for CIR0- CIR15 and Table 5-11 shows CIR16-CIR31.

Table 5-9 WSBase Register for Codec/Mixer Applications

7	6	5	4	3	2	1	0
WSBase+04h			**Codec Index Address Register (R/W, exists in Codec and shadowed in 82C935)**				**Default = 00h**
Initialization: This bit is set when the codec is in a state which cannot respond to parallel bus cycles.(1)	Mode change: 0 = Disable 1 = Enable	Transfer request:(2) 0 = Transfers enabled during interrupt 1 = Transfers disabled by interrupt	Index address: These bits specify which Codec Indirect Register (CIR) is to be accessed. Note CIR16 through CIR31 are Expanded Modes and require that MCIR12[5] = 1. (Refer to Table 5-10 and Table 5-11 for these registers bit formats.)				
			00000 = CIR0: MIXOUTL Output Cntrl 00001 = CIR1: MIXOUTR Output Cntrl 00010 = CIR2: CDL Input Cntrl 00011 = CIR3: CDR Input Cntrl 00100 = CIR4: FML Input Cntrl 00101 = CIR5: FMR Input Cntrl 00110 = CIR6: DACL Input Cntrl 00111 = CIR7: DACR Input Cntrl 01000 = CIR8: Fs & Playback Data Format 01001 = CIR9: Interface Configuration 01010 = CIR10: Pin Cntrl 01011 = CIR11: Error Status & Initialization 01100 = CIR12: Mode and ID (Mode 2 Bit) 01101 = CIR13: Reserved 01110 = CIR14: Playback Upper Base 01111 = CIR15: Playback Lower Base	**Expanded Mode Registers** 10000 = CIR16: AUXL Input Cntrl 10001 = CIR17: AUXR Input Cntrl 10010 = CIR18: LINEL Input Cntrl 10011 = CIR19: LINER Input Cntrl 10100 = CIR20: MICL Input Cntrl 10101 = CIR21: MICR Input Cntrl 10110 = CIR22: OUTL Gain Cntrl 10111 = CIR23: OUTR Gain Cntrl 11000 = CIR24: Reserved 11001 = CIR25: Reserved 11010 = CIR26: Reserved 11011 = CIR27: Reserved 11100 = CIR28: Capture Data Format 11101 = CIR29: Reserved 11110 = CIR30: Capture Upper Base 11111 = CIR31: Capture Lower Base		

(1) Immediately after reset and once the codec has left the initialization state, the initial value of this register will be "0100 0000" (40h). During codec initialization, the Codec Index Register cannot be written and is always read 1000 0000 (80h).

(2) When bit 5 is set, DMA transfers cease when bit 0 of the Codec Status Register (WSBase+06h) = 1.

WSBase+05h	**Codec Indexed Data Register (R/W, exists in Codec only)**	**Default = 00h**
	Contains the contents of the Codec register referenced by the Index Data Register. During codec initialization, this register cannot be written and is always read as "1000 0000" (80h).	

7	6	5	4	3	2	1	0
WSBase+06h			**Codec Status Register (R/W, exists in Codec only)**				**Default = 44h**
PIO capture data is ready for upper or lower byte (RO): 0 = Lower 1 = Upper (or any 8-bit mode)	PIO capture data is waiting for right or left channel ADC (RO): 0 = Right 1 = Left (or mono)	PIO Capture Data Register contains data ready for reading by host (RO):(1) 0 = Stale ADC data (do not reread) 1 = Fresh ADC data (ready for next host data read)	Sample over/underrun (RO): Indicates that the most recent sample was not serviced in time; therefore either an overrun for ADC capture or underrun for DAC playback has occurred.(2)	PIO playback data is needed for upper or lower byte (RO): 0 = Lower 1 = Upper (or any 8-bit mode)	PIO playback data is needed for right or left channel DAC (RO): 0 = Right 1 = Left (or mono)	PIO Playback Data Register ready for more data (RO):(1) 0 = Valid DAC data (do not overwrite) 1 = Stale DAC data (ready for next host data write value)	Interrupt: 0 = Disable 1 = Enable

(1) These bits (5 and 1) should only be programmed when direct programmed I/O data transfers are desired.

(2) If both capture and playback are enabled, the source which set bit 4 ca be determined by reading COR and PUR. Bit 4 changes on a sample-by-sample basis.

Note: Bits 5, 1, and 0 can change asynchronously to host accesses. The host may access this register while the bits are transitioning. The host read may return a zero value just as these bits are changing (e.g., a value of 1 would not be read until the next host access). This register's initial state after reset is "1100 1100".

Table 5-9 WSBase Register for Codec/Mixer Applications (cont.)

7	6	5	4	3	2	1	0
WSBase+07h			**Codec Direct Data Register - Capture Mode (RO, exists in Codec only)**				**Default = 00h**
The Codec Direct Data Registers are two registers mapped to the same address. Writes send data to the PIO Playback Data Register (PD7:0). Reads will receive data from the PIO Capture Data Register (CD7:0). During initialization, the PIO Playback Data Register cannot be written and the Capture Data Register is always read "1000 0000" (80h). **PIO Capture Data Register:** This is the control register where capture data is read during programmed I/O data transfers. The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status Register. Once all relevant bytes have been read, the state machine will stay pointed to the last byte of the sample until a new sample is received from the ADCs. Once this has occurred, the state machine and status register will point to the first byte of the sample. Until a new sample is received, reads from this register will return the most significant byte of the sample.							
WSBase+07h			**Codec Direct Data Register - Playback Mode (WO, exists in Codec only)**				**Default = 00h**
The Codec Direct Data Registers are two registers mapped to the same address. Writes send data to the PIO Playback Data Register (PD7:0). Reads will receive data from the PIO Capture Data Register (CD7:0). During initialization, the PIO Playback Data Register cannot be written and the Capture Data Register is always read "1000 0000" (80h). **PIO Playback Data Register:** This is the control register where playback data is written during programmed I/O data transfers. Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset when the current sample is sent to the DACs.							

Table 5-10 Codec Indirect Registers

D7	D6	D5	D4	D3	D2	D1	D0
CIR0			**MIXOUTL Output Control Register**				**Default = 00h**
Source select: 00 = LINE 10 = MIC 01 = CD 11 = MIXER		MIC +20dB Gain: 0 = Disable 1 = Enable	Reserved	Gain select for MIXOUTL (dB): 0000 = 0 0110 = +9.0 1011 = +16.5 0001 = +1.5 0111 = +10.5 1100 = +18.0 0010 = +3.0 1000 = +12.0 1101 = +19.5 0011 = +4.5 1001 = +13.5 1110 = +21.0 0100 = +6.0 1010 = +15.0 1111 = +22.5 0101 = +7.5			
CIR1			**MIXOUTR Output Control Register**				**Default = 00h**
Source select: 00 = LINE 10 = MIC 01 = CD 11 = MIXER		MIC +20dB Gain: 0 = Disable 1 = Enable	Reserved	Gain select for MIXOUTR (dB): Refer to CIR0[3:0] for decode.			
CIR2			**CDL Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for CDL (dB): 0000 = +12 0110 = –6 1011 = –21 0001 = +9 0111 = –9 1100 = –24 0010 = +6 1000 = –12 1101 = –27 0011 = +3 1001 = –15 1110 = –30 0100 = 0 1010 = –18 1111 = –33 0101 = –3 Note: This decode is also applicable for the MIC, LINE, AUX, and FM inputs.				Reserved

Table 5-10 Codec Indirect Registers (cont.)

D7	D6	D5	D4	D3	D2	D1	D0
CIR3			**CDR Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select CDR (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR4			**FML Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select FML (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR5			**FMR Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select FMR (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR6			**DACL Input Control Register**				**Default = 80h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for DAC inputs (dB): *00000 = 0 00001 = –1.5 00010 = –3.0 00011 = –4.5 00100 = –6.0 00101 = –7.5 00110 = –9.0 00111 = –10.5	01000 = –12.0 01001 = –13.5 01010 = –15.0 01011 = –16.5 01100 = –18.0 01101 = –19.5 01110 = –21.0 01111 = –22.5	10000 = –24.0 10001 = –25.5 10010 = –27.0 10011 = –28.5 10100 = –30.0 10101 = –31.5 10110 = –33.0 10111 = –34.5	11000 = –36.0 11001 = –37.5 11010 = –39.0 11011 = –40.5 11100 = –42.0 11101 = –43.5 11110 = –45.0 11111 = –46.5	
CIR7			**DACR Input Control Register**				**Default = 80h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for DAC inputs (dB): Refer to CIR6[4:0] for decode.				
CIR8			**Fs and Playback Data Format Register**				**Default = 00h**
Audio data format - linear PCM or companded for all input and output data (used in conjunction with bit 5):(1) 000 = Linear, 8-bit unsigned 001 = µ-law, 8-bit companded 010 = Linear, 16-bit two's complement, Little Endian 011 = A-Law, 8-bit companded 100 = Reserved 101 = ADPCM, 4-bit, IMA compatible 110 = Linear, 16-bit two's complement, Big Endian 111 = Reserved **Note:** Bit 7 is not available in Mode 1 (forced to 0).			Stereo/mono:(2) 0 = Mono 1 = Stereo	Clock frequency divide / audio sample rate frequency: 0000 = 8.0kHz 0010 = 16.0kHz 0100 = 27.42857kHz 0110 = 32.0kHz 1000 = Reserved 1010 = Reserved 1100 = 48.0kHz 1110 = 9.6kHz		0001 = 5.5125kHz 0011 = 11.025kHz 0101 = 18.9kHz 0111 = 22.05kHz 1001 = 37.8kHz 1011 = 44.1kHz 1101 = 33.075kHz 1111 = 6.615kHz	

(1) SB/WSS mode switch: In Sound Blaster mode, the software driver should set CDF to 8 bit PCM mode (R8: FM1,FM-,C_L).

(2) Selecting stereo results with alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left audio channel.

Note: The contents of this register can only be changed if the mode change bit (WSBase+04h[6]) is enabled (set to 1). Writes to this register without the mode change bit enabled will have no affect.

Table 5-10 Codec Indirect Registers (cont.)

D7	D6	D5	D4	D3	D2	D1	D0
CIR9			**Interface Configuration Register**				**Default = 00h**
Transfer capture data via DMA or PIO: 0 = DMA 1 = PIO	Transfer playback data via DMA or PIO: 0 = DMA 1 = PIO	Reserved		Autocalibrate: 0 = Disable 1 = Enable (autocalibration after power down/reset or mode change	DMA channel mode:(1) 0 = Dual 1 = Single	Capture data in format selected:(2) 0 = Disable 1 = Enable	Playback data in format selected:(3) 0 = Disable 1 = Enable
(1) In Sound Blaster mode, bit 2 is set when playback or capture DMA starts and is reset when DMA ends. (2) The codec generates CDRQ and responds to CDAK# when bit 1 = 1 and bit 7 = 0. If bit 7 = 1, bit 1 enables PIO capture mode. (3) The codec generates PDRQ and repents to PDAK# when bit 0 = 1 and bit 6 = 0. If bit 6 = 1, bit 1 enables PIO playback mode							
CIR10			**Pin Control Register**				**Default = 00h**
Reserved						Interrupt pin:(1) 0 = Disable 1 = Enable (Interrupt pin goes active high when the number of samples programmed in the Base Count Register is reached.)	Reserved
2. In Sound Blaster mode, the software driver should set bit 1 = 1.							
CIR11			**Error Status and Initialization Register (RO)**				**Default = 00h**
Capture overrun:(1) This bit is set when capture data has not been read by the host before the next sample arrives. The sample being read will not be overwritten by the new sample. The new sample is ignored.	Playback underrun:(1) This bit is set when playback data has not arrived from the host in time to be played. This results in a midscale value sent to the DACs.	Autocalibration state: 0 = In progress 1 = Not in progress	Current status of PDRQ and CDRQ: 0 = Inactive (low) 1 = Active (high)	Indicates under/over range on right input channel:(1) 0 = Less than –1dB under range 1 = Between –1dB and 0dB under range 2 = Between 0dB and +1dB over range 3 = Greater than +1dB over range		Indicates under/over range on left input channel:(1) 0 = Less than –1dB under range 1 = Between –1dB and 0dB under range 2 = Between 0dB and +1dB over range 3 = Greater than +1dB over range	
(1) Bit changes on a sample-by-sample basis. (2) The occurrence of a capture overrun and/or playback underrun is designated in the Status Register's sample overrun/underrun bit (WSBase+06h[4]). The sample overrun/underrun bit is the logical OR of bits 7 and 6. This enables a polling host CPU to detect an overrun/underrun condition while checking other status bits.							
CIR12			**ID Register**				**Default = 0Ah**
Reserved				Revision ID (RO): These bits define the revision level of the codec.			

Table 5-10 Codec Indirect Registers (cont.)

D7	D6	D5	D4	D3	D2	D1	D0
CIR13			**Reserved**				**Default = 00h**
CIR14			**Playback Upper Base Count Register**				**Default = 00h**
Upper Base Count: This byte is the upper byte of the base count register containing the eight most significant bits of the 16-bit base register. Reads from this register return the same value which was written The current count contained in the counters can not be read. When enabled for SB Mode, this register is used for both the Playback and Capture Base Registers.							
CIR15			**Playback Lower Base Count Register**				**Default = 00h**
Lower Base Count: This byte is the lower byte of the base count register containing the eight least significant bits of the 16-bit base register. Reads from this register return the same value which was written The current count contained in the counters can not be read. When enabled for SD Mode, this register is used for both the Playback and Capture Base Registers.							

Table 5-11 Expanded Mode CIR

7	6	5	4	3	2	1	0
CIR16			**AUXL Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for AUXL (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR17			**AUXR Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for AUXR (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR18			**LINEL Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for LINEL (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR19			**LINER Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for LINER inputs (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR20			**MICL Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	MICR mixed into OUTL: 0 = Disable 1 = Enable	Reserved	Gain select for MICL (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR21			**MICR Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	MICL mixed into OUTR: 0 = Disable 1 = Enable	Reserved	Gain select for MICR (dB): Refer to CIR2[4:1] for decode.				Reserved

Table 5-11 Expanded Mode CIR (cont.)

7	6	5	4	3	2	1	0
CIR22			**OUTL Output Control Register**				**Default = 80h**
Mute: 0 = Disable 1 = Enable	Reserved	Gain select for OUTL (dB): 00000 = 0 00001 = –3 00010 = –6 00011 = –9 00100 = –12 00101 = –15 00110 = –18 00111 = –21		01000 = –24 01001 = –27 01010 = –30 01011 = –33 01100 = –36 01101 = –39 01110 = –42 01111 = –45	10000 = –48 10001 = –51 10010 = –54 10011 = –57 10100 = –60 10101 = –63 10110 = –66 10111 = –69	11000 = –72 11001 = –75 11010 = –78 11011 = –81 11100 = –84 11101 = –87 11110 = –90 11111 = –93	Reserved
CIR23			**OUTR Output Control Register**				**Default = 80h**
Mute: 0 = Disable 1 = Enable	Reserved	Gain select for OUTR (dB): Refer to CIR22[5:1] for decode.					Reserved
CIR24-CIR27			**Reserved**				**Default = 00h**
CIR28			**Capture Data Format**				**Default = 00h**
Audio data format - linear PCM or companded for all input and output data (used in conjunction with bit 5):(1) 000 = Linear, 8-bit unsigned 001 = µ-law, 8-bit companded 010 = Linear, 16-bit two's complement, Little Endian 011 = A-Law, 8-bit companded 100 = Reserved 101 = ADPCM, 4-bit, IMA compatible 110 = Linear, 16-bit two's complement, Big Endian 111 = Reserved **Note:** Bit 7 is not available in Mode 1 (forced to 0).			Stereo/mono:(2) 0 = Mono 1 = Stereo	Reserved			
(1) SB/WSS mode switch: In Sound Blaster mode, the software driver should set CDF to 8 bit PCM mode (R8: FM1,FM-,C_L). (2) Selecting stereo results with alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left audio channel. **Note:** The contents of this register can only be changed if the mode change bit (WSBase+04h[6]) is enabled (set to 1). Writes to this register without the mode change bit enabled will have no affect.							
CIR29			**Reserved**				**Default = 00h**
CIR30			**Capture Upper Base Count**				**Default = 00h**
Upper Base Count: This byte is the upper byte of the base count register containing the eight most significant bits of the 16-bit base register. Reads from this register return the same value which was written.							
CIR31			**Capture Lower Base Count**				**Default = 00h**
Upper Base Count: This byte is the lower byte of the base count register containing the eight most significant bits of the 16-bit base register. Reads from this register return the same value which was written.							

6.0 Electrical Specification

Stresses above those listed in the following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied.

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VCC	Supply Voltage	4.5	5.5	V
AVCC	Analog Supply Voltage	4.75	5.25	V
VIN	Input Voltage	–0.5	VCC + 0.5	V
VOUT	Output Voltage	–0.5	VCC + 0.5	V
TOP	Operating Temperature	0	70	°C
TSTG	Storage Temperature	–40	125	°C
ESD[a]	ESD Tolerance (Human Body Model MIL883C, 3015.7, Notice 8)		1000	V

a. ESD sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the 82C935 features ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

6.2 DC Characteristics: 5.0 Volt (VCC = 5.0V ±5%, TA = 0°C to +70°C)

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Low Level Input Voltage	–0.3	0.8	V	VCC = 5.5V
VIH	High Level Input Voltage	2.4	VCC + 0.3	V	VCC = 4.5V
VIHa	High Level Input Voltage for RESET	3.5	VCC + 0.3	V	VCC = 4.5V
VOL	Low Level Output Voltage		0.2	V	IOL = 4mA, VCC = 4.5
VOH	High Level Output Voltage	VCC – 0.5	5.5	V	IOH = –4mA VCC = 5.5V
IIL	Input Leakage Current		10	µA	VCC = 5.5V
IILa	Input Leakage Current with 5K ohm Pull-up Resistor	–100	–500	µA	VIN = 0V
IILb	Input Leakage Current with 50K ohm Pull-up Resistor	–10	–50	µA	VIN = 0V
IOL	Output Leakage Current		10	µA	VCC = 5.5V
IPD	Static or Power-down Mode Current		300	µA	VCC = 5.5V

6.3 General Specifications: 5.0 Volt (VCC = 5.0V ±5%, TA = 0°C to +70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
IIL	Low Level Input Current	–10		10	µA	VIN = GND
IIH	High Level Input Current	–10		10	µA	VIN = VCC
IOZ	Tristate Output Leakage Current	–10		10	µA	VOUT = 0/VCC
V-	Schmitt Negative Threshold	0.8 1.5		1.3 2.5	V	TTL-STATIC CMOS-STATIC
V+	Schmitt Positive Threshold	1.4 2.5		2.1 3.5	V	TTL-STATIC CMOS-STATIC
VH	Schmitt Hysteresis		0.6 1.0		V	TTL-STATIC CMOS-STATIC
VIL	low Level Input Voltage			0.8	V	TTL-STATIC
VIH	High Level Input Voltage	2.0			V	TTL-STATIC
VOL	Low Level Output Voltage			0.4	V	TTL-STATIC
VOH	High Level Output Voltage	2.4			V	TTL-STATIC
RPD	Pull-down Resistance	50		200	KΩ	VIN = VCC
RPU	Pull-up Resistance	50		200	KΩ	VIN = VCC
CIN	Input Capacitance			5	pF	Frequency = 1MHz @ 0V
COUT	Output Capacitance			5	pF	Frequency = 1MHz @ 0V
CIO	Bidirectional Capacitance			5	pF	Frequency = 1MHz @ 0V
IOS	Short Circuit Output Current		2	25	mA	VOUT = 0V
IKLU	I/O Latch-Up Current	100			mA	V < GND, V > VCC
VESD	Electrostatic Protection	2000			V	C = 100pF, R = 1.5KΩ

6.4 Pin Specifications - Analog (VCC = 5.0V, 25°C)

Pin Name	Parameter	Min	Typ	Max	Unit	Condition
Inputs						
MICR, MICL, LINER, LINEL, CDR, CDL, AUXR, AUXL, CINR, CINL	Signal Bandwidth Input Range	10 0.5		20K 3.0	Hz V	Sine Wave
Outputs						
OUTR, OUTL	Signal Bandwidth Output Range	10 0.5		20K 3.0	Hz V	Sine Wave Load = 10KΩ, 25pF
MIXOUTR, MIXOUTL	Signal Bandwidth Output Range	10		20K	Hz	Sine Wave
VREF1 VREF2			1.75 1.85		V	DC DC

6.5 Volume Setting

Parameter	Min	Typ	Max	Unit	Test Conditions
Input Gain/Atten. Range: 16 levels (MIC, LINE, CD, AUX) 16 levels (ADC) 32 levels (DAC) 32 levels (LOUT)	 –33 0 –93 –46.5		 12 22.5 0 0	dB	Input @ 1Hz, 2.5Vpp wrt ACOM
Step Size: 16 levels (MIC, LINE, CD, AUX) 16 levels (ADC) 32 levels (DAC) 32 levels (LOUT)	 2.6 1.3 2.6 2.0 1.3	 3.0 1.5 3.0 3.0 1.5	 3.4 1.7 3.4 4.0 1.7	dB	 90 to -81dB) (-84 to -93dB)
Mute Level		–80		dB	
Signal to Noise Ratio		–80		dB	
Total Harmonic Distortion		0.04		%	
Total Dynamic Range		80		dB	
Interchannel Isolation		60		dB	
Interchannel Gain Mismatch	–0.5		0.5	dB	
Gain Drift		100		ppm/°C	

6.6 Analog Characteristics

Test conditions
Temp=25 ◦C, VDD, VCC=+5v, Input signal= 1kHz sine wave, Analog output passband: 20 Hz to 20kHz, Sample freq = 44.1 kHz

DAC test conditions
16-bit linear mode, Full Scale input, 10 kΩ output load, measured at Line Out.

ADC test conditions
16-bit linear mode, 0 dB Gain, Line Input.

6.6.1 Analog Inputs

Parameters	Min	Typ	Max	Units
Input voltage LINE/CD/AUX/CIN	2.6	2.8	3.1	Vp-p
MIC with 0dB gain	2.6	2.8	3.1	Vp-p
MIC with 20dB gain	0.26	0.28	0.31	Vp-p
Input impedance	10	20		kΩ
Input capacitance			15	pF

6.6.2 Analog Outputs (10kΩ, 25pF)

Parameters	Min	Typ	Max	Units
Full-scale output voltage (OUTR & OUTL)	2.5	2.8	3.1	Vp-p
Vref		1.85		Volts
Output impedance			600	W
External load impedance	10			kΩ

6.6.3 Volume Settings

Parameter	Min	Typ	Max	Units
Master volume step size	1.3	1.5	1.7	dB
Master volume output atten range		46.5		dB
Mute level		80		dB

6.6.4 Analog-to-Digital Converters

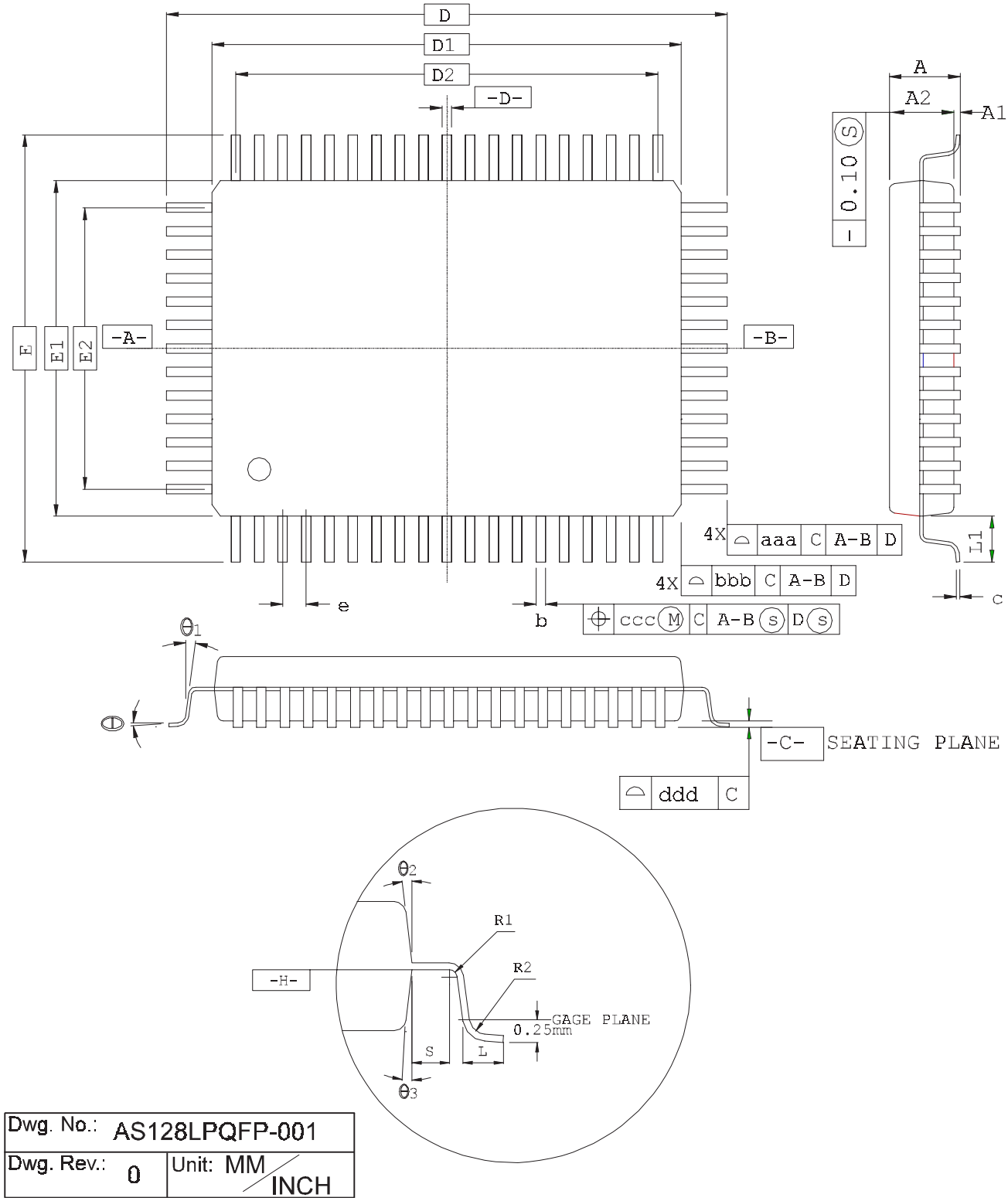
Parameters	Min	Typ	Max	Units
Resolution		16		bits
Total dynamic range	75	85		dB
THD			.025	%
Interchannel isolation: Line to Line/CD/Aux/Mic		80		dB
Interchannel gain mismatch	-0.5		+0.5	dB
Gain drift		100		ppm/◦C

6.6.5 Digital-to-Analog Converters

Parameters	Min	Typ	Max	Units
Resolution		16		bits
Total dynamic range	78	95		dB
THD			.022	%
Interchannel isolation:		80		dB
Interchannel gain mismatch	-0.5		+0.5	dB
Gain drift		100		ppm/◦C

7.0 Mechanical Package Outlines

Figure 7-1 128-Pin PQFP/LQFP*



* Refer to Table 4-1 for PQFP Variable Dimensions, and Table 4-2 for LQFP Variable Dimensions.

Table 7-1 128-Pin PQFP Variable Dimensions

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	3.40	—	—	0.134
A_1	0.25	—	—	0.010	—	—
A_2	2.50	2.72	2.90	0.098	0.107	0.114
b	0.170	0.200	0.270	0.007	0.008	0.011
c	0.11	0.15	0.23	0.004	0.006	0.009
D	23.20 BASIC			0.913 BASIC		
D_1	20.00 BASIC			0.787 BASIC		
D_2	18.50			0.728		
e	0.50 BASIC			0.020 BASIC		
E	17.20 BASIC			0.677 BASIC		
E_1	14.00 BASIC			0.551 BASIC		
E_2	12.50			0.492		
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 REF			0.063 REF		
R_1	0.13	—	—	0.005	—	—
R_2	0.13	—	0.30	0.005	—	0.012
S	0.20	—	—	0.008	—	—
θ	0°	—	7°	0°	—	7°
θ_1	0°	—	—	0°	—	—
ALLOY 42 L/F θ_2, θ_3	7° REF			7° REF		
COPPER L/F θ_2, θ_3	15° REF			15° REF		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	—	0.08	—	—	0.003	—
ddd	—	0.08	—	—	0.003	—

Note: Control dimensions are in millimeters.

Note: 1) Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane -H-.

Note: 2) Dimension b does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot.

Table 7-2 128-Pin LQFP Variable Dimensions

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.170	0.200	0.270	0.007	0.008	0.011
c	0.09	—	0.20	0.004	—	0.008
D	22.00 BASIC			0.866 BASIC		
D_1	20.00 BASIC			0.787 BASIC		
D_2	18.50			0.728		
e	0.50 BASIC			0.020 BASIC		
E	16.00 BASIC			0.630 BASIC		
E_1	14.00 BASIC			0.551 BASIC		
E_2	12.50			0.492		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	—	0.08	—	—	0.003	—
ddd	—	0.08	—	—	0.003	—

Note: Control dimensions are in millimeters.

Note: 1) Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.

Note: 2) Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more that 0.08mm. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.