Section 4 : Configuration Registers

4.1 Register Description

This section includes the register description of four devices inside the M1543C. Section 4.1.1 introduces the M1543C's PCI to ISA Bridge configuration registers. Section 4.1.2 introduces IDE master M5229 configuration register. Section 4.1.3 introduces USB Controller M5237 configuration register. Section 4.1.4 introduces PMU device M7101 configuration register.

4.1.1 M1543C PCI to ISA Bridge Configuration Space (IDSEL= AD18)

The indices before 40h are read-only. All reserved bits are read as 0's. The following table shows the register summary :

Byte Index	Mnemonic	Definition	Attribute (R/W)	Default Value
01h-00h	VID	Vender ID	R	10B9h
03h-02h	DID	Device ID	R	1533h
05h-04h	COM	Command	R/W	000Fh
07h-06h	DS	Status	R/W Clear	0200h
08h	RID	Revision ID	R	C0h
0Bh-09h	CC	Class Code	R~~/W~~	060100h
0Dh-0Ch	Reserved	Reserved	R	0000h
0Eh	HT	Header Type	R	00h
2Bh-0Fh	Reserved	Reserved	R	00h
2Dh-2Ch	SVID	Subsystem Vendor ID	R/W Lock	0000h
2Fh-2Eh	SDID	Subsystem Device ID	R/W Lock	0000h
3Fh-30h	Reserved	Reserved	R	00h
40h	PIC	PCI Interface Control	R/W	00h
41h	IORC	I/O Recovery Control	R/W	00h
42h	ISACI	ISA Bus Cycle Control I	R/W	00h
43h	ISACII	ISA Bus Cycle Control II	R/W	00h
44h	IDENRI	IDE Native Mode Interrupt Routing I	R/W	00h
45h	PIPM	PCI Interrupt Polling Mode	R/W	00h
46h	Reserved	Reserved	R	00h
47h	BCSC	BIOS Chip Select Control	R/W	00h
48h	PIRTI	PCI Interrupt to ISA IRQ Routing Table I	R/W	00h
49h	PIRTII	PCI Interrupt to ISA IRQ Routing Table II	R/W	00h
4Ah	PIRTIII	PCI Interrupt to ISA IRQ Routing Table III	R/W	00h
4Bh	PIRTIV	PCI Interrupt to ISA IRQ Routing Table IV	R/W	00h
4Ch	PILET	PCI Interrupt Level to Edge Transfer	R/W	00h
4Fh-4Dh	Reserved	Reserved	R	00h
51h-50h	IOPWI	I/O Cycle Posted-Write First Port Definition	R/W	0000h
53h-52h	IOPWII	I/O Cycle Posted-Write Second Port Definition	R/W	0000h
54h	HSSB	Hardware Setting Status Bits	R	Strobed Value
57h-55h	PCSAD	Programmable Chip Select (Pin PCSJ) Address Definition	R/W	000002h
58h	IDEIC	IDE Interface Control	R/W	00h
59h	GPIS	General Purpose Input (GPI) Multiplexed Pin Select	R/W	00h
5Bh-5Ah	GPOS	General Purpose Output (GPO) Multiplexed Pin Select	R/W	0000h
5Dh-5Ch	DMDC	Docking Mode Decode Control	R/W	0000h
5Eh	SMCCI	Suspend Mode Clock Control I	R/W	00h
5Fh	SMCCII	Suspend Mode Clock Control II	R/W	00h

Byte Index	Mnemonic	Definition	Attribute (R/W)	Default Value
6Ch-60h	Reserved	Reserved	R	00h
6Dh	RAM	ROM Address Mapping	R/W	00h
6Eh	ISPSS	ISP Shadow I/O Port Select	R/W	00h
6Fh	ISPSD	ISP Shadow I/O Select Port Data	R	00h
70h	SIRQCR	Serial IRQ (IRQSER) Control Register	R/W	00h
71h	DDMAS	Distributed DMA Channel on PCI or ISA Side	R/W	00h
72h	USBIDS	USB IDSEL Mux Select	R/W	00h
73h	DDMABA	Distributed DMA Base Address	R/W	00h
74h	USBIR	USB Interrupt Routing Table	R/W	00h
75h	IDENRII	IDE Native Mode Interrupt Routing II	R/W	00h
76h	SCIIR	PMU System Control Interrupt Routing Table	R/W	00h
77h	SMBIR	SMB Controller Event Interrupt Routing Table	R/W	00h
78h	AGPIS	AGP Interrupt Selection	R/W	00h
7Bh-79h	Reserved	Reserved	R	00h
FFh-7Ch	MAPR	M7101 Mapping Register	R/W	00h

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Register Index : **01h-00h**
Register Name : **VID - Vendor ID Register**
Attribute : Read Only
Default Value : 10B9h

Bit No.	Description
15-0 (10B9h)	This is a 16-bit value assigned to Acer Labs Inc. This register is combined with 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Register Index : **03h-02h**
Register Name : **DID - Device ID Register**
Attribute : Read Only
Default Value : 1533h

Bit No.	Description
15-0 (1533h)	This register holds a unique 16-bit value assigned to a device, and combined with the vendor ID, it identifies any PCI device. Write to this register has no effect.

Register Index : **05h-04h**
Register Name : **COM - Command Register**
Attribute : Read/Write
Default Value : 000Fh

Bit No.	Description
15-5(000h)	Reserved. These bits are always 0.
4(0b)	Memory Write and Invalidate Command. The M1543C will never issue Memory Write and Invalidate commands. This bit is always 0. Write to this bit has no effect.
3(1b)	Enable Special Cycle. The M1543C can always accept special cycles on the PCI. This bit is always 1. Write to this bit has no effect.
2(1b)	Enable PCI Master. The M1543C does not disable bus master operations. This bit is set to 1 during Power-On to enable PCI master operartions. Write to this bit has no effect.
1(1b)	Enable Response to Memory Access. The M1543C as a target always responds to memory cycles. This bit is always 1. Write to this bit has no effect.
0(1b)	Enable Response to I/O Access. The M1543C as a target always responds to I/O cycles. This bit is always 1. Write to this bit has no effect.

Register Index : **07h-06h**
Register Name : **DS - Device Status Register**
Attribute : Read Only, Read/Write Clear
Default Value : 0200h

Bit No.	Description
15(0b)	Detected Parity Error. This bit is always 0 in the M1543C implementation.
14(0b)	SERRJ Status. This bit is always 0 in the M1543C implementation.
13(0b)	Received Master Abort Status. This bit is set to 1 when the M1543C, acting as a PCI master, aborts a PCI bus memory cycle. This bit is cleared (reset to 0) by writing a 1 to it.
12(0b)	Received Target Abort Status. This bit is set to 1 when the M1543C generates PCI cycle (M1543C is the PCI master) is aborted by a PCI target. This bit is cleared (reset to 0) by writing a 1 to it.
11(0b)	Sent Target Abort Status. The M1543C as a slave never generates a Target abort. This bit is always 0.
10-9(01b)	DEVSELJ Timing. Read only bits indicating DEVSELJ timing when performing a positive decode. 00 : Fast. 01 : Medium. 10 : Slow. Since DEVSELJ is asserted by the M1543C to meet the medium timing, these bits are encoded as 01b.
8-0(000h)	Reserved. These bits are always 0.

Register Index : **08h**
Register Name : **RID - Revision ID Register**
Attribute : Read only
Default Value : C0h

Bit No.	Description
7-0(C0h)	This register contains the version number of the M1543C.

Register Index : **0B-09h**
Register Name : **CC - Class Code Register**
Attribute : Read Only
Default Value : 060100h

Bit No.	Description
23-0 (060100h)	This register identifies the Class Code of the M1543C.

Register Index : **0Dh - 0Ch**
Register Name : **Reserved Register**
Attribute : Read Only
Default Value : 0000h

Register Index : **0Eh**
Register Name : **HT - Header Type Register**
Attribute : Read only
Default Value : 00h

Bit No.	Description
7-0(00h)	This register identifies the type of predefined header in the configuration space. Since the M1543C is a single function device and not a PCI-to-PCI bridge, this byte should be read as 00h.

Register Index : **2Bh-0Fh**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index: **2Dh-02Ch**
Register Name: **SVID - Subsystem Vendor ID**
Attribute: Read/Write Lock
Default Value: 0000h

Bit	Description
15-0 (0000h)	If the M1543C Register Index 74h bit6 = 0, then this register is Readable/Writeable. Else, this register is Read-Only. BIOS should program a value to this register and then lock it by setting the M1543C Register Index 74h bit6 = 1.

Register Index : **2Fh-02Eh**
Register Name : **SDID - Subsystem Device ID**
Attribute : Read/Write Lock
Default Value : 0000h

Bit	Description
15-0 (0000h)	If the M1543C Register Index 74h bit6 = 0, then this register can Read/Write. Else, this register is Read-Only. BIOS should program a value to this register and then lock it by setting the M1543C Register Index 74h bit6 = 1.

Register Index : **3Fh-30h**
Register Name : **Reserved Register**
Attribute : Read Only
Default Value : 00h

Register Index : **40h**
Register Name : **PIC - PCI Interface Control**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	Reserved.
6 (0b)	Sound Card I/O Posted-Write Enable/Disable. 0 : Disable. 1 : Enable. The usage of this bit is as follows : 1. When enabling this bit, the M1543C register Index-40h bit2 should be enabled simultaneously. 2. This bit is a enable/disable switch of the M1543C register Index-50h-53h sound card I/O Posted Write Buffer. All the I/O ports defined in Index-50h-53h will utilize the PCI-to-ISA Posted Write Buffer. 3. This bit has no effect on internal I/O port, eg. 8254, 8259, 8237 ports.
5 (0b)	Select ISA Master to PCI Bus Request Method. 0 : Bus request at each time ISA Master requests the bus. 1 : Bus request only when ISA Master asserts command. This bit combined with the M1543C register Index-40h bit4 to control the Passive Release feature. When this bit is set to 1, the M1543C will de-assert PHOLDJ between consecutive ISA master accesses to allow PCI arbiter (in North Bridge) to grant PCI bus to another PCI master. When this bit is reset as 0, the M1543C will not de-assert PHOLDJ between consecutive ISA master accesses. In this setting, PCI arbiter (in North Bridge) will not grant PCI bus to another PCI master between consecutive ISA master accesses. Value 1 is recommended for best system performance.
4 (0b)	Passive Release Feature. 0 : Disable. 1 : Enable. Enable the Passive Release feature can allow PCI arbiter (in North Bridge) to grant to another PCI master during ISA master access (by de-asserting PHOLDJ signal). Disable this feature, PCI bus will be occupied by the whole cycles during ISA master access. If this feature is enabled, the same feature setting in North Bridge should be enabled also. Only North Bridge or South Bridge is enabled at one side, there will be unexpected behaviour to cause system failure. Value 1 is recommended for best system performance.
3 (0b)	Delayed Transaction for PCI Spec. 2.1 Enable/Disable. 0 : Disable. 1 : Enable. This bit is used to enable Delay Transaction feature for PCI specification 2.1. When this feature is enabled, the M1543C will decode the access, latch the cycle request, and terminate the cycle with Retry. Then the M1543C will compete the cycle request, and then complete the PCI transaction when the retry PCI cycle is back. If this bit is disabled, all the cycles decoded by M1543C will wait until the access is finished.
2 (0b)	PCI-to-ISA Posted Write Buffer Enable/Disable. 0 : Disable. 1 : Enable. This bit is used to enable PCI-to-ISA Posted Write Buffer, and it includes PCI to ISA Memory Post Write (all Memory Cycles) and I/O Post Write (defined by same register bit 6 and the M1543C register Index-50h-53h).
1 (0b)	ISA Master Line Buffer Enable/Disable. 0 : Disable. 1 : Enable. This bit is used to enable ISA master line buffer. When this bit is set to 1, all ISA Master accesses will utilize the 8-byte bi-directional Line Buffer to enhance the performance. Value 1 is recommended for best system performance.
0 (0b)	DMA Line Buffer Enable/Disable. 0 : Disable. 1 : Enable. This bit is used to enable DMA master line buffer. When this bit is set to 1, all DMA accesses will utilize the 8-byte bidirectional Line Buffer to enhance the performance. Value 1 is recommended for best system performance.

Register Index : **41h**
Register Name : **IORC - I/O Recovery Control**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	PS/2 Keyboard Present Feature. 0 : Without PS/2 keyboard (AT IRQ1). 1 : With PS/2 Keyboard. This bit is used to control the IRQ1 signal before it connects to internal 8259. Since IRQ1 timing is different in PS/2 and AT keyboards, this bit needs to be programmed correctly. If PS/2 keyboard is used, this bit must set to 1 to enable IRQ1 latch when IRQ1 goes high. IRQ1 will keep high and then go low until the M1543C decodes a read I/O Port 60h cycle. If AT keyboard is used, this bit must reset to 0 and will directly connect IRQ1 to internal 8259.
6 (0b)	PS/2 Mouse/AT Mouse select 0 : AT mouse. 1 : With PS/2 mouse. This bit is used to control the IRQ12 signal before it connects to internal 8259. Since IRQ12 timing is different in PS/2 and AT mice, this bit needs to be programmed correctly. If PS/2 mouse is used, this bit must set to 1 to enable IRQ12 latch when IRQ12 goes high. IRQ12 will keep high and then go low until the M1543C decodes a read I/O Port 60h cycle. If AT mouse is used, this bit must reset to 0 and will directly connect IRQ12 to internal 8259. Note : If IRQ[12] is used in PCI routing or ISA slot, this bit must be 0.
5-2 (0h)	I/O Recovery Period. 0,0,0,0 : 0 us. 0,0,0,1 : 0.25 us (2*ATCLK). 0,0,1,0 : 0.5 us (4*ATCLK). 0,0,1,1 : 0.75 us (6*ATCLK). 0,1,0,0 : 1 us (8*ATCLK). 0,1,0,1 : 1.25 us (10*ATCLK). 0,1,1,0 : 1.5 us (12*ATCLK). 0,1,1,1 : 1.75 us (14*ATCLK). 1,0,0,0 : 2 us (16*ATCLK). 1,0,0,1 : 2.25 us (18*ATCLK). 1,0,1,0 : 2.5 us (20*ATCLK). 1,0,1,1 : 2.75 us (22*ATCLK). 1,1,0,0 : 3 us (24*ATCLK). 1,1,0,1 : 3.25 us (26*ATCLK). 1,1,1,0 : 3.5 us (28*ATCLK). 1,1,1,1 : 3.75 us (30*ATCLK). Long period setting will hurt the system performance especially when some ISA cards have a lot of I/O cycle accesses. It is recommended not to program the period longer than 1 us.
1 (0b)	On-Chip I/O Recovery Feature. 0 : Disable. 1 : Enable. This bit is used for the M1543C internal I/O Port I/O recovery timer. This bit will only take effect when bit0 = 1. The period of time will be defined in bits[5:2].
0 (0b)	ISA I/O Recovery Feature. 0 : Disable. 1 : Enable. I/O Recovery timer is used to guarantee the recovery time between back to back I/O cycles. This bit is used to enable ISA I/O recovery timer. The period of time will be defined in bits[5:2]. Value 1 is recommended for some old ISA card compatibility issue.

Register Index : **42h**
Register Name : **ISACI - ISA Bus Cycle Control I**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	Configuration Port Read Data Mask Function. 0 : Normal I/O read/write. 1 : Read from Index-40h to -FFh are all 0's. When this bit is set to 1, the configuration read cycle from register Index-40h to Index-FFh will output all 0's no matter what the real contents are. This feature is for test purposes only. Value 0 is recommended for normal operation.
6 (0b)	DMA High Page Register Enable/Disable. 0 : Disable. (24 Bits Addressing) 1 : Enable. (32 Bits Addressing) This bit is used to enable DMA 32-bit addressing support.
5 (0b)	Reserved (must be 0).
4 (0b)	Reserved (must be 0).
3 (0b)	Decoupled Refresh Control. 0 : Normal refresh. 1 : Decoupled refresh. If this bit is reset to 0, Refresh Master will own ISA and PCI bus (by assertion PHOLDJ to own PCI bus). When this bit is set to 1, refresh master will only own ISA Bus, and PCI bus is still available for the access. The refresh period is defined in the M1543C register Index-43h bits[5:4]. Value 1 is recommended for best system performance.
2-0 (0h)	ISA Clock SYSCLK Frequency Select. 000 : 7.16 MHz. 001 : PCICLK/2. 010 : PCICLK/3. 011 : PCICLK/4. 100 : PCICLK/5. 101 : PCICLK/6. 110 : Reserved. 111 : Reserved. These three bits are used to define the ISA SYSCLK generated by OSC14M divided by 2, or by PCICLK divider. Programmer should not program these bits to support ISA clock specifications.

Register Index : **43h**
Register Name : **ISACII - ISA Bus Cycle Control II**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	Port-92h RC/GATEA20 Selection. 0 : Disable Port-92h. 1 : Enable Port-92h. Port-92h is used to start FAST RC/GATEA20 sequence. This bit is used to enable Port 92h.
6 (0b)	Enable/Disable Coprocessor Interface. 0 : Disable (Pin FERRJ as IRQ13; IGNNEJ always 1) 1 : Enable (Pin FERRJ as FERRJ) This bit is enabled to support the coprocessor error reporting, and FERRJ and IGNNEJ are connected to CPU. When it is disabled, pin FERRJ will become IRQ13 function and pin IGNNEJ will always be driven high.
5-4 (0h)	ISA Refresh Period Setting. 0,0 : 15 us Refresh Period. 0,1 : 30 us. 1,0 : 60 us. 1,1 : 120 us. These two bits are used to set the ISA refresh period. When the programmed time is up, the M1543C will start an ISA bus refresh cycle to allow ISA card DRAM memory to do refresh.
3-2 (0h)	16-bit ISA Memory Command Insert Wait Count. 0,0 : Normal 16 bit access. 0,1 : Insert 1 wait. 1,0 : Insert 2 waits. 1,1 : Insert 3 waits. These two bits are used to insert wait state for 16-bit ISA Memory command. Insert 1 wait means to extend the Memory command for 1 ISA clock.
1-0 (0h)	16-bit ISA I/O Command Insert Wait Count. 0,0 : Normal 16-bit access. 0,1 : Insert 1 wait. 1,0 : Insert 2 waits. 1,1 : Insert 3 waits. These two bits are used to insert wait state for 16-bit ISA I/O command. Insert 1 wait means to extend the I/O command for 1 ISA clock.

Register Index : **44h**
Register Name : **IDENRI - IDE Native Mode Interrupt Routing I**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	PCI Soft Reset Control. 0 : When CPU soft reset initializes, PCIRSTJ will not be active. 1 : When CPU soft reset initializes, PCIRSTJ will be active. This bit is used to control the assertion of PCIRSTJ when CPU soft reset is initialized. Some PCI cards may need to be reset during CPU soft reset. BIOS can use this bit to solve this issue by resetting the whole PCI bus.
6 (0b)	On-Chip I/O Decode. (No. include DMA I/O ports, they are always subtractively decoded.) 0 : Positively decode. 1 : Subtractively decode. Please refer to section 3.5 Addressing Decoding for more detailed information.
5 (0b)	Reserved. '0'
4 (0b)	On-chip IDE Controller (M5229) Primary Channel Interrupt Signal Transform Enable/Disable. 0 : Disable. (Bypass) 1 : Enable. (Level -> Edge) This bit is used to transfer the level of on-chip IDE controller (M5229) Primary Channel Interrupt input signal. When this bit is set to 1, internal circuit will transfer the level to edge before connecting to 8259.
3-0 (0h)	On-chip IDE Controller (M5229) Primary Channel Interrupt Routing When Native Mode is Enabled. Bit 3-2-1-0 0 0 0 0 : Disable. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to decide on-chip IDE controller Primary channel Interrupt routing table when native mode is enabled. It is recommended to connect IDE primary channel Interrupt to pin SIRQI and use this table to route the interrupt to any available 8259 Interrupt lines. Please refer to the M1543C Register Index-58h for more information.

Register Index : **45h**
Register Name : **PIPM - PCI Interrupt Polling Mode**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	PCI Interrupt Polling Mode Enable/Disable. 0 : Disable. 1 : Enable. This bit is used to enable PCI Interrupt Polling Mode to support 8 PCI interrupts routing. A 74F151 (or 74LS151) is needed when the Polling mode is enabled. The polling clock is based on PCI Clock or OSC14M selected by the M1543C Register Index 57h-55h bit20. 74F151 is needed if PCI Clock is selected. Otherwise, 74F151 or 74LS51 are both OK if OSC14M is selected. If this bit is disabled, 4 PCI Interrupts are supported and directly connect to the M1543C. No 74F151 (or 74LS151) is needed.
6 (0b)	Pin ROMKBCSJ activated when accessing I/O 62h and 66h Port. 0 : Disable. 1 : Enable. If this bit is enabled, pin ROMKBCSJ will be active when accessing I/O 60,64,62,66h ports. This feature is designed for some embedded application to decode I/O 62h and 66h ports.
5 (0b)	Reserved.
4 (0b)	Reserved.
3 (0b)	Delayed Transaction Timeout Counter Enable/Disable. 0 : Disable. 1 : Enable. The bit is used to enable the Discard Timer timeout defined by PCI specification 2.1. When this bit is enabled, the M1543C will discard the Delayed Transaction completion when the PCI master has not repeated the request within 2**15 PCICLKs. If this bit is disabled, the M1543C will keep waiting until the PCI master access is back. Value 1 is recommended when Delayed Transaction feature is enabled (M1543C register Index-40h bit3 = 1).
2 (0b)	Reserved.
1 (0b)	Distributed DMA Enable/Disable. 0 : Disable. 1 : Enable. This bit is used to enable the Distributed DMA feature. Distributed DMA feature is used to solve software legacy issue when Audio is moved to PCI bus.
0 (0b)	Parity Check Enable/Disable. 0 : Disable. 1 : Enable. This bit is used to enable the Parity Check. If this bit is enabled, the M1543C will issue NMI to CPU when it detects the SERRJ assertion, IOCHKJ assertion, and PCI bus parity error. When this bit is disabled, the M1543C will never assert NMI to inform Parity error.

Register Index : **46h**
Register Name : **Reserved Register**
Attribute : Read Only
Default Value : 00h

Register Index : **47h**
Register Name : **BCSC - BIOS Chip Select Control**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	SA16 Inverter Control. 0 : Normal SA[16]. 1 : Invert SA[16] when ROM Chip Select Active. This bit is used to enable the internal Inverter of ISA SA16 when ROM chip select is active. BIOS can use this bit to invert the PCI bus address AD[16] before it passes to ISA bus address SA[16].
6 (0b)	Flash ROM Read/Write Control (Write Protect). 0 : Disable. 1 : Enable. When this bit is disabled, ROMKBCSJ will be active only in memory read cycle. When this bit is enabled, ROMKBCSJ will be active in memory read/write cycles. BIOS can use this bit to write protect or flush ROM content.
5 (0b)	Extended ROM Region Enable/Disable. 0 : Disable. 1 : Enable. ROMKBCSJ will be active when a PCI master accesses memory address range 000D0000h-000DFFFFh and this bit is enabled.
4 (0b)	Shared Memory VGA BIOS Region Decode. 0 : Disable. 1 : Enable. ROMKBCSJ will be active when a PCI master accesses memory address range 000C8000h-000CFFFFh and this bit is enabled.
3 (0b)	Shared Memory VGA BIOS Region Decode. 0 : Disable. 1 : Enable. ROMKBCSJ will be active when a PCI master accesses memory address range 000C0000-000C7FFF and this bit is enabled.
2 (0b)	Extended ROM Region Enable/Disable. 0 : Disable. 1 : Enable. ROMKBCSJ will be active when a PCI master accesses memory address range FFFC0000-FFFDFFFF and this bit is enabled. This bit will enlarge the ROM size to 256 KB.
1 (0b)	Extended ROM Region Enable/Disable. 0 : Disable. 1 : Enable. ROMKBCSJ will be active when a PCI master accesses memory address range FFFE0000-FFFEFFFF and this bit is enabled.
0 (0b)	ROM Size Define for ROM Chip Select Decode. 0 : 64 KB (000F0000h-000FFFFFh or FFFF0000h-FFFFFFFFh). 1 : 128 KB (000E0000h-000FFFFFh or FFFF0000h-FFFFFFFFh). This bit is used to decide the ROMKBCSJ decode region. When this bit is 0, only 64KB (000F0000h-000FFFFFh or FFFF0000h-FFFFFFFFh) address range is decoded and asserts ROMKBCSJ. When this bit is 1, 128KB (000E0000h-000FFFFFh or FFFF0000h-FFFFFFFFh) address range is decoded and asserts ROMKBCSJ.

Register Index : **48h**
Register Name : **PIRTI - PCI Interrupt to ISA IRQ Routing Table I**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-4 (0h)	INT2J (in Polling Mode) or INTBJS0 to ISA IRQ Routing Table. 0 0 0 0 : Disable. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to route INT2J (in Polling mode) or INTBJS0 to any 8259 Interrupt lines. The BIOS should inhibit to set the reserved value. The reserved setting will disable the IRQ at the present design.
3-0 (0h)	INT1J (in Polling Mode) or INTAJ_MI to ISA IRQ Routing Table. 0 0 0 0 : Disable. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to route INT1J (in Polling mode) or INTAJ_MI to any 8259 Interrupt lines. The BIOS should inhibit to set the reserved value. The reserved setting will disable the IRQ at the present design.

Register Index : **49h**
Register Name : **PIRTII - PCI Interrupt to ISA IRQ Routing Table II**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-4 (0h)	INT4J (in Polling Mode) or INTDJS2 to ISA IRQ Routing Table. 0 0 0 0 : Disable. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to route INT4J (in Polling Mode) or INTDJS2 to any 8259 Interrupt lines. The BIOS should inhibit to set the reserved value. The reserved setting will disable the IRQ at the present design.
3-0 (0h)	INT3J (in Polling Mode) or INTCJS1 to ISA IRQ Routing Table. 0 0 0 0 : Disable. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to route INT3J (in Polling Mode) or INTCJS1 to any 8259 Interrupt lines. The BIOS should inhibit to set the reserved value. The reserved setting will disable the IRQ at the present design.

Register Index : **4Ah**
Register Name : **PIRTIII - PCI Interrupt to ISA IRQ Routing Table III**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-4 (0h)	INT6J (in Polling Mode) to ISA IRQ Routing Table. 0 0 0 0 : Disable. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to route INT6J (in Polling Mode) to any 8259 Interrupt lines. The BIOS should inhibit to set the reserved value. The reserved setting will disable the IRQ at the present design.
3-0 (0h)	INT5J (in Polling Mode) to ISA IRQ Routing Table. 0 0 0 0 : Disable. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to route INT5J (in Polling Mode) to any 8259 Interrupt lines. The BIOS should inhibit to set the reserved value. The reserved setting will disable the IRQ at the present design.

Register Index : **4Bh**
Register Name : **PIRTIV - PCI Interrupt to ISA IRQ Routing Table IV**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-4 (0h)	INT8J (in Polling Mode) or IRQ[15]/AGP_INTBJ (in Non-Polling Mode) to ISA IRQ Routing Table. 0 0 0 0 : Disable. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to route INT8J (in Polling Mode) or IRQ[15]/AGP_INTBJ (in Non-Polling Mode) to any 8259 Interrupt lines. The BIOS should inhibit to set the reserved value. The reserved setting will disable the IRQ at the present design.
3-0 (0h)	INT7J (in Polling Mode) or IRQ[14]/AGP_INTAJ (in Non-Polling Mode) to ISA IRQ Routing Table. 0 0 0 0 : Disable. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to route INT7J (in Polling Mode) or IRQ[14]/AGP_INTAJ (in Non-Polling Mode) to any 8259 Interrupt lines. The BIOS should inhibit to set the reserved value. The reserved setting will disable the IRQ at the present design.

Register Index : **4Ch**
Register Name : **PILET - PCI Interrupt Level to Edge Transfer**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	INT8J (in Polling Mode) or IRQ[15]/AGP_INTBJ (in non-polling mode) Level to Edge Transfer. 0 : Disable. (Bypass) 1 : Enable. (Level -> Edge) When this bit is reset as 0, INT8J will be bypassed as level trigger to M8259. When this bit is set to 1, INT8J will be transformed to be Edge trigger to M8259.
6 (0b)	INT7J (in Polling Mode) or IRQ[14]/AGP_INTAJ (in non-polling mode) Level to Edge Transfer. 0 : Disable. (Bypass) 1 : Enable. (Level -> Edge) When this bit is reset as 0, INT7J will be bypassed as level trigger to M8259. When this bit is set to 1, INT7J will be transformed to be Edge trigger to M8259.
5 (0b)	INT6J (in Polling Mode) Level to Edge Transfer. 0 : Disable. (Bypass) 1 : Enable. (Level -> Edge) When this bit is reset as 0, INT6J will be bypassed as level trigger to M8259. When this bit is set to 1, INT6J will be transformed to be Edge trigger to M8259.
4 (0b)	INT5J (in Polling Mode) Level to Edge Transfer. 0 : Disable. (Bypass) 1 : Enable. (Level -> Edge) When this bit is reset as 0, INT5J will be bypassed as level trigger to M8259. When this bit is set to 1, INT5J will be transformed to be Edge trigger to M8259.
3 (0b)	INT4J (in Polling Mode) or INTDJS2 Level to Edge Transfer. 0 : Disable. (Bypass) 1 : Enable. (Level -> Edge) When this bit is reset as 0, INT4J (in Polling Mode) or INTDJS2 will be bypassed as level trigger to M8259. When this bit is set to 1, INT4J (in Polling Mode) or INTDJS2 will be transformed to be Edge trigger to M8259.
2 (0b)	INT3J (in Polling Mode) or INTCJS1 Level to Edge Transfer. 0 : Disable. (Bypass) 1 : Enable. (Level -> Edge) When this bit is reset as 0, INT3J (in Polling mode) or INTCJS1 will be bypassed as level trigger to M8259. When this bit is set to 1, INT3J (in Polling mode) or INTCJS1 will be transformed to be edge trigger to M8259.
1 (0b)	INT2J (in Polling Mode) or INTBJS0 Level to Edge Transfer. 0 : Disable. (Bypass) 1 : Enable. (Level -> Edge) When this bit is reset as 0, INT2J (in Polling mode) or INTBJS0 will be bypassed as level trigger to M8259. When this bit is set to 1, INT2J (in Polling mode) or INTBJS0 will be transformed to be Edge trigger to M8259.
0 (0b)	INT1J (in Polling Mode) or INTAJ_MI Level to Edge Transfer. 0 : Disable. (Bypass) 1 : Enable. (Level -> Edge) When this bit is reset as 0, INT1J (in Polling mode) or INTAJ_MI will be bypassed as level trigger to M8259. When this bit is set to 1, INT1J (in Polling mode) or INTAJ_MI will be transformed to be Edge trigger to M8259.

Register Index : **4Fh-4Dh**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **51h-50h**
Register Name : **IOPWI - I/O Cycle Posted-Write First Port Definition**
Attribute : Read/Write
Default Value : 0000h

Bit No.	Description
15 (0b)	I/O Cycle Posted-Write First Port Definition. 0 : Disable. 1 : Enable. This bit is used to enable the I/O cycle Posted-Write First Port Definition in bits[11:0].
14-12 (0h)	Reserved.
11-0 (000h)	I/O Cycle Posted-Write First Port Defined Address A[11:0]. When bit15 = 1 and M1543C register Index-40h bit2 = 1 and bit 6 = 1, the defined address will utilize the PCI-to-ISA Posted Write Buffer.

Register Index : **53h-52h**
Register Name : **IOPWII - I/O Cycle Posted-Write Second Port Definition**
Attribute : Read/Write
Default Value : 0000h

Bit No.	Description
15 (0b)	I/O Cycle Posted-Write Second Port Definition. 0 : Disable. 1 : Enable. This bit is used to enable the I/O cycle Posted-Write Second Port Definition in bits[11:0].
14 (0b)	On-chip USB Device Enable/Disable. 0 : Enable. 1 : Disable. When this bit is set to 1, on-chip USB (M5237) will be disabled and become invincible to software. It can be used for the motherboard designer to fully disable internal USB function.
13 (0b)	RTC address index port (70h,72h) read enable. 0 : disable 1 : enable
12 (0b)	USB IRQ[1]/IRQ[12] filter enable. 0 : disable, bypass 1 : enable, IRQ[1]/IRQ[12] low to high transition generates an IRQ pulse.
11-0 (000h)	I/O Cycle Posted-Write Second Port Defined Address A[11:0]. When bit15 = 1 and M1543C register Index-40h bit2 = 1 and bit6 = 1, the defined address will utilize the PCI-to-ISA Posted Write Buffer.

Register Index : **54h**
Register Name : **HSSB - Hardware Setting Status Bits**
Attribute : Read only
Default Value : Strobed Value

Bit No.	Description
7	PCSJ Hardware Setting Status. 0 : Pull-low, Hotkey function enable. 1 : Pull-high, Hotkey function disable. Please refer to section 1.4 for more detailed information.
6	PHOLDJ Hardware Setting Status. 0 : Pull-low, USB in test mode. (for test purposes only) 1 : Pull-high, USB in normal mode. In normal operation, this pin must be pulled high.
5	Reserved.
4	SPLED Hardware Setting Status. 0 : Pull-low, support 256KB ROM. 1 : Pull-high, not support 256KB ROM. Please refer to section 2.5 for more detailed information.
3	XDIR Hardware Setting Status. 0 : Pull-low, Pentium II CPU is used. 1 : Pull-high, Pentium CPU is used. Please refer to section 2.5 for more detailed information.
2	TC Hardware Setting Status. 0 : Pull-low, pins SD/GPIO[7:0] are SD[7:0], external LS245 is not required. 1 : Pull-high, pins SD/GPIO[7:0] are GPIO[7:0], external LS245 is required. Please refer to section 1.4 for more information.
1	SPKR Hardware Setting Status. 0 : Pull-low, internal Super I/O test mode is enabled. (for test purposes only) 1 : Pull-high, internal Super I/O test mode is disabled. In normal operation, this pin must be pulled high.
0	ROMKBCSJ Hardware Setting Status. 0 : Pull-low, chip test mode is enabled. (for test only) 1 : Pull-high, chip test mode is disabled. In normal operation, this pin must be pulled high.

Register Index : **57h-55h**
Register Name : **PCSAD - Programmable Chip Select (Pin PCSJ) Address Definition**
Attribute : Read/Write
Default Value : 000002h

Bit No.	Description
23 (0b)	Include I/O Ports 62h, 66h for Decode PCSJ Enable/Disable. 0 : Disable. 1 : Enable. When this bit is enabled, I/O ports 62h, 66h access will assert PCSJ.
22 (0b)	Chip Select Qualified by ISA Bus IOWJ Enable/Disable. 0 : Disable. 1 : Enable. When this bit is enabled, the assertion of PCSJ will qualify IOWJ command. Otherwise, PCSJ will be asserted when the programmed address matches and will not be qualified by IOWJ command. When index 78h D4 = 1, this bit should be 0.
21 (0b)	Chip Select Qualified by ISA Bus IORJ Enable/Disable. 0 : Disable. 1 : Enable. When this bit is enabled, the assertion of PCSJ will qualify IORJ command. Otherwise, PCSJ will be asserted when the programmed address matches and will not be qualified by IORJ command. When index 78h D4 = 1, this bit should be 0.
20 (0b)	Select PCI Interrupt Polling Clock. 0 : PCI Clock. 1 : OSC14M. This bit is used to select the PCI Interrupt Polling clock when PCI Interrupt Polling mode is enabled (M1543C Register Index-45h bit 7 = 1). If PCI clock is chosen, 74F151 is needed. If OSC14M is selected, 74LS151 is enough.
19-16 (0h)	Reserved.
15-2 (0000h)	When index 78h D4 = 1, D15-D5 are defined as the programmable memory address A15-A5 for APICCSJ. D4-D2 are not used. When index 78h D4 =0, D15-D2 are defined as the Programmable I/O Port Address A15-A2 for chip select signal PCSJ.
1-0 (2h)	00 : Compare A15-A2 for chip select signal PCSJ. (4 bytes). 01 : Compare A15-A3 for chip select signal PCSJ. (8 bytes). 10 : Disable. Chip select signal PCSJ is always inactive ('1'). 11 : Compare A15-A4 for chip select signal PCSJ. (16 bytes). These two bits define the compare byte count for the PCSJ address decode. When index 78h D4 =1, these two bits should be '11'.

Register Index : **58h**
Register Name : **IDEIC - IDE Interface Control**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	Reserved. (Must be read as 0)
6 (0b)	On-chip IDE Controller Enable/Disable. 0 : Disable. 1 : Enable. This bit is used to enable/disable on-chip IDE controller (M5229). When it is disabled, M5229 will become invisible by software.
5-4 (0h)	IDE IDSEL Address Select When Internal IDE Controller is Enable. 00 : A27. (default) 01 : A26. 10 : A25. 11 : A24. These two bits are used to select the IDSEL address for on-chip IDE controller. A27 is the default value and programmer can change the address by software for the system implementation flexibility.
3 (0b)	IDE ATA Secondary Bus Signals Pad Control. 0 : Disable, i.e. tri-state the secondary channel pins. 1 : Enable, i.e. internal IDE control it. This bit can be used to tri-state IDE ATA Secondary Bus signal. Some applications may use the ATA Secondary Bus signals wired together with other device signals. Then this bit can be used to swap the devices.
2 (0b)	IDE ATA Primary Bus Signals Pad Control. 0 : Disable, i.e. tri-state the primary channel pins. 1 : Enable, i.e. internal IDE control it. This bit can be used to tri-state IDE ATA Primary Bus signal. Some applications may use the ATA Primary Bus signals wired together with other device signals. Then this bit can be used to swap the devices.
1-0 (0h)	ATA Bus IDE Interrupt Connection Definition. (H/W connected on motherboard). Primary IRQ Secondary IRQ 00 : SIRQI SIRQII 01 : IRQ[14] IRQ[15] 10 : IRQ[14] SIRQII 11 : IRQ[14] SIRQI These two bits must correctively reflect the hardware implementaion regarding the IDE Interrupt connection. If SIRQI and SIRQII are selected for the IDE Interrupt connection, the following rules should be taken into consideration : 1. When IDE Native mode is enabled, "Primary" channel routing table is defined in the M1543C register Index-44h bits[3:0]. 2. When IDE Native mode is enabled, "Secondary" channel routing table is defined in the M1543C register Index-75h bits[3:0].

Register Index : **59h**
Register Name : **GPIS - General Purpose Input (GPI) Multiplexed Pin Select**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-4(0h)	Reserved.
3(0b)	Pin PCIREQJ/GPI[3] Function Select. 0 : PCIREQJ. 1 : GPI[3]. This bit is used to select the pin function for PCIREQJ/GPI[3]. Please refer to section 2.7 for more information.
2(0b)	Pin SERIRQ/GPI[2] Function Select. 0 : GPI[2]. 1 : SERIRQ. This bit is used to select the pin function for SERIRQ/GPI[2]. Please refer to section 2.7 for more information.
1(0b)	Reserved.
0(0b)	Pin OVCRJ/GPI[0] Function Select. 0 : OVCRJ. 1 : GPI[0]. This bit is used to select the pin function for OVCRJ/GPI[0]. Please refer to section 2.7 for more information.

Note : These pins will be power off when entering Suspend to DRAM or Suspend to Disk system state.

Register Index : **5B-5Ah**
Register Name : **GPOS - General Purpose Output (GPO) Multiplexed Pin Select**.
Attribute : Read/Write
Default Value : 0000h

Bit No.	Description
15-10(00h)	Reserved.
9-8(0h)	Pin SQWO/GPIOW/GPO[9] Function Select. 00 : SQWO. 01 : GPIOW. 10 : GPO[9]. 11 : GPO[9]. This bit is used to select the pin function for SQWO/GPIOW/GPO[9]. Please refer to section 1.4 & 2.5 for more information.
7-4(0h)	Reserved.
3(0b)	Pin PCI_STPJ/GPO[3] Function Select. 0 : PCI_STPJ. 1 : GPO[3]. This bit is used to select the pin function for PCI_STPJ/GPO[3]. Please refer to section 2.7 for more information.
2(0b)	Pin CPU_STPJ/GPO[2] Function Select. 0 : CPU_STPJ. 1 : GPO[2]. This bit is used to select the pin function for CPU_STPJ/GPO[2]. Please refer to section 2.7 for more information.
1(0b)	Pin ZZ/GPO[1] Function Select. 0 : ZZ. 1 : GPO[1]. This bit is used to select the pin function for ZZ/GPO[1]. Please refer to section 2.7 for more information.
0(0b)	Pin PCSJ/GPO[0] Function Select. 0 : PCSJ. 1 : GPO[0]. This bit is used to select the pin function for PCSJ/GPO[0]. Please refer to section 2.7 for more information.

Note: These pins will be power off when entering Suspend to DRAM or Suspend to Disk system state except SQWO/GPIOW/GPO[9].

Register Index : **5Dh-5Ch**
Register Name : **DMDC - Docking Mode Decode Control**.
Attribute : Read/Write
Default Value : 0000h

Bit No.	Description
15-10 (00h)	Reserved.
9 (0b)	I/O Group C Positive Decode Enable/Disable when Docking Mode is Enable. 0 : No response by the M1543C. 1 : Positive decode. The bit is a switch to enable the I/O Group C ports positive decode in docking mode. The decoding I/O ports addresses are defined in M7101 Register Index-A4h-A5h. If the PCI I/O address matches the defined address, this cycle will be positively decoded by the M1543C and not forward it to docking chip.
8-7 (0h)	Reserved.
6 (0b)	Parallel I/O Ports Positive Decode Enable/Disable when Docking Mode is Enable. 0 : No response by M1543C. 1 : Positive decode. The bit is a switch to enable the Parallel I/O ports positive decode in docking mode. The decoding I/O ports addresses are defined in M7101 Register Index-71h bit [5:0]. If the PCI I/O address matches the defined address, this cycle will be positively decoded by the M1543C and not forward it to docking chip.
5 (0b)	Keyboard I/O Ports Positive Decode Enable/Disable when Docking Mode is Enable. 0 : No response by M1543C. 1 : Positive decode. The bit is a switch to enable the Keyboard I/O ports positive decode in docking mode. The decoding I/O ports addresses are I/O address 60h and 64h. If the PCI I/O address matches the defined address, this cycle will be positively decoded by the M1543C and not forward it to docking chip.
4 (0b)	Serial I/O Ports Positive Decode Enable/Disable when Docking Mode is Enable. 0 : No response by M1543C. 1 : Positive decode. The bit is a switch to enable the Serial I/O ports positive decode in docking mode. The decoding I/O ports addresses are defined in M7101 Register Index-70h bit [7:0]. If the PCI I/O address matches the defined address, this cycle will be positively decoded by the M1543C and not forward it to docking chip.
3 (0b)	Floppy I/O Ports Positive Decode Enable/Disable when Docking Mode is Enable. 0 : No response by M1543C. 1 : Positive decode. The bit is a switch to enable the Floppy I/O ports positive decode in docking mode. The decoding I/O ports addresses are defined in M7101 Register Index-68h bit 0. If the PCI I/O address matches the defined address, this cycle will be positively decoded by the M1543C and not forward it to docking chip.
2 (0b)	Video I/O Ports Positive Decode Enable/Disable when Docking Mode is Enable. 0 : No response by M1543C. 1 : Positive decode. The bit is a switch to enable the Video I/O ports positive decode in docking mode. The decoding I/O ports addresses are from I/O address 3B0h to 3DFh. If the PCI I/O address matches the defined address, this cycle will be positively decoded by the M1543C and not forward it to docking chip.
1 (0b)	Audio I/O Ports Positive Decode Enable/Disablewhen Docking Mode is Enable. 0 : No response by M1543C. 1 : Positive decode. The bit is a switch to enable the Audio I/O ports positive decode in docking mode. The decoding I/O ports addresses are defined in M7101 Register Index-6Ch-6Dh bits [15:2]. If the PCI I/O address matches the defined address, this cycle will be positively decoded by the M1543C and not forward it to docking chip.
0 (0b)	Docking Mode Positive Decode Enable/Disable. 0 : Disable. 1 : Enable. When docking mode positive decode is disabled, all ports defined above are meaningless. The address will be substractive decode and forward to ISA bus behind the M1543C if no PCI card decodes as its own cycle. When docking mode positive decode is enabled, all ports defined above are positive decoded. The decoding address must be well programmed by software. If the address is not positively decoded by the M1543C, the cycle will forward to docking chip instead of the ISA bus behind the M1543C.

Register Index : **5Eh**
Register Name : **SMCCI - Suspend Mode Clock Control I**.
Attribute : Read/Write
Default Value : 00h

Bit	Description
7 (0b)	Stop USB PCICLK Enable/Disable when Entering Suspend Mode. 0 : Disable. USB PCICLK is still running during suspend mode. 1 : Enable. USB PCICLK is stopped during suspend mode. This bit is used to enable the USB PCICLK stop function during suspend mode to save more system power. It is not recommended to enable in Desktop applications.
6 (0b)	Stop ISP DMACLK Enable/Disable when Entering Suspend Mode. 0 : Disable. ISP DMACLK is still running during suspend mode. 1 : Enable. ISP DMACLK is stopped during suspend mode. This bit is used to enable the ISP DMACLK stop function during suspend mode to save more system power. It is not recommended to enable in Desktop applications.
5 (0b)	Stop ISP PCICLK Enable/Disable when Entering Suspend Mode. 0 : Disable. ISP PCICLK is still running during suspend mode. 1 : Enable. ISP PCICLK is stopped during suspend mode. This bit is used to enable the ISP PCICLK stop function during suspend mode to save more system power. It is not recommended to enable in Desktop applications.
4-1 (0h)	Reserved (must be "0000").
0 (0b)	Passive Release control during delayed transaction cycle. 0 : disable 1 : enable

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Register Index : **5Fh**
Register Name : **SMCCII - Suspend Mode Clock Control II**.
Attribute : Read/Write
Default Value : 00h

Bit	Description
7 (0b)	Stop Output SYSCLK Enable/Disable During Suspend Mode. 0 : Disable. SYSCLK is still running during suspend mode. 1 : Enable. SYSCLK is stopped during suspend mode. This bit is used to enable the SYSCLK stop function during suspend mode to save more system power. It is not recommended to enable in Desktop applications.
6 (0b)	Stop Internal KB Clock Enable/Disable During Suspend Mode. 0 : Disable. Internal Keyboard clock is still running during suspend mode. 1 : Enable. Internal Keyboard clock is stopped during suspend mode. This bit is used to enable the Keyboard Clock stop function during suspend mode to save more system power. It is not recommended to enable in Desktop applications.
5 (0b)	STOP AT CLOCK DIVIDER Enable/Disable During Suspend Mode. 0 : Disable. All AT clocks (including SYSCLK and KBCLK) are still running during suspend mode. 1 : Enable. All AT clocks (including SYSCLK and KBCLK) are stopped during suspend mode. This bit is used to enable the AT clocks stop function during suspend mode to save more system power. It is not recommended to enable in Desktop applications.
4 (0b)	Stop 14.318 MHz Clock of CLKRST Circuit Enable/Disable During Suspend Mode. 0 : Disable. The 119 KHz of M8254 and cold reset counter are still running during suspend mode. 1 : Enable. The 119 KHz of M8254 and cold reset counter are stopped during suspend mode. This bit is used to enable the 14.318 MHz clock stop function in CLKRST circuit during suspend mode to save more system power. It is not recommended to enable in Desktop applications.
3 (0b)	M1543C Register Index-04h Bits[9:4] Lock/Unlock Control. 0 : Lock. (cannot read/write) 1 : Unlock. (can read/write) When this bit is locked, the M1543C command register Index-04h bits[9:4] are read-only. When this bit is unlocked, these bits are writeable. Value 0 is recommended for some test programs which define those bits that must be read-only.
2 (0b)	On-chip PCI PMU Device M7101 Enable/Disable. 0 : Enable. 1 : Disable. When this bit is set to 1, M7101 will become invisible to software, and PMU (M7101) Configuration Registers Index 7Ch-FFh will be mapped to the M1543C Configuration Registers Index 7Ch-FFh. Software can program PMU function through the M1543C instead of M7101 when M7101 is disabled.
1-0 (0h)	Reserved. (Must be as 00)

Register Index : **6Ch-60h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **6Dh**
Register Name : **RAM - ROM Address Mapping**.
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	Float ISA Output Pads when entering Suspend Mode. 0 : Floating. 1 : Driving. This bit is used to control the ISA Pads Floating or Driving when entering Suspend Mode.
6 (0b)	Reserved (must be 0).
5 (0b)	ISA/DMA Master Cycle Retry, Release/Not Release PCI Bus. 0 : Not release. 1 : Release. This bit is used to control the PHOLDJ behaviour when the ISA/DMA Master cycle access is retried by the target (North Bridge). If this bit is set to 1, the M1543C will de-assert the PHOLDJ for 2 PCI clocks and then assert the PHOLDJ again to allow the PCI arbiter to grant the PCI bus to another PCI master. If this bit is reset as 0, the M1543C will keep asserting PHOLDJ until the ISA/DMA Master cycle is finished. Value 1 is recommended for normal operation.
4 (0b)	Super I/O FIR Mode Enable/Disable. 0 : Disable. Pins GPIO[3:0]/(CVROFF,IRRX, IRRXH, IRTX) are GPIO[3:0] when TC is pull-high. 1 : Enable. Pins GPIO[3:0]/(CVROFF,IRRX, IRRXH, IRTX) are CVROFF,IRRX, IRRXH, IRTX for FIR function when TC is pull-high. Please refer to section 1.4 for more information.
3-2 (0h)	On-Chip Arbiter Priority Assignment. 00 : Rotate mode. ISA->USB->IDE->D_DMA->ISA.... 01 : Fixed mode. ISA is the highest priority. If ISA is servicing, USB is highest priority for next arbitration. 10 : Fixed mode. USB is highest priority. USB->ISA->IDE->D_DMA. If USB is servicing, ISA is highest priority for next arbitration. 11 : Common Architecture mode and Rotate mode. ISA->USB->IDE->D_DMA->ISA....
1-0 (0h)	Output Pins BIOSA17, BIOSA16 Mapping when E0000-EFFFF Region is Accessed and ROM 256KB Mode Is Enabled. 00 : BIOSA17=1; BIOSA16=0. (default) 01 : BIOSA17=0; BIOSA16=1. 1x : BIOSA17=0; BIOSA16=0. These two bits are used to support ROM address mapping when 256KB ROM mode is enabled (pin SPLED is pulled low). When these two bits are programmed as 00, PCI address E-segment will map to ROM address E-segment. When these two bits are programmed as 01, PCI address E-segment will map to ROM address D-segment. When these two bits are programmed as 1x, PCI address E-segment will map to ROM address C-segment.

Register Index : **6Eh**
Register Name : **ISPSS - ISP Shadow I/O Port Select**
Attribute : Read/Write
Default Value : 00h
The following register is the preliminary index for accessing shadow ISP port data :

Bit No.	Description
7-5 (0h)	Select Device. 000 : Reserved. 001 : 8254 Programmable Timer. 010 : Master 8259. 011 : Slave 8259. 100 : Master 8237. 101 : Slave 8237. 110 : Reserved. 111 : Reserved. These three bits are used to select the access device.
4-0 (00h)	Select Device's Ports.
	<< If Master 8237 is selected.>> 0 0 0 0 0 Master-37 channel[0] Mode register. 0 0 0 0 1 Master-37 channel[1] Mode register. 0 0 0 1 0 Master-37 channel[2] Mode register. 0 0 0 1 1 Master-37 channel[3] Mode register. 0 0 1 0 0 Master-37 Request register & Mask register combined. 0 0 1 0 1 Master-37 channel[0] Base Address register Low byte. 0 0 1 1 0 Master-37 channel[0] Base Address register High byte. 0 0 1 1 1 Master-37 channel[0] Base Word Count register Low byte. 0 1 0 0 0 Master-37 channel[0] Base Word Count register High byte. 0 1 0 0 1 Master-37 channel[1] Base Address register Low byte. 0 1 0 1 0 Master-37 channel[1] Base Address register High byte. 0 1 0 1 1 Master-37 channel[1] Base Word Count register Low byte. 0 1 1 0 0 Master-37 channel[1] Base Word Count register High byte. 0 1 1 0 1 Master-37 channel[2] Base Address register Low byte. 0 1 1 1 0 Master-37 channel[2] Base Address register High byte. 0 1 1 1 1 Master-37 channel[2] Base Word Count register Low byte. 1 0 0 0 0 Master-37 channel[2] Base Word Count register High byte. 1 0 0 0 1 Master-37 channel[3] Base Address register Low byte. 1 0 0 1 0 Master-37 channel[3] Base Address register High byte. 1 0 0 1 1 Master-37 channel[3] Base Word Count register Low byte. 1 0 1 0 0 Master-37 channel[3] Base Word Count register High byte. Others : Reserved.

Bit No.	Description
	<< If Slave 8237 is selected.>> 0 0 0 0 0 Slave-37 channel[0] Mode register. 0 0 0 0 1 Slave-37 channel[1] Mode register. 0 0 0 1 0 Slave-37 channel[2] Mode register. 0 0 0 1 1 Slave-37 channel[3] Mode register. 0 0 1 0 0 Slave-37 Request register & Mask register combined. 0 0 1 0 1 Slave-37 channel[0] Base Address register Low byte. 0 0 1 1 0 Slave-37 channel[0] Base Address register High byte. 0 0 1 1 1 Slave-37 channel[0] Base Word Count register Low byte. 0 1 0 0 0 Slave-37 channel[0] Base Word Count register High byte. 0 1 0 0 1 Slave-37 channel[1] Base Address register Low byte. 0 1 0 1 0 Slave-37 channel[1] Base Address register High byte. 0 1 0 1 1 Slave-37 channel[1] Base Word Count register Low byte. 0 1 1 0 0 Slave-37 channel[1] Base Word Count register High byte. 0 1 1 0 1 Slave-37 channel[2] Base Address register Low byte. 0 1 1 1 0 Slave-37 channel[2] Base Address register High byte. 0 1 1 1 1 Slave-37 channel[2] Base Word Count register Low byte. 1 0 0 0 0 Slave-37 channel[2] Base Word Count register High byte. 1 0 0 0 1 Slave-37 channel[3] Base Address register Low byte. 1 0 0 1 0 Slave-37 channel[3] Base Address register High byte. 1 0 0 1 1 Slave-37 channel[3] Base Word Count register Low byte. 1 0 1 0 0 Slave-37 channel[3] Base Word Count register High byte. Others : Reserved.
	<< If Master 8259 is selected.>> 0 0 0 0 0 Master-59 ICW1. 0 0 0 0 1 Master-59 ICW2. 0 0 0 1 0 Master-59 ICW3. 0 0 0 1 1 Master-59 ICW4. 0 0 1 0 0 Master-59 OCW1. 0 0 1 0 1 Master-59 OCW2. 0 0 1 1 0 Master-59 OCW3. Others: Reserved.
	<< If Slave 8259 is selected.>> 0 0 0 0 0 Slave-59 ICW1. 0 0 0 0 1 Slave-59 ICW2. 0 0 0 1 0 Slave-59 ICW3. 0 0 0 1 1 Slave-59 ICW4. 0 0 1 0 0 Slave-59 OCW1. 0 0 1 0 1 Slave-59 OCW2. 0 0 1 1 0 Slave-59 OCW3. Others: Reserved.
	<< If 8254 is selected.>> 0 0 0 0 0 Counter[0] Low byte. 0 0 0 0 1 Counter[0] High byte. 0 0 0 1 0 Counter[1] Low byte. 0 0 0 1 1 Counter[1] High byte. 0 0 1 0 0 Counter[2] Low byte. 0 0 1 0 1 Counter[2] High byte. Others: Reserved.

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M8259's Supported Shadow I/O ports

	D7	D6	D5	D4	D3	D2	D1	D0
ICW1	0	0	0	1	0	0	SNGL	IC4
ICW2	A15/T7	A14/T6	A13/T5	A12/T4	A11/T3	A10	A9	A8
MICW3 (master)	0	0	0	0	0	1	0	0
SICW3 (slave)	0	0	0	0	0	0	1	0
ICW4	0	0	0	SFNM	0	0	AEOI	1
OCW1	M7	M6	M5	M4	M3	M2	M1	M0
OCW2	R	SL	EOI	0	0	0	0	0
OCW3	0	1	SMM	0	1	POLL	1	RIS

Register Index : **6Fh**
Register Name : **ISPSD - ISP Shadow I/O Select Port Data**
Attribute : Read only
Default Value : 00h
This register must be used with register Index-6Eh. Program the device and register first, and then the port data can be read by this register read.

Register Index : **70h**
Register Name : **SIRQCR - Serial IRQ (IRQSER) Control Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	Serial IRQ (IRQSER) Enable/Disable 0 : Disable. 1 : Enable. To enable the Serial IRQ, follow the programming sequences : 1. Program the M1543C Register Index-59h bit2 = 1 to select the pin SERIRQ/GPI[2] function as SERIRQ. 2. Program the M1543C Register Index-72h bit5 = 1 to enable the continuous mode repetition. 3. Program this bit to enable the Serial IRQ function.
6 (0b)	Stop Frame Pulse Width. (Quiet/Continuous Mode) 0 : 2 PCICLKs (Quiet Mode). 1 : 3 PCICLKs (Continuous Mode). This bit is used to program the Stop Frame pulse width. When this bit is reset to 0, the pulse width is 2 PCICLKs and the Quiet mode is selected. If this bit is set to 1, the pulse width is 3 PCICLKs and the Continuous mode is selected.
5-2(0000b)	Number of IRQ/Data Frames. 0000 : 17 Slots. 0001 : 18 Slots. 0010 : 19 Slots. 0011 : 20 Slots. 0100 : 21 Slots. (recommended for BIOS setting) 0101 : 22 Slots. 0110 : 23 Slots. 0111 : 24 Slots. 1000 : 25 Slots. 1001 : 26 Slots. 1010 : 27 Slots. 1011 : 28 Slots. 1100 : 29 Slots. 1101 : 30 Slots. 1110 : 31 Slots. 1111 : 32 Slots. These four bits are used to define the number of IRQ/Data Frame Slots (PCICLKs). 21 Slots are recommended for BIOS setting.
1-0(00b)	Start Frame Pulse Width. 00 : 4 PCICLKs. 01 : 6 PCICLKs. 10 : 8 PCICLKs. 11 : Reserved. These two bits are used to select the Start Frame pulse width from 4 PCICLKs to 8 PCICLKs. 8 PCICLKs are recommended when the M1543C resides in Primary PCI bus. For some special applications, when the M1543C does not reside in Primary PCI bus, 6 PCICLKs are recommended.

Register Index : **71h**
Register Name : **DDMAS - Distributed DMA Channel on PCI or ISA side.**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	DMA Channel 7 Device Location. 0 : DMA Device on ISA Slot. (default) 1 : DMA Device on PCI Slot. This bit is used to select the DMA Channel 7 device location. When this bit is set to 1, DMA Channel 7 device is on the PCI slot. Otherwise, it is on the ISA bus.
6 (0b)	DMA Channel 6 Device Location. 0 : DMA Device on ISA Slot. (default) 1 : DMA Device on PCI Slot. This bit is used to select the DMA Channel 6 device location. When this bit is set to 1, DMA Channel 6 device is on the PCI slot. Otherwise, it is on the ISA bus.
5 (0b)	DMA Channel 5 Device Location. 0 : DMA Device on ISA Slot. (default) 1 : DMA Device on PCI Slot. This bit is used to select the DMA Channel 5 device location. When this bit is set to 1, DMA Channel 5 device is on the PCI slot. Otherwise, it is on the ISA bus.
4 (0b)	Reserved.
3 (0b)	DMA Channel 3 Device Location. 0 : DMA Device on ISA Slot. (default) 1 : DMA Device on PCI Slot. This bit is used to select the DMA Channel 3 device location. When this bit is set to 1, DMA Channel 3 device is on the PCI slot. Otherwise, it is on the ISA bus.
2 (0b)	DMA Channel 2 Device Location. 0 : DMA Device on ISA Slot. (default) 1 : DMA Device on PCI Slot. This bit is used to select the DMA Channel 2 device location. When this bit is set to 1, DMA Channel 2 device is on the PCI slot. Otherwise, it is on the ISA bus.
1 (0b)	DMA Channel 1 Device Location. 0 : DMA Device on ISA Slot. (default) 1 : DMA Device on PCI Slot. This bit is used to select the DMA Channel 1 device location. When this bit is set to 1, DMA Channel 1 device is on the PCI slot. Otherwise, it is on the ISA bus.
0 (0b)	DMA Channel 0 Device Location. 0 : DMA Device on ISA Slot. (default) 1 : DMA Device on PCI Slot. This bit is used to select the DMA Channel 0 device location. When this bit is set to 1, DMA Channel 0 device is on the PCI slot. Otherwise, it is on the ISA bus.

Register Index : **72h**
Register Name : **USBIDS - USB IDSEL Mux Select**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	Routing Table IRQ Output Synchronization Enable/Disable. 0 : Disable. (Bypass) 1 : Enable. (Sync. by PCICLK) This bit is used to enable the synchronization for the routing table IRQ output. This function is for test pattern generation use only. Value 0 is recommended for normal operation.
6 (0b)	USB PWRENJ Output Via Pins GPIO[7] Enable/Disable. 0 : Disable. 1 : Enable. Please refer to section 1.4 for more detailed information.
5 (0b)	Repeat Serial IRQ Continuous Mode Enable/Disable. 0 : Disable. 1 : Enable. This bit is used to enable the Serial IRQ Continuous mode repetition. This bit must be enabled when Serial IRQ function is enabled. Please refer to the M1543C Register Index-70h bit7 description.
4 (0b)	Reserved.
3-2 (00b)	PMU (M7101) IDSEL Address Select. 00 : A28. (default) 01 : A29. 10 : A14. 11 : A15. These two bits are used to select the IDSEL address for on-chip PMU controller (M7101). A28 is the default value and programmer can change the address by software for system implementation flexibility.
1-0 (00b)	USB (M5237) IDSEL Address when internal USB is enabled. 00 : A31. (default) 01 : A30. 10 : A13. 11 : A12. These two bits are used to select the IDSEL address for on-chip USB controller. A31 is the default value and programmer can change the address by software for system implementation flexibility.

Register Index : **73h**
Register Name : **DDMABA - Distributed DMA Base Address**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-0 (00h)	Distributed DMA BASE Address. This register is used to define the Distributed DMA base address. All the access issued by the M1543C Distributed DMA function will add the base address to the PCI Audio card.

Register Index : **74h**
Register Name : **USBIR - USB Interrupt Routing Table**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	IOCHRDY driven case during DMA Cycle. 0 : IOCHRDY will be driven during DMA cycle. 1 : IOCHRDY will not be driven during DMA cycle. This bit is used to control the IOCHRDY signal during DMA cycle. When this bit is set to 1, the M1543C will not drive the IOCHRDY signal during DMA cycle. If this bit is reset as 0, the M1543C will drive the IOCHRDY signal out during DMA cycle when the command needs to add some wait state. Since it is not necessary to drive the IOCHRDY signal out during DMA cycle, value 1 is recommended for normal operation.
6 (0b)	The M1543C ISA Bridge & M7101 Subsystem Vendor ID and Subsystem Device ID (Index-2Ch-2Fh) Read/Write Control. 0 : Read/Write. 1 : Read Only. This bit is used to lock the M1543C & M7101 Register Index-2Ch-2Fh. Please refer to the M1543C and M7101 Index-2Ch-2Fh for more detailed information.
5 (0b)	Reserved.
4 (0b)	On-chip USB Master INTAJ Level to Edge Transform Enable/Disable. 0 : Disable. (bypass) 1 : Enable. (level -> edge) This bit is used to transfer the level of USB (M5237) Interrupt input signal. When this bit is set to 1, internal circuit will transfer the level to edge before connecting to 8259.
3-0 (0h)	On-chip USB Master Interrupt Routing Table. Bits 3-2-1-0 0 0 0 0 : Disable. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to route USB Master Interrupt to any 8259 Interrupt lines. The BIOS should inhibit to set the reserved value. The reserved setting will disable the IRQ at the present design.

Register Index : **75h**
Register Name : **IDENRII- IDE Native Mode Interrupt Routing II**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-5 (0h)	Reserved. (Read as '0')
4 (0b)	On-chip IDE Controller (M5229) Secondary Channel Interrupt Signal Transform Enable/Disable. 0 : Disable. (Bypass) 1 : Enable. (Level -> Edge) This bit is used to transfer the level of on-chip IDE controller (M5229) Secondary Channel Interrupt input signal. When this bit is set to 1, internal circuit will transfer the level to edge before connecting to 8259.
3-0 (0h)	On-chip IDE Controller (M5229) Secondary Channel Interrupt Routing When Native Mode is Enable. Bits 3-2-1-0 0 0 0 0 : Disable. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to decide on-chip IDE controller Secondary channel INTAJ routing table when native mode is enabled. It is recommended to connect IDE secondary channel Interrupt to pin SIRQII and use this table to route the interrupt to any available 8259 Interrupt lines. Please refer to the M1543C register Index-58h for more information.

Register Index : **76h**
Register Name : **SCIIR - PMU System Control Interrupt Routing Table**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	SCI Routing to IRQ[13] Enable/Disable. 0 : Enable. 1 : Disable. This bit is used to provide a mechanism to disable the SCI Interrupt. When this bit is set to 1 and the M1543C Register Index-76h bits[3:0] = 0h, SCI Interrupt will be disabled. Otherwise, SCI Interrupt will be decided by the M1543C Register Index-76h bits[3:0].
6-5 (0h)	Reserved.
4 (0b)	On-chip PMU System Control Interrupt (SCI) Level to Edge Transform Enable/Disable. 0 : Disable. (bypass) 1 : Enable. (level -> edge) This bit is used to transfer the level of PMU System Control Interrupt input signal (SCI). When this bit is set to 1, internal circuit will transfer the level to edge before connecting to 8259.
3-0 (0h)	On-chip PMU System Control Interrupt (SCI) Routing Table. Bits 3 -2 -1 -0 0 0 0 0 : IRQ[13]. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to route PMU System Control Interrupt (SCI) to any 8259 Interrupt lines. The BIOS should inhibit to set the reserved value. The reserved setting will disable the IRQ at the present design.

Register Index : **77h**
Register Name : **SMBIR - SMB Controller Event Interrupt Routing Table**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-5 (0h)	Reserved.
4 (0b)	On-chip SMB Controller Event Interrupt Level to Edge Transform Enable/Disable. 0 : Disable. (bypass) 1 : Enable. (level -> edge) This bit is used to transfer the level of SMB Control Event Interrupt input signal. When this bit is set to 1, internal circuit will transfer the level to edge before connecting to 8259.
3-0 (0h)	On-chip SMB Controller Event Interrupt Routing Table. Bits 3 -2 -1 -0 0 0 0 0 : Disable. 0 0 0 1 : IRQ[9]. 0 0 1 0 : IRQ[3]. 0 0 1 1 : IRQ[10]. 0 1 0 0 : IRQ[4]. 0 1 0 1 : IRQ[5]. 0 1 1 0 : IRQ[7]. 0 1 1 1 : IRQ[6]. 1 0 0 0 : IRQ[1]. 1 0 0 1 : IRQ[11]. 1 0 1 0 : Reserved. 1 0 1 1 : IRQ[12]. 1 1 0 0 : Reserved. 1 1 0 1 : IRQ[14]. 1 1 1 0 : Reserved. 1 1 1 1 : IRQ[15]. These four bits are used to route SMB Control Event Interrupt to any 8259 Interrupt lines. The BIOS should inhibit to set the reserved value. The reserved setting will disable the IRQ at the present design.

Register Index : **78h**
Register Name : **AGPIS - AGP Interrupt Selection**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-6 (00b)	Reserved
5 (0b)	IRQ Output Enable 0 : disable 1 : enable This is used for external IOAPIC. In a system with IOAPIC, all south bridge's internal IRQ signals should be connected to the IOAPIC. When this function is enabled, internal IRQ[0], IRQ[1], IRQ[12] are driven from SA[17], SA[18], SA[19] respectively. IRQ[3-7], IRQ[9-11], IRQ[14-15] become output signals to reflect the IRQs used by PCI INT and internal super I/O.
4 (0b)	APIC chip select (APICCSJ) enable 0 : disable 1 : enable APICCSJ is multiplexed with PCSJ. When APICCSJ is enabled, the function of PCSJ is disabled. The new definition of PCSJ configuration (CFG57h-55h) are redefined as follows : a. D1-D0 should be '11' b. D22-D21 should be '00' c. D15-D5 is the memory port address A15-A5 for APICCSJ This setting should be programmed before enabling this bit. For APICCSJ, the active memory region is defined as follows : a. A31-A16 is fixed as FEC0h b. A15-A5 is set in PCSJ configuration CFG 57h-55h D15-D5 c. A4-A0 don't care.
3-2 (00b)	Reserved.
1 (0b)	IRQ[12] Release ~~for AT KB~~ 0 : Do not release IRQ[12] 1 : Release IRQ[12] When this bit is set to 1, IRQ[12] will be released for ISA interrupt resource. When this bit is reset as 0, IRQ[12] will not be released even when only AT keyboard is used (PS2 mouse is not used). This bit must not be set to 1 when PS2 mouse is used. Otherwise, it will cause PS2 mouse interrupt to fail.
0 (0b)	AGP Interrupt Pins IRQ[14]/AGP_INTAJ, IRQ[15]/AGP_INTBJ function select. 0 : IRQ[14], IRQ[15] 1 : AGP_INTAJ, AGP_INTBJ

Register Index : **7Bh-79h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **FFh-7Ch**
Register Name : **MAPR - M7101 Mapping Register**
Attribute : Read/Write
Default Value : 00h

Note : When M7101 is disabled (M1543C Register Index-5Fh bit2 = 1), M7101 Configuration Register Index FFh-7Ch will map to these registers. BIOS can access these registers through the M1543C when M7101 is disabled.

4.1.2 IDE Master M5229 Configuration Registers (IDSEL = AD27 (default) , AD26, AD25, AD24)

The IDSEL can be changed by the M1543C Register Index-58h bits[5:4]. The following table shows the register summary :

Byte Index	Mnemonic	Definition	Attribute (R/W)	Default Value
01h-00h	VID	Vender ID	R	10B9h
03h-02h	DID	Device ID	R	5229h
05h-04h	COM	Command	R/W	0000h
07h-06h	DS	Status	R/W Clear	0280h
08h	RID	Revision ID	R	C1h
0Bh-09h	CC	Class Code	R/W	0101FAh
0Ch	Reserved	Reserved	R	00h
0Dh	LT	Latency Timer	R/W	00h
0Eh	HT	Header Type	R	00h
0Fh	Reserved	Reserved	R	00h
13h-10h	BAI	Base Address Register I	R/W	000001F1h
17h-14h	BAII	Base Address Register II	R/W	000003F5h
1Bh-18h	BAIII	Base Address Register III	R/W	00000171h
1Fh-1Ch	BAIV	Base Address Register IV	R/W	00000375h
23h-20h	BAV	Base Address Register V	R/W	0000F001h
2Dh-2Ch	SVID	Subsystem Vendor ID	R/W Lock	0000h
2Fh-2Eh	SDID	Subsystem Device ID	R/W Lock	0000h
3Bh-30h	Reserved	Reserved	R	00h
3Ch	IL	Interrupt Line	R/W	00h
3Dh	IP	Interrupt Pin	R	01h
3Eh	MG	Min_Gnt	R	02h
3Fh	ML	Max_Lat	R	04h
42h-40h	Reserved	Reserved	R	00h
43h	CCAI	Class Code Attribute I	R/W	00h
4Ah-44h	Reserved	Reserved	R	00h
4Bh	UT	Ultra DMA Test	R/W	4Ah
4Ch	Reserved	Reserved	R	00h
4Dh	CCAII	Class Code Attribute II	R/W	00h
4Fh-4Eh	Reserved	Reserved	R	1ABAh
50h	CCAIII	Class Code Attribute III	R/W	00h
51h	RAT	Reset And Testing	R/W	00h
52h	FCS	FCS	R/W	00h
53h	CDRC	CD_ROM Control	R/W	00h
54h	FTHP	FIFO Threshold of Primary Channel	R/W	55h
55h	FTHS	FIFO Threshold of Secondary Channel	R/W	55h
56h	UDMAP	Ultra DMA Setting for Primary Channel	R/W	44h
57h	UDMAS	Ultra DMA Setting for Secondary Channel	R/W	44h
58h	PCAS	Primary Channel Address Setup Timing	R/W	00h
59h	PCCB	Primary Channel Command Block Timing	R/W	00h
5Ah	PCDT0	Primary Channel Drive 0 Data Read/Write Timing	R/W	00h
5Bh	PCDT1	Primary Channel Drive 1 Data Read/Write Timing	R/W	00h
5Ch	SCAS	Secondary Channel Address Setup Timing	R/W	00h
5Dh	SCCB	Secondary Channel Command Block Timing	R/W	00h

Byte Index	Mnemonic	Definition	Attribute (R/W)	Default Value
5Eh	SCDT0	Secondary Channel Drive 0 Data Read/Write Timing	R/W	00h
5Fh	SCDT1	Secondary Channel Drive 1 Data Read/Write Timing	R/W	00h
76h-60h	Debug	Hardware Debug Registers	R	00h
77h	Reserved	Reserved	R	00h
78h	IDEC	IDE Clock Frequency	R/W	21h
FFh-79h	Reserved	Reserved	R	00h

Register Index : **01h-00h**
Register Name : **VID - Vendor ID Register**
Attribute : Read only
Default Value : 10B9h

Bit No.	Description
15-0 (10B9h)	This is a 16-bit value assigned to Acer Labs Inc. This register is combined with 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Register Index : **03h-02h**
Register Name : **DID - Device ID Register**
Attribute : Read only
Default Value : 5229h

Bit No.	Description
15-0 (5229h)	This register holds a unique 16-bit value assigned to a device, and combined with the vendor ID, it identifies any PCI device. Write to this register has no effect.

Register Index **05h-04h**
Register Name : **COM - Command Register**
Attribute : Read/Write
Default Value 0000h

Bit No.	Description
15-10(0h)	Reserved. These bits are always 0.
9(0b)	Back to Back Enable. M5229 only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
8(0b)	Enable the SERRJ driver. When this bit is set, M5229 will enable SERRJ output driver. This bit is reset to 0 and will set to 1 when it detects an address parity error. SERRJ is not asserted if this bit is 0.
7(0b)	Wait Cycle Control - M5229 does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
6(0b)	Respond to Parity Errors. If set to 1, M5229 will assert PERRJ when it is the agent receiving data AND it detects a data parity error. PERRJ is not asserted if this bit is 0.
5(0b)	Enable VGA Palette Snooping. This bit is always 0.
4(0b)	Memory Write and Invalidate Command. M5229 will never issue Memory Write and Invalidate commands. This bit is always 0. Write to this bit has no effect.
3(0b)	Enable Special Cycle. M5229 will not accept special cycles on PCI. This bit is always 0. Write to this bit has no effect.
2(0b)	Enable PCI Master. This bit is reset as 0 during Power-On to disable PCI master operations. This bit must be enabled for the normal IDE master operation.
1(0b)	Enable Response to Memory Access. M5229 will never respond to Memory access. This bit is always 0. Write to this bit has no effect.
0(0b)	Enable Response to I/O Access. This bit is reset as 0 during Power-On to disable the response to I/O access. This bit must be enabled for normal IDE I/O access.

Register Index : **07h-06h**
Register Name : **DS - Device Status Register**
Attribute : Read Only, Read/Write Clear
Default Value 0280h

Bit No.	Description
15(0b)	Detected Parity Error. This bit is set by M5229 to 1 whenever it detects a parity error, even if the Respond to Parity Errors bit (command register, bit 6) is disabled. This bit is cleared (reset to 0) by writing a 1 to it.
14(0b)	SERRJ Status. This bit is set by M5229 to 1 whenever it detects a PCI address parity error. This bit is cleared (reset to 0) by writing a 1 to it.
13(0b)	Received Master Abort Status. This bit is set to 1 when M5229, acting as a PCI master, aborts a PCI bus memory cycle. This bit is cleared (reset to 0) by writing a 1 to it.
12(0b)	Received Target Abort Status. This bit is set to 1 when an M5229 generated PCI cycle (M5229 is the PCI master) is aborted by a PCI target. This bit is cleared (reset to 0) by writing a 1 to it.
11(0b)	Sent Target Abort Status. M5229 as a slave never generates a Target abort. This bit is always 0.
10-9(01b)	DEVSELJ Timing. Read only bits indicating DEVSELJ timing when performing a positive decode. 00 : Fast. 01 : Medium. 10 : Slow. Since DEVSELJ is asserted by M5229 to meet the medium timing, these bits are encoded as 01b.
8(0b)	Data Parity Reported. Set to 1 if the Respond to Parity Error bit (Command Register bit 6) is set, and M5229 detects PERRJ asserted while acting as PCI master (whether PERRJ was driven by M5229 or not).
7(1b)	Fast Back-to-Back Capable. M5229 does support fast back-to-back transactions when the transactions are not to the same agent. This bit is always 1.
6-0(00h)	Reserved. These bits are always 0.

Register Index : **08h**
Register Name : **RID - Revision ID Register**
Attribute : Read only
Default Value : C1h

Bit No.	Description
7-0(C1h)	This register contains the version number of the M5229.

Register Index **0Bh-09h**
Register Name : **CC - Class Code Register**
Attribute : Read/Write
Default Value 0101FAh

Bit No.	Description
23-8(0101h)	Bits[23:8] identify the Base Class and Sub-Class Code of M5229. Value 0101h means IDE Controller.
7-0(FAh)	Bits[7:0] identify the Interface of M5229. Meaning of each bit is as follows:
7(1b)	Master or Slave IDE Device. 0 : Slave. 1 : Master. The M5229 is a Master IDE Device. This bit is always 1.
6(1b)	Does the Device support the Reporting of IDE Channel Status ? 0 : No, this is the default zero value of the PCI Specification 2.1. 1 : Yes, bit 4 and bit 5 can be used to determine the status of the IDE Channels. When this bit is reset as 0, bit 4 and bit 5 are meaningless from software point of view. If this bit is set to 1, bit 4 and bit 5 are meaningful and software can use these two bits to enable/disable Primary and Secondary Channel. Bits[6:4] are defined differently in PCI Specification 2.1 and Microsoft's proposal. The old SCT test program will define these three bits to be 0h and read only to compliant PCI Specification 2.1. But based on Microsoft's proposal, bit 4 and bit 5 are used by OS to disable/enable IDE Channel. For the old SCT issue, M5229 Register Index 43h or Index 4Dh bit 7 or Index 50h bit 1 are all usable to change the attribute and value for bits[6:4].
5(1b)	Enable/Disable IDE Primary Channel. 0 : Disable. 1 : Enable. This bit is used to disable or enable IDE Primary Channel no matter what the bit 6 value is. This bit must be set to 1 to enable IDE Primary Channel.
4(1b)	Enable/Disable IDE Secondary Channel. 0 : Disable. 1 : Enable. This bit is used to disable or enable IDE Secondary Channel no matter what bit 6's value is. This bit must be set to 1 to enable IDE Secondary Channel.
3(1b)	This bit indicates whether or not the Secondary Channel has a Fix Mode of Operation. 0 : Operation mode is fixed and is determined by the value of bit 2. 1 : Channel supports both modes and may be set to either mode by writing bit 2. The M5229 supports both modes defined in bit 2. This bit is always 1.
2(0b)	Secondary Channel Operation Mode. 0 : Compatible Mode. 1 : Native Mode. This bit is used to determine the operation mode for Secondary Channel.
1(1b)	This bit indicates whether or not the Primary Channel has a Fix Mode of Operation. 0 : Operation mode is fixed and is determined by the value of bit 0. 1 : Channel supports both modes and may be set to either mode by writing bit 0. The M5229 supports both modes defined in bit 0. This bit is always 1.
0(0b)	Secondary Channel Operation Mode. 0 : Compatible Mode. 1 : Native Mode. This bit is used to determine the operation mode for Primary Channel.

Register Index : **0Ch**
Register Name : **Reserved Register**
Attribute : Read Only
Default Value 00h

Register Index : **0Dh**
Register Name : **LT - Latency Timer**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-0(0h)	This register identifies the value of latency timer in PCI clocks for PCI bus master cycles.

Register Index : **0Eh**
Register Name : **HT - Header Type Register**
Attribute : Read only
Default Value 00h

Bit No.	Description
7-0(00h)	This register identifies the type of predefined header in the configuration space. Since M5229 is a single function device and not a PCI-to-PCI bridge, this byte should be read as 00h.

Register Index : **0Fh**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **13h-10h**
Register Name : **BA - Base Address Register I**
Attribute : Read/Write
Default Value : 000001F1h

Bit No.	Description
31-2 (0000007Ch)	Base Address. POST writes the value of the memory base address to this register.
1(0b)	Reserved. Always 0.
0(1b)	Always 1. Indicates that the operational registers are mapped into I/O space.

Register Index : **17h-14h**
Register Name : **BAII - Base Address Register II**
Attribute : Read/Write
Default Value : 000003F5h

Bit No.	Description
31-2 (000000FDh)	Base Address. POST writes the value of the memory base address to this register.
1(0b)	Reserved. Always 0.
0(1b)	Always 0. Indicates that the operational registers are mapped into memory space.

Register Index : **1Bh-18h**
Register Name : **BAIII - Base Address Register III**
Attribute : Read/Write
Default Value : 00000171h

Bit No.	Description
31-2 (0000005Ch)	Base Address. POST writes the value of the memory base address to this register.
1(0b)	Reserved. Always 0.
0(1b)	Always 1. Indicates that the operational registers are mapped into I/O space.

Register Index : **1Fh-1Ch**
Register Name : **BAIV - Base Address Register IV**
Attribute : Read/Write
Default Value : 00000375h

Bit No.	Description
31-2 (000000DDh)	Base Address. POST writes the value of the memory base address to this register.
1(0b)	Reserved. Always 0.
0(1b)	Always 1. Indicates that the operational registers are mapped into I/O space.

Register Index : **23h-20h**
Register Name : **BAV - Base Address Register V**
Attribute : Read/Write
Default Value : 0000F001h

Bit No.	Description
31-2 (00003C00h)	Base Address. POST writes the value of the memory base address to this register.
1(0b)	Reserved. Always 0.
0(1b)	Always 1. Indicates that the operational registers are mapped into I/O space.

Register Index : **2Bh-24h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index: **2Dh-02Ch**
Register Name: **SVID - Subsystem Vendor ID**
Attribute: Read/Write Lock
Default Value: 0000h

Bit	Description
15-0 (0000h)	If M5229 Register Index 53h bit7 = 0, then this register is Readable/Writeable. Else, this register is Read-Only. BIOS should program a value to this register and then lock it by setting M5229 Register Index 53h bit7 = 1.

Register Index : **2Fh-02Eh**
Register Name : **SDID - Subsystem Device ID**
Attribute : Read/Write Lock
Default Value : 0000h

Bit	Description
15-0 (0000h)	If M5229 Register Index 53h bit7 = 0, then this register is Readable/Writeable. Else, this register is Read-Only. BIOS should program a value to this register and then lock it by setting M5229 Register Index 53h bit7 = 1.

Register Index : **3Bh-30h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **3Ch**
Register Name : **IL - Interrupt Line Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-0(0h)	This register identifies which of the system interrupt controllers the devices interrupt pin is connected to. The value of this register is used by device drivers and has no direct meaning to M5229.

Register Index : **3Dh**
Register Name : **IP - Interrupt Pin Register**
Attribute : Read only
Default Value : 01h

Bit No.	Description
7-0(01h)	This register identifies which interrupt pin a device uses. Since M5229 uses INTAJ, this value is set to 01h.

Register Index **3Eh**
Register Name : **MG - Min Gnt Register**
Attribute : Read only
Default Value : 02h

Bit No.	Description
7-0(0h)	This register specifies the desired settings for how long a burst M5229 needs assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.

Register Index **3Fh**
Register Name : **ML - Max Lat Register**
Attribute : Read only
Default Value : 04h

Bit No.	Description
7-0(0h)	This register specifies the desired settings for how often the M1543C's USB needs access to the PCI bus assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.

Register Index : **42h-40h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **43h**
Register Name : **CCAI - Class Code Attribute Register I**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7(0b)	Reserved.
6 (0b)	Index 09h bit 6 Attribute. 0 : Read/Write. 1 : Read Only. This bit can be used to change the attribute of Index 09h bit 6. When this bit is reset as 0, Index 09h bit 6 can be read/write. If this bit is set to 1, Index 09h bit 6 can be read only.
5 (0b)	Index 09h bit 5 Attribute. 0 : Read/Write. 1 : Read Only. This bit can be used to change the attribute of Index 09h bit 5. When this bit is reset as 0, Index 09h bit 5 can be read/write. If this bit is set to 1, Index 09h bit 5 can be read only.
4 (0b)	Index 09h bit 4 Attribute. 0 : Read/Write. 1 : Read Only. This bit can be used to change the attribute of Index 09h bit 4. When this bit is reset as 0, Index 09h bit 4 can be read/write. If this bit is set to 1, Index 09h bit 4 can be read only.
3 (0b)	Index 09h bit 3 Attribute. 0 : Read/Write. 1 : Read Only. This bit can be used to change the attribute of Index 09h bit 3. When this bit is reset as 0, Index 09h bit 3 can be read/write. If this bit is set to 1, Index 09h bit 3 can be read only.
2 (0b)	Index 09h bit 2 Attribute. 0 : Read/Write. 1 : Read Only. This bit can be used to change the attribute of Index 09h bit 2. When this bit is reset as 0, Index 09h bit 2 can be read/write. If this bit is set to 1, Index 09h bit 2 can be read only.
1 (0b)	Index 09h bit 1 Attribute. 0 : Read/Write. 1 : Read Only. This bit can be used to change the attribute of Index 09h bit 1. When this bit is reset as 0, Index 09h bit 1 can be read/write. If this bit is set to 1, Index 09h bit 1 can be read only.
0 (0b)	Index 09h bit 0 Attribute. 0 : Read/Write. 1 : Read Only. This bit can be used to change the attribute of Index 09h bit 0. When this bit is reset as 0, Index 09h bit 0 can be read/write. If this bit is set to 1, Index 09h bit 0 can be read only.

Register Index : **4Ah-44h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **4Bh**
Register Name : **UT - Ultra DMA Test Register**
Attribute : Read/Write
Default Value : 4Ah
This bit is for Ultra DMA test only. Must not be programmed by BIOS.

Register Index : **4Ch**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **4Dh**
Register Name : **CCA - Class Code Attribute Register II**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7 (0b)	Programming M5229 Register Index 09h Class Code bits[6:4] R/W or Read Only. 0 : Read/Write. 1 : Read Only. This bit is used to control the attribute of M5229 Register Index 09h bits[6:4]. These three bits are defined as reserved bits in PCI 2.1 specification and some old SCT test program will define these three bits as read-only. So, this bit can be set to 1 by BIOS to comply with the PCI 2.1 specification. Since current SCT test program has no longer defined these three bits as read only. Value 0 is recommended for normal operation.
6-0 (00h)	Reserved.

Register Index : **4Fh-4Eh**
Register Name : **Reserved**
Attribute : Read Only
Default Value : 1ABAh

Register Index : **50h**
Register Name : **CCAIII - Class Code Attribute Register III**
Attribute : Read/Write
Default Value : 02h

Bit No.	Description
7-6 (0h)	Reserved.
5(0b)	Decoding Methods for the third byte of BAII and BAIV during Native Mode. 0 : All 4 bytes are master IDE's cycle. (default) 1 : Only the 3rd byte is master IDE's cycle. This bit is used to control the internal decoding methods for the third byte of BAII and BAIV registers during native mode. When this bit is reset as 0, all the four bytes defined by the Base Address Register II (M5229 Index 17h-14h) and Base Address Register IV (M5229 Index 1Fh-1Ch) will decode as M5229 cycle and pass on to the ATA bus. If this bit is set to 1, only the third byte will decode as M5229 cycle and pass on to the ATA bus.
4(0b)	Reserved.
3(0b)	Decoding Method for I/O Address 3F6h and 376h. 0 : Decode 3F6h and 376h that only uses address. 1 : Use byte enable decoding. This bit is used to control the internal decoding method for I/O ports 3F6h and 376h. When this bit is reset as 0, M5229 will decode only the PCI AD address and ignore the byte enable signals. If this bit is set to 1, M5229 will not ignore the byte enable signals, which means, only CBEJ[2] = 0 will decode as IDE 3F6h and 376h cycles.
2(0b)	Reserved.
1(1b)	Index 09h Bits[6:4] Programming Interface. 0 : Return 000b during read. 1 : Return the real contents. Since the old SCT program defined Index 09h bits[6:4] as reserved and the value must be 000b, this bit can be reset as 0 to meet the request. For Microsoft proposal and normal operation, this bit needs to set to 1 to allow hardware to reflect the real contents. Software can enable/disable IDE Channel based on the real value.
0(0b)	Enable Internal IDE Function. 0 : Disable(default). 1 : Enable. This bit is used to enable the internal M5229 IDE function. This bit has the same effect as M1543C Register Index 58h bit 6. If IDE function is disable, this device will become invisible from the software and hardware point of view.

Register Index : **51h**
Register Name : **RAT - Reset and Testing Register**
Attribute : Read/Write
Default Value : 00h
This register is for the testing purpose only. It should not be programmed by BIOS in normal operation.

Bit No.	Description
7(0b)	CFG_CHIPRST, Chip Reset. Writing a '1' to this bit will reset the whole chip as hardware reset. It generates a one cycle pulse only.
6(0b)	CFG_SOFTRST, Soft Reset. Writing a '1' to this bit will reset all the blocks except the configuration space. It generates a one cycle pulse only.
5(0b)	CFG_RSTCH2, Soft Reset. Writing a '1' to this bit will reset the ATASTATE (ATA State Machine) and AUTOPOL2 (PIO Mode State Machine). It generates a one cycle pulse only.
4(0b)	CFG_RSTCH1, Soft Reset. Writing a '1' to this bit will reset the ATASTATE (ATA State Machine) and AUTOPOL1 (PIO Mode State Machine). It generates a one cycle pulse only.
3(0b)	Reserved.
2(0b)	CFG_ATA_TEST, Auto Polling Test Mode Enable. 0 : Disable.(default) 1 : Enable. Writing a '1' to this bit will enable the Auto Polling test mode.
1(0b)	CFG_LATEST, Latency Timer Test Mode Enable. 0 : Disable.(default) 1 : Enable. Writing a '1' to this bit will enable the Latency Timer test mode.
0(0b)	CFG_FIFO_TEST, FIFO Test Mode Enable. 0 : Disable.(default) 1 : Enable. Writing a '1' to this bit will enable the FIFO test mode.

Register Index : **52h**
Register Name : **FCS - Flexible Channel Setting Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7(0b)	Exchange the two Hard Drives. 0: Primary Channel is Master IDE and Secondary Channel is Slave IDE when configuring the two channels to the same channel. (default) 1: Secondary Channel is Master IDE and Primary Channel is Slave IDE when configuring the two channels to the same channel. This bit is used with bit6 and bit5 to redefine which IDE drive is master or slave. BIOS can utilize these three bits to easily change the booting device.
6(0b)	Configure the two Channels to Secondary Channel. 0: Supports two channel IDE controller. One is Primary Channel and the other is Secondary Channel. (default) 1: The two channels all belong to Secondary Channel and each channel only supports one Hard Drive. One channel is defined as Master drive and the other is Slave drive. The two channels devices can be exchanged by bit 7 setting.
5(0b)	Configure the two Channels to Primary Channel. 0: Supports two channel IDE controller. One is Primary Channel and the other is Secondary Channel. (default) - 1: Both channels belong to Primary Channel and each channel only supports one HDD. One channel is defined as Master drive and the other is Slave drive. The two-channel device can be exchanged by bit 7 setting.
4(0b)	Exchanging the two Channels. 0: Channel one is primary channel and channel two is secondary channel. (default) 1: Channel two is primary channel and channel one is secondary channel. This bit is used to exchange the two channels for some applications. For example, BIOS can easily choose the booting device by using bits[7:4] programming.
3(0b)	Select Data Transfer Timing for Drive 0 (Master Drive) of Primary Channel. 0: Use M5229 Register Index 5Ah for data transfer timing. (default) 1: Use M5229 Register Index 59h (Command Block Timing Register) for data transfer timing. This bit can be used by software for other special applications.
2(0b)	Select Data Transfer Timing for Drive 1 (Slave Drive) of Primary Channel. 0: Use M5229 Register Index 5Bh for data transfer timing. (default) 1: Use M5229 Register Index 59h (Command Block Timing Register) for data transfer timing. This bit can be used by software for other special applications.
1(0b)	Select Data Transfer Timing for Drive 0 (Master Drive) of Secondary Channel. 0: Use M5229 Register Index 5Eh for data transfer timing. (default) 1: Use M5229 Register Index 5Dh (Command Block Timing Register) for data transfer timing. This bit can be used by software for other special applications.
0(0b)	Select Data Transfer Timing for Drive 1 (Slave Drive) of Secondary Channel. 0: Use M5229 Register Index 5Fh for data transfer timing. (default) 1: Use M5229 Register Index 5Dh (Command Block Timing Register) for data transfer timing. This bit can be used by software for other special applications.

Register Index : **53h**
Register Name : **CDRC - CD_ROM Control Register**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7(0b)	Sub_System Vendor and Device ID Registers (M5229 Register Index 2Fh-2Ch) Attribute Control. 0 : Read/Write. 1 : Read Only. This bit is used to control the attribute of M5229 Register Index 2Fh-2Ch. BIOS can use this bit to lock the content of Subsystem Vendor and Device ID Registers. Value 1 is suggested for some SCT test program.
6-4(0h)	Reserved.
3(0b)	Mask Base Address During Compatibility Mode. 0 : Unmask 1 : Mask (return 00h). This bit is used to mask the contents as 00h in M5229 Registers Index 1Fh-10h (Based Address Register I to IV). During compatibility mode (defined by Index 09h bit 2 and bit 0), some SCT test program will require the contents in Base Address Registers to be 00h. Value 1 is recommended for the setting to meet the SCT test program requirement.')
2(0b)	Reserved.
1(0b)	CD_ROM FIFO Operation in PIO Mode. 0 : Utilize the internal FIFO if the operation level is program as PIO mode in Index 54h-55h for CD_ROM device. (default) 1 : Disable the internal FIFO if the operation level is program as PIO mode in Index 54h-55h for CD_ROM device. When this bit is set to 1, M5229 will be forced to disable the hardware FIFO for the CD_ROM and ignore the PIO mode setting in Index 54h-55h. If this bit is reset as 0 and Index 54h-55h has defined the operation level as PIO mode, and the internal FIFO will be enabled for CD_ROM device. Value 0 is recommended in normal operation. This bit is only useful for the CD_ROM PIO mode setting. Bit 0 is combined with Index 56h-57h to program CD_ROM DMA and Ultra DMA mode.
0(0b)	Supports CD_ROM DMA Mode. 0 : Disable. (default) 1 : Enable. This bit is used to enable the CD_ROM DMA or Ultra DMA mode. When this bit is reset as 0, M5229 will only support PIO mode for CD_ROM device and bit 1 and Index 54h-55h operation level will decide FIFO on/off. If this bit is set to 1, CD_ROM will support DMA mode for CD_ROM when Index 56h-57h Ultra DMA feature is not enabled. If this bit is set to 1 and Index 56h-57h Ultra DMA feature is enabled, CD_ROM will support Ultra DMA mode for CD_ROM.

Register Index : **54h**
Register Name : **FTHP - FIFO Threshold of Primary Channel Drive 0 and Drive 1**
Default Value : Read/Write
Default Value : 55h

Bit No.	Description
7-6(01b)	Operation level. Defines the Operation Level of Primary Channel Drive 1. 00 : PIO mode and FIFO off. 01 : PIO mode. 10 : DMA mode. 11 : PIO master mode. Operation level is used to define the ATA bus operation mode. 00 is the only setting to disable internal FIFO. Other modes will enable internal FIFO. 11 is a special mode supported by M5229. In this mode, ATA bus will run the PIO mode, but M5229 will act as a PCI master to access the DRAM. This mode is special but BIOS must not set to this mode.
5-4(01b)	FIFO Threshold Register. Defines when to Start Master Transaction of Primary Channel Drive 1. 00 : 4 WORDs. 01 : 8 WORDs. 10 : 16 WORDs. 11 : 24 WORDs. This FIFO threshold is only meaningful for DMA, PIO master, and Ultra DMA modes. M5229 will act like a PCI master during these modes. Thresh value is used to control the start point for PCI master transaction. It can divide into two different actions. First of all, for ATA read and PCI master write behaviour, ATA bus will keep prefetching data ahead from Hard Disk Drive, and M5229 will only issue the PCI master write cycle when the FIFO available data count is greater than the threshold value. Secondly, for PCI master read and ATA write behaviour, M5229 will start to prefetch the data from DRAM when the FIFO available data count is smaller than the threshold value.
3-2(01b)	Operation level. Defines the Operation Level of Primary Channel Drive 0. 00 : PIO mode and FIFO off. 01 : PIO mode. 10 : DMA mode. 11 : PIO master mode. Operation level is used to define the ATA bus operation mode. 00 is the only setting to disable internal FIFO. Other modes will enable internal FIFO. 11 is a special mode supported by M5229. In this mode, ATA bus will run the PIO mode, but M5229 will act as a PCI master to access the DRAM. This mode is special and BIOS must not set to this mode.
1-0(01b)	FIFO threshold register. Defines when to Start Master Transaction of Primary Channel Drive 0. 00 : 4 WORDs. 01 : 8 WORDs. 10 : 16 WORDs. 11 : 24 WORDs. This FIFO threshold is only meaningful for DMA, PIO master, and Ultra DMA modes. M5229 will act like a PCI master during these modes. Thresh value is used to control the start point for PCI master transaction. It can divide into two different actions. First of all, for ATA read and PCI master write behaviour, ATA bus will keep prefetching data ahead from Hard Disk Drive, and M5229 will only issue the PCI master write cycle when the FIFO available data count is greater than the threshold value. Secondly, for PCI master read and ATA write behaviour, M5229 will start to prefetch the data from DRAM when the FIFO available data count is smaller than the threshold value.

Register Index : **55h**
Register Name : **FTHS - FIFO Threshold of Secondary Channel Drive 0 And Drive 1**
Attribute : Read/Write
Default Value : 55h

Bit No.	Description
7-6(01b)	Operation level. Defines the Operation Level of Secondary Channel Drive 1. 00 : PIO mode and FIFO off. 01 : PIO mode. 10 : DMA mode. 11 : PIO master mode. Operation level is used to define the ATA bus operation mode. 00 is the only setting to disable internal FIFO. Other modes will enable internal FIFO. 11 is a special mode supported by M5229. In this mode, ATA bus will run the PIO mode, but M5229 will act as a PCI master to access the DRAM. This mode is special but BIOS must not set to this mode.
5-4(01b)	FIFO Threshold Register. Defines When to Start Master Transaction of Secondary Channel Drive 1. 00 : 4 WORDs. 01 : 8 WORDs. 10 : 16 WORDs. 11 : 24 WORDs. This FIFO threshold is only meaningful for DMA, PIO master, and Ultra DMA modes. M5229 will act like a PCI master during these modes. Thresh value is used to control the start point for PCI master transaction. It can divide into two different actions. First of all, for ATA read and PCI master write behaviour, ATA bus will keep prefetching data ahead from Hard Disk Drive, and M5229 will only issue the PCI master write cycle when the FIFO available data count is greater than the threshold value. Secondly, for PCI master read and ATA write behaviour, M5229 will start to prefetch the data from DRAM when the FIFO available data count is smaller than the threshold value.
3-2(01b)	Operation level. Defines the Operation Level of Secondary Channel Drive 0. 00 : PIO mode and FIFO off. 01 : PIO mode. 10 : DMA mode. 11 : PIO master mode. Operation level is used to define the ATA bus operation mode. 00 is the only setting to disable internal FIFO. Other modes will enable internal FIFO. 11 is a special mode supported by M5229. In this mode, ATA bus will run the PIO mode, but M5229 will act as a PCI master to access the DRAM. This mode is special but BIOS must not set to this mode.
1-0(01b)	FIFO threshold register. Defines when to Start Master Transaction of Secondary Channel Drive 0. 00 : 4 WORDs. 01 : 8 WORDs. 10 : 16 WORDs. 11 : 24 WORDs. This FIFO threshold is only meaningful for DMA, PIO master, and Ultra DMA modes. M5229 will act like a PCI master during these modes. Thresh value is used to control the start point for PCI master transaction. It can divide into two different actions. First of all, for ATA read and PCI master write behaviour, ATA bus will keep prefetching data ahead from Hard Disk Drive, and M5229 will only issue the PCI master write cycle when the FIFO available data count is greater than the threshold value. Secondly, for PCI master read and ATA write behaviour, M5229 will start to prefetch the data from DRAM when the FIFO available data count is smaller than the threshold value.

Register Index : **56h**
Register Name : **UDMAP - Ultra DMA /33 Setting for Primary Channel Drive 0 and Drive 1**
Attribute : Read/Write
Default Value : 44h

Bit No.	Description
7(0b)	Enable Primary Channel Device 1 for Ultra DMA/33. 0: Disable. 1: Enable. This bit is used to enable the Ultra DMA mode for Primary Channel Device 1. When this bit is set to 1, the operation level defined in Index 54h bits[7:6] will be ignored by M5229, and will support Ultra DMA mode for Primary Channel Device 1.
6-4(0h)	Ultra DMA/33 Cycle Time for Primary Channel Device 1. 000 : Reserved. 001 : 1.5T. 010 : 2T. (mode 2) 011 : 3T. (mode1) 100 : 4T. (mode 0) 101 : 2.5T. 110 : 6T. 111 : 3.5T. These three bits are used to program the cycle time for Primary Channel Device 1 when Ultra DMA mode is set by bit 7. These three bits are meaningless when bit 7 is reset as 0. T is defined by the PCI clock cycle time. BIOS can use the different values to meet different Ultra DMA modes (from mode 2 to mode 0).
3(0b)	Enable Primary Channel Device 0 for Ultra DMA/33. 0 : Disable. 1 : Enable. This bit is used to enable the Ultra DMA mode for Primary Channel Device 0. When this bit is set to 1, the operation level defined in Index 54h bits[3:2] will be ignored by M5229, and will support Ultra DMA mode for Primary Channel Device 0.
2-0(0h)	Ultra DMA/33 Cycle Time for Primary Channel Device 0. 000 : Reserved. 001 : 1.5T. 010 : 2T. (mode 2) 011 : 3T. (mode1) 100 : 4T. (mode 0) 101 : 2.5T. 110 : 6T. 111 : 3.5T. These three bits are used to program the cycle time for Primary Channel Device 0 when Ultra DMA mode is set by bit 3. These three bits are meaningless when bit 3 is reset as 0. T is defined by the PCI clock cycle time. BIOS can use the different values to meet different Ultra DMA modes (from mode 2 to mode 0).

Register Index : **57h**
Register Name : **UDMAS - Ultra DMA /33 Setting for Secondary Channel Drive 0 And Drive 1**
Attribute : Read/Write
Default Value : 44h

Bit No.	Description
7(0b)	Enable Secondary Channel Device 1 for Ultra DMA/33. 0: Disable. 1: Enable. This bit is used to enable the Ultra DMA mode for Secondary Channel Device 1. When this bit is set to 1, the operation level defined in Index 55h bits[7:6] will be ignored by M5229, and will support Ultra DMA mode for Secondary Channel Device 1.
6-4(0h)	Ultra DMA/33 Cycle Time for Secondary Channel Device 1. 000 : Reserved. 001 : 1.5T. 010 : 2T. (mode 2) 011 : 3T. (mode1) 100 : 4T. (mode 0) 101 : 2.5T. 110 : 6T. 111 : 3.5T. These three bits are used to program the cycle time for Secondary Channel Device 1 when Ultra DMA mode is set by bit 7. These three bits are meaningless when bit 7 is reset as 0. T is defined by the PCI clock cycle time. BIOS can use the different values to meet different Ultra DMA modes (from mode 2 to mode 0).
3(0b)	Enable Secondary Channel Device 0 for Ultra DMA/33. 0: Disable. 1: Enable. This bit is used to enable the Ultra DMA mode for Secondary Channel Device 0. When this bit is set to 1, the operation level defined in Index 55h bits[3:2] will be ignored by M5229, and will support Ultra DMA mode for Secondary Channel Device 0.
2-0(0h)	Ultra DMA/33 Cycle Time for Secondary Channel Device 0. 000 : Reserved. 001 : 1.5T. 010 : 2T. (mode 2) 011 : 3T. (mode1) 100 : 4T. (mode 0) 101 : 2.5T. 110 : 6T. 111 : 3.5T. These three bits are used to program the cycle time for Secondary Channel Device 0 when Ultra DMA mode is set by bit 3. These three bits are meaningless when bit 3 is reset as 0. T is defined by the PCI clock cycle time. BIOS can use the different values to meet different Ultra DMA modes (from mode 2 to mode 0).

Register Index : **58h**
Register Name : **PCAS - Primary Channel Address Setup Timing Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-3(0h)	Reserved.
2-0(0h)	Address Setup Timing Count for Primary Channel. 000 : 8 clks. (default) 001 : 1 clk. 010 : 2 clks. 011 : 3 clks. 100 : 4 clks. 101 : 5 clks. 110 : 6 clks. 111 : 7 clks. These three bits are used to program the address setup time count for Primary Channel. Clock defined by PCI clock cycle time. The setting value will take effect for command and data access.

Register Index : **59h**
Register Name : **PCCB - Primary Channel Command Block Timing Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7(0b)	Reserved.
6-4(0h)	Command Active Count. 000 : 8 clks. (default) 001 : 1 clk. 010 : 2 clks. 011 : 3 clks. 100 : 4 clks. 101 : 5 clks. 110 : 6 clks. 111 : 7 clks. These three bits are used to program the command block active timing count for Primary Channel. Clock is defined by PCI clock cycle time. The setting value will take effect for command block access only.
3-0(0h)	Command Recovery Count. 0000 : 16 clks. (default) 0001 : 1 clk. 0010 : 2 clks. 0011 : 3 clks. 0100 : 4 clks. 0101 : 5 clks. 0110 : 6 clks. 0111 : 7 clks. 1000 : 8 clks. 1001 : 9 clks. 1010 : 10 clks. 1011 : 11 clks. 1100 : 12 clks. 1101 : 13 clks. 1110 : 14 clks. 1111 : 15 clks. These four bits are used to program the command block recovery timing count for Primary Channel. Clock is defined by PCI clock cycle time. The setting value will take effect for command block access only.

Register Index : **5Ah**
Register Name : **PCDT0 - Primary Channel Drive 0 Data Read/Write Timing Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7(0b)	Reserved.
6-4(0h)	Data Read/Write Active Count. 000 : 8 clks. (default) 001 : 1 clk. 010 : 2 clks. 011 : 3 clks. 100 : 4 clks. 101 : 5 clks. 110 : 6 clks. 111 : 7 clks. These three bits are used to program the data read/write active timing count for Primary Channel Drive 0. Clock is defined by PCI clock cycle time. The setting value will take effect for Primary Channel Drive 0 data access only.
3-0(0h)	Data Read/Write Recovery Count. 0000 : 16 clks. (default) 0001 : 1 clk. 0010 : 2 clks. 0011 : 3 clks. 0100 : 4 clks. 0101 : 5 clks. 0110 : 6 clks. 0111 : 7 clks. 1000 : 8 clks. 1001 : 9 clks. 1010 : 10 clks. 1011 : 11 clks. 1100 : 12 clks. 1101 : 13 clks. 1110 : 14 clks. 1111 : 15 clks. These four bits are used to program the data read/write recovery timing count for Primary Channel Drive 0. Clock is defined by PCI clock cycle time. The setting value will take effect for Primary Channel Drive 0 data access only.

Register Index : **5Bh**
Register Name : **PCDT1 - Primary Channel Drive 1 Data Read/Write Timing Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7(0b)	Reserved.
6-4(0h)	Data Read/Write Active Count. 000 : 8 clks. (default) 001 : 1 clk. 010 : 2 clks. 011 : 3 clks. 100 : 4 clks. 101 : 5 clks. 110 : 6 clks. 111 : 7 clks. These three bits are used to program the data read/write active timing count for Primary Channel Drive 1. Clock is defined by PCI clock cycle time. The setting value will take effect for Primary Channel Drive 1 data access only.
3-0(0h)	Data Read/Write Recovery Count. 0000 : 16 clks. (default) 0001 : 1 clk. 0010 : 2 clks. 0011 : 3 clks. 0100 : 4 clks. 0101 : 5 clks. 0110 : 6 clks. 0111 : 7 clks. 1000 : 8 clks. 1001 : 9 clks. 1010 : 10 clks. 1011 : 11 clks. 1100 : 12 clks. 1101 : 13 clks. 1110 : 14 clks. 1111 : 15 clks. These four bits are used to program the data read/write recovery timing count for Primary Channel Drive 1. Clock is defined by PCI clock cycle time. The setting value will take effect for Primary Channel Drive 1 data access only.

Register Index : **5Ch**
Register Name : **SCAS - Secondary Channel Address Setup Timing Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-3(0h)	Reserved.
2-0(0h)	Address Setup Timing Count for Secondary Channel. 000 : 8 clks. (default) 001 : 1 clk. 010 : 2 clks. 011 : 3 clks. 100 : 4 clks. 101 : 5 clks. 110 : 6 clks. 111 : 7 clks. These three bits are used to program the address setup time count for Secondary Channel. Clock is defined by PCI clock cycle time. The setting value will take effect for command and data access.

Register Index : **5Dh**
Register Name : **SCCB - Secondary Channel Command Block Timing Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7(0b)	Reserved.
6-4(0h)	Command Active Count. 000 : 8 clks. (default) 001 : 1 clk. 010 : 2 clks. 011 : 3 clks. 100 : 4 clks. 101 : 5 clks. 110 : 6 clks. 111 : 7 clks. These three bits are used to program the command block active timing count for Secondary Channel. Clock is defined by PCI clock cycle time. The setting value will take effect for command block access only.
3-0(0h)	Command Recovery Count. 0000 : 16 clks. (default) 0001 : 1 clk. 0010 : 2 clks. 0011 : 3 clks. 0100 : 4 clks. 0101 : 5 clks. 0110 : 6 clks. 0111 : 7 clks. 1000 : 8 clks. 1001 : 9 clks. 1010 : 10 clks. 1011 : 11 clks. 1100 : 12 clks. 1101 : 13 clks. 1110 : 14 clks. 1111 : 15 clks. These four bits are used to program the command block recovery timing count for Secondary Channel. Clock is defined by PCI clock cycle time. The setting value will take effect for command block access only.

Register Index : **5Eh**
Register Name : **SCDT0 - Secondary Channel Drive 0 Data Read/Write Timing Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7(0b)	Reserved.
6-4(0h)	Data Read/Write Active Count. 000 : 8 clks. (default) 001 : 1 clk. 010 : 2 clks. 011 : 3 clks. 100 : 4 clks. 101 : 5 clks. 110 : 6 clks. 111 : 7 clks. These three bits are used to program the data read/write active timing count for Secondary Channel Drive 0. Clock is defined by PCI clock cycle time. The setting value will take effect for Secondary Channel Drive 0 data access only.
3-0(0h)	Data Read/Write Recovery Count. 0000 : 16 clks. (default) 0001 : 1 clk. 0010 : 2 clks. 0011 : 3 clks. 0100 : 4 clks. 0101 : 5 clks. 0110 : 6 clks. 0111 : 7 clks. 1000 : 8 clks. 1001 : 9 clks. 1010 : 10 clks. 1011 : 11 clks. 1100 : 12 clks. 1101 : 13 clks. 1110 : 14 clks. 1111 : 15 clks. These four bits are used to program the data read/write recovery timing count for Secondary Channel Drive 0. Clock is defined by PCI clock cycle time. The setting value will take effect for Secondary Channel Drive 0 data access only.

Register Index : **5Fh**
Register Name : **SCDT1 - Secondary Channel Drive 1 Data Read/Write Timing Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7(0b)	Reserved.
6-4(0h)	Data Read/Write Active Count. 000 : 8 clks. (default) 001 : 1 clk. 010 : 2 clks. 011 : 3 clks. 100 : 4 clks. 101 : 5 clks. 110 : 6 clks. 111 : 7 clks. These three bits are used to program the data read/write active timing count for Secondary Channel Drive 1. Clock is defined by PCI clock cycle time. The setting value will take effect for Secondary Channel Drive 1 data access only.
3-0(0h)	Data Read/Write Recovery Count. 0000 : 16 clks. (default) 0001 : 1 clk. 0010 : 2 clks. 0011 : 3 clks. 0100 : 4 clks. 0101 : 5 clks. 0110 : 6 clks. 0111 : 7 clks. 1000 : 8 clks. 1001 : 9 clks. 1010 : 10 clks. 1011 : 11 clks. 1100 : 12 clks. 1101 : 13 clks. 1110 : 14 clks. 1111 : 15 clks. These four bits are used to program the data read/write recovery timing count for Secondary Channel Drive 1. Clock is defined by PCI clock cycle time. The setting value will take effect for Secondary Channel Drive 1 data access only.

Register Index : **60-61h**
Register Name: **MBCPRD - Master Byte Counter for each PRD Table Entry**
Attribute : Read only
Default Value : 00h
This register is for hardware debug only.

Register Index : **62h**
Register Name : **LTPI - Latency Timer of PCI Interface**
Attribute : Read only
Default Value : 00h
This register is for hardware debug only.

Register Index : **63h**
Register Name : **LTEI - Latency Timer Expire Indicator**
Attribute : Read only
Default Value : 01h
This register is for hardware debug only.

Register Index : **64-65h**
Register Name : **BSATA - Byte Counter for Counting in ATA State Machine**
Attribute : Read only
Default Value : 0002h
This register is for hardware debug only.

Register Index : **66h**
Register Name : **SCCATA - Sector Count Counter for Counting in ATA State Machine**
Attribute : Read only
Default Value : 00h
This register is for hardware debug only.

Register Index : **67h**
Register Name : **BSCATA - Block Size Counter for Counting in ATA State Machine**
Attribute : Read only
Default Value : 01h
This register is for hardware debug only.

Register Index : **68h**
Register Name : **PCBS0 - Block Size Register of Device 0 on Primary Channel**
Attribute : Read only
Default Value : 00h
This register is for hardware debug only.

Register Index : **69h**
Register Name : **PCBS1 - Block Size Register of Device 1 on Primary Channel**
Attribute : read only
Default Value 00h
This register is for hardware debug only.

Register Index : **6Ah**
Register Name : **SCBS0 - Block Size Register of Device 0 on Secondary Channel**
Attribute : Read only
Default Value 00h
This register is for hardware debug only.

Register Index : **6Bh**
Register Name : **SCBS1 - Block Size Register of Device 1 on Secondary Channel**
Attribute : Read only
Default Value 00h
This register is for hardware debug only.

Register Index : **6Ch**
Register Name : **PCSC - Primary Channel Sector Count Register**
Attribute : Read only
Default Value : 00h
This register is for hardware debug only and is the duplicate of 1F2.

Register Index : **6Dh**
Register Name : **SCSC - Secondary Channel Sector Count Register**
Attribute : Read only
Default Value : 00h
This register is for hardware debug only and is the duplicate of 172.

Register Index : **6Eh**
Register Name : **PCC - Primary Channel Command Register**
Attribute : Read only
Default Value: 00h
This register is for hardware debug only and is the duplicate of 1F7.

Register Index : **6Fh**
Register Name : **SCC - Secondary Channel Command Register**
Attribute : Read only
Default Value : 00h
This register is for hardware debug only and is the duplicate of 177.

Register Index : **70h**
Register Name : **PCBCL - Primary Channel Byte Count Low Register**.
Attribute : Read only
Default Value : 00h
This register is for hardware debug only and is the duplicate of 1F4.

Register Index : **71h**
Register Name : **PCBCH - Primary Channel Byte Count High Register**.
Attribute : Read only
Default value : 00h
This register is for hardware debug only and is the duplicate of 1F5.

Register Index : **72h**
Register Name : **SCBCL - Secondary Channel Byte Count Low Register**
Attribute : Read only
Default value : 00h
This register is for hardware debug only and is the duplicate of 174.

Register Index : **73h**
Register Name : **SCBCH - Secondary Channel Byte Count High Register**
Attribute : Read only
Default Value : 00h
This register is for hardware debug only and is the duplicate of 175.

Register Index : **74h**
Register Name : **FIFOS - FIFO Status Register**
Attribute : Read only
Default Value : 00h
This register is for hardware debug only.

Bit No.	Description
7(0b)	FIFO_OVERRD. '1' means error condition occurs when FIFO is over read. This bit must be cleared by reset.
6(0b)	FIFO_OVERWR. '1' means error condition occur when FIFO is over written. This bit must be cleared by reset.
5-0(0h)	FIFO_FLAG. Indicates how many words are in FIFO currently. It is binary coded.

Register Index : **75h**
Register Name : **CHIDS - Primary & Secondary Channel Interrupt and Drive Select Status Register**
Attribute : Read only
Default Value : 00h
This register is for hardware debug only.

Bit No.	Description
3(0b)	Secondary Channel Drive Select (the duplicate of 176h bit 4). 0 : Select drive 2. 1 : Select drive 3.
2(0b)	Primary Channel Drive Select (the duplicate of 1F6h bit 4). 0 : Select drive 0. 1 : Select drive 1.
1(0b)	Secondary Channel Interrupt Status. 0 : No Interrupt Pending. 1 : Interrupt Pending.
0(0b)	Primary Channel Interrupt Status. 0 : No Interrupt Pending. 1 : Interrupt Pending.

Register Index : **76h**
Register Name : **CHS - Primary & Secondary Channel Status Register**
Attribute : Read only
Default Value : 00h
This register is for hardware debug only.

Bit No.	Description
6-4(0h)	Secondary Channel's Status. D4 - Error. D5 - DRQ. D6 - Busy.
2-0(0h)	Primary Channel's Status. D0 - Error. D1 - DRQ. D2 - Busy.

Register Index : **77h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **78h**
Register Name : **IDEC - IDE Clock Frequency**
Attribute : Read/Write
Default Value : 21h

Bit No.	Description
7-0(21h)	IDE Clock's Frequency. (default value is 33 = 21H) This register can be used by BIOS to save the M5229 IDE Clock frequency. The hex value represents the Clock frequency.

Register Index : **FFh-79h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

4.1.3 USB M5237 Configuration Register (IDSEL = AD31(default), AD30, AD13, AD12)

The IDSEL can be changed by the M1543C Register Index-72h bits[1:0]. The following table shows the register summary:

Byte Index	Mnemonic	Definition	Attribute (R/W)	Default Value
01h-00h	VID	Vender ID	R	10B9h
03h-02h	DID	Device ID	R	5237h
05h-04h	COM	Command	R/W	0000h
07h-06h	DS	Status	R/W Clear	0280h
08h	RID	Revision ID	R	03h
0Bh-09h	CC	Class Code	R	0C0310h
0Ch	CLS	Cache Line Size	R/W	00h
0Dh	LT	Latency Timer	R/W	00h
0Eh	HT	Header Type	R	00h
0Fh	BIST	Built In Self Test	R	00h
13h-10h	BA	Base Address Register	R/W	00000000h
2Bh-14h	Reserved	Reserved	R	00h
2Dh-2Ch	SVID	Subsystem Vendor ID	R/W Lock	0000h
2Fh-2Eh	SDID	Subsystem Device ID	R/W Lock	0000h
3Bh-30h	Reserved	Reserved	R	00h
3Ch	IL	Interrupt Line	R/W	00h
3Dh	IP	Interrupt Pin	R	01h
3Eh	MG	Min_Gnt	R	00h
3Fh	ML	Max_Lat	R	50h
43h-40h	TM	Test Mode	R/W	00000000h
FFh-44h	Reserved	Reserved	R	00h

Register Index : **01h-00h**
Register Name : **VID - Vendor ID Register**
Attribute : Read only
Default Value : 10B9h

Bit No.	Description
15-0	This is a 16-bit value assigned to Acer Labs Inc. This register is combined with 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Register Index : **03h-02h**
Register Name : **DID - Device ID Register**
Attribute : Read only
Default Value : 5237h

Bit No.	Description
15-0	This register holds a unique 16-bit value assigned to a device, and combined with the vendor ID, it identifies any PCI device.

Register Index **05h-04h**
Register Name : **COM - Command Register**
Attribute : Read/Write
Default Value 0000h

Bit No.	Description
15-10(00h)	Reserved. These bits are always 0.
9(0b)	Back to Back Enable. M5237 only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
8(0b)	Enable the SERRJ Driver. When this bit is set, M5237 will enable SERRJ output driver. This bit is reset to 0 and will set to 1 when it detects an address parity error. SERRJ is not asserted if this bit is 0.
7(0b)	Wait Cycle Control. M5237 does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
6(0b)	Respond to Parity Errors. If set to 1, M5237 will assert PERRJ when it is the agent receiving data and it detects a data parity error. PERRJ is not asserted if this bit is 0.
5(0b)	Enable VGA Palette Snooping. This bit is always 0.
4(0b)	Memory Write and Invalidate Command. If set to 1, M5237 is enabled to run Memory Write and Invalidate commands. The Memory Write and Invalidate Command will only occur if the cacheline size is set to 32 bytes and the memory write is exactly one cacheline.
3(0b)	Enable Special Cycle. M5237 does not run special cycles on PCI. This bit is always 0.
2(0b)	Enable PCI Master. If set to 1, M5237 is enabled to run PCI Master cycles. This bit must be enabled for the normal USB Master access.
1(0b)	Enable Response to Memory Access. If set to 1, M5237 is enabled to respond as a target to memory cycles. This bit must be enabled for the USB Memory access.
0(0b)	Enable Response to I/O Access. If set to 1, M5237 is enabled to respond as a target to I/O cycles. This bit must be enabled for the normal USB I/O access.

Register Index : **07h-06h**
Register Name : **DS - Status Register**
Attribute : Read only, Write clear
Default Value : 0280h

Bit No.	Description
15(0b)	Detected Parity Error. This bit is set by M5237 to 1 whenever it detects a parity error, even if the Respond to Parity Errors bit (command register, bit 6) is disabled. This bit is cleared (reset to 0) by writing a 1 to it.
14(0b)	SERRJ Status. This bit is set by M5237 to 1 whenever it detects a PCI address parity error. This bit is cleared (reset to 0) by writing a 1 to it.
13(0b)	Received Master Abort Status. This bit is set to 1 when M5237, acting as a PCI master, aborts a PCI bus memory cycle. This bit is cleared (reset to 0) by writing a 1 to it.
12(0b)	Received Target Abort Status. This bit is set to 1 when M5237 generates a PCI cycle (M5237 is the PCI master) is aborted by a PCI target. This bit is cleared (reset to 0) by writing a 1 to it.
11(0b)	Sent Target Abort Status. This bit is set to 1 when M5237 signals target abort. This bit is cleared (reset to 0) by writing a 1 to it.
10-9(01b)	DEVSELJ Timing. Read only bits indicating DEVSELJ timing when performing a positive decode. 00 : Fast 01 : Medium 10 : Slow Since DEVSELJ is asserted by M5237 to meet the medium timing, these bits are encoded as 01b.
8(0b)	Data Parity Reported. Set to 1 if the Respond to Parity Error bit (Command Register bit 6) is set, and M5237 detects PERRJ asserted while acting as PCI master (whether PERRJ was driven by M5237 or not).
7(1b)	Fast Back-to-Back Capable. M5237 does support fast back-to-back transactions when the transactions are not to the same agent. This bit is always 1.
6-0(0h)	Reserved. These bits are always 0.

Register Index : **08h**
Register Name : **RID - Revision ID Register**
Attribute : Read only
Default Value : 03h

Bit No.	Description
7-0(03h)	Functional Revision Level (00000011b)

Register Index : **0B-09h**
Register Name : **CC - Class Code Register**
Attribute : Read only
Default Value 0C0310h

Bit No.	Description
23-0 (0C0310h)	This register identifies the generic function of M5237 the specific register level programming interface. The Base Class is 0Ch (Serial Bus Controller). The SubClass is 03h (Universal Serial Bus). The Programming Interface is 10h (OpenHCI).

Register Index : **0Ch**
Register Name : **CLS - Cache Line Size**
Attribute : Read/Write
Default Value 00h

Bit No.	Description
7-0(0h)	This register identifies the system cacheline size in units of 32-bit words. M5237 will only store the value of bit 3 in this register since the cacheline size of 32 bytes is the only value applicable to the design. Any value other than 08h written to this register will be read back as 00h.

Register Index : **0Dh**
Register Name : **LT - Latency Timer**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-0(0h)	This register identifies the value of latency timer in PCI clocks for PCI bus master cycles.

Register Index : **0Eh**
Register Name : **HT - Header Type Register**
Attribute : Read Only
Default Value 00h

Bit No.	Description
7-0(0h)	This register identifies the type of predefined header in the configuration space. Since M5237 is a single function device and not a PCI-to-PCI bridge, this byte should be read as 00h.

Register Index : **0Fh**
Register Name : **BIST - Built In Self Test**
Attribute : Read only
Default Value : 00h

Bit No.	Description
7-0(0h)	This register identifies the control and status of Built In Self Test. M5237 does not implement BIST, so this register is read only.

Register Index : **13-10h**
Register Name : **BA - Base Address Register**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
31-12(0h)	Base Address. POST writes the value of the memory base address to this register.
11-4(0h)	Always 0. Indicates a 4K byte address range is requested.
3(0b)	Always 0. Indicates there is no support for prefetchable memory.
2-1(0h)	Always 0. Indicates that the base register is 32-bit wide and can be placed anywhere in 32-bit memory space.
0(0b)	Always 0. Indicates that the operational registers are mapped into memory space.

Register Index : **2Bh-14h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index: **2Dh-02Ch**
Register Name: **SVID - Subsystem Vendor ID**
Attribute: Read/Write
Default Value: 0000h

Bit	Description
15-0	If the Test Mode Register Index 40h bit20=0, then this register can be Read/Write. Else, this register is Read-Only. BIOS should program a value to this register and then lock it by setting M5237 Register Index 40h bit20 = 1.

Register Index : **2Fh-02Eh**
Register Name : **SDID - Subsystem Device ID**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15-0	If the Test Mode Register Index 40h bit20=0, then this register can be Read/Write. Else, this register is Read-Only. BIOS should program a value to this register and then lock it by setting M5237 Register Index 40h bit20 = 1.

Register Index : **3Ch**
Register Name : **IL - Interrupt Line Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-0(0h)	This register identifies which of the system interrupt controllers the device interrupt pin is connected to. The value of this register is used by device drivers and has no direct meaning to M5237.

Register Index : **3Dh**
Register Name : **IP - Interrupt Pin Register**
Attribute : Read only
Default Value : 01h

Bit No.	Description
7-0(01h)	This register identifies which interrupt pin a device uses. Since M5237 uses INTAJ, this value is set to 01h.

Register Index **3Eh**
Register Name : **MG - Min Gnt Register**
Attribute : Read only
Default Value : 00h

Bit No.	Description
7-0(0h)	This register specifies the desired settings for how long a burst M5237 needs assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.

Register Index **3Fh**
Register Name : **ML - Max Lat Register**
Attribute : Read only
Default Value : 50h

Bit No.	Description
7-0(0h)	This register specifies the desired settings for how often M5237 needs access to the PCI bus assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.

Register Index: **43h-040h**
Register Name: **TM - Test Mode Register**
Attribute: Read/Write
Default Value: 00000000h

Bit	Description
31-27(00h)	Reserved. Must always write 0's.
26 (0b)	Third USB port Enable bit 0 : disable 1 : enable
25-21 (00h)	Reserved. Must always write 0's.
20(0b)	Subsystem Vendor/Device ID (Index 2Fh-02Ch) Lock Bit. 0 : Index 2Fh-02Ch can be Read/Write. 1 : Index 2Fh-02Ch is Read-Only. This bit is used to control the attribute of M5237 Register Index 2Fh-2Ch. BIOS can use this bit to lock the content of Subsystem Vendor and Device ID Registers. Value 1 is suggested for some SCT test program.
19-0(00000h)	Reserved. Must always write 0's.

Register Index : **FFh - 44h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

4.1.4 PMU M7101 Configuration Registers Description (IDSEL=AD28(default), AD29, AD14, AD15)

The IDSEL can be changed by the M1543C Register Index-72h bits[3:2]. The following table shows the register summary :

Byte Index	Mnemonic	Definition	Attribute	Default Value
01h-00h	VID	Vender ID	R	10B9h
03h-02h	DID	Device ID	R	7101h
05h-04h	COM	Command	R/W	0000h
07h-06h	DS	Status	R/W	0200h
08h	RID	Revision ID	R	00h
0Bh-09h	CC	Class Code	R	TBD
0Dh-0Ch	Reserved	Reserved	R	0000h
0Eh	HT	Header Type	R	00h
0Fh	Reserved	Reserved	R	00h
13h-10h	PBA	PMU I/O Base Address Register	R/W	00000001h
17h-14h	SBA	SMB I/O Base Address Register	R/W	00000001h
2Bh-18h	Reserved	Reserved	R	00h
2Dh-2Ch	SVID	Subsystem Vendor ID	R/W Lock	0000h
2Fh-2Eh	SDID	Subsystem Device ID	R/W Lock	0000h
3Fh-30h	Reserved	Reserved	R	00h
41h-40h	SEOG	SMI Enable When ON to Green	R/W	0000h
43h-42h	SSOG	SMI Status When ON to Green	R/W	0000h
46h-44h	SEWS	SMI Enable When Wake Up from Standby	R/W	200000h
47h	Reserved	Reserved	R	00h
4Ah-48h	SSWS	SMI Status When Wake Up from Standby	R/W	000000h
4Bh	Reserved	Reserved	R	00h
4Dh-4Ch	EESS	Enable of External Switch SMI	R/W	0000h
4Fh-4Eh	SESS	Status of External Switch SMI	R/W	0000h
51h-50h	EEGS	Enable of Extended GPI SMI	R/W	0000h
53h-52h	SEGS	Status of Extended GPI SMI	R/W	0000h
54h	ST	Standby Timer	R/W	00h
55h	APMTA	APM Timer A	R/W	00h
58h-56h	Reserved	Reserved	R	00h
59h	GDT	Global Display Timer	R/W	00h
5Ah	Reserved	Reserved	R	00h
5Bh	ATPC	ACPI Test Program Control	R/W	00h
5Fh-5Ch	Reserved	Reserved	R	00h
63h-60h	SEMST	System Events Monitored by Standby Timer	R/W	00000000h
65h-64h	DEMDT	Display Events Monitored by Display Timer	R/W	0000h
67h-66h	Reserved	Reserved	R	00h
68h	SEDI	System Event Definition I	R/W	00h
6Bh-69h	Reserved	Reserved	R	00h
6Fh-6Ch	SEDII	System Event Definition II	R/W	00000000h
71h-70h	SEDIII	System Event Definition III	R/W	0000h
73h-72h	SEDIV	System Event Definition IV	R/W	0000h
74h	SWUS	System Wake Up Status	R/W	00h
75h	TIMBA	Time Interval to Measure Bus Activity	R/W	00h
76h	TNTDTI	Threshold Number of TRDYJ Detected in the Time Interval	R/W	00h
77h	SMI_CNTL	SMI Control Register	R/W	00h
79h-78h	PTS	PLL Timer Setting	R/W	0000h
7Ah	PIIGS	Pentium II Green State Select	R/W	00h
7Bh	SCC	STPCLKJ Control	R/W	00h
7Ch	BESI	Break Events for STPCLKJ I	R/W	00h
7Dh	DCGPIO	Direction Control of GPIO[7:0]	R/W	00h
7Eh	DOGPIO	Data Output of GPIO[7:0]	R/W	00h

Byte Index	Mnemonic	Definition	Attribute	Default Value
7Fh	DIGPIO	Data Input from GPIO[7:0]	R only	00h
82h-80h	COESI	Control of External Switch I	R/W	000000h
83h	Reserved	Reserved	R	00h
87h-84h	COEGI	Control of Extended GPI I	R/W	00000000h
8Bh-88h	COEGII	Control of Extended GPI II	R/W	00000000h
8Eh-8Ch	COESII	Control of External Switch II	R/W	000000h
8Fh	Reserved	Reserved	R	00h
90h	CGPESI	Control of General Purpose External Switch I	R/W	00h
91h	CGPESII	Control of General Purpose External Switch II	R/W	00h
93h-92h	Reserved	Reserved	R	00h
97h-94h	MGA	Memory Group A	R/W	00000000h
98h-99h	SLEE	Select Level /Edge trigger of Extended GPI	R/W	0000h
A3h-9Ah	Reserved	Reserved	R	00h
A5h-A4h	IOGC	I/O Group C	R/W	0000h
B1h-A6h	Reserved	Reserved	R	00h
B2h	CSS	Current System State	R/W	00h
B3h	SC	Speaker Control	R/W	00h
B4h	SLED	Suspend LED	R/W	00h
B5h	LEDC	LED Control	R/W	00h
B6h	Reserved	Reserved	R	00h
B7h	RIC	Ring In Counter	R/W	00h
B9h-B8h	ODEGPO	Output Data of EGPO[15:0]	R/W	00h
BBh-BAh	IDEGPI	Input Data of EGPI[15:0]	R only	00h
BCh	SRIO70	Shadow Register of IO Port 70h	R/W	00h
BDH	PCCA	PMU Class Code Attribute	R/W	00h
BEh	PSANS	Power Saving of All Normal Switches	R/W	00h
BFh	Reserved	Reserved	R	00h
C2h-C0h	DOGPOI	Data Output to GPO Pins	R/W	000000h
C3h	DOGPOII	Data Output for GPO[23:22]	R/W	00h
C5h-C4h	IDGPI	Input Data of GPI[11:0]	R	00h
C6h	SMIRB	Select Multifunction in Resume Block	R/W	00h
C7h	Reserved	Reserved	R	00h
C8h	MMEAT	Mask Monitored Events of All Timers	R/W	00h
C9h	LRWACR	Lock Read/Write off All Configuration Registers	R/W	00h
CAh	WBP	Write Beep Port	W	00h
CBh	Reserved	Reserved	R	00h
CDh-CCh	DCC	Dynamic Clock Control	R/W	0000h
D3h-CEh	Reserved	Reserved	R	00h
D4h	SMT	Suspend Test Mode Disable/Enable	R/W	00h
D5h	HSSI	Hardware Setting Status Bits I	R	xxh
D6h	HSSII	Hardware Setting Status Bits II	R	xxh
D7h	Reserved	Reserved	R	00h
D8h	DSC	Delay SMI Control	R/W	00h
D9h	BESII	Break Event for STPCLKJ II	R/W	00h
DFh-DAh	Reserved	Reserved	R	00h
E0h	SMBHSI	SMBus Host & Slave Interface Configuration	R/W	00h
E1h	SMBHSC	SMBus Host Slave Command Register	R/W	00h
E2h	SMBHCBC	SMBus Host Controller Base Clock Setting	R/W	20h
FFh-E3h	Reserved	Reserved	R	00h

All reserved bits are read as 0's.

Register Index : **01h-00h**
Register Name : **VID - Vendor ID Register**
Attribute : Read only
Default Value : 10B9h

Bit No.	Description
15-0 (10B9h)	This is a 16-bit value assigned to Acer Labs Inc. This register is combined with 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Register Index : **03h-02h**
Register Name : **DID - Device ID Register**
Attribute : Read only
Default Value : 7101h

Bit No.	Description
15-0 (7101h)	This register holds a unique 16-bit value assigned to a device, and combined with the vendor ID, it identifies any PCI device. Write to this register has no effect.

Register Index : **05h-04h**
Register Name : **COM - Command Register**
Attribute : Read/Write
Default Value 0000h

Bit No.	Description
15-5(000h)	Reserved. These bits are always 0.
4(0b)	Memory Write and Invalidate Command. M7101 will never issue Memory Write and Invalidate commands. This bit is always 0. Write to this bit has no effect.
3(0b)	Enable Special Cycle. M7101 will never accept special cycles on PCI. This bit is always 0. Write to this bit has no effect.
2(0b)	Enable PCI Master. M7101 will never act as a PCI master. This bit is always 0. Write to this bit has no effect.
1(0b)	Enable Response to Memory Access. M7101 will never respond to any Memory access. All the access is defineded as I/O access. This bit is always 0. Write to this bit has no effect.
0(0b)	Enable Response to I/O Access. This bit is used to enable M7101 response to PMU and SMB I/O space registers. The I/O Base Address Registers of Index 13h-17h must be set before this bit is set.

Register Index : **07h-06h**
Register Name : **DS - Device Status Register**
Attribute : Read Only, Read/Write Clear
Default Value 0200h

Bit No.	Description
15(0b)	Detected Parity Error. This bit is always 0 in M7101 implementation.
14(0b)	SERRJ Status. This bit is always 0 in M7101 implementation.
13(0b)	Received Master Abort Status. Since M7101 never acts as a PCI master, this bit is not implemented and always 0.
12(0b)	Received Target Abort Status. Since M7101 never acts as a PCI master, this bit is not implemented and always 0.
11(0b)	Sent Target Abort Status. M7101 as a slave never generates a Target abort. This bit is always 0.
10-9(01b)	DEVSELJ Timing. Read only bits indicating DEVSELJ timing when performing a positive decode. 00 : Fast. 01 : Medium. 10 : Slow. Since DEVSELJ is asserted by M7101 to meet the medium timing, these bits are encoded as 01b.
8-0(000h)	Reserved. These bits are always 0.

Register Index : **08h**
Register Name : **RID - Revision ID Register**
Attribute : Read only
Default Value : 00h

Bit No.	Description
7-0(C0h)	This register contains the version number of M7101. Since there is no PMU Class Code defined in PCI Specification, the value is TBD. M7101 Register Index BDh bit3 can change this register attribute to be read/write or read only.

Register Index **0B-09h**
Register Name : **CC - Class Code Register**
Attribute : Read only
Default Value TBD

Bit No.	Description
23-0 (TBD)	This register identifies the Class Code of M7101.

Register Index : **0Dh - 0Ch**
Register Name : **Reserved Register**
Attribute : Read Only
Default Value 0000h

Register Index : **0Eh**
Register Name : **HT - Header Type Register**
Attribute : Read only
Default Value 00h

Bit No.	Description
7-0(00h)	This register identifies the type of predefined header in the configuration space. Since M7101 is a single function device and not a PCI-to-PCI bridge, this byte should be read as 00h.

Register Index : **0Fh**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **13h-10h**
Register Name : **PBA - PMU I/O Base Address Register**
Attribute : Read/Write
Default Value : 00000001h

Bit No.	Description
31-16 (0000h)	Reserved. Must be written as 0000h.
15-6 (000h)	Corresponds to PMU I/O start address AD[15:6]. The minimum PMU I/O start address is 64Bytes size.
1(0b)	Reserved. Always 0.
0(1b)	Always 1. Indicates that the operational registers are mapped into I/O space.

Register Index : **17h-14h**
Register Name : **SBA - SMB I/O Base Address Register**
Attribute : Read/Write
Default Value : 00000001h

Bit No.	Description
31-16 (0000h)	Reserved. Must be written as 0000h.
15-6 (000h)	Corresponds to SMB I/O start address AD[15:5]. The minimum SMB I/O start address is 32Bytes size.
1(0b)	Reserved. Always 0.
0(1b)	Always 1. Indicates that the operational registers are mapped into I/O space.

Register Index : **2Bh-18h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **2Dh-2Ch**
Register Name : **SVID - Subsystem Vendor ID**
Attribute : Read/Write Lock
Default Value : 0000h

Bit	Description
15-0 (0000h)	If the M1543C Register Index 74h bit6 = 0, then this register is Readable/Writeable. Else, this register is Read-Only. BIOS should program a value to this register and then lock it by setting the M1543C Register Index 74h bit6 = 1.

Register Index : **2Fh-2Eh**
Register Name : **SDID - Subsystem Device ID**
Attribute : Read/Write Lock
Default Value : 0000h

Bit	Description
15-0 (0000h)	If the M1543C Register Index 74h bit6 = 0, then this register is Readable/Writeable. Else, this register is Read-Only. BIOS should program a value to this register and then lock it by setting the M1543C Register Index 74h bit6 = 1.

Register Index : **3Fh-30h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **41h-40h**
Register Name : **SEOG - SMI Enable When ON to Green**
Attribute : Read/Write
Default Value : 0000h
Index 41h-40h are used to control the SMI enable when system is at fully On state. BIOS can enable this register to generate SMI to enter into the different Green states. Index 43h-42h are the respective SMI status bits.

Bit	Description
15-13 (0h)	Reserved.
12 (0b)	Soft SMI, Caused by Writing IO Port 0B1h. This bit is used to enable software SMI. When hardware detects an I/O port 0B1h write and this bit is enabled, an SMI will be generated and the status bit in Index 43h-42h bit12 will be set to 1.
11-5 (00h)	Reserved.
4 (0b)	APM Timer A Timeout SMI. This bit is used to enable APM timer A Timeout SMI. APM timer A timeout is defined in M7101 Register Index 55h. APM timer A will not monitor any event. It is a pure timer function. When the timer is up and this bit is enabled, an SMI will be generated and the status bit in Index 43h-42h bit4 will be set to 1.
3 (0b)	RTC SMI, caused by Assertion of IRQ8J. This bit is used to enable RTC SMI. When this bit is enabled and hardware detects IRQ8J signal level from high to low, an SMI will be generated and the status bit in Index 43h-42h bit3 will be set to 1.
2 (0b)	PWRBTNJ (Power Button) SMI. This bit is used to enable Hardware pin PWRBNJ event to generate SMI. The generation mode is defined in M7101 Register Index 90h bit0 and bit3. When the programmed mode is match and this bit is enabled, an SMI will be generated and the status bit in Index 43h-42h bit2 will be set to 1.
1 (0b)	Display Timer Timeout SMI. This bit is used to enable Display Timer Timeout SMI. Display timer is defined in M7101 Register Index 59h, and its moniter events are defined in M7101 Register Index 65h-64h. A display timer timeout SMI will be generated and the status bit in Index 43h-42h bit1 will be set to 1 when the timer in Index 59h is up and does not detect any monitored events defined in Index 65h-64h.
0 (0b)	Standby Timer Timeout SMI. This bit is used to enable Standby Timer Timeout SMI. Standby timer is defined in M7101 Register Index 54h, and its moniter events are defined in M7101 Register Index 63h-60h. A standby timer timeout SMI will be generated and the status bit in Index 43h-42h bit0 will be set to 1 when the timer in Index 54h is up and does not detect any monitored events defined in Index 63h-60h.

Register Index : **43h-042h**
Register Name : **SSOG - SMI Status when ON to Green**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15-13 (0h)	Reserved.
12 (0b)	Soft SMI Status Bit, caused by writing I/O port 0B1h. Please refer to M7101 Register Index 41h-40h bit 12.
11-5 (00h)	Reserved.
4 (0b)	APM timer A Timeout SMI Status Bit. Please refer to M7101 Register Index 41h-40h bit 4.
3 (0b)	RTC SMI Status Bit, caused by Assertion of IRQ8J. Please refer to M7101 Register Index 41h-40h bit 3.
2 (0b)	PWRBTNJ (Power Button) SMI Status Bit. Please refer to M7101 Register Index 41h-40h bit 2.
1 (0b)	Display Timer Timeout SMI Status Bit. Please refer to M7101 Register Index 41h-40h bit 1.
0 (0b)	Standby Timer Timeout SMI Status Bit. Please refer to M7101 Register Index 41h-40h bit 0.

Register Index : **46h-44h**
Register Name : **SEWS - SMI Enable When Wake Up from Standby**
Attribute : Read/Write
Default Value : 200000h
Index 46h-44h are used to control the SMI enable to wake up the system from Standby state. BIOS can enable this register to generate SMI to wake up the system from Standby state. Index 46h-44h are the respective SMI status bits.

Bit	Description
23-21 (001b)	Reserved.
20 (0b)	SIRQ Access SMI. When the system is in Standby state, this bit is enabled, and the SIRQ acces event notified by internal Serial IRQ circuit block has been detected, an SMI will be generated and the status bit in Index 4Ah-48h bit 20 will be set to 1. BIOS can utilize this SMI and identify the SIRQ access to wake up the system.
19 (0b)	SMB Bus SMI. When the system is in Standby state, this bit is enabled, and the SMB Bus event notified by internal SMB controller has been detected, a SMI will be generated and the status bit in Index 4Ah-48h bit 19 will be set to 1. BIOS can utilize this SMI and identify the SMB Bus event to wake up the system.
18-16 (0h)	Reserved.
15 (0b)	I/O Group C I/O Access SMI. When the system is in Standby state, this bit is enabled, and the I/O Group C cycle defined in M7101 Register Index 71h bits[5:4] and Index A5h-A4h has been detected, a SMI will be generated and the status bit in Index 4Ah-48h bit 15 will be set to 1. BIOS can utilize this SMI and identify the I/O Group C access to wake up the system.
14-13 (0h)	Reserved.
12 (0b)	Parallel Port I/O Access SMI. When the system is in Standby state, this bit is enabled, and the Parallel Port I/O cycle defined in M7101 Register Index 71h bits[2:0] has been detected, a SMI will be generated and the status bit in Index 4Ah-48h bit 12 will be set to 1. BIOS can utilize this SMI and identify the Parallel Port I/O access to wake up the system.
11 (0b)	Keyboard I/O Access SMI. Serial I/O Access SMI. When the system is in Standby state, this bit is enabled, and the Keyboard I/O Ports (60h and 64h) cycle has been detected, a SMI will be generated and the status bit in Index 4Ah-48h bit 11 will be set to 1. BIOS can utilize this SMI and identify the Keyboard I/O Ports access to wake up the system.
10 (0b)	Serial I/O Access SMI. When the system is in Standby state, this bit is enabled, and the Serial I/O Ports cycle defined in M7101 Register Index 70h bits[7:0] has been detected, an SMI will be generated and the status bit in Index 4Ah-48h bit 10 will be set to 1. BIOS can utilize this SMI and identify the Serial I/O Ports access to wake up the system.
9 (0b)	Floppy I/O Access SMI. When the system is in Standby state, this bit is enabled, and the Floppy I/O Ports cycle defined in M7101 Register Index 68h bit0 has been detected, an SMI will be generated and the status bit in Index 4Ah-48h bit 9 will be set to 1. BIOS can utilize this SMI and identify the Floppy I/O Ports access to wake up the system.
8 (0b)	Video I/O Access SMI. When the system is in Standby state, this bit is enabled, and the Video I/O Ports (3B0h-3DFh) cycle has been detected, an SMI will be generated and the status bit in Index 4Ah-48h bit 8 will be set to 1. BIOS can utilize this SMI and identify the Video I/O Ports access to wake up the system.
7 (0b)	Audio I/O Access SMI. When the system is in Standby state, this bit is enabled, and the Audio I/O Ports cycle defined in M7101 Register Index 6Fh-6Ch bits[15:2] has been detected, an SMI will be generated and the status bit in Index 4Ah-48h bit 7 will be set to 1. BIOS can utilize this SMI and identify the Audio I/O Ports access to wake up the system.
6 (0b)	IDE Secondary Channel Drive I/O Access SMI. When the system is in Standby state, this bit is enabled, and the IDE Secondary Channel Drive I/O Ports cycle has been detected, an SMI will be generated and the status bit in Index 4Ah-48h bit 6 will be set to 1. The IDE Secondary Channel Drive I/O Ports are defined as 170h-177h and 376h when M7101 Register Index D9h-D8h bit7 is set to 1, or notified by internal IDE controller (M5229) when it is enabled. BIOS can utilize this SMI and identify the IDE Secondary Channel Drive I/O Ports access to wake up the system.

5 (0b)	IDE Primary Channel Drive I/O Access SMI. When the system is in Standby state, this bit is enabled, and the IDE Primary Channel Drive I/O Ports cycle has been detected, an SMI will be generated and the status bit in Index 4Ah-48h bit 5 will be set to 1. The IDE Primary Channel Drive I/O Ports are defined as 1F0h-1F7h and 3F6h when M7101 Register Index D9h-D8h bit7 is set to 1, or notified by internal IDE controller (M5229) when it is enabled. BIOS can utilize this SMI and identify the IDE Primary Channel Drive I/O Ports access to wake up the system.
4 (0b)	Modem RING IN SMI. When the system is in Standby state, this bit is enabled, and the Modem Ring In pin has been detected active, an SMI will be generated and the status bit in Index 4Ah-48h bit 4 will be set to 1. BIOS can utilize this SMI and identify the Modem Ring In to wake up the system.
3 (0b)	BUS_Master Active SMI. When the system is in Standby state, this bit is enabled, and Bus master activity has been detected (monitor PHOLDJ and PCIREQJ), an SMI will be generated and the status bit in Index 4Ah-48h bit 3 will be set to 1. BIOS can utilize this SMI and identify the Bus master activity to wake up the system.
2 (0b)	USB Access SMI. When the system is in Standby state, this bit is enabled, and the USB access event coming from internal USB block has activity, an SMI will be generated and the status bit in Index 4Ah-48h bit 2 will be set to 1. BIOS can utilize this SMI and identify the USB event to wake up the system.
1 (0b)	Display Timeout Activity SMI. When the system is in Standby state, this bit is enabled, and the monitor event defined in M7101 Register Index 65h-64h has activity, an SMI will be generated and the status bit in Index 4Ah-48h bit 1 will be set to 1. BIOS can utilize this SMI and identify the event to wake up the system.
0 (0b)	Standby to ON SMI. When the system is in Standby state, this bit is enabled, and the monitor event defined in M7101 Register Index 63h-60h has activity, an SMI will be generated and the status bit in Index 4Ah-48h bit 0 will be set to 1. BIOS can utilize this SMI and identify the event to wake up the system. Also, M7101 Register Index 74h defines another system event to wake up system from Standby State.

Register Index : **47h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **4Ah-48h**
Register Name : **SSWS - SMI Status When Wake Up from Standby**
Attribute : Read/Write
Default Value : 000000h

Bit	Description
23-22 (0h)	Reserved.
21 (0b)	USB Bus SMI Status. This bit is set when USB needs CPU service, and an SMI will always be generated.
20 (0b)	SIRQ Access Status. Please refer to M7101 Register Index 46h-44h bit 20.
19 (0b)	SMB Bus Status. Please refer to M7101 Register Index 46h-44h bit 19.
18-16 (0h)	Reserved.
15 (0b)	IO Group C I/O Access Status. Please refer to M7101 Register Index 46h-44h bit 15.
14-13 (0h)	Reserved.
12 (0b)	Parallel Port I/O Access Status. Please refer to M7101 Register Index 46h-44h bit 12.
11 (0b)	Keyboard I/O Access Status. Please refer to M7101 Register Index 46h-44h bit 11.
10 (0b)	Serial I/O Access Status. Please refer to M7101 Register Index 46h-44h bit 10.
9 (0b)	Floppy I/O Access Status. Please refer to M7101 Register Index 46h-44h bit 9.
8 (0b)	Video I/O Access Status. Please refer to M7101 Register Index 46h-44h bit 8.
7 (0b)	Audio I/O Access Status. Please refer to M7101 Register Index 46h-44h bit 7.
6 (0b)	IDE Secondary Channel Drive I/O access status. Please refer to M7101 Register Index 46h-44h bit 6.
5 (0b)	IDE Primary Channel Drive I/O Access Status. Please refer to M7101 Register Index 46h-44h bit 5.
4 (0b)	Modem RING IN Status. Please refer to M7101 Register Index 46h-44h bit 4.
3 (0b)	BUS_Master Status. Please refer to M7101 Register Index 46h-44h bit 3.
2 (0b)	USB Access Status. This bit is set when USB bus is busy. Please refer to M7101 Register Index 46h-44h bit 2.
1 (0b)	Display Timeout Activity Status. Please refer to M7101 Register Index 46h-44h bit 1.
0 (0b)	Standby to ON Status. Please refer to M7101 Register Index 46h-44h bit 0.

Register Index : **4Bh**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **4Dh-4Ch**
Register Name : **EESS - Enable of External Switch SMI**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15-9 (00h)	Reserved.
8 (0b)	THRMJ Rising/Falling Toggle SMI. When this bit is enabled, and the Thermal input pin THRMJ has been detected a toggle , the edge is defined in M7101 Register Index 82h-80h bits[14:12], an SMI will be generated and the status bit in Index 4Fh-4Eh bit 8 will be set to 1. BIOS can utilize this SMI and identify the THRMJ input toggle.
7-3 (0h)	Reserved.
2 (0b)	DOCKJ Rising/Falling Toggle SMI. When this bit is enabled, and the input pin DOCKJ has been detected a toggle , the edge is defined in M7101 Register Index 8Eh-8Ch bits[2:1], an SMI will be generated and the status bit in Index 4Fh-4Eh bit 2 will be set to 1. BIOS can utilize this SMI and identify the DOCKJ input toggle.
1 (0b)	Reserved.
0 (0b)	AC Power Rising/Falling Toggle SMI. When this bit is enabled, and the AC Power input pin ACPWR has been detected a toggle , the edge is defined in M7101 Register Index 8Eh-8Ch bits[10:9], an SMI will be generated and the status bit in Index 4Fh-4Eh bit 0 will be set to 1. BIOS can utilize this SMI and identify the ACPWR input toggle.

Register Index : **4Fh-4Eh**
Register Name : **SESS - Status of External Switch SMI**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15-9 (00h)	Reserved.
8 (0b)	THRMJ Rising/Falling Toggle Status. Please refer to M7101 Register Index 4Dh-4Ch bit 8.
7-3 (0h)	Reserved.
2 (0b)	DOCKJ Rising/Falling Toggle Status. Please refer to M7101 Register Index 4Dh-4Ch bit 2.
1 (0b)	Reserved.
0 (0b)	AC Power Rising/Falling Toggle Status. Please refer to M7101 Register Index 4Dh-4Ch bit 0.

Register Index : **51h-50h**
Register Name : **Enable of Extended GPI SMI**
Attribute : Read/Write
Default Value : 00h

Bit	Description
15 (0b)	Enable/disable of EGPI15 SMI.
14	Enable/disable of EGPI14 SMI.
13	Enable/disable of EGPI13 SMI.
12	Enable/disable of EGPI12 SMI.
11	Enable/disable of EGPI11 SMI.
10	Enable/disable of EGPI10 SMI.
9	Enable/disable of EGPI9 SMI.
8	Enable/disable of EGPI8 SMI.
7	Enable/disable of EGPI7 SMI.
6	Enable/disable of EGPI6 SMI.
5	Enable/disable of EGPI5 SMI.
4	Enable/disable of EGPI4 SMI.
3	Enable/disable of EGPI3 SMI.
2	Enable/disable of EGPI2 SMI.
1	Enable/disable of EGPI1 SMI.
0	Enable/disable of EGPI0 SMI.

Register Index : **53h-52h**
Register Name : **Status of Extended GPI SMI**
Attribute : Read/Write(Write '1' to clear)
Default Value : 00h

Bit	Description
15	EGPI 15 rising /falling toggle status.
14	EGPI 14 rising /falling toggle status.
13	EGPI 13 rising /falling toggle status.
12	EGPI 12 rising /falling toggle status.
11	EGPI 11 rising /falling toggle status.
10	EGPI 10 rising /falling toggle status.
9	EGPI 9 rising /falling toggle status.
8	EGPI 8 rising /falling toggle status.
7	EGPI 7 rising /falling toggle status.
6	EGPI 6 rising /falling toggle status.
5	EGPI 5 rising /falling toggle status.
4	EGPI 4 rising /falling toggle status.
3	EGPI 3 rising /falling toggle status.
2	EGPI 2 rising /falling toggle status.
1	EGPI 1 rising /falling toggle status.
0	EGPI 0 rising /falling toggle status.

Register Index : **54h**
Register Name : **ST - Standby Timer**
Attribute : Read/Write
Default Value : 00h
This register defines the Standby timer. It can be used to generate Standby timer timeout SMI to alow the BIOS to control the system to enter into different Green states when it is timeout and there is no any activity in Standby timer monitor event. The timer will be reset by the Standby timer monitor events if it is not timeout yet. Also it can be used to generate Standby to On SMI when the Standby monitor events occurs after timeout. The monitored events are selected by M7101 Register Index 63h-60h.

Bit	Description
7-0 (00h)	Count. (=0, when disabled)(timebase = 1min) The timer value is defined by the content x 1min.

Register Index : **55h**
Register Name : **APMTA - APM Timer A**
Attribute : Read/Write
Default Value : 00h
This register defines the APM timer A. It can be used to generate APM timer A timeout SMI to allow the BIOS to control the system to enter into different Green States when it is timeout. APM timer A will not monitor any system event, it is a timer function only. There are two modes defined in bit 6: Normal mode and Repeat mode. In Normal mode, the timer will only begin to count after the register is set each time. After timeout, it will not count until next register setting. If in Repeat mode, timer will be reset to count again after timeout.

Bit	Description
7 (0b)	Reserved.
6 (0b)	Timer Normal/Repeat Mode. 0 : Normal Mode. 1 : Repeat Mode.
5-4 (0h)	Timebase of APM Timer A. 00 : 1ms. 01 : 1sec. 10 : 1min. 11 : reserved.
3-0 (0h)	Count. (=0, when disabled) The timer value is defined by the content x unit (defined in bits[5:4]).

Register Index : **58h-56h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **59h**
Register Name : **GDT - Global Display Timer**
Attribute : Read/Write
Default Value : 00h
This register defines the Global Display timer. It can be used to generate Global Display timer timeout SMI to alow the BIOS to control the system to enter into different Green states when it is timeout and there is no any activity in Display timer monitor event. The timer will be reset by the Display timer monitor events if it is not timeout yet. Also it can be used to generate Display Activity SMI when the Display monitor events occurs after timeout. The monitored events are selected by M7101 Register Index 65h-64h.

Bit	Description
7-5 (0h)	Reserved.
4 (0b)	Timebase of Display Timer. 0 : 5sec. 1 : 1min.
3-0 (0h)	Count. (=0, when disabled) The timer value is defined by the content x unit (defined in bit4).

Register Index : **5Ah**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **5Bh**
Register Name : **ATPC - ACPI Test Program Control**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
6 (0b)	Enable/disable Break Event Reset Throttle When Clock is High. 0 : Enable. 1 : Disable. This bit is used to control the STPCLKJ affected by break event defined in M7101 Register Index 7Ch when Clock Throttling feature is enabled and STPCLKJ is at high state. When this bit is reset as 0, the break event will force STPCLKJ to keep high to stop clock throttle function. Otherwise, the break event will not affect the STPCLKJ signal. For some ACPI test program, this bit must set to 1.
7, 5 (00b)	Select Throttle Period. 00 : Throttle period is 32 us. 01 : Throttle period is 128 us. 10 : Throttle period is 512 us. 11 : Throttle period is 2 ms. This bit is used to program the throttle period. The other clock throttle controls are located in ACPI P-CNTRL Regitser bits[4:1] (ACPI Register Index 13h-10h).
4 (0b)	Bits[31:5] of ACPI P_CNTRL Register Lock/Unlock Control. 0 : Unlock (can be read/write). 1 : Lock (cannot be read/write). This bit is used to control the attribute of ACPI P_CNTRL Register bits[31:5] (ACPI Register Index 13h-10h). Some old HCT test program might define they are read-only.
3 (0b)	~~Enable/disable Break Event When Throttle Clock Is Low.~~ ~~0 : Enable. 1 : Disable.~~ ~~This bit is used to control the STPCLKJ affected by break event defined in M7101 Register Index 7Ch when Clock Throttling feature is enabled and STPCLKJ is at low state. When this bit is reset as 0, the break event will force STPCLKJ to become high to stop clock throttle function. Otherwise, the break event will not affect the STPCLKJ signal. For some ACPI test program, this bit must set to 1.~~ Reserved.
2 (0b)	SMB I/O Base Address Register Control. 0 : Read/Write. 1 : Read Only. This bit is used to control the attribute of M7101 Register Index 17h-14h (SMB I/O Base Address Register). When this bit is reset as 0, the register can be read/write. Otherwise, the register is read-only.
1 (0b)	ACPI I/O Base Address Register Control. 0 : Read/Write. 1 : Read Only. This bit is used to control the attribute of M7101 Register Index 13h-10h (ACPI I/O Base Address Register). When this bit is reset as 0, the register can be read/write. Otherwise, the register is read-only.'.
0 (0b)	DRAM Self Refresh Enable/Disable during STPCLK Mode. 0 : Enable. 1 : Disable. This bit is used to control the pin SUSTAT1J output status during STPCLK mode. When this bit is reset as 0, SUSTAT1J will be asserted to notify North Bridge to do DRAM self refresh during STPCLK mode. Otherwise, SUSTAT1J will be de-asserted.

Register Index : **5Fh-5Ch**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **63h-60h**
Register Name : **SEMST - Enable/disable System Events Monitored by Standby Timer**
Attribute : Read/Write
Default Value : 00000000h
This register is used to define the system events monitored by Standby Timer. Please refer to section 5 for more detailed information.

Bit	Description
31-27 (0h)	Reserved.
26 (0b)	BUS_ACT Detected.
25 (0b)	PCI_REQJ or PHOLDJ Asserted.
24 (0b)	IRQ[3-7], IRQ[9-15], NMI, INIT or SMIJ Asserted.
23 (0b)	IRQ[1] or IRQ[12] Asserted.
22 (0b)	IRQ[0].
21 (0b)	PWRBTNJ (Power Button).
20 (0b)	USB.
19-17 (0h)	Reserved.
16 (0b)	I/O Group C.
15-13 (0h)	Reserved.
12 (0b)	Memory Group A.
11-10 (0h)	Reserved.
9 (0b)	Modem RING IN.
8 (0b)	RTC.
7 (0b)	Parallel Ports.
6 (0b)	Keyboard.
5 (0b)	Serial I/O.
4 (0b)	Floppy.
3 (0b)	Video.
2 (0b)	Audio.
1 (0b)	Secondary Channel HDD.
0 (0b)	Primary Channel HDD.

Register Index : **65h-64h**
Register Name : **DEMDT - Enable/disable Display Events Monitored by Display Timer**
Attribute : Read/Write
Default Value : 0000h
This register is used to define the system events monitored by Display Timer. Please refer to section 5 for more detailed information.

Bit	Description
15-13 (0h)	Reserved.
12 (0b)	I/O group C.
11-9 (0h)	Reserved.
8 (0b)	Memory Group A.
7 (0b)	Parallel Ports.
6 (0b)	Keyboard.
5 (0b)	Serial I/O.
4 (0b)	Floppy.
3 (0b)	Video.
2 (0b)	Audio.
1 (0b)	Secondary Channel HDD.
0 (0b)	Primary Channel HDD.

Register Index : **67h-66h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **68h**
Register Name : **SEDI - System Event Definition I**
Attribute : Read/Write
Default Value : 00h
This register is used to define the system event for Parallel Port and FDD.

Bit	Description
7-3 (0h)	Reserved.
2-1 (0h)	Select DRQ of Parallel Port Event. 00 : DRQ0. 01 : DRQ1. 10 : DRQ3. 11 : Reserved. These two bits are used to select which DRQ is for the Parallel Port event when M7101 Register Index 71h-70h bit11 is set to 1. The selected DRQ activity will be decoded as Parallel Port system event.
0 (0b)	I/O Address of FDD Port. 0 : 3F0h-3F7h. 1 : 370h-377h. This bit is used to select the I/O address for FDD port. The selected I/O address will be decoded as Floppy system event.

Register Index : **6Bh-69h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **6Fh-6Ch**
Register Name : **SEDII - System Event Definition II**
Attribute : Read/Write
Default Value : 00000000h
This register is used to define the system event for Keyboard, Floppy, Video, Audio, and IDE.

Bit	Description
31-29 (0h)	Reserved.
28 (0b)	Keyboard Event Detect IRQ[12]. When this bit is set to 1, IRQ[12] activity will decode as Keyboard system event.
27 (0b)	Keyboard Event Detect IRQ[1]. When this bit is set to 1, IRQ[1] activity will decode as Keyboard system event.
26 (0b)	Floppy Event Detect DRQ2. When this bit is set to 1, DRQ2 activity will decode as Floppy system event.
25 (0b)	Video Event Detect Graphic IO. When this bit is set to 1, Graphic I/O port 3B0h-3DFh will decode as Video system event.
24 (0b)	Reserved.
23 (0b)	Video Event Detect A-B Pages. When this bit is set to 1, Segment A-B memory access will decode as Video system event.
22 (0b)	Reserved.
21 (0b)	Audio Event Detect DRQ7. When this bit is set to 1, DRQ7 activity will decode as Audio system event.
20 (0b)	Audio Event Detect DRQ6. When this bit is set to 1, DRQ6 activity will decode as Audio system event.
19 (0b)	Audio Event Detect DRQ5. When this bit is set to 1, DRQ5 activity will decode as Audio system event.
18 (0b)	Audio Event Detect DRQ3. When this bit is set to 1, DRQ3 activity will decode as Audio system event.
17 (0b)	Audio Event Detect DRQ1. When this bit is set to 1, DRQ1 activity will decode as Audio system event.
16 (0b)	Audio Event Detect DRQ0. When this bit is set to 1, DRQ0 activity will decode as Audio system event.
15-12 (0h)	I/O Port of MS_Sound Port. The following four bits are used to select the MS_Sound I/O address. The selected address will decode as Audio system event.
15 (0b) 14 (0b) 13 (0b) 12 (0b)	Audio Event Detect F40h-F47h. Audio Event Detect E80h-E87h. Audio Event Detect 604h-60Bh. Audio Event Detect 530h-537h.
11-8 (0h)	I/O Port of SoundB-8/16 port. The following four bits are used to select the Audio Sound Blaster-8/16 I/O address. The selected address will decode as Audio system event.
11 (0b) 10 (0b) 9 (0b) 8 (0b)	Audio Event Detect 280h-293h. Audio Event Detect 260h-273h. Audio Event Detect 240h-253h. Audio Event Detect 220h-233h.
7-4 (0h)	I/O Port of MIDI Port. The following four bits are used to select the MIDI I/O address. The selected address will decode as Audio system event.
7 (0b) 6 (0b) 5 (0b) 4 (0b)	Audio Event Detect 330h-333h. Audio Event Detect 320h-323h. Audio Event Detect 310h-313h. Audio Event Detect 300h-303h.
3 (0b)	Audio Event Detect ADLIB Port, 338h-33Bh. When this bit is set to 1, ADLIB Port 338h-33Bh access will decode as Audio system event.
2 (0b)	Audio Event Detect GAME Port, 200h-207h. When this bit is set to 1, Game Port 200h-207h access will decode as Audio system event.
1 (0b)	IDE Secondary Channel Drive Event Detect SIDE_DRQ. When this bit is set to 1, SIDE_DRQ activity will decode as IDE Secondary Channel system event.
0 (0b)	IDE Primary Channel Drive Event Detect PIDE_DRQ. When this bit is set to 1, PIDE_DRQ activity will decode as IDE Primary Channel system event.

Register Index : **71h-70h**
Register Name : **SEDIII - System Event Definition III**
Attribute : Read/Write
Default Value : 0000h
This register is used to define the system event for I/O Group C, Parallel Port, and Serial Port.

Bit	Description
15-14 (0h)	Reserved.
13 (0b)	IOGPC detects I/O Group Range C defined in M7101 Register IndexA5-A4h.
12 (0b)	IOGPC detects 62h, 66h.
11-8 (0h) 11 (0b) 10 (0b) 9 (0b) 8 (0b)	Select I/O Port and DRQ for Parallel Port Event. The following four bits are used to select Parallel Port event. The selected address and DRQ will decode as Parallel Port system event.Parallel Port Event Detect DRQ0,1,3(Chosen one by M7101 Register Index 68h bits[2:1]). Parallel Port Event Detect 3BCh-3BEh. Parallel Port Event Detect 278h-27Fh. Parallel Port Event Detect 378h-37Fh.
7-0 (00h)	Select I/O Port for Serial Port Event. The following eight bits are used to select Serial I/O Port address. The selected address will decode as Serial Port system event.
7 (0b) 6 (0b) 5 (0b) 4 (0b) 3 (0b) 2 (0b) 1 (0b) 0 (0b)	Serial Port event detect 338h-33Fh. Serial Port event detect 238h-23Fh. Serial Port event detect 228h-22Fh. Serial Port event detect 220h-227h. Serial Port event detect 2E8h-2EFh. Serial Port event detect 3E8h-3EFh. Serial Port event detect 2F8h-2FFh. Serial Port event detect 3F8h-3FFh.

Register Index : **73h-72h**
Register Name : **SEDIV - System Event Definition IV**
Attribute : Read/Write
Default Value : 0000h
This register is used to define the system event for Video, Audio, and Primary HDD based on different GPI pins.

Bit	Description
15-4 (000h)	Reserved.
3 (0b)	Video Detect GPI(3). When this bit is set to 1, GPI(3) activity will decode as Video system event.
2 (0b)	Audio Detect GPI(2). When this bit is set to 1, GPI(2) activity will decode as Audio system event.
1 (0b)	Reserved.
0 (0b)	Primary HDD Detect GPI(0). When this bit is set to 1, GPI(0) activity will decode as IDE Primary Channel system event.

Register Index : **74h**
Register Name : **SWUS - System Wake Up Status**
Attribute : Read/Write
Default Value : 00h
The status is set when the occurrence of the corresponding event causes a Standby to On SMI. They are another system event to set M7101 Register Index 46h-44h bit0 to 1 and generate an SMI to wake up system.

Bit	Description
7-6 (0h)	Reserved.
5 (0b)	System Wake Up by RTC (IRQ8J).
4 (0b)	System Wake Up by PWRBTNJ (Power Button).
3-2 (0h)	Reserved.
1 (0b)	System Wake Up by RING IN.
0 (0b)	System Wake Up by DRQ2.

Register Index : **75h**
Register Name : **TIMBA - Time Interval to Measure Bus Activity**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-0 (00h)	Count. (timebase = PCICLK). The time interval will be counted as x PCICLK.

Register Index : **76h**
Register Name : **TNTDTI - Threshold Number of TRDYJ detected in the Time Interval**
Default Value : 00h
Attribute : Read/Write
If the detected TRDYJ number in the time interval as set at M7101 Register Index 75h is larger than the threshold number. Then, a BUS_ACT activity event (M7101 Register Index 63h-60h bit 26) will be generated.

Bit	Description
7 (0b)	Reserved.
6 (0b)	Enable/disable BUS_ACT. 0 : Disable. 1 : Enable. This bit is used to enable the BUS_ACT circuit.
5-0 (00h)	Threshold Number.

Register Index : **77h**
Register Name : **SMI_CNTL - SMI Control Register**
Attribute : Read/Write
Default Value : 00h
Note: Only level SMI is generated.

Bit	Description
7 (0b)	Select ACPI Mode or M7101 Mode. 0 : ACPI mode, status bit is set as soon as event occurs no matter whether the SMI is enabled or not. 1 : M7101 mode, status bit is set if and only if both events occur and the SMI is enabled. When ACPI mode is selected, status bit will be set no matter the respective event is enabled or disabled. In M7101 mode, the status will not be set until the respective event is enabled.
6 (0b)	SMI Acknowledge Control. 0 : SMIACK deasserted. 1 : SMIACK asserted. This bit is used by SMM routine to notify the M1543C SMIACK has been asserted. SMM routine must assert SMIACK when it enters SMM state and deassert SMIACK when it leaves SMM state.
5 (0b)	Clear both ACPI and Legacy Status. 0 : Clear status bits will reset both ACPI and Legacy status. 1 : Clear status bits only one side. There are common status bits defined in ACPI and M7101 register. This bit is used to control the method to clear the common status bit. When this bit is reset as 0, clear each side status bit will clear the other side too. Otherwise, software must clear for both sides.
4 (0b)	Read/Write Clear SMI. 0 : The status bit of all status registers can only be cleared by writing '1' to it. 1 : Reading the status registers will clear the registers also. This bit is used to program the method to clear the status registers. When this bit is reset as 0, the status can only be cleared by writing a 1 to it. When this bit is set to 1, reading the status bit will clear the status.
3 (0b)	Enable/Disable SMI. 0 : Disable. 1 : Enable. This bit is the total switch of SMI. When this bit is reset as 0, no SMI will be generated. When this bit is set to 1, an SMI can be generated based on the monitored events or by software programming.
2 (0b)	Enable/Disable Delayed Soft SMI. 0 : Disable. 1 : Enable. A Soft SMI can be generated by writing I/O Port B1. This bit is used to enable the delay function defined in bit0 of this register.
1-0 (0h)	SMI Delay Time. 00 : No delay. 01 : 125ms. 10 : 250ms. 11 : 500ms. These two bits are used to select the SMIJ delay time, and the delay is for ACPWR (enabled by M7101 Register Index D8h bit2), THRMJ , DOCKJ (enabled by M7101 Register Index D8h bit0), and Soft SMI (enabled by bit2 above). When the above SMI event occurs, an SMI will be generated after the timeout of programmed time. Any coming event defined in Standby Timer Monitored Event Enable/Disable Register (M7101 Register Index 63h-60h) will reset this timer, and force the timer to count again. An SMI will be generated when the timer is up.

*Clock management
Register Index : **79h-78h**
Register Name : **PTS - PLL Timer Setting**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15-12 (0h)	Reserved.
11-9 (0h)	Selection of Switching Time of SUSPEND to NORMAL. 000 : 0 ms. 001 : 128 us. 010 : 256 us. 011 : 512 us. 100 : 1 ms. 101 : 2 ms. 110 : 4 ms. 111 : 8 ms. When system switches from SUSPEND to NORMAL, the STPCLKJ control signal can not be deasserted until the refresh circuit is switched to normal refresh. The programmed period of time is needed for the North Bridge to change from suspend refresh to normal refresh. The assertion of STPCLKJ will guarantee no CPU cycle during that time.
8-6 (0h)	Selection of Switching Time of NORMAL to SUSPEND. 000 : 0 ms. 001 : 128 us. 010 : 256 us. 011 : 512 us. 100 : 1 ms. 101 : 2 ms. 110 : 4 ms. 111 : 8 ms. When system switches from NORMAL to SUSPEND, the OFF_PWR1 signal cannot assert until the refresh circuit is switched to suspend refresh. The programmed period of time is needed for the North Bridge to flush its internal DRAM Write Buffer data to DRAM.
5-3 (0h)	Selection of CPU PLL Time. 000 : 0 ms. 001 : 0.25 ms. 010 : 0.50 ms. 011 : 1 ms. 100 : 2 ms. 101 : 4 ms. 110 : 8 ms. 111 : 16 ms. When CPU is from STPCLK to STPGNT state, STPCLKJ signal will keep assertion for the programmed period of time to allow the CPU internal PLL to stabilize.
2-0 (0h)	Selection of Clock Generator PLL Time. 000 : 0 ms. 001 : 1 ms. 010 : 2 ms. 011 : 4 ms. 100 : 8 ms. 101 : 16 ms. 110 : 32 ms. 111 : 64 ms. When clock generator changes from Off to On, CPU_STPJ and PCI_STPJ signals will keep assertion for the programmed period of time to allow internal PLL to stabilize when system is resumed from Sleep State.

Register Index : **7Ah**
Register Name : **PIIGS - Pentium II Green State Select**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-3 (00h)	Reserved.
2 (0b)	Enable/Disable monitor HALT cycle 0 : Enable clock control to monitor HALT cycle 1 : Disable clock control to monitor HALT cycle
1 (0b)	Select Mask of INTR, SMI and INIT 0 : Start masking when STPCLKJ is asserted 1 : Start masking when STOP Grant cycle is issued. This bit is used to control the mask of INTR, SMI and INIT. When this bit is reset as 0, INTR, SMI and INIT will be masked as soon as STPCLKJ is asserted. Otherwise, INTR, SMI and INIT will be masked when STOP Grant cycle is issued.
0 (0b)	Pentium II Green State Select Bit I(PII_GSSI). ~~0 : Start masking when STPCLKJ is asserted.~~ ~~1 : Start masking when Stop Grant cycle is issued.~~ This bit combines with M7101 Register Index 7Bh bit3 to define the Pentium II Green State Select. They are defined with Read I/O Port Address B2h to enter different green states. Please refer to the table following Index 7Bh.

Register Index : **7Bh**
Register Name : **SCC - STPCLKJ Control**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7 (0b)	Pentium II Green State Select Bit III (PII_GSSIII). When bit1 = '1' 0 : Sleep 1 : Deep sleep When bit 1 = '0', no meaning. This bit combines with Read ACPI I/O Index 15h (LVL3) to define the Pentium II Green State Select. Please refer to the table following Index 7Bh or section 5.1 for more details.
6 (0b)	Pentium II Green State Select Bit II (PII_GSSII). When bit1 = '1' 0 : STPGNT 1 : Sleep When bit1 = '0', no meaning. This bit combines with Read ACPI I/O Index 14h (LVL2) to define the Pentium II Green State Select. Please refer to the table following Index 7Bh or section 5.1 for more details.
5 (0b)	Select High/Low Active of Auto Thermal Throttle. 0 : High active. 1 : Low active. This bit is used to define the active level of THRMJ pin. 0 is defined as active high, 1 is defined as active low.
4 (0b)	Auto Thermal Throttle Enabled. 0 : Disable. 1 : Enable. When auto thermal throttle is enabled and THRMJ is active for 2 seconds, clock throttle function will be enabled and the duty cycle is defined in ACPI Register Index 13h-10h bits[3:1]. In the M1543C, there are two clock throttle sources: Auto Thermal Throttle defined in this bit, and Clock Throttle function enabled by ACPI Register Index 13h-10h bit[4]. The throttle period is defined in M7101 Register Index 5Bh bit[5] & bit[7].
3 (0b)	Enable/Disable STPCLK Function. (STPCLK_EN) This bit is used to select function when Soft STPCLK is enabled (Read IO port 0B2h). Please refer to the following table next page.
2 (0b)	Software STPCLK Enable/Disable. (Soft_STPCLK) 0 : Disable. 1 : Enable. This bit is used to enable the Software STPCLK (Read IO port 0B2h). Please refer to the following table next page.
1 (0b)	Select Pentium /Pentium II 0 : Pentium. 1 : Pentium II. When Pentium II is selected, SLEEPJ is enabled as well.
0 (0b)	Enable/Disable ZZ Output. 0 : Disable. 1 : Enable. This bit is used to enable ZZ output to powerdown PBSRAM.

Note : The following table shows the methods to enter STPGNT or STPCLK state for Pentium CPU through ACPI register or M7101 register.

ACPI	register	
CPU State	R_LVL2	R_LVL3
STPGNT	1	0
STPCLK	0	1

Soft	STPCLK	
CPU State	STPCLK_EN	Soft_STPCLK
STPGNT	0	1
STPCLK	1	1

The following table shows the methods to enter STPGNT or STPCLK state for Pentium II CPU through ACPI register or M7101 register.

	ACPI	register			Soft STPCLK		
CPU State	R_LVL2	R_LVL3	PII_GSSII	PII_GSSIII	PII_GSSI	STPCLK_EN	Soft_STPCLK
STPGNT	1	0	0	-	0	0	1
Sleep	1	0	1	-	1	0	1
Sleep	0	1	-	0	-	-	-
Deep Sleep	0	1	-	1	0	1	1

Note : 1. All the functions listed above runs only when ACPI Register Index 13h-10h, bit9 has been enabled. Please refer to section 5.1 for more details.
2. Soft_STPCLK = 1 means the access of reading IO port 0B2h and index 7Bh bit 2.
3. R_LVL2 = 1 means the access of reading ACPI IO index 014h.
4. R_LVL3 = 1 means the access of reading ACPI IO index 015h.

Register Index : **7Ch**
Register Name : **BESI - Break Event for STPCLKJ I**
Attribute : Read/Write
Default Value : 00h
This register is used to define the break event for STPCLKJ. The break event is used to wake up the system from STPGNT state or STPCLK state of Pentium, or STPGNT, SLEEP or DEEP SLEEP of Pentium II. Also it will affect the Clock Throttle function enabled by M7101 Register Index 5Bh bit6 and bit3. Besides, there are other options for break event, please refer to register index 0D9h.

Bit	Description
7 (0b)	Enable/Disable Break Event of PCI_Master. 0 : Disable. 1 : Enable. This break event is defined as PCI_Master event. When there is PCI_Master activity detected by chip, a break event happens.
6 (0b)	Enable/Disable Break Event of All Devices. 0 : Disable. 1 : Enable. This break event is defined as all the devices event defined by M7101 Register Index 63h-60h. When there is any defined activity detected by chip, a break event happens.
5 (0b)	Enable/Disable Break Event of PWRBTNJ. 0 : Disable. 1 : Enable. This break event is defined as PWRBTNJ from high level to low level. When there is a PWRBTNJ edge detected by chip, a break event happens.
4 (0b)	Enable/Disable Break Event of INTR. 0 : Disable. 1 : Enable. This break event is defined as INTR from low level to high level. When there is an INTR edge detected by chip, a break event happens.
3 (0b)	Enable/Disable Break Event of IRQ[1-7], IRQ[9-15], NMI, INIT and SMI. 0 : Disable. 1 : Enable. This break event is defined as IRQ[1-7], IRQ[9-15], NMI, INIT and SMI events. When there is any IRQ[1-7], IRQ[9-15], NMI, INIT and SMI edge detected by chip, a break event happens.
2 (0b)	Enable/Disable Break Event of IRQ8J. 0 : Disable. 1 : Enable. This break event is defined as IRQ8J from high level to low level. When there is an IRQ8J edge detected by chip, a break event happens.
1 (0b)	Enable/Disable Break Event of IRQ[0]. 0 : Disable. 1 : Enable. This break event is defined as IRQ[0] from low level to high level. When there is an IRQ[0] edge detected by chip, a break event happens.
0 (0b)	Enable/Disable Break Event of PCI Access. 0 : Disable. 1 : Enable. This break event is defined as PCI access. When there is a PCI cycle detected by chip, a break event happens.

Register Index : **7Dh**
Register Name : **DCGPIO - Direction Control of GPIO[7:0].**
Attribute : Read/Write
Default Value : 00h
This register is used to select the function for GPIO[7:0]. 0 is selected as GPI, 1 is selected as GPO.

Bit	Description
7 (0b)	Direction of GPIO[7]. 0 : GPIO[7] is a General purpose input pin. 1 : GPIO[7] is a General purpose output pin.
6 (0b)	Direction of GPIO[6]. 0 : GPIO[6] is a General purpose input pin. 1 : GPIO[6] is a General purpose output pin.
5 (0b)	Direction of GPIO[5]. 0 : GPIO[5] is a General purpose input pin. 1 : GPIO[5] is a General purpose output pin.
4 (0b)	Direction of GPIO[4]. 0 : GPIO[4] is a General purpose input pin. 1 : GPIO[4] is a General purpose output pin.
3 (0b)	Direction of GPIO[3]. 0 : GPIO[3] is a General purpose input pin. 1 : GPIO[3] is a General purpose output pin.
2 (0b)	Direction of GPIO[2]. 0 : GPIO[2] is a General purpose input pin. 1 : GPIO[2] is a General purpose output pin.
1 (0b)	Direction of GPIO[1]. 0 : GPIO[1] is a General purpose input pin. 1 : GPIO[1] is a General purpose output pin.
0 (0b)	Direction of GPIO[0]. 0 : GPIO[0] is a General purpose input pin. 1 : GPIO[0] is a General purpose output pin.

Register Index : **7Eh**
Register Name : **DOGPIO - Data Output to GPIO[7:0] when pin GPIO[n] is set as General Purpose Output Pin**
Attribute : Read/Write
Default Value : 00h
The output values of GPIO[7:0] are decided by this register when GPIO[7:0] are set as GPO pins.

Bit	Description
7 (0b)	Data of GPIO[7].
6 (0b)	Data of GPIO[6].
5 (0b)	Data of GPIO[5].
4 (0b)	Data of GPIO[4].
3 (0b)	Data of GPIO[3].
2 (0b)	Data of GPIO[2].
1 (0b)	Data of GPIO[1].
0 (0b)	Data of GPIO[0].

Register Index : **7Fh**
Register Name: **Data Input from GPIO[7:0] when pin GPIO[n] is set as General Purpose Input Pin**
Attribute : Read
Default Value : xxh
The register will reflect the GPIO[7:0] input values when GPIO[7:0] are set as GPI pins.

Bit	Description
7	Data input of GPIO[7].
6	Data input of GPIO[6].
5	Data input of GPIO[5].
4	Data input of GPIO[4].
3	Data input of GPIO[3].
2	Data input of GPIO[2].
1	Data input of GPIO[1].
0	Data input of GPIO[0].

*SWITCH control
Register Index : **82h-80h**
Register Name : **COESI - Control of External SWITCH I**
Attribute : Read/Write
Default Value : 000000h
This register is used to define the external switch event for the pins THRMJ. Please refer to M7101 Register Index 4Dh-4Ch for more details.

Bit	Description
23-17 (00h)	Reserved.
16 (0b)	Set Edge/Level trigger of THRMJ 0 : Edge trigger 1 : Level trigger
15 (0b)	Status of Pin THRMJ. This bit is used to refect the pin status of THRMJ.
14 (0b)	Detects Rising Edge of THRMJ. When this bit is set to 1, and a THRMJ rising edge has been detected, an external switch event will be issued.
13 (0b)	Detects Falling Edge of THRMJ. When this bit is set to 1, and a THRMJ falling edge has been detected, an external switch event will be issued.
12 (0b)	Enable/Disable Debounce Circuit of THRMJ. 0 : Disable. 1 : Enable. This bit is used to enable the debounce circuit for the pin THRMJ. BIOS should set this bit depending on the board implementation.
11-0 (0b)	Reserved.

Register Index : **83h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **87h-84h**
Register Name : **COEGI - Control of Extended GPI I**
Attribute : Read/Write
Default Value : 00h

Bit	Description
31	Status of pin EGPI7
30	Detect rising edge / high level of EGPI 7
29	Detect falling edge / low level of EGPI 7
28	Enable/ disable of debounce circuit of EGPI7
27	Status of pin EGPI6
26	Detect rising edge / high level of EGPI 6
25	Detect falling edge / low level of EGPI 6
24	Enable/ disable of debounce circuit of EGPI6
23	Status of pin EGPI5
22	Detect rising edge / high level of EGPI 5
21	Detect falling edge / low level of EGPI 5
20	Enable/ disable of debounce circuit of EGPI5
19	Status of pin EGPI4
18	Detect rising edge / high level of EGPI 4
17	Detect falling edge / low level of EGPI 4
16	Enable/ disable of debounce circuit of EGPI4
15	Status of pin EGPI3
14	Detect rising edge / high level of EGPI 3
13	Detect falling edge / low level of EGPI 3
12	Enable/ disable of debounce circuit of EGPI3
11	Status of pin EGPI2
10	Detect rising edge / high level of EGPI 2
9	Detect falling edge / low level of EGPI 2
8	Enable/ disable of debounce circuit of EGPI2
7	Status of pin EGPI1
6	Detect rising edge / high level of EGPI 1
5	Detect falling edge / low level of EGPI 1
4	Enable/ disable of debounce circuit of EGPI1
3	Status of pin EGPI0
2	Detect rising edge / high level of EGPI 0
1	Detect falling edge / low level of EGPI 0
0	Enable/ disable of debounce circuit of EGPI0

Register Index : **8Bh-88h**
Register Name : **COEGII - Control of Extended GPI II**
Attribute : Read/Write
Default Value : 00h

Bit	Description
31	Status of pin EGPI15
30	Detect rising edge / high level of EGPI15
29	Detect falling edge / low level of EGPI15
28	Enable/ disable of debounce circuit of EGPI15
27	Status of pin EGPI14
26	Detect rising edge / high level of EGPI14
25	Detect falling edge / low level of EGPI14
24	Enable/ disable of debounce circuit of EGPI14
23	Status of pin EGPI13
22	Detect rising edge / high level of EGPI13
21	Detect falling edge / low level of EGPI13
20	Enable/ disable of debounce circuit of EGPI13
19	Status of pin EGPI12
18	Detect rising edge / high level of EGPI12
17	Detect falling edge / low level of EGPI12
16	Enable/ disable of debounce circuit of EGPI12
15	Status of pin EGPI11
14	Detect rising edge / high level of EGPI11
13	Detect falling edge / low level of EGPI11
12	Enable/ disable of debounce circuit of EGPI11
11	Status of pin EGPI10
10	Detect rising edge / high level of EGPI10
9	Detect falling edge / low level of EGPI10
8	Enable/ disable of debounce circuit of EGPI10
7	Status of pin EGPI9
6	Detect rising edge / high level of EGPI9
5	Detect falling edge / low level of EGPI9
4	Enable/ disable of debounce circuit of EGPI9
3	Status of pin EGPI8
2	Detect rising edge / high level of EGPI8
1	Detect falling edge / low level of EGPI8
0	Enable/ disable of debounce circuit of EGPI8

Register Index : **8Eh-8Ch**
Register Name : **COESII - Control of External Switch II**
Attribute : Read/Write
Default Value : 000000h
This register is used to define the external switch event for the pins ACPWR, and DOCKJ. Please refer to M7101 Register Index 4Dh-4Ch for more details.

Bit	Description
23-13 (000h)	Reserved.
12 (0b)	Set Edge /Level trigger of ACPWR. 0 : Edge trigger 1 : Level trigger
11 (0b)	Status of Pin AC Power. This bit is used to reflect the pin status of ACPWR.
10 (0b)	Detect Rising Edge/High Level of AC Power. When 8Ch D12 =0, this bit is set to 1 and an ACPWR rising edge has been detected, an external switch event will be issued. When 8Ch D12 =1, this bit is set to 1 and an ACPWR high level has been detected, an external switch event will be issued.
9 (0b)	Detect Falling Edge/Low Level of AC Power. When 8Ch D12 =0, this bit is set to 1 and an ACPWR falling edge has been detected, an external switch event will be issued. When 8Ch D12 =1, this bit is set to 1 and an ACPWR low level has been detected, an external switch event will be issued.
8 (0b)	Enable/Disable Debounce Circuit of AC Power. 0 : Disable. 1 : Enable. This bit is used to enable the debounce circuit for the pin ACPWR. BIOS should set this bit depending on the board implementation.
7-4 (0h)	Reserved.
3 (0b)	Status of Pin DOCKJ. This bit is used to reflect the pin status of DOCKJ.
2 (0b)	Detect Rising Edge/High Level of DOCKJ. When 90h D1 =0, this bit is set to 1 and a DOCKJ rising edge has been detected, an external switch event will be issued. When 90h D1 =0, this bit is set to 1 and a DOCKJ high level has been detected, an external switch event will be issued.
1 (0b)	Detect Falling Edge/Low Level of DOCKJ. When 90h D1 =0, this bit is set to 1 and a DOCKJ falling edge has been detected, an external switch event will be issued. When 90h D1 =1, this bit is set to 1 and a DOCKJ low level has been detected, an external switch event will be issued.
0 (0b)	Enable/Disable Debounce Circuit of DOCKJ. 0 : Disable. 1 : Enable. This bit is used to enable the debounce circuit for the pin DOCKJ. BIOS should set this bit depending on the board implementation.

Register Index : **8Fh**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **90h**
Register Name : **CGPESI - Control of General Purpose External Switch I**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-4 (0h)	Reserved.
3 (0b)	Select Level/Edge Trigger of PWRBTNJ. 0 : Edge. 1 : Level. This bit is used to select the trigger function for the pin PWRBTNJ. When this bit is reset as 0, edge trigger function is selected. When this bit is reset as 1, level trigger function is selected.
2 (0b)	Select Active Level for Modem Ring In. 0 : Active High. 1 : Active Low. This bit is used to select the active level for pin RI. When this bit is reset as 0, active high level is selected. Otherwise, active low level is selected.
1 (0b)	Set Edge /Level trigger of DOCKJ 0 : Edge trigger 1 : Level trigger
0 (0b)	Select PWRBTNJ Mode. 0 : The falling edge of PWRBTNJ will generate SMIJ first. If it is asserted over four seconds, a hardware Soft-Off proceeds automatically. 1 : Generating XSMIJ at the rising edge of PWRBTNJ if it is not asserted over four seconds. If it is asserted over four seconds before the rising edge, a hardware Soft-Off proceeds automatically.

Register Index : **91h**
Register Name : **CGPESII - Control of General Purpose External Switch II**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-2 (00h)	Reserved
1 (0b)	Select DOCKJ/SLPBTNJ multi-function 0 : DOCKJ 1 : SLPBTNJ
0 (0b)	Reserved

Register Index : **93h-92h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **97h-94h**
Register Name : **MGA - Memory Group A**
Attribute : Read/Write
Default Value : 00000000h
This register is used to define Memory Group A address. Bits[31:14] are the memory address bits A[31:14], and A[23:14] can be masked by bits[13:4]. Chip will decode memory address and issue Memory Group A event if the address matches the programmed value.

Bit	Description
31-14 (00000h)	Address of A[31:14].
13-4 (000h)	Mask of Address A[23:14].
3-0 (0h)	Reserved.

Register Index : **99h-98h**
Register Name : **SLEE- Select Level/Edge trigger of Extended GPI[15:0]**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15(0b)	0 : Sense edge of EGPI[15] 1 : Sense level of EGPI[15]
14(0b)	0 : Sense edge of EGPI[14] 1 : Sense level of EGPI[14]
13(0b)	0 : Sense edge of EGPI[13] 1 : Sense level of EGPI[13]
12(0b)	0 : Sense edge of EGPI[12] 1 : Sense level of EGPI[12]
11(0b)	0 : Sense edge of EGPI[11] 1 : Sense level of EGPI[11]
10(0b)	0 : Sense edge of EGPI[10] 1 : Sense level of EGPI[10]
9(0b)	0 : Sense edge of EGPI[9] 1 : Sense level of EGPI[9]
8(0b)	0 : Sense edge of EGPI[8] 1 : Sense level of EGPI[8]
7(0b)	0 : Sense edge of EGPI[7] 1 : Sense level of EGPI[7]
6(0b)	0 : Sense edge of EGPI[6] 1 : Sense level of EGPI[6]
5(0b)	0 : Sense edge of EGPI[5] 1 : Sense level of EGPI[5]
4(0b)	0 : Sense edge of EGPI[4] 1 : Sense level of EGPI[4]
3(0b)	0 : Sense edge of EGPI[3] 1 : Sense level of EGPI[3]
2(0b)	0 : Sense edge of EGPI[2] 1 : Sense level of EGPI[2]
1(0b)	0 : Sense edge of EGPI[1] 1 : Sense level of EGPI[1]
0(0b)	0 : Sense edge of EGPI[0] 1 : Sense level of EGPI[0]

Register Index : **A3h-9Ah**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **A5h-A4h**
Register Name : **IOGC - IO Group C**
Attribute : Read/Write
Default Value : 0000h
This register is used to define I/O Group C address. Bits[15:2] are the I/O address bits A[15:2], and A[3:2] can be masked by bits[1:0]. Chip will decode I/O address and issue I/O Group C event if the address matches the programmed value.

Bit	Description
15-2 (0000h)	Address of A[15:2].
1-0 (0h)	Mask of address A[3:2].

Register Index : **B1h-A6h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **B2h**
Register Name : **CSS - Current System State**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-1 (00h)	Reserved.
0 (0b)	System State. 0 : ON. 1 : Standby. This bit has two functions: The first one is used to reflect the system state in On or Standby. The second one is used to control Standby timer (defined in M7101 Register Index 54h). Writing a 1 to this bit will stop the Standby timer, and the timer will continue by writing a 0 to it.

Register Index : **B3h**
Register Name : **SC - Speaker Control**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7 (0b)	Reserved.
6 (0b)	Enable/Disable Speak Function. 0 : Disable speak function. 1 : Enable speak function. This bit is the total switch of Speak function. There are two control methods for the Speak function: The first one is through bits[5:4] and M7101 Register Index CAh writing. The second one is through the 4-beep function control defined in bits[3:0].
5-4 (0h)	Latency Time of Write Beep Function When Writing M7101 Register Index CAh. 00 : 125 ms. 01 : 62.5 ms. 10 : 31.25 ms. 11 : 15.625 ms. These two bits are used to select the latency time of the write Beep function. Writing M7101 Register Index CAh will cause a beep, and the beep latency time is decided by these two bits.
3-2 (0h)	4-beep Function Control. 00 : Disable 4-beep function. 01 : 4 beeps in 1 sec. 10 : 4 beeps in 2 sec. 11 : 4 beeps in 4 sec. These two bits are used to control the 4-beep function. When the function is enabled, there will be four beeps in the programmed period of time.
1-0 (0h)	Interval Time of Periodic 4-beep Function. 00 : 60 sec. 01 : 30 sec. 10 : 15 sec. 11 : Reserved. These two bits are used to define the interval time if the periodic 4-beep function is enabled. Combining with the program of bits[3:2], software can generate 4-beep function with different periods and interval of time.

Register Index : **B4h**
Register Name: **SLED - Suspend LED (Resume Block)**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7 (0b)	Reserved.
6-4 (0h)	Debounce Clock of Debounce Circuits of All External Pins. 000 : 128 Hz. 001 : 64 Hz. 010 : 32 Hz. 011 : 16 Hz. 100 : 8 Hz. 101 : 4 Hz. 110 : 2 Hz. 111 : 1 Hz. These three bits are used to select the debounce clock for the debounce circuits of all external pins.
3 (0b)	Enable Power Saving of All Resume Switches. 0 : Disable. 1 : Enable. This bit is used to enable the gated off clock for internal circuit regarding all switches located in resume block.
2 (0b)	Power Button Override Enable/Disable. 0 : Enable. 1 : Disable. This bit is used to disbale ACPI Power Button Override function. When this bit is reset as 0, press Power Button over 4 seconds will force the system entering Soft Off Mode. When this bit is set to 1, press Power Button over 4 seconds will not force the system entering Soft Off Mode.
1-0 (0h)	Reserved.

Register Index : **B5h**
Register Name : **LEDC - LED Control**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-4 (0h)	Reserved.
3-2 (0h)	SQWO Control. 00 : Low. 01 : High. 10 : 1Hz. 11 : 2Hz. These two bits are used to control the pin SQWO output. When these two bits are reset as 00b, the output will become low. When these two bits are set as 01b, the output will become high. When these two bits are set as 10b, the output will become 1Hz wave. When these two bits are set as 11b, the output will become 2Hz wave.
1-0 (0h)	SPLED Control. 00 : Low. 01 : High. 10 : 1Hz. 11 : 2Hz. These two bits are used to control the pin SPLED output. When these two bits are reset as 00b, the output will become low. When these two bits are set as 01b, the output will become high. When these two bits are set as 10b, the output will become 1Hz wave. When these two bits are set as 11b, the output will become 2Hz wave.

Register Index : **B6h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **B7h**
Register Name : **RIC - Ring In Counter**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-4 (0h)	Reserved.
3-0 (0h)	Count. These four bits are used to set the count for the edge of Ring In pin. When RI edge count (from low to high) matches this programmed number, the Ring In event will be triggered internally. Writing a 1 to M7101 Register Index 90h bit2 can change to count from high to low level since RI pin has become active low.

Register Index : **B9h-B8h**
Register Name : **ODEGPO - Output Data of EGPO[15:0]**
Attribute : Read/Write
Default Value : 00h

Bit	Description
15-0 (00h)	These registers are used to control the output data of extended General Purpose Output pins EGPO[15:0]. Please refer to section 1.4 about the extended GPIO implementation.

Register Index : **BBh-BAh**
Register Name : **IDEGPI - Input Data of EGPI[15:0]**
Attribute : Read Only
Default Value : 00h

Bit	Description
15-0 (00h)	These registers are used to reflect the input data of extended General Purpose Input pins EGPI[15:0]. Please refer to section 1.4 about the extended GPIO implementation.

Register Index : **BCh**
Register Name : **SRIO70 - Shadow Register of IO Port 70h**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-0 (00h)	This register has the same value as IO port 70h. In SMM routine, writing to I/O port 70h does not change this register value. And the value of port 70h will be updated as this register value when exiting SMM routine.

Register Index : **BDh**
Register Name : **PCCA - PMU Class Code Attribute**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-4 (0h)	Reserved.
3 (0b)	PMU Class Code Writable Enable/Disable. 0 : Enable. 1 : Disable. This bit is used to program the PMU Class Code register as Readable/Writeable (0) or read-only (1).
2 (0b)	Select 24/32 Bits PM Timer. 0 : 24 Bits. 1 : 32 Bits. The bit is used to select ACPI PM timer is 24 bits or 32 bits. 32bits timer is suggested for the most updated ACPI specification.
1-0 (0h)	ACPI 24/32 Bits Timer Test Mode Select (for Testing). 0 : Normal Mode. 1 : Test Mode. This bit is used for the ACPI 24/32 bits timer test mode. For normal operation, it must be in normal mode.

Register Index : **BEh**
Register Name : **PSANS - Power Saving of All Normal Switches**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-2 (00h)	Reserved.
1 (0b)	Enable Power Saving of All Normal Switches. 0 : Disable. 1 : Enable. This bit is used to enable the gated off clock for internal circuit regarding all normal switches located in non resume block.
0 (0b)	Disable Internal USB SMIACKJ. 0 : Enable. 1 : Disable. This bit is used to control the SMIACKJ to USB block. M7101 Register Index 77h bit 6 is programmed to notify the whole chip that SMIACKJ has been asserted. Before it goes into USB block, it will qualify by this bit setting. When this bit is set to 1, USB SMIACKJ will be masked.

Register Index : **BFh**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

* GPO and GPI functions
Register Index : **C2h-C0h**
Register Name : **DOGPOI - Data Output to GPO Pins**
Attribute : Read/Write
Default Value : 000000h
This register is used to control the output data of GPO[20:18], GPO[12], GPO[9], and GPO[3:0].

Bit	Description
23-21 (0h)	Reserved.
20 (0b)	GPO[20].
19 (0b)	GPO[19].
18 (0b)	GPO[18].
17 (0b)	Reserved.
16 (0b)	Reserved.
15 (0b)	Reserved.
14 (0b)	Reserved.
13 (0b)	Reserved.
12 (0b)	GPO[12].
11-10 (0h)	Reserved.
9 (0b)	GPO[9].
8-4 (00h)	Reserved.
3 (0b)	GPO[3].
2 (0b)	GPO[2].
1 (0b)	GPO[1].
0 (0b)	GPO[0].

Register Index : **C3h**
Register Name : **ODGPOII - Data Output for GPO[23:22]**
Attribute : Read/Write
Default Value : 00h
This register is used to control the output data of GPO[23:22].

Bit	Description
7-3 (0h)	Reserved.
2 (0b)	GPO[23].
1 (0b)	GPO[22].
0 (0b)	Reserved.

Register Index : **C5h-C4h**
Register Name : **IDGPI - Input Data of GPI[11:0]**
Attribute : Read
Default Value : 0xxxh
This register value reflects the input data of GPI[11:9], GPI[3:2], and GPI[0].

Bit	Description
15-12	Reserved.
11	GPI[11].
10	GPI[10].
9	GPI[9].
8-4	Reserved.
3	GPI[3].
2	GPI[2].
1	Reserved.
0	GPI[0].

Register Index : **C6h**
Register Name : **SMIRB - Select Multifunctions in Resume Block**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-3 (00h)	Reserved.
2 (0b)	OFF_PWR2/GPO[23] Select. 0 : OFF_PWR2. 1 : GPO[23]. This bit is used to select the function for the multifunction pin OFF_PWR2/GPO[23]. When it is reset as 0, OFF_PWR1 is selected. Otherwise, GPO[23] is selected.
1 (0b)	OFF_PWR1/GPO[22] Select. 0 : OFF_PWR1. 1 : GPO[22]. This bit is used to select the function for the multifunction pin OFF_PWR1/GPO[22]. When it is reset as 0, OFF_PWR1 is selected. Otherwise, GPO[22] is selected.
0 (0b)	Reserved.

Register Index : **C7h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **C8h**
Register Name : **MMEAT - Mask Monitored Events of All Timers**
Attribute : Read/Write
Default Value : 00h
When this register value is programmed as 00h, all timers can be reset by their monitored event. When this register value is programmed as 01h, all timers cannot be reset by their monitored event, which means all the monitored events defined in Index 60h-65h will be masked, which means all the monitored events defined in M7101 Register Index 65h-60h will be masked.

Register Index : **C9h**
Register Name : **LRWACR - Lock Read/Write of All Configure Registers**
Attribute : Read/Write
Default Value : 00h
When this register value is programmed as 00h, all configuration registers of M7101 from Index 40h-FFh can be read/write. When this register value is programmed as 01h, all configuration registers of M7101 from Index 40h-FFh cannot be read/write except Index C9h.

Register Index : **CAh**
Register Name : **WBP - Write Beep Port**
Attribute : Write Only
Write to this port will cause a beep, and the latency time of the beep will be decided by M7101 Register Index B3h bits[5:4].

Register Index : **D3h-CEh, CBh**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **0CDh-0CCh**
Register Name : **DCC- Dynamic Clock Control**.
Attribute : R/W
Default Value : 0000h

Bit	Description
15-14	Reserved.
13	Enable/disable STPCLKJ mask PHOLDJ.
12	Enable/disable Dynamic Clock Control.
11-10	Reserved.
9-8	Select time threshold for STPGNT/SLEEP(P-II)/STPCLK active time. 00 : 1-2 ms. 01 : 2-3 ms. 10 : 3-4 ms. 11 : 4-5 ms.
7-5	Reserved.
4	Enable/disable checking asserted time of ZZ. 0 : Disable. 1 : Enable. STPGNT is issued instead of STPCLK when ZZ is shorter than the time set at bits 9-8.
3	Enable/disable Monitor master cycle and the last 15 ms after it is de-asserted. 0 : Disable. 1 : Enable. STPGNT is issued instead of STPCLK when the condition matches.
2	Enable/disable Monitor master cycles before STPCLKJ is asserted. 0 : disable. 1 : Enable. STPGNT is issued instead of STPCLK if a master cycle is monitored.
1	Enable/disable monitor DMA_ON. 0 : Disable. 1 : Enable. STPGNT is issued instead of STPCLK if DMA_ON is active. Note : DMA_ON is asserted when any access to IO 00h-1Fh or 0C0h-0DFh and de-asserted at the rising edge of PHOLDJ.
0	Enable/disable monitor MOTOR_ONJ. 0 : Disable. 1 : Enable. STPGNT is issued instead of STPCLK if MOTOR_ONJ is active.

Register Index : **D4h**
Register Name : **STM - Suspend TEST Mode Disable/Enable**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-1 (00h)	Reserved
0 (0b)	Suspend Mode Test Disable/Enable 0 : Disable. 1 : Enable. This bit is for the Suspend Mode Test only. During normal operation, it must not be enabled.

Register Index : **D5h**
Register Name : **HSSI - Hardware Setting Status bits I (Resume)**
Attribute : Read only
Default Value : xxh

Bit	Description
7	PCSJ hardware setting status. (powerpcj) 0 : Pull-low, POWER PC mode 1 : Pull-high, INTEL PC mode
6	XPHOLDJ hardware setting status.(usb_testj) 0 : Pull-low, USB in test mode. 1 : Pull-high, USB in normal mode. Test isolate USB mode: Hardware setting : ROMKBCSJ pull-low and XPHOLDJ pull-low, then USB test mode is enabled. The multiplexed pins are: TEST_I_SIG1 <----- XIO16J (i) TEST_I_SIG2 <----- XIRQ8J (i) TEST_I_SIG3 <----- XSIRQII (i) TST_SER_DATA_IN <----- XEXTSW (i) I_IRQ1IN <----- XIERQ0 (i) I_IRQ12IN <----- XIERQ1 (i) TEST_O_SIG1 <----- XDACK0J[5] (o) TEST_O_SIG2 <----- XDACK0J[6] (o) TEST_O_SIG3 <----- XDACK0J[7] (o) TEST_O_SIG4 <----- XDACK1J[3] (o) TEST_O_SIG5 <----- XDACK1J[2] (o) TEST_O_SIG6 <----- XDACK1J[1] (o) TEST_O_SIG7 <----- XDACK1J[0] (o) O_PCIINTJ <----- XPCSJ (o) O_USBREQJ <----- XPHOLDJ (o) -- mux in pci_arb.sch I_USBGNTJ <----- XPHLDAJ (i) -- mux in pci_arb.sch
5	Reserved. //SQWO hardware setting status.(en_apicj)
4	SPLED hardware setting status.(rom256kbj) 0 : Pull-low, supports 256KB ROM 1 : Pull-high, does not support 256KB ROM
3	XDIR hardware setting status. (pro_cpuj) 0 : Pull-low, Pentium II CPU is used. 1 : Pull-high, Pentium CPU is used.
2:	TC hardware setting status. (internal_sdj) 0 : Pull-low, pins SD/GPIO[7:0] are SD[7:0]; external LS245 is not required. 1 : Pull-high, pins SD/GPIO[7:0] are GPIO[7:0]; external LS245 is required.
1	SPKR hardware setting status.(sio_testj) 0 : Pull-low, on_chip super I/O test mode enabled 1 : Pull-high, on_chip super I/O test mode disabled,
0	ROMKBCSJ hardware setting status. (testj) 0 : Pull-low, chip test mode is enabled. (for test only) 1 : Pull-high, chip test mode is disabled.

Register Index : **0D6h**
Register Name : **HSSII- Hardware Setting Status bits II**. (Resume)
Attribute : Read only
Default Value : xxh

Bit	Description
7-2	Reserved.
1	CLK32KO hardware setting status. 0 : Pull low, 32KHz clock test mode from input signal. 1 : Pull high, 32KHz clock from crystal oscillator.
0	ACPWR hardware setting status. 0 : Pull low, AT Power supply is supported. (Normal) 1 : Pull high, ATX Power supply is supported. (Suspend)

Register Index : **D7h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **D8h**
Register Name : **DSC - Delay SMI Control**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7 (0b)	Enable/Disable HDD Monitored Access of 1F0-1F7h, 3F6h, 170-177h and 376h. 0 : Disable. 1 : Enable. This bit is used to enable I/O Ports 1F0-1F7h, 3F6h, 170-177h, and 376h decoded as HDD event. Please refer to M7101 Register Index 46h-44h bits[6:5] for more details.
6 (0b)	Enable/Disable of Sleeping State Stop External PCICLK. 0 : Disable. 1 : Enable. During entering Power On Suspend state, the internal resume block clock will change from PCICLK to 32K since the external PCICLK clock will be stopped by assertion of PCI_STPJ. This bit is used to control the timing of PCI_STPJ. When this bit is disabled, PCI_STPJ will assert immediately to stop PCICLK. When this bit is enabled, PCI_STPJ will be synchronized by 32K before it is asserted to stop external PCICLK.
5 (0b)	Subsystem Vendor ID Write Enable/Disable. 0 : Enable. 1 : Disable.
4 (0b)	IRQ[1]/IRQ[12] Source Select. 0 : IRQ[1] & IRQ[12]. 1 : KBCLK & MSCLK. This bit is used to change the Keyboard resume event source. When this bit is 0, IRQ[1] & IRQ[12] coming from 8259 are selected. When this bit is 1, KBCLK and MSCLK pins are selected as the source. This bit must be used with 7101 Register Index 6Fh-6Ch bits[28:27] if internal KB/Mouse Controller is disabled.
3 (0b)	Enable CPU_STPJ Monitor PHOLDJ. 0 : Disable. 1 : Enable. When this bit is enabled, CPU_STPJ will be inactive when PHOLDJ is asserted. Otherwise, CPU_STPJ will not qualify the signal PHOLDJ.
2 (0b)	Enable Delayed SMI of ACPWR. 0 : Disable. 1 : Enable. This bit is used to enable SMI delay function for ACPWR. Please refer to 7101 Register Index 77h bits[1:0] for more details.
1 (0b)	Reserved.
0 (0b)	Enable Delayed SMI of THRMJ and DOCKJ. 0 : Disable. 1 : Enable. This bit is used to enable SMI delay function for THRMJ and DOCKJ. Please refer to 7101 Register Index 77h bits[1:0] for more details.

Register Index : **D9h**
Register Name : **BESII – Break Event for STPCLKJ II**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-6 (00b)	Reserved
5 (0b)	Enable IRQ[15-14] to be break event 0 : Disable 1 : Enable
4 (0b)	Enable IRQ[11-10] to be break event 0 : Disable 1 : Enable
3 (0b)	Enable IRQ[7,9] to be break event 0 : Disable 1 : Enable
2 (0b)	Enable IRQ[6-5] to be break event 0 : Disable 1 : Enable
1 (0b)	Enable IRQ[4-3] to be break event 0 : Disable 1 : Enable
0 (0b)	Enable IRQ[12,1] to be break event 0 : Disable 1 : Enable

Register Index : **DFh-DAh**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

Register Index : **E0h**
Register Name : **SMBHSI - SMBus Host & Slave Interface Configuration**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-2 (00h)	Reserved.
1 (0b)	Slave Interface of Internal SMBus Controller Enable. 0 : Disable. 1 : Enable. This bit is used to program the internal SMBus controller as a Host or a Slave Controller. When it is a Host, it will drive SMBus. Otherwise, it will receive the incoming command driven by another SMBus Host controller. Please refer to 7101 Register Index E1h for more details.
0 (0b)	SMB Host Controller Interface Enable. 0 : Disable. 1 : Enable. This bit is used to enable the internal SMBus controller.

Register Index : **E1h**
Register Name : **SMBHSC - SMBus Host Slave Command Register**
Attribute : Read/Write
Default Value : 00h
While SMB controller is program as a slave device on the SMBus and the register matches the receiving command data, the internal SMB controller will process the cycle and generate SMI or Interrupt event after the access.

Bit	Description
7-0 (00h)	SMB Host Slave Command Port.

Register Index : **E2h**
Register Name : **SMBHCBC - SMBus Host Controller Base Clock Setting**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7-5 (001b)	SMB Clock Select. [7:5] : "clock" 000 : 149K 001 : 74K (recommended) 010 : 37K 100 : 223K 101 : 111K 110 : 55K These three bits are used to select the base clock for internal state machine. All the timings will be based on this clock. The clock is derived from OSC14M.
4-3 (0h)	Idle Delay Setting. [4:3] : "idle time" 00 : BaseClk*64 53.76 us ref. 1.19M base clock. (default) 01 : BaseClk*32 10 : BaseClk*128 Others : Reserved These two bits are used to decide the idle time to qualify SMBus is in idle state. The time is calculated based on the base clock defined in bits[7:5].
2-0 (0h)	Reserved.

Register Index : **FFh-E3h**
Register Name : **Reserved Register**
Attribute : Read only
Default Value : 00h

4.2 Other I/O and Memory Spaces

4.2.1 DMA Register Description

a. Command Register, it is the same as 82C37.
b. DMA Channel Mode Register, it is the same as 82C37.
c. DMA Channel Extended Mode Register,
Channels 0-3 port address - 040Bh.
Channels 4-7 port address - 04D6h.

Bit No.	Description
7-6 (00b)	Reserved.
5-4 (00b)	DMA Cycle Timing Mode. 00 : Compatible Timing. 01 : Compatible Timing. 10 : Compatible Timing. 11 : Type F.
3-2 (00b)	Reserved.
1-0 (00b)	DMA Channel Select. 00 : Channel 0(4) select. 01 : Channel 1(5) select. 10 : Channel 2(6) select. 11 : Channel 3(7) select.

Compatible Timing : runs at 9 SYSCLKs (1080 nsec/ single cycle) and 8 SYSCLKs (960 nsec/cycle) during the repeated portion of a BLOCK or DEMAND mode.
Type F Timing : runs at 3 SYSCLKs (360 nsec/single cycle) and 2 SYSCLKs (240 nsec/ cycle) during the repeated portion of a BLOCK or DEMAND mode.

d. DMA Request Register, it is the same as 82C37.
e. Mask Register-Write Single Mask Bit, it is the same as 82C37.
f. Mask Register-Write All Mask Register Bits, it is the same as 82C37.
g. Status Register, it is the same as 82C37.
h. DMA Base and Current Address Register 8237 Compatible Segment.
i. DMA Base and Current Byte/Word Count Register 8237 Compatible Segment.
j. DMA Memory Low/High Page Register.
DMA Memory Base Low Page Register.
DMA Channel 0 port address - 087h.
DMA Channel 1 port address - 083h.
DMA Channel 2 port address - 081h.
DMA Channel 3 port address - 082h.
DMA Channel 5 port address - 08Bh.
DMA Channel 6 port address - 089h.
DMA Channel 7 port address - 08Ah.
DMA Memory Base High Page Register.
(Before using 32-bit addressing, the M1543C Register Index 42h bit6 must be set to '1'.)
DMA Channel 0 port address - 487h.
DMA Channel 1 port address - 483h.
DMA Channel 2 port address - 481h.
DMA Channel 3 port address - 482h.
DMA Channel 5 port address - 48Bh.
DMA Channel 6 port address - 489h.
DMA Channel 7 port address - 48Ah.
These bits form the full 32-bit address for a DMA transfer.
k. Clear Byte Pointer Flip-Flop, it is the same as 82C37.
l. Master Clear, it is the same as 82C37.
m. Clear Mask Register, it is the same as 82C37.

4.2.1.2 TIMER UNIT Register Description

a. Timer Control Word Register, it is the same as 82C54.
b. Interval Timer Read Back Command, it is the same as 82C54.
c. Interval Timer Status Byte Format, it is the same as 82C54.
d. Counter Latch Command Register, it is the same as 82C54.
e. Counter Access Ports, it is the same as 82C54.

4.2.1.3 INTERRUPT UNIT Register Description

Initialization Command Word 1 (ICW1) :

Port 020h (W/O) -- INT Controller 1
Port 0A0h (W/O) -- INT Controller 2

Bit No.	Description
7-5	Reserved.
4	Must be 1.
3	0 : Edge triggered interrupts for all channels. 1 : Level triggered interrupts for all channels. This bit is used to define the trigger by edge or level.
2	Reserved
1	0 : Cascade Controller. (The M1543C must write 0) 1 : Single Controller.
0	0 : No ICW4 needed. 1 : ICW4 is needed. (The M1543C must write 1)

Initialization Command Word 2 (ICW2):

Port 021h (W/O) -- INT Controller 1
Port 0A1h (W/O) -- INT Controller 2

Bit No.	Description
7-3	Interrupt Vector Address.
2-0	Reserved.

Initialization Command Word 3 (ICW3):

Port 021h (W/O) -- INT Controller 1

The M1543C must be programmed to 04h, indicating INT of CTRL-2 is cascaded to IRQ[2] of CTRL-1.

Bit No.	Description
7-0	0 : IR Input does not have a slave . 1 : IR Input has a slave.

Port 0A1h (W/O) -- INT Controller 2

The M1543C must be programmed to 02h, indicating CTRL-2 is cascaded to IRQ[2] of CTRL-1.

Bit No.	Description
7-3	Must be 0h.
2-0	Slave identification code.

Initialization Command Word 4 (ICW4) :

Port 021h (W/O) -- INT Controller 1
Port 0A1h (W/O) -- INT Controller 2

Bit No.	Description
7-5	Must be 0h.
4	0 : Not Specially Fully Nested Mode. 1 : Specially Fully Nested Mode.
3-2	0x : Non Buffered Mode. 10 : Buffer Mode/Slave. 11 : Buffer Mode/Master.
1	0 : Normal EOI. 1 : Auto EOI.
0	0 : MCS-80/85 Mode. 1 : 80x86 Mode. (M1543C must write 1)

Operation Command Word 1 (OCW1) :

Port 021h (R/W) -- INT Controller 1
Port 0A1h (R/W) -- INT Controller 2

Bit No.	Description
7-0	0 : Reset IRQ<x> mask. 1 : Set IRQ<x> mask.

Operation Command Word 2 (OCW2) :
Port 020h (W/O) -- INT Controller 1
Port 0A0h (W/O) -- INT Controller 2

Bit No.	Description
7-5	EOI, SL, R. 000 : Rotate in Auto EOI Command(Clear). 001 : Non Specific EOI Command. 010 : Set Priority Command * L2-L0 are used. 011 : * Specific EOI Command. 100 : Rotate in Auto EOI Command (Set). 101 : Rotate Non Specific EOI Command. 110 : * Set Priority Command. 111 : * Rotate on Specific EOI Command.
4-3	Must be 00b to select OCW2.
2-0	L2,L1,L0 - Interrupt Level Select. 000 : IRQ<0(8)> select. 001 : IRQ<1(9)> select. 010 : IRQ<2(10)> select. 011 : IRQ<3(11)> select. 100 : IRQ<4(12)> select. 101 : IRQ<5(13)> select. 110 : IRQ<6(14)> select. 111 : IRQ<7(15)> select.

Operation Command Word 3 (OCW3) :

Port 020h (R/W) -- INT Controller 1
Port 0A0h (R/W) -- INT Controller 2

Bit No.	Description
7	Reserved, must be 0b.
6-5	0x : No Action. 10 : Reset Special Mask Mode. 11 : Set Special Mask Mode.
4-3	Must be 01b to select OCW3.
2	0 : No Poll Command. 1 : Poll Command.
1-0	0x : No Action. 10 : Read IRQ Register. 11 : Read IS Register.

Interrupt Unit Edge/Level Control Register (ELCR) :

Port 04D0h (R/W) -- INT Controller 1
Port 04D1h (R/W) -- INT Controller 2

Bit No.	Description
7	0 : IRQ<7(15)> Edge trigger. 1 : IRQ<7(15)> Level trigger.
6	0 : IRQ<6(14)> Edge trigger. 1 : IRQ<6(14)> Level trigger.
5	0 : IRQ<5(13)> Edge trigger. 1 : IRQ<5(13)> Level trigger.
4	0 : IRQ<4(12)> Edge trigger. 1 : IRQ<4(12)> Level trigger.
3	0 : IRQ<3(11)> Edge trigger. 1 : IRQ<3(11)> Level trigger.
2	0 : IRQ<2(10)> Edge trigger. 1 : IRQ<2(10)> Level trigger.
1	0 : IRQ<1(9)> Edge trigger. 1 : IRQ<1(9)> Level trigger.
0	0 : IRQ<0(8)> Edge trigger. 1 : IRQ<0(8)> Level trigger.

4.2.1.4 NMI Registers

NMI Enable/Disable and RTC Address register :

Port 70h, 72h
Attribute : Write Only
Default value : 0xxxxxxxb

Bit No.	Description
7	0 : Enable NMI interrupt. 1 : Disable all NMI sources.
6-0	RTC Memory addressing.

Note : When I/O write port 70h or 72h, pin RTCAS will be active. Port 72h is used to support 256byte RTC.

Port 71h, 73h
Note : When I/O write port 71h or 73h, pin RTCRW will be active (low). When I/O read port 71h or 73h, pin RTCDS will be active (low).

NMI Status and Control register(Port B):

Port 61h
Attribute : Read/Write
Default value : 00h

Bit No.	Description
7 (R only)	0 : No SERRJ from System Board. 1 : SERRJ active, NMI requested. To reset this interrupt, set bit 2 to 1.
6 (R only)	0 : No NMI Interrupt from IOCHKJ. 1 : IOCHKJ is active and NMI requested. To reset this interrupt, set bit 3 to 1.
5 (R only)	Timer Counter 2 OUT status.
4 (R only)	Toggled from 0 to 1 or 1 to 0 following every refresh cycle.
3 (R/W)	0 : IOCHKJ NMI enable. 1 : IOCHKJ NMI disable and clear.
2 (R/W)	0 : System board error enable. 1 : System board error disable and clear.
1 (R/W)	0 : Pin SPKR output is always '0'. 1 : Pin SPKR output is the Timer Counter 2 OUT signal value.
0 (R/W)	0 : Timer Counter 2 disable. 1 : Timer Counter 2 enable.

4.2.1.5 FAST RC/GATE-A20 Registers.

Port 92h
Default value : 24h
Attribute : Read/Write

Bit No.	Description
7	Reserved (must be read as a 0).
6	Reserved (must be read as a 0).
5	Reserved (must be read as a 1).
4	Reserved (must be read as a 0).
3	Reserved (must be read as a 0).
2	Reserved (must be read as a 1).
1	Directly reflects the A20MJ signal. 0 : A20MJ is driven inactive (low). 1 : A20MJ is driven active (high).
0	0 : Allow FAST RC to be pulsed. 1 : FAST RC is pulsed active.

4.2.2 USB OpenHCI Registers

The M5237 contains a set of on-chip registers which are mapped into a non-cacheable portion of the system addressable memory space. All the registers should be read and written as Dwords. The memory address is defined in M5237 PCI configuration register Index 13h-10h.

4.2.2.1 Operational Registers

Register Index : **03h-00h**
Register name : **HcRevision**
Attribute : Read only
Default value : 00000110h

Bit No.	Description
31-9(000000h)	Reserved.
8(0b)	Legacy. This read-only field is 1 to indicate that the legacy support registers are present in M5237.
7-0(10h)	Revision. Indicates the OpenHCI Specification revision number implemented by the Hardware. M5237 supports 1.0 specification. (X.Y = XYh)

Register Index : **07h-04h**
Register name : **HcControl**
Attribute : Read/Write
Default value : 00000000h

Bit No.	Description
31-11(000000h)	Reserved.
10(0b)	RemoteWakeupConnectedEnable. If a remote wakeup signal is supported, this bit enables that operation. Since there is no remote wakeup signal supported, this bit is ignored.
9(0b)	RemoteWakeupConnected. This bit indicated whether the HC supports a remote wakeup signal. This implementation does not support any such signal. The bit is hard-coded to '0.'
8(0b)	InterruptRouting. This bit is used for interrupt routing: 0 : Interrupts routed to normal interrupt mechanism (INT). 1 : Interrupts routed to SMI.
7-6(00b)	HostControllerFunctionalState. This field sets the Host Controller state. The Controller may force a state change from USBSUSPEND to USBRESUME after detecting resume signaling from a downstream port. States are: 00 : USBRESET 01 : USBRESUME 10 : USBOPERATIONAL 11 : USBSUSPEND
5(0b)	BulkListEnable. When set, this bit enables processing of the Bulk list.
4(0b)	ControlListEnable. When set, this bit enables processing of the Control list.
3(0b)	IsochronousEnable. When clear, this bit disables the Isochronous List when the Periodic List is enabled (so Interrupt EDs may be serviced). While processing the Periodic List, the Host Controller will check this bit when it finds an isochronous ED.
2(0b)	PeriodicListEnable. When set, this bit enables processing of the Periodic (interrupt and isochronous) list. The Host Controller checks this bit prior to attempting any periodic transfers in a frame.
1-0(00b)	ControlBulkServiceRatio. Specifies the number of Control Endpoints serviced for every Bulk Endpoint. Encoding is N-1 where N is the number of Control Endpoints (i.e. '00' = 1 Control Endpoint; '11' = 3 Control Endpoints)

Register Index : **0Bh-08h**
Register name : **HcCommandStatus**
Attribute : Read/Write
Default value : 00000000h

Bit No.	Description
31-18(0000h)	Reserved.
17-16(00b)	ScheduleOverrunCount. This field increments every time the SchedulingOverrun bit in HcInterruptStatus is set. The count wraps from '11' to '00'.
15-4(000h)	Reserved.
3(0b)	OwnershipChangeRequest. When set by software, this bit sets the OwnershipChange field in HcInterruptStatus. The bit is cleared by software.
2(0b)	BulkListFilled. Set to indicate there is an active ED on the Bulk List. The bit may be set by either software or the Host Controller and cleared by the Host Controller each time it begins processing the head of the Bulk List.
1(0b)	ControlListFilled. Set to indicate there is an active ED on the Control List. It may be set by either software or the Host Controller and cleared by the Host Controller each time it begins processing the head of the Control List.
0(0b)	HostControllerReset. This bit is set to initiate a software reset. This bit is cleared by the Host Controller upon completion of the reset operation.

Register Index : **0Fh-0Ch**
Register Name : **HcInterruptStatus**
Attribute : Read/Write
Default Value : 00000000h
(set by hardware and cleared by software)

Bit No.	Description
31(0b)	Reserved.
30(0b)	OwnershipChange. This bit is set when the OwnershipChangeRequest bit of HcCommandStatus is set.
29-7(000000h)	Reserved.
6(0b)	RootHubStatusChange. This bit is set when the content of HcRhStatus or the content of any HcRhPortStatus register has changed.
5(0b)	FrameNumberOverflow. Set when bit 15 of FrameNumber changes value.
4(0b)	UnrecoverableError. This event is not implemented and is hard-coded to '0'. Writes are ignored.
3(0b)	ResumeDetected. Set when Host Controller detects resume signaling on a downstream port.
2(0b)	StartOfFrame. Set when the Frame Management block signals a 'Start of Frame' event.
1(0b)	WritebackDoneHead. Set after the Host Controller has written HcDoneHead to HccaDoneHead.
0(0b)	SchedulingOverrun. Set when the List Processor determines a Schedule Overrun has occurred.

Register Index : **13h-10h**
Register Name : **HcInterruptEnable**
Attribute : Read/Write
Default Value : 00000000h
(Write '1' : sets the bit. Write '0' : leaves the bit unchanged.)

Bit No.	Description
31(0b)	MasterInterruptEnable. This bit is a global interrupt enable. A write of '1' allows interrupts to be enabled via the specific enable bits listed above.
30(0b)	OwnershipChangeEnable 0 : Ignore 1 : Enable interrupt generation due to Ownership Change.
29-7(000000h)	Reserved.
6(0b)	RootHubStatusChangeEnable 0 : Ignore 1 : Enable interrupt generation due to Root Hub Status Change.
5(0b)	FrameNumberOverflowEnable 0 : Ignore 1 : Enable interrupt generation due to Frame Number Overflow.
4(0b)	UnrecoverableErrorEnable. This event is not implemented. All writes to this bit are ignored.
3(0b)	ResumeDetectedEnable 0 : Ignore 1 : Enable interrupt generation due to Resume Detected.
2(0b)	StartOfFrameEnable 0 : Ignore 1 : Enable interrupt generation due to Start of Frame.
1(0b)	WritebackDoneHeadEnable 0 : Ignore 1 : Enable interrupt generation due to Writeback Done Head.
0(0b)	SchedulingOverrunEnable 0 : Ignore 1 : Enable interrupt generation due to Scheduling Overrun.

Register Index : **17h-14h**
Register Name : **HcInterruptDisable**
Attribute : Read/Write
Default Value : 00000000h
(Read : The current value of HcInterruptEnable register is returned.)
(Write '1' : clears the bit. Write '0' : leaves the bit unchanged.)

Bit No.	Description
31(0b)	MasterInterruptEnable. Global interrupt disable. A write of '1' disables all interrupts.
30(0b)	OwnershipChangeEnable 0 : Ignore 1 : Disable interrupt generation due to Ownership Change.
29-7(000000h)	Reserved.
6(0b)	RootHubStatusChangeEnable 0 : Ignore 1 : Disable interrupt generation due to Root Hub Status Change.
5(0b)	FrameNumberOverflowEnable 0 : Ignore 1 : Disable interrupt generation due to Frame Number Overflow.
4(0b)	UnrecoverableErrorEnable This event is not implemented. All writes to this bit will be ignored.
3(0b)	ResumeDetectedEnable 0 : Ignore 1 : Disable interrupt generation due to Resume Detected.
2(0b)	StartOfFrameEnable 0 : Ignore 1 : Disable interrupt generation due to Start of Frame.
1(0b)	WritebackDoneHeadEnable 0 : Ignore 1 : Disable interrupt generation due to Writeback Done Head.
0(0b)	SchedulingOverrunEnable 0 : Ignore 1 : Disable interrupt generation due to Scheduling Overrun.

Register Index : **1Bh-17h**
Register Name : **HcHCCA**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
31-8(000000h)	HCCA. Pointer to HCCA base address.
7-0(00h)	Reserved.

Register Index : **1Fh-1Ch**
Register Name : **HcPeriodCurrentED**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
31-4(0000000h)	PeriodCurrentED Pointer to the current Periodic List ED.
3-0(0h)	Reserved.

Register Index : **23h-20h**
Register Name : **HcControlHeadED**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
31-4(0000000h)	ControlHeadED. Pointer to the Control List Head ED.
3-0(0h)	Reserved.

Register Index : **27h-24h**
Register Name : **HcControlCurrentED**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
31-4(0000000h)	ControlCurrentED. Pointer to the current Control List ED.
3-0(0h)	Reserved.

Register Index : **2Bh-28h**
Register Name : **HcBulkHeadED**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
31-4(0000000h)	BulkHeadED Pointer to the Bulk List Head ED.
3-0(0h)	Reserved.

Register Index : **2Fh-2Ch**
Register Name : **HcBulkCurrentED**
Attribute : Read/Write
Default value : 00000000h

Bit No.	Description
31-4(0000000h)	BulkCurrentED. Pointer to the current Bulk List ED.
3-0(0h)	Reserved.

Register Index : **33h-30h**
Register Name : **HcDoneHead**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
31-4(0000000h)	DoneHead. Pointer to the current Done List Head ED.
3-0(0h)	Reserved.

Register Index : **37h-34h**
Register Name : **HcFmInterval**
Attribute : Read/Write
Default Value : 00002EDFh

Bit No.	Description
31(0b)	FrameIntervalToggle. This bit is toggled by HCD when it loads a new value into FrameInterval.
30-16(0000h)	FSLargestDataPacket. This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame.
15-14(0h)	Reserved.
13-0(2EDFh)	FrameInterval. This field specifies the length of a frame as (bit times - 1). For 12,000 bit times in a frame, a value of 11,999 is stored here.

Register Index : **3Bh-38h**
Register Name : **HcFrameRemaining**
Attribute : Read Only
Default Value : 00000000h

Bit No.	Description
31(0b)	FrameRemainingToggle. Loaded with FrameIntervalToggle when FrameRemaining is loaded.
30-14(0000h)	Reserved.
13-0(0000h)	FrameRemaining. When the Host Controller is in the USBOPERATIONAL state, this 14-bit field decrements each 12 MHz clock period. When the count reaches 0, (end of frame) the counter reloads with FrameInterval. In addition, the counter loads when the Host Controller transitions into USBOPERATIONAL.

Register Index : **3Fh-3Ch**
Register Name : **HcFmNumber**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
31-16(0000h)	Reserved.
15-0(0000h)	FrameNumber. This 16-bit incrementing counter field is incremented coincident with the loading of FrameRemaining. The count rolls over from 'FFFFh' to '0h.'

Register Index : **43h-40h**
Register Name : **HcPeriodicStart**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
31-14(0000h)	Reserved.
13-0(0000h)	PeriodicStart. This field contains a value used by the List Processor to determine where in a frame the Periodic List processing must begin.

Register Index : **47h-44h**
Register Name : **HcLSThreshold**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
31-12(00000h)	Reserved.
11-0(000h)	LSThreshold. This field contains a value used by the Frame Management block to determine whether or not a low speed transaction can be started in the current frame.

Register Index : **4Bh-48h**
Register Name : **HcRhDescriptorA**
Attribute : Read/Write
Default Value : 01000002h/01000003h
(This register is only reset by hardware reset. It is written during system initialization to configure the Root Hub. These bit should not be written during normal operation.)

Bit No.	Description
31-24(01h)	PowerOnToPowerGoodTime. This field value is represented as the number of 2 ms intervals, ensuring that the power switching is effective within 2 ms. Only bits [25:24] are implemented as R/W. The remaining bits are read only as '0'. It is not expected that these bits be written to anything other than 1h, but limited adjustment is provided. This field should be written to support system implementation. This field should always be written to a non-zero value.
23-13(000h)	Reserved.
12(0b)	NoOverCurrentProtection. Global over-current reporting implemented in M5237. This bit should be written to support the external system port over-current implementation. 0 = Over-current status is reported 1 = Over-current status is not reported
11(0b)	OverCurrentProtectionMode. Global over-current reporting implemented in M5237. This bit should be written 0 and is only valid when NoOverCurrentProtection is cleared. 0 = Global Over-Current 1 = Individual Over-Current
10(0b)	DeviceType. M5237 is not a compound device. This bit should be read/write 0.
9(0b)	NoPowerSwitching. Global power switching implemented in M5237. This bit should be written to support the external system port power switching implementation. 0 = Ports are power switched. 1 = Ports are always powered on.
8(0b)	PowerSwitchingModeThis bit is only valid when NoPowerSwitching is cleared. This bit should be written '0'. Because only global power switching mode is implemented in M5237. 0 = Global Switching 1 = Individual Switching
7-0(02h/03h)	NumberDownstreamPorts. This read-only bits indicates how many ports supported by M5237. If M5237 PCI configuration register Index 40h bit 26 = 1, then 03h will be reported (3rd USB port enable), else 02h will be reported.

Register Index : **4Fh-4Ch**
Register Name : **HcRhDescriptorB**
Attribute : Read/Write
Default Value : 00000000h
(This register is only reset by hardware reset. It is written during system initialization to configure the Root Hub. These bit should not be written during normal operation.)

Bit No.	Description
31-16(0000h)	PortPowerControlMask. Global-power switching. This field is only valid if NoPowerSwitching is cleared and PowerSwitchingMode is set (individual port switching). When set, the port only responds to individual port power switching commands (Set/ClearPortPower). When cleared, the port only responds to global power switching commands (Set/ClearGlobalPower). 0 = Port responds to global power switching commands 1 = Port responds to individual port power switching commands Port Bit relationship 0 : Reserved 1 : Port 1 2 : Port 2 ... 15 : Port 15 Unimplemented ports are reserved, read/write '0'.
15-0(0000h)	DeviceRemoveable. M5237's ports default to removable devices. 0 = Device removable 1 = Device not removable Port Bit relationship 0 : Reserved 1 : Port 1 2 : Port 2 ... 15 : Port 15 Unimplemented ports are reserved, read/write '0'.

Register Index : **53h-50h**
Register Name : **HcRhStatus**
Attribute : Read/Write
Default Value : 00000000h
(This register is reset by the USBRESET state.)

Bit No.	Description
31(0b)	(read) Not supported. Always read '0'. (write) ClearRemoteWakeupEnable Writing a '1' to this bit clears DeviceRemoteWakeupEnable. Writing a '0' has no effect.
30-18(0000h)	Reserved.
17(0b)	OverCurrentIndicatorChange. This bit is set when OverCurrentIndicator changes. Writing a '1' clears this bit. Writing a '0' has no effect.
16(0b)	(read) LocalPowerStatusChange Not supported. Always read '0'. (write) SetGlobalPower Writing a '1' issues a SetGlobalPower command to the ports. Writing a '0' has no effect.
15(0b)	(read) DeviceRemoteWakeupEnable This bit enables ports' ConnectStatusChange as a remote wakeup event. 0 = disable 1 = enable (write) SetRemoteWakeupEnable Writing a '1' sets DeviceRemoteWakeupEnable. Writing a '0' has no effect.
14-2(0000h)	Reserved.
1(0b)	OverCurrentIndicator. This bit reflects the state of the OVRCUR pin. This field is only valid if NoOverCurrentProtection and OverCurrentProtectionMode are cleared. 0 = No over-current condition 1 = Over-current condition
0(0b)	(read) LocalPowerStatus Not Supported. Always read '0'. (write) ClearGlobalPower Writing a '1' issues a ClearGlobalPower command to the ports. Writing a '0' has no effect.

Register Index : **5Fh-5Ch,5Bh-58h,57h-54h**
Register Name : **HcRhPortStatus[2:1]/[3:1]**
Attribute : Read/Write
Default Value : 00000000h
(This register is reset by the USBRESET state.)
(5Fh-5Ch only valid when M5237 PCI configuration register Index 40h bit 26 = 1)

Bit No.	Description
31-21(000h)	Reserved.
20(0b)	PortResetStatusChange. This bit indicates that the port reset signal has completed. 0 = Port reset is not complete. 1 = Port reset is complete.
19(0b)	PortOverCurrentIndicatorChange. This bit is set when OverCurrentIndicator changes. Writing a '1' clears this bit. Writing a '0' has no effect.
18(0b)	PortSuspendStatusChange This bit indicates the completion of the selective resume sequence for the port. 0 = Port is not resumed. 1 = Port resume is complete.
17(0b)	PortEnableStatusChange. This bit indicates that the port has been disabled due to a hardware event (cleared PortEnableStatus). 0 = Port has not been disabled. 1 = PortEnableStatus has been cleared.
16(0b)	ConnectStatusChange. This bit indicates a connect or disconnect event has been detected. Writing a '1' clears this bit. Writing a '0' has no effect. 0 = No connect/disconnect event. 1 = Hardware detection of connect/disconnect event. Note: If DeviceRemoveable is set, this bit resets to '1'.
15-10(00h)	Reserved.
9(0b)	(read) LowSpeedDeviceAttached. This bit defines the speed (and bud idle) of the attached device. It is only valid when CurrentConnectStatus is set. 0 = Full Speed device 1 = Low Speed device (write) ClearPortPower Writing a '1' clears PortPowerStatus. Writing a '0' has no effect
8(0b)	(read) PortPowerStatus. This bit reflects the power state of the port regardless of the power switching mode. 0 = Port power is off. 1 = Port power is on. Note: If NoPowerSwitching is set, this bit is always read as '1'. (write) SetPortPower Writing a '1' sets PortPowerStatus. Writing a '0' has no effect.
7-5(000b)	Reserved.
4(0b)	(read) PortResetStatus 0 = Port reset signal is not active. 1 = Port reset signal is active. (write) SetPortReset Writing a '1' sets PortResetStatus. Writing a '0' has no effect.
3(0b)	(read) PortOverCurrentIndicator M5237 supports global over-current reporting. This bit reflects the state of the OVRCUR pin dedicated to this port. This field is only valid if NoOverCurrentProtection is cleared and OverCurrentProtectionMode is set. 0 = No over-current condition 1 = Over-current condition (write) ClearPortSuspend Writing a '1' initiates the selective resume sequence for the port. Writing a '0' has no effect.

Bit No.	Description
2(0b)	(read) PortSuspendStatus 0 = Port is not suspended 1 = Port is selectively suspended (write) SetPortSuspend Writing a '1' sets PortSuspendStatus. Writing a '0' has no effect.
1(0b)	(read) PortEnableStatus 0 = Port disabled. 1 = Port enabled. (write) SetPortEnable Writing a '1' sets PortEnableStatus. Writing a '0' has no effect.
0(0b)	(read) CurrentConnectStatus 0 = No device connected. 1 = Device connected. NOTE: If DeviceRemoveable is set (not removable) this bit is always '1'. (write) ClearPortEnable Writing '1' a clears PortEnableStatus. Writing a '0' has no effect.

4.2.2.2 Legacy Support Interface Register

Register Index **103h-100h**
Register Name : **HceControl Register**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
31-9(000000h)	Reserved. Read as 0. I/O data that is written to ports 60h and 64h is captured in this register when emulation is enabled. This register may be read or written directly by accessing it with its memory address in the Host Controller's operational register space. When accessed directly with a memory cycle, reads and writes of this register have no side effects.
8(0b)	A20 State. This bit indicates current state of Gate A20 on keyboard controller. This bit is used to compare against value written to 60h when GateA20Sequence is active.
7(0b)	IRQ[12] Active. This bit indicates that a positive transition on IRQ[12] from keyboard controller has occurred. Software may write a 1 to this bit to clear it (set it to 0). Software write of a 0 to this bit has no effect.
6(0b)	IRQ[1] Active. Indicates that a positive transition on IRQ[1] from keyboard controller has occurred. Software may write a 1 to this bit to clear it (set it to 0). Software write of a 0 to this bit has no effect.
5(0b)	GateA20Sequence. Set by HC when data value of D1h is written to I/O port 64h. Cleared by HC when data value of FFh is written to I/O port 64h.
4(0b)	ExternalIRQEn. When set to 1, IRQ[1] and IRQ[12] from the keyboard controller will cause an emulation interrupt. The function controlled by this bit is independent of the setting of the EmulationEnable bit in this register.
3(0b)	IRQEn. When set, the Host Controller will generate IRQ[1] or IRQ[12] as long as the OutputFull bit in HceStatus is set to 1. If the AuxOutputFull bit of HceStatus is 0, then IRQ[1] is generated and if it is 1, then an IRQ[12] is generated.
2(0b)	CharacterPending. When set, an emulation interrupt will be generated when the OutputFull bit of the HceStatus register is set to 0.
1(0b)	EmulationInterrupt (Read) This bit is a static decode of the emulation interrupt condition.
0(0b)	EmulationEnable. When set to 1, the Host Controller will be enabled for legacy emulation. The Host Controller will decode accesses to I/O registers 60H and 64H and generate IRQ[1] and/or IRQ[12] when appropriate. Additionally, the host controller will generate an emulation interrupt at appropriate times to invoke the emulation software.

Register Index : **107h-104h**
Register Name : **HceInput Register**
Attribute : Read/Write
Default Value : 000000xxh

Bit No.	Description
31-8(000000h)	Reserved. Read as 0.
7-0(xxh)	InputData. This register holds data that is written to I/O ports 60h and 64h. The data placed in this register by the emulation software is returned when I/O port 60h is read and emulation is enabled. On a read of this location, the OutputFull bit in HceStatus is set to 0.

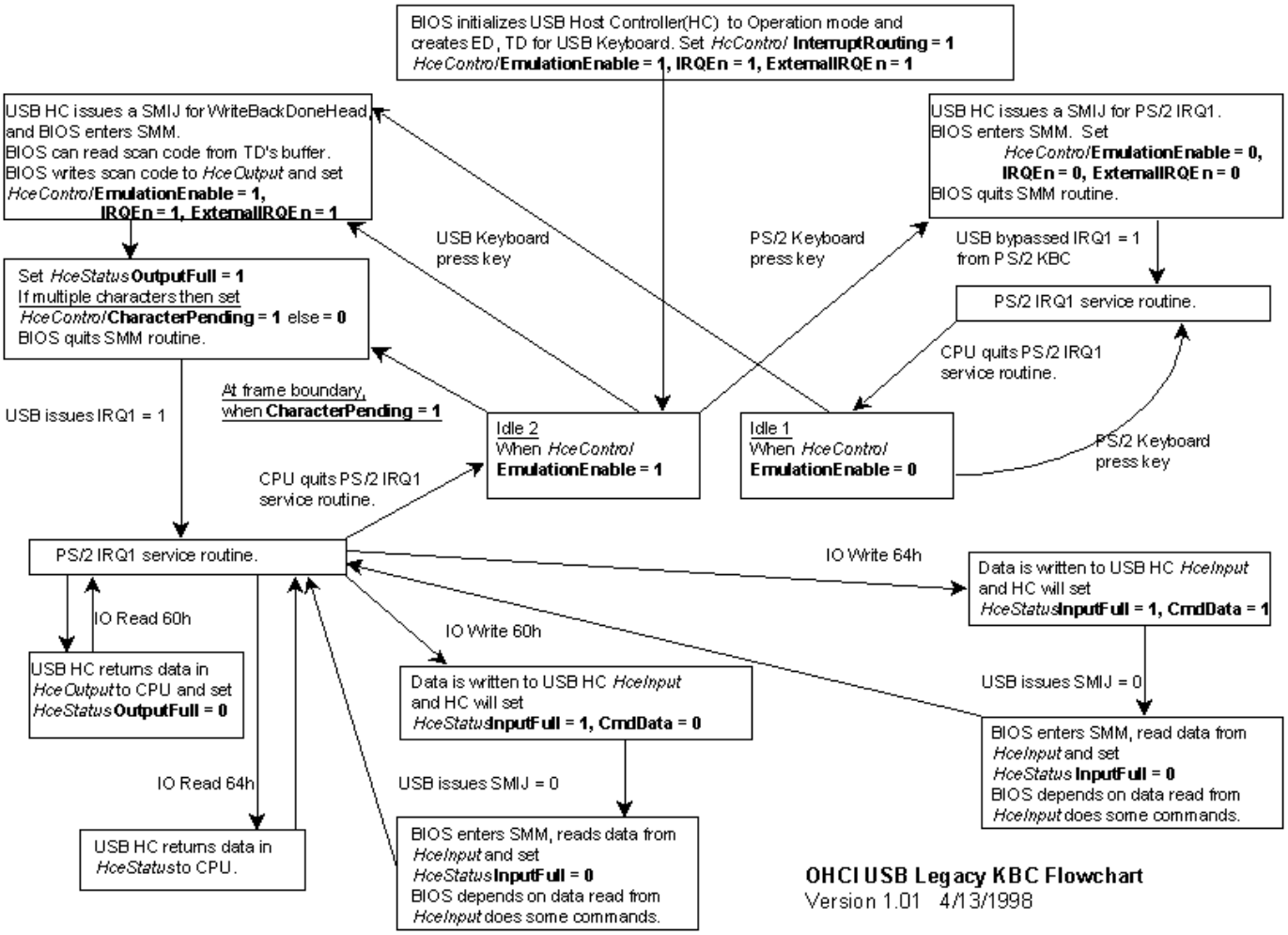
Register Index : **10Bh-108h**
Register Name : **HceOutput Register**
Attribute : Read/Write
Default Value : 000000xxh

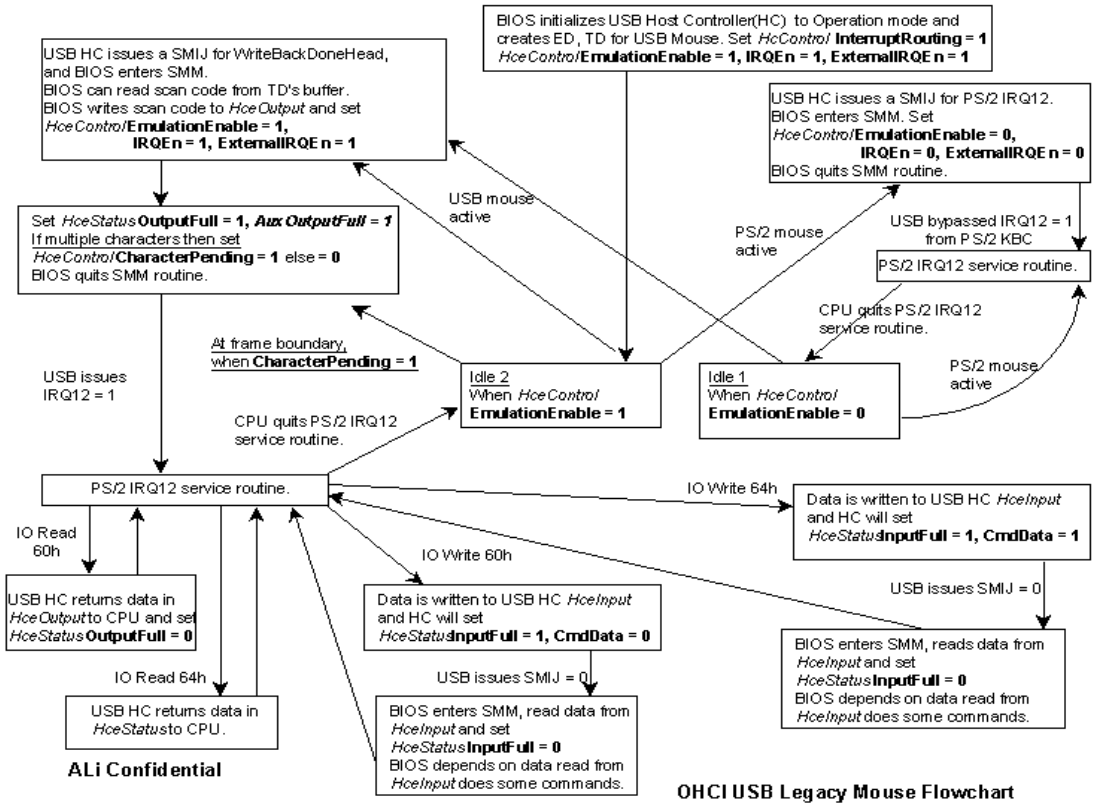
Bit No.	Description
31-8(000000h)	Reserved. Read as 0. The contents of the HceStatus Register is returned on an I/O Read of port 64h when emulation is enabled. Reads and writes of port 60h and writes to port 64h can cause changes in this register. Emulation software can directly access this register through its memory address in the Host Controller's operational register space. Access of this register through its memory address produces no side effects.
7-0(xxh)	OutputData. This register hosts data that is returned when an I/O read of port 60h is performed by application software.

Register Index : **10Fh-10Ch**
Register Name : **HceStatus Register**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
31-8(000000h)	Reserved. Read as 0.
7(0b)	Parity. Indicates parity error on keyboard/mouse data.
6(0b)	Timeout. This is used to indicate a time-out.
5(0b)	AuxOutputFull. IRQ[12] is asserted whenever this bit is set to 1 and OutputFull is set to 1 and the IRQEn bit is set.
4(0b)	Inhibit Switch. This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.
3(0b)	CmdData. The HC will set this bit to 0 on an I/O write to port 60h and on an I/O write to port 64h, the HC will set this bit to 1.
2(0b)	Flag. Nominally used as a system flag by software to indicate a warm or cold boot.
1(0b)	InputFull. Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
0(0b)	OutputFull. The HC will set this bit to 0 on a read of I/O port 60h. If IRQEn is set and AuxOutputFull is set to 0 then an IRQ[1] is generated as long as this bit is set to 1. If IRQEn is set and AuxOutputFull is set to 1 then an IRQ[12] will be generated as long as this bit is set to 1. While this bit is 0 and CharacterPending in HceControl is set to 1, an emulation interrupt condition exists.

4.2.2.3 Legacy Programming Diagram





OHCI USB Legacy Mouse Flowchart

4.2.3 Power Management I/O Space Registers

4.2.3.1 ACPI I/O Registers

The "Base" address is programmed in the 7101 PMU PCI DEVICE Configuration Space Index 13h-10h.

Byte Index	Mnemonic	Definition	Attribute (R/W)	Default Value
01h-00h	PM1_STS	Power Management 1 Status Register	R/W	0000h
03h-02h	PM1_EN	Power Management 1 Enable Register	R/W	0000h
05h-04h	PM1_CNTRL	Power Management 1 Control Register	R/W	1000h
07h-06h	Reserved	Reserved	R	0000h
0Bh-08h	PM1_TMR	Power Management 1 Timer Register	R	xxh
0Fh-0Ch	Reserved	Reserved	R	00h
13h-10h	P_CNTRL	Processor Control Register	R/W	00000000h
14h	LVL2	Processor Level 2 Register	R	00h
15h	LVL3	Processor Level 3 Register	R	00h
17h-16h	Reserved	Reserved	R	0000h
19h-18h	GPE0_STS	General Purpose Event0 Status Register	R/W	0000h
1Bh-1Ah	GPE0_EN	General Purpose Event0 Enable Register	R/W	0000h
1Dh-1Ch	GPE1_STS	General Purpose Event1 Status Register	R/W	0000h
1Fh-1Eh	GPE1_EN	General Purpose Event1 Enable Register	R/W	0000h
27h-20h	GPE1_CTL	General Purpose Event1 Control Register	R/W	00h
2Fh-28h	Reserved	Reserved	R	00h
30h	PM2_CNTRL	Power Management 2 Control Register	R/W	00h
3Fh-31h	Reserved	Reserved	R	00h

Register Index : **01h-00h**
Register Name : **PM1_STS - Power Management 1 Status Register**
Attribute : Read/Write
Default Value : 0000h

Bit No.	Description
15 (0b)	Wakeup Status (WAK_STS). 0 : Cleared by writing '1' to this position. 1 : An enabled resume event occurs when system is in the suspend state. The resume event is enabled by ACPI Register Index 1Bh-1Ah and Index 1Fh-1Eh. The respective status will be set in ACPI Register Index 19h-18h and Index 1Dh-1Ch.
14-11 (0h)	Reserved. Read as 0's.
10 (0b)	RTC Status (RTC_STS). 0 : Cleared by writing '1' to this position. 1 : RTC generates an alarm. (IRQ8J Assert) When IRQ8J is asserted, this bit will be set to 1.
9 (0b)	Reserved. Read as 0's.
8 (0b)	Power Button Status (PWRBTN_STS). 0 : Cleared by writing '1' to this position or by Power Button Override condition. 1 : PWRBTNJ is asserted LOW. When PWRBTNJ is asserted, this bit will be set to 1.
7-6 (0h)	Reserved. Read as 0's.
5 (0b)	Global Status (GBL_STS). 0 : Cleared by writing '1' to this position. 1 : The BIOS wanting the attention of the SCI handler (by writing a 1 to the BIOS_RLS bit).
4 (0b)	Bus Master Status (BM_STS). 0 : Cleared by writing '1' to this position. 1 : Anytime a system bus master requests the system bus. When a system bus master requests the system bus (it may come from PCI master, ISA master, DMA request, USB, and IDE master), this bit will be set to 1.
3-1 (0h)	Reserved. Read as 0's
0 (0b)	Power Management Timer Carry Status(PMTC_STS). 0 : Cleared by writing '1' to this position. 1 : The 22nd (30th) bit of the 24-bit (32-bit) PM timer goes high to low.

Register Index : **03h-02h**
Register Name : **PM1_EN - Power Management 1 Enable Register**
Attribute : Read/Write
Default Value : 0000h

Bit No.	Description
15-11 (0h)	Reserved. Read as 0's.
10 (0b)	RTC Enable (RTC_EN). 0 : No event is generated. 1 : An SCI, SMI or RSM event is generated anytime the RTC_STS bit is set.
9 (0b)	Reserved. Read as 0's.
8 (0b)	Power Button Enable (PWRBTN_EN). 0 : No event is generated. 1 : An SCI, SMI or RSM event is generated anytime the PWRBTN_STS bit is set.
7-6 (0h)	Reserved. Read as 0's.
5 (0b)	Global Enable (GBL_EN). 0 : No SCI event is generated. 1 : An SCI event is generated anytime the GBL_STS bit is set.
4-1 (0h)	Reserved. Read as 0's.
0 (0b)	Power Management Timer Carry Enable (PMTC_EN). 0 : No SCI event is generated. 1 : An SCI event is generated anytime the PMTC_STS bit is set.

Register Index : **05h-04h**
Register Name : **PM1_CNTRL - Power Management 1 Control Register**
Attribute : Read/Write
Default Value : 1000h

Bit No.	Description
15-14 (0h)	Reserved. Read as 0's.
13 (0b)	Suspend Enable(SLP_EN) -- Writable and Read as 0's. 0 : No suspend mode is entering. 1 : Causes the system to slip into the suspend mode defined by the SLP_TYP field.
12-10 (10b)	Suspend Type(SLP_TYP). This 3-bit field defines the type of hardware suspend mode. The system should enter the following mode when SLP_EN bit is set. 100 : Working. 011 : Sleeping. 010 : Suspend To DRAM. 001 : Suspend To DISK. 000 : Soft Off. other : Reserved. The SUS_TYP field is used by the BIOS and OS code to determine the suspend mode that system is resuming from. Before entering any low state(LVL2 or LVL3), this field should be programmed to the Working mode.
9-3 (00h)	Reserved. Read as 0's.
2 (0b)	Global Release(GBL_RLS). 0 : The resource ownership for ACPI software is not released. 1 : Set by ACPI software to raise SMI event to inform BIOS software, the resource ownership is released.
1 (0b)	Bus Master Break Event Enable (BM_RLD). 0 : Bus master request does not effect the processor state. 1 : Bus master request will change processor from clock control state(C3) to normal state(C0).
0 (0b)	SCI Enable (SCI_EN). 0 : These events will generate SMI interrupt. 1 : These events will generate SCI interrupt.

Register Index : **07h-06h**
Register Name : **Reserved Register**
Attribute : Read Only
Default Value 0000h

Register Index : **0Bh-08h**
Register Name : **PM1_TMR - Power Management 1 Timer Register**
Attribute : Read Only

Bit No.	Description
31-24	Extend Power Management Timer Value(E_PMT_VAL). Return the upper eight bits of a 32-bit power management timer.
23-0	Power Management Timer Value(PMT_VAL). Return the running count of the power management timer currently.

Register Index : **0Fh-0Ch**
Register Name : **Reserved Register**
Attribute : Read Only
Default Value 0000h

Register Index : **13h-10h**
Register Name : **P_CNTRL - Processor Control Register**
Attribute : Read/Write
Default Value : 0000h

Bit No.	Description
31-18 (0000h)	Reserved. Read as 0's.
17 (0b)	Throttle Status(THRO_STS) -- R0. 0 : The clock control state is exiting throttling mode. 1 : The clock control state is in the throttling mode.
16-14 (0h)	Reserved. Read as 0's.
13 (0b)	Clock Run Enable (CR_EN). 0 : Disable. 1 : Enable. When this bit is enabled, the M1543C becomes a PCI CLKRUN host controller. It will detect PCI IDLE CYCLE to stop PCI clock.
12-10 (0h)	Reserved. Read as 0's.
9 (0b)	Clock Control Enable(CLK_EN). 0 : Disable the clock control function. 1 : Enable the clock control function, read to the LVL2 and LVL3 register will cause the M1543C to enter the enabled clock control mode. This bit is the switch for the clock control of M1543C. All the clock controls (Throttle, Stop Grant, Stop clock, sleeping) only can be enabled by setting this bit to 1. Otherwise, it will not take effect.
8-5 (0h)	Reserved. Read as 0's.
4 (0b)	Throttle Enable(THRO_EN). 0 : Disable the CPU clock throttling function. 1 : Enable the CPU clock throttling function.
3-1 (0h)	Throttle Duty Setting Values (THRO_DTY). This 3-bit duty width field (Dutyset) determines the performance of the processor by the following equation. %Performance = Dutyset/ $2^{dutywidth}$ x 100 % Dutyset: %Performance 000 : Reserved. 001 : 0-12.5% (about 1/8 high and 7/8 low per throttle period). 010 : 12.5-25%(about 2/8 high and 6/8 low per throttle period). 011 : 25-37.5%(about 3/8 high and 5/8 low per throttle period). 100 : 37.5-50%(about 4/8 high and 4/8 low per throttle period). 101 : 50-62.5%(about 5/8 high and 3/8 low per throttle period). 110 : 62.5-75%(about 6/8 high and 2/8 low per throttle period). 111 : 75-87.5%(about 7/8 high and 1/8 low per throttle period).
0 (0b)	Reserved. Read as 0's.

Register Index : **14h**
Register Name : **LVL2 - Processor Level 2 Register**
Default Value : 00h
Attribute : Read Only

Bit No.	Description
7-0	Reads to this register will generate an enter to level 2 power state command to the clock control logic.

Register Index : **15h**
Register Name : **LVL3 - Processor Level 3 Register**
Default Value : 00h
Attribute : Read Only

Bit No.	Description
7-0	Reads to this register will generate an enter to level 3 power state command to the clock control logic.

Register Index : **17h-16h**
Register Name : **Reserved Register**
Attribute : Read Only
Default Value 0000h

Register Index : **19h-18h**
Register Name : **GPE0_STS - General Purpose Event0 Status Register**
Attribute : Read/Write
Default Value : 0000h

Bit No.	Description
15-12 (0h)	Reserved. Read as 0's.
11 (0b)	RI Status(RING_STS). 0 : Cleared by writing '1' to this position. 1 : Anytime the RIJ signal is asserted .
10 (0b)	ACPWR Status(ACPWR_STS). 0 : Cleared by writing '1' to this position. 1 : The ACPWR signal is asserted.
9 (0b)	Reserved. Read as 0's.
8 (0b)	DOCKJ Status(DOCK_STS). 0 : Cleared by writing '1' to this position. 1 : The DOCKJ signal is asserted .
7 (0b)	Extended GPI11 status (EGPI11_STS) 0 : Cleared by writing '1' to this position 1 : EGPI11 signal is toggled.
6 (0b)	Extended GPI10 status (EGPI10_STS) 0 : Cleared by writing '1' to this position 1 : EGPI10 signal is toggled.
5 (0b)	Extended GPI9 status (EGPI9_STS) 0 : Cleared by writing '1' to this position 1 : EGPI9 signal is toggled.
4 (0b)	Extended GPI8 status (EGPI8_STS) 0 : Cleared by writing '1' to this position 1 : EGPI8 signal is toggled.
3 (0b)	Reserved. Read as 0's.
2 (0b)	USB Event Status(USBE_STS). 0 : Cleared by writing '1' to this position. 1 : Anytime the USB Event is activated.
1 (0b)	Thermal Override Status(THEROR_STS). 0 : Cleared by writing '1' to this position. 1 : Anytime the THRMJ signal is driven active for more than 2 seconds,and starts throttling the CPU's clock at the THTL_DTY ratio (when Auto Thermal Throttle is enabled)
0 (0b)	Thermal Status(THER_STS). 0 : Cleared by writing '1' to this position. 1 : Anytime the THRMJ signal is driven active as defined by the THRM_POL bit.

Register Index : **1Bh-1Ah**
Register Name : **GPE0_EN - General Purpose Event0 Enable Register**
Attribute : Read/Write
Default Value : 0000h

Bit No.	Description
15-12 (0h)	Reserved. Read as 0's.
11 (0b)	RI Enable (RING_EN). 0 : No event is generated. 1 : An SCI,SMI or RSM event generated anytime the RING_STS bit is set.
10 (0b)	ACPWR Enable (ACPWR_EN). 0 : No event is generated. 1 : An SCI,SMI or RSM event is generated anytime the ACPWR_STS bit is set.
9 (0b)	Reserved. Read as 0's.
8 (0b)	DOCKJ Enable (DOCK_EN). 0 : No event is generated. 1 : An SCI, SMI or RSM event is generated anytime the DOCK_STS bit is set.
7 (0b)	Extended GPI11 enable (EGPI11_EN) 0 : No event is generated. 1 : An SCI, SMI event is generated anytime the EGPI11_STS bit is set.
6 (0b)	Extended GPI10 enable (EGPI10_EN) 0 : No event is generated. 1 : An SCI, SMI event is generated anytime the EGPI10_STS bit is set.
5 (0b)	Extended GPI9 enable (EGPI9_EN) 0 : No event is generated 1 : An SCI, SMI event is generated anytime the EGPI9_STS bit is set.
4 (0b)	Extended GPI8 enable (EGPI8_EN) 0 : No event is generated 1 : An SCI, SMI event is generated anytime the EGPI8_STS bit is set.
3 (0b)	Reserved. Read as 0's.
2 (0b)	USB Event Enable (USBE_EN). 0 : No event is generated. 1 : An SCI,SMI or RSM event is generated anytime the USBE_STS bit is set.
1 (0b)	Thermal Override Enable (THEROR_EN). 0 : No event is generated. 1 : An SCI or SMI event is generated anytime the THEROR_STS bit is set.
0 (0b)	Thermal Enable (THER_EN). 0 : No event is generated. 1 : An SCI or SMI event is generated anytime the THER_STS bit is set.

Register Index : **1Dh-1Ch**
Register Name : **GPE1_STS - General Purpose Event1 Status Register**
Attribute : Read/Write
Default Value : 0000h

Bit No.	Description
15(0b)	IRQ[14,15] Resume Status (IRQ1415_RSM_STS) 0 : Cleared by writing '1' to this position. 1 : IRQ[14] or IRQ[15] signal is asserted.
14(0b)	IRQ[13] Resume Status (IRQ13_RSM_STS) 0 : Cleared by writing '1' to this position. 1 : IRQ[13] signal is asserted.
13(0b)	IRQ[10,11] Resume Status (IRQ1011_RSM_STS) 0 : Cleared by writing '1' to this position. 1 : IRQ[10] or IRQ[11] signal is asserted.
12(0b)	IRQ[7,9] Resume Status (IRQ79_RSM_STS) 0 : Cleared by writing '1' to this position. 1 : IRQ[7] or IRQ[9] signal is asserted.
11(0b)	IRQ[5,6] Resume Status (IRQ56_RSM_STS) 0 : Cleared by writing '1' to this position. 1 : IRQ[5] or IRQ[6] signal is asserted.
10(0b)	IRQ[3,4] Resume Status (IRQ34_RSM_STS) 0 : Cleared by writing '1' to this position. 1 : IRQ[3] or IRQ[4] signal is asserted.
9(0b)	IRQ[1,12] Resume Status (IRQ112_RSM_STS) 0 : Cleared by writing '1' to this position. 1 : IRQ[1] or IRQ[12] signal is asserted.
8(0b)	IRQ[0] Resume Status (IRQ0_RSM_STS) 0 : Cleared by writing '1' to this position. 1 : IRQ[0] signal is asserted.
7(0b)	Extended GPI 7 status (EGPI7_STS) 0 : Cleared by writing '1' to this position. 1 : EGPI7 signal is toggled.
6(0b)	Extended GPI 6 status (EGPI6_STS) 0 : Cleared by writing '1' to this position. 1 : EGPI6 signal is toggled.
5(0b)	Extended GPI 5 status (EGPI5_STS) 0 : Cleared by writing '1' to this position. 1 : EGPI5 signal is toggled.
4(0b)	Extended GPI 4 status (EGPI4_STS) 0 : Cleared by writing '1' to this position. 1 : EGPI4 signal is toggled.
3(0b)	Extended GPI 3 status (EGPI3_STS) 0 : Cleared by writing '1' to this position. 1 : EGPI3 signal is toggled.
2(0b)	Extended GPI 2 status (EGPI2_STS) 0 : Cleared by writing '1' to this position. 1 : EGPI2 signal is toggled.
1(0b)	Extended GPI 1 status (EGPI1_STS) 0 : Cleared by writing '1' to this position. 1 : EGPI1 signal is toggled.
0 (0b)	BIOS Status(BIOS_STS). 0 : Cleared by writing '1' to this position. 1 : ACPI software requesting attention (by writing a '1' to the GBL_RLS bit).

Register Index : **1Fh-1Eh**
Register Name : **General Purpose Event1 Enable Register (GPE1_EN)**
Attribute : Read/Write
Default Value : 0000h

Bit No.	Description
15 (0b)	IRQ[14,15] Resume Enable (IRQ1415_RSM_EN) 0 : No event is generated. 1 : An RSM event is generated anytime the IRQ1415_RSM_STS is set (only in the sleeping state)
14(0b)	IRQ[13] Resume Enable (IRQ13_RSM_EN) 0 : No event is generated. 1 : An RSM event is generated anytime the IRQ13_RSM_STS is set (only in the sleeping state)
13(0b)	IRQ[10,11] Resume Enable (IRQ1011_RSM_EN) 0 : No event is generated. 1 : An RSM event is generated anytime the IRQ1011_RSM_STS is set (only in the sleeping state)
12(0b)	IRQ[7,9] Resume Enable (IRQ79_RSM_EN) 0 : No event is generated. 1 : An RSM event is generated anytime the IRQ79_RSM_STS is set (only in the sleeping state)
11(0b)	IRQ[5,6] Resume Enable (IRQ56_RSM_EN) 0 : No event is generated. 1 : An RSM event is generated anytime the IRQ56_RSM_STS is set (only in the sleeping state)
10(0b)	IRQ[3,4] Resume Enable (IRQ34_RSM_EN) 0 : No event is generated. 1 : An RSM event is generated anytime the IRQ34_RSM_STS is set (only in the sleeping state)
9(0b)	IRQ[1,12] Resume Enable (IRQ112_RSM_EN) 0 : No event is generated. 1 : An RSM event is generated anytime the IRQ112_RSM_STS is set (only in the sleeping state)
8(0b)	IRQ[0] Resume Enable (IRQ0_RSM_EN) 0 : No event is generated. 1 : An RSM event is generated anytime the IRQ0_RSM_STS is set (only in the sleeping state)
7(0b)	Extended GPI7 enable (EGPI7_EN) 0 : No event is generated 1 : An SCI, SMI event is generated anytime the EGPI7_STS bit is set.
6(0b)	Extended GPI6 enable (EGPI6_EN) 0 : No event is generated 1 : An SCI, SMI event is generated anytime the EGPI6_STS bit is set.
5(0b)	Extended GPI5 enable (EGPI5_EN) 0 : No event is generated 1 : An SCI, SMI event is generated anytime the EGPI5_STS bit is set.
4(0b)	Extended GPI4 enable (EGPI4_EN) 0 : No event is generated 1 : An SCI, SMI event is generated anytime the EGPI4_STS bit is set.
3(0b)	Extended GPI3 enable (EGPI3_EN) 0 : No event is generated 1 : An SCI, SMI event is generated anytime the EGPI3_STS bit is set.
2(0b)	Extended GPI2 enable (EGPI2_EN) 0 : No event is generated 1 : An SCI, SMI event is generated anytime the EGPI2_STS bit is set.
1(0b)	Extended GPI1 enable (EGPI1_EN) 0 : No event is generated 1 : An SCI, SMI event is generated anytime the EGPI1_STS bit is set.
0 (0b)	BIOS Enable(BIOS_EN). 0 : When reset, then no SMI is generated. 1 : When set, the SMI is generated anytime the BIOS_STS is set.

Register Index : **20h**
Register Name : **BIOS Release Control Register**
Attribute : Read/Write
Default Value : 00000000h

Bit No.	Description
7-2 (00h)	Reserved. Read as 0's.
1 (0b)	BIOS Release(BIOS_RLS) – Always read as 0. Write results in following : 0 : The resource ownership for BIOS software is not released. 1 : Set by BIOS software to raise SCI event to inform ACPI software, the resource ownership is released.
0 (0b)	Reserved. Read as 0's.

Register Index : **2Fh-21h**
Register Name : **Reserved Register**
Attribute : Read Only
Default Value 0000h

Register Index : **30h**
Register Name : **PM2_CNTRL - Power Management 2 Control Register**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-1 (00h)	Reserved. Read as 0's.
0 (0b)	Arbiter Disable(ARB_DIS). 0 : The arbiter is enabled. 1 : The arbiter is disabled and default CPU has ownership of the system.

Register Index : **3Fh-31h**
Register Name : **Reserved Register**
Attribute : Read Only
Default Value 0000h

4.2.3.2 Advanced Power Management Registers

Register Index : **B1h**
Register Name : **Advances Power Management Access Port (I/O)**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-0	Write to this port will generate an SMI.

Register Index : **B2h**
Register Name : **Advances Power Management Access Port (I/O)**
Attribute : Read Only
Default Value : 00h

Bit No.	Description
7-0	Reading this port will cause the STPCLKJ signal to be asserted.

Register Index : **B3h**
Register Name : **Advances Power Management Status Port (I/O)**
Attribute : Read/Write
Default Value : 00h

Bit No.	Description
7-0	Pass status information between the OS and SMI handler.

4.2.3.3 SMB I/O Space Registers

The "Base" address is programmed in the PMU PCI DEVICE Configuration Space Offset 14-17h

Register Index : **00h**
Register Name : **SMBSTS : SMBus Host/Slave Status Register**
Attribute : (Read/Write, & write '1' clear)
Default Value : 00h

Bit	Description
7 (0b)	TERMINATE, '1' means the interrupt (or SMI) was caused by a terminated bus transaction in response to "ABORT".
6 (0b)	BUS_COLLI, Bus Collision, '1' means the interrupt (or SMI) was caused by the collision of bus transaction or no acknowledge.
5 (0b)	DEVICE_ERR, Device Error, '1' means the interrupt (or SMI) was caused by the SMB controller or device due to the generation of an error.
4 (0b)	SMI_I_STS, '1' means that the Interrupt (or SMI) was caused by the SMB controller after completing a command. (RO)
3 (0b)	HST_BSY, Host Controller Busy, '1' means that the SMB host controller is going to complete a command.(RO)
2 (0b)	IDL_STS, '1' means SMBus at Idle Status. (RO)
1 (0b)	HSTSLV_STS, Host Slave Status, '1' means the interrupt (or SMI) was caused by the host SMB slave interface.
0 (0b)	HSTSLV_BSY, Host Slave Busy, '1' means that SMB slave interface is going to receive a command. (RO)

Register Index : **01h**
Register Name : **SMBCMD : SMBus Host/Slave Command**
Attribute : Write Only
Default Value : 00h

Bit	Description
7 (0b)	SMB_BLK_CLR, SMB Block Register Pointer Reset, to reset block register's pointer.(WO)
6-4 (000b)	SMB_COMMAND, SMB Command, indicates which kind of command is asked to perform. (R/W) [6:4] : Command 000 : Quick command 001 : Send/Receive Byte 010 : Write/Read Byte 011 : Write/Read Word 100 : Write/Read Block Others : Reserved
3 (0b)	T_OUT_CMD, like "Abort" command, it (WO) performs the Time Out condition on the SMBus to reset not only Host controller but also other devices on the SMBus. -->DEVICE_ERR
2 (0b)	Abort, reset Host controller. --> TERMINATE (WO)
1-0 (0h)	Reserved.

Register Index : **02h**
Register Name : **I/O Port to Start to Generate the Programmed Cycle on the SMBus (STRT_PRT)**
Attribute : Write
Default Value : 00h

Register Index : **03h**
Register Name : **SMBus Address Register for Host Controller**
Default Value : 00h
Attribute : Read/Write

Register Index : **04h**
Register Name : **SMBus DataA Register for Host Controller**
Attribute : Read/Write
Default Value : 00h
This register should be programmed with the value that will be transmitted in DataA field of the SMBus host interface transaction protocol. It means the count of block registers for a block write and read command.

Register Index : **05h**
Register Name : **SMBus DataB Register for Host Controller**
Attribute : Read/Write
Default Value : 00h
This register should be programmed with the value that will be transmitted in DataB field of the SMBus host interface transaction protocol. In byte transaction, only DataA is used. In write/read word transaction, both DataA and DataB are used. However, which byte is the high byte depends on the device.

Register Index : **06h**
Register Name : **SMBus Block Register for Host Controller**
Attribute : Read/Write
Default Value : 00h
This register is used to access 32-byte block data for block write and read SMBus protocol. Before reading or writing to this register, to set the block register index to 0 is needed. It is done by writing '1' to SMB_BLK_CLR in SMB I/O Space Register index 01h.

Register Index : **07h**
Register Name : **SMBus Command Register for Host Controller**
Default Value : 00h
Attribute : Read/Write
This register should be programmed with the value that will be transmitted in the command field of the SMBus host interface transaction protocol. For some device, this register acts as an index register to select the desired function, please refer to example 1.

Register Index : **1Eh-08h**
Register Name : **Reserved Register**
Attribute : Read Only
Default Value 0000h

Example1:
LM75 Read/Write Word

```
;; get SMB I/O based address from index 14h-17h of PMU device (M7101)
mov     dx,SMB_base_addr+0
mov     al,0ffh                         ; cls status
out     dx,al
```

```
@@:
mov     dx,SMB_base_addr+0
in      al,dx
jcxz    short $+2                       ; delay
jcxz    short $+2
jcxz    short $+2
test    al,4h
jz      short @B                        ; nz ,SMBus is at idle status

mov     dx,SMB_base_addr+3
mov     al,091h                         ; set lm75 Address and Read it
out     dx,al

mov     dx,SMB_base_addr+1
;;  mov al,020h                         ; set Read/Write Byte command
mov     al,030h                         ; set Read/Write Word command
out     dx,al

;; AL = 00h --> temperature register of LM75 ,read only
;;      01h --> configuration register of LM75
;;      10h -->       T (HYST) register of LM75
;;      11h -->       T (OS) register of LM75

mov     dx,SMB_base_addr+7
mov     al,00h                          ; read temperature register
out     dx,al

mov     dx,SMB_base_addr+2
mov     al,0ffh                         ; set Start command
out     dx,al

@@:
mov     dx,SMBUS_BASE_ADDRESS+0
in      al,dx
jcxz    short $+2
jcxz    short $+2
test    al,60h
jnz     short @F                        ; nz ,have error
test    al,10h
jz      short @B                        ; nz ,is successful

mov     dx,SMB_base_addr+4
in      al,dx                           ; read high byte data
jcxz    short $+2

xchg    ah,al

mov     dx,SMB_base_addr+5
in      al,dx                           ; read low byte data
jcxz    short $+2
@@:
END
```

Example2 :
ICS9148-36, Write Block

```
        mov     dx,SMBUS_BASE_ADDRESS+0
        mov     al,0ffh                         ; cls status
        out     dx,al
        @@:
        mov     dx,SMBUS_BASE_ADDRESS+0
        in      al,dx
        jcxz    short $+2
        jcxz    short $+2
        jcxz    short $+2
        test    al,4h
        jz      short @B                        ; nz ,SMBus is at idle status

        mov     dx,SMBUS_BASE_ADDRESS+3
        mov     al,0d2h                         ; set device address
        out     dx,al

        mov     dx,SMBUS_BASE_ADDRESS+1
        mov     al,0C0h                         ; Block Read/Write command
        out     dx,al

        ;; the command is depend on device
        ;   mov  dx,SMBUS_BASE_ADDRESS+7
        ;   mov  al,00h
        ;   out  dx,al

        mov     dx,SMBUS_BASE_ADDRESS+4
        mov     al,07h                          ; total 7 bytes
        out     dx,al

        ;;;AL data by H/W circuit design
        mov     dx,SMBUS_BASE_ADDRESS+6         ; Byte 0
        out     dx,al                   ;

        ;;;AL data by H/W circuit design
        ;  mov  al,0ffh                         ; CPUCLK
        mov     dx,SMBUS_BASE_ADDRESS+6         ; Byte 1
        out     dx,al

        ;;;AL data by H/W circuit design
        ; mov   al,0ffh                         ; PCICLK
        mov     dx,SMBUS_BASE_ADDRESS+6         ; Byte 2
        out     dx,al

        ;;;AL data by H/W circuit design
        ; mov   al,0ffh
        mov     dx,SMBUS_BASE_ADDRESS+6         ; Byte 3
        out     dx,al

        ;;;AL data by H/W circuit design
        ; mov   al,0ffh
        mov     dx,SMBUS_BASE_ADDRESS+6         ; Byte 4
        out     dx,al
```

```
;;;AL data by H/W circuit design
;  mov   al,0ffh                          ; AGP
mov     dx,SMBUS_BASE_ADDRESS+6    ; Byte 5
out     dx,al

;;;AL data by H/W circuit design
;  mov   al,0ffh                          ; power-up default
mov     dx,SMBUS_BASE_ADDRESS+6    ; Byte 6
out     dx,al

mov     dx,SMBUS_BASE_ADDRESS+2
mov     al,0ffh                        ; set Start command
out     dx,al
jcxz    short $+2
@@:
mov     dx,SMBUS_BASE_ADDRESS+0
in      al,dx
jcxz    short $+2
jcxz    short $+2
test    al,60h
jnz     short @F                       ; nz ,have error
test    al,10h
jz      short @B                       ; nz ,is successful

@@:

END
```

4.2.3.4 PCI IDE Controller I/O Space Registers Definition

This section contains more information regarding the IDE Master controller 5229 inside the M1543C.

1. The Primary and Secondary Channel can be disabled by setting built in 5229 Register Index 09h. The following shows the detailed definition of each bit.

Index 09h - bit7 - bus master IDE
0 : No, it is not a bus master IDE.
1 : Yes, it is a bus master IDE.

Index 09h - bit6 - Report IDE channel status
0 : No, this is the default zero value of PCI 2.1 specification.
1 : Yes, bits[5:4] can be queried to determine status of the IDE controller.

Index 09h - bit5 - Primary Channel
0 : No, the Primary channel is disabled.
1 : Yes, the Primary channel is enabled.

Index 09h - bit4 - Secondary Channel
0 : No, the Secondary channel is disabled.
1 : Yes, the Secondary channel is enabled.

Index 09h - bit3 - Secondary Channel Support
0 : Compatibility only.
1 : Both compatibility and native mode.

Index 09h - bit2 - Operation of Secondary channel
0 : Compatibility mode.
1 : Native mode.

Index 09h - bit1 - Primary Channel Support
0 : Compatibility mode only.
1 : Both compatibility and native mode.

Index 09h - bit0 - Operation of Primary Channel
0 : Compatibility mode.
1 : Native mode.

2. The PIO Mode IDE I/O Space Definition.

a. Compatibility Mode.
Primary channel I/O space is from 1F0H to 1F7H and 3F6H. Secondary channel I/O space is from 170H to 177H and 376H.
b. Native Mode.
Primary Channel I/O space can be programmed at Index 10h-14h. The I/O range is 8bytes that is described at Index 10h and1 byte is described at Index 14h. Secondary Channel I/O space can be programmed at Index 18h-1Ch. The I/O range is 8 bytes that is described at Index 18h and 1 byte is described at Index 1Ch.

3. Bus Master IDE Register Description.

Bus Master IDE function uses 16 bytes of I/O space. All bus master IDE I/O space can be accessed as byte, word, or Dword quantities. The description of the 16 bytes of I/O registers are as follows :

Offset from Base Address	Register	Register Access
00h	Bus Master IDE Command Register Primary	R/W
01h	Device Specific	
02h	Bus Master IDE Status Register Primary	RWC
03h	Device Specific	
04h-07h	Bus Master IDE PRD Table Address Primary	R/W
08h	Bus Master IDE Command Register Secondary	R/W
09h	Device Specific	
0Ah	Bus Master IDE Status Register Secondary	RWC
0Bh	Device Specific	
0Ch-0Fh	Bus Master IDE PRD Table Address Secondary	R/W

a. Register Name : Bus Master IDE Command register
Address Offset:
Primary Channel - Base address defined in Index 20h + 00h
Secondary Channel - Base address defined in Index 20h + 08h
Base address : F001h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit	Description
7-4 (0h)	Reserved. Must be 0.
3 (0b)	Read or Write Control. This bit sets the direction of the bus master transfer. 0 : PCI bus master read. 1 : PCI bus master write. This bit must not be changed when the bus master function is active.
2-1 (0h)	Reserved. Must be 0.
0 (0b)	Start/Stop Bus Master. Writing a '1' to this bit enables bus master operation of the controller. Bus Master operation begins when this bit has detected a change from zero to one. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a '0' to this bit. All state information is lost when a '0' is written; Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active and the drive has not yet finished its data transfer, the bus master command is said to be aborted and data transfered from the drive maybe discarded before being written to system memory. This bit is intended to be reset after the data transfer is completed, as indicated by either the Bus Master IDE active bit or the interrupt bit of the Bus master IDE status register for that IDE channel being set, or both.

b. Register Name: Bus Master IDE Status Register Address Offset :
Primary Channel - Base address defined in Index 20h + 02h
Secondary Channel - Base address defined in Index 20h + 0Ah
Base Address : F001h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

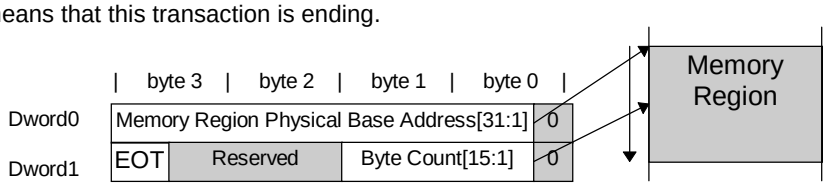
Bit	Description
7 (0b)	**Simplex Only**. (RO) This bit indicates whether or not both bus master channels (primary and secondary) can be operated at the same time. 0 : Channels operate independently and can be used at a time. 1 : Only one channel can be used at a time.
6 (0b)	**Drive 1 DMA capable**. (R/W) This bit is set by device dependent codes (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.
5 (0b)	**Drive 0 DMA capable**. (R/W) This bit is set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.
4-3 (0h)	Reserved. Must be 0.
2 (0b)	**Interrupt**. This bit is set by the rising edge of the IDE interrupt line. This bit is cleared when a '1' is written to it by software. Software can use this bit to determine if an IDE device has asserted its interrupt line. When this bit is one, all data transferred from the drive is visible in system memory.
1 (0b)	**Error**. This bit is set when the controller encounters an error in transferring data to/from memory. The exact error condition is bus specific and can be determined in a bus specific manner. This bit is cleared when a '1' is written to it by software.
0 (0b)	**Bus Master IDE active**. This bit is set when the Start bit is written to the Command Register. This bit is cleared when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared when the Start bit is cleared in the Command register. When this bit is read as a zero, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted.

c. Register Name : Descriptor Table Pointer Register
Primary Channel - Base address defined in Index 20h + 04h
Secondary Channel - Base address defined in Index 20h + 0Ch
Base address : F001h
Default Value : 00000000h
Attribute : Read/Write
Size : 32 bits

Bit	Description
31-2 (00000000h)	Base address of Descriptor table. Corresponds to A[31:2]
1-0 (0h)	Reserved.

4. Physical Region Descriptor Table

Before the controller starts a master transfer it is given a pointer to a Physical Region Descriptor Table. This table contains some number of Physical Region Descriptor (PRD) which describes the areas of memory that are involved in the data transfer. The PRD table must be aligned on a 4-byte boundary and the table cannot cross a 64K boundary in memory. The EOT is "END of TABLE". It means that this transaction is ending.



4.3 ISA Compatible Registers Summary :

The ISA compatible registers of the M1543C are summarized as below :

I/O Address	Attribute	Register Name
0000h	Read/Write	DMA1 (slave) CH0 Base and Current Address
0001h	Read/Write	DMA1 (slave) CH0 Base and Current Count
0002h	Read/Write	DMA1 (slave) CH1 Base and Current Address
0003h	Read/Write	DMA1 (slave) CH1 Base and Current Count
0004h	Read/Write	DMA1 (slave) CH2 Base and Current Address
0005h	Read/Write	DMA1 (slave) CH2 Base and Current Count
0006h	Read/Write	DMA1 (slave) CH3 Base and Current Address
0007h	Read/Write	DMA1 (slave) CH3 Base and Current Count
0008h	Read/Write	DMA1 (slave) Status(R)/Command(W)
0009h	Write-only	DMA1 (slave) Write Request
000Ah	Write-only	DMA1 (slave) Write Single Mask Bit
000Bh	Write-only	DMA1 (slave) Write Mode
000Ch	Write-only	DMA1 (slave) Clear Byte Pointer
000Dh	Write-only	DMA1 (slave) Master Clear
000Eh	Write-only	DMA1 (slave) Clear Mask
000Fh	Read/Write	DMA1 (slave) Read/Write All Mask Register Bits
0020h	Read/Write	INT_1 (master) Control Register
0021h	Read/Write	INT_1 (master) Mask Register
0040h	Read/Write	Timer Counter - Channel 0 Count
0041h	Read/Write	Timer Counter - Channel 1 Count
0042h	Read/Write	Timer Counter - Channel 2 Count
0043h	Read/Write	Timer Counter Command Mode Register
0060h	Read_access	Clear IRQ[12] (for PS2), IRQ[1] Latched Status
0060h	Read/Write	Keyboard Data Buffer
0061h	Read/Write	NMI and Speaker Status and Control
0064h	Read/Write	Keyboard Status(R)/Command(W)
0070h	Write-only	CMOS RAM Address Port and NMI Mask Register
0071h	Read/Write	CMOS Data Register Port
0081h	Read/Write	DMA Channel 2 Page Register
0082h	Read/Write	DMA Channel 3 Page Register
0083h	Read/Write	DMA Channel 1 Page Register
0087h	Read/Write	DMA Channel 0 Page Register
0089h	Read/Write	DMA Channel 6 Page Register
008Ah	Read/Write	DMA Channel 7 Page Register
008Bh	Read/Write	DMA Channel 5 Page Register
008Fh	Read/Write	Refresh Address Register for Address 23 to 17

The ISA compatible registers of the M1543C (continued)

I/O Address	Attribute	Register Name
00A0h	Read/Write	INT_2 (slave) Control Register
00A1h	Read/Write	INT_2 (slave) Mask Register
00C0h	Read/Write	DMA2 (master) CH0 Base and Current Address
00C2h	Read/Write	DMA2 (master) CH0 Base and Current Count
00C4h	Read/Write	DMA2 (master) CH1 Base and Current Address
00C6h	Read/Write	DMA2 (master) CH1 Base and Current Count
00C8h	Read/Write	DMA2 (master) CH2 Base and Current Address
00CAh	Read/Write	DMA2 (master) CH2 Base and Current Count
00CCh	Read/Write	DMA2 (master) CH3 Base and Current Address
00CEh	Read/Write	DMA2 (master) CH3 Base and Current Count
00D0h	Read/Write	DMA2 (master) Status(R)/Command(W)
00D2h	Write-only	DMA2 (master) Write Request
00D4h	Write-only	DMA2 (master) Write Single Mask Bit
00D6h	Write-only	DMA2 (master) Write Mode
00D8h	Write-only	DMA2 (master) Clear Byte Pointer
00DAh	Write-only	DMA2 (master) Master Clear
00DCh	Write-only	DMA2 (master) Clear Mask
00DEh	Read/Write	DMA2 (master) Read/Write All Mask Register Bits
00F0h	Write-only	Coprocessor Error Ignored Register
040Bh	Write only	DMA1 Extended Mode Register
0481h	Read/Write	DMA CH2 High Page Register
0482h	Read/Write	DMA CH3 High Page Register
0483h	Read/Write	DMA CH1 High Page Register
0487h	Read/Write	DMA CH0 High Page Register
0489h	Read/Write	DMA CH6 High Page Register
048Ah	Read/Write	DMA CH7 High Page Register
048Bh	Read/Write	DMA CH5 High Page Register
04D0h	Read/Write	INT_1 (master) Edge/Level Control
04D1h	Read/Write	INT_2 (slave) Edge/Level Control
04D6h	Write only	DMA2 Extended Mode Register

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4.4 Super I/O with FIR
4.4.1 Configuration Port

This configuration is based on the typical Plug-and-Play architecture and allows the BIOS to assign resources at POST.
To assign the M1543C a configuration key, <0x51, 0x23>, must be written to CONFIG PORT to enter the CONFIGURE mode. Then follow the Plug-and-Play procedure to configure each device.
A configuration key = < 0xBB > must be written to CONFIG PORT to exit the CONFIGURE mode and enter the NORMAL mode.
After a hard reset or Power on reset, the M1543C is in the NORMAL mode with all logical devices disable except KBC. The hardware setting pins control the KBC after the hard reset. The hardware settings are listed on table below.
All logical devices may be configured through 2 standard Configuration I/O Ports (INDEX and DATA) by placing the M1543C into Configuration Mode. The BIOS uses these configuration ports to initialize the logical devices during POST. The INDEX and DATA ports are only valid when the M1543C is in Configuration Mode.

A hardware setting pin CFG_PORT is latched to select the CFG_PORT as 3F0h or 370h.

Port Name	CFG_PORT=1	CFG_PORT=0	Type
CONFIG PORT	0x3F0h	0x370h	W
INDEX PORT	0x3F0h	0x370h	W
DATA PORT	0x3F1h	0x371h	R/W

Programming Example

```
;---------------------------------------
; Enter Configuration mode,
;---------------------------------------
MOV     DX,3F0H
MOV     AX,051H
CLI
OUT     DX,AL
MOV     AX,023H
OUT     DX,AL

;-------------------------------------------------------
; Program register 0x60 of Logic Device 4
;-------------------------------------------------------
MOV     DX,3F0H
MOV     AL,07H
OUT     DX,AL    ; Point to Device Select Register
MOV     DX,3F1H
MOV     AL,04H
OUT     DX,AL    ; Point to Device 4
MOV     DX,3F0H
MOV     AL,060H
OUT     DX,AL    ; Point to Register 60H
MOV     DX,3F1H
MOV     AL,02H
OUT     DX,AL    ; Update content of register 60H
(repeat for other devices)
;---------------------------------
;Exit Configuration Mode
;---------------------------------
MOV     DX,3F0H
MOV     AL,0BBH
OUT     DX,AL
```

Note : The selected logic device number will keep its old value until the next new one is written.

CHIP LEVEL REGISTERS

Index name **Hard reset, Soft reset default values**

Index 0x02h 0x00, 0x00

Bit	Description
7-1	Reserved
0	1 : Soft reset the configuration registers. This bit is automatically cleared after write. This register is write only.

Index 0x07h 0x00, 0x00

Bit	Description
7-0	Select the current logic device. This allows the access to each logical device's registers.

Index 0x1Fh ALi defined device version.

Index 0x20h 0x43, 0x43
ALi defined device identification. (read only)

Index 0x21h 0x15, 0x15
ALi defined device identification. (read only)

Index 0x22h 0x00, 0x00

Bit	Description
7	Read as 0.
6	Direct powerdown UART3 *0 0 : disable 1 : enable
5	Direct powerdown UART2 *0 0 : disable 1 : enable
4	Direct powerdown UART1 *0 0 : disable 1 : enable
3	Direct powerdown Parallel Port *0 0 : disable 1 : enable
2-1	Read as 0.
0	Direct powerdown FDC *0 0 : disable 1 : enable

*0 - During direct powerdown, access to I/O ports are denied. To wake up the device, a write of '0' to corresponding bit is required.

Index 0x23h 0x00, 0x00

Bit	Description
7	Read as 0
6	Auto powerdown UART3. 0 : disable 1 : enable
5	Auto powerdown UART2. 0 : disable 1 : enable
4	Auto powerdown UART1. 0 : disable 1 : enable
3	Auto powerdown Parallel Port. 0 : disable 1 : enable
2-0	Read as 0.

Index 0x2Ch Reserved for test

Index 0x2Dh 0x20, 0x20

Bit	Description
7-6,4-0	Reserved
5	0 : UART2 device number = 5 UART3 device number = B 1 : UART2 device number = B UART3 device number = 5

Index 0x2Eh Reserved

LOGICAL DEVICE 0 REGISTERS (FDC)

Index 0x30h 0x00, 0x00

Bit	Description
7-1	Read as 0.
0	FDC *1 0 : disable 1 : enable

*1 - The disable function of the device has the same behavior as direct powerdown function except the device remains at reset state.

Index 0x60h 0x03, 0x03

Bit	Description
7-0	The higher address of the FDC's I/O base address.

Index 0x61h 0xF0, 0xF0

Bit	Description
7-3	The lower address of the FDC's I/O base address.
2-0	Set to 0.

Index 0x70h 0x06, 0x06

Bit	Description
7-4	Read as 0.
3-0	Select IRQ channel used by FDC. 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

Index 0x74h 0x02, 0x02

Bit	Description
7-3	Read as 0.
2-0	Select DMA channel used by FDC 000 : DMA0 001 : DMA1 010 : DMA2 011 : DMA3 100 : None

Index 0xF0h 0x08, 0x08

Bit	Description
7	0: Normal write protect signal 1: Force write protect signal
6-5	Read as 0
4	0 : No swap. 1 : Swap Drive 0 and Drive 1
3	0 : PS2 mode 1 : AT mode
2	Read as 0.
1	0 : Burst DMA mode. 1 : Non-burst DMA mode
0	reserved

Index 0xF1h 0x00, 0x00

Bit	Description
7-4	Reserved
3-2	Density Select. 0x : Normal 10 : force to 1 11 : force to 0
1-0	External Floppy Select. 0x : internal FDC 10 : external FDC 11 : Drive A internal, Drive B external

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Index 0xF2h 0xFF, 0xFF

Bit	Description
7-0	Reserved

Index 0xF4h 0x00, 0x00

Bit	Description
7-5, 2	Read as 0.
3	Data Rate Table Select 0 : Regular drive 1 : 3-mode drive
4, 1-0	Reserved.

LOGICAL DEVICE 3 REGISTERS (Parallel Port)

Index 0x30h 0x00, 0x00

Bit	Description
7-1	Read as 0.
0	Activate Parallel Port. *1 0 : disable 1 : enable

*1 - The disable function of the device has the same behavior as direct powerdown function except the device remains at reset state.

Index 0x60h 0x03, 0x03

Bit	Description
7-0	The higher address of the Parallel Port's I/O base address.

Index 0x61h 0x78, 0x78

Bit	Description
7-2	The lower address of the Parallel Port's I/O base address.
1-0	Set to 0.

Note : An 8-byte boundary is required if EPP is available

Index 0x70h 0x05, 0x05

Bit	Description
7-4	Read as 0.
3-0	Select IRQ channel used by Parallel Port. 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

Index 0x74h 0x04, 0x04

Bit	Description
7-3	Read as 0.
2-0	Select DMA channel used by Parallel Port. 000 : DMA0 001 : DMA1 010 : DMA2 011 : DMA3 100 : None

Index 0xF0h 0x8C, 0x8C

Bit	Description
7	Parallel Port IRQ polarity 1 : active low 0 : active high
6-3	ECP FIFO threshold value. Default is 0001.
2-0	Parallel Port mode.select 000 : PS2 001 : EPP 1.9 010 : ECP 011 : ECP+EPP1.9 100 : SPP (default) 101 : EPP 1.7 111 : ECP+EPP 1.7

Index 0xF1h 0x85, 0x85

Bit	Description
7	0 : Normal 1 : Force Parallel Port into extend mode
6-3	Read as 0.
2	Parallel Port operation clock 0: 24MHz 1: 12MHz
1	EPP time-out interrupt. 0 : disable 1 : enable
0	0 : Non-burst DMA mode. 1 : Burst DMA transfer mode in ECP

LOGICAL DEVICE 4 REGISTERS (UART1)

Index 0x30h 0x00, 0x00

Bit	Description
7-1	Read as 0.
0	UART1 *1 0 : disable 1 : enable

Index 0x60h 0x03, 0x03

Bit	Description
7-0	The higher address of the UART1's I/O base address.

Index 0x61h 0xF8, 0xF8

Bit	Description
7-3	The lower address of the UART1's I/O base address.
2-0	Set to 0.

Index 0x70h 0x04, 0x04

Bit	Description
7-4	Read as 0.
3-0	Select IRQ used by UART1. 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

Index 0xF0h 0x00, 0x00

Bit	Description
7-3	Read as 0.
2	0 : Normal 1 : 8MHz clock source for UART1
1	High speed mode 0 : disable 1 : enable
0	MIDI support 0 : disable 1 : enable

Index 0xF1h 0x00, 0x00

Bit	Description
7-5	Read as 0.
4-3	IR mode. 00 : Normal 01 : IrDA 10 : ASK IR 11 : Normal
2	0 : Full duplex in IR 1 : Half duplex in IR
1	IR transmit polarity. 0 : active high 1 : active low
0	IR receive polarity. 0 : active high 1 : active low

Index 0xF2h 0x0C, 0x0C

Bit	Description
7-5	Read as 0.
4-3	IR half-duplex time-out time control. 00 : 41-bit time for Tx, 39-bit time for Rx. 01 : 42-bit time for Tx, 39-bit time for Rx. 1x : 40-bit time for Tx and Rx.
2	IR half-duplex Rx-to-Tx time-out timer. 0 : disable 1 : enable
1	IR half-duplex Tx-to-Rx time-out timer. 0 : disable 1 : enable
0	Baud Rate output on RI1. 0 : disable 1 : enable

LOGICAL DEVICE 5 REGISTERS (UART2)
(or LOGICAL DEVICE B REGISTERS)

Index 0x30h 0x00, 0x00

Bit	Description
7	FIR function 0 : disable 1 : enable
6-1	Read as 0.
0	UART2 *1 0 : disable 1 : enable

Index 0x60h 0x03, 0x03

Bit	Description
7-0	Higher address of the UART2's I/O base address.

Index 0x61h 0xE8, 0xE8

Bit	Description
7-3	The lower address of the UART2's I/O base address.
2-0	Set to 0.

Index 0x70h 0x09, 0x09

Bit	Description
7-4	Read as 0.
3-0	Select IRQ channel used by UART2 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

Index 0x74 0x04, 0x04

Bit	Description
7-3	Read as 0.
2-0	Select DMA channel used by FIR 000: DMA0 001: DMA1 010: DMA2 011: DMA3 100: None

Index 0xF0h 0x80, 0x80

Bit	Description
7	FIR transceiver module type 0: IBM like module 1: HP like module
6	FIR transceiver connector type 0: 5-pin (Vcc,IRRXH,IRRX2,Gnd,IRTX2) 1: 6-pin (Vcc,IRRXH,IRRX2,Gnd,IRTX2,CVROFF)
5-3,1-0	Read as 0.
2	1 : 8MHz clock source for UART2 0 : Normal

Index 0xF1h 0x00, 0x00

Bit	Description
7-5	Read as 0.
4-3	IR mode. 00 : Normal 01 : IrDA 10 : ASK IR 11 : Normal
2	1 : Half duplex in IR 0 : Full duplex in IR.
1	IR transmit polarity. 0: active high 1: active low
0	IR receive polarity. 0 : active high 1 : active low

Index 0xF2h 0x0C, 0x0C

Bit	Description
7-5	Read as 0.
4-3	IR half-duplex time-out time control. 1x : 40-bit time for Tx and RX 01 : 42-bit time for Tx, 39-bit time for Rx 00 : 41-bit time for Tx, 39-bit time for Rx
2	IR half-duplex Rx-to-Tx time-out timer 0 : disable 1 : enable
1	IR half-duplex Tx-to-Rx time-out timer. 0 : disable 1 : enable
0	Baud Rate output on IRRXH 0 : disable 1 : enable

Note : As UART2 enable bit =1 and FIR enable bit =1, (1) Change registers from NS16550 to FIR, have to continuously write bit 7-5 of base address +4 (Modem Control Register) as following : 001,011,100, (2) Change registers from FIR to NS-16550, write one to bit 7 of base address +7 (FIR master block control register)

LOGICAL DEVICE 7 REGISTERS (KEYBOARD)

Index 0x30h N/A, 0x00

Bit	Description
7-1	Read as 0.
0	Keyboard controller. This bit is initialized by hardware setting through RTS2J. 0 : disable 1 : enable

Index 0x70h 0x01, 0x01

Bit	Description
7-4	Read as 0.
3-0	Select IRQ channel used by Keyboard. 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

Index 0x72h 0x00, 0x00

Bit	Description
7-4	Read as 0.
3-0	Select IRQ channel used by PS/2 Mouse. 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

Index 0xF0h 0x00, 0x00

Bit	Description
7	Read as 0.
6	Read only. Indicates the type of keyboard 0 : PS2. 1 : AT
5-4	Keyboard clock source speed 00 : 8MHz 01 : 12MHz 10 : 16MHz 11 : Reserved
3-0	Read as 0.

LOGICAL DEVICE B REGISTERS (UART3)
(or LOGICAL DEVICE 5 REGISTERS)

Index 0x30h 0x00, 0x00

Bit	Description
7-1	Read as 0.
0	UART3 *1 0 : disable 1 : enable

Index 0x60h 0x02, 0x02

Bit	Description
7-0	The higher address of the UART3's I/O base address.

Index 0x61h 0xF8, 0xF8

Bit	Description
7-3	The lower address of the UART3's I/O base address.
2-0	Set to 0.

Index 0x70h 0x03, 0x03

Bit	Description
7-4	Read as 0.
3-0	Select IRQ used by UART3. 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

Index 0xF0h 0x00, 0x00

Bit	Description
7-3	Read as 0.
2	0 : Normal 1 : 8MHz clock source for UART3
1	High speed mode 0 : disable 1 : enable
0	MIDI support 0 : disable 1 : enable

Index 0xF1h 0x00, 0x00

Bit	Description
7,5	Read as 0.
6	UART3 serial input signal source 0 : SIN2 1 : IRRX2
4-3	IR mode. 00 : Normal 01 : IrDA 10 : ASK IR 11 : Normal
2	0 : Full duplex in IR 1 : Half duplex in IR
1	IR transmit polarity. 0 : active high 1 : active low
0	IR receive polarity. 0 : active high 1 : active low

Index 0xF2h 0x0C, 0x0C

Bit	Description
7-5	Read as 0.
4-3	IR half-duplex time-out time control. 00: 41-bit time for Tx, 39-bit time for Rx 01: 42-bit time for Tx, 39-bit time for Rx 1x: 40-bit time for Tx and Rx
2	IR half-duplex Rx-to-Tx time-out timer. 0 : disable 1 : enable
1	IR half-duplex Tx-to-Rx time-out timer. 0 : disable 1 : enable
0	Baud Rate output on RI2. 0 : disable 1 : enable

LOGICAL DEVICE C REGISTERS (HOTKEY)

Index 0x30h N/A, N/A

Bit	Description
7-1	Read as 0.
0	HOTKEY 0 : disable 1 : enable

Index 0xF0h 0x35, 0x35

Bit	Description
7-6	Read as 0.
5	Hotkey C is the last pressed key 0 : No 1 : Yes
4	Hotkey C 0 : disable 1 : enable
3	Hotkey B is the last pressed key 0 : No 1 : Yes
2	Hotkey B 0 : disable 1 : enable
1	Hotkey A is the last pressed key 0 : No 1 : Yes
0	Hotkey A 0 : disable 1 : enable

Index 0xF1h 0x14, 0x14 (Ctrl)

Bit	Description
7-0	Make code of Hotkey A

Index 0xF2h 0x11, 0x11 (Alt)

Bit	Description
7-0	Make code of Hotkey B

Index 0xF3h 0x71, 0x71 (Del)

Bit	Description
7-0	Make code of Hotkey C

Index 0xF4h 0x42, 0x42

Bit	Description
7	Hotkey issue level 0 : HOTKEY issue a pulse 1 : HOTKEY issue a level signal
6	Bypass KBC 0 : KCLK is controlled by KBC & HOTKEY 1 : KCLK is controlled by HOTKEY only
5-4	Reserved.
3	Read as 0.
2-0	Pulse width of Hotkey event 000 : 8ms 001 : 16ms 010 : 32ms (Default) 011 : 64ms 100 : 128ms 101 : 256ms 110 : 512ms 111 : 1sec

Table 4-1 M1543C Super I/O Hardware Setting Configuration

Pin Name	Function
RTS1J 0 1	CFG_PORT 0x370h 0x3F0h
RTS2J 0 1	KBC_EN disable enable
DTR2J 0 1	PS2_ATJ (KBC) AT mode PS2 mode

Table 4-2 Drive Mode bit mapping for DENSEL pin

Data Rate	Bit 1-0 of 3F7h	Drive Mode bit of Index 0xF4	DENSEL
1Mbps	11	0	1
500Kbps	00	0	1
300Kbps	01	0	0
250Kbps	10	0	0
1Mbbs	11	1	1
500Kbps	00	1	1
500Kbps	01	1	0
250Kbps	10	1	0

4.4.2 Power Management Features

The M1543C contains power management features that makes it ideal for design of notebook and portable personal computers. These features are not recommended for ACPI compliant function.

4.4.2.1 Powerdown Modes of FDC

The FDC is powered down in two ways: direct powerdown and automatic powerdown. Direct powerdown results in immediate powerdown of the part regardless the current state of the part. Automatic powerdown results when certain conditions become true within the part.

A. Direct Powerdown

Direct powerdown is conducted via the POWER-DOWN bit in the DSR register (bit 6). Programming this bit high will powerdown the M1543C after the part is internally reset. All current status is lost if this type of powerdown mode is used. The part can exit powerdown from this mode via any hardware or software reset. This type of powerdown will override the automatic powerdown. If the part is in automatic powerdown when the DSR powerdown is issued, then all the previous status of the part will be lost, and the M1543C will be reset to its default values.

B. Auto Powerdown

Automatic powerdown is conducted via a "Powerdown Mode" command. There are four conditions required before the part will enter powerdown. All these conditions must be true for the part to initiate the powerdown sequence. These conditions are listed as follows :

1. The motor enable pins MOT0 and MOT1 must be inactive,
2. The part must be idle; this is indicated by MSR = 80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupt),
3. The head unload timer must have expired, and
4. The auto powerdown timer must have timed out.

The command can be used to enable powerdown by setting the APD bit in the command to high. The command also provides a capability of programming a minimum power-up time via the DLY bit in the command. The minimum power-up time refers to a minimum amount of time the part will remain powered-up after being awakened or reset. An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down provided all the remaining conditions are met. Any software reset will re-initialize the timer.
Disabling the auto powerdown mode cancels the timers and holds the M1543C out of auto powerdown.

4.4.2.2 WAKE UP MODES of FDC

This section describes the conditions for awakening the FDC from both direct and automatic powerdown. Some amount of time is required for the FDC to exit powerdown state and prepare the internal microcontroller to accept commands. Thus the recovery time of the wake-up process must be carefully controlled by the system software.

A. Wake Up from DSR Powerdown

If the M1543C enters powerdown through the DSR powerdown bit, it must be reset to exit. Any form of software or hardware reset will reset the DSR's powerdown bit, although reset the bit through DSR is recommended. No other register access will awaken the part.
If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened by a software reset, the auto powerdown command (including the minimum delay timer) will again become effective as previously programmed. If the part is awakened via a hardware reset, the auto powerdown is disabled.
After reset, the part will go through a normal sequence. The drive status will be initialized. The FIFO mode will be set to default mode on a hardware reset or on a software reset if the LOCK command is not blocking it. Finally, after a delay, the polling interrupt will be issued.

B. Wake Up from Auto Powerdown

If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.
If a hardware or software reset is used, then the part goes through the normal reset sequence. If the access is through the selected registers, then the M1543C resumes operation as though it was never in powerdown. Besides activating the MR pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake-up the FDC also:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not wake-up the part)
2. A read from the MSR register
3. A read or write to the FIFO register

Any of these actions will wake-up the FDC. Once awake, the M1543C will initiate the auto powerdown time for 10 ms or 0.5 sec. (Depending on the DLY bit the auto powerdown command). The part will powerdown again when all the powerdown conditions stated in the *Auto Powerdown* section are satisfied.

4.4.2.3 Powerdown Mode of UART and Printer

UART1, UART2 and printer can enter auto powerdown by setting their relative powerdown bit in index 0x23.

4.4.3 Floppy Disk Controller

4.4.3.1 Register Overview

The FDC of the M1543C is register and hardware-level compatible with the industry standard 765A and 82077SL standards. Table 4-3 below lists the I/O address map of the FDC controller.

Table 4-3 FDC Controller I/O Address Map

A2	A1	A0	R/W	Register
0	0	0	R	Status Register A,SRA
0	0	1	R	Status Register B, SRB
0	1	0	R/W	Digital Output Register DOR
0	1	1	R/W	Tape Drive Register TDR
1	0	0	R	Main Status Register MSR
1	0	0	W	Data Rate Select Register DSR
1	0	1	R/W	Data Register (FIFO)
1	1	0	X	Reserved
1	1	1	R	Digital Input Register DIR
1	1	1	W	Configuration Control Register CCR

Status Register A (SRA), Read Only

This is a read-only diagnostic register that is part of the PS/2 FDC register set, and is enabled when in the PS/2 mode. This register monitors the state of the IRQ6 pin and some of the disk interface signals. The SRO can be read at any time when in PS/2 mode. In PC-AT mode, SD[7-0] are tri-state during a read.

Bit	Description
7	**Interrupt Pending** : The state of the Floppy Disk Interrupt output (active high).
6	**2nd Drive Installed** : Indicates if a second drive has been installed
5	**Step** : Active high status of the STEPJ pin
4	**Track 0** : Active low status of the TRK0J pin
3	**Head Select** : Active high status of the HDSELJ pin
2	**Index** : Active low status of the INDEXJ pin.
1	**Write Protect** : Active low status of the WPJ pin.
0	**Direction** : Active high status of the DIRJ pin.

Status Register B (SRB), Read Only

Bit	Description
7-6	**Reserved** : Always read as a logic "1"
5	**Drive Select 0** : Reflects the status of the Drive Select bit 0 of DOR (address 3F2, bit 0). This bit is cleared after a hardware reset, it is unaffected by a software reset
4	**Write Data Toggle** : This bit changes state at every inactive edge of the WDATAJ
3	**Read Data Toggle** : Every inactive edge of the RDATAJ input causes this bit to change state.
2	**Write Gate** : Active high status of the WGATEJ pin.
1	**Motor Enable 1** : The MOT1J disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.
0	**Motor Enable 0** : The MOT0J disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

Digital Output Register (R/W)

Digital Output Register Description

Bit	Description
7	**Motor Enable 3:** This controls the Motor for drive 3, MOT3. The output is high when it is inactive, and low when it is active. This bit and DOR bit 6 provide information that controls the MOT1 and MOT0 pins, respectively when bit 7 of the configuration register is set.
6	**Motor Enable 2:** Same function as D7 except for drive 2's motor. Note that this signal is not brought out to a pin.
5	**Motor Enable 1:** This bit controls the Motor for drive 1's motor. When this bit is 0, the MOT1 output is high.
4	**Motor Enable 0:** Same as D5 except for drive 0's motor.
3	**DMA Enable:** When set to a 1, this enables the DRQ, DAK, and INT pins. A zero disables these signals.
2	**Reset Controller:** This bit resets the controller when 0 and enables normal operation when it is a 1. It does not affect the drive control or data rate registers which are reset only by a hardware reset.
1~0	**Drive Select:** These two pins are encoded for the four drive select, and are gated with the motor enable lines, so that only one drive is selected when its motor enable is active.

Table 4-4 Internal 4 Drive Decode - Normal

Digital Output Register						Drive Select Outputs		Motor on Outputs	
D7	D6	D5	D4	D1	D0	DRV1	DRV0	MOT1	MOT0
x	x	x	1	0	0	1	0	/D5	/D4
x	x	1	x	0	1	0	1	/D5	/D4
x	1	x	x	1	0	1	1	/D5	/D4
1	x	x	x	1	1	1	1	/D5	/D4
0	0	0	0	x	x	1	1	/D5	/D4

Table 4-5 Internal 4 Drive Decode - Drives 0 and 1 Swapped

Digital Output Register						Drive Select Outputs		Motor on Outputs	
D7	D6	D5	D4	D1	D0	DRV1	DRV0	MOT1	MOT0
x	x	x	1	0	0	0	1	/D4	/D5
x	x	1	x	0	1	1	0	/D4	/D5
x	1	x	x	1	0	1	1	/D4	/D5
1	x	x	x	1	1	1	1	/D4	/D5
0	0	0	0	x	x	1	1	/D4	/D5

Tape Drive Register (TDR)

This register allows the user to assign tape support to a particular drive during initialization. A hardware reset sets all bits in this register to 0 making drive 0 not available for tape support. Drive 0 is reserved for the floppy boot drive.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Reg 3F3	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	tapesel1	tapesel0

Main Status Register

The read-only main status register indicates the current status of the disk controller. It is always available to be read. One of its functions is to control the flow of data to and from the data register. It also indicates when the disk controller is ready to send or receive data. It should be read before each byte is transferred to or from the data register except during a DMA transfer. No delay is required when reading this register after a data transfer.

Main Status Register Description

Bit	Description
7	**Request for Master (RQM) :** Indicates that the data register is ready to send or receive data from the CPU. This bit is cleared immediately after a byte transfer, and is set again as soon as the disk controller is ready for the next byte.
6	**Data Direction (DIO) :** Indicates whether the controller is expecting a byte to be written to (0) or read from (1) the data register.
5	**Non-DMA Execution:** Bit is set only during the execution phase of a command if it is in the non-DMA mode. In other words, if this bit is set, the multiple byte data transfer (in the execution phase) must be monitored by the CPU either through interrupts, or software polling as described in the processor software interface section.
4	**Command in Progress:** Bit is set after the first byte of the command phase is written. Bit is cleared after the last byte of the result phase is read. If there is no result phase in a command, the bit is cleared after the last byte of the command phase is written.
3~0	**Drives 3~0 Seeking:** Set after the last byte of the command phase of a seek or recalibrate command is issued for drives 3~0, respectively. Cleared after reading the first byte in the result phase of the sense interrupt command for this drive.

Data Rate Select Register (DSR)

Datarate Select Register Description

Bit	Description
7	**S/W RESET** behaves the same as DOR RESET except that this reset is self clearing.
6	**POWERDOWN** bit implements direct powerdown. Setting this bit high puts the FDC into the powerdown state regardless of the state of the part. The part is reset internally and then put into powerdown. No status is saved and any operation in progress is aborted. Any hardware or software reset will exit the M1543C from this powerdown state.
5	**reserved**
4~2	**PRECOMP 0-2** adjusts the WRDATA output to the and disk to compensate for magnetic media phenomena known as bit shifting. The data patterns that are susceptible to bit shifting are well understood and the M1543C compensates the data pattern as it is written to the disk. The amount of precompensation depends upon the drive and media but in most cases the default value is acceptable. The M1543C starts precompensating the data pattern starting on Track 0. The CONFIGURE command can change the starting track for precompensation. The default value is selected if the three bits are zeros.
1~0	**DRATE 0-1** select one of the four data rates as listed in table next page. The default value is 250 Kbps upon a chip ("Hardware") reset. Other ("Software") Resets do not affect the DRATE or PRECOMP bits.

Table 4-6 Precompensation Delay Values Table

PRECOMP 432 bits	Precompensation Delay--DISABLED
111	0.00ns
001	41.67ns
010	83.34ns
011	125.00ns
100	166.67ns
101	208.33ns
110	250.00ns
000	DEFAULT

Table 4-7 Default Precompensation Delay Values

Data Rate	Precompensation Delay
1 Mbps	41.67ns
500 Kbps	125ns
300 Kbps	125ns
250 Kbps	125ns

Table 4-8 Data Rate

DRATESEL		Data Rate	
		MFM	FM
1	1	1 Mbps	Illegal
0	0	500 Kbps	250 Kbps
0	1	300 Kbps	150 Kbps
1	0	250 Kbps	125 Kbps

Data Register (R/W)

This is the location through which all commands, data, and status flow between the CPU and the FDC. During the command phase, the CPU loads the controller's commands into this register based on the status register request for master and data direction bits. The result phase transfers the status registers and header information to the CPU in the same fashion.

All command parameter information and disk data transfers go through the FIFO. The 16-byte FIFO has programmable threshold values. Data transfers are generated by the RQM and DIO bits in the Main Status Register.

The FIFO default to an 765A compatible mode. The default values can be changed through the CONFIGURE command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk error. Table below gives several examples of the delays with a FIFO. The data is based upon the following formula:

Threshold# * 1/DATA RATE * 8 - 1.5_{us} = DELAY

Table 4-9 FIFO Service Delay Table

FIFO Threshold Examples	Maximum Delay to Servicing at 1 Mbps Data Rate
1 byte	$1 * 8_{us} - 1.5_{us} = 6.5_{us}$
2 bytes	$2 * 8_{us} - 1.5_{us} = 14.5_{us}$
8 bytes	$8 * 8_{us} - 1.5_{us} = 62.5_{us}$
15 bytes	$15 * 8_{us} - 1.5_{us} = 118.5_{us}$
FIFO Threshold Examples	**Maximum Delay to Servicing at 500 Mbps Data Rate**
1 byte	$1 * 16_{us} - 1.5_{us} = 14.5_{us}$
2 bytes	$2 * 16_{us} - 1.5_{us} = 30.5_{us}$
8 bytes	$8 * 16_{us} - 1.5_{us} = 126.5_{us}$
15 bytes	$15 * 16_{us} - 1.5_{us} = 238.5_{us}$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the M1543C enters the command execution phase, it clears the FIFO of any data to ensure that invalid data is not transferred.
An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC.

Configuration Control Register (CCR, PC-AT Modes)

Configuration Control Register Description

Bit	Description
7~2	Not used.
1, 0	**Data Rate Select:** These bits set the data-rate and write-precompensation values for the disk controller. After a hardware reset, these bits are set to 1, 0 (250 Kbps).

Digital Input Register (DIR, Read)

Digital Input Register Description (PC/AT mode)

Bit	Description
7	DSKCHG monitors the pin of the same name and reflects the opposite value seen on the disk cable. The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits remain tri-stated.
6~0	These bits are reserved for use by the hard disk controller, thus during a read of this register, these bits are in high impedance state.

Digital Input Register (PS/2 mode)

Bit	Description
7	DSKCHG monitors the pin of the same name and reflects the opposite value seen on the disk cable.
6~3	undefined, always read as logic "1".
2~1	Data rate select. These bits control the data rate of the floppy controller. These bits are unaffected by a software reset, and are set to 250 kbps after a hardware reset.
0	High density. This bit is low whenever the 500 kbps or 1 Mbps data rates are selected, and high when 250 kbps and 300 kbps are selected.

4.4.3.2 Result Phase Status Registers

The result phase of a command contains bytes that hold status information. The format of these bytes are described in the following sections. Do not confuse these register bytes with the main status register which is a read-only register that is always available. The result phase status registers are read from the data register only during the result phase.

Status Register 0 (ST0)

Status Register 0 Description

Bit	Description
7~6	Interrupt Code : 00 = Normal termination of command. 01 = Abnormal termination of command. Command was executed, but not successfully completed. 10 = Invalid command issue. Command issued was not recognized as a valid command. 11 = Ready changed state during the polling mode.
5	Seek End: This bit is set after a seek or recalibrate command is completed by the controller. Used during sense interrupt command.
4	Equipment Check: This bit is set after a recalibrate command track 0 signal failed to occur. Used during sense interrupt command.
3	Not Used: 0
2	Head Number: At end of execution phase.
1, 0	Drive Select: At end of execution phase. 00 = Drive 0 selected 01 = Drive 1 selected 10 = Drive 2 selected 11 = Drive 3 selected

Status Register 1 (ST1)

Status Register 1 Description

Bit	Description
7	**End of Track:** This bit is set when the controller has transferred the last byte of the last sector without the TC pin becoming active. The last sector is the end-of-track sector number programmed in the command phase.
6, 3	**Not Used:** 0
5	**CRC Error:** If this bit is set and bit 5 of ST2 is clear, then there was a CRC error in the address field of the correct sector. If bit 5 of ST2 is set, then there was a CRC error in the data field.
4	**Over Run:** This bit is set when the controller was not serviced by the CPU soon enough during a data transfer in the execution phase.
2	**No Data:** This bit is set for any three possible problems: 1. Controller cannot find the sector specified in the command phase during the execution of a read, write, or scan command. An address mark was found even if it is not a blank disk. 2. Controller cannot read any address fields without a CRC error during read ID command. 3. Controller cannot find the starting sector during execution of read a track command.
1	**Not Writable:** Set if the write protect pin is active when a write or format command is issued.
0	**Missing Address Mark:** If this bit is set and bit 0 of ST2 is clear then the disk controller cannot detect any address field address mark after two disk revolutions. If bit 0 of ST2 is set, then the disk controller cannot detect the data field address mark.

Status Register 2 (ST2)

Status Register 2 Description

Bit	Description
7	**Not Used:** 0
6	**Control Mark:** This bit is set if the controller tried to read a sector which contained a deleted data address mark during execution of read-data or scan commands. Or, if a read-deleted-data command was executed, a regular address mark was detected.
5	**CRC Error in Data Field:** This bit is set if the controller detected a CRC error in the data field. Bit 5 of ST1 is also set.
4	**Wrong Track:** This bit is only set if the desired sector is not found, and the track number recorded on any sector of the current track is different from that stored in the track register.
3	**Scan Equal Hit:** This bit is only set if the equal condition is satisfied during any scan command.
2	**Scan Not Satisfied:** This bit is set if the controller cannot find a sector on the track number recorded on any sector on the track which meets the desired condition during scan command.
1	**Bad Track:** This bit is only set if the desired sector is not found, and the track number recorded on any sector on the track is different from that stored in the track register and the recorded track number is FF.
0	**Missing Address Mark in Data Field:** This bit is set if the controller cannot find the data field address mark during read/scan command. Bit 0 of ST1 is also set.

Status Register 3 (ST3)

Status Register 3 Description

Bit	Description
7	**Not Used:** 0
6	**Write Protect Status:** This bit is the complement of the associated FDC interface pin for the drive selected in DCR.
5	**Not Used:** 1
4	**Track 0 Status:** This bit is the complement of the associated FDC interface pin for the drive selected in the DCR.
3	**Not Used:** 0
2	**Head Select Status:** This bit shows the status of the associated bit in the sense-drive-status command phase.
1, 0	**Drive Selected:** These bits show the status of the associated bits in the sense-drive-status command phase. These bits show the same status as ST0 bits 1, 0. 00 = Drive 0 selected 01 = Drive 1 selected 10 = Drive 2 selected 11 = Drive 3 selected

4.4.3.3 Controller Functional Description

Controller Phases
The FDC handles commands in three phases—command, execution and result. Each phase is described below.

Command Phase
The CPU writes a series of bytes to the data register. These bytes indicate the command desired and the particular parameters required for the command. All the bytes must be written in the order specified in the command description table. The execution phase starts immediately after the last byte in the command phase is written.
The Main Status Register controls the flow of command bytes, and must be polled by the software before writing each Command Phase byte to the Data Register. Prior to writing a command byte, the bit 7 must be set and bit 6 must be cleared in the MSR. After the first command byte is written to the Data Register, the bit 4 in MSR is also set and remain set until the last Result Phase byte is read. If there is no Result Phase, it is cleared after the last command byte is written. A new command may be initiated after reading all the result bytes from the previous command.

Execution Phase

The disk controller performs the desired command. Some commands require the CPU to read or write data to or from the data register during this phase. Some commands such as Seek control the read/write head movement on the disk drive. Some commands does not involve any action by the uP or disk drive, and consists of an internal operation by the controller.
If there is data to be transfer between the uP and the controller, there are three methods that can be used, DMA mode, interrupt mode, and software polling mode. All of these data transfer mode work with the FIFO enabled or disabled.

DMA Mode

If the DMA mode is selected, a DMA request is generated in the execution phase when each byte is ready to be transferred. To enable DMA operations during the execution phase, the DMA mode bit in the Specify command must be enabled, and the DMA signals must be enabled in the Drive Control Register. The DMA controller responds to the DMA request with a DMA-acknowledge and a read- or write-strobe. The DMA request is cleared by the active edge of the DMA-acknowledge. After the last byte is transferred, an interrupt is generated, indicating the beginning of the result phase. TC is asserted to terminate an operation. Due to internal gating, TC is only recognized when the -DAK input is low.

Interrupt Mode

If the non-DMA mode is selected, an interrupt is generated in the execution phase when each byte is ready to be transferred. The Main Status Register should be read to verify that the interrupt is for a data transfer. Bits 5 and 7 of the Main Status Register is set. The interrupt is cleared when the byte is transferred to or from the data register. The CPU should transfer the byte within the allotted time. If the byte is not transferred within the time allotted, an overrun error is indicated in the result phase when the command terminates at the end of the current sector.

An interrupt is also generated after the last byte is transferred. This indicates the beginning of the Result Phase.

Software Polling
If the non-DMA mode is selected and interrupts are not suitable, the CPU can poll the Main Status Register during the execution phase to determine when a byte is ready to be transferred. The bit 7 of the Main Status Register reflects the state of the interrupt pin. Otherwise, the data transfer is similar to the interrupt mode described above.

Result Phase

During the Result Phase, the uP reads a series of bytes from the data register. These bytes indicate the status of the command. This status may indicate whether the command executed properly, or contain some control information. The bit 7 and bit 6 in the MSR must both be set before each result byte can be read. After the last result byte is read, the bit 4 in the MSR is cleared, and the controller is ready for the next command.

Command Set Descriptions

Summary of the command set.

Table 4-10 M1543C FDC Command Table

READ DATA

Command Phase

MT	MFM	SK	0	0	1	1	0
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ A TRACK

Command Phase

0	MFM	0	0	0	0	1	0
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ DELETED DATA

Command Phase

MT	MFM	SK	0	1	1	0	0
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ ID

Command Phase

0	MFM	0	0	1	0	1	0
0	0	0	0	0	HD	DR1	DR0

Execution Phase: Controller reads first ID Field header bytes it can find and reports these bytes to the system in the result bytes

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

WRITE DATA

Command Phase

MT	MFM	0	0	0	1	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data is transferred form the system to the controller via DMA or Non-DMA modes and written to the disk.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

WRITE DELETED DATA

Command Phase

MT	MFM	0	0	1	0	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data is transferred form the system to the controller via DMA or Non-DMA modes and written to the disk.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

FORMAT A TRACK

Command Phase

0	MFM	0	0	1	1	0	1
0	0	0	0	0	HD	DR1	DR0
Bytes per Sector							
Sector per Track							
Format Gap							
Data Pattern							

Execution Phase: System transfers four ID bytes per sector to the floppy controller via DMA or Non-DMA modes. The entire track is formatted. The data block in the Data Field of each sector is filled with the data pattern byte

Result Phase

Status Register 0
Status Register 1
Status Register 2
Undefined
Undefined
Undefined
Undefined

SCAN EQUAL

Command Phase

MT	MFM	SK	1	0	0	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data transfer from system to controller is compared to data read from disk

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

SCAN HIGH OR EQUAL

Command Phase

MT	MFM	SK	1	1	1	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data transfer from system to controller is compared to data read from disk

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

SCAN LOW OR EQUAL

Command Phase

MT	MFM	SK	1	0	0	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data transfer from system to controller is compared to data read from disk

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

VERIFY

Command Phase

MT	MFM	SK	1	0	1	1	0
0	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data is read from disk but not transferred to the system.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

DUMPREG

Command Phase

0	0	0	0	1	1	1	0

Execution Phase: Internal registers read

Result Phase

Present Track Number on Drive 0							
Present Track Number on Drive 1							
Present Track Number on Drive 2							
Present Track Number on Drive 3							
Step Rate Time				Motor Off Time			
Motor On Time							DMA
Sector per Track/End of Track							
LOCK	0	D3	D2	D1	D0	GAP	WG
0	EIS	FIFO	POLL	FIFOTHR			
PRETRK							

PERPENDICULAR MODE

Command Phase

0	0	0	1	0	0	1	0
OW	0	D3	D2	D1	D0	GAP	WG

Execution Phase: Internal registers are written.

No Result Phase.

CONFIGURE

Command Phase

0	0	0	1	0	0	1	1
0	0	0	0	0	0	0	0
0	EIS	FIFO	POLL	FIFOTHR			
PRETRK							

Execution Phase: Internal registers are written.
No Result Phase

RECALIBRATE

Command Phase

0	0	0	0	0	1	1	1
0	0	0	0	0	0	DR1	DR0

Execution Phase: Disk drive head is stepped out to Track 0.
No Result Phase

RELATIVE SEEK

Command Phase

1	DIR	0	0	1	1	1	1
0	0	0	0	0	HD	DR1	DR0
Relative Track Number							

Execution Phase: Disk drive head stepped in or out from a programmable number of tracks.
No Result Phase

SEEK

Command Phase

0	0	0	0	1	1	1	1
0	0	0	0	0	HD	DR1	DR0
New Track Number							

Execution Phase: Disk drive head is stepped in or out to a desired track.
No Result Phase

SENSE DRIVE STATUS

Command Phase

0	0	0	0	0	1	0	0
0	0	0	0	0	HD	DR1	DR0

Execution Phase: Disk drive status information is detected and reported.
Result Phase

Status Register 3

SENSE INTERRUPT

Command Phase

0	0	0	0	1	0	0	0

Execution Phase: Status of interrupt is reported
Result Phase

Status Register 0
Present Track Number

SPECIFY

Command Phase

0	0	0	0	0	0	1	1
Step Rate Time				Motor Off Time			
Motor On Time							DMA

Execution Phase: Internal registers are written.
No Result Phase

POWERDOWN MODE

Command Phase

0	0	0	1	0	1	1	1
0	0	0	0	0	0	DLY	APD

Execution Phase: Internal registers are written
Result Phase

0	0	0	0	0	0	DLY	APD

VERSION

Command Phase

0	0	0	1	0	0	0	0

Result Phase

1	0	0	1	0	0	0	0

LOCK

Command Phase

LOCK	0	0	1	0	1	0	0

Execution Phase: Internal registers are written.
Result Phase

0	0	0	LOCK	0	0	0	0

INVALID

Command Phase

Invalid Codes

Result Phase

Status Register 0 (80H)

4.4.3.4 Command Description

Read Data

The read data op-code is written to the data register followed by 8 bytes as specified in the command table. After the last byte is written, the controller starts looking for the correct sector header. Once the controller is found, the controller sends data to the CPU. After one sector is finished, the sector number is incremented by one and this new sector is searched for. If MT (multi-track) is set, both sides of one track can be read. Starting on side zero, the sectors are read until the sector number specified by end of track sector number is reached. Then, side one is read by starting with sector number one.

In DMA mode, the read-data command continues to read until the TC pin is set. This means that the DMA controller should be programmed to transfer the correct number of bytes. TC should be controlled by the CPU and be asserted when enough bytes are received. An alternative to these methods of stopping the read-data command is to program the end of track sector number as the last sector number that to be read. The controller stops reading the disk with an error message indicating that it tried to access a sector number beyond the end of the track.

The number of data bytes per sector parameter is defined in table below. If this is set to zero, the data length parameter defines the number of bytes that the controller transfers to the CPU. If the data length specified is smaller than 128, the controller still reads the entire 128 byte sector and checks the CRC, though only the number of bytes specified by the data length parameter are transferred to the CPU. Data length parameter should not be set to zero. If the number of bytes per sector parameter is not zero, the data length parameter has no meaning and should be set to FFh.

Table 4-11 Sector Size Selection

Bytes/Sector Code	Number of Bytes in Data Field
0	128
1	256
2	512
3	1024
4	2048
5	4096
6	8192

If the implied seek mode is enabled by both the CONFIGURE command and the IPS bit in this command, a seek is performed to the track number specified in the command phase. The controller also waits for the head-settle-time if the implied seek is enabled. After all these conditions are met, the controller searches for the specified sector by comparing the track number, head number, sector number, and number of bytes/sector given in the command phase with the appropriate bytes read off the disk in the address fields.

If the correct sector is found, but there is a CRC error in the address field, bit 5 of ST1 (CRC error) is set and an abnormal termination is indicated. If the correct sector is not found, bit 2 of ST1 (no data) is set and an abnormal termination is indicated. In addition to this, if any address field track number is FF, bit 1 of ST2 (bad track) is set or, if any address field track number is different from that specified in the command phase, bit 4 of ST2 (wrong track) is set.

After finding the correct sector, the controller reads that data field. If a deleted data mark is found and the SK bit is set, the sector is not read, bit 6 of ST2 (control mark) is set, and the next sector is searched for. If a deleted data mark is found and the SK bit is not set, the sector is read, bit 6 of ST2 (control mark) is set, and the read terminates with a normal termination. If a CRC error is detected in the data field, bit 5 is set to both ST1 and ST2 (CRC error) and an abnormal termination is indicated.

If no problems occur in the read command, the read continues from one sector to the next in logical order (not physical order) until either TC is set or an error occurs. If a disk has not been inserted into the disk drive, there are many opportunities for the controller to hang. It does this if it is waiting for a certain number of disk revolutions. If this occurs, the controller can be forced to abort the command by writing a byte to the data register.

An interrupt is generated when an execution phase of the read data command terminates. Following table shows the values that are read back in the result phase. If an error occurs, the result bytes indicate the sector being read when the error occurred.

Table 4-12 Result Phase Termination Values with No Error Table

Last	ID Information at Result Phase					
MT	**HD**	**Sector**	**Track**	**Head**	**Sector**	**B/S**
0	0	< EOT	NC	NC	S + 1	NC
0	0	= EOT	T + 1	NC	1	NC
0	1	< EOT	NC	NC	S + 1	NC
0	1	= EOT	T + 1	NC	1	NC
1	0	< EOT	NC	NC	S + 1	NC
1	0	= EOT	NC	1	1	NC
1	1	< EOT	NC	NC	S + 1	NC
1	1	= EOT	T + 1	0	1	NC

EOT = End of track sector number from command phase NC = No change in value
S = Sector number last operated on by controller T = Track number programmed in command phase

Read-Deleted-Data
This command is the same as the read-data command except for how it handles a deleted data mark. If a deleted data mark is read, the sector is read normally. If a regular data mark is found and the SK bit is set, the sector is not read, bit 6 of ST2 (control mark) is set, and the next sector is searched for. If a regular data mark is found and the SK bit is not set, the sector is read, bit 6 of ST2 (control mark) is set, and the read terminates with a normal termination.

Write-Data
The write-data command is very similar to the read-data command except that data is transferred from the CPU to the disk rather than the other way around. If the controller detects the write-protect signal, bit 1 of ST1 (not writable) is set and an abnormal termination is indicated.

Write-Deleted-Data
This command is the same as the write-data command except that a deleted-data mark is written at the beginning of the data field instead of the normal data mark.

Read a Track
This command is similar to the read-data command except for the following: the controller starts at the index hole and reads the sectors in their physical order, not their logical order.
Even though the controller reads sectors in their physical order, it still compares the header ID bytes with the data programmed in the command phase. The exception to this is the sector number. Internally, this is set to one, then incremented for each successive sector read. Whether or not the programmed address field matches that read from the disk, the sectors are still read in their physical order. If a header ID comparison fails, bit 2 of ST1 (No data) is set, but the operation continues. If there is a CRC error in the address or data field, the read also continues. The command terminates when it has read the number of sectors programmed in the EOT parameter.

Read ID

This command causes the controller to read the first address field it finds. The result phase contains the header bytes that are read. There is no data transfer during the execution phase of this command. An interrupt is generated when the execution phase is completed.

Format-a-Track

This command formats one track on the disk. After the index hole is detected, data patterns are written on the disk including all gaps, address marks, address fields, and data fields. The exact details of the number of bytes for each field is controlled by the parameters given in the format-a-track command, The data field consists of the fill-byte specified in the command, repeated to fill the entire sector. To allow for floppy formatting, the CPU must supply the four address field bytes (track, head, sector, number of bytes) for each sector formatted during the execution phase. In other words, as the controller formats each sector, it requests four bytes through either DMA requests or interrupts. This allows for non-sequential sector interleaving. Following tables show some typical values for the programmable gap size.

The format command terminates when the index hole is detected a second time, at which point an interrupt is generated. Only the first three status bytes in the result phase are significant.

Table 4-13 Gap Length for Various Sector Sizes and Disk Types Table

Mode	Sector Size (Dec)	Sector Code (Dec)	EOT (Hex)	Sector Gap (Hex)	Format* Gap (Hex)
8-inch Drives (360 RPM, 500 kb/s)					
FM	128	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM	256	01	0F	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5.25-inch Drives (300 RPM, 250 kb/s)					
FM	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3.5-inch Drives (300 RPM, 250 kb/s)					
FM	128	00	0F	07	1B
	256	01	09	0E	2A
	512	02	05	1B	3A
MFM	256	01	0F	0E	36
	512	02	09	1B	54
	1024	03	05	35	74

Table 4-14 Format Table for PC-Compatible Diskette Media Table

Media Type	Sector Size (Dec)	Sector Code (Hex)	EOT (Hex)	Sector Gap (Hex)	Format* Gap (Hex)
360 K	512	02	09	2A	50
1.2 M	512	02	0F	1B	54
720 M	512	02	09	1B	50
1.44 M	512	02	12	1B	6C
2.88 M	512	02	24	1b	54

* Format gap is the gap length used only for the format command.

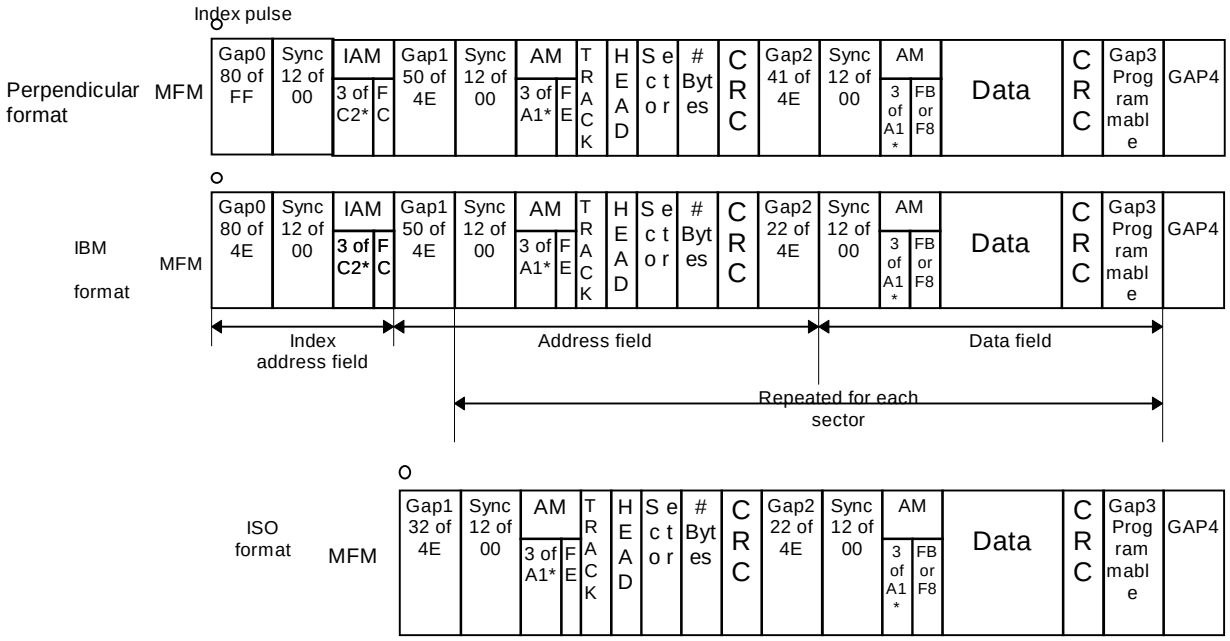

Figure 4-1 IBM, Perpendicular, and ISO Formats Supported by the Format Command

Scan Commands

The scan commands allow data read from the disk to be compared against data sent from the CPU. There are three scan commands to choose from:

Scan equal	Disk data = CPU data
Scan less than or equal	Disk data ≤ CPU data
Scan greater than or equal	Disk data ≥ CPU data

Each sector is interpreted with the most significant byte first. If the wildcard mode is enabled from the mode command, an FFh from either the disk or CPU is used as a "don't care" byte that always matches equal. If each sector is read, the desired condition has not been met, and the next sector is read. The next sector is defined as the current sector number plus the sector step-size specified.

The scan command continues until the scan condition has been met, or the end of track sector number has been reached, or if TC is asserted. If the SK bit is set, sectors with deleted data marks are ignored. If all sectors read are skipped, the command terminates with D3 of ST2 set (scan equal hit). Table 4-15 shows the result phase of the command.

Table 4-15 Scan Command Termination Values

Status Register Command	D2	D3	Conditions
Scan equal	0	1	Disk = CPU
	1	0	Disk <> CPU
Scan low	0	1	Disk = CPU
or equal	0	0	Disk < CPU
	1	0	Disk > CPU
Scan high	0	1	Disk = CPU
or equal	0	0	Disk < CPU
	1	0	Disk > CPU

Seek

There are two ways to move the disk drive head to the desired track number. The first method is to enable the implied seek mode. This way, each individual read or write command automatically moves the head to the track specified in the command.

The second method is by using the seek command. During the execution phase of the seek command, the track number to seek for is compared with the present track number, and a step pulse is produced to move the head one track closer to the desired track number. This is repeated at the rate specified by the specify command until the head reaches the correct track. At this point, an interrupt is generated and a sense-interrupt command is required to clear the interrupt.

During the execution phase of the seek command, the only indication via software that a seek command is in progress is bits 0~3 (drive busy) of the main status register. Bit 4 of the main status register (command in progress) is not set. While the internal micro-engine is capable of multiple seeks on two or more drives at the same time since the drives are selected via the drive-control register in software, software should ensure that only one drive performs the seek command at one time. No other command except the sense-interrupt command is issued while a seek command is in progress.

Relative Seek

The Relative Seek command steps the selected drive in or out a given number of steps. This command will step the read/write head an incremental number of tracks from the current track number, contrasting to step it to the desired track number as Seek command. The Relative Seek parameters are defined as follows:

DIR: Read/Write Head Step Direction Control
0=Step Head Out, 1=Step Head In

RTN: Relative Track Number. This value will determine how many incremental tracks to step the head in or out from the current track number.

Recalibrate

The recalibrate command is very similar to the seek command. It is used to step a drive head out to track zero. Step pulses are produced until the track zero signal from the drive becomes true. If the track zero signal does not go true before 80 step pulses are issued, an error is generated.

Recalibrations on more than one drive at a time should not be issued for the same reason as explained in the seek command. No other command except the sense-interrupt command should be issued while a recalibrate command is in progress.

Sense-Interrupt Status

An interrupt is generated by the controller when any of the following conditions occur:

1. Upon entering the result phase of :
   a. Read-data command
   b. Read-deleted-data command
   c. Write-data command
   d. Write-deleted-data command
   e. Read-a-track command
   f. Read-ID command
   g. Format command
   h. Scan commands

2. During data transfers in the execution phase while in the non-DMA mode

3. Internal ready signal changes state (only occurs immediately after a hardware or software reset).

4. Seek or recalibrate command termination

An interrupt generated for reasons 1 and 2 above occurs during normal command operations and are easily recognized by the CPU. During an execution phase in non-DMA mode, bit 5 (execution mode) in the MSR is set to 1. Upon entering result phase, this bit is set to 0.

Reasons 1 and 2 do not require the sense interrupt status command. The interrupt is cleared by reading or writing information to the data register. Interrupts caused by reasons 3 and 4 are identified with the aid of the sense interrupt status command. This command resets the interrupt when the command byte is written.

Following table shows how to identify the cause of the interrupt by using bits 5, 6 and 7 of ST0.

Issuing a sense-interrupt status command without an interrupt pending is treated as an invalid command. If the extended track range mode is enabled, a third byte should be read in the result phase which indicates the four most significant bits of the present track number. Otherwise, only two bytes should be read.

Specify

The specify command sets the initial values for each of the three internal timers. Table below shows the timer programming values.

The head-load and head-unload timers are artifacts of the UPD765A. These timers determine the delay from loading the head until a read or write command is started, and unloading the head sometime after the command was completed.

The step-rate time defines the time interval between adjacent step pulses during a seek, implied-seek, or recalibrate command. The times stated in Table 4-28 are affected by the data rate. These values are for 500 kb/s MFM (250 Kb/s FM) and 1 Mb/s MFM (500 Kb/s FM). For 300 kb/s MFM data rate (150 Kb/s FM), these values, multiply by 1.6667, and for 250 Kb/s MFM (125 Kb/s FM) double these values.

The choice of DMA or non-DMA operation is made by the non-DMA bit. When this bit is 1, the non-DMA mode is selected, and when this bit is 0, DMA mode is selected. This command does not generate an interrupt.

Table 4-16 Status Register 0 Termination Codes

Interrupt Code D7	D6	D5	Seek End Cause
1	1	0	Internal ready went true
0	0	1	Normal seek termination
0	1	1	Abnormal seek termination

Table 4-17 Step, Head, Load and Unload Timer Definitions (500 kb/s MFM)

Timer	Mode 1 Value	Range	Mode 2 Value	Range	Unit
Step Rate	(16 - N)	1~16	(16 - N)	1~16	ms
Head Unload	N x 16	0~240	N x 512	0~7680	ms
Head Load	N x 2	0~254	N x 32	0~4064	ms

Sense Drive Status
This two-byte command obtains the status of a disk drive. Status register 3 is returned in the result phase and contains the drive status. This command does not generate an interrupt.

Verify
The VERIFY command is used to verify the data stored on a disk. This command acts exactly like a READ DATA command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previouly stored value.

Version
The Version command can be used to determine the floppy controller being used. The result phase uniquely identifies the floppy controller version. The FDC returns a value of 90h in order to be compatible with the 82077. For older version compatible with NEC765 controller a value of 80h (invalid command) will return.

Dumpreg
The DUMPREG command is designed to support system run-time diagnostics and application software developmennt and debug. The command returns important information regarding the status of many of the programmed field in the FDC. This can be used to verify the values initialized in the FDC.

Configure
The Configure command controls some operation modes of the controller. It should be issued during the initialization of the FDC after power up. These bits are set to their default values after a hardware reset.
EIS: Enable implied seek. When EIS=1, the FDC will perform a SEEK operation before executing a read/write command. The default value is 0 (no implied seek).
EFIFO: Enable FIFO. When EFIFO=1, the FIFO is disabled (NEC765A compatible mode). This means data is transferred on a byte by byte basis. The default value is 1 (FIFO disable).
POLL: Disable Plooing. When POLL=1, polling of the drives is disabled. POLL defaults to 0 (polling enable). When enabled, a single interrupt is generated after reset.

FIFOTHR: The FIFO threshold in the execution phase of a read/write command. This is programmable from 1 to 16 bytes.FIFOTHR defaults to 00. A 00h selects one byte and 0Fh selects 16 bytes.
PRETRK: Precompensation start track number.
Programmable from track 0 to 255. PRETRK defaults to track 0. A 00h selects track 0 and a FFh selects track 255.

Powerdown Mode

The Powerdown mode command allows the automatic power management. The use of the command can extend the battery life in portable PC applications. To enable auto powerdown the command may be issued during the BIOS power on self test (POST).
DLY: Minimum powerup timer. This bit is active only if APD bit is enabled. Set this bit to 0 assigns a 10msec timer, and to 1 assigns a 0.5sec timer. The timer will be re-initialized after a command execution is finished (idle state) and start to countdown. When the timer is expired, the FDC will enter the powerdown state automatically.
APD: Enable auto powerdown. When set to 1, the auto powerdown is enabled.

Lock

The Lock command allows the user full control of the FIFO parameters after a software reset. If the LOCK bit is set to 1, then the EFIFO, FIFOTHR and PRETRK bits in the Configure command are not affected by a software reset.
After the command byte is written, the result byte must be read before continuing to the next command.

Invalid

If an invalid command (illegal Opcode byte in the command phase) is received by the controller, the controller responds with ST0 in the Result Phase. The controller does not generate an interrupt during this condition. The system reads an 80h from ST0 indicating an invalid command was received.

Perpendicular Mode

The Perpendicular Mode command is designed to support the Perpendicular Recording disk drives (4Mbytes unformatted capacity). The Perpendicular Mode command configures each of the four logical drives as a perpendicular or conventional disk drive. Configuration of the four logical disk drives is done via the D3-D0 bits, or with the GAP and WG control bits. This command should be issued during the initialization of the floppy controller.
A 0 written to Dn sets drive n to conventional mode, and a 1 sets drive n to perpendicular mode. Also, the OW bit offers additional control. When OW=1, changing the values of D3-D0 is enabled. When OW=0, the internal values of D3-D0 are unaffected, regardless of what is written to D3-D0.
The function of the Dn bits must also be qualified by setting both WG and GAP to 0. If WG and GAP are not set to 00, they overrides whatever is programmed in the Dn bits. Table below indicates the operation of the FDC based on the values of GAP and WG. D3-D0 are unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset. A hardware reset resets all the bits to zero.

Table 4-18 Effects of WG and GAP bits Table

GAP	WG	Mode	GAP2 Length during Format	Portion of GAP2 re-written by Write Data Command
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1Mbps)	41 Bytes	38 Bytes

4.4.3.5 Parallel Port Mode FDC

In this mode, the floppy disk control signals are available on the parallel port pins. When this mode is selected, the parallel port is not available. There are four modes of operation. These modes can be selected in index 0xF1 of FDC configuration space. The FDC signals are multiplexed onto the Parallel port pins as shown in table below.

0xF1[1:0]		Parallel port function
0	0	printer
0	1	printer
1	0	FDC(drive 0 or 1)
1	0	FDC(drive 1)

Conn Pin no.	SPP mode	Type	FDC mode	Type
1	STROBJ	I/O	DRV0	O
2	PD[0]	I/O	INDEXJ	I
3	PD[1]	I/O	TRK0J	I
4	PD[2]	I/O	WPJ	I
5	PD[3	I/O	RDATAJ	I
6	PD[4]	I/O	DSKCHGJ	I
7	PD[5]	I/O		
8	PD[6]	I/O	MOT0	O
9	PD[7	I/O		
10	ACKJ	I	DRV1	O
11	BUSY	I	MOT1	O
12	PE	I	WDATAJ	O
13	SLCT	I	WGATEJ	O
14	AUTOFDJ	I/O	DENSEL	O
15	ERRORJ	I	HDSELJ	O
16	INITJ	I/O	DIRJ	O
17	SLCTINJ	I/O	STEPJ	O

4.4.4 Serial Port Registers

Each of the serial ports function as data input/output interface in a microcomputer system. The system software determines the functional configuration of the UARTs via a tri-state 8-bit bi-directional data bus.

The UARTs are completely independent and perform serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of any of the UARTs at any time during the functional operation. Status information reported includes the type and condition of the transfer operations performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The UARTs have programmable baud rate generator capable of dividing the timing reference clock input by divisors of 1 to (2^{16} - 1), and producing a 16 X clock for driving the internal transmitter logic. Provisions are also included to use this 16 X clock to drive the receiver logic. The UARTs have complete modem-control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle communications link.

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Following table 4-19 lists the register addresses A2 ~ A0 (AEN is equal to zero). DLAB is the divisor latch access bit.

Table 4-19 Serial Port Registers Table

Register Address	Access (AEN=0)	Abbreviation	Register Name	Access
Base +	DLAB			
0h	0	THR	Transmit Holding Register	W
0h	0	RBR	Receiver Buffer Register	R
0h	1	DLL	Divisor Latch LSB	R/W
1h	1	DLM	Divisor Latch MSB	R/W
1h	0	IER	Interrupt Enable Register	R/W
2h	-	IIR	Interrupt Identification Register	R
2h	-	FCR	FIFO Control Register	W
3h	-	LCR	Line Control Register	R/W
4h	-	MCR	Modem Control Register	R/W
5h	-	LSR	Line Status Register	R
6h	-	MSR	Modem Status Register	R
7h	-	SCR	Scratch Pad Register	R/W

Table 4-20 Register Summary for each UART Channel Table

			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	Receiver Buffer Register (Read only)	RBR	Data bit 0 (Note 1)	Data bit 1	Data bit 2	Data bit 3	Data bit 4	Data bit 5	Data bit 6	Data bit 7
0	Transmitter Holding Register (Write only)	THR	Data bit 0	Data bit 1	Data bit 2	Data bit 3	Data bit 4	Data bit 5	Data bit 6	Data bit 7
1	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Modem Status Interrupt (EMSI)	0	0	0	0
2	Interrupt Ident. Register (Read only)	IIR	'0' if interrupt pending	Interrupt ID bit	Interrupt ID bit	0	0	0	FIFO enable	FIFO enable
2	FIFO control register (write only)	FCR	FIFO enable	RCVR FIFO Reset	Xmit FIFO reset	reserved	reserved	Reserved	RCVR Trigger (LSB)	RCVR Trigger (MSB)
3	Line control register	LCR	Word Length Select bit 0 (WLS0)	Word Length Select bit 1 (WLS1)	Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
4	Modem control register	MCR	Data Terminal ready (DTR)	Request to send (RTS)	Out 1 (Note 2)	IRQ Enable (Note 2)	Loop	0	0	0
5	Line status register	LSR	Data ready (DR)	Overrun error (OE)	Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register Empty (THRE)	Transmitter Empty (TEMT)	Error in RCVR FIFO
6	Modem status register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)	Trailing Edge ring indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
7	Scratch register (Note 4)	SCR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0 DLAB=1	Divisor latch (LS)	DLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 DLAB=1	Divisor latch (MS)	DLM	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 1. Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
2. This bit no longer has a pin associated with it.

Line Control Register (LCR)

The system programmer uses this read/write register to specify the format of the asynchronous data communications exchange and set the divisor latch access bit.

LCR Registers

Bit	Description
7	Divisor latch access bit (DLAB). 1 = To access divisor latches of the baud generator. 0 = To access other registers.
6	Break control bit. This bit causes a break condition to be transmitted to the receiving UART. 1 = Serial output (SOUT) is forced to the spacing logic (logic 0) 0 = Break is disabled This bit acts only on SOUT and has no effect on transmitter logic. This enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters are transmitted because of the break: 1. Load all 0s, pad character in response to THRE. 2. Set break after the next THRE. 3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored. During the break, the transmitter can be used as a character timer to accurately establish the break duration.
5	Stick parity bit. When parity is enabled, it is used in conjunction with bit 4 to select, mark or space parity. 1 = Enable stick parity 0 = Disable stick parity
4	Parity select bit. Selects either an odd or even number of 1's to be transmitted/checked in the data word bit and parity bit. 0 = Odd number of 1's (parity bit is a logic 1, mark parity) 1 = Even number of 1's (parity bit is a logic 0, space parity)
3	Parity enable bit. The parity bit is used to produce an even or odd number of 1's when the data bits and the parity bit are summed. A parity bit is generated (transmit data) or checked (received data) between the last data bit and the stop bit of the serial data. 0 = Parity bit is not generated/checked 1 = Parity bit is generated/checked
2	Specifies the number of stop bits transmitted with each serial character. The receiver checks the first stop bit only, regardless of the number of stop bits selected. 0 = 1 stop bit 1 = 1.5 stop bits, when a 5-bit data length is selected 1 = 2 stop bits, when 6-, 7-, or 8-bit data length is selected
0-1	Specify the number of data bits (data length) in each transmitted or received serial character. The following are the bit values: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits

Programmable Baud Generator

The UART contains two independently programmable baud generators. The 24-MHz crystal oscillator frequency input is divided by 13, resulting in a frequency of 1.8462-MHz. This is sent to each baud generator and divided by the divisor for the associated UART. The output frequency of the baud generator is 16 X the baud rate, [divisor # = (frequency input) / (baud rate x 16)]. The output of each baud generator drives the transmitter and receiver sections of the associated serial channel. Two 8-bit latches per channel store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud generator. Upon loading either of the divisor latches, a 16-bit baud counter is loaded.

Table next page provides decimal divisors to use with crystal frequencies of 24-MHz. The oscillator input to the chip should always be 24-MHz to ensure that the FDC timing is accurate and that the UART divisors are compatible with existing software. Using a divisor of zero is not recommended.

Line Status Register (LSR)

This register provides status information to the CPU concerning the data transfer. LSR is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

Line Status Register Function Definition

Bit	Description
7	In FIFO, LSR7 is set when there is at least one parity error, framing error or break indication in the FIFO LSR7 is cleared when the CPU read the LSR, if there are no subsequent errors in the FIFO.
6	This bit is the transmitter empty (TEMT) indicator. It is set to 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to 0 whenever either the THR or TSR contains a data character.
5	**Transmitter Holding Register Empty (THRE) indicator**. It indicates that the UART is ready to accept a new character for transmission. It also causes the UART to issue an interrupt to the CPU when the THRE interrupt enable is set high. It is set to 1 when a character is transferred from the THRE into TSR. It is reset to 0 whenever the CPU loads the THRE.
4	**Break interrupt (BI) indicator**. It is set to 1 when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (that is, the total time of start bit + data bits + parity +stop bits). It is reset whenever the CPU reads the contents of the LSR. Restarting after a break is received requires the SIN pin to be logical 1 for at least 1/2-bit time.
3	**Framing error (FE) indicator**. This bit indicates that the received character did not have a valid stop bit. It is set to 1 whenever the stop bit following the last data bit or parity bit is a logic 0 (spacing level). The FE indicator is reset whenever the CPU reads the contents of LSR. The UART tries to resynchronize after a framing error. To do this, it assumes that the FE was due at the next start bit, so it samples this start bit twice and then takes in the data.
2	**Parity error (PE) indicator**. This bit indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. It is set to 1 upon detection of a parity error and reset to 0 whenever the CPU reads the contents of the LSR.
1	**Overrun error (OE) indicator**. It indicates that data in the RBR was not read by the CPU before the next data was transferred into the RBR, thereby destroying the previous data. It is set to 1 upon detection of an overrun condition and reset to 0 whenever the CPU reads the contents of the LSR.
0	**Receive data ready (DR) indicator**. It is set to 1 whenever a complete incoming character has been received and transferred into the RBR. It is reset to 0 by reading the data in the RBR.

Table 4-21 Baud rates using 1.8462 MHz Clock (24 MHz/13)

Desired baud rate	Decimal Divisor for 16X Clock	Percent Error	High speed mode bit in Index F0h
50	2304	0.1%	X
75	1536	0.2%	X
110	1047	0.2%	X
134.5	857	0.4%	X
150	768	0.2%	X
300	384	0.2%	X
600	192	0.2%	X
1200	96	0.2%	X
1800	64	0.2%	X
2000	58	0.5%	X
2400	48	0.2%	X
3600	32	0.2%	X
4800	24	0.2%	X
7200	16	0.2%	X
9600	12	0.2%	X
19200	6	0.2%	X
38400	3	0.2%	X
57600	2	0.2%	X
115200	1	0.2%	X
230400	32770	0.2%	1
460800	32769	0.2%	1

Interrupt Identification Register (IIR)

This register keeps a record of the four interrupts prioritized by the UART to reduce software overhead during data transfers. The four levels of interrupt conditions in order of priority are: receiver-line-status, received-data-ready, transmitter-holding-register-empty, and modem-status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete.

Interrupt Identification Register

Bit	Description
7~6	These two bits are set when the FIFO control register bit 0 equals 1.
5~4	Always '0'.
3	In non-FIFO mode, this bit is a logic 0. In FIFO mode, this bit is set along with bit 2 when a timeout interrupt is pending.
2~1	Identifies the highest interrupt pending.
0	Used in an interrupt environment to indicate whether an interrupt condition is pending. If yes, the IIR contents may be used as a pointer to the appropriate interrupt service routine. 0 = Interrupt pending 1 = No interrupt pending

Table 4-22 Interrupt Control Table

FIFO mode only	Interrupt ID. register	Interrupt Set and Reset Functions			
D3	D2-D1-D0	**Priority level**	**Interrupt type**	**Interrupt source**	**Interrupt Reset control**
0	0- 0- 1	-	None	None	-
0	1- 1- 0	highest	Receiver line status	Overrun error, Parity error, Framing error Break interrupt	Reading the line status register
0	1- 0- 0	second	Received data available	Received data available	Read receiver buffer or the FIFO drops below the trigger level
1	1- 0- 0	second	Character timeout Indication	No characters have been removed from or input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time.	Reading the Receiver Buffer Register
0	0- 1- 0	third	Transmitter holding register empty	Transmitter Holding Register Empty	Reading the IIR Register or writing the transmitter holding register
0	0- 0- 0	fourth	MODEM status	Clear to send or data set ready or Ring indicator or Data Carrier Detect	Reading the Modem status register

Interrupt Enable Register (IER)

This register enables the four types of UART interrupts. Each interrupt can individually activate the UART's IRQ output signals. Resetting bits 0 ~ 3 of the IER disables the interrupt system. Similarly, setting bits of this register to 1 enables the selected interrupts. Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the interrupt output signal. All other system functions operate in their normal manner, including the setting of the line status and modem status registers.

Interrupt Enable Register Table

Bit	Description
7-4	Always 0
3	Enables the modem-status interrupt
2	Enables the receiver-line-status interrupt
1	Enables the THRE interrupt
0	Enables the received-data-available interrupt

FIFO Control Register

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level.

Bit 0: Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed.

Bit 1: Writing a 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3,4, 5: FCR3 to FCR5 are reserved for future use.

Bit 6, 7: FCR6 and FCR7 are used to set the trigger level for the RCVR FIFO interrupt.

7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Modem Control Register (MCR)

This register controls the interface with the modem or data set (or a peripheral emulating a modem).

Modem Control Register

Bit	Description
7~5	Set to logic 0.
4	This bit provides a local loopback feature for the UART diagnostic testing. When set to 1, the following occurs: the transmitter serial output (SOUT) is set to the marking (1) state; the receiver serial input (SIN) is disconnected; the output of the transmitter shift register is looped back into the receiver shift register input; the four modem control inputs (DSRJ, CTSJ, RIJ, and DCDJ) are disconnected; and four Modem control outputs (DTRJ, RTSJ, OUT1J, IRQ) are internally connected to the four Modem control inputs. The modem control output pins are forced to their high (inactive) states. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and-receive data paths of the serial port. In the diagnostic mode, the receiver and transmitter interrupts status are fully operational. Their sources are external to the part. The Modem Control interrupts are also operational, but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four Modem control inputs. The interrupts are still controlled by the Interrupt Enable Register.
3	This bit enables the interrupt when set. In local loopback mode, this bit controls bit 7 of the MSR.
2	This is the OUT1 bit. It does not have an output pin associated with it. It can be written to and read by the CPU. In local loopback mode, this bit controls bit 6 of the MSR.
1	Controls the RTSJ output. In local loopback mode, this bit controls bit 4 of the MSR.
0	Controls the DTRJ output. In local loopback mode, this bit controls bit 5 of the MSR. 1 = DTRJ output is forced to 0 0 = DTRJ output is forced to 1

Modem Status Register (MSR)

This register gives the current state of the control lines from the modem to the CPU. The four LSB bits are set to 1 whenever a control input from the modem changes state, and set to 0 when CPU reads the MSR.

Modem Status Register

Bit	Description
7	Complement of the DCDJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to IRQ enable in the MCR.
6	Complement of the RIJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to OUT1 in the MCR.
5	Complement of the DSRJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to DTR in the MCR.
4	Complement of the CTSJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to RTS in the MCR.
3	Delta data carrier detect (DDCD) indicator indicates that the DCDJ input to the chip has changed state.Whenever bit 0, 1, 2 or 3 is set to 1, a modem status interrupt is generated.
2	Trailing edge of ring indicator (TERI) detector indicates that the RIJ input of the chip has changed from a low to high state.
1	Delta data set ready (DDSR) indicator indicates that the DSRJ input to the chip has changed its state since the last time it was read by the CPU.
0	Delta clear to send (DCTS) indicator indicates that CTSJ input to the chip has changed its state since the last time it was read by CPU.

Scratchpad Register (SCR)

The 8-bit read/write register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Infrared Interface

The M1543C provide pins with infrared communications capabilities. It operates in the following modes:

- Sharp-IR
- IrDA SIR
- IrDA MIR
- IrDA FIR

Sharp-IR Mode

This mode supports bidirectional data communication with a remote device using infrared radiation as the transmission medium. Sharp-IR uses Amplitude Shift Key (ASK) and allows serial communication at baud rates up to 38.4K Baud. The format of the serial data is similar to the UART data format, a zero value start bit, followed by up to 8 data bits, an optional parity bit, and ending with at least one stop bit with a binary value of one. A zero is signalled by sending a 500KHz continuous pulse train of infrared radiation. A one is signalled by the absence of any infrared signal.
The device operation in Sharp-IR mode is similar to the operation in UART. The main difference is that the data transfer is normally performed in half duplex fashion, and the modem control and status signals are not used. Selection of this mode is controlled by the IR mode bits in the UART's configuration space. Only UART2 can be programmed in this mode. The transfer signals will rout to IRRX and IRTX.

IrDA SIR Mode

This is an operation mode similar to Sharp-IR. The IrDA 1.0 SIR allows serial communication at baud rates up to 115.2K Baud. The data format is the same as Sharp-IR mode except no parity bit is needed. A zero is signalled by sending a single infrared pulse. A one is signalled by not sending any pulse. The width of each pulse is 3/16ths of a single bit time.
The device operation in IrDA 1.0 SIR mode is similar to the operation in UART. The main difference is that the data transfer is normally performed in half duplex fashion, and the modem control and status signals are not used. Selection of this mode is controlled by the IR mode bits in the UART's configuration space. All of the three UARTs can be programmed in this mode. The transfer signals will rout to SIN1/SIN2/IRRX and SOUT1/SOUT2/IRTX.

IrDA MIR and FIR

The M1543C supports both IrDA 1.1 MIR and FIR modes, with data rates of 0.576Mbps, 1.152Mbps and 4.0Mbps respectively. Details on the frame format, encoding schemes, CRC sequences, etc. are provided in the appropriate IrDA documents. The MIR and FIR communications are available on UART2 only and signals are routed to IRTX, IRRX, and IRRXH only.

FIR Register Set

Before accessing the FIR registers, the UART2 and FIR enable bits (bit 0 and bit 7) of index 0x30 in the UART2's configuration space must set to 1 first. After this, the user can switch between the conventional UART registers and FIR registers space by the procedure described below.

To change from the conventional space to FIR space, the bits 7-5 of the MCR (Modem Control Register) are written to 001, 011, and 100 consecutively. And all of the four banks of FIR registers are available by switching between the bank select bits in the Master Control register. Write one to bit 7 of the Master Control register will switch back to conventional UART register space immediately.

Table 4-23 FIR Register Bank Summary

Bank	Alias	Type	Register Name	Def.
X	Base+7	R/W	FIR Master Control	00
0	Base+0	R/W	FIR DATA Register	00
0	Base+1	R/W	FIR Interrupt Enable	00
0	Base+2	RO	FIR Interrupt Identification	00
0	Base+3	R/W	FIR Line Control A	00
0	Base+4	R/W	FIR Line Control B	07
0	Base+5	R/W	FIR Line Status	00
0*	Base+6	R/W	FIR Bus Status	00
1	Base+0	R/W	FIR Configuration	00
1	Base+1	R/W	FIR FIFO Threshold	01
1 *	Base+2	R/W	ISA DMA Threshold	00
1 *	Base+3	R/O	FIFO Flag Register	00
1 *	Base+3	W/O	Timer Interrupt Interval Register	11
1 *	Base+4	R/O	FIFO Read Address	00
1 *	Base+5	R/O	FIFO Write Address	00
1 *	Base+6	WO	Test	00
2	Base+0	R/W	IrDA Control	00
2	Base+1	R/W	BOF Count	00
2	Base+2	R/W	Brick Wall Count	00
2	Base+3	R/W	TX DATA Size (high)	00
2	Base+4	R/W	TX DATA Size (low)	00
2	Base+5	R/O	RX DATA Size (high)	00
2	Base+6	R/O	RX DATA Size (low)	00
3	Base+0	R/O	FIR ID version	00
3	Base+1	R/W	FIR module control	N/A
3	Base+2	R/O	FIR higher I/O base address	N/A
3	Base+3	R/O	FIR lower I/O base address	N/A
3	Base+4	R/O	FIR IRQ channel	N/A
3	Base+5	R/O	FIR DMA channel	N/A

Master Control Register

This register is a read/write register and its default value is 00h. It is accessible regardless which bank is on now. The definition of this register is described below.

Bit	Description
7	Register Space Switch. Write a 1 to this bit will switch the FIR register space back to conventional UART space.
6	Master Reset. Setting the Master Reset bit resets all registers in FIR. The Master Reset bit will return to zero following the reset operation.
5	Master Interrupt Enable. Setting the Master Interrupt Enable bit to zero will disable all FIR interrupts regardless of the state of their individual enables.
4	Error Reset. Writing a one to Error Reset bit will reset the FIR Line Status Register and reset the Message Count bits to zero. The Error Reset bit will return to zero following the reset operation.
3-2	Reserved
1-0	FIR Register Bank Select 0 0 : Bank 0 0 1 : Bank 1 1 0 : Bank 2 1 1 : Bank 3

Bank 0 Registers

Alias 0, FIR Data Register (R/W)

The Data register is the FIR FIFO access port. The FIR FIFO is written when transmitting and read when receiving. Host read is blocked when the FIFO is empty and host write is blocked when the FIFO is full.

Alias 1, FIR Interrupt Enable Register (R/W)

Bit	Description
7	Active Frame Interrupt Enable
6	End of Message Interrupt Enable
5	Timer Interrupt Enable
4	FIR FIFO Interrupt Enable
3-0	Reserved

Alias 2, FIR Interrupt Identification Register (Read only)

Bit	Description
7	Active Frame Interrupt. When this bit is one, an Active Frame has occurred. The interrupt request (IRQ) line would be active when set the Active Frame Interrupt Enable bit to one and set the Master Interrupt Enable bit, and this bit is one.
6	End of Message Interrupt. When this bit is one, an End of Message has occurred. The EOM indicates that an IrDA FIR frame has transferred completely or abort. Reading the FIR Interrupt Identification Register will reset this bit. The interrupt request (IRQ) line would be active when set the EOM Interrupt Enable bit to one and set the Master Interrupt Enable bit, and this bit is one.
5	Timer Interrupt. When this bit is one, timer interrupt has occurred. The timer interval can be programmed. There are four intervals that can be selected, 500 us, 1ms, 2ms, 4ms.
4	FIR FIFO Interrupt. When this bit is one, a FIFO interrupt source has occurred. The FIR FIFO interrupt indicates that the FIR FIFO Interrupt enable is active and either a TxServReq or RxServReq has occurred. The FIR FIFO Interrupt bit is cleared when the interrupt source is inactive. That is, this bit would not be cleared by reading FIR Interrupt Identification Register. The interrupt request (IRQ) line would be active when set the Master Interrupt Enable bit, and this bit is one.
3-0	Reserved

Alias 3, FIR Line Control Register A (R/W)

Bit	Description
7	FIFO Reset When setting this bit to one, the FIFO Full and Not Empty flags of the 32-byte FIR FIFO would be cleared. The FIFO Reset bit will return to zero automatically.
6-3	Reserved
2	Abort. When setting this bit to one, the current transmitting process will be terminated, the EOM flag is activated and the FIR FIFO is cleared. The Abort bit is reset by the End-of-Frame. The Abort is only used in transmit mode.
1	Data Done. The Data Done bit is used during transmitting to distinguish an end-of-valid-message-data condition (Data-Done-Bit=1) from a FIFO Underrun (Data-Done-Bit=0) that indicates incomplete message data. The Data Done bit is set by host in PIO mode. The Terminal Count automatically activates the Data Done bit in transmit DMA mode. The Data Done bit is automatically reset to zero at the end of a message only if the FIR FIFO is empty.
0	BWLF Set (Back to Back last frame set) This bit is set, the last frame will end automatically, if the FIFO is empty. Thus this bit must be set at the last frame in Back to Back transfer.

Alias 4, FIR Line Control Register B (R/W)

Bit	Description
7-6	FIR Mode **Bit 7 Bit 6 Mode Description** 0 0 Receive and Transmit both disable (default) 0 1 Transmit mode 1 0 Receive mode 1 1 Reserved Transmission is active whenever TC goes active, or the FIFO Threshold has been exceeded.
5	SIP Enable. When set the SIP Enable bit to one, an SIR Interaction Pulse will assert every 500ms if no transmitting or receiving has occurred.
4	Brick Wall. The Data Size Register can also be used when the Brick Wall bit is active to send back-to-back IrDA FIR frames when the DMA data block is larger than the IrDA message length. In this case, if the maximum number of data bytes according to the data size register have been transferred and the DMA terminal count or FIFO Empty flags have not been activated, the next message is brick walled to the previous message.
3-0	Message Count. The four Message Count bits controls hardware access to the Line Status Registers and are unaffected by the Status Register Address bits. The Message Count bits are incremented after active frame.

Alias 5, FIR Line Status Register (R/W)

There are eight FIR Line Status Registers. The bits 7-3 of each register is read-only and is accessed by programming the three FIR Line Status Address bits (bits 2-0). The status of all eight FIR Line Status registers are reset by Master reset, Power-on-reset, and Error reset. The current FIR Line Status register pointed by Message Count would be reset following a valid IrDA BOF sequence.

Bit	Description
7	FIFO Under/Overrun (Read only). In transmit mode, the FIFO Underrun bit gets set to one when the transmitter runs out of the FIFO and the Data Done bit is not active. In receive model, the FIFO Overrun gets set to one when the receiver tries to write a data to the FIFO when the FIFO is full.
6	Frame Error (Read only). The Frame Error bit gets set to one when IrDA errors are detected.
5	Size Error (Read only). The Size Error gets set to one whenever the receiver decrements the RX Data Size count to zero before the End-of-Frame, or whenever the Brick Wall bit is inactive and the transmitter decrements the TX Data Size count to zero before FIFO Empty goes active.
4	CRC Error (Read only). The CRC Error bit gets set to one when the Frame-Check-Sequence errors have occurred in this receive message frame.
3	Frame Abort (Read only) The Frame Abort bit gets set to one as ; 1) a forced abort, by setting the Abort bit of FIR Line Control Register A; 2) a FIFO underrun with the Data Done bit inactive during transmitting; 3) a FIFO overrun during receiving; 4) frame errors during receiving. Note: The Frame Abort bit will not go active during transmitting if the TX Data Size register decrements to zero when the last byte is read from the FIFO with the Data Done bit not set.
2-0	FIR Line Status Address (R/W) The Status Register Address bits control software read access to the eight FIR Line Status Registers at same I/O address(alias 5, bank 0). To access any one of the eight FIR Line Status Registers, first write the address of the appropriate register (0-7), then read the appropriate register contents.

Alias 6, FIR Bus Status Register (Read only)

Bit	Description
7	FIFO Not Empty When this bit is one, there is one or more data in the FIR FIFO.
6	FIFO Full When this bit is one, there is no room for loading data to FIFO.
5	End of message
4	SIP assert bit Reflection of the SIP signal.
3	Read Ready
2-0	Reserved

Bank 1 Registers

Alias 0, FIR Configuration Register (R/W)

Bit	Description
7-4, 2	Reserved
3	Timer enable. When this bit is set, timer begins to count.
1	DMA Burst Mode. When the DMA Burst Mode bit is one, DMA Burst (Demand) mode is selected. When the DMA Burst Mode bit is zero, DMA Single Byte mode is selected.
0	DMA Enable. When the DMA Enable bit is one, the DMA host interface is active.

Alias 1, FIR FIFO Threshold Register (R/W)

Bit	Description
7-5	Reserved
4-0	FIR FIFO Threshold Bits The FIR FIFO Threshold bits contain the programmable FIFO threshold count. The threshold is from 0 to 31 for the FIR FIFO. If the data in FIFO is larger than FIR FIFO threshold, the transfer starts in TX mode.

Alias 2, FIR DMA Threshold Register (R/W)

Bit	Description
7-5	Reserved
4-0	ISA DMA Threshold Bits ISA DMA transfer starts only if data in FIFO is larger than ISA DMA Threshold in RX mode or if data in FIFO is smaller than ISA DMA Threshold in TX mode. The threshold is from 0 to 32 for the FIR FIFO.

Alias 3, FIR Timer interrupt interval register(W/O)

Bit	Description
7-2	Reserved
1-0	Timer interrupt scale register “00” => 500us, “01” => 1ms, “10” => 2ms, “11” => 4ms

Alias 3, FIR FIFO Flag register (R/O)

Bit	Description
7-6	Reserved
5-0	FIFO Flag Bits. These bits record the data in FIFO.

Alias 4, FIR FIFO Read Address register (R/O)

Bit	Description
7-5	Reserved
4-0	FIFO Read address These bits are current FIFO read address.

Alias 5, FIR FIFO Write Address register (R/O)

Bit	Description
7-5,	Reserved
4-0	FIFO Flag Bits These bits are current FIFO write address.

Alias 6, Test register(WO)

Bit	Description
7-0	Reserved for test only

Bank 2 Registers

Alias 0, IrDA Control Register (R/W)

Bit	Description
7	1.152Mbps HDLC Select. This bit is used to select bit rate in FIR HDLC mode. When the 1.152 Select bit is one, the IrDA 1.152Mbps HDLC-type FIR data rate is selected. Otherwise, the IrDA 0.576Mbps HDLC_type FIR data rate is selected.
6	CRC Select. When the CRC Select bit is one, a hardware-generated CRC is appended to the transmitting frame between data field and STO flag, and a hardware CRC checking sequence is active during receiving frame.
5	HDLC select. When this bit asserts, HDLC mode select
4	Hp mode (read only) As the bit is 1, the FIR is connected in HP type transceiver module.
3	SD/MODE State. When the SD/MODE State bit is one, the signal IRRXH is set to one. When the SD/MODE State bit is zero, the signal IRRXH is set to zero. The combination of this signal and IRTX will determine the operation speed of the transceiver module (IBM or TEMIC).
2	FIR SIN Select. When the FIR SIN Select bit is zero, the input signal of the fast infrared data comes from IRRX pin . When the SIN Select bit is one, the input signal of the fast infrared data comes from IRRXH pin. When the M1543C is used with IBM(or TEMIC) transceiver module, IRRX is used as the infrared data input signal and SD/MODE will be used to control the speed of the module . When the M1543C is used with HP transceiver module, IRRX is used as the input signal of the serial infrared data and IRRXH is used as the input signal of the fast infrared data.
1-0	SOUT State. These bits control the serial output signal (IRTX). **Bit1 Bit0 SOUT signal state** 0 X Normal TX output signal 1 0 force to 0 1 1 force to 1

Alias 1, BOF Count Register (R/W)

The BOF Count register specifies the number of additional flags that is used in the BOF sequence of a frame, excluding brick wall frames. The BOF Count is 8-bit value. The BOF means the STA flags in IrDA FIR HDLC (1.152/0.576Mbps) mode or the PAs in IrDA FIR 4PPM (4Mbps) mode.

Alias 2, Brick Wall Count Register (R/W)

The Brick Wall Count register specifies the number of additional interframe padding flags used for brick wall messages. The Brick Wall Count is 8-bit value.

Alias 3, TX Data Size Register (high) (R/W)

Bit	Description
7-4	Reserved
3-0	TX Data Size High Byte

Alias 4, TX Data Size Register (low) (R/W)

Bit	Description
7-0	TX Data Size Low Byte. The TX Data Size count is 12-bit value. The TX Data Size registers specify the IrLAP-negotiated maximum number of payload data bytes per IrDA transmit message frame if the software CRC is selected, or the IrLAP-negotiated maximum number of payload data bytes minus the number of CRC bytes if hardware CRC is selected. The TX Data Size registers are used to 1) constrain the transmitter to a valid IrDA frame size, 2) simplify multi-frame windowing for transmit data blocks that are larger than the maximum packet size. If the TX Data Size registers are zero, the IrDA transmit message size is unlimited; i.e., the transmitter will operate until the FIR FIFO is empty.

Alias 5, RX Data Size Register (high) (R/W)

Bit	Description
7-4	Reserved
3-0	RX Data Size High Byte

Alias 6, RX Data Size Register (low) (R/W)

Bit	Description
7-0	RX Data Size Low Byte. The RX Data Size count is 12-bit value. The RX Data Size registers specify the IrLAP-negotiated maximum number of payload data bytes per IrDA receive message frame. The RX Data Size registers are used to check each IrDA FIR receive frame for valid size. If the RX Data Size register are zero, the IrDA receive message size is unlimited; i.e., a size error cannot occur because the receive frame size checking is disable.

Bank 3 Registers

Alias 0, FIR ID Version Register (R/O)

This register is used to distinguish the different versions of the FIR. The value is 00 in the M1543C.

Alias 1, FIR Module Control Register (R/W)

Bit	Description
7	IR module type. This bit will control the type of connected IR module. This bit is a mirror of bit 7 in index 0xF0h of logical device 5.
6	This bit will reflect the signal on pin IRRXH. This is used for the detection of IR module.
5-0	read as 0

Alias 2, FIR Higher I/O Base Address Register (R/O)

Bit	Description
7-0	Reflect the content of index 0x60h of the UART2.

Alias 3, FIR Lower I/O Base Address Register (R/O)

Bit	Description
7-3	Reflect the content of index 0x61h of the UART2.
2-0	Reserved.

Alias 4, FIR IRQ Channel Register (R/O)

Bit	Description
7-4	Reserved.
3-0	Reflect the content of index 0x70h of the UART2.

Alias 5, FIR DMA Channel Register (R/O)

Bit	Description
7-3	Reserved.
2-0	Reflect the content of index 0x74h of the UART2.

4.4.5 Keyboard Controller

The keyboard controller is a general purpose 8-bit microcontroller. It is software compatible to the industry standard keyboard controller 8042AH. The controller consists of 256 bytes of data memory and 2K bytes of read -only program memory (ROM). The ROM may be programmed, during manufacture, according to customer requirements.

Host System Interface

The keyboard controller is interfaced to the host system through a common system interface. The interface consists of SA15-0, AEN, SD7-0, IOWJ, IORJ, KIRQ and MIRQ for Keyboard and Mouse interrupts. The M1543C decodes the keyboard controller chip-select at 60h and 64h. Following table shows the register address decoding utilized by the keyboard controller system interface.

Table 4-24 Summary of Sytem Interface Operations Table

ISA Address	IOWJ	IORJ	Operation
0x60	0	1	Data Write Buffer
	1	0	Data Read Buffer
0x64	0	1	Command Write Buffer
	1	0	Read Status Register

Data Write Buffer

This is an 8 bit write only register. When written, the C/D status bit of the status register is cleared to zero and the IBF bit is set.

Data Read Buffer

This is an 8 bit read only register. The Keyboard controller will set the OBF to 1 when the data is available. When read by the host, OBF bit will reset to 0.

Command Write Buffer

This is an 8 bit write only register. When written, the C/D status bit of the status register is set to one and the IBF bit is set.

Read Status Register

This is an 8 bit read only register and holds status information related to the system interface.

Hardware Emulated Hotkey

The M1543C also provides a hardware emulation hotkey algorithm for the convenience of waking up the system by pressing the keyboard. There are three programmable keys for different combination. Each key can be programmed as valid or not valid. One of the keys must be programmed as the last pressed key. When the system is down, the hardware will compare the make code received from the keyboard and generate a low pulse to turn on the power, like the power-on button on the front panel.

4.4.6 Parallel Port

Parallel Port Interface

The parallel interface is designed to provide all of the signals and registers needed to communicate using the IEEE1284 standard. It includes ISA-compatible and PS/2-comaptibe modes, EPP mode, and ECP mode. The programming of the base address, mode selection, and function disable for the Parallel Port can be found in Section 3.
Special circuitry is provided to protect against damage that might be caused when the printer is powered.

Compatible Parallel Port

The address decoding of the compatible parallel port registers utilizing A0 and A1 is shown below.

A1	A0	Port	Access
0	0	Data port	Read/Write
0	1	Status port	Read only
1	0	Control port	Read/Write
1	1	NIL	Tri-state

Data Port

This is a bidirectional data port that transfers 8-bit data. The direction is determined by bit 5 in the Control port. In extended modes (PS/2-compatible, EPP, and ECP), the bit 5 will determine the data direction in conjunction with the Read and Write strobes. In ISA-compatible mode, the parallel port operates in the output mode only.

Status Port
This register provides status for the signals listed below. It is a read only register. Writing to it is an invalid operation that has no effect on the Parallel Port.

Bit 0 - Time-out Status
When in EPP mode, this is the time-out status bit. When this bit is 0, no time-out. When this bit is 1, time-out occurred on EPP cycle (min. 10us). It is cleared to 0 after writing a "1" to this register. When not in EPP mode, this bit is 0.

Bits 1, 2 - are reserved bits. During a read of the Status register, these bits are at low level.

Bit 3 - Printer Error Status
This bit represents the current state of the printer error signal (ERRORJ). The printer sets this low when there is a printer error. This bit follows the state of the ERRORJ pin.

BIT 4 - Printer Selected Status
This bit presents the current state of the printer select signal (SLCT). The printer sets this bit high when it is "On Line" and selected. This bit follows the state of the SLCT pin.

Bit 5 - Paper End Status
This bit represents the current state of the printer end signal (PE). The printer sets this bit high when it detects the end of the paper. This bit follows the state of the PE pin.

BIT 6 - Printer Acknowledge Status
This bit represents the current state of the printer acknowledge signal (ACKJ). The printer pulses this signal low after it has received a character and is ready to receive another one. This bit follows the state of the ACKJ pin.

BIT 7 - Busy Status
This bit represents the current state of the printer busy signal. The printer sets this bit low when it is busy and cannot accept another character. This bit is the complement of the BUSY pin.

Control Port
This register provides all the output signals to control the printer except for bit 5.

Bit 0 - Strobe Control
This bit directly controls the data strobe signal to the printer via the STROBJ pin. This bit is the inverse of the STROBJ pin.

Bit 1 - Autofeed Control
This bit directly controls the automatic feed signal to the printer via the AUTOFDJ pin. Setting this bit high causes the printer to automatically feed after each line is printed. This bit is the inverse of the AUTOFDJ pin.

Bit 2 - Initiate Control
This bit directly controls the signal to initialize the printer via the INITJ pin. Setting this bit to low initializes the printer. The INITJ pin follows this bit.

Bit 3 - Printer Selected Input Control
This bit directly controls the select in signal to the printer via the SLCTINJ pin. Setting this bit high selects the printer. It is the inverse of the SLCTINJ pin.

Bit 4 - Interrupt Request Enable Control
This bit controls the interrupt generated by the ACKJ signal. Its function changes slightly depending on the parallel port mode selected. In the following description, IRQx indicates the interrupt line allocated by the Parallel Port
ISA-compatible and PS/2-compatible mode
when bit 4=0, IRQx is floated
when bit 4=1, IRQx follows ACKJ transitions.
ECP and EPP mode
when bit 4=0, IRQx is floated.
When bit 4=1, IRQx set active on ACKJ trailing edge

Bit 5 - Direction Control
Parallel control direction is valid in extended mode only. In ISA-compatible mode, the direction is always out regardless of the state of this bit. In extended mode, a logic 0 means that the printer port is in output mode (forward direction); a logic 1 means that the printer port is in input mode (reverse direction).

Bits 6 and 7 during a read are at low level, and cannot be written.

Enhanced Parallel Port (EPP)
EPP mode provides for greater throughput than compatible mode by supporting faster transfer time and a mechanism that allows the host to address peripheral device register directly. Faster transfers are achieved by automatically generating the address and data strobes. EPP consists of eight single-byte registers as shown below. It also supports two operation modes: EPP1.7 and EPP1.9.
In Legacy mode, EPP is supported for a parallel port whose base address is 278h or 378h, but not for a parallel port whose base address is 3BCh. There are four EPP transfer operations: address write, address read, data write and data read. An EPP transfer operation is composed of a host read or write cycle and an EPP read or write cycle.

The software must write zero to bits 0,1 and 3 of the control register before executing EPP cycles, since the pins controlled by these bits are controlled by hardware during EPP access. Once these bits are reset to zero, the software may issue multiple EPP access cycles.

EPP Operation

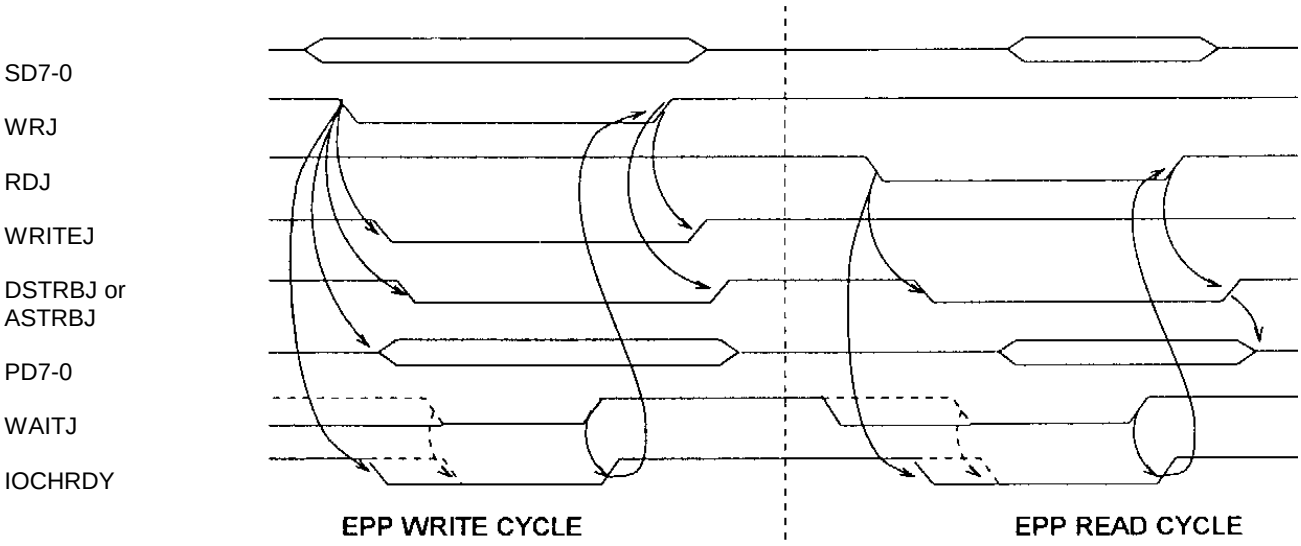
When the EPP mode is selected in the configuration register, the ISA-compatible and PS/2-compatible modes are also available. If no EPP read, write or address cycle is currently running, then the PD7-0 bus is in the compatible mode and all output signals (STROBJ, AUTOFDJ, INIT) are as set by the control register and direction is controlled by the direction bit in the control register.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system hang-up. The timer indicates if more than 10 usec have elapsed from the start of the EPP cycle (IORJ or IOWJ asserted) and the IOCHRDY will be deasserted. If a time-out condition occurs, the current EPP cycle is aborted and the time-out condition is indicated in the bit 0 of status register.

Table 4-25

Name	Offset	Mode	Type	Description
Compatible Data Register	0	SPP/EPP	R/W	This is the compatible mode data register.
Status Register	1	SPP/EPP	R	This is the status register.
Control Register	2	SPP/EPP	R/W	This is the control register.
EPP Address	3	EPP	R/W	This port is read/write. A write operation to it initiates an EPP device's register selection operation.
EPP Data Port 0	4	EPP	R/W	This is a read/write data port. It used to transfer bits 7-0 in an 8-bit host bus interface.
EPP Data Port 1	5	EPP	R/W	This is the second EPP data port. It is used to transfer bits 8 to 15 in a 16-bit host bus interface.
EPP Data Port 2	6	EPP	R/W	This is the third EPP data port. It is used to transfer bits 16-23 in a 32-bit host bus interface.
EPP Data Port 3	7	EPP	R/W	This is the fourth EPP data port. It is used to transfer bits 23-31 in a 32-bit host bus interface.

EPP mode version 1.7 Timing



The timing for a Write/Read EPP 1.7 operation is shown in timing diagram above
The sequence of operation is :

EPP 1.7 Data/Address Write

1. The host writes a byte to Data (Address) port. WRJ goes low to drive data to PD7-0.
2. The EPP pulls WRITEJ low to indicate it's a write cycle.
3. The EPP pulls DSTRBJ (ASTRBJ) low to signal that data is valid.
4. If WAITJ goes low during the cycle, IOCHRDY is pulled low.
5. When WAITJ goes high, the EPP pulls IOCHRDY high and then WRJ will go high
6. When WRJ goes high, it pulls WRITEJ & DSTRBJ (ASTRBJ) high, and then the EPP can change PD7-0

EPP 1.7 Data/Address Read

1. The host reads a byte from Data (Address) port. RDJ goes low to input data from PD7-0.
2. The EPP keeps WRITEJ high to indicate it's a read cycle.
3. The EPP pulls DSTRBJ (ASTRBJ) low to indicate that peripheral have to start sending data.
4. If WAITJ is low during the cycle, IOCHRDY is pulled low.
5. When WAITJ goes high, the EPP pulls IOCHRDY high and then RDJ will go high
6. When RDJ goes high, it pulls WRITEJ & DSTRBJ (ASTRBJ) high, and then the peripheral can tri-state PD7-0

EPP mode version 1.9 Timing

SD7-0

WRJ

RDJ

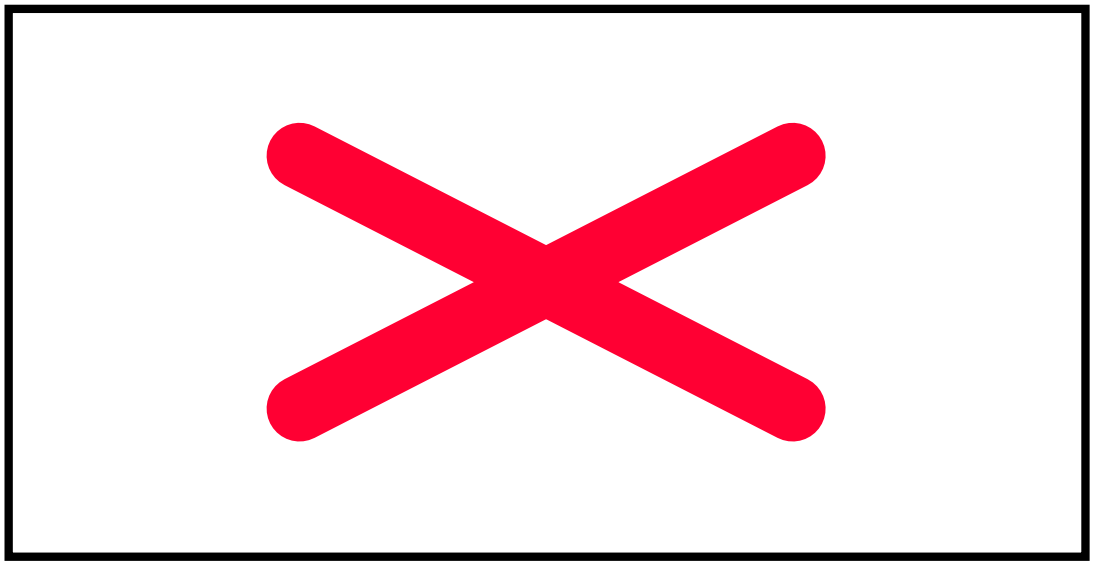
WRITEJ

DSTRBJ or ASTRBJ

PD7-0

WAITJ

IOCHRDY



The timing for a Write/Read EPP 1.9 operation is shown in timing diagram above
The sequence of Write/Read operation is :

EPP 1.9 Data/Address Write

1. The host writes a byte to Data (Address) port. WRJ goes low to drive data to PD7-0.
2. IOCHRDY goes low and waits for WAITJ to go low.
3. If WAITJ goes low or already low, the EPP pulls or keeps WRITEJ low to show being a write cycle.
4. The EPP pulls DSTRBJ (ASTRBJ) low to indicate that data is ready and waits for WAITJ to go high.
5. When WAITJ goes high, it pulls IOCHRDY and DSTRBJ (ASTRBJ) high, and then WRJ will go high to turn off this cycle.

EPP 1.9 Data/Address Read

1. The host reads a byte from Data (Address) port. RDJ goes low to input data from PD7-0.
2. IOCHRDY goes low and waits for WAITJ to go low.
3. If WAITJ goes low or already low, the EPP pulls or keeps WRITEJ high to indicate being a read cycle.
4. The EPP pulls DSTRBJ (ASTRBJ) low to signal the peripheral to start sending data and waits for WAITJ to go high.
5. When WAITJ goes high, the EPP pulls IOCHRDY high and then RDJ will go high
6. When RDJ goes high, it pulls WRITEJ & DSTRBJ(ASTRBJ) high, and then the peripheral can tri-state PD7-0.

Extended Capabilities Parallel Port

Introduction

The ECP support includes a 16-byte FIFO that can be configured for either direction, command/data FIFO tags (one per byte), a FIFO threshold interrupt for both directions, FIFO empty and full status bits, automatic generation of commands and data cycle, and a RLE (run length encoding) expanding (decompression) as explained later.
The ECP is enabled through the configuration registers. Once enabled, its mode is controlled via the bit 7-5 of ECR register.
The AFIFO, SDFIFO, and TFIFO registers access the same ECP FIFO. FIFO can be accessed by host DMA cycles as well as host PIO cycles.
When DMA is configured and enabled (bit 3 of ECR is 1 and bit 2 of ECR is 0), the ECP automatically issues DMA requests to fill the FIFO (in the forward direction when bit 5 of DCR is 0) or to empty the FIFO (in the reverse direction when bit 5 of DCR is 1). All DMA transfers are to or from the FIFO. The ECP does not assert DMA request for more than 32 consecutive DMA cycles. The ECP stops requesting DMA when TC is detected during an ECP DMA cycle.
Please refer to the document IEEE1284 Extended Capabilities Port Protocol and ISA Interface Standard for software operation detail.

Register Description

This section contains the registers used in ECP mode. The I/O address alignment for this register set is shown below and the register descriptions are as follows.

DATAR and AFIFO
Modes 000 and 001 (Data Register)
The Data Register latches the contents of the data bus on the rising edge of the IOWJ input. The contents of this register are buffered and output to the PD7-0. During a read operation, PD7-0 is read and output to the host CPU.

Mode 011 (ECP Address/RLE FIFO)
This register provides a channel address or a Run Length Count to the peripheral, depending on the state of bit 7. The bytes written to this register are placed in the FIFO and transmitted over PD7-0 using ECP protocol. The peripheral device should interpret bit 6-0 as a channel address when bit 7=1 and as a run length count when bit 7=0. The M1543C will assert AUTOFDJ to low to indicate that the information on PD7-0 which represents a command (address/RLE). The AUTOFDJ will drive high when PD7-0 is transferring data.

Status Register (DSR)
Please refer to Section 4.4.6.

Control Register (DCR)
Please refer to Section 4.4.6. Note that the bit 0 of DCR is written to 0 in mode 010 and 011 because the STROBJ signal is controlled by hardware. The bit1 of DCR is written to 0 in mode 011 also. Moreover, in modes 010 and 011, the bit 4 of DCR should be set to 0 to stop the generation of interrupts via ACKJ signal.

SDFIFO (Standard Parallel Port Data FIFO)
Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral device using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

Table 4-26

Name	Address	I/O	Mode type (bit 7-5 of ECR)	Function
DATAR	Base+000h	R/W	000,001	Data register.
AFIFO	Base+000h	W	011	ECP address FIFO.
DSR	Base+001h	R	all	Status register.
DCR	Base+002h	R/W	all	Control register.
SDFIFO	Base+400h	W	010	Standard Parallel Port data FIFO.
DFIFO	Base+400h	R/W	011	ECP data FIFO.
TFIFO	Base+400h	R/W	110	TEST FIFO.
CNFGA	Base+400h	R	111	Configuration register A.
CNFGB	Base+401h	R	111	Configuration register B.
ECR	Base+402h	R/W	all	Extended control register.

DFIFO (ECP Data FIFO)
In the forward direction (bit 5 of DCR is 0), a byte written, or DMAed, to this register is pushed into the FIFO and tagged as data. The data is transmitted by a hardware handshake to the peripheral device using the ECP parallel port protocol.
In the backward direction (bit 5 of DCR is 1) the ECP automatically issues ECP read cycles to fill the FIFO. Reading this register pops a byte from the FIFO.

TFIFO (Test FIFO Mode)
Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction. However the ECP does not issue an ECP cycle to transfer the data to or from the device.
The TFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full TFIFO, the new data is not accepted into the TFIFO. If an attempt is made to read data from an empty TFIFO, the last data byte is re-read again. Data bytes are always read from the head of TFIFO regardless of the value of the direction bit. For example, if 44h, 33h, 22h is written to the FIFO, then reading the FIFO will return 44h, 33h, 22h in the same order as was written.

CNFGA (Configuration Register A)
This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation.

CNFGB (Configuration Register B)
Bit 7 - compress
This bit is read only. During a read, it is a low level. This means that this chip does not support hardware RLE compression. It only supports hardware de-compression.

Bit 6 - IntrValue
Returns the value on the ISA IRQ line.

Bits 5~0 - These bits reflect the IRQ and DRQ selected by the configuration register.

IRQ selected	Config.Reg. B Bits 5: 3
14	110
13	101
11	100
10	011
9	010
7	001
5	111
Others	000

DMA selected	Config.Reg. B Bits 2: 0
3	011
2	010
1	001
Others	000

ECR (Extended Control Register)
This register controls the extended ECP parallel port functions.

Bits 7, 6, 5
These bits are Read/Write and select the operation mode
000: ISA-compatible mode. Write cycles are performed under software control. The FIFO is reset.
001: PS/2-compatible mode. Read and write cycles are performed under software control. The FIFO is reset.
010: ISA-compatible FIFO mode. Write cycles are performed under hardware control (STROBJ is controlled by hardware). Bit 5 of DCR is forced to 0 internally and PD7-0 are driven.
011: ECP mode. The FIFO direction is controlled by bit 5 of DCR. Read and write cycles to the device are performed under hardware control (STROBJ and AUTOFDJ are controlled by hardware).
100: EPP mode. In this mode, EPP is selected if the Parallel Port mode select bits in the configuration register are set to 011 (EPP1.9) or 111 (EPP1.7).
101: Reserved.
110: FIFO test mode. The FIFO is accessible via the TFIFO register. The ECP does not issue ECP cycles to fill/empty the FIFO.
111: Configuration mode. The CNFGA and CNFGB registers are accessible in this mode.

Bit 4 - ECP ERRORJ interrupt mask bit.
When this bit is 0, an interrupt is generated on the high-to-low edge of ERRORJ signal. The ERRORJ signal is used by the peripheral device to request a reverse transfer. An interrupt is also generated when ERRORJ is asserted while this bit is changed from 1 to 0. This prevents the loss of an interrupt between ECR read and ECR write. When this bit is 1, no interrupt is generated.

Bit 3 - ECP DMA enable bit
1: Enable DMA (DMA starts when bit 2 of ECR is 0).
0: Disable DMA unconditionally.

BIT 2 - ECP service interrupt mask/status bit.
When this bit is written to 0 and one of the three interrupt events occur, an interrupt is generated and this bit is set to 1 by hardware.
1) Bit 3 of ECR is 1 and TC is reached during DMA.
2) Bit 3 of ECR is 0 and bit 5 of DCR is 0 (forward direction) and there are free bytes in the FIFO which are equal or greater than the threshold value. A threshold value of 0 means the interrupt is generated when FIFO is empty.
3) Bit 3 of ECR is 0 and bit 5 of DCR is 1 (reverse direction) and there are valid bytes in the FIFO which are equal or greater than the threshold value. A threshold value of 0 means the interrupt is generated when FIFO is full.

When this bit is written to 1, DMA and the above three interrupts are disabled. Writing 1 to this bit does not cause an interrupt.

Bit 1 - FIFO full bit (read only)
1: The FIFO is full.
0: The FIFO has at least 1 free byte.

Bit 0 FIFO empty bit (read only)
1: The FIFO is empty.
0: The FIFO contains at least 1 byte of data.

ISA-compatible and PS/2-compatible Modes (mode 000 and 001)

The software generates cycles by modifying the DCR register and reading the DSR register. The negotiation phase in the ECP mode are also performed in these modes.

ISA-compatible FIFO mode (mode 010)

The ISA-compatible mode uses the same signaling protocol on the parallel port interface as the ISA-compatible mode. However, there are two major operational differences. First data is written to a 16-byte FIFO via SDFIFO location. The FIFO empty and full bits in the ECR provide FIFO status. In addition, DMA can be used to transfer data to the FIFO by enabling this feature in the ECR. Second, the data is transferred to the peripheral using an automatic hardware handshake. This handshake emulates the standard ISA-compatible style software generated handshake. In this mode, the monitoring of ACKJ signal is not required. Interrupts are enabled and reported via the ECR (bit 2). The generation of interrupts is based on the state of the FIFO and not individual transfers (using ACKJ) as is in the standard ISA-compatible mode.

ECP mode (mode 011)

In ECP mode, both data and commands (address/RLE) are transferred using the FIFO. This information can be either written or read from the FIFO using DMA or non-DMA ISA bus transfers. The parallel port interface transfers use an automatic handshake protocol. The host controls the transfer direction by programming the direction bit in the DCR.
When the host is writing to the device (forward direction), STROBJ and BUSY provide the automatic handshake for transfer on the parallel port interface. AUTOFDJ indicates whether PD7-0 contain data (AUTOFDJ is high) or a command (AUTOFDJ is low). For commands, the host writes to the AFIFO and for data the host writes to the DFIFO.
When the host is reading from the device (reverse direction), AUTOFDJ and ACKJ provide the automatic handshake for transfer on the parallel port interface. Data/commands from the device are placed in the DFIFO using this handshake. In this case, BUSY indicates whether PD7-0 contain data (BUSY is high) or a command (BUSY is low).

Test Mode (mode 111)

This mode is for testing the FIFO in PIO and DMA cycles. Both read and write operations are supported, regardless of the direction bit. It can be used to measure the host to ECP cycle throughput, usually with DMA cycles. This mode can also be used to check the FIFO depth and its interrupt threshold, usually with PIO cycles.

Section 5 : Power Management Unit Programming Guide

There are two important parts in Power Management Unit of the M1543C. They are Legacy Power Management Unit (Implemented in M7101) and Advanced Configuration and Power Interface Specification (abbreviated as ACPI). BIOS or Software can control Power Management through the legacy power management unit or ACPI. The details of both are listed below.

5.1 Legacy Power Management Unit (Implemented in M7101)

A. Top View.
B. Timers.
C. Event Configuration.
D. External Switches.
E. Clock Control.
F. General Purpose Input/Output.
G. SMI control.
H. Others.

A. Top View.
The Legacy Power Management Unit based on the default functions of M1533, supports all the requirements for the desktop. It can be divided into several parts:
When talking about the traditional power management, as it is familiar to every one, the SMI or SMM. It is the major method of how the BIOS communicates with the hardware. The SMI sources are all included in Configuration Space of M7101 Register Index 40h-53h. There are two idle timer timeout SMIs (Standby timer and Global Display timer), one APM timer timeout SMIs, IO traps, external switches SMIs and general purpose switch SMIs. The configuration of all timers are at in Configuration Space of M7101 Register Index 54h-5Dh. The Standby timer is defined in Index 54h, APM timer A is defined in Index 55h, and Global Display timer is defined in Index 59h. The monitored events of the timers and the IO traps are set in Configuration Space of M7101 Register Index 60h-73h. Index 74h is the status bit that indicates which event resets the Standby timer when system is in Standby State. Index 75h-76h configures the busy condition of the PCI bus. The External Switches' event is configured at Index 80h-82h and 8Ch-8Eh. Furthermore, the programmable monitored IO/Memory range can be set at Index 94h-97h (Memory Group A) and A4h-A5h (I/O Group C).
Besides the SMI sources and the monitored events, CPU clock control is also an important method for power saving. The M1543C supports Pentium and Pentium II clock controls. It can transfer the Pentium CPU into STPGNT or STPCLK states, and transfer Pentium II CPU into STPGNT or SLEEP or Deep SLEEP states. Also the system clock controls such as clock throttling function are also supported. Most of all, the Auto Thermal throttling can be enabled to prevent system overheat. All of the this control is implemented in M7101 Registers Index 78h-7Ch. Note that some configuration registers of throttling are set at Index 10h-13h of ACPI IO space. Some other functions, such as Speaker control, etc., are set at Index B2h-BEh. Most important of all is the Suspend states supported. There are three states supported by the M1543C, named as the Power On Suspend, Suspend to DRAM and Suspend to Disk. An overview of design for suspend is introduced at ACPI. The details of how to design the hardware or program the registers are described below.

B. Timers.
There are three timers implemented in the M1543C:
a. Standby timer and System state.
There are two states, ON & STANDBY, implemented in this chip. The transition between both is determined by Standby timer and what events it monitors. The monitored events can be selected at Index 60h-63h and the Standby timer can be programmed at Index 54h. For example, assume Standby timer is programmed as 27 minutes and the monitored events as 01h. Then the timer begins to count immediately after being programmed. If there is any Primary HDD access (the enabled monitored event in Index 63h-60h bit 0) detected before timeout (27 minutes), the timer will be reset and recount again. Otherwise, if it is timeout (after pass 27 minutes) because no monitored event (Primary HDD access) occurs, it will stop the timer, the system will transfer to STANDBY state, and the system state defined in Index B2h bit 0 will be set to 1. At the same time, the Standby timeout SMI is generated. BIOS or software can ultilize this SMI to enter Standby system state defined by system designer. If there is an event detected in STANDBY state (Primary HDD access), the timer will be reset to count again and a STANDBY to ON SMI will be generated. As soon as the SMI is generated, system will transfer to ON state, and the system state defined in Index B2h bit 0 will be reset as 0. By the way, system states can be changed by reading or writing Index B2h bit0.

b. Display timer.
This timer is similar to the Standby timer except that it has no relation with the System state. If there is an enabled Display access event detected, the timer will be reset immediately no matter what state it is in. The only difference is that the Display timeout SMI is generated when no monitored events are detected and the timer is timeout. And Display Activity SMI is generated when there is an event detected after timeout. The timer can be configured at Index 59h and the monitored events are defined at Index 64h-65h.
Note : All of the monitored events monitored by the idle timers are masked when Index C8h is set.

c. APM timers.
There is an APM timer that can be used for Advanced Power Management. It has two modes: When Index 55h bit6='0', the timer will generate an SMI when timeout and then stop until it is written again. The operation mode is called Normal mode. When Index 55h bit6='1', the timer would reset to count again when it is timeout and a SMI is generated. This operation mode is called Repeat mode. The timer can be programmed at Index 55h.

List of timers : a. Standby timer (PMU cfg.54h) b. Display timer (PMU cfg.59h) c. APM timer A (PMU cfg.55h)

C. Event Configuration.
There are more than twenty events that should be configured before use. Listed below are those devices events. Besides, some devices can monitor another GPI pin as an input event. Please refer to Index 72h-73h for Vedio, Audio, and Primary HDD.

a. Primary Channel HDD (Index 63h-60h bit0 for Standby Timer, and Index 65h-64h bit0 for Display Timer).
This event monitors 01F0h-01F7h and 3F6h, optionally defined in Index D9h-D8h bit7. When internal IDE is enabled, any IO cycle decoded as M5229 Primary HDD cycle would be monitored, too. Besides, Primary Channel IDE DMA Channel DMA request PIDE_DRQ can be enabled/disabled as the monitored event through Index 6Ch bit0 setting.

b. Secondary Channel HDD (Index 63h-60h bit1 for Standby Timer, and Index 65h-64h bit1 for Display Timer).
This event monitors 0170h-0177h and 376h, optionally defined in Index D9h-D8h bit7. When internal IDE is enabled, any IO cycle decoded as M5229 Secondary HDD cycle would be monitored, too. Besides, Secondary Channel IDE DMA Channel DMA request SIDE_DRQ can be enabled/disabled as the monitored event through Index 6Ch bit1 setting.

c. Audio (Index 63h-60h bit2 for Standby Timer, and Index 65h-64h bit2 for Display Timer).
The audio access is decided by monitoring accesses to MIDI, SoundB, MS_Sound, ADLIB and GAME ports which are selected at Index 6Fh-6Ch bits[15:2]. Besides, which DRQ is monitored or not is decided at Index 6Fh-6Ch bits[21:16].

d. Video (Index 63h-60h bit3 for Standby Timer, and Index 65h-64h bit3 for Display Timer).
There are two sources of Video Events, including Memory access A0000-BFFFF enabled by M7101 Register Index 6Fh-6Ch bit[23], and Graphic I/O(3B0h-3DFh) enabled by M7101 Register Index 6Fh-6Ch bit[25].

e. FDD (Index 63h-60h bit4 for Standby Timer, and Index 65h-64h bit4 for Display Timer).
The default monitor range of FDD Event is 3F0h-3F7h. It can be changed to 370h-377h by writing a '1' to Index 68h bit0. Besides, whether DRQ2 would be monitored is decided at Index 6Fh-6Ch bit[26].

f. Serial IO (Index 63h-60h bit5 for Standby Timer, and Index 65h-64h bit5 for Display Timer).
There are eight COM ports to be monitored at most. They can be enabled/disabled individually at Index 70h bits[7:0].

g. Keyboard (Index 63h-60h bit6 for Standby Timer, and Index 65h-64h bit6 for Display Timer).
IO access ports 060h and 064h will generate Keyboard Event. Moreover, IRQ[1] or IRQ[12] can be monitored by enabling Index 6Fh-6Ch bits[28:27]. And Index D9h-D8h bit[4] can change IRQ[1], IRQ[12] source to become KBCLK, and MSCLK if internal KB/Mouse controller has been disabled.

h. Parallel IO (Index 63h-60h bit7 for Standby Timer, and Index 65h-64h bit7 for Display Timer).
Parallel IO Event monitors D8-D11 of Index 71h-70h bits[11:8]. Note that only one of DRQ0, DRQ1 and DRQ3 can be selected to monitor. It is selected Index 68h bits[2:1].

i. RTC (Index 63h-60h bit8 for Standby Timer).
RTC event monitors pin IRQ8J. If IRQ8J goes from high to low, the falling edge will trigger an event.

j. Modem Ring In (Index 63h-60h bit9 for Standby Timer).
Modem Ring In event monitors pin RI. If RI goes from low to high for the programmed count defined in Index B7h bits[3:0], the final rising edge will trigger an event. Writing a '1' to M7101 Register Index 90h bit2 can change RI to become active low, which means the final programmed falling edge will trigger an event.

k. Memory Group Range (Index 63h-60h bit12 for Standby Timer, and Index 65h-64h bit8 for Display Timer).
There is one Programmable Monitored Memory ranges, Memory Group A, programmable at Index 97h-94h. An example of how to program Memory Group A is shown below: Now, suppose there is a device that occupies memory range from 012340000h to 01235FFFFh. Since bits[31:14] of Index 97h-94h are the address bits of A[31:14], it must be programmed as 0001_0010_0011_010X_XXb where 'X' means "don't care". Because bits[13:4] are the masks of address bits A[23:14], it must be programmed as 00_0000_0111b. As a result, the written value is 012340070h.

l. I/O Group Range (Index 63h-60h bit16 for Standby Timer, and Index 65h-64h bit12 for Display Timer).
There is one Programmable Monitored IO Range, I/O Group C, that can be configured to monitor two programmed range: I/O ports 062h and 066h enabled by Index 71h-70h bit12, and I/O Group Range C enabled by Index 71h-70h bit13. An example of how to program I/O Group C is shown below. Programmer can follow the steps. Suppose IO range 01230h-01237h is to be monitored. If Index A5h-A4h bits[15:2] are the address bits of A[15:2], then it must be programmed as 0001_0010_ 0011_0Xb. Because bits[1:0] are the masks of address bits A[3:2], it must be programmed as 01b. As a result, the written value is 01231h.

m. USB (Index 63h-60h bit20 for Standby Timer).
USB Event is generated when there is a device plugged in/out or the USB bus is busy. It is notified by internal USB block.

n. PWRBTNJ (Index 63h-60h bit21 for Standby Timer).
Power Button Event is generated from the falling/rising edge defined by Index 90h bit0. Or, it can change to become level trigger by setting Index 90h bit3 to 1. Press PWRBTNJ over 4 seconds will force the hardware to Soff-Off mode. It is called Power Button Override function, and can be disabled by setting Index B4h bit2 to 1.

o. IRQ[0] (Index 63h-60h bit22 for Standby Timer).
IRQ0 is system timer interrupt. When it goes from low to high, an event will be triggerred.

p. IRQ[1] or IRQ[12] (Index 63h-60h bit23 for Standby Timer).
IRQ[1] or IRQ[12] come from internal 8259. When each one goes from low to high, an event will be trogger. And Index D9h-D8h bit[4] can change IRQ[1], IRQ[12] source to become KBCLK, and MSCLK if internal KB/Mouse controller has been disabled.

q. IRQ[3-7], IRQ[9-15], NMI, INIT, or SMIJ Asserted (Index 63h-60h bit24 for Standby Timer).
When IRQ[3-7], IRQ[9-15], NMI, INT, or SMI is asserted, an event will be triggerred.

r. PCI_REQJ, or PHOLDJ Asserted (Index 63h-60h bit25 for Standby Timer).
When PCI_REQJ, or PHOLDJ is asserted, an event will be triggerred. PCI_REQJ is coming from North Bridge to indicate there is a PCI master request is on the way. PHOLDJ is asserted when there is an internal master is on the way, it maybe IDE, USB, DMA, or ISA master.

s. BUS_ACT.
BUS_ACT event is active when the PCI bus is busy. How frequent the PCI access can be defined is indicated in Index 76h-75h. Suppose Index 75h is written as 80h (=128 in decimal) and Index 76h bits[5:0] as 10h (=16 in decimal). Index 76h bit6 must set to 1 to enable BUS_ACT circuit. Then the M1543C starts to count number of TRDYJs in every period of 128 PCICLKs. If it is more than 16 TRDYJs in the period, a BUS_ACT Event will be generated.

The following table shows the event and corresponding register summary:

Event	**Corresponding Register**
Primary Driver IO access	Bit7 of Index D9h-D8h Enable/Disable of internal IDE Controller
Primary HDD event	Primary Driver IO access Bit0 of Index 6Fh-6Ch Bit0 of Index 73h-72h.
Secondary Driver IO access	Bit7 of Index D9h-D8h Enable/Disable of internal IDE Controller
Secondary HDD event	Secondary Driver IO access Bit1 of Index 6Fh-6Ch
Audio IO access	Bits[15:2] of Index 6Fh-6Ch
Audio event	Audio IO access Bits[21:16] of Index 6Fh-6Ch Bit2 of Index 73h-72h
Video IO access	Bit25 of Index 6Fh-6Ch (I/O Ports 3B0h-3DFh)
Video Event	Video I/O access Bits23 of Index 6Fh-6Ch Bit3 of Index 73h-72h
Floppy IO access	Bit0 of Index 68h
Floppy Event	Floppy IO access Bit26 of Index 6Fh-6Ch
Serial IO access	Bits[7:0] of Index 71h-70h
Serial Event	Serial IO access
Keyboard IO access	Any access to IO port 60h, 64h
Keyboard Event	Keyboard IO access. Bits[28:27] of Index 6Fh-6Ch
Parallel IO access	Bits[10:8] of Index 71h-70h
Parallel IO event	Parallel IO access Bit11 of Index 71h-70h Bits[2:1] of Index 68h
IO group C IO access/ IOGP C event	Index A5h-A4h Bits[13:12] of Index 71h-70h
Memory group A event	Index 97h -94h
RTC event	IRQ8J asserted
Ring IN event	Count number of Ring IN until matching Index B7h bis[3:0]
USB	Internal USB controller
Power Button	PWRBTNJ pin activity Bit0 of Index 90h Bit3 of Index 90h
IRQ0	System Timer Interrupt
IRQ1 or IRQ12	IRQ1 or IRQ12 activity Bit4 of Index D9h-D8h
IRQ3-7, IRQ9-15, NMI, INIT, or SMIJ	Pins activity
PCI_REQJ, or PHOLDJ	Pin asserted
BUS_ACT event	Index 76h-75h

D. External Switches.
There are 2 specified External Switches (THRMJ and DOCKJ) because ACPWR is used as a hardware setting pin to select AT/ATX mode. For the specified External Switches, they can be programmed to be sensed by rising/falling/debounce at Index 82h-80h and 8Eh-8Ch. Moreover, some specified switches are used not only to generate SMI, but also for some other functions. For example, THRMJ pin can be used as auto thermal throttle as described in the following section. In general, when rising (falling) is enabled and is sensed, then an SMI will be generated to inform CPU. When debounce circuit is enabled, the debounce clock of all switches can be selected at Index B4h bits[6:4].

E. Clock Control.
Before using any function of Clock Control, the Clock Control should be enabled first at Bit9 of Index 13h-10h in ACPI IO space. Every function is influenced by the Break Events selected at Index 7Ch of M7101 configuration space. Followings are the Clock Control Functions supported by the M1543C.

a. Normal Throttle.
In addition to the Clock Control Enable described above, the Duty cycle (bits[3:1] of Index 13h-10h in ACPI IO space) should be configured in advance and then set Throttle Enable bit (bit4 of Index 13h-10h in ACPI IO space) to start Normal Throttle. When it is enabled, the STPCLKJ deasserted and asserted periodically with 32us/128us/512us/2ms period selected in Index5Bh bit7 & bit5. The Break Events will deassert STPCLKJ immediately and reset the high/low timer through Index 5Bh bit6 & bit3 control. That is, STPCLKJ would start throttling again if there is no Break Event for a period of time. Disabling the Throttle Enable bit can stop this function.

b. Auto Thermal Throttle.
It must be done first to program the Duty Cycle of Index 13h-10h bits[3:1] of ACPI IO space and set bit4 of Index 7Bh of M7101 configure space to Enable the Auto Thermal Throttle. When it is enabled and THRMJ has asserted for 2 seconds (active level is defined in Index 7Bh bit5), clock throttling is started. The Break Events will deassert STPCLKJ immediately and reset the high/low timer through Index 5Bh bit6 & bit3 control, too. Throttling is disabled immediately when THRMJ has been deasserted or this feature is disabled.

c. STPGNT (For Pentium CPU).
Before using STPGNT function, the bit0 of Index 7Bh of M7101 Configuration Space should be selected first, and bit1 of Index 7Bh must be reset as 0 to select Pentium CPU. If STPGNT green mode is demanded, bit3 of Index 7Bh should be set to '0' to select STPGNT. Then, READ I/O port address B2h for Soft STPCLK or READ Index 14h of ACPI I/O space for Processor Level 2 will force CPU entering into the STPGNT state by asserting STPCLKJ. At this system state, CPU_STPJ will not be asserted to stop CPUCLK. Besides, ZZ is used to force L2 cache into Powerdown mode enabled by bit0 of Index 7Bh. STPCLKJ will be deasserted when any Break Event occurs defined in M7101 Register Index 7Ch. By the way, Soft STPCLK or READ LVL2 will cause the same result.

d. STPCLK (For Pentium CPU).
Before using STPCLK function, the bit0 of index 7Bh of M7101 Configure Space should be selected first, and bit1 of Index 7Bh must be reset as 0 to select Pentium CPU.. If STPCLK green mode is demanded, bit3 of Index 7Bh should be set to '1' to select STPCLK. Then, READ I/O port address B2h for Soft STPCLK or READ Index 15h of ACPI I/O space for Processor Level 3 both will force CPU entering into the STPCLK state by asserting STPCLKJ, and CPU_STPJ to stop CPUCLK. They will be deasserted when any Break Event occurs. By the way, Soft STPCLK or READ LVL3 will cause the same result.

e. SLEEP (For Pentium II CPU).
Before using SLEEP function, the bit0 of Index 7Bh of M7101 Configuration Space should be selected first, and bit1 of Index 7Bh must be set to 1 to select Pentium II CPU. If SLEEP green mode is demanded, bit3 of Index 7Bh and bit0 of Index 7Ah should be set to '01' to select SLEEP function. Then, READ I/O port address B2h for Soft STPCLK, or READ Index 14h of ACPI I/O space for Processor Level 2 with setting M7101 Register Index 7Bh bit6 to 1, or READ Index 15h of ACPI I/O space for Processor Level 3 with resetting M7101 Register Index 7Bh bit7 as 0, will force CPU entering into the SLEEP state by asserting STPCLKJ, and SLEEPJ. At this system state, CPU_STPJ will not be asserted to stop CPUCLK. Besides, ZZ is used to force L2 cache into Powerdown mode enabled by bit0 of Index 7Bh. STPCLKJ will be deasserted when any Break Event occurs defined in Index 7Ch.

f. STPGNT (For Pentium II CPU).
Before using STPGNT function, the bit0 of Index 7Bh of M7101 Configuration Space should be selected first, and bit1 of Index 7Bh must be set to 1 to select Pentium II CPU. If STPGNT green mode is demanded, bit3 of Index 7Bh and bit0 of Index 7Ah should be set to '00' to select STPGNT function. Then, READ I/O port address B2h for Soft STPCLK, or READ Index 14h of ACPI I/O space for Processor Level 2 with resetting M7101 Register Index 7Bh bit6 as 0, will force CPU entering into the STPGNT state by asserting STPCLKJ. At this system state, CPU_STPJ will not be asserted to stop CPUCLK. Besides, ZZ is used to force L2 cache into Powerdown mode enabled by bit0 of Index 7Bh. STPCLKJ will be deasserted when any Break Event occurs defined in Index 7Ch.

g. DEEP SLEEP (For Pentium II CPU).
Before using STPGNT function, the bit0 of Index 7Bh of M7101 Configuration Space should be selected first, and bit1 of Index 7Bh must be set to 1 to select Pentium II CPU. If STPGNT green mode is demanded, bit3 of Index 7Bh and bit0 of Index 7Ah should be set to '10' to select DEEP SLEEP function. Then, READ I/O port address B2h for Soft STPCLK, or READ Index 14h of ACPI I/O space for Processor Level 2 with setting M7101 Register Index 7Bh bit7 to 1, will force CPU entering into the DEEP SLEEP state by asserting STPCLKJ, SLEEPJ, and CPU_STPJ. At this system state, CPU_STPJ will be asserted to stop CPUCLK. Besides, ZZ is used to force L2 cache into Powerdown mode enabled by bit0 of Index 7Bh. STPCLKJ will be deasserted when any Break Event occurs defined in Index 7Ch.
Note : Bits[5:3] of Index 79h-78h are the CPU PLL time when CPU transfers from STPCLK state to STPGNT state. Also, Please refer to the tables after M7101 Register Index 7Bh for more detail information.

F. General Purpose Input/Output.
There are 11 General Purpose Output pins, 6 General Purpose Input pins, 8 General Purpose IO pins, 16 extended GPIs, and 16 extended GPOs . Please refer to section 2.7 for more detail information. As most of these pins are multi-function pins, they must be enabled by programming Index 59h-5Bh of configuration space of device M1543C (not PMU) and Index C6h of configuration space of PMU device.

a. GPI. The input status of GPI pins can be read from Index C5h-C4h.
b. GPO. The output level of GPO pins can be programmed at Index C3h-C0h.
c. GPIO[7:0].
   1. Programming the directions of GPIO[7:0] at Index 7Dh.
   2. Programming the output level of GPIOx at Index 7Eh, if they are configured as outputs.
   3. Read the status of GPIOx at Index 7Fh, if they are configured as inputs.
d. EGPI[15:0]. The input status of GPI pins can be read from Index BBh-BAh.
e. EGPO[15:0]. The output level of GPO pins can be programmed at Index B9h-B8h.

G. SMI control.

a. ACPI mode/M7101 mode.

When set as ACPI mode, the status bit of any event is set as soon as the event occurs, no matter whether its corresponding enable/disable bit is set or not. As M7101 mode, the status bit is set if and only if both event occurs and the enable/disable bit is set. The mode is selected by setting Index 77h bit7.

b. Soft SMI.

Write I/O port address B1h will generate a Soft SMI. It can be delayed to generate Soft SMI if bit2 of Index 77h is set.

c. Read/Write clear SMI.

When set as Read Clear SMI, all status port in configure space are cleared when it is read by software. As Write Clear SMI, writing a '1' to the corresponding status bit can clear it. It is selected by setting Index 77h bit4.

d. Delayed SMI.

SMI will be generated after a period of time when an SMI source is generated. Moreover, the SMI will be delayed again if there is any event monitored by Standby timer occurs. Only when no event occurs during that period of time, then SMI is generated. The sequence to delay SMI will be:

1. Select Delayed time at bits[1:0] of Index 77h.
2. Enable/Disable delayed SMI at bit2 of Index 77h for Soft SMI and bit2 & bit0 of Index D8h for ACPWR, THRMJ, and DOCKJ.

e. SMI sources

1. 3 timeout timers *	6. Bus Master Active *	9. Serial IRQ SMI*
2. Power button press	7. SMBus SMI *	10. Thermal override (>2sec)
3. RTC alarm	8. I/O access (1st , 2nd HDD, Audio, Video, floppy, serial, parallel,	11. THRMJ, DOCKJ, ACPWR input switch pins assert
4. Software SMI *	keyboard, IO group C	12. USB activity(Plug in/out or active device)
5. USB bus SMI *		
	* - Pure SMI source	

H. Others.

a. Write Beep function.

1. Enable bit6 of Index B3h.
2. Select Beep latency time at bits[5:4] of Index B3h.
3. Write Index CAh to generate Beeps. Maximum of 3 writings are allowed at one time.

b. Periodical Beep function.

1. Enable bit6 of Index B3h.
2. Select Beep period at bits[1:0] of Index B3h.
3. Select Beep latency time at bits[3:2] of Index B3h.

Note : As soon as bits[3:2] of Index B3h are not "00", the Periodical Beep function is enabled and the first beep begins to beep.

c. LED control.

Two LED output controls are supported.

1. SPLED and SQWO. Programmed at Index B5h.

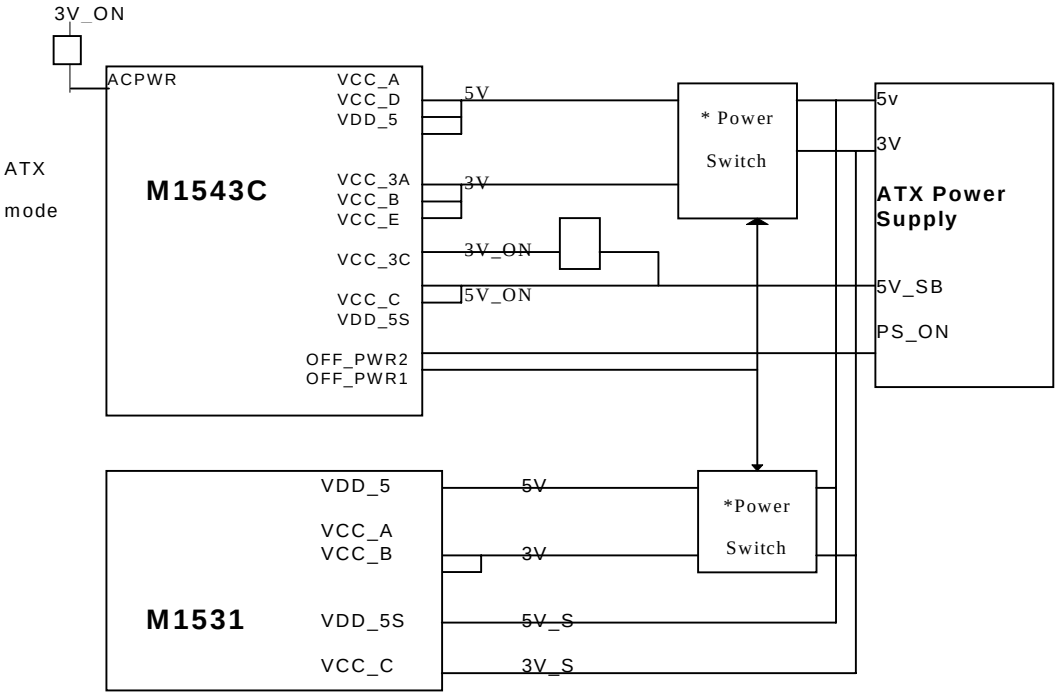
d. AT/ATX mode select

The ACPWR input pin pull 'low' to select legacy AT mode, pull "high" to select ATX mode. In ATX mode, the system enters soft-off state. User can use power button (PWRBTNJ) to power on system.

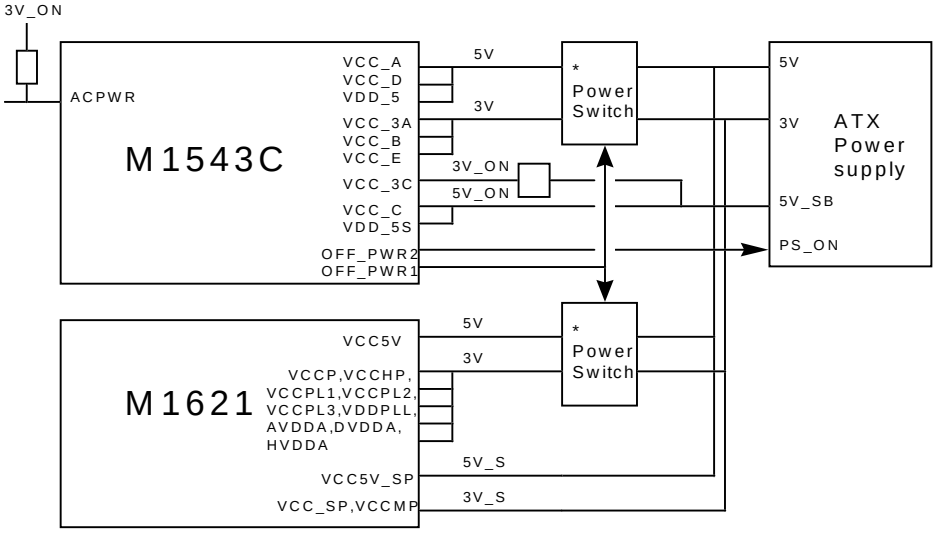
e. Supports PCI PMEJ pin (use DOCKJ pin)

Select DOCKJ pin to level trigger (offset 0x90h bit 1 = '1')

f. Power Control Connection

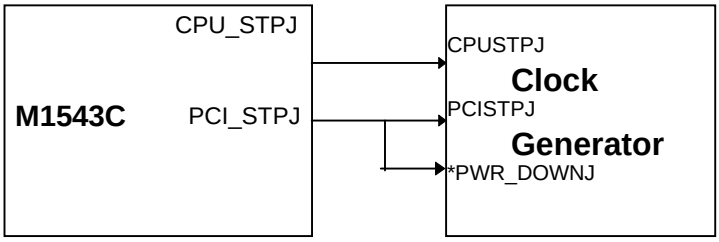


* If the system does not support S3 state, the power switch can be removed.



* If the system does not support S3 state, the power switch can be removed.

g. Clock Control Connection



* If the system must stop all clocks in S1 state, the PCI_STPJ can connect to PWR_DOWNJ pin of clock generator.

5.2 Advanced Configuration and Power Interface Specification.

A. Top View.
B. Power Management Timer.
C. SCI(SMI) Sources.
D. Suspend Modes.
E. Clock Control.
F. Resume Events.
G. Global Lock.
H. Point for Attention.

A. Top View.
The M1543C supports the ACPI (ver. 1.0) specification, includes the SCI interrupt, 24/32bit Power Management Timer, System Suspend modes, CPU Power saving modes and ACPI I/O Registers.

B. Power Management Timer.
The M1543C supports a 24-bit or 32-bit (Selected by M7101 Register Index BDh bit2) fixed rate free running count-up Power Management Timer. The ACPI uses the read-only port (ACPI Index 0Bh-08h, 32bit) to read the current value of the timer. To allow software to extend the number of bits in the timer, the Status bit (ACPI Index 00h bit0) is set at any time the bit-22 or bit-30 of the timer goes from HIGH to LOW. If the Enable bit (ACPI Index 02h bit0) is set, then the timer generates a system control interrupt (SCI).

C. SCI(SMI) Sources.

Source	**Status Reg**	**Enable Reg**	**Interrupt**
Power Management Timer	ACPI Index 00h bit0	ACPI Index 02h bit0	SCI
BIOS Release	ACPI Index 00h bit5	ACPI Index 02h bit5	SCI
Power Button	ACPI Index 01h bit0	ACPI Index 03h bit0	SCI/SMI
RTC alarm	ACPI Index 01h bit2	ACPI Index 03h bit2	SCI/SMI
Thermal Control	ACPI Index 18h bit0	ACPI Index 1Ah bit0	SCI/SMI
Thermal Override	ACPI Index 18h bit1	ACPI Index 1Ah bit1	SCI/SMI (THRMJ assert > 2sec)
USB Event	ACPI Index 18h bit2	ACPI Index 1Ah bit2	SCI/SMI
Docking	ACPI Index 19h bit0	ACPI Index 1Bh bit0	SCI/SMI
AC Adapter	ACPI Index 19h bit2	ACPI Index 1Bh bit2	SCI/SMI
Ring	ACPI Index 19h bit3	ACPI Index 1Bh bit3	SCI/SMI
ACPI Release	ACPI Index 1Ch bit0	ACPI Index 1Eh bit0	SMI

Some sources can be enabled to generate the ACPI interrupt, SCI or an SMI. (SCI_EN, Index 04h bit0)

D. Suspend Modes.

The M1543C supports five types of system suspend modes.

1)S0: Working

2)S1: Sleeping(Sleeping with Processor Context Maintained)

- .CPU enters the STOP CLOCK state (using STPCLKJ, CPU_STPJ)
- .SRAM Power Saving Mode (using ZZ, M7101 Register Index 7Bh bit0)
- .Pentium II Sleep Mode (using SLEEPJ, M7101 Register Index 7Bh bit1, Hardware Setting)
- .Inform North Bridge to switch to Suspend Refresh mode (using SUSTAT1J)
- .PAD enters Power Saving Mode
- .Stop Clock Run Option:
  - .Stop ISP PCICLK (M1543C Register Index 5Eh bit5)
  - .Stop ISP DMACLK (M1543C Register Index 5Eh bit6)
  - .Stop USB PCICLK (M1543C Register Index 5Eh bit7)
  - .Stop 119 KHz clock of M8254 and cold reset counter clock (M1543C Register Index 5Fh bit4)
  - .Stop All AT clocks, including SYSCLK and KB CLK (M1543C Register Index 5Fh bit5)
  - .Stop Internal Keyboard clock (M1543C Register Index 5Fh bit6)
  - .Stop SYSCLK (M1543C Register Index 5Fh bit7)

3)S3: Suspend To DRAM (Sleeping with Processor Context Lost)

- .Inform North Bridge to switch to Suspend Refresh mode (using SUSTAT1J)
- .All Power Off except Resume Block
- .Stop the M1543C PCICLK (using OFF_PWR1)
- .Stop the M1543C OSC14M (using OFF_PWR1)
- .Run the M1543C CLK32O (As the base clock for DRAM Suspend Refresh)
- .Run the M1543C CLK32I

4)S4: Suspend To DISK(Non_volatile storage)

- .All Power Off except Resume Block
- .Stop the M1543C PCICLK (using OFF_PWR1)
- .Stop the M1543C OSC14M (using OFF_PWR1)
- .Stop the M1543C CLK32O
- .Run the M1543C CLK32I

5)S5: Soft Off

- .The same as S4

Using CPU_STPJ to control clock generator to stop CPU clock and M1531 host clock
Using PCI_STPJ to control clock generator to stop PCI slots clock and M1531 PCI clock
Using OFF_PWR1 to control power plane to stop M1531, M1533 off-power and on-board devices except RAM power regions
Using OFF_PWR2 to control power plane to stop M1531 total power, M1533 off-power and on-board devices power regions.

How to enter S1 state :

- .Set CLK_EN='1' (ACPI Index 11h bit1)
- .Program the time of Switch Normal to Suspend Refresh (PG_78_D6-8,suggest 128 us)
- .Program the stable time of Clock Generator PLL, when system is from S1 to S0 (PG_78_D0-2,suggest 1 ms)
- .Program the stable time of CPU PLL, when system is from S1 to S0 (PG_78_D3-5,suggest 4 ms)
- .Program the time of Switch Suspend to Normal Refresh (PG_78_D9-11,suggest 128 us)
- .Set SLP_EN='1', SLP_TYP="011" (ACPI Index 05h bit5, bits[4:2])

How to enter S2 state:

- .Set SLP_EN='1', SLP_TYP="010" (ACPI Index 05h bit5, bits[4:2])

How to enter S3 state:

- .Set SLP_EN='1', SLP_TYP="001" (ACPI Index 05h bit5, bits[4:2])

How to enter S4 state:

- .Set SLP_EN='1', SLP_TYP="000" (ACPI Index 05h bit5, bits[4:2]) or
  - .Power Button Override Event (PWRBTNJ Assert > 4 sec, M7101 Register Index B4h bit2)

E. Clock Control.

.CPU Clock Control(CLK_EN)
.THROTTLE (THRO_EN=>ACPI Index 10h bit4, THRO_DTY=> ACPI Index 10h bits[3:1])
.STOP GRANT STATE (Read LVL2, ACPI Index 14h bits[7:0])
.STOP CLOCK STATE (Read LVL3, ACPI Index 15h bits[7:0])

F. Resume Events.

Event	Status Reg	Enable Reg	Resume from
Power Button	ACPI Index 01h bit0	ACPI Index 03h bit0	S1/S3/S4/S5
RTC alarm	ACPI Index 01h bit2	ACPI Index 03h bit2	S1/S3/S4/S5
USB Event	ACPI Index 18h bit2	ACPI Index 1Ah bit2	S1
Docking	ACPI Index 19h bit0	ACPI Index 1Bh bit0	S1/S3/S4/S5
AC Adapter	ACPI Index 19h bit2	ACPI Index 1Bh bit2	S1/S3/S4/S5
Ring	ACPI Index 19h bit3	ACPI Index 1Bh bit3	S1/S3/S4/S5
IRQ[0]	ACPI Index 1Dh bit0	ACPI Index 1Fh bit0	S1
IRQ[1],IRQ[12]	ACPI Index 1Dh bit1	ACPI Index 1Fh bit1	S1
IRQ[3],IRQ[4]	ACPI Index 1Dh bit2	ACPI Index 1Fh bit2	S1
IRQ[5],IRQ[6]	ACPI Index 1Dh bit3	ACPI Index 1Fh bit3	S1
IRQ[7],IRQ[9]	ACPI Index 1Dh bit4	ACPI Index 1Fh bit4	S1
IRQ[10],IRQ[11]	ACPI Index 1Dh bit5	ACPI Index 1Fh bit5	S1
IRQ[13]	ACPI Index 1Dh bit6	ACPI Index 1Fh bit6	S1
IRQ[14],IRQ[15]	ACPI Index 1Dh bit7	ACPI Index 1Fh bit7	S1

G. Global Lock.

The M1543C supports two sets of Registers :
a. BIOS_RLS(ACPI IO Index 20h bit1), GLB_STS(ACPI IO Index 00h bit5), GLB_EN(ACPI IO Index 02h bit5).
b. GLB_RLS(ACPI IO Index 04h bit2), BIOS_STS(ACPI IO Index 1Ch bit0), BIOS_EN(ACPI IO Index 1Eh bit0).

In the event of a resource conflict, the Global Lock is used by the ACPI driver to inform the BIOS driver that it is finished using a shared resource, or used by the BIOS driver to inform the ACPI driver.

H. Point of Attention.

.The ACPI Status Registers only support "write '1'" clear method.
.The Legacy Status Registers support "write '1'" clear or "Read Clear" method. (M7101 Register Index 77h bit4)
.The ACPI and Legacy Common Status Registers can clear both or one side. (M7101 Register Index 77h bit5)
.The ACPI and Legacy SMI method can select ACPI or 7101 mode. (M7101 Register Index 77h bit7)

I. ACPI Programming Guide

ACPI BIOS initialize chipset registers :

1) Program ACPI/SMB IO address (programmed by BIOS, ex. DF00h/DF80h)

Chip	Space	Offset	Value
PMU	CFG	10h	00h
PMU	CFG	11h	DFh
PMU	CFG	14h	80h
PMU	CFG	15h	DFh
PMU	CFG	04h	01h(Bit0)->Enable IO command

2) Reset PMU clock control circuit.

PMU	CFG	7Ch	12h(bit4,1)
PMU	CFG	7ch	00h ->must set ‘high’ to ‘low’

3) Program North Bridge arbiter control IO address to DF30h and pass to PCI bus.

Chip	Space	Offset	Value
M1531/M1541/M1621	CFG	70h/E8h/A0h	30h
M1531/M1541/M1621	CFG	71h/E9h/A1h	DFh
M1531/M1541	CFG	72h/EAh	01h(bit1-0)-> pass to PCI bus
M1531/M1541	CFG	77h/Ebh	80h(bit7)-> Enable memory data bus gated clock during S1.

4) Program South Bridge

M1543C	CFG	5Eh	E0h (bit7-5) -> Stop USB, ISP, clock during S1.
M1543C	CFG	5Fh	F0h(bit7-4)-> Stop SYSCLK, KBC, AT, 14M clock during S1.
M1543C	CFG	76h	81h(bit7) -> disable SCI routing to IRQ13. (bit4-0) -> SCI routing to IRQ9 and level trigger.

5) Program PMU

PMU	CFG	5Bh	4Fh
PMU	CFG	78h	69h
PMU	CFG	79h	02h -> for M1531B 0Ah -> for M1541
PMU	CFG	7Ah	06h(bit2,1)-> Start masking INTR,SMI and INIT when STOP GRANT cycle is issued, disable clock control to monitor HALT cycle.
PMU	CFG	7Ch	12h(bit4,1)-> Set INTR, IRQ0 as break event.
PMU	CFG	BDh	04h(bit2) -> Set ACPI free run 32-bit timer.
PMU	CFG	D8h	40h(bit6) -> Stop south bridge PCI clock during S1.

6) Enable clock control function

ACPI	IO	DF11h	02h(bit1) -> Enable clock control

7) Initialize the ACPI event features.

ACPI	IO	DF00h	FFh->Clear ACPI event status.
ACPI	IO	DF01h	FFh-> Clear ACPI event status.
ACPI	IO	DF18h	FFh-> Clear ACPI event status.
ACPI	IO	DF19h	FFh-> Clear ACPI event status.
ACPI	IO	DF1Ch	FFh-> Clear ACPI event status.
ACPI	IO	DF1Dh	FFh-> Clear ACPI event status.
ACPI	IO	DF02h	00h-> Disable ACPI event.
ACPI	IO	DF03h	00h-> Disable ACPI event.
ACPI	IO	DF1Ah	00h-> Disable ACPI event.
ACPI	IO	DF1Bh	00h-> Disable ACPI event.
ACPI	IO	DF1Eh	00h-> Disable ACPI event.
ACPI	IO	DF1Fh	00h-> Disable ACPI event.

ACPI compatible OS initialization :

1. Scanning memory for ACPI tables.
2. Turn on ACPI
   . Write ACPI_Enable value to SMI_CMD port ->described in the FACP table, ex. 0 AA B1
   . Hardware assert software SMI to BIOS.
   . BIOS check port value, if ACPI_ENABLE:
   1) ACPI IO DF04h 01h(bit0) -> Enable SCI
   2) M1543C CFG 5Fh F4h(bit3) -> Disable PMU device.

5.3 System Management Bus Host Controller Programming Example

Programming Guide for SMBus
* if PMU(M7101) Register index 14h-17h set to be 00003A81h
* For SMB Host Controller to be a master only, just set M7101's Register Index E0h = "01h" & E2h = "20h".
* then below Example's index "03h" will be "00003A80h+03h" that is 'I/O address of SMB Host Controller' = "00003A83h".
Example:
1. A "Write Byte" cycle for Smart Battery Selector (address="14h"), and the write data is 3Ah (DataA="3Ah") with "Command Reg" being "22h".
=> write '1' clear to let read index 00h to be "04h" (Idle).
=> write index 03h "14h"(address="14h" and write cycle).
=> write index 01h "20h"(Write/Read Byte command).
=> write index 04h "3Ah"(DataA is for Byte data use).
=> write index 07h "22h"(Command Reg = "22h").
=> write index 02h "XXh"(write any data for index 02h to start).
=> wait SMI (or Interrupt).
=> read index 00h, if bit4='1' it means complete successfully.
=> else then write '1' clear and restart the protocol.

2. A "Write Word" cycle for Smart Battery (address="16h"), and the write data is Low Byte=27h (DataA="27h"), and High Byte=D1h (DataB="D1h") with "Command Reg" being "33h".
=> write '1' clear to let read index 00h to be "04h" (Idle).
=> write index 03h "16h"(address="16h" and write cycle).
=> write index 01h "30h"(Write/Read Word command).
=> write index 04h "27h"(DataA is for Low Byte data use).
=> write index 05h "D1h"(DataB is for High Byte data use).
=> write index 07h "33h"(Command Reg = "33h").
=> write index 02h "XXh"(write any data for index 02h to start).
=> wait SMI (or Interrupt).
=> read index 00h, if bit4='1' it means complete successfully .
=> else then write '1' clear and restart the protocol.

3. A "Read Word" cycle for Thermal (address="90h"-"9Eh"), this procedure is based on the address="92h" with "Command Reg" being "45h".
=> write '1' clear to let read index 00h to be "04h" (Idle).
=> write index 03h "93h"(address="92h" and read cycle).
=> write index 01h "30h"(Write/Read Word command).
=> write index 07h "45h"(Command Reg = "45h").
=> write index 02h "XXh"(write any data for index 02h to start).
=> wait SMI (or Interrupt).
=> read index 00h, if bit4='1' it means complete successfully .
=> else then write '1' clear and reinitial the procedure.
=> if succeed, read index 04h for Low Byte (DataA) , and index 05h for High Byte (DataB).

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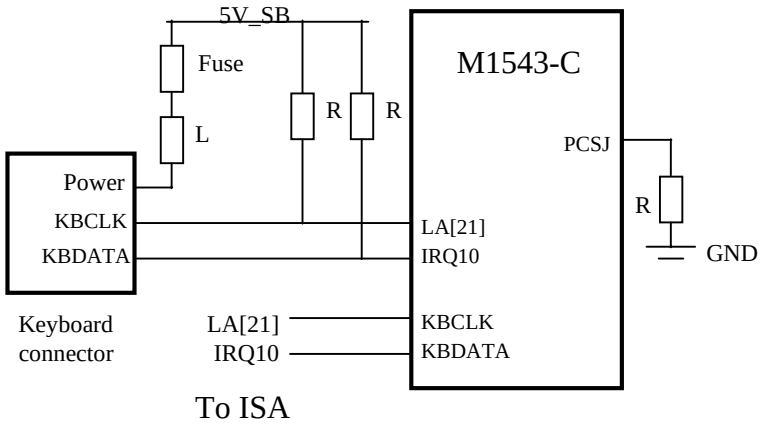
4. A "Write Block" cycle for Clock Synthesizer (address="D2h"). It has a total of 6 bytes data, for example, to send and the write data is "07h", "2A", "51h", "D0h", "46h" and "38h" with "Command Reg" being "77h" .
=> write '1' clear to let read index 00h to be "04h" (Idle).
=> write index 03h "D2h"(address="D2h" and write cycle).
=> write index 01h "C0h"(Write/Read Block command and reset Block Register Pointer).
=> write index 04h "06h"(DataA is for Block Byte number).
=> write index 06h "07h"(Block Data).
=> write index 06h "2Ah"(Block Data).
=> write index 06h "51h"(Block Data).
=> write index 06h "D0h"(Block Data).
=> write index 06h "46h"(Block Data).
=> write index 06h "38h"(Block Data).
=> write index 07h "77h"(Command Reg = "77h").
=> write index 02h "XXh"(write any data for index 02h to start).
=> wait SMI (or Interrupt).
=> read index 00h, if bit4='1' it means complete successfully .
=> else then write '1' clear and restart the protocol.

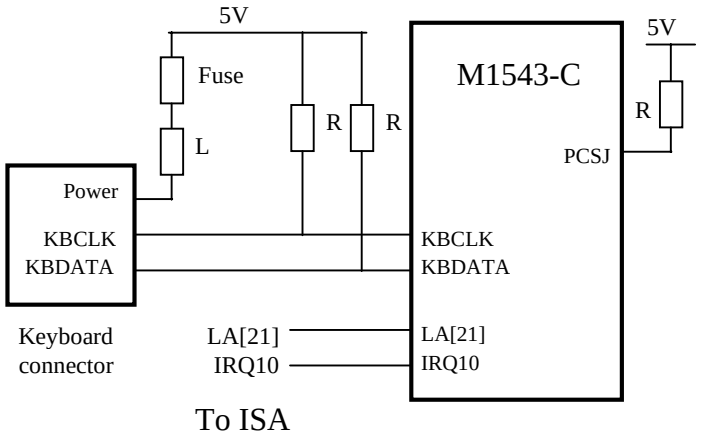
5.4 Hotkey Function Implementation

5.4.1 Hotkey Hardware Design Guide

Hotkey Enable



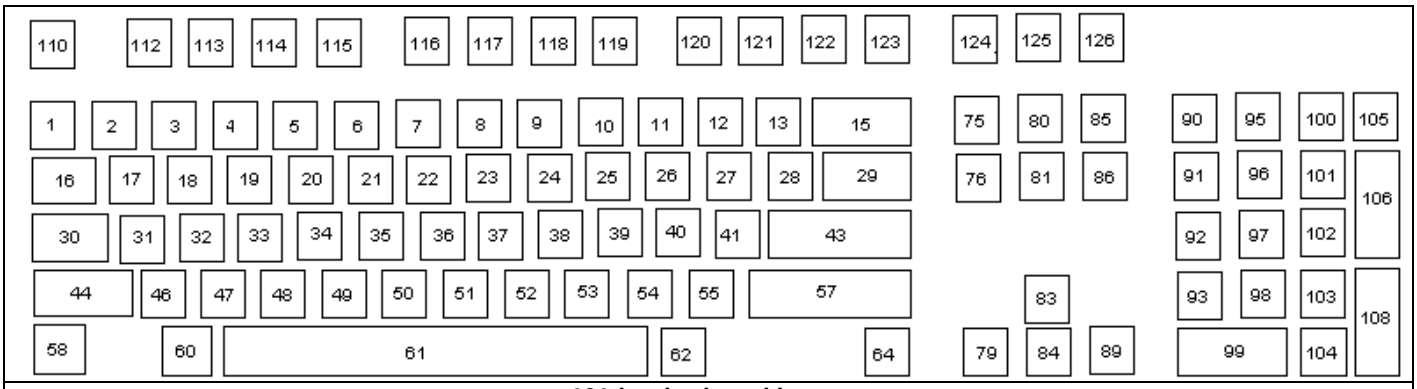
Hotkey Disable



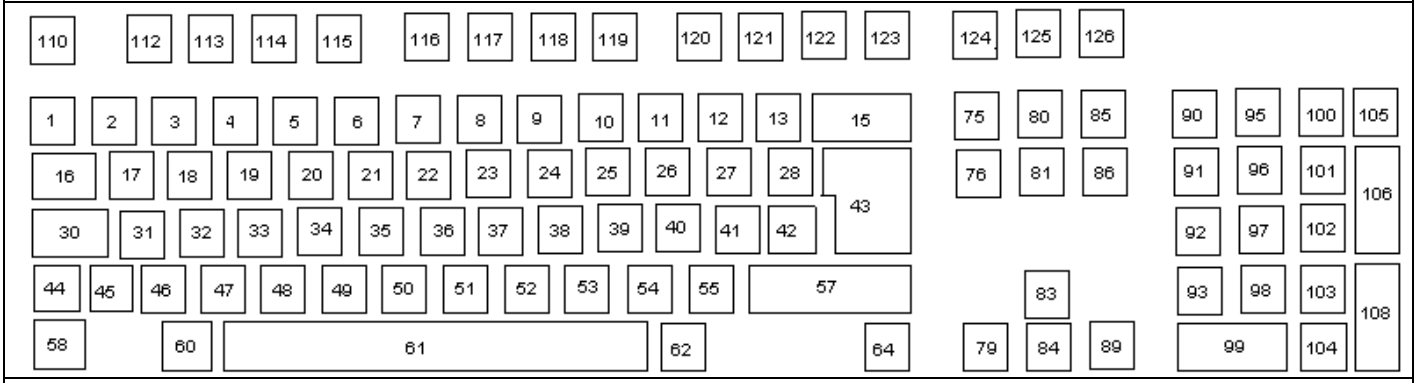
5.4.2 Hotkey Programming Guide

1. Check the M1543C PCI configuration register index 54h bit7. If index 54h bit7 = 1 then hotkey hardware is supported. If index 54h bit7 =0 then hotkey hardware is not supported.
2. Set Super I/O logical device C index 30h bit0 to 1 to enable hotkey function.
3. Super I/O logical device C index F0h is suggested to use default value
4. Write three make codes into Super I/O logical device C index F1h, F2h, F3h to define which key combination is hotkey.
5. The suggested value of Super I/O logical device C index F4h is 82h.

5.4.3 Keyboard Scan Codes and Make Codes



101-key keyboard layout



102-key keyboard layout

Scan Codes
The following tables list the key numbers of the three scan code sets and their hexadecimal values.

Scan Code Tables
In scan code, each key is assigned a unique 8-bit make scan code, which is sent when the key is pressed. Each key also sends a break code when the key is released. The break code consists of 2 bytes, the first of which is the break code prefix (hex F0). The second byte is the same as the make scan code for that key. The typematic scan code for a key is the same as the make code.

The following charts show the keys and the scan codes the keys send, regardless of any shift states in the key board or the system.

Keyboard Scan Codes (Part 1 of 5)

Key no.	Make Code	Break Code	Key no.	Make code	Break code
1	0E	F0 0E	47	22	F0 22
2	16	F0 16	48	21	F0 21
3	1E	F0 1E	49	2A	F0 2A
4	26	F0 26	50	32	F0 32
5	25	F0 25	51	31	F0 31
6	2E	F0 2E	52*	3A	F0 3A
7	36	F0 36	53	41	F0 41
8*	3D	F0 3D	54*	49	F0 49
9*	3E	F0 3E	55	4A	F0 4A
10*	46	F0 46	57	59	F0 59
11	45	F0 45	58	14	F0 14
12*	4E	F0 4E	60	11	F0 11
13*	55	F0 55	61	29	F0 29
15	66	F0 66	62	E0 11	E0 F0 11
16	0D	F0 0D	64	E0 14	E0 F0 14
17	15	F0 15	90	77	F0 77
18	1D	F0 1D	91	6C	F0 6C
19	24	F0 24	92	6B	F0 6B
20	2D	F0 2D	93	69	F0 69
21	2C	F0 2C	96	75	F0 75
22	35	F0 35	97	73	F0 73
23*	3C	F0 3C	98	72	F0 72
24*	43	F0 43	99	70	F0 70
25*	44	F0 44	100	7C	F0 7C
26	4D	F0 4D	101	7D	F0 7D
27	54	F0 54	102	74	F0 74
28	5B	F0 5B	103	7A	F0 7A
29**	5D	F0 5D	104	71	F0 71
30	58	F0 58	105	7B	F0 7B
31	1C	F0 1C	106	79	F0 79
32	1B	F0 1B	108	E0 5A	E0 F0 5A
33	23	F0 23	110	76	F0 76
34	2B	F0 2B	112	05	F0 05
35	34	F0 34	113	06	F0 06
36	33	F0 33	114	04	F0 04
37*	3B	F0 3B	115	0C	F0 0C
38*	42	F0 42	116	03	F0 03
39*	4B	F0 4B	117	0B	F0 0B
40*	4C	F0 4C	118	83	F0 83
41	52	F0 52	119	0A	F0 0A
42***	5D	F0 5D	120	01	F0 01
43*	5A	F0 5A	121	09	F0 09
44	12	F0 12	122	78	F0 78
45***	61	F0 61	123	07	F0 07
46	1A	F0 1A	125	7E	F0 7E

* See 84/85-key keyboard in this section
** Key 29 on US keyboards only
*** Keys 42 and 45 on all but US keyboards.

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Keyboard Scan Codes, 84/85 Numeric keypad

Key no.	Make Code	Break Code	Key no.	Make code	Break code
8	47	C7	25	4D	CD
9	48	C8	37	4F	CF
10	48	C9	38	50	D0
12	4A	CA	39	51	D1
13	4E	CE	40	37	B7
23	4B	CB	52	52	D2
24	4C	CC	54	53	D3

The remaining keys send a series of codes dependent on the state of the shift keys (Ctrl, Alt and Shift) and the state of Num Lock (On or Off). Because the base scan code is identical to that of another key, an extra code (hex E0) has been added to the base code to make it unique.

The following charts show the make/break code using the left Shift key. If the right Shift key is used, substitute its make/break code for that of the left Shift key.

Keyboard Scan Codes (part 2 of 5)

Key no.	Base Case, or Shift +Num Lock make/break	Shift case Make/break	Num Lock on Make/Break
75	E0 70 /E0 F0 70	E0 F0 12 E0 70 /E0 F0 70 E0 12	E0 12 E0 70 /E0 F0 70 E0 F0 12
76	E0 71 /E0 F0 71	E0 F0 12 E0 71 /E0 F0 71 E0 12	E0 12 E0 71 /E0 F0 71 E0 F0 12
79	E0 6B /E0 F0 6B	E0 F0 12 E0 6B /E0 F0 6B E0 12	E0 12 E0 6B /E0 F0 6B E0 F0 12
80	E0 6C /E0 F0 6C	E0 F0 12 E0 6C /E0 F0 6C E0 12	E0 12 E0 6C /E0 F0 6C E0 F0 12
81	E0 69 /E0 F0 69	E0 F0 12 E0 69 /E0 F0 69 E0 12	E0 12 E0 69 /E0 F0 69 E0 F0 12
83	E0 75 /E0 F0 75	E0 F0 12 E0 75 /E0 F0 75 E0 12	E0 12 E0 75 /E0 F0 75 E0 F0 12
84	E0 72 /E0 F0 72	E0 F0 72 E0 72 E0 F0 12 E0 7D	E0 12 E0 72 /E0 F0 72 E0 F0 12
85	E0 7D /E0 F0 7D	E0 F0 12 E0 7D /E0 F0 7D E0 12	E0 12 E0 7D /E0 F0 7D E0 F0 12
86	E0 7A /E0 F0 7A	E0 F0 12 E0 7A /E0 F0 7A E0 12	E0 12 E0 7A /E0 F0 7A E0 F0 12
89	E0 74 /E0 F0 74	E0 F0 12 E0 74 /E0 F0 74 E0 12	E0 12 E0 74 /E0 F0 74 E0 F0 12

Keyboard Scan Codes (part 3 of 5)

Key no.	Scan Code Make/Break	Shift Case Make/Break
95	E0 4A /E0 F0 4A	E0 F0 12 4A/E0 12 F0 4A

Keyboard Scan Codes (part 4 of 5)

Key no.	Scan Code Make/Break	Ctrl Case, Shift Case Make/Break	Alt Case Make/Break
124	E0 12 E0 7C /E0 F0 7C E0 F0 12	E0 7C /E0 F0 7C	84/F0 84

Keyboard Scan Codes (part 5 of 5)

Key no.	Make Code	Ctrl key Pressed
126*	E1 14 77 E1 F0 14 F0 77	E0 7E E0 F0 7E

*This key is not typematic. All associated scan codes occur on the make of the key.

Section 6 : Electrical Characteristics

6.1 Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics. Unless otherwise specified, all voltages are referenced to ground.

If military/ aerospace specified devices are required, contact the sales office/ distributors for availability and specifications.

Table 6-1 Absolute Maximum Ratings

case temperature under bias	0 ^{o}C to 70 ^{o}C
Storage temperature range (TSTG)	-40^{o}C to 125^{o}C
Supply voltage VDD	-0.5V to +7V
Operating supply voltage	4.5V to 5.5V 3.0V to 3.6V
ESD tolerance (CZAP)	100 pF
All input and output voltages with respect to VSS	-0.5V to VCC +0.5V
voltage on any pin with respect to ground	-0.5 V to 7 V (for 5V pins) -0.5 V to 5 V (for 3V pins)
supply voltage with respect to Vss	-0.5 V to 5.5 V (for 5V pins) -0.5 V to 3.6 V (for 3V pins)

Table 6-2 DC Specifications

Vcc_5V = 5V ± 5%, Vcc_3V = 3.3V ± 5%, T_{case} = 0 to +70^{o}C					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
V_{IL}	input low voltage	-	0.8	V	TTL level
V_{IH}	input high voltage	2.0	-	V	TTL level
V_{OL}	output low voltage	-	0.4	V	TTL level, at 8 mA load
V_{OH}	output high voltage	2.4	-	V	TTL level, at 6 mA load (for 3V pins)
I_{LI}	input leakage current	-	0.05	uA	$0 \le V_{IN} \le V_{CC}$, for input without pull up and pull down
I_{IL}	input leakage current	-	400	uA	V_{IN} = 0.45V, for input with pull up
I_{IH}	input leakage current	-	50	uA	V_{IN} = 2.40V, for input with pull down
C_{IN}	input capacitance	-	10	pF	f = 1MHz, Vcc=0V, not 100% tested
C_O	output capacitance	-	10	pF	f = 1MHz, Vcc=0V, not 100% tested

6.2 North Bridge AC Specifications

6.2.1 CPU Interface Timing

Vcc_5V = 5V ± 5%, Vcc_3V = 3.3V ± 5%, T_{case} = 0 to +70^{o}C						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
CPUCLK	CPU operating frequency		100	MHz		
PCICLK	PCI operating frequency		33	MHz		
t_1	ADSJ, WRJ, BEJ[7..0], CACHEJ, MIOJ, HITMJ, DCJ, HLOCKJ, SMIACTJ, setup time to HCLK rising	6		nsec	3	
t_2	ADSJ, HITMJ, WRJ, MIOJ, DCJ, BEJ[7..0], HLOCKJ, CACHEJ, SMIACTJ hold time from HCLK rising	1		nsec	3	
t_3	HA[31..3] setup time to HCLK rising	5		nsec	3	
t_4	HA[31..3] hold time from HCLK rising	1		nsec	3	
t_5	HA[31..3] valid delay from HCLK rising		11	nsec	1	C_L = 30pf
t_6	HA[31..3] float delay from HCLK rising		11	nsec	2	C_L = 30pf
t_7	BRDYJ, NAJ valid delay from HCLK rising		8	nsec	1	C_L = 30pf
t_8	AHOLD valid delay from HCLK rising		7	nsec	1	C_L = 30pf
t_9	BOFFJ valid delay from HCLK rising		8	nsec	1	C_L = 30pf
t_{10}	EADSJ valid delay from HCLK rising		7	nsec	1	C_L = 30pf
t_{11}	KENJ/INV valid delay from HCLK rising		8	nsec	1	C_L = 20pf
t_{12}	HD[63..0] setup time to HCLK rising	5		nsec	3	
t_{13}	HD[63..0] hold time from HCLK rising	1		nsec	3	
t_{14}	HD[63..0] valid delay from HCLK rising		8	nsec	1	C_L = 30pf
t_{15}	HD[63..0] float delay from HCLK rising		8	nsec	2	C_L = 30pf

6.2.2 External Cache Timing

Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{16}	COEJ valid delay from HCLK rising		10	nsec	1	C_L = 60pf
t_{17}	TIO[10..0] valid delay from HCLK rising		10	nsec	1	C_L = 20pf
t_{18}	TIO[10..0] float delay from HCLK rising		10	nsec	2	C_L = 20pf
t_{19}	TIO[10..0] setup time to HCLK rising	6		nsec	3	
t_{20}	TIO[10..0] hold time from HCLK rising	2		nsec	3	
t_{21}	TWEJ valid delay from HCLK rising		8	nsec	1	C_L = 20pf
t_{22}	GWEJ, BWEJ, CCSJ, valid delay from HCLK rising		8	nsec	1	C_L = 60pf
t_{23}	CADSJ valid delay from HCLK rising		8	nsec	1	C_L = 60pf
t_{24}	CADVJ valid delay from HCLK rising		8	nsec	1	C_L = 60pf

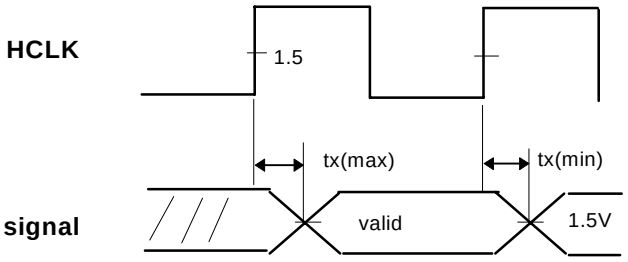
6.2.3 DRAM Interface Timing

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{25}	RASJ[7..0] valid delay from HCLK rising		13	nsec	1	C_L = 150pf
t_{26}	CASJ[7..0] valid delay from HCLK rising		12	nsec	1	C_L = 150pf
t_{27}	MWEJ valid delay from HCLK rising		16	nsec	1	C_L = 150pf
t_{28}	MA[11..2] valid delay from HCLK rising		18	nsec	1	C_L = 300pf
t_{29}	MAA/B[1..0] valid delay from HCLK rising		15	nsec	1	C_L = 150pf
t_{30}	MD[63..0] setup time to HCLK rising	2		nsec	3	
t_{31}	MD[63..0], MPD[7..0] hold time from HCLK rising	3		nsec	3	
t_{32}	MD[63..0], MPD[7..0] valid delay from HCLK rising		8	nsec	1	C_L = 60pf
t_{33}	MD[63..0], MPD[7..0] float delay from HCLK rising		8	nsec	2	C_L = 60pf
t_{34}	MPD[7..0] setup time to HCLK rising	2		nsec	3	

6.2.4 PCI Interface Timing

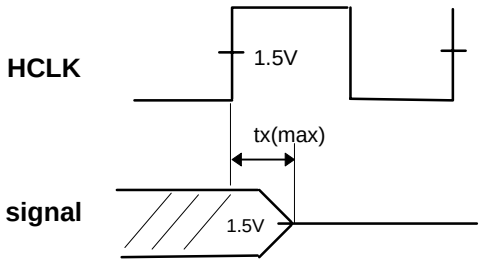
Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{35}	AD[31..0] valid delay from PCICLK rising		14	nsec	4	C_L = 100pf
t_{36}	AD[31..0] float delay from PCICLK rising		14	nsec	5	C_L = 100pf
t_{37}	AD[31..0] setup time to PCICLK rising	7		nsec	6	
t_{38}	AD[31..0] hold time from PCICLK rising	1		nsec	6	
t_{39}	CBEJ[3..0], FRAMEJ, TRDYJ, IRDYJ, STOPJ, LOCKJ, PAR, DEVSELJ valid delay from PCICLK rising		14	nsec	4	C_L = 100pf
t_{40}	CBEJ[3..0], FRAMEJ, TRDYJ, IRDYJ, STOPJ, LOCKJ, PAR, DEVSELJ float delay from PCICLK rising		16	nsec	5	
t_{41}	CBEJ[3..0], FRAMEJ, TRDYJ, IRDYJ, STOPJ, LOCKJ, PAR, DEVSELJ setup time to PCICLK rising	7		nsec	6	
t_{42}	CBEJ[3..0], FRAMEJ, TRDYJ, IRDYJ, STOPJ, LOCKJ, PAR, DEVSELJ hold time from PCICLK rising	1		nsec	6	
t_{43}	PHLDAJ valid delay from PCICLK rising		10	nsec	4	C_L = 20pf
t_{44}	PHLDJ setup time to PCICLK rising	10		nsec	6	
t_{45}	PHLDJ hold time from PCICLK rising	1		nsec	6	
t_{46}	GNT[3..0] valid delay from PCICLK rising		10	nsec	4	C_L = 20pf
t_{47}	REQ[3..0] setup time to PCICLK rising	10		nsec	6	
t_{48}	REQ[3..0] hold time from PCICLK rising	1		nsec	6	

Table 6-3 North Bridge AC Specifications



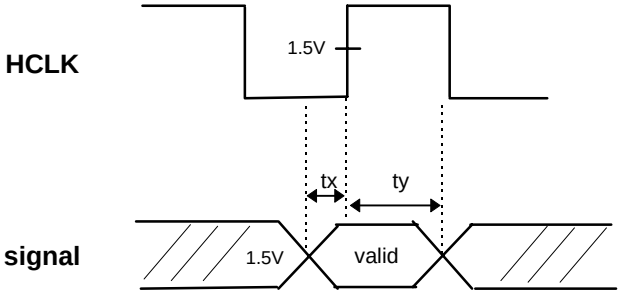
tx = t5, t7, t8, t9, t10, t11, t14, t16, t17, t21, t22, t23,
t24, t25, t26, t27, t28, t29, t32

Fig. 1 : Valid Delay Timings



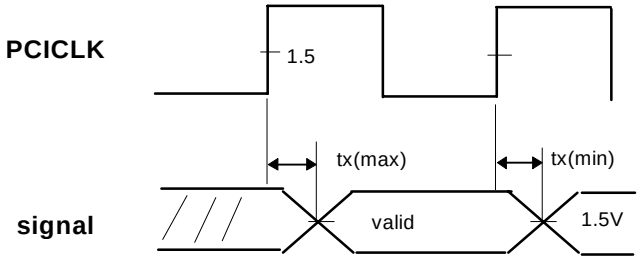
tx = t6,t15,t18,t33

Fig.2 : Float Delay Timings



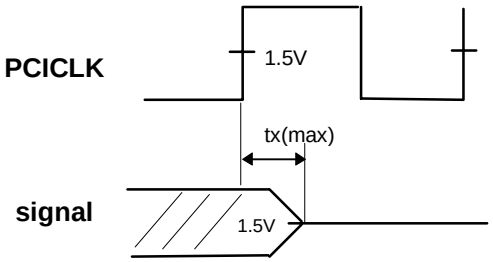
tx = t1, t3, t12, t19, t30, t34
ty = t2, t4, t13, t20, t31

Fig. 3 : Setup and Hold Timings



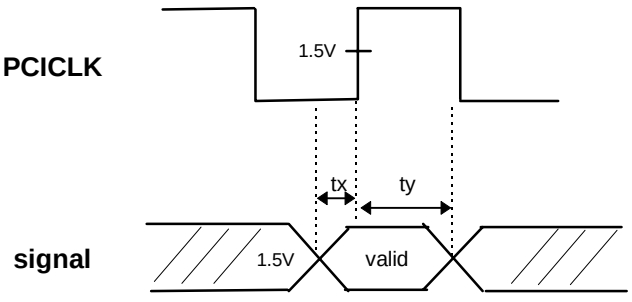
tx = t35,t39,t43,t46

Fig. 4 : Valid Delay Timings



tx = t36, t40

Fig. 5 : Float Delay Timings



tx = t37, t41, t44, t47
ty = t38, t42, t45, t48

Fig. 6 : Setup and Hold Timings

6.3 South Bridge AC Specifications

6.3.1 PCI Interface Timing

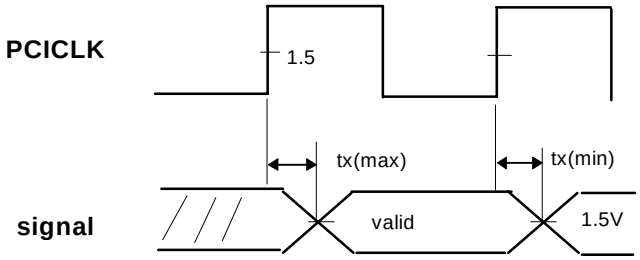
Symbol	Parameter	Min	Max	Unit	Notes
t_{49}	AD[31..0] valid delay	2	11	ns	
t_{50}	AD[31..0] setup time	7		ns	
t_{51}	AD[31..0] hold time	0		ns	
t_{52}	CBEJ[3..0], FRAMEJ, TRDYJ, IRDY, STOPJ, PAR, SERRJ, IDSEL, DEVSELJ valid delay from PCICLK rising	2	11	ns	
t_{53}	CBEJ[3..0], FRAMEJ, TRDYJ, IRDY, STOPJ, PAR, SERRJ, IDSEL, DEVSELJ float delay from PCICLK rising		28	ns	
t_{54}	CBEJ[3..0], FRAMEJ, TRDYJ, IRDY, STOPJ, PAR, SERRJ, IDSEL, DEVSELJ setup time to PCICLK rising	7		ns	
t_{55}	CBEJ[3..0], FRAMEJ, TRDYJ, IRDY, STOPJ, PAR, SERRJ, IDSEL, DEVSELJ hold time from PCICLK rising	0		ns	
t_{56}	PCIRSTJ low pulse width	1		ms	

6.3.2 System Power Management Timing

Symbol	Parameter	Min	Max	Unit	Notes
	SMIJ active pulse width	1		PCICLK	
	SMIJ inactive pulse width	1		PCICLK	
	STPCLKJ inactive pulse width	10		PCICLK	

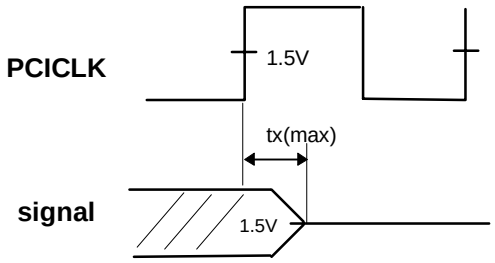
6.3.3 PCI Bus IDE Timing

Symbol	Parameter	Min	Max	Unit	Notes
t_{57}	IDE_D[15..0] valid delay from PCICLK		18	ns	
t_{58}	IDE_D[15..0] setup time to PCICLK	26		ns	
t_{59}	IDE_D[15..0] hold time from PCICLK	14		ns	
t_{60}	IDE_A[2..0] valid delay from PCICLK		13	ns	
t_{61}	IDE_CS1J, IDE_CS3J valid delay from PCICLK rising		13	ns	
t_{62}	IDE_DACK[1..0] valid delay from PCICLK rising		13	ns	



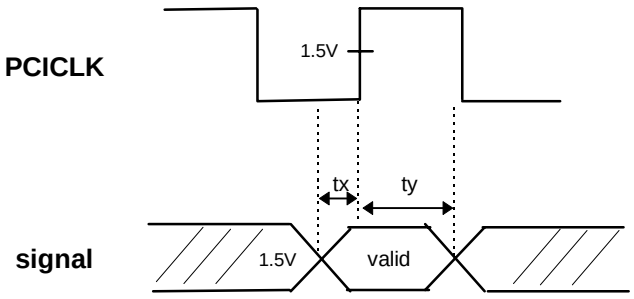
tx = t49,t52,t57,t60,t61,t62

Fig. 7 : Valid Delay Timings



tx = t53

Fig. 8 : Float Delay Timings



tx = t50, t54, t58
ty = t51, t55, t59

Fig. 9 : Setup and Hold Timings

6.4 FDC AC Characteristics

TA = 0^{O}C to +70^{O}C, VDD = +5V ± 10%.

All AC timings can be met with current loads that do not exceed 3.2 mA or -8 uA at 100 pF capacitive loading. For capacitive loads that exceed 100 pF, the following typical derating factors should be used:

100 pF < CL ≤ 150 pF, t = (0.10 ns/pF) (CL - 100 pF) typical
150 pF < CL ≤ 200 pF, t = (0.08 ns/pF) (CL - 100 pF) and
t = (0.5 ns/mA) (ISINK mA) or t = -(0.5 ns/mA) (ISOURCE mA)
tSOURCE is always negative, ISINK ≤ 4.8 mA, ISOURCE ≤ -120 uA, CL ≤ 250 pF.

Table 6-3 lists the AC Characteristics of the M1543C.

Table 6-3 AC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
tAR	Delay from address to RDJ		19		ns
tAW	Delay from address to WRJ		19		ns
tCH	Duration of clock high pulse	see Note A	16		ns
tCL	Duration of clock low pulse	see Note A	16		ns
tDH	Data hold time		10		ns
tDS	Data setup time		19		ns
tHZ	RDJ to floating data delay	see Note B	13		ns
tRA	Address hold time from RDJ		0		ns
tRC	Read cycle update		36		ns
tRD	RDJ strobe width		60		ns
tTPS	Port setup		13		ns
tRI	Read strobe to clear IRQ6		52		ns
tRVD	Delay from RDJ to data		31		ns
tRW	Reset pulse width		100		ns
tWA	Address hold time from WRJ		0		ns
tWC	Write cycle update		36		ns
tWI	Write strobe to clear IRQ6		52		ns
tWO	Write to output		41		ns
tWR	WRJ strobe width		50		ns
RC	Read cycle = tAR + tRD + tRC		115		ns
WC	Write cycle = tAW + tWR + tWC		105		ns

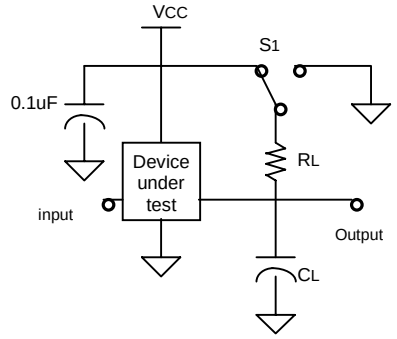
Note: *A. Clock is derived from USB clock/2 (24 MHz maximum).*
B. Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

6.5 AC Test Conditions

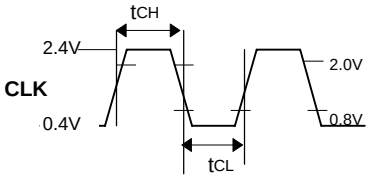
In Table 6-4, CL = 100 pF. This includes jig and scope capacitance. S1 is open for push-pull outputs. S1 is equal to VCC for high impedance to active low, and active low to high impedance measurements. S1 is equal to GND for high impedance to active high, and active high to high impedance measurements. RL = 1.0 kohm for CPU interface pins. For the open drain drive interface pins S1 = VCC and RL = 150 ohms.

Table 6-4 AC Test Conditions

Input pulse levels	GND to 3.0V
Input rise and fall times	6 ns
I/O reference levels	1.3V
Tri-state reference levels	Active high - 0.5V Active low + 0.5V



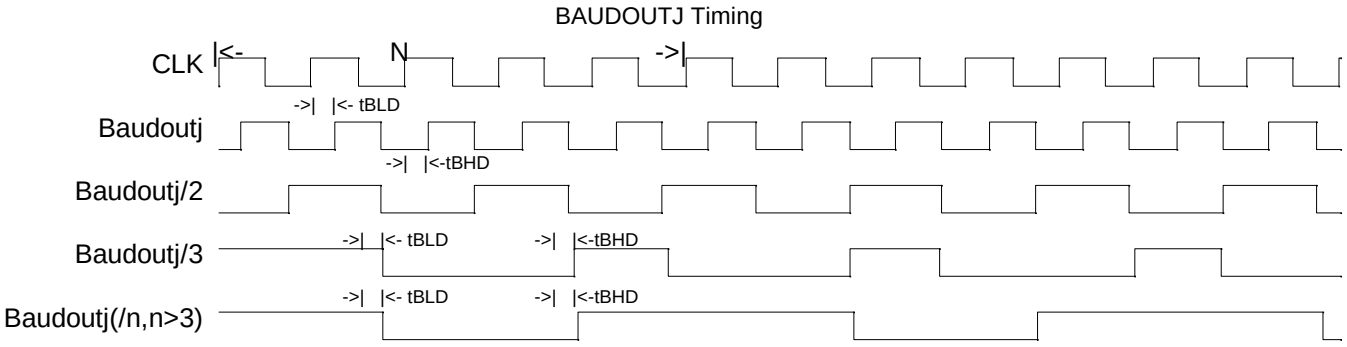
Clock Input = USB clock/2(24 MHz)



The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing

Table 6-5 Serial Interface Baud Generator

Symbol	Parameter	Conditions	Min	Max	Unit
N	Baud Divisor		12^{16} - 1		
tBHD	Baud output positive edge delay	CLK = 24 MHz / 2, 100 pF load		56	ns
tBLD	Baud output negative edge delay	CLK = 24 MHz / 2, 100 pF load		56	ns

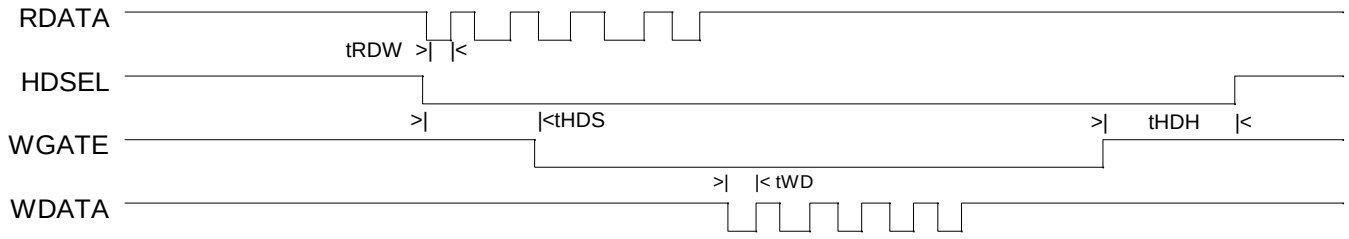


Drive Read and Write Timing

Table 6-6 Drive Read and Write Timing

Symbol	Parameter	Conditions	Min	Unit
tRDW	Read-data pulse-width		25	ns
tWD	Write-data pulse-width	250 kb/s (MFM)	500	ns
tHDS	Head-select setup to write-gate-assertion		40	us
tHDH	Head-select hold from write-gate		12	ns
		300 kb/s (MFM)	416	ns
		500 kb/s (MFM)	250	ns
		1000 kb/s (MFM)	225	ns

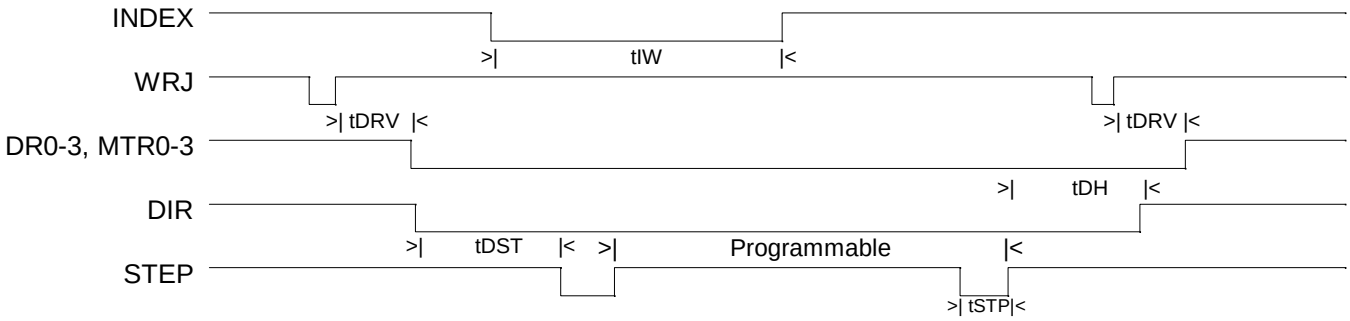
Note : *Whenever WGATE is asserted, the WDATA line is active. At the end of each write, one dummy byte is written before WGATE is deasserted.*



Drive Track Access Timing

Table 6-7 Drive Track Access Timing

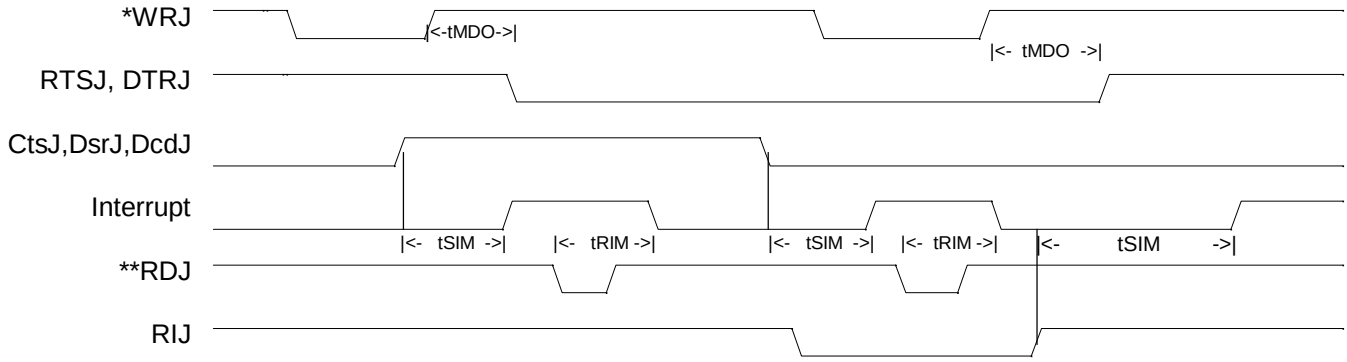
Symbol	Parameter	Min	Max	Unit
tDH	Direction hold from end-of-step	1		step time
tDRV	Drive-select or motor-time from write-strobe		100	ns
tDST	Direction-setup prior to step	6		us
tIW	Index pulse-width	100		ns
tSTP	Step pulse-width	8		us



Modem Control

Table 6-8 Modem Control

Symbol	Parameter	Max	Unit
tMDO	Delay from WRJ (WR MCR) to output	50	ns
tRIM	Delay to reset interrupt from RDJ (RD MSR)	98	ns
tSIM	Delay to set interrupt from modem input	50	ns



* : See Write Cycle Timing ** : See Read Cycle Timing

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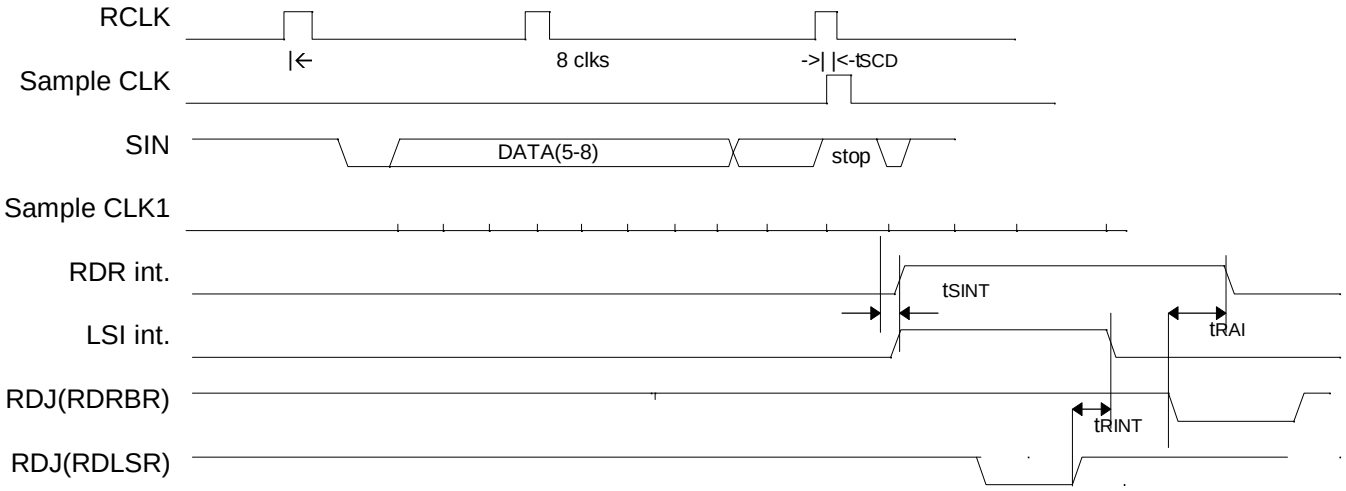
Receiver

Table 6-9 Receiver

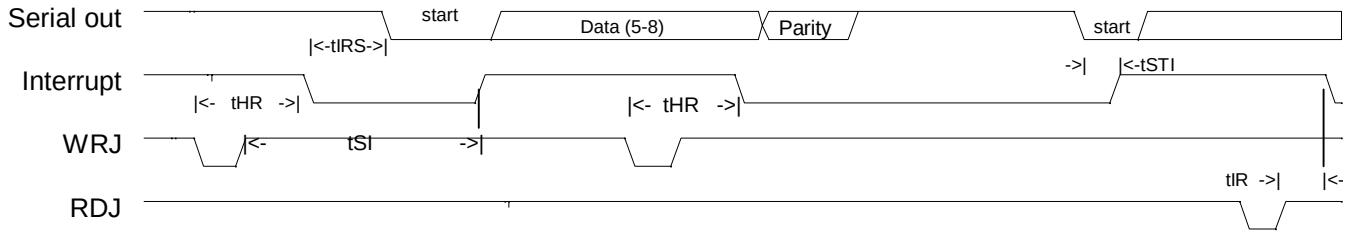
Symbol	Parameter	Max	Unit
t_{RAI}	Delay from active edge of RDJ to reset interrupt	98	ns
t_{RINT}	Delay from inactive edge of RDJ (RD LSR) to reset interrupt	50	ns
t_{SCD}	Delay from RCLK to sample time	41	ns
t_{SINT}	Delay from stop to set interrupt	2	Baudout cycles



Transmitter

Table 6-10 Transmitter

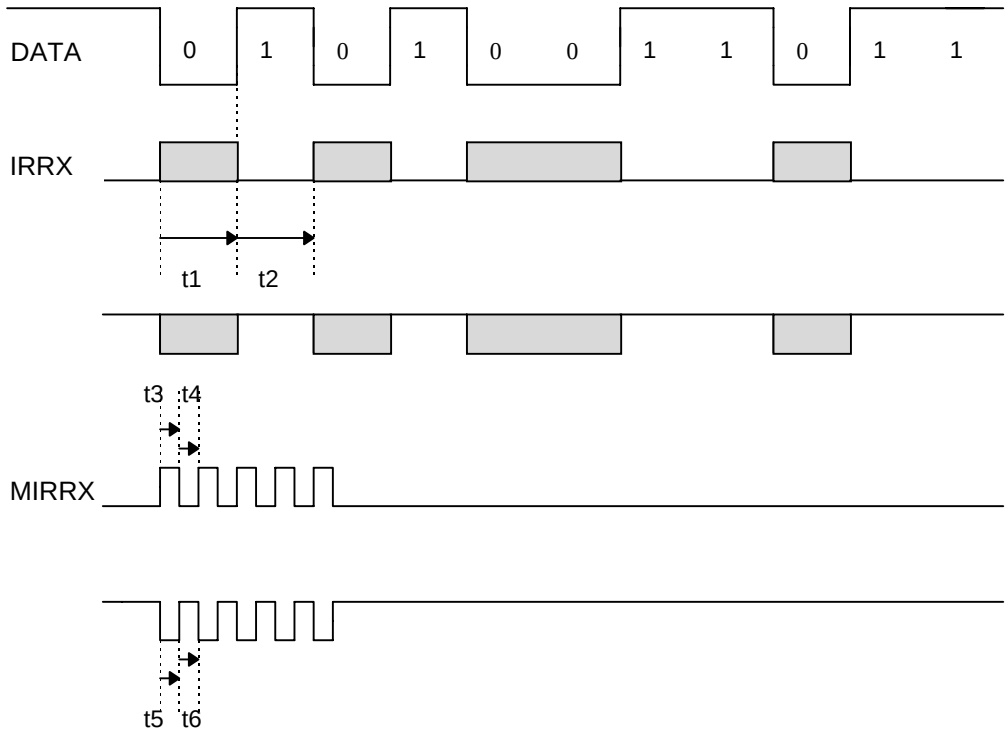
Symbol	Parameter	Min	Max	Unit
tHR	Delay from WRJ (WR THR) to reset interrupt		50	ns
tIR	Delay from RDJ (RD IIR) to reset interrupt (THRE)		50	ns
tIRS	Delay from initial INTR reset to transmit start	8	24	Baudout cycles
tSI	Delay from initial write to interrupt	16	24	Baudout cycles
tSTI	Delay from start to interrupt (THRE)		8	Baudout cycles



Amplitude Shift Keyed IR Receive Timing

Table 6-11. ASK IR Receive Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	Modulated output bit time				us
t2	Off bit time				us
t3	Modulated output "off"	0.8	1	1.2	us
t4	Modulated output "on"	0.8	1	1.2	us
t5	Modulated output "on"	0.8	1	1.2	us
t6	Modulated output "off"	0.8	1	1.2	us



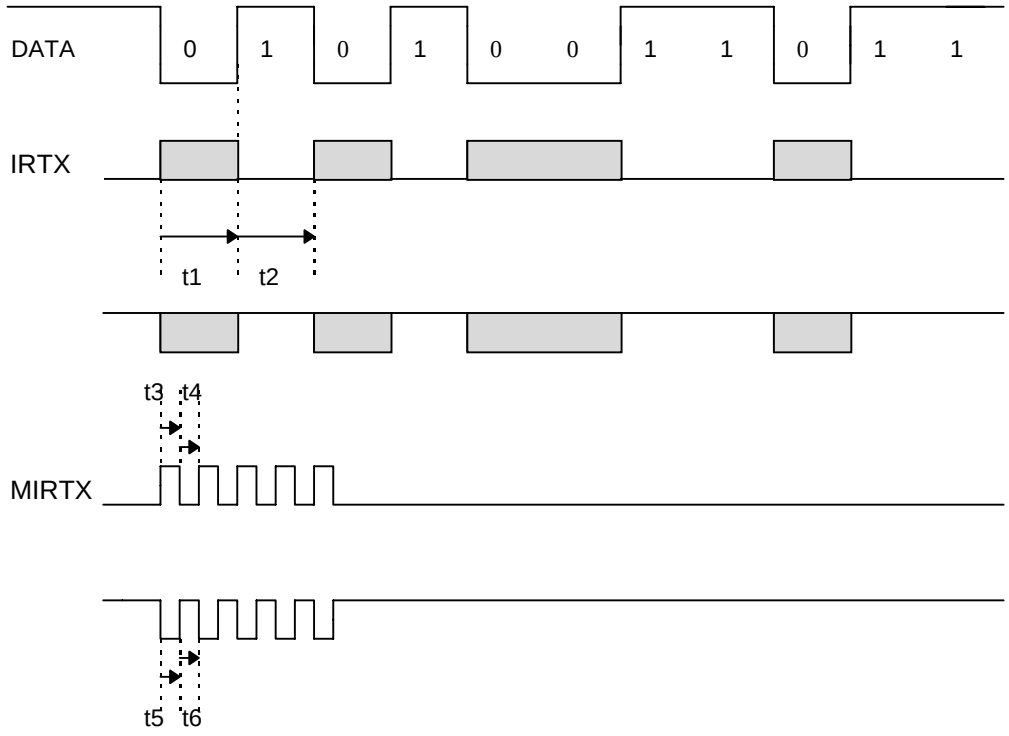
Notes :

1. t1, t2 timing referred to IrDA Receive Timing @ each baud rate.
2. UART1, UART2, UART3 0xF1 bit 0 : 1 = receive active low
   0 = receive active high (default)
3. MIRRX are the modulated outputs. (500k)

Amplitude Shift Keyed IR Transmit Timing

Table 6-12. ASK IR Transmit Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	Modulated output bit time				us
t2	Off bit time				us
t3	Modulated output "off"	0.8	1	1.2	us
t4	Modulated output "on"	0.8	1	1.2	us
t5	Modulated output "on"	0.8	1	1.2	us
t6	Modulated output "off"	0.8	1	1.2	us



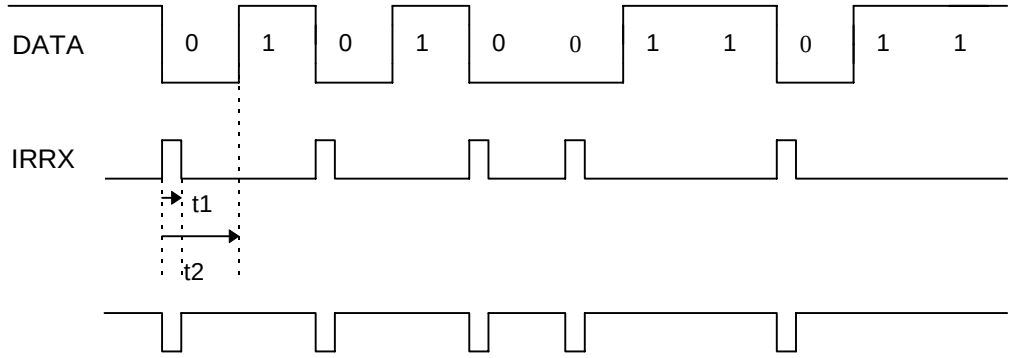
Notes :

1. t1, t2 timing referred to IrDA Transmit Timing @ each baud rate.
2. UART1, UART2, UART3 0xF1 bit 1: 1 = receive active low
   0 = receive active high (default)
3. MIRTX are the modulated outputs. (500k)

IrDA Receive Timing

Table 6-13. IrDA Receive Timing

Symbol	Parameter	Min	Typ	Max	Unit
T1	Pulse width at 115k baud	1.4	1.6	2.71	us
T1	Pulse width at 57.6k baud	1.4	3.22	3.69	us
t1	Pulse width at 38.4k baud	1.4	4.8	5.53	us
t1	Pulse width at 19.2k baud	1.4	9.7	11.07	us
t1	Pulse width at 9.6k baud	1.4	19.5	22.13	us
t1	Pulse width at 4.8k baud	1.4	39	44.27	us
t1	Pulse width at 2.4k baud	1.4	78	88.55	us
t2	Bit time at 115k baud		8.68		us
t2	Bit time at 57.6k baud		17.4		us
t2	Bit time at 38.4k baud		26		us
t2	Bit time at 19.2k baud		52		us
t2	Bit time at 9.6k baud		104		us
t2	Bit time at 4.8k baud		208		us
t2	Bit time at 2.4k baud		416		us



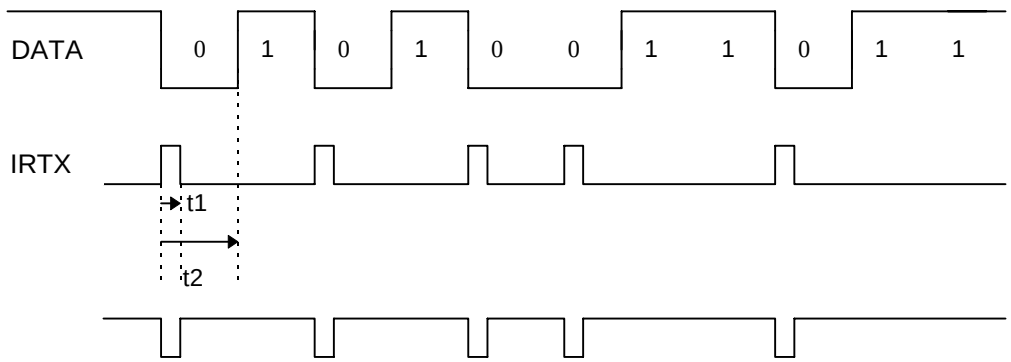
Notes :

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. UART1, UART2, UART3 0xF1 bit 0 : 1 = receive active low
   0 = receive active high (default)

IrDA Transmit Timing

Table 6-14. IrDA Transmit Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	Pulse width at 115k baud	1.4	1.6	2.71	us
t1	Pulse width at 57.6k baud	1.4	3.22	3.69	us
t1	Pulse width at 38.4k baud	1.4	4.8	5.53	us
t1	Pulse width at 19.2k baud	1.4	9.7	11.07	us
t1	Pulse width at 9.6k baud	1.4	19.5	22.13	us
t1	Pulse width at 4.8k baud	1.4	39	44.27	us
t1	Pulse width at 2.4k baud	1.4	78	88.55	us
t2	Bit time at 115k baud		8.68		us
t2	Bit time at 57.6k baud		17.4		us
t2	Bit time at 38.4k baud		26		us
t2	Bit time at 19.2k baud		52		us
t2	Bit time at 9.6k baud		104		us
t2	Bit time at 4.8k baud		208		us
t2	Bit time at 2.4k baud		416		us



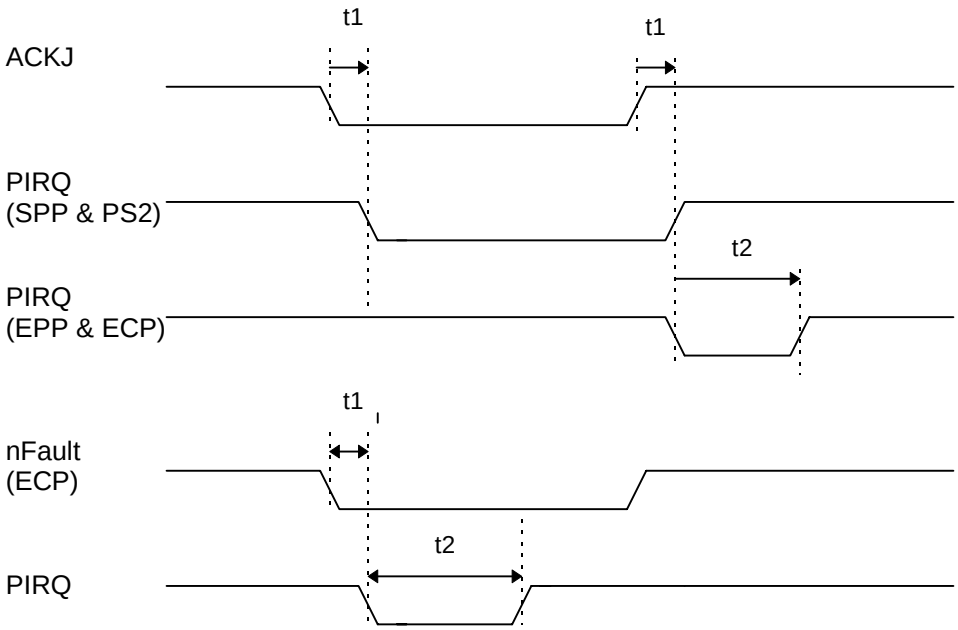
Notes :

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. UART1, UART2, UART3 0xF1 bit 1 : 1 = transmit active low
   0 = transmit active high (default)

Parallel Port Interrupt Timing

Table 6-15. Parallel Port Interrupt Timing

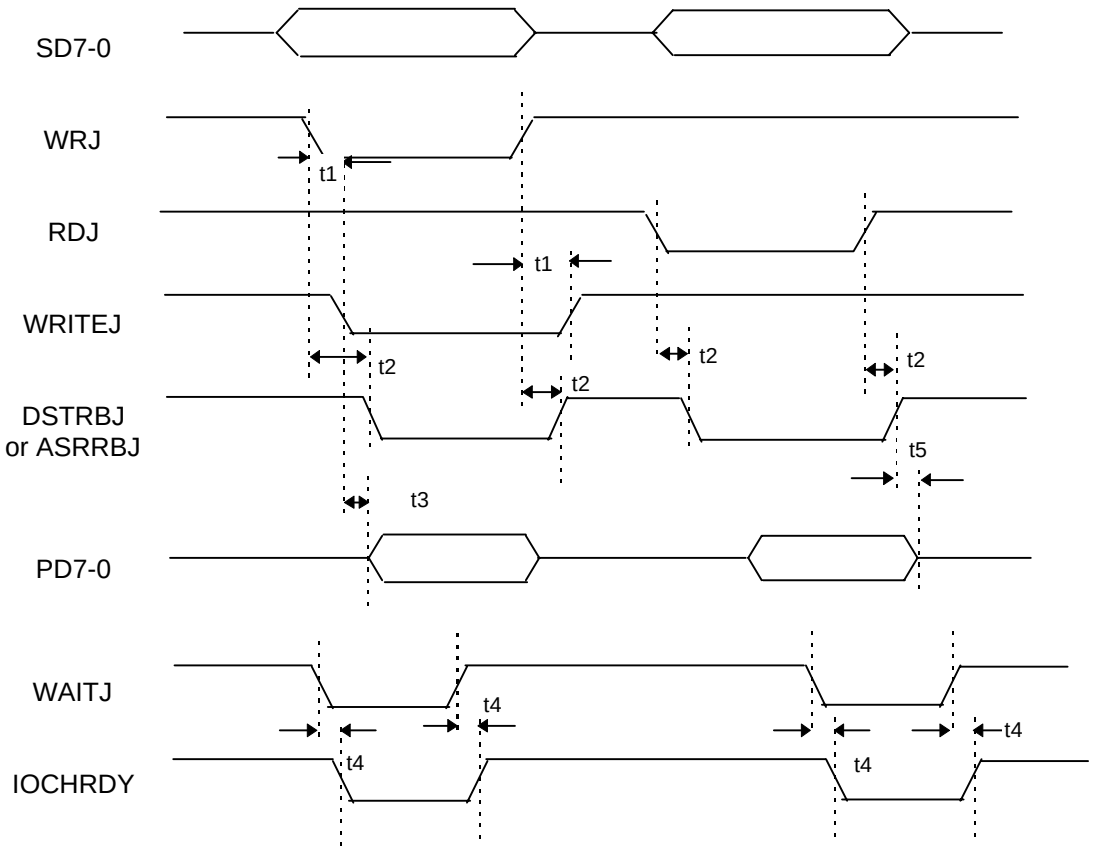
Symbol	Parameter	Min	Typ	Max	Unit
t1	PIRQ delay from ACKJ, nFault			30	ns
t2	PIRQ active in EPP & ECP modes	250		375	ns



EPP Mode Version 1.7 Timing

Table 6-16. EPP Mode Version 1.7 Timing

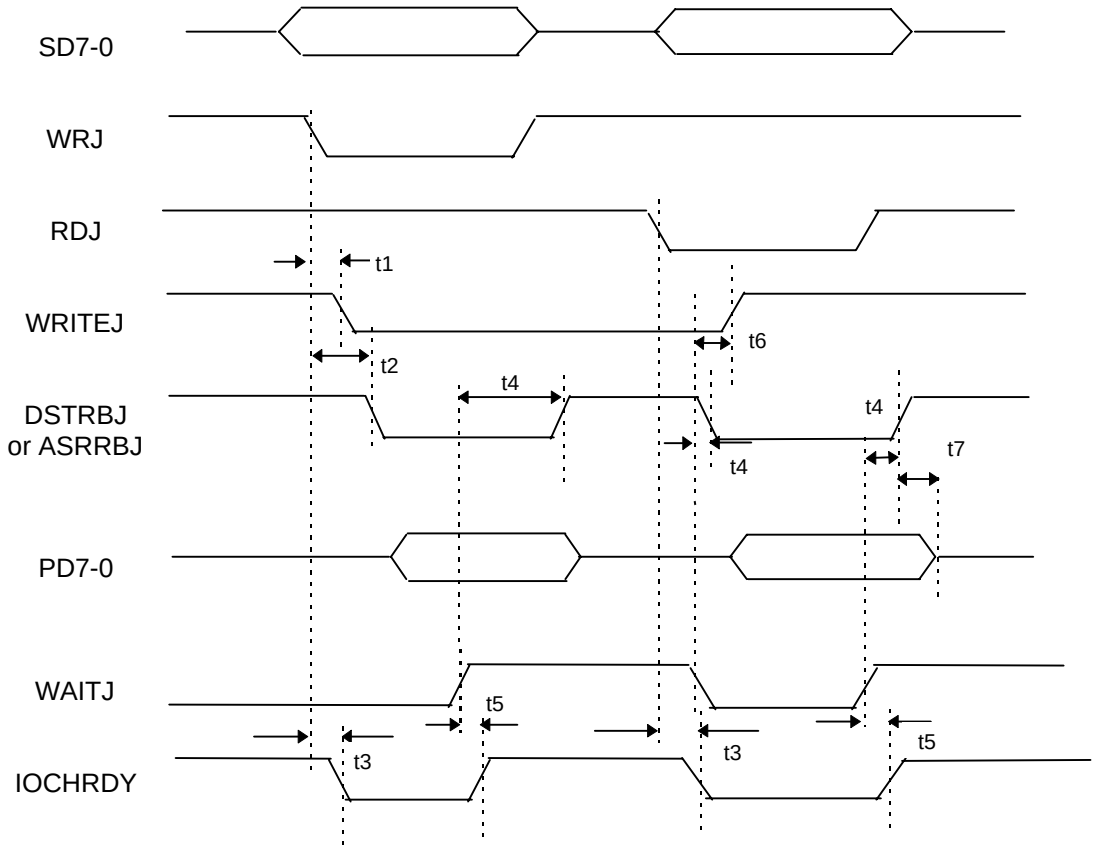
Symbol	Parameter	Min	Typ	Max	Unit
t1	WRJ active to WRITEJ active			95	ns
t2	WRJ active to WRITEJ & DSTRBJ/ASTRBJ active			140	ns
t3	WRITEJ active to PD7-0 valid			40	ns
t4	WAITJ active to IOCHRDYJ active			180	ns
t5	DSTRBJ/ASTRBJ inactive to PD7-0 invalid	90			ns



EPP Mode version 1.9 Timing

Table 6-17. EPP Mode version 1.9 Timing

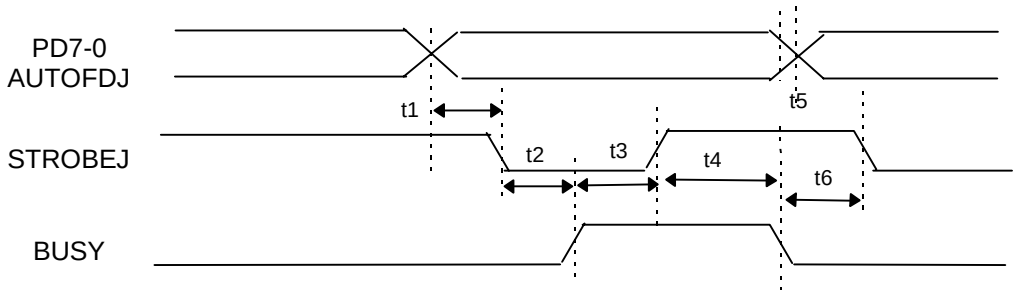
Symbol	Parameter	Min	Typ	Max	Unit
t1	WRJ active to WRITEJ active			95	ns
t2	WRJ active to DSTRBJ/ASTRBJ active			220	ns
t3	WRJ active to IOCHRDY active			180	ns
t4	WAITJ inactive to DSTRBJ/ASTRBJ inactive			700	ns
t5	WAITJ inactive to IOCHRDYJ inactive			180	ns
t6	WAITJ active to WRITEJ inactive			180	ns
t7	DSTRBJ/ASTRBJ inactive to PD7-0 invalid	90			ns



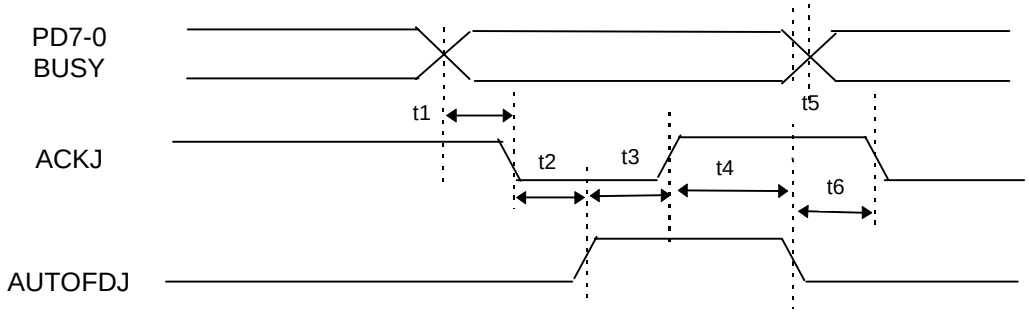
ECP Mode Timing

Table 6-18. ECP Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	DATA valid to STROBEJ active	0			ns
t2	STROBEJ active to BUSY active	0		130	ns
t3	BUSY active to STROBEJ inactive	75			ns
t4	STROBEJ inactive to BUSY inactive	0		135	ns
t5	BUSY inactive to DATA update	0		1.1	us
t6	BUSY inactive to STROBEJ active	0			ns



ECP Forward Timing Diagram

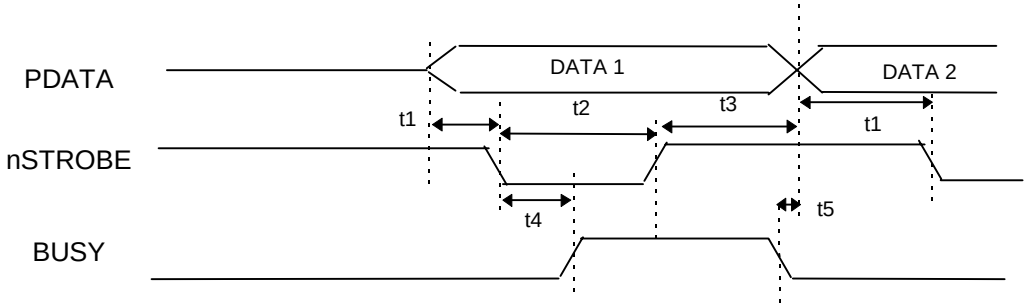


ECP Backward Timing Diagram

Compatible FIFO Mode Timing

Table 6-19. Compatible FIFO Mode Timing

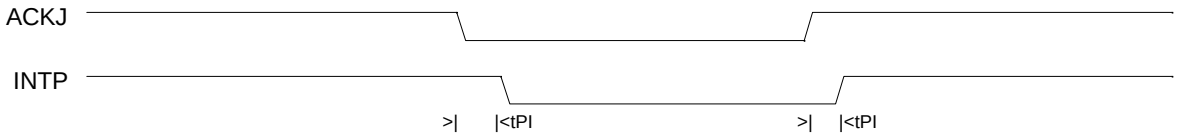
Symbol	Parameter	Min	Typ	Max	Unit
t1	Data valid to nSTROBE active		500		ns
t2	nSTROBE active pulse width		500		ns
t3	Data hold from nSTROBE inactive		500		ns
t4	nSTROBE active to BUSY active		500		ns
t5	BUSY inactive to PDATA TRANSING	80			ns



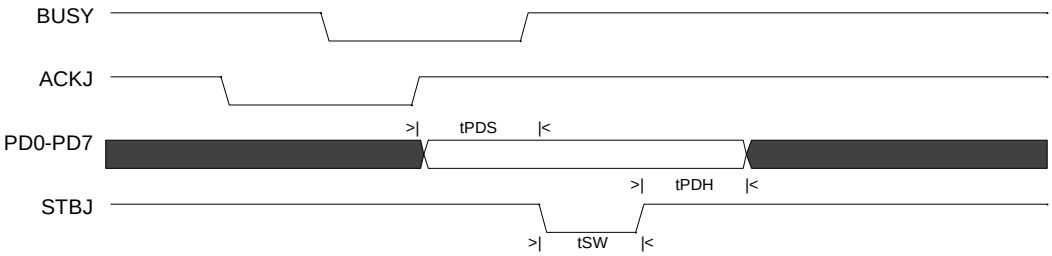
Parallel Interface

Table 6-20. Parallel Interface

Symbol	Parameter	Min	Max	Unit
tPDH	Port data hold	500		ns
tPDS	Port data setup	500		ns
tPI	Port interrupt	33		ns
tSW	Strobe width	500		ns



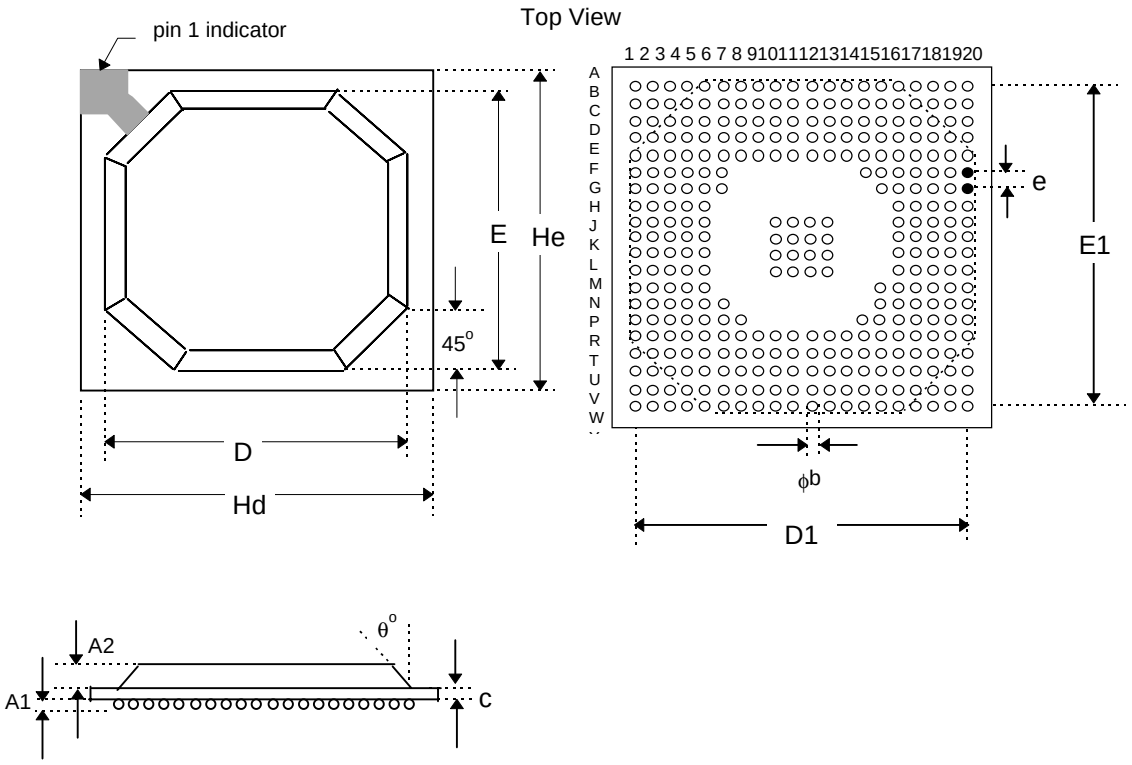
Interrupt Timing



Typical Peripheral Data Exchange

Section 7 : Packaging Information

328L BGA Dimension Spec (27 x 27 mm)



Symbol	Min.	Nom.	Max.
A1	0.55	0.60	0.65
A2	1.12	1.17	1.22
ϕb	0.60	0.75	0.90
c	0.51	0.56	0.61
D	23.80	24.00	24.20
D1	23.93	24.13	24.33
E	23.80	24.00	24.20
E1	23.93	24.13	24.33
e		1.27	
Hd	26.80	27.00	27.20
He	26.80	27.00	27.20
θ°	23°	30°	37°
Y (radius of ball)			0.25

Section 8 : Revision History

p.61,71,83,145,146,147,154, 155		05/08/98		
p.199-219, 257-259, 268		05/11/98		
p.242-244,246-248,253,256,258		06/01/98		
p.2,6,11,18,20,21,22,24,27,44,52,61-63,65,70,77,83,122-123,134,137,145,148,152,153,155,156,165-168,170, 178-191(Operational Registers,Legacy Support I/F,Legacy Prog.) 203,205-209,220,223,228, (277)293, 296-303(Keyboard Scan /Make Codes) (298)320-(300)322,(305)326	v1.0	06/26/98	CCKuo	

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