VT8371

KX133 Athlon™ North Bridge

Single-Chip North Bridge
for Slot-A Based Athlon™ CPUs
with 200 MHz Front Side Bus
for Desktop PC Systems
with AGP4x and PCI
plus Advanced ECC Memory Controller
supporting PC133 / PC100 SDRAM & VCM

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REVISION HISTORY

Document Release	Date	Revision	Initials
0.1	4/12/99	Initial internal release	DH
0.2	6/14/99	Updated feature bullets, overview and pin descriptions Added ballout per engineering document revision 0.2 Added registers from 694X data sheet rev 0.61 (bank ending addresses fixed) Updated package mechanical to 510 BGA	EC DH
0.21	6/17/99	Fixed formatting problems on electrical specs page	DH
0.3	7/2/99	Updated feature bullets, overview, and block diagram Updated pinouts (changed CPU interface and some DRAM data & AGP pins) Updated package mechanical to BGA512 Updated register specs to reflect K7 register set (rev 0.2 was a copy of 694X)	DH
0.41	7/13/99	Fixed pinout errors in center VCC/GND and changed AGP & MD areas Fixed strap options Fixed device 0 registers Rx58-59, 61-63, 69, 7B, AC, AE, B4 Updated mechanical specs to 516 BGA	DH
0.5	7/20/99	Fixed typographical error in feature bullets regarding package pin count Fixed formatting errors in page footer revision numbers and document date Updated pinouts per engineering ballout rev 0.6: swapped PWROK & WSC# Updated pinouts per engineering ballout rev 0.7: swapped D37# and VTT Changed Device 0 and Device 1 Rx2 Device ID values Fixed Device 0 Rx10[27-20] typographical error, Rx88[2] bit function, and RxA0 and RxA4 default values (typographical errors)	DH
0.51	7/22/99	Fixed Device 0 Rx54[0] bit definition and Device 1 Rx2 Device ID Added Device 0 RxC0-C7 Power Management registers	DH
0.6	8/26/99	Fixed GCKRUN# pin direction Added strap to register cross references to MAA/MAB pin descriptions Device 0 Fixed Rx3-2 (Device ID), 52[3], 68[0], 76[3-0], 7B[1], F0-F7 Fixed RxB4[3-2] strapping & RxB5[7,3] polarity; added RxB4-5 defaults Device 1 Fixed Rx3-2 (Device ID), 1F-1E, Rx40[3], 42[4, 0], 44[4-1], 82[5], 83[2-1]	DH
1.0	11/1/99	Changed “K7” to Athlon” and reworded document title Changed feature bullets in DRAM controller section Removed “NDA Required” disclaimer (product announced) Fixed minor typo in pinout table (pin lists and descriptions were correct) Added Device 0 Rx55[1], moved Device 0 registers RxB4-B6 to B3-B5	DH
1.01	1/7/00	Removed “Socket-462” from description (chip is optimized for Slot-A) Updated VIA Logo to “Delivering Value” format	DH
1.02	1/17/00	Fixed typos in DRAM controller feature bullets and Device 0 RxB2[0]	DH

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- **High Performance and High Integration Athlon AGP 4x / PC133 Chipset with Advanced System Power Management**
  - **KX133** Chipset: **VT8371** system controller and **VT82C686A** PCI to ISA bridge
  - Single chip Athlon system controller with 64-bit Slot-A / Athlon CPU, 64-bit system memory, 32-bit PCI and 32-bit AGP interfaces
  - PCI-to-ISA bridge chip includes UltraDMA-33/66 EIDE, 4 USB Ports, Integrated Super-I/O, AC97 / MC97 link (for Audio and Modem support), Hardware Monitoring, Power Management, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip
  - Supports separately powered 3.3V (5V tolerant) interface to system memory, AGP, and PCI bus
  - Modular power management and clock control for advanced system power management
- **High Performance Athlon CPU Interface**
  - Supports Slot-A (AMD Athlon) processors
  - HSTL-like 1.5V high-speed transceiver logic signal levels
  - Support independent address, data, and snoop interfaces
  - 100 MHz DDR (Double Data Rate) transfer on Athlon CPU address and data buses
  - Built-in PLL (Phase Lock Loop) circuitry for optimal skew control within and between clocking regions
  - Four-entry command queue to accommodate maximum CPU throughput
  - Four-entry probe queue to stores probes from the system to the processor
  - Twenty four-entry processor system data and control queue to store system data control commands in two separate read and write buffers for data movement in and out of processor interface
  - Supports WC (Write Combining) cycles
  - Sleep mode support
  - System management interrupt, memory remap and STPCLK mechanism

- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - Synchronous and pseudo-synchronous with the host CPU bus with optimal skew control

PCI	AGP	CPU	Mode
33 MHz	66 MHz	100 MHz DDR	3x synchronous

  - AGP v2.0 compliant
  - Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
  - Supports 66 MHz 1x, 2x and 4x modes for AD and SBA signaling
  - Pipelined split-transaction long-burst transfers up to 1GB/sec
  - Thirty-two level read request queue
  - Four level posted-write request queue
  - Thirty-two level (quadwords) read data FIFO (256 bytes)
  - Sixteen level (quadwords) write data FIFO (128 bytes)
  - Intelligent request reordering for maximum AGP bus utilization
  - Supports Flush/Fence commands
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme
  - Windows 95 OSR-2 VXD and integrated Windows 98 / Windows 2000 miniport driver support
- **Concurrent PCI Bus Controller**
  - PCI buses are synchronous / pseudo-synchronous to host CPU bus
  - 33 MHz operation on the primary PCI bus
  - 66 MHz PCI operation on the AGP bus
  - PCI-to-PCI bridge configuration on the 66MHz PCI bus
  - Supports up to five PCI masters
  - Peer concurrency
  - Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
  - Zero wait state PCI master and slave burst transfer rate
  - PCI to system memory data streaming up to 132Mbyte/sec
  - Two lines (32 double-words) of CPU to PCI posted write buffers
  - Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
  - Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
  - Thirty-two levels (double-words) of post write buffers from PCI masters to DRAM
    (two cache lines / 16 double-words for PCI bus, two cache lines / 16 double-words for Athlon processor interface)
  - Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
  - Delay transaction from PCI master accessing DRAM
  - Read caching for PCI master reading DRAM
  - Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
  - Symmetric arbitration between Host/PCI bus for optimized system performance
  - Complete steerable PCI interrupts
  - PCI-2.2 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

- **Advanced High-Performance DRAM Controller**
  - Supports PC133 and PC100 SDRAM and Virtual Channel Memory (VCM) SDRAM up to 4 DIMMs
  - Concurrent CPU, AGP, and PCI access
  - Different DRAM types may be used in mixed combinations
  - Different DRAM timing for each bank
  - Dynamic Clock Enable (CKE) control for SDRAM power reduction in high speed systems
  - Mixed 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs
  - Support up to 2.0 GB memory space (256Mb DRAM technology)
  - Flexible row and column addresses
  - 64-bit data width and 3.3V DRAM interface
  - Programmable I/O drive capability for MA, command, and MD signals
  - Dual copies of MA signals for improved drive
  - Optional bank-by-bank ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
  - Two-bank interleaving for 16Mbit SDRAM support
  - Two-bank and four bank interleaving for 64Mbit SDRAM support
  - Supports maximum 16-bank interleave (i.e., 16 pages open simultaneously); banks are allocated based on LRU
  - Independent SDRAM control for each bank
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
  - Four cache lines (32 quadwords) of CPU to DRAM write buffers
  - Four cache lines (32 quadwords) of CPU to DRAM read prefetch buffers
  - Read around write capability for non-stalled CPU read
  - Burst read and write operation
  - BIOS shadow at 16KB increment
  - Decoupled and burst DRAM refresh
  - CAS before RAS or self refresh
- **Advanced System Power Management Support**
  - Dynamic power down of SDRAM (CKE)
  - PCI and AGP bus clock run and clock generator control
  - VTT suspend power plane preserves memory data
  - Suspend-to-DRAM and Self-Refresh operation
  - SDRAM self-refresh power down
  - 8 bytes of BIOS scratch registers
  - Low-leakage I/O pads
- **Built-in NAND-tree pin scan test capability**
- **3.3V, 0.35um, high speed / low power CMOS process**
- **35 x 35 mm, 516 pin BGA Package**

OVERVIEW

The **KX133 / VT8371 and VT82C686A** chipset is a high performance, cost-effective and energy efficient system controller for the implementation of AGP / PCI / ISA desktop personal computer systems based on 64-bit Slot-A (AMD Athlon) processors.

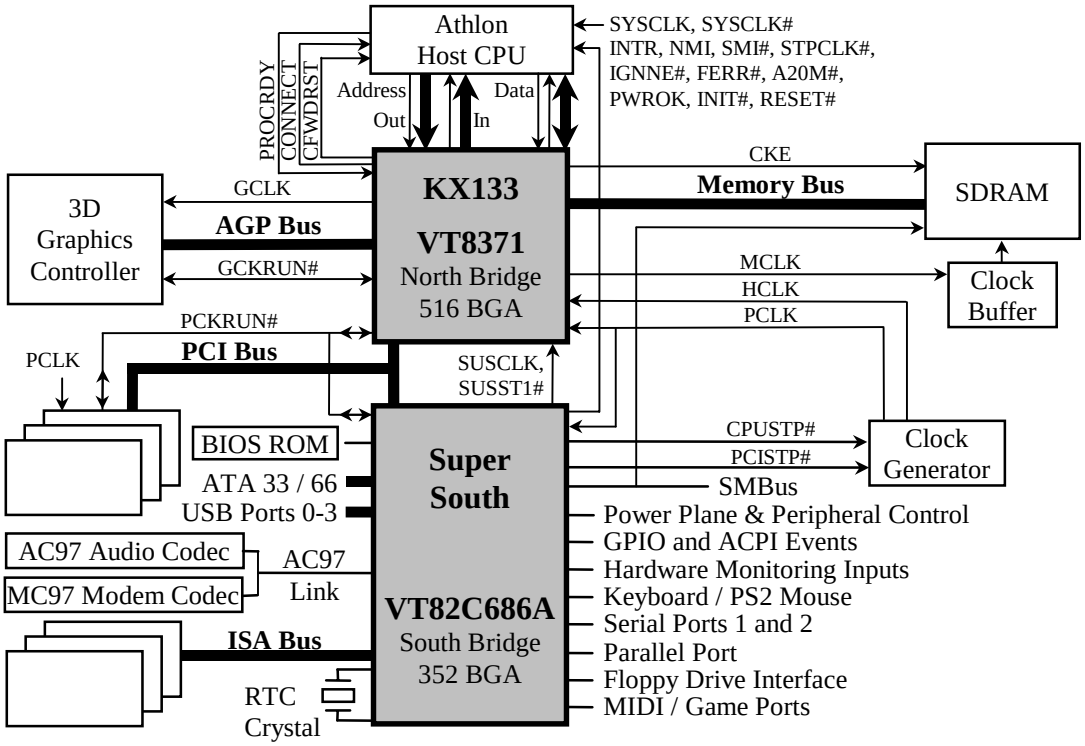

Figure 1. KX133 System Block Diagram Using the VT82C686A South Bridge

The KX133 chip set consists of the VT8371 system controller (516 pin BGA) and the VT82C686A PCI to ISA bridge (352 pin BGA). The system controller provides superior performance between the CPU, DRAM, AGP bus, and PCI bus with pipelined, burst, and concurrent operation.

The VT8371 supports eight banks of DRAMs up to 2.0 GB. The DRAM controller supports standard Synchronous DRAM (SDRAM) and Virtual Channel SDRAM (VC SDRAM), in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 66/100/133 MHz. The eight banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability separately selectable on a bank-by-bank basis.

The VT8371 system controller also supports full AGP v2.0 capability for maximum bus utilization including 1x, 2x and 4x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / Windows 2000 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

The VT8371 supports two 32-bit 3.3 / 5V system buses (one AGP and one PCI) that are synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent

PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1/L2 write-back forward to PCI master, and L1/L2 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The 352-pin Ball Grid Array VT82C686A PCI to ISA bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT82C686A also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-33/66 for 33/66 MB/sec transfer rate, integrated USB interface with root hub and four function ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface. The VT82C686A also includes an AC97 / MC97 link for interface to external audio and modem codecs, and all “Super-I/O” functions (serial ports, parallel port, and floppy drive interface and game port).

For sophisticated power management, KX133 provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. The VT82C686A also includes a complete hardware monitoring subsystem for monitoring and control of internal and external (motherboard and system) conditions including voltages, temperatures, fan speeds, switch open/close states, etc. Coupled with the VT82C686A south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

The KX133 chipset is ideal for high performance, high quality, high energy efficient and high integration desktop AGP / PCI / ISA computer systems.