



IT8700F

Simple Low Pin Count Input / Output (Simple LPC I/O)

Preliminary Specification V0.1



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CONTENTS

1. Features	1
2. General Description	3
3. Block Diagram	5
4. Pin Configuration	7
5. IT8700F Pin Descriptions	11
6. List of GPIO Pins	21
7. Power On Strapping Options	25
8. Configuration	27
8.1 Configuring Sequence Description	27
8.2 Description of the Configuration Registers	28
8.2.1 Logical Device Base Address	34
8.3 Global Configuration Registers (LDN: All)	35
8.3.1 Configure Control (Index=02h)	35
8.3.2 Logical Device Number (LDN, Index=07h)	35
8.3.3 Chip ID Byte 1 (Index=20h, Default=87h)	35
8.3.4 Chip ID Byte 2 (Index=21h, Default=05h)	35
8.3.5 Configuration Select and Chip Version (Index=22h, Default=02h)	35
8.3.6 Software Suspend (Index=23h, Default=00h)	35
8.3.7 Clock Selection and Flash ROM I/F Control Register (Index=24h, Default=sssss000b)	36
8.3.8 GPIO Set 1 Multi-Function Pin Selection Register (Index=25h, Default=00h)	36
8.3.9 GPIO Set 2 Multi-Function Pin Selection Register (Index=26h, Default=00h)	37
8.3.10 GPIO Set 3 Multi-Function Pin Selection Register (Index=27h, Default=00h)	37
8.3.11 GPIO Set 4 Multi-Function Pin Selection Register (Index=28h, Default=FFh)	38
8.3.12 GPIO Set 5 Multi-Function Pin Selection Register (Index=29h, Default=E0h)	39
8.3.13 GPIO Set 6 Multi-Function Pin Selection Register (Index=2Ah, Default=FFh)	40
8.3.14 Test Mode Register 1 (Index=2Eh, Default=00h)	40
8.3.15 Test Mode Register 2 (Index=2Fh, Default=00h)	40
8.4 FDC Configuration Registers (LDN=00h)	41
8.4.1 FDC Activate (Index=30h, Default=00h)	41
8.4.2 FDC Base Address MSB Register (Index=60h, Default=03h)	41
8.4.3 FDC Base Address LSB Register (Index=61h, Default=F0h)	41
8.4.4 FDC Interrupt Level Select (Index=70h, Default=06h)	41
8.4.5 FDC DMA Channel Select (Index=74h, Default=02h)	41
8.4.6 FDC Special Configuration Register 1 (Index=F0h, Default=00h)	42
8.4.7 FDC Special Configuration Register 2 (Index=F1h, Default=00h)	42
8.5 Serial Port 1 Configuration Registers (LDN=01h)	42
8.5.1 Serial Port 1 Activate (Index=30h, Default=00h)	42
8.5.2 Serial Port 1 Base Address MSB Register (Index=60h, Default=03h)	42
8.5.3 Serial Port 1 Base Address LSB Register (Index=61h, Default=F8h)	43
8.5.4 Serial Port 1 Interrupt Level Select (Index=70h, Default=04h)	43
8.5.5 Serial Port 1 Special Configuration Register (Index=F0h, Default=00h)	43
8.6 Serial Port 2 Configuration Registers (LDN=02h)	43
8.6.1 Serial Port 2 Activate (Index=30h, Default=00h)	43
8.6.2 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h)	43
8.6.3 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h)	44
8.6.4 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h)	44
8.6.5 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h)	44
8.6.6 Serial Port 2 Special Configuration Register 2 (Index=F1h, Default=50h)	44
8.6.7 Serial Port 2 Special Configuration Register 3 (Index=F2h, Default=00h)	45

8.6.8	Serial Port 2 Special Configuration Register 4 (Index=F3h, Default=7Fh)	45
8.7	Parallel Port Configuration Registers (LDN=03h).....	45
8.7.1	Parallel Port Activate (Index=30h, Default=00h)	45
8.7.2	Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h)	45
8.7.3	Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h)	46
8.7.4	Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h)	46
8.7.5	Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h).....	46
8.7.6	POST Data Port Base Address MSB Register (Index=64h, Default=00h)	46
8.7.7	POST Data Port Base Address LSB Register (Index=65h, Default=80h).....	46
8.7.8	Parallel Port Interrupt Level Select (Index =70h, Default=07h).....	46
8.7.9	Parallel Port DMA Channel Select (Index=74h, Default=03h)	47
8.7.10	Parallel Port Special Configuration Register (Index=F0h, Default=03h).....	47
8.8	FAN Controller Configuration Registers (LDN=04h).....	47
8.8.1	FAN Controller Activate Register (Index=30h, Default=00h)	47
8.8.2	FAN Controller Primary Base Address MSB Register (Index=60h, Default=02h).....	47
8.8.3	FAN Controller Primary Base Address LSB Register (Index=61h, Default=90h).....	47
8.8.4	PME Direct Access Base Address MSB Register (Index=62h, Default=02h).....	48
8.8.5	PME Direct Access Base Address LSB Register (Index=63h, Default=30h).....	48
8.8.6	FAN Controller Interrupt Level Select (Index=70h, Default=09h)	48
8.8.7	PME Event Enable Register (Index=F0h, Default=00h).....	48
8.8.8	PME Status Register (Index=F1h, Default=00h)	49
8.8.9	PME Control Register 1 (PCR 1) (Index=F2h, Default=00h).....	49
8.8.10	FAN Controller Special Configuration Register (Index=F3h, Default=00h).....	49
8.8.11	PME Control Register 2 (PCR2) (Index=F4h, Default=00h).....	49
8.8.12	PME Special Code Index Register (Index=F5h).....	49
8.8.13	PME Special Code Data Register (Index=F6h)	50
8.9	GPIO Configuration Registers (LDN=05h).....	50
8.9.1	Simple I/O Base Address MSB Register (Index=60h, Default=00h).....	50
8.9.2	Simple I/O Base Address LSB Register (Index=61h, Default=00h).....	50
8.9.3	Panel Button De-bounce Base Address MSB Register (Index=62h, Default=00h)	50
8.9.4	Panel Button De-bounce Base Address LSB Register (Index=63h, Default=00h).....	50
8.9.5	SMI# Normal Run Access Base Address MSB Register (Index=64h, Default=00h)	50
8.9.6	SMI# Normal Run Access Base Address LSB Register (Index=65h, Default=00h)	50
8.9.7	Panel Button De-bounce Interrupt Level Select Register (Index=70h, Default=00h)	51
8.9.8	IRQ Routing Input 0 and 1 Interrupt Level Select Register (Index=71h, Default=00h).....	51
8.9.9	IRQ Routing Input 2 and 3 Interrupt Level Select Register (Index=72h, Default=00h).....	51
8.9.10	GPIO Pin Set 1, 2, 3, 4, 5 and 6 Polarity Registers (Index=B0h, B1h, B2h, B3h, B4h and B5h, Default=00h)	51
8.9.11	GPIO Pin Set 1, 2, 3, 4, 5 and 6 Pin Internal Pull-up Enable Registers (Index=B8h, B9h, BAh, BBh, BCh and BDh, Default=00h).....	52
8.9.12	Simple I/O Set 1, 2, 3, 4, 5 and 6 Enable Registers (Index=C0h, C1h, C2h, C3h,C4h and C5h, Default=00h).....	52
8.9.13	Simple I/O Set 1, 2, 3, 4, 5 and 6 Output Enable Registers (Index=C8h,C9h,CAh,CBh,CCCh and CDh, Default=00h)	52
8.9.14	Panel Button De-bounce Control Register (Index=D0h, Default=00h)	52
8.9.15	Panel Button De-bounce Set 1, 2, 3, 4, 5 and 6 Enable Registers (Index=D1h, D2h, D3h, D4h, D5h and D6h, Default=00h)	53
8.9.16	SMI# Control Register (Index=F0h, Default=00h)	53
8.9.17	SMI# Status Register (Index=F2h, Default=00h).....	53
8.9.18	SMI# Pin Mapping Register (Index=F5h, Default=00h)	54
8.9.19	FAN Controller Alert Beep Pin Mapping Register (Index=F6h, Default=00h)	54
8.9.20	GP LED Blinking 1 Pin Mapping Register (Index=F7h, Default=00h).....	54
8.9.21	GP LED Blinking 1 Control Register (Index=F8h, Default=00h).....	54



8.9.22	GP LED Blinking 2 Pin Mapping Register (Index=F9h, Default=00h).....	54
8.9.23	GP LED Blinking 2 Control Register (Index=FAh, Default=00h)	55
8.9.24	Watch Dog Timer Control Register (Index=FBh, Default=00h)	55
8.9.25	Watch Dog Timer Time-out Output Pin Mapping Register (Index=FCh, Default=00h).....	55
8.9.26	Watch Dog Timer Time-out Value Register (Index=FDh, Default=00h).....	55
8.9.27	VID Input Register (Index=FEh, Default= --)	56
8.9.28	VID Output Register (Index=FFh, Default=00h)	56
8.10	Game Port Configuration Registers (LDN=06h).....	56
8.10.1	Game Port Activate (Index=30h, Default=00h).....	56
8.10.2	Game Port Base Address MSB Register (Index=60h, Default=02h).....	56
8.10.3	Game Port Base Address LSB Register (Index=61h, Default=01h).....	56
8.11	Consumer IR Configuration Registers (LDN=07h)	56
8.11.1	Consumer IR Activate (Index=30h, Default=00h)	56
8.11.2	Consumer IR Base Address MSB Register (Index=60h, Default=03h)	57
8.11.3	Consumer IR Base Address LSB Register (Index=61h, Default=10h)	57
8.11.4	Consumer IR Interrupt Level Select (Index=70h, Default=0Bh)	57
8.11.5	Consumer IR Special Configuration Register (Index=F0h, Default=00h)	57
8.12	MIDI Port Configuration Registers (LDN=08h).....	57
8.12.1	MIDI Port Activate (Index=30h, Default=00h).....	57
8.12.2	MIDI Port Base Address MSB Register (Index=60h, Default=03h).....	57
8.12.3	MIDI Port Base Address LSB Register (Index=61h, Default=00h).....	58
8.12.4	MIDI Port Interrupt Level Select (Index=70h, Default=0Ah).....	58
8.12.5	MIDI Port Special Configuration Register (Index=F0h, Default=00h)	58
9.	Functional Description	61
9.1	LPC Interface	61
9.1.1	LPC Transactions.....	61
9.1.2	LDRQ# Encoding.....	61
9.2	Serialized IRQ	61
9.2.1	Continuous Mode.....	61
9.2.2	Quiet Mode.....	62
9.2.3	Waveform Samples of SERIRQ Sequence	62
9.2.4	SERIRQ Sampling Slot	63
9.3	General Purpose I/O.....	63
9.4	Power Management Event (PME#).....	64
9.5	FAN Controller.....	65
9.5.1	Overview.....	65
9.5.2	Interfaces.....	65
9.5.3	Registers.....	65
9.5.3.1	Address Port (Base+05h, Default=00h):.....	65
9.5.3.2	Register Description	67
9.5.3.2.1	Configuration Register (Index=00h, Default=18h)	67
9.5.3.2.2	Interrupt Status Register 1 (Index=01h, Default=00h)	67
9.5.3.2.3	Reserved Register (Index=02h, Default=00h)	67
9.5.3.2.4	Reserved Register (Index=03h, Default=00h)	67
9.5.3.2.5	SMI# Mask Register 1 (Index=04h, Default=00h).....	67
9.5.3.2.6	SMI# Mask Register 2 (Index=05h, Default=00h).....	68
9.5.3.2.7	SMI# Mask Register 3 (Index=06h, Default=00h).....	68
9.5.3.2.8	Interrupt Mask Register 1 (Index=07h, Default=00h)	68
9.5.3.2.9	Reserved Register (Index=08h, Default=00h)	68
9.5.3.2.10	Reserved Register (Index=09h, Default=00h)	68
9.5.3.2.11	Fan Tachometer Divisor Register (Index=0Bh, Default=09h).....	68
9.5.3.2.12	Fan Tachometer 1-3 Reading Registers (Index=0Dh-0Fh)	69
9.5.3.2.13	Fan Tachometer 1-3 Limit Registers (Index=10h-12h)	69

9.5.3.2.14	Fan Controller Main Control Register (Index=13h, Default=00h)	69
9.5.3.2.15	FAN_CTL Control Register (Index=14h, Default=00h).....	69
9.5.3.2.16	FAN_CTL1 PWM Control Register (Index=15h, Default=00h)	70
9.5.3.2.17	FAN_CTL2 PWM Control Register (Index=16h, Default=00h)	70
9.5.3.2.18	FAN_CTL3 PWM Control Register (Index=17h, Default=00h)	70
9.5.3.2.19	Vendor ID Register (Index=58h, Default=90h)	70
9.5.3.2.20	Special Control and Beep Event Enable Register (Index=5Ch, Default=00h)	70
9.5.3.2.21	Beep Frequency Divisor of Fan Event Register (Index=5Dh, Default=00h)	70
9.5.4	Operation.....	71
9.5.4.1	Power On RESET and Software RESET.....	71
9.5.4.2	Fan Tachometer.....	71
9.5.4.3	Interrupt of the FAN controller.....	71
9.6	Floppy Disk Controller (FDC)	71
9.6.1	Introduction.....	71
9.6.2	Reset.....	71
9.6.3	Hardware Reset (LRESET# Pin).....	72
9.6.4	Software Reset (DOR Reset and DSR Reset)	72
9.6.5	Digital Data Separator.....	72
9.6.6	Write Precompensation.....	72
9.6.7	Data Rate Selection.....	73
9.6.8	Status, Data and Control Registers.....	73
9.6.8.1	Digital Output Register (DOR, FDC Base Address + 02h)	73
9.6.8.2	Tape Drive Register (TDR, FDC Base Address + 03h)	73
9.6.8.3	Main Status Register (MSR, FDC Base Address + 04h)	74
9.6.8.4	Data Rate Select Register (DSR, FDC Base Address + 04h).....	74
9.6.8.5	Data Register (FIFO, FDC Base Address + 05h).....	75
9.6.8.6	Digital Input Register (DIR, FDC Base Address + 07h).....	76
9.6.8.7	Diskette Control Register (DCR, FDC Base Address + 07h).....	76
9.6.9	Controller Phases.....	76
9.6.9.1	Command Phase.....	76
9.6.9.2	Execution Phase.....	77
9.6.9.3	Result Phase	77
9.6.9.4	Result Phase Status Registers.....	77
9.6.10	Command Set.....	80
9.6.11	Data Transfer Commands	90
9.6.11.1	READ DATA.....	90
9.6.11.2	READ DELETED DATA.....	91
9.6.11.3	READ A TRACK.....	91
9.6.11.4	WRITE DATA	91
9.6.11.5	WRITE DELETED DATA	91
9.6.11.6	FORMAT A TRACK.....	91
9.6.11.7	SCAN.....	92
9.6.11.8	VERIFY	92
9.6.12	Control Commands	93
9.6.12.1	READ ID.....	93
9.6.12.2	CONFIGURE.....	93
9.6.12.3	RE-CALIBRATE	94
9.6.12.4	SEEK	94
9.6.12.5	RELATIVE SEEK.....	94
9.6.12.6	DUMPREG.....	94
9.6.12.7	LOCK.....	95



9.6.12.8	VERSION	95
9.6.12.9	SENSE INTERRUPT STATUS	95
9.6.12.10	SENSE DRIVE STATUS.....	95
9.6.12.11	SPECIFY.....	95
9.6.12.12	PERPENDICULAR MODE.....	96
9.6.12.13	INVALID	97
9.6.13	DMA Transfers.....	97
9.6.14	Low Power Mode	97
9.7	Serial Port (UART) Register Description.....	98
9.7.1	Data Registers	98
9.7.2	Control Registers: IER, IIR, FCR, DLL, DLM, LCR and MCR	98
9.7.3	Status Registers: LSR and MSR	105
9.7.4	Reset	107
9.7.5	Programming	107
9.7.6	Software Reset	107
9.7.7	Clock Input Operation	107
9.7.8	FIFO Interrupt Mode Operation	107
9.8	Parallel Port.....	109
9.8.1	SPP and EPP Modes	109
9.8.2	EPP Mode Operation	110
9.8.3	ECP Mode Operation	112
9.9	Consumer Remote Control (TV Remote) IR (CIR).....	118
9.9.1	Overview.....	118
9.9.2	Features	118
9.9.3	Block Diagram	118
9.9.4	Transmit Operation	119
9.9.5	Receive Operation	119
9.9.6	Register Descriptions and Address.....	119
9.9.6.1	CIR Data Register (DR)	120
9.9.6.2	CIR Interrupt Enable Register (IER)	120
9.9.6.3	CIR Receiver Control Register (RCR)	121
9.9.6.4	CIR Transmitter Control Register 1 (TCR1).....	122
9.9.6.5	CIR Transmitter Control Register 2 (TCR2).....	123
9.9.6.6	CIR Baud Rate Divisor Low Byte Register (BDLR)	126
9.9.6.7	CIR Baud Rate Divisor Register High Byte (BDHR).....	126
9.9.6.8	CIR Transmitter Status Register (TSR)	126
9.9.6.9	CIR Receiver FIFO Status Register (RSR).....	127
9.9.6.10	CIR Interrupt Identification Register (IIR).....	127
9.10	Game Port Interface	127
9.10.1	Game Port (Base+0h)	128
9.11	FLASH ROM Interface.....	128
9.12	MIDI Interface.....	129
9.12.1	MPU-401 Register Interface.....	129
9.12.2	Operation.....	130
10.	DC Electrical Characteristics.....	131
11.	AC Characteristics (Vcc = 5.0V ± 5%, Ta = 0°C to + 70°C)	133
11.1	Clock Input Timings	133
11.2	LCLK (PCICLK) and LRESET#	133
11.3	LPC and SERIRQ Timings.....	134
11.4	Serial Port, ASKIR, SIR and Consumer Remote Control Timings	135
11.5	Modem Control Timings	136
11.6	Floppy Disk Drive Timings	137

11.7	EPP Address or Data Write Cycle	138
11.8	EPP Address or Data Read Cycle.....	139
11.9	ECP Parallel Port Forward Timings.....	140
11.10	ECP Parallel Port Backward Timings	141
11.11	Flash ROM I/F Write Timings	142
11.12	Flash ROM I/F Read Timings.....	143
12.	Package Information.....	145
13.	Ordering Information.....	147

Timing Diagrams

Figure 11-1.	Clock Input Timings.....	133
Figure 11-2.	LCLK (PCICLK) and LRESET# Timings	133
Figure 11-3.	LPC and SERIRQ Timings	134
Figure 11-4.	Serial Port, ASKIR, SIR and Consumer Remote Control Timings.....	135
Figure 11-5.	Modem Control Timings	136
Figure 11-6.	Floppy Disk Drive Timings.....	137
Figure 11-7.	EPP Address or Data Write Cycle	138
Figure 11-8.	EPP Address or Data Read Cycle	139
Figure 11-9.	ECP Parallel Port Forward Timings	140
Figure 11-10.	ECP Parallel Port Backward Timings.....	141
Figure 11-11.	Flash ROM I/F Write Timings.....	142
Figure 11-12.	Flash ROM I/F Read Timings	143

FIGURES

Figure 9-1.	Start Frame Timings.....	62
Figure 9-2.	Stop Frame Timings.....	62
Figure 9-3.	General Logic of GPIO Function.....	64
Figure 9-4.	CIR Block Diagram.....	118
Figure 9-5.	FLASH ROM Interface Diagram	128

TABLES

Table 4-1.	Pins Listed in Numeric Order.....	8
Table 4-2.	Pins Listed in Alphabetical Order.....	9
Table 5-1.	Pin Description of Supplies Signals	11
Table 5-2.	Pin Description of LPC Bus Interface Signals.....	11
Table 5-3.	Pin Description of Fan Controller Signals ^{Note}	12
Table 5-4.	Pin Description of Infrared Port Signals ^{Note}	12
Table 5-5.	Pin Description of Game Port Signals.....	13
Table 6-1.	General Purpose I/O Group 1.....	21
Table 6-2.	General Purpose I/O Group 2.....	21



Table 6-3. General Purpose I/O Group 3.....	22
Table 6-4. General Purpose I/O Group 4.....	22
Table 6-5. General Purpose I/O Group 5.....	22
Table 6-6. General Purpose I/O Group 6 ^{Note}	23
Table 6-7. Programming of Pins 82, 83, 84, and 85.....	23
Table 7-1. Power On Strapping Options.....	25
Table 8-1. Global Configuration Registers.....	28
Table 8-2. FDC Configuration Registers.....	29
Table 8-3. Serial Port 1 Configuration Registers.....	29
Table 8-4. Serial Port 2 Configuration Registers.....	29
Table 8-5. Parallel Port Configuration Registers.....	30
Table 8-6. FAN Controller Configuration Registers.....	30
Table 8-7. GPIO Configuration Registers.....	31
Table 8-8. Game Port Configuration Registers.....	32
Table 8-9. Consumer IR Configuration Registers.....	33
Table 8-10. MIDI Port Configuration Registers.....	33
Table 8-11. Base Address of Logical Devices.....	34
Table 9-1. Address Map on the ISA Bus.....	65
Table 9-2. FAN Controller Registers.....	66
Table 9-3. Digital Output Register (DOR).....	73
Table 9-4. Tape Drive Register (TDR).....	73
Table 9-5. Main Status Register (MSR).....	74
Table 9-6. Data Rate Select Register (DSR).....	75
Table 9-7. Data Register (FIFO).....	75
Table 9-8. Digital Input Register (DIR).....	76
Table 9-9. Diskette Control Register (DCR).....	76
Table 9-10. Status Register 0 (ST0).....	77
Table 9-11. Status Register 1 (ST1).....	78
Table 9-12. Status Register 2 (ST2).....	79
Table 9-13. Status Register 3 (ST3).....	79
Table 9-14. Command Set Symbol Descriptions.....	80
Table 9-15. Command Set Summary.....	82
Table 9-16. Effects of MT and N Bits.....	90
Table 9-17. SCAN Command Result.....	92
Table 9-18. VERIFY Command Result.....	93
Table 9-19. Interrupt Identification.....	95
Table 9-20. HUT Values (ms).....	95
Table 9-21. SRT Values (ms).....	96
Table 9-22. HLT Values.....	96
Table 9-23. Effects of GAP and WG on FORMAT A TRACK and WRITE DATA Commands.....	96

IT8700F

Table 9-24. Effects of Drive Mode and Data Rate on FORMAT A TRACK and WRITE DATA Commands.....	97
Table 9-25. Serial Channel Registers	98
Table 9-26. Interrupt Enable Register Description	99
Table 9-27. Interrupt Identification Register	100
Table 9-28. FIFO Control Register Description	101
Table 9-29. Receiver FIFO Trigger Level Encoding	101
Table 9-30. Baud Rates Using (24 MHz ÷ 13) Clock.....	102
Table 9-31. Line Control Register Description	103
Table 9-32. Stop Bits Number Encoding.....	103
Table 9-33. Modem Control Register Description	104
Table 9-34. Line Status Register Description.....	105
Table 9-35. Modem Status Register Description.....	106
Table 9-36. Reset Control of Registers and Pinout Signals.....	107
Table 9-37. Parallel Port Connector in Different Modes	109
Table 9-38. Address Map and Bit Map for SPP and EPP Modes	109
Table 9-39. Bit Map of the ECP Registers	112
Table 9-40. ECP Register Definitions	112
Table 9-41. ECP Mode Descriptions.....	113
Table 9-42. ECP Pin Descriptions	113
Table 9-43. Extended Control Register (ECR) Mode and Description	115
Table 9-44. List of CIR Registers.....	119
Table 9-45. Modulation Carrier Frequency	124
Table 9-46. Receiver Demodulation Low Frequency (HCFS = 0).....	125
Table 9-47. Receiver Demodulation High Frequency (HCFS = 1)	126
Table 11-1. Clock Input Timings AC Table	133
Table 11-2. LCLK (PCICLK) and LRESET# AC Table	133
Table 11-3. LPC and SERIRQ Timings AC Table.....	134
Table 11-4. Serial Port, ASKIR, SIR and Consumer Remote Control Timings AC Table	135
Table 11-5. Modem Control Timings AC Table.....	136
Table 11-6. Floppy Disk Drive Timings AC Table.....	137
Table 11-7. EPP Address or Data Write Cycle AC Table	138
Table 11-8. EPP Address or Data Read Cycle AC Table.....	139
Table 11-9. ECP Parallel Port Forward Timings AC Table	140
Table 11-10. ECP Parallel Port Backward Timings AC Table.....	141
Table 11-11. Flash ROM I/F Write Timing AC Table.....	142
Table 11-12. Flash ROM I/F Read Timings AC Table	143



1. Features

- **Low Pin Count Interface**
 - Compliant with Intel LPC Interface Specification Rev.1.0 (Sept. 29, 1997)
 - Supports Serial IRQ Protocol
 - Supports PCI PME# Interface
- **PC98/PC99, ACPI Compliant**
 - PC98 & PC99 compliant
 - Register sets compatible with “Plug and Play ISA Specification Rev. 1.0a”
 - ACPI V. 1.0 compliant
 - Supports 9 logical devices
- **Fan Speed Controller**
 - Provides Fan ON/OFF and PWM control
 - 3 programmable Pulse Width Modulation (PWM) Fan control outputs
 - Each PWM output supports 128 steps of PWM modes
 - Monitors 3 Fan tachometer inputs
- **Game Port**
 - Built-in 558 quad timers and buffer chips
 - Supports direct connection of two joysticks
 - Game port signals are multiplexed with GPIOs
- **Two 16C550 UARTs**
 - Supports two standard Serial ports
 - UART1 is dedicated for Serial port
 - UART2 supports either Serial Port or IrDA 1.0/ASKIR
- **MIDI Interface**
 - UART implementation
 - Supports direct connection to MPU-401 MIDI
- **Consumer Remote Control (TV remote) IR with Power-up Feature**
- **IEEE 1284 Parallel Port**
 - Standard mode -- Bi-directional SPP compliant
 - Enhanced mode -- EPP V.1.7 and 1.9 compliant
 - High speed mode -- ECP, IEEE 1284 compliant
 - Backdrive current reduction
 - Printer power-on damage reduction
 - Supports POST (Power-On Self Test) Data Port
- **Floppy Disk Controller**
 - Supports two 360K/ 720K/ 1.2M/ 1.44M/ 2.88M floppy disk drives
 - Enhanced digital data separator
 - 3-Mode drives supported
 - Supports automatic write protection via software
- **Smart Card Reader**
 - Compliant with Personal Computer Smart Card (PC/SC) Working Group standard
 - Compliant with smart card (ISO 7816) protocols
 - Supports card present detect
 - Supports one programmable clock frequency, 7.1 MHz, and 3.5 MHz (default) card clocks
- **48 General Purpose I/O Pins**
 - Input mode supports switch de-bounce
 - SMI is routed through GPIOs
 - Power LED Blinking Control
 - FAN Controller Warning Beep Output
 - External IRQ Inputs Routing into Serial IRQ
 - Watch Dog Timer
- **Flash ROM Interface**
 - Up to 4M bits flash supported
- **Single 24/48 MHz Clock Inputs**
- **Single +5V Power Supply**
- **128-Pin PQFP**



2. General Description

The IT8700F is a LPC Interface based highly integrated Super I/O. The IT8700F provides the most commonly used legacy Super I/O functionality plus the Fan Speed Controller and Smart Card Reader interface. The device's LPC interface complies with Intel "LPC Interface Specification Rev. 1.0" (Sept. 29, 1997). The IT8700F meets the "Microsoft® PC98 & PC99 System Design Guide" requirements and is ACPI compliant.

The IT8700F features a PC/SC and ISO 7816 compliant Smart Card Reader.

The IT8700F has integrated nine logical devices, featuring a FAN Speed Controller (controls three Fans). One Fan Speed Controller is responsible to control three fan speeds through three 128 steps of Pulse Width Modulation (PWM) output pins and to monitor three fans' tachometer inputs.

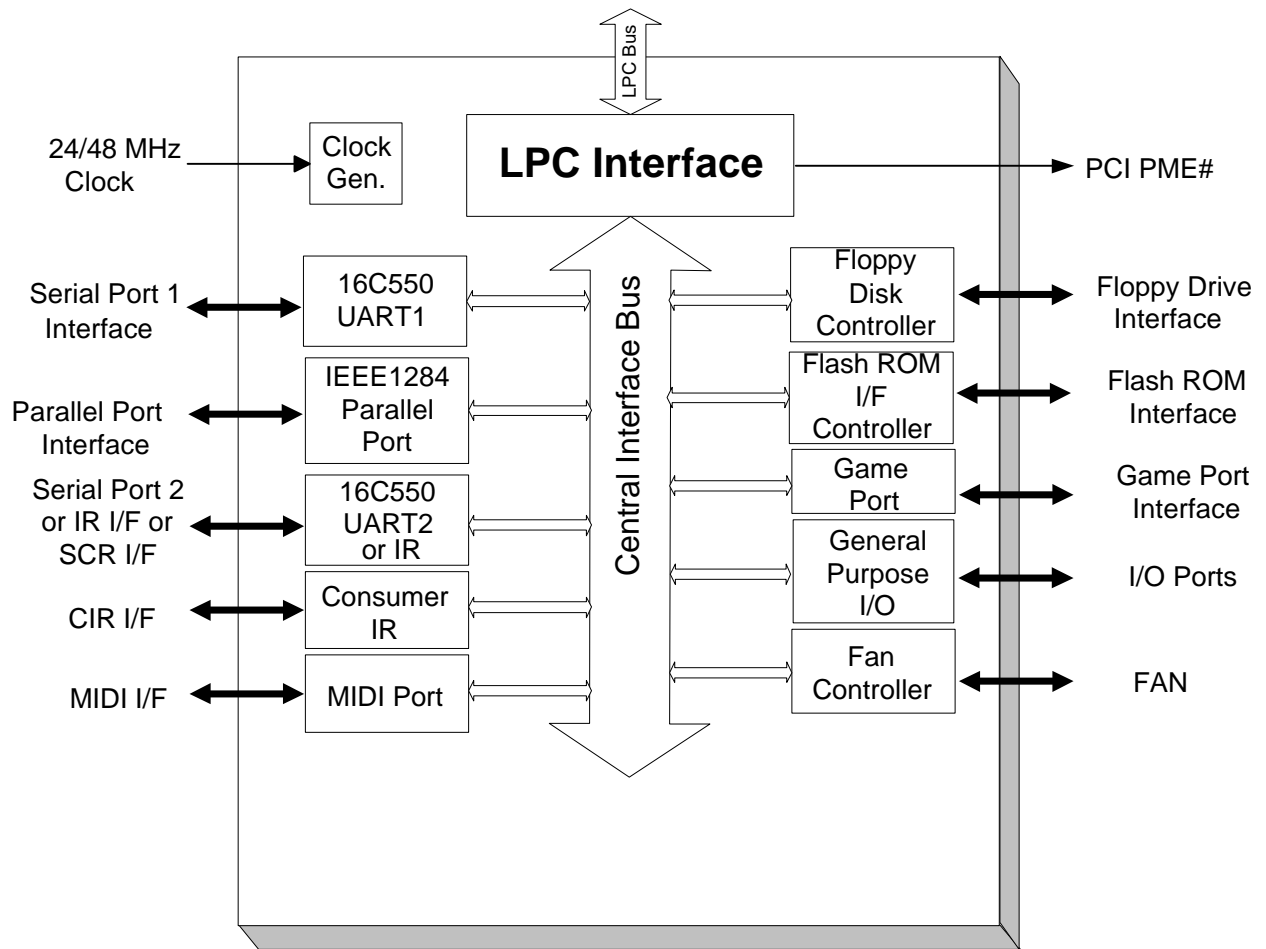
Other features include one high-performance 2.88MB floppy disk controller, with digital data separator, supporting two 360K/ 720K/ 1.2M/ 1.44M/ 2.88M floppy disk drives. One multi-mode high-performance parallel port features the bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP V. 1.7 and EPP V. 1.9 are supported), and the IEEE 1284 compliant Extended Capabilities Port (ECP). Two 16C550 standard compatible enhanced UARTs perform asynchronous communication, and support SIR and one consumer remote control (TV remote) IR, one MPU-401 UART mode compatible MIDI port, one game port with built-in 558 quad timers and buffer chips to support direct connection of 2 joysticks, and six ports (48 GPIO pins). There is also a flash ROM interface with Address (FA[0:18]), Data (FD[0:7]), and supporting three control signals FCS#, FWE# and FRD#.

These nine logical devices can be individually enabled or disabled via software configuration registers. The IT8700F utilizes power-efficient circuitry to reduce power consumption. Once a logical device is disabled, the inputs are gated inhibit, the outputs are TRI-STATE and the input clock is disabled. The IT8700F requires a single 48/24 MHz clock input and operates with a single +5V power supply.

The IT8700F is available in 128-pin PQFP (Plastic Quad Flat Package).

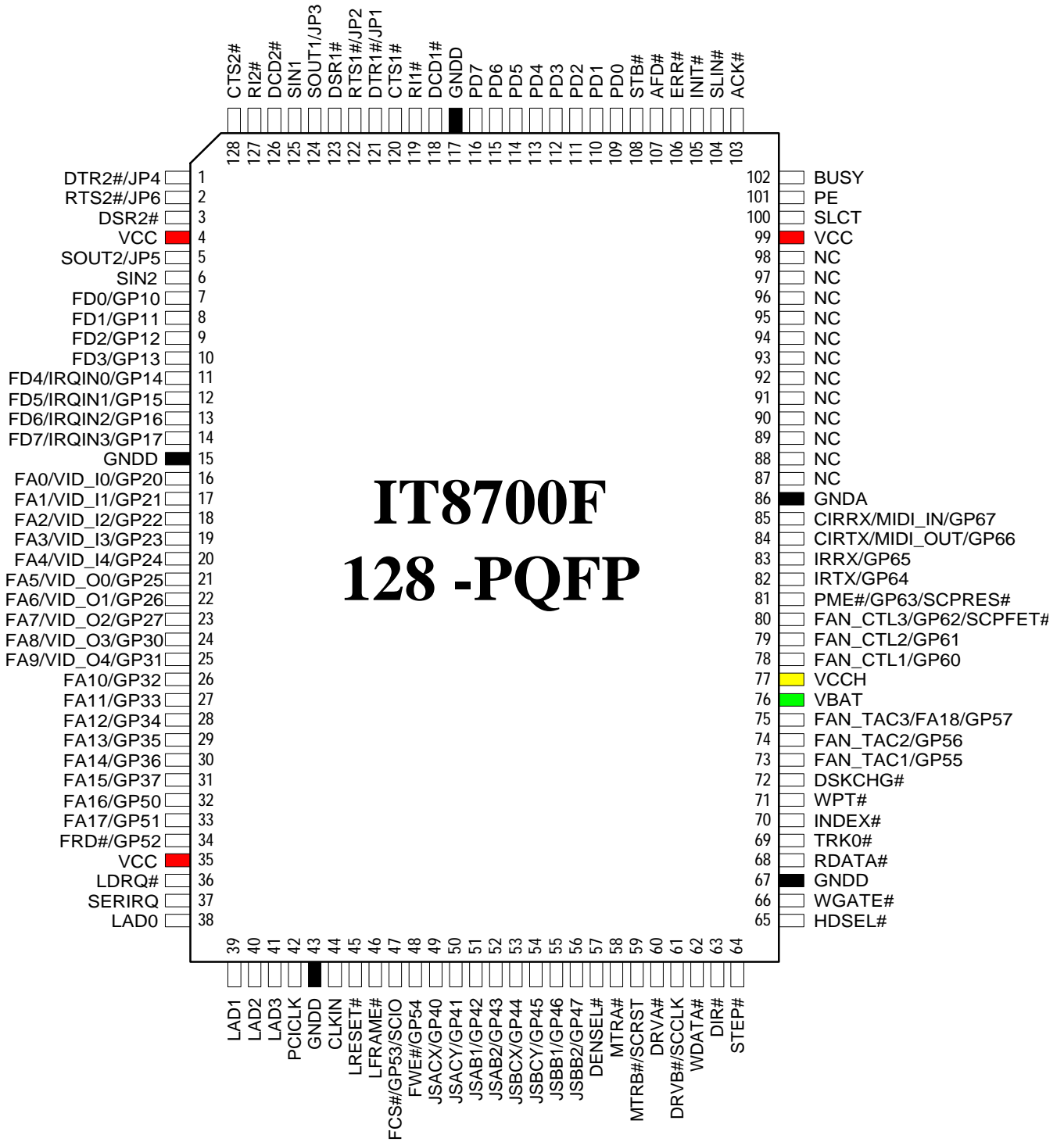


3. Block Diagram





4. Pin Configuration



IT8700F**Table 4-1. Pins Listed in Numeric Order**

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	DTR2#/JP4	33	FA17/GP51	65	HDSEL#	97	NC
2	RTS2#/JP6	34	FRD#/GP52	66	WGATE#	98	NC
3	DSR2#	35	VCC	67	GNDD	99	VCC
4	VCC	36	LDRQ#	68	RDATA#	100	SLCT
5	SOUT2	37	SERIRQ	69	TRK0#	101	PE
6	SIN2	38	LAD0	70	INDEX#	102	BUSY
7	FD0/GP10	39	LAD1	71	WPT#	103	ACK#
8	FD1/GP11	40	LAD2	72	DSKCHG#	104	SLIN#
9	FD2/GP12	41	LAD3	73	FAN_TAC1/GP55	105	INIT#
10	FD3/GP13	42	PCICLK	74	FAN_TAC2/GP56	106	ERR#
11	FD4/IRQIN0/ GP14	43	GNDD	75	FAN_TAC3/FA18/ GP57	107	AFD#
12	FD5/IRQIN1/ GP15	44	CLKIN	76	VBAT	108	STB#
13	FD6/IRQIN2/ GP16	45	LRESET#	77	VCCH	109	PD0
14	FD7/IRQIN3/ GP17	46	LFRAME#	78	FAN_CTL1/GP60	110	PD1
15	GNDD	47	FCS#/SCIO/GP53	79	FAN_CTL2/GP61	111	PD2
16	FA0/VID_I0/GP20	48	FWE#/GP54	80	FAN_CTL3/GP62/ SCPFET#	112	PD3
17	FA1/VID_I1/GP21	49	JSACX/GP40	81	PME#/GP63/ SCPRES#	113	PD4
18	FA2/VID_I2/GP22	50	JSACY/GP41	82	IRTX/MIDI_OUT/ GP64	114	PD5
19	FA3/VID_I3/GP23	51	JSAB1/GP42	83	IRRX/MIDI_IN/ GP65	115	PD6
20	FA4/VID_I4/GP24	52	JSAB2/GP43	84	CIRTX/GP66	116	PD7
21	FA5/VID_O0/ GP25	53	JSBCX/GP44	85	CIRRX/GP67	117	GNDD
22	FA6/VID_O1/ GP26	54	JSBCY/GP45	86	GNDA	118	DCD1#
23	FA7/VID_O2/ GP27	55	JSBB1/GP46	87	NC	119	RI1#
24	FA8/VID_O3/ GP30	56	JSBB2/GP47	88	NC	120	CTS1#
25	FA9/VID_O4/ GP31	57	DENSEL#	89	NC	121	DTR1#/JP1
26	FA10/GP32	58	MTRA#	90	NC	122	RTS1#/JP2
27	FA11/GP33	59	MTRB#/SCRST	91	NC	123	DSR1#
28	FA12/GP34	60	DRVA#	92	NC	124	SOUT1/JP3
29	FA13/GP35	61	DRVB#/SCCLK	93	NC	125	SIN1
30	FA14/GP36	62	WDATA#	94	NC	126	DCD2#
31	FA15/GP37	63	DIR#	95	NC	127	RI2#
32	FA16/GP50	64	STEP#	96	NC	128	CTS2#



Pin Configuration

Table 4-2. Pins Listed in Alphabetical Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ACK#	103	FA4/VID_I4/GP24	20	IRTX/MIDI_OUT/ GP64	82	PD1	110
AFD#	107	FA5/VID_O0/ GP25	21	JSAB1/GP42	51	PD2	111
BUSY	102	FA6/VID_O1/ GP26	22	JSAB2/GP43	52	PD3	112
CIRRX/GP67	85	FA7/VID_O2/ GP27	23	JSACX/GP40	49	PD4	113
CIRTX/GP66	84	FA8/VID_O3/ GP30	24	JSACY/GP41	50	PD5	114
CLKIN	44	FA9/VID_O4/ GP31	25	JSBB1/GP46	55	PD6	115
CTS1#	120	FAN_CTL1/GP60	78	JSBB2/GP47	56	PD7	116
CTS2#	128	FAN_CTL2/GP61	79	JSBCX/GP44	53	PE	101
DCD1#	118	FAN_CTL3/GP62/ SCPFET#	80	JSBCY/GP45	54	PME#/GP63/ SCPRES#	81
DCD2#	126	FAN_TAC1/GP55	73	LAD0	38	RDATA#	68
DENSEL#	57	FAN_TAC2/GP56	74	LAD1	39	RI1#	119
DIR#	63	FAN_TAC3/FA18/ GP57	75	LAD2	40	RI2#	127
DRVA#	60	FCS#/GP53/SCIO	47	LAD3	41	RTS1#/JP2	122
DRVB#/SCCLK	61	FD0/GP10	7	LDRQ#	36	RTS2#/JP6	2
DSKCHG#	72	FD1/GP11	8	LFRAME#	46	SERIRQ	37
DSR1#	123	FD2/GP12	9	LRESET#	45	SIN1	125
DSR2#	3	FD3/GP13	10	MTRA#	58	SIN2	6
DTR1#/JP1	121	FD4/GP14	11	MTRB#/SCRST	59	SLCT	100
DTR2#/JP4	1	FD5/GP15	12	NC	87	SLIN#	104
ERR#	106	FD6/GP16	13	NC	88	SOUT1/JP3	124
FA0/VID_I0/GP20	16	FD7/GP17	14	NC	89	SOUT2	5
FA1/VID_I1/GP21	17	FRD#/GP52	34	NC	90	STB#	108
FA10/GP32	26	FWE#/GP54	48	NC	91	STEP#	64
FA11/GP33	27	GND	86	NC	92	TRK0#	69
FA12/GP34	28	GNDD	15	NC	93	VBAT	76
FA13/GP35	29	GNDD	43	NC	94	VCC	4
FA14/GP36	30	GNDD	67	NC	95	VCC	35
FA15/GP37	31	GNDD	117	NC	96	VCC	99
FA16/GP50	32	HDSEL#	65	NC	97	VCC	77
FA17/GP51	33	INDEX#	70	NC	98	WDATA#	62
FA2/VID_I2/GP22	18	INIT#	105	PCICLK	42	WGATE#	66
FA3/VID_I3/GP23	19	IRRX/MIDI_IN/ GP65	83	PD0	109	WPT#	71



IT8700F Pin Descriptions

5. IT8700F Pin Descriptions

Table 5-1. Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
4, 35, 99	VCC	PWR		+5V Power Supply.
76	VBAT	PWR		+3.3V Battery Supply.
77	VCCH	PWR		+5V VCC Help Supply.
15, 43, 67, 117	GNDD	GND		Digital Ground.
86	GNDA	GND		Analog Ground.

Table 5-2. Pin Description of LPC Bus Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
36	LDRQ#	DO16	VCC	LPC DMA Request #. An encoded signal for DMA channel select.
37	SERIRQ	DIO16	VCC	Serial IRQ.
38 – 41	LAD[0:3]	DIO16	VCC	LPC Address/Data 0-3. 4-bit LPC address / bi-directional data lines. LAD0 is the LSB and LAD3 is the MSB.
42	PCICLK	DI	VCC	LPC Clock. 33 MHz PCI Clock Input.
45	LRESET#	DI	VCC	LPC RESET #.
46	LFRAME#	DI	VCC	LPC Frame #. This signal indicates the start of the LPC cycle.
81	PME#/GP63/ SCPRES#	DOD8/ DIOD8/ DI	VCCH	Power Management Event # / General Purpose I/O 63. / Smart Card Present Detect #. <ul style="list-style-type: none"> The first function of this pin is the power management event #, and supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from D3 (cold) state. This pin is backed by VCCH. The second function of this pin is the General Purpose I/O Port 6 Bit 3. The third function of this pin is Smart Card Present Detect #. This pin provides the Smart Card insertion detection for the Smart Card Reader interface. Upon detecting the insertion of the Smart Card, this pin will trigger the power-on event. The function configuration of this pin is determined by programming the software configuration registers.

Table 5-3. Pin Description of Fan Controller Signals ^{Note}

Pin(s) No.	Symbol	Attribute	Power	Description
73 – 74	FAN_TAC [1:2]/ GP5[5:6]	DI/ DIOD8	VCC	Fan Tachometer Inputs [1:2] / General Purpose I/O 5[5:6]. <ul style="list-style-type: none"> The first functions of these pins are Fan tachometer inputs [1:2]. (0 to +5V amplitude fan tachometer input) The second functions of these pins are General Purpose I/O Port 5 Bits 5-6. The function configurations of these pins are determined by programming the software configuration registers.
75	FAN_TAC3/ FA18/ GP57	DI/ DO/ DIOD8	VCC	Fan Tachometer Inputs 3 / Flash ROM Interface Address 18 / General Purpose I/O 57. <ul style="list-style-type: none"> The first function of this pin is Fan Tachometer Inputs 3 (0 to +5V amplitude fan tachometer input). The second function of this pin is the Flash ROM Interface Address 18. The third function of this pin is General Purpose I/O Port 5 Bit 7. The function configuration of this pin is determined by programming the software configuration registers.
78 – 79	FAN_CTL [1:2]/ GP6[0:1]	DOD8/ DIOD8	VCCH	FAN Control Outputs [1:2] / General Purpose I/O 6[0:1]. <ul style="list-style-type: none"> The first functions of these pins are Fan Control Outputs [1:2]. (PWM output signal to Fan's FET.) The second functions of these pins are General Purpose I/O Port 6 Bits 0-1. The function configurations of these pins are determined by programming the software configuration registers.
80	FAN_CTL3/ GP62/ SCPFET#	DOD8/ DIOD8/ DOD8	VCCH	FAN Control Output 3 / General Purpose I/O 62 / Smart Card Power FET Control Output#. <ul style="list-style-type: none"> The first functions of these pins are Fan Control Outputs [1:3]. (PWM output signal to Fan's FET.) The second functions of these pins are General Purpose I/O Port 6 Bits 0-2. The third function of this pin is Smart Card Power FET Control Output #. The Smart Card Reader interface requires this pin to drive an external Power FET to supply the current for the Smart Card (65 mA typical, 100 mA short to ground). The function configurations of these pins are determined by programming the software configuration registers.

Note: The GPIO registers of these pins are powered by VCC, not VCCH.

Table 5-4. Pin Description of Infrared Port Signals ^{Note}

Pin(s) No.	Symbol	Attribute	Power	Description
82	IRTX/GP64	DO8/ DIOD8	VCCH	Infrared Transmit Output / General Purpose I/O 64. <ul style="list-style-type: none"> The first function of this pin is the Infrared Transmit Output. The second function of this pin is the General Purpose I/O Port 6 Bit 4. The function configuration of this pin is determined by programming the software configuration registers.
83	IRRX/GP65	DI/ DIOD8	VCCH	Infrared Receive Input / General Purpose I/O 65. <ul style="list-style-type: none"> The first function of this pin is the Infrared Receive Input. The second function of this pin is the General Purpose I/O Port 6 Bit 5. The function configuration of this pin is determined by programming the software configuration registers.



IT8700F Pin Descriptions

Table 5-4. Pin Description of Infrared Port Signals (cont' d)

Pin(s) No.	Symbol	Attribute	Power	Description
84	CIRTX/ MIDI_OUT/ GP66	DO8/ DO8/ DIOD8	VCCH	Consumer Infrared Transmit Output / MIDI Output / General Purpose I/O 66. <ul style="list-style-type: none"> The first function of this pin is the Consumer Infrared Transmit Output. The second function of this pin is the MIDI Output. The third function of this pin is the General Purpose I/O Port 6 Bit 6. The function configuration of this pin is determined by programming the software configuration registers.
85	CIRRX/ MIDI_IN/ GP67	DI/ DI/ DIOD8	VCCH	Consumer Infrared Receive Input / MIDI Input / General Purpose I/O 67. <ul style="list-style-type: none"> The first function of this pin is the Consumer Infrared Receive Input. The second function of this pin is the MIDI Input. The third function of this pin is the General Purpose I/O Port 6 Bit 7. The function configuration of this pin is determined by programming the software configuration registers.

Note: The GPIO registers of these pins are powered by VCC, not VCCH.

Table 5-5. Pin Description of Game Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
49	JSACX/ GP40	DIOD8/ DIOD8	VCC	Joystick A Coordinate X / General Purpose I/O 40. <ul style="list-style-type: none"> The first function of this pin is the joystick A Coordinate X. The second function of this pin is the General Purpose I/O Port 4 Bit 0. The function configuration of this pin is determined by programming the software configuration registers.
50	JSACY/ GP41	DIOD8/ DIOD8	VCC	Joystick A Coordinate Y / General Purpose I/O 41. <ul style="list-style-type: none"> The first function of this pin is the joystick A Coordinate Y. The second function of this pin is the General Purpose I/O Port 4 Bit 1. The function configuration of this pin is determined by programming the software configuration registers.
51	JSAB1/ GP42	DI/ DIOD8	VCC	Joystick A Button 1 / General Purpose I/O 42. <ul style="list-style-type: none"> The first function of this pin is the joystick A Button 1. The second function of this pin is the General Purpose I/O Port 4 Bit 2. The function configuration of this pin is determined by programming the software configuration registers.
52	JSAB2/ GP43	DI/ DIOD8	VCC	Joystick A Button 2 / General Purpose I/O 43. <ul style="list-style-type: none"> The first function of this pin is the joystick A Button 2. The second function of this pin is the General Purpose I/O Port 4 Bit 3. The function configuration of this pin is determined by programming the software configuration registers.
53	JSBCX/ GP44	DIOD8/ DIOD8	VCC	Joystick B Coordinate X / General Purpose I/O 44. <ul style="list-style-type: none"> The first function of this pin is the joystick B Coordinate X. The second function of this pin is the General Purpose I/O Port 4 Bit 4. The function configuration of this pin is determined by programming the software configuration registers.

Table 5-5. Pin Description of Game Port Signals (cont' d)

Pin(s) No.	Symbol	Attribute	Power	Description
54	JSBCY/ GP45	DIOD8/ DIOD8	VCC	Joystick B Coordinate Y / General Purpose I/O 45. <ul style="list-style-type: none"> The first function of this pin is the joystick B Coordinate Y. The second function of this pin is the General Purpose I/O Port 4 Bit 5. The function configuration of this pin is determined by programming the software configuration registers.
55	JSBB1/ GP46	DI/ DIOD8	VCC	Joystick B Button 1 / General Purpose I/O 46. <ul style="list-style-type: none"> The first function of this pin is the joystick B Button 1 Input. The second function of this pin is the General Purpose I/O Port 4 Bit 6. The function configuration of this pin is determined by programming the software configuration registers.
56	JSBB2/ GP47	DI/ DIOD8	VCC	Joystick B Button 2 / General Purpose I/O 47. <ul style="list-style-type: none"> The first function of this pin is the joystick B Button 2 Input. The second function of this pin is the General Purpose I/O Port 4 Bit 7. The function configuration of this pin is determined by programming the software configuration registers.

Table 5-7. Pin Description of Serial Port 1 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
118	DCD1#	DI	VCC	Data Carrier Detect 1 #. When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
119	RI1#	DI	VCC	Ring Indicator 1 #. When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
120	CTS1#	DI	VCC	Clear to Send 1 #. When the signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
121	DTR1#/JP1	DO8/DI	VCC	Data Terminal Ready 1 # / JP1. When the signal is low, this output indicates to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. <u>During LRESET#, this pin is input for JP1 power-on strapping option.</u>
122	RTS1#/JP2	DO8/DI	VCC	Request to Send 1 # / JP2. When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. <u>During LRESET#, this pin is input for JP2 power-on strapping option.</u>
123	DSR1#	DI	VCC	Data Set Ready 1 #. When this signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.



IT8700F Pin Descriptions

Table 5-7. Pin Description of Serial Port 1 Signals (cont' d)

Pin(s) No.	Symbol	Attribute	Power	Description
124	SOUT1/JP3	DO8/DI	VCC	Serial Data Out 1 / JP3. This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation. <u>During LRESET#, this pin is input for JP3 power-on strapping option.</u>
125	SIN1	DI	VCC	Serial Data In 1. This input receives serial data from the communications link.

Table 5-8. Pin Description of Serial Port 2 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
126	DCD2#	DI	VCC	Data Carrier Detect 2 #. When this signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
127	RI2#	DI	VCC	Ring Indicator 2 #. When this signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI signal is a MODEM status input whose condition can be tested by reading the MSR register.
128	CTS2#	DI	VCC	Clear to Send 2 #. When this signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
1	DTR2#/JP4	DO8/DI	VCC	Data Terminal ready 2 # / JP4. DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. <u>During LRESET#, this pin is input for JP4 power-on strapping option.</u>
2	RTS2#/JP6	DO8/DI	VCC	Request to Send 2 # / JP6. When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. During LRESET#, this pin is input for JP6 power-on strapping option.
3	DSR2#	DI	VCC	Data Set Ready 2 #. When this signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
5	SOUT2/JP5	DO8/DI	VCC	Serial Data Out 2 / JP5. This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes. <u>During LRESET#, this pin is input for JP5 power-on strapping option.</u>
6	SIN2	DI	VCC	Serial Data In 2. This input receives serial data from the communications link.

Table 5-9. Pin Description of Parallel Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
100	SLCT	DI	VCC	Printer Select. This signal goes high when the line printer has been selected.
101	PE	DI	VCC	Printer Paper End. This signal is set high by the printer when it runs out of paper.
102	BUSY	DI	VCC	Printer Busy. This signal goes high when the line printer has a local operation in progress and cannot accept data.
103	ACK#	DI	VCC	Printer Acknowledge #. This signal goes low to indicate that the printer has already received a character and is ready to accept another.
104	SLIN#	DIO24	VCC	Printer Select Input #. When this signal is low, the printer is selected. This signal is derived from the complement of the bit 3 of the printer control register.
105	INIT#	DIO24	VCC	Printer Initialize #. When this signal is active low, this signal is derived from the bit 2 of the printer control register, and is used to initialize the printer.
106	ERR#	DI	VCC	Printer Error #. When this signal is active low, it indicates that the printer has encountered an error. The error message can be read from the bit 3 of the printer status register.
107	AFD#	DIO24	VCC	Printer Auto Line Feed #. This signal is active low, and is derived from the complement of the bit 1 of the printer control register, and is used to advance one line after each line is printed.
108	STB#	DIO24	VCC	Printer Strobe #. This signal is active low, and is derived from the complement of the bit 0 of the printer control register, and is used to strobe the printing data into the printer.
109 – 116	PD[0:7]	DIO24	VCC	Parallel Port Data Bus 0-7. This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is de-selected.



IT8700F Pin Descriptions

Table 5-10. Pin Description of Floppy Disk Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
57	DENSEL#	DO40	VCC	FDD Density Select #. DENSEL# is high for high data rates (500 Kbps, 1 Mbps). DENSEL# is low for low data rates (250 Kbps, 300 Kbps).
58	MTRA#	DO40	VCC	FDD Motor A Enable #. Active low.
59	MTRB#/ SCRST	DO40/ DOD40	VCC	FDD Motor B Enable #. / Smart Card Reset. <ul style="list-style-type: none"> The first function of this pin is FDD Motor B Enable #. The second function of this pin is Smart Card Reset. The function configuration of this pin is decided by the software configuration registers.
60	DRVA#	DO40	VCC	FDD Drive A Enable #. Active low.
61	DRVB#/ SCCLK	DO40/ DOD40	VCC	FDD Drive B Enable # / Smart Card Clock. <ul style="list-style-type: none"> The first function of this pin is the FDD Drive B Enable #. The second function of this pin is Smart Card Clock. Three different card clocks are selectable from this pin: high speed (7.1 MHz), low speed (Default: 3.5 MHz) and a programmable card clock. The function configuration of this pin is determined by the software configuration registers.
62	WDATA#	DO40	VCC	FDD Write Serial Data to the Drive #. Active low.
63	DIR#	DO40	VCC	FDD Head Direction #. This output determines the direction the FDC head movement during the SEEK operation. When the output is high, the head will step in. Otherwise, the head will step out.
64	STEP#	DO40	VCC	FDD Step Pulse #. Active low.
65	HDSEL#	DO40	VCC	FDD Head Select #. Active low.
66	WGATE#	DO40	VCC	FDD Write Gate Enable #. Active low.
68	RDATA#	DI	VCC	FDD Read Disk Data #. Active low. Serial data input from the FDD.
69	TRK0#	DI	VCC	FDD Track 0 #. Active low. Indicates that the head of the selected drive is on track 0.
70	INDEX#	DI	VCC	FDD Index #. Active low. Indicates the beginning of a disk track.
71	WPT#	DI	VCC	FDD Write Protect #. Active low. Indicates that the disk of the selected drive is write-protected.
72	DSKCHG#	DI	VCC	Floppy Disk Change #. Active low. This is an input pin that senses whether the drive door has been opened or a diskette has been changed.

IT8700F



Table 5-11. Pin Description of Flash ROM Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
7 – 10	FD[0:3]/ GP1[0:3]	DO8/ DIOD8	VCC	Flash ROM Interface Data [0:3] / General Purpose I/O 1[0:3]. <ul style="list-style-type: none"> The first functions of these pins are the Flash ROM interface Data [0:3]. The second functions of these pins are the General Purpose I/O Port 1 Bits 0-3. The function configurations of these pins are determined by programming the software configuration registers.
11 – 14	FD[4:7]/ GP1[4:7]/ IRQIN[0:3]	DO8/ DIOD8/ DI	VCC	Flash ROM Interface Data [4:7] / General Purpose I/O 1[4:7] / Interrupt Request Routing Input [0: 3]. <ul style="list-style-type: none"> The first functions of these pins are the Flash ROM interface Data [4:7]. The second functions of these pins are the General Purpose I/O Port 1 Bits 4-7. The third functions of these pins are the Interrupt Request Routing Input [0:3]. The function configurations of these pins are determined by programming the software configuration registers.
16 – 20	FA[0:4]/ GP2[0:4]/ VID_I[0:4]	DO8/ DIOD8/ DI	VCC	Flash ROM Interface Address[0:4] / General Purpose I/O 2[0:4] / Voltage ID Input [0:4]. <ul style="list-style-type: none"> The first functions of these pins are the Flash ROM Interface Address [0:4]. The second functions of these pins are the General Purpose I/O Port 2 Bits 0-4. The third functions of these pins are the Voltage ID Input [0:4]. The function configurations of these pins are determined by programming the software configuration registers.
21 – 23	FA[5:7]/ GP2[5:7]/ VID_O[0:2]	DO8/ DIOD8/ DO8	VCC	Flash ROM Interface Address[5:7] / General Purpose I/O 2[5:7] / Voltage ID Output [0:2]. <ul style="list-style-type: none"> The first functions of these pins are the Flash ROM Interface Address [5:7]. The second functions of these pins are the General Purpose I/O Port 2 Bits 5-7. The third functions of these pins are the Voltage ID Output [0:2]. The function configurations of these pins are determined by programming the software configuration registers.
24 – 25	FA[8:9]/ GP3[0:1]/ VID_O[3:4]	DO8/ DIOD8/ DO8	VCC	Flash ROM Interface Address[8:9] / General Purpose I/O 3[0:1] / Voltage ID Output [3:4]. <ul style="list-style-type: none"> The first functions of these pins are the Flash ROM Interface Address [8:9]. The second functions of these pins are the General Purpose I/O Port 3 Bits 0-1. The third functions of these pins are the Voltage ID Output [3:4]. The function configuration of this pin is determined by programming the software configuration registers.
26 – 31	FA[10:15]/ GP3[2:7]	DO8/ DIOD8	VCC	Flash ROM Interface Address[10:15] / General Purpose I/O 3[2:7]. <ul style="list-style-type: none"> The first functions of these pins are the Flash ROM Interface Address [10:15]. The second functions of these pins are the General Purpose I/O Port 3 Bits 2-7. The function configuration of this pin is determined by programming the software configuration registers.



IT8700F Pin Descriptions

Table 5-11. Pin Description of Flash ROM Interface Signals (cont' d)

Pin(s) No.	Symbol	Attribute	Power	Description
32 – 33	FA[16:17]/ GP5[0:1]	DO8/ DIOD8	VCC	Flash ROM Interface Address[16:17]/ General Purpose I/O 5[0:1]. <ul style="list-style-type: none"> The first function of these pins is Flash ROM Interface address [16:17]. The second function of these pins is General Purpose I/O Port 5 Bits 0-1. The function configurations of these pins are determined by programming the software configuration registers.
34	FRD#/GP52	DO8/ DIOD8	VCC	Flash ROM Interface Read Strobe # / General Purpose I/O 52. <ul style="list-style-type: none"> The first function of this pin is the Flash ROM Interface Read Strobe#. The second function of this pin is the General Purpose I/O Port 5 Bit 2. The function configuration of this pin is determined by programming the software configuration registers.
47	FCS#/GP53/ SCIO	DO8/ DIOD8/ DIOD8	VCC	Flash ROM Interface Chip Select # / General Purpose I/O 53 / Smart Card Serial Data I/O. <ul style="list-style-type: none"> The first function of this pin is the Flash ROM Interface Chip Select #. The second function of this pin is the General Purpose I/O Port 5 Bit 3. The third function of this pin is Smart Card Serial Data I/O. The function configuration of this pin is determined by programming the software configuration registers.
48	FWE#/GP54	DO8/ DIOD8	VCC	Flash ROM Interface Write Enable # / General Purpose I/O 54. <ul style="list-style-type: none"> The first function of this pin is the Flash ROM Interface Write Enable #. The second function of this pin is the General Purpose I/O Port 5 Bit 4. The function configuration of this pin is determined by programming the software configuration registers.

Table 5-12. Pin Description of Miscellaneous Signals

Pin(s) No.	Symbol	Attribute	Power	Description
44	CLKIN	DI	VCC	24 MHz or 48 MHz Clock Input.
87 - 98	NC	-	-	No Connection.



IT8700F

IO Cell:

DO: Digital Output

DO8: 8mA Digital output buffer

DO16: 16mA Digital output buffer

DO40: 48mA Digital output buffer

DOD40: 48mA Digital Open-Drain output buffer

DIOD8: 8mA Digital Open-Drain Input/Output buffer

DIO8: 8mA Digital Input/Output buffer

DIO24: 24mA Digital Input/Output buffer

DI: Digital Input

AI: Analog Input

AO: Analog Output



6. List of GPIO Pins

Table 6-1. General Purpose I/O Group 1

Symbol	Pin #	Attribute	Description
FD0/GP10	7	DO8/ DIOD8	Flash ROM Interface Data 0 / General Purpose I/O Port 1 Bit 0.
FD1/GP11	8	DO8/ DIOD8	Flash ROM Interface Data 1 / General Purpose I/O Port 1 Bit 1.
FD2/GP12	9	DO8/ DIOD8	Flash ROM Interface Data 2 / General Purpose I/O Port 1 Bit 2.
FD3/GP13	10	DO8/ DIOD8	Flash ROM Interface Data 3 / General Purpose I/O Port 1 Bit 3.
FD4/IRQIN0/ GP14	11	DO8/DI/ DIOD8	Flash ROM Interface Data 4 / Interrupt Request Routing Input 0 / General Purpose I/O Port 1 Bit 4.
FD5/IRQIN1/ GP15	12	DO8/DI/ DIOD8	Flash ROM Interface Data 5 / Interrupt Request Routing Input 1 / General Purpose I/O Port 1 Bit 5.
FD6/IRQIN2/ GP16	13	DO8/DI/ DIOD8	Flash ROM Interface Data 6 / Interrupt Request Routing Input 2 / General Purpose I/O Port 1 Bit 6.
FD7/IRQIN3/ GP17	14	DO8/DI/ DIOD8	Flash ROM Interface Data 7 / Interrupt Request Routing Input 3 / General Purpose I/O Port 1 Bit 7.

Table 6-2. General Purpose I/O Group 2

Symbol	Pin #	Attribute	Description
FA0/GP20/ VID_I0	16	DO8/ DIOD8/DI	Flash ROM Interface Address 0 / General Purpose I/O Port 2 Bit 0 / Voltage ID Input 0.
FA1/GP21/ VID_I1	17	DO8/ DIOD8/DI	Flash ROM Interface Address 1 / General Purpose I/O Port 2 Bit 1 / Voltage ID Input 1.
FA2/GP22/ VID_I2	18	DO8/ DIOD8/DI	Flash ROM Interface Address 2 / General Purpose I/O Port 2 Bit 2 / Voltage ID Input 2.
FA3/GP23/ VID_I3	19	DO8/ DIOD8/DI	Flash ROM Interface Address 3 / General Purpose I/O Port 2 Bit 3 / Voltage ID Input 3.
FA4/GP24/ VID_I4	20	DO8/ DIOD8/DI	Flash ROM Interface Address 4 / General Purpose I/O Port 2 Bit 4 / Voltage ID Input 4.
FA5/GP25/ VID_O0	21	DO8/ DIOD8/DO	Flash ROM Interface Address 5 / General Purpose I/O Port 2 Bit 5 / Voltage ID Output 0.
FA6/GP26/ VID_O1	22	DO8/ DIOD8/DO	Flash ROM Interface Address 6 / General Purpose I/O Port 2 Bit 6 / Voltage ID Output 1.
FA7/GP27/ VID_O2	23	DO8/ DIOD8/DO	Flash ROM Interface Address 7 / General Purpose I/O Port 2 Bit 7 / Voltage ID Output 2.

Table 6-3. General Purpose I/O Group 3

Symbol	Pin #	Attribute	Description
FA8/GPIO30 /VID_O3	24	DO8/ DIOD8/DO	Flash ROM Interface Address 8 / General Purpose I/O Port 3 Bit 0 / Voltage ID Output 3.
FA9/GPIO31 /VID_O4	25	DO8/ DIOD8/DO	Flash ROM Interface Address 9 / General Purpose I/O Port 3 Bit 1 / Voltage ID Output 4.
FA10/ GPIO32	26	DO8/ DIOD8	Flash ROM Interface Address 10 / General Purpose I/O Port 3 Bit 2.
FA11/ GPIO33	27	DO8/ DIOD8	Flash ROM Interface Address 11 / General Purpose I/O Port 3 Bit 3.
FA12/ GPIO34	28	DO8/ DIOD8	Flash ROM Interface Address 12 / General Purpose I/O Port 3 Bit 4.
FA13/ GPIO35	29	DO8/ DIOD8	Flash ROM Interface Address 13 / General Purpose I/O Port 3 Bit 5.
FA14/ GPIO36	30	DO8/ DIOD8	Flash ROM Interface Address 14 / General Purpose I/O Port 3 Bit 6.
FA15/ GPIO37	31	DO8/ DIOD8	Flash ROM Interface Address 15 / General Purpose I/O Port 3 Bit 7.

Table 6-4. General Purpose I/O Group 4

Symbol	Pin #	Attribute	Description
JSACX/ GP40	49	DIOD8/ DIOD8	Joystick A Coordinate X / General Purpose I/O Port 4 Bit 0.
JSACY/ GP41	50	DIOD8/ DIOD8	Joystick A Coordinate Y / General Purpose I/O Port 4 Bit 1.
JSAB1/ GP42	51	DI/ DIOD8	Joystick A Button 1 / General Purpose I/O Port 4 Bit 2.
JSAB2/ GP43	52	DI/ DIOD8	Joystick A Button 2 / General Purpose I/O Port 4 Bit 3.
JSBCX/ GP44	53	DIOD8/ DIOD8	Joystick B Coordinate X / General Purpose I/O Port 4 Bit 4.
JSBCY/ GP45	54	DIOD8/ DIOD8	Joystick B Coordinate Y / General Purpose I/O Port 4 Bit 5.
JSBB1/ GP46	55	DI/ DIOD8	Joystick B Button 1 / General Purpose I/O Port 4 Bit 6.
JSBB2/ GP47	56	DI/ DIOD8	Joystick B Button 2 / General Purpose I/O Port 4 Bit 7.

Table 6-5. General Purpose I/O Group 5

Symbol	Pin #	Attribute	Description
FA16/ GP50	32	DO8/ DIOD8	Flash ROM Interface Address 16 / General Purpose I/O Port 5 Bit 0.
FA17/ GP51	33	DO8/ DIOD8	Flash ROM Interface Address 17 / General Purpose I/O Port 5 Bit 1.
FRD#/ GP52	34	DO8/ DIOD8	Flash ROM Interface Read Strobe # / General Purpose I/O Port 5 Bit 2.
FCS#/ GP53/ SCIO	47	DO8/DIOD 8/DIOD8	Flash ROM Interface Chip Select # / General Purpose I/O Port 5 Bit 3 / Smart Card Serial Data I/O.
FWE#/ GP54	48	DO8/ DIOD8	Flash ROM Interface Write Enable # / General Purpose I/O Port 5 Bit 4.
FAN_TAC1/ GP55	73	DI/ DIOD8	Fan Tachometer Input 1 / General Purpose I/O Port 5 Bit 5.
FAN_TAC2/ GP56	74	DI/ DIOD8	Fan Tachometer Input 2 / General Purpose I/O Port 5 Bit 6.
FAN_TAC3/ FA18/GP57	75	DI/DO8/ DIOD8	Fan Tachometer Input 3 / Flash ROM Interface Address 18 / General Purpose I/O Port 5 Bit 7.



List of GPIO Pins

Table 6-6. General Purpose I/O Group 6^{Note}

Symbol	Pin #	Attribute	Description
FAN_CTL1/ GP60	78	DOD8/ DIOD8	Fan Control Output 1 / General Purpose I/O Port 6 Bit 0.
FAN_CTL2/ GP61	79	DOD8/ DIOD8	Fan Control Output 2 / General Purpose I/O Port 6 Bit 1.
FAN_CTL3/ GP62/ SCPFET#	80	DOD8/ DIOD8/ DOD8	Fan Control Output 3 / General Purpose I/O Port 6 Bit 2 / Smart Card Power FET Control Output#.
PME#/GP63/ SCPRES#	81	DOD8/ DIOD8/DI	Power Management Event # / General Purpose I/O Port 6 Bit 3 / Smart Card Present Detect#.
IRTX/GP64	82	DO8/ DIOD8	Infrared Transmit Output / General Purpose I/O Port 6 Bit 4.
IRRX/GP65	83	DI/ DIOD8	Infrared Receive Input / General Purpose I/O Port 6 Bit 5.
CIRTX/ MIDI_OUT/ GP66	84	DO8/ DO8/ DIOD8	Consumer Infrared Transmit Output / MIDI Output / General Purpose I/O Port 6 Bit 6.
CIRRX/ MIDI_IN/ GP67	85	DI/DI/ DIOD8	Consumer Infrared Receive Input / MIDI Input / General Purpose I/O Port 6 Bit 7.

Note: The GPIO registers of these pins are powered by VCC, not VCCH.

Table 6-7. Programming of Pins 82, 83, 84, and 85

Programming Condition			Pin 82
All, 2Ah, Bit 4	LDN4, F4h, Bit 6	LDN7, F0h, Bit 5	
1	X	X	GP64
0	0	X	IRTX
0	1	0	IRTX
0	1	1	CIRTX

Programming Condition		Pin 83
All, 2Ah, Bit 5	LDN4, F4h, Bit 6	
1	X	GP65
0	0	IRRX
0	1	IRRX/CIRRX

Programming Condition		Pin 84
All, 2Ah, Bit 6	LDN4, F4h, Bit 6	
1	X	GP66
0	0	CIRTX
0	1	MIDI_OUT

Programming Condition		Pin 85
All, 2Ah, Bit 7	LDN4, F4h, Bit 6	
1	X	GP67
0	0	CIRRX
0	1	MIDI_IN



7. Power On Strapping Options

Table 7-1. Power On Strapping Options

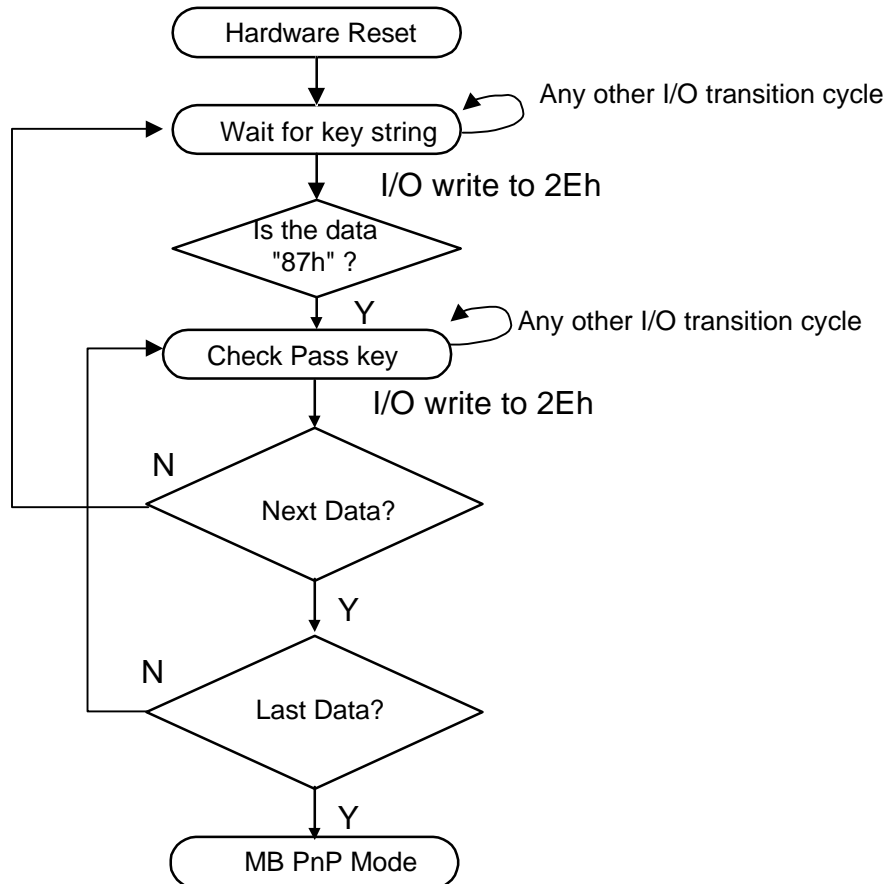
	Symbol	Description
JP1	Flash_Seg1	Flash ROM Interface Address Segment 1 (FFFF0000h-FFFFFFFFh, FFFE0000h-FFFEFFFFFFh) Enable.
JP2	Flash_Seg2	Flash ROM Interface Address Segment 2 (FEEF0000h-FFEEFFFFh, FFEE0000h-FFEEFFFFFFh) Enable.
JP3	Flash_Seg3	Flash ROM Interface Address Segment 3 (FFF80000h-FFFDFFFFh, FFFE0000h-FFFEFFFFFFh) Enable.
JP4	Flash_Seg4	Flash ROM Interface Address Segment 4 (000F0000h-000FFFFFFh, 000E0000h-000EFFFFFFh) Enable.
JP5	4M_Flash_En	4M Flash ROM Enable (Pin 75 is selected as FA18).
JP6	Chip_sel	Chip selection in Configuration.



8. Configuration

8.1 Configuring Sequence Description

After the hardware reset or power-on reset, the IT8700F enters the normal mode with all logical devices disabled.



There are three steps to completing the Motherboard mode of configuration. Step one is to enter the MB PnP mode. Step two is modifying the data of configuration registers. Step three is exiting the MB PnP mode. These three steps are explained below. Please note that step three must be followed or an undefined state will occur.

(1) Enter the MB PnP Mode

To enter the MB PnP Mode, 4 special I/O write operations must be performed during Wait for Key state. To ensure the initial state of the key-check logic, it is necessary to perform four I/O write operations to the Special Address port (2Eh). Two different enter keys are provided to select configuration ports (2Eh/2Fh or 4Eh/4Fh) as required in the next step.

IT8700F



	<u>Address Port</u>	<u>Data Port</u>
87h, 01h, 55h, 55h;	2Eh	2Fh
or 87h, 01h, 55h, AAh;	4Eh	4Fh

(2) Modifying the Data of the Configuration Registers

Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global Configuration registers. All registers can be accessed in this mode.

(3) Exit the MB PnP Mode

Set bit 1 of the Configure Control Register (Index: 02h) to "1" to exit the MB PnP mode.

8.2 Description of the Configuration Registers

All the registers will be reset to the default states when RESET is activated, except LDN=4' s PME registers.

Table 8-1. Global Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
All	02h	W	NA	Configure Control
All	07h	R/W	NA	Logical Device Number(LDN)
All	20h	RO	87h	Chip ID Byte 1
All	21h	RO	05h	Chip ID Byte 2
All	22h	W-RO	00h	Configuration Select and Chip Version
All	23h	R/W	00h	Software Suspend
All	24h	R/W	-	Clock Selection and Flash ROM I/F Control Register
05h ^{*1}	25h	R/W	00h	GPIO Set 1 Multi-Function Pin Selection Register
05h ^{*1}	26h	R/W	00h	GPIO Set 2 Multi-Function Pin Selection Register
05h ^{*1}	27h	R/W	00h	GPIO Set 3 Multi-Function Pin Selection Register
05h ^{*1}	28h	R/W	FFh	GPIO Set 4 Multi-Function Pin Selection Register
05h ^{*1}	29h	R/W	E0h	GPIO Set 5 Multi-Function Pin Selection Register
05h ^{*1}	2Ah	R/W	FFh	GPIO Set 6 Multi-Function Pin Selection Register
F4h ^{*1}	2Eh	R/W	00h	Test Mode Register 1
F4h ^{*1}	2Fh	R/W	00h	Test Mode Register 2


Table 8-2. FDC Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
00h	30h	R/W	00h	FDC Activate
00h	60h	R/W	03h	FDC Base Address MSB Register
00h	61h	R/W	F0h	FDC Base Address LSB Register
00h	70h	R/W	06h	FDC Interrupt Level Select
00h	74h	R/W	02h	FDC DMA Channel Select
00h	F0h	R/W	00h	FDC Special Configuration Register 1
00h	F1h	R/W	00h	FDC Special Configuration Register 2

Table 8-3. Serial Port 1 Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
01h	30h	R/W	00h	Serial Port 1 Activate
01h	60h	R/W	03h	Serial Port 1 Base Address MSB Register
01h	61h	R/W	F8h	Serial Port 1 Base Address LSB Register
01h	70h	R/W	04h	Serial Port 1 Interrupt Level Select
01h	F0h	R/W	00h	Serial Port 1 Special Configuration Register

Table 8-4. Serial Port 2 Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
02h	30h	R/W	00h	Serial Port 2 Activate
02h	60h	R/W	02h	Serial Port 2 Base Address MSB Register
02h	61h	R/W	F8h	Serial Port 2 Base Address LSB Register
02h	70h	R/W	03h	Serial Port 2 Interrupt Level Select
02h	F0h	R/W	00h	Serial Port 2 Special Configuration Register 1
02h	F1h	R/W	50h	Serial Port 2 Special Configuration Register 2
02h	F2h	R/W	00h	Serial Port 2 Special Configuration Register 3
02h	F3h	R/W	7Fh	Serial Port 2 Special Configuration Register 4

Table 8-5. Parallel Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
03h	30h	R/W	00h	Parallel Port Activate
03h	60h	R/W	03h	Parallel Port Primary Base Address MSB Register
03h	61h	R/W	78h	Parallel Port Primary Base Address LSB Register
03h	62h	R/W	07h	Parallel Port Secondary Base Address MSB Register
03h	63h	R/W	78h	Parallel Port Secondary Base Address LSB Register
03h	64h	R/W	00h	POST Data Port Base Address MSB Register
03h	65h	R/W	80h	POST Data Port Base Address LSB Register
03h	70h	R/W	07h	Parallel Port Interrupt Level Select
03h	74h	R/W	03h	Parallel Port DMA Channel Select ²
03h	F0h	R/W	03h ³	Parallel Port Special Configuration Register

Table 8-6. FAN Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
04h	30h	R/W	00h	FAN Controller Activate
04h	60h	R/W	02h	FAN Controller Primary Base Address MSB Register
04h	61h	R/W	90h	FAN Controller Primary Base Address LSB Register
04h	62h	R/W	02h	PME Direct Access Base Address MSB Register
04h	63h	R/W	30h	PME Direct Access Base Address LSB Register
04h	70h	R/W	09h	FAN Controller Interrupt Level Select
04h	F0h	R/W	00h	PME Event Enable Register
04h	F1h	R/W	00h	PME Status Register
04h	F2h	R/W	00h	PME Control Register 1
04h	F3h	R/W	00h	FAN Controller Special Configuration Register
04h	F4h	R-R/W	00h	PME Control Register 2
04h	F5h	R/W	-	PME Special Code Index Register
04h	F6h	R/W	-	PME Special Code Data Register


Table 8-7. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
05h	60h	R/W	00h	Simple I/O Base Address MSB Register
05h	61h	R/W	00h	Simple I/O Base Address LSB Register
05h	62h	R/W	00h	Panel Button De-bounce Base Address MSB Register
05h	63h	R/W	00h	Panel Button De-bounce Base Address LSB Register
05h	64h	R/W	00h	SMI# Normal Run Access Base Address MSB Register
05h	65h	R/W	00h	SMI# Normal Run Access Base Address LSB Register
05h	70h	R/W	00h	Panel Button De-bounce Interrupt Level Select Register
05h	71h	R/W	00h	IRQ Routing Input 0 and 1 Interrupt Level Select Register
05h	72h	R/W	00h	IRQ Routing Input 2 and 3 Interrupt Level Select Register
05h	B0h	R/W	00h	GPIO Set 1 Pin Polarity Register
05h	B1h	R/W	00h	GPIO Set 2 Pin Polarity Register
05h	B2h	R/W	00h	GPIO Set 3 Pin Polarity Register
05h	B3h	R/W	00h	GPIO Set 4 Pin Polarity Register
05h	B4h	R/W	00h	GPIO Set 5 Pin Polarity Register
05h	B5h	R/W	00h	GPIO Set 6 Pin Polarity Register
05h	B8h	R/W	00h	GPIO Set 1 Pin Internal Pull-up Enable Register
05h	B9h	R/W	00h	GPIO Set 2 Pin Internal Pull-up Enable Register
05h	BAh	R/W	00h	GPIO Set 3 Pin Internal Pull-up Enable Register
05h	BBh	R/W	00h	GPIO Set 4 Pin Internal Pull-up Enable Register
05h	BCh	R/W	00h	GPIO Set 5 Pin Internal Pull-up Enable Register
05h	BDh	R/W	00h	GPIO Set 6 Pin Internal Pull-up Enable Register
05h	C0h	R/W	00h	Simple I/O Set 1 Enable Register
05h	C1h	R/W	00h	Simple I/O Set 2 Enable Register
05h	C2h	R/W	00h	Simple I/O Set 3 Enable Register
05h	C3h	R/W	00h	Simple I/O Set 4 Enable Register

Table 8-7. GPIO Configuration Registers [cont' d]

LDN	Index	R/W	Reset	Configuration Registers or Action
05h	C4h	R/W	00h	Simple I/O Set 5 Enable Register
05h	C5h	R/W	00h	Simple I/O Set 6 Enable Register
05h	C8h	R/W	00h	Simple I/O Set 1 Output Enable Register
05h	C9h	R/W	00h	Simple I/O Set 2 Output Enable Register
05h	CAh	R/W	00h	Simple I/O Set 3 Output Enable Register
05h	CBh	R/W	00h	Simple I/O Set 4 Output Enable Register
05h	CCh	R/W	00h	Simple I/O Set 5 Output Enable Register
05h	CDh	R/W	00h	Simple I/O Set 6 Output Enable Register
05h	D0h	R/W	00h	Panel Button De-bounce Control Register
05h	D1h	R/W	00h	Panel Button De-bounce Set 1 Enable Register
05h	D2h	R/W	00h	Panel Button De-bounce Set 2 Enable Register
05h	D3h	R/W	00h	Panel Button De-bounce Set 3 Enable Register
05h	D4h	R/W	00h	Panel Button De-bounce Set 4 Enable Register
05h	D5h	R/W	00h	Panel Button De-bounce Set 5 Enable Register
05h	D6h	R/W	00h	Panel Button De-bounce Set 6 Enable Register
05h	F0h	R/W	00h	SMI# Control Register
05h	F1h	R/W	00h	Reserved
05h	F2h	R/W	00h	SMI# Status Register
05h	F5h	R/W	00h	SMI# Pin Mapping
05h	F6h	R/W	00h	FAN Controller Alert Beep Pin Mapping Register
05h	F7h	R/W	00h	GP LED Blinking 1 Pin Mapping Register
05h	F8h	R/W	00h	GP LED Blinking 1 Control Register
05h	F9h	R/W	00h	GP LED Blinking 2 Pin Mapping Register
05h	FAh	R/W	00h	GP LED Blinking 2 Control Register
05h	FBh	R/W	00h	Watch Dog Timer Control Register
05h	FCh	R/W	00h	Watch Dog Timer Time-out output Pin Mapping Register
05h	FDh	R/W	00h	Watch Dog Timer Time-out Value Register
05h	FEh	RO	--	VID Input Register
05h	FFh	R/W	00h	VID Output Register

Table 8-8. Game Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
06h	30h	R/W	00h	Game Port Activate
06h	60h	R/W	02h	Game Port Base Address MSB Register
06h	61h	R/W	01h	Game Port Base Address LSB Register



Table 8-9. Consumer IR Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
07h	30h	R/W	00h	Consumer IR Activate
07h	60h	R/W	03h	Consumer IR Base Address MSB Register
07h	61h	R/W	10h	Consumer IR Base Address LSB Register
07h	70h	R/W	0Bh	Consumer IR Interrupt Level Select
07h	F0h	R/W	00h	Consumer IR Special Configuration Register

Table 8-10. MIDI Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
08h	30h	R/W	00h	MIDI Port Activate
08h	60h	R/W	03h	MIDI Port Base Address MSB Register
08h	61h	R/W	00h	MIDI Port Base Address LSB Register
08h	70h	R/W	0Ah	MIDI Port Interrupt Level Select
08h	F0h	R/W	00h	MIDI Port Special Configuration Register

Notes:

*1: All these registers can be read from all LDNs.

*2: When the ECP mode is not enabled, this register is **read only** as "04h", and cannot be written.

*3: When the bit 2 of the base address of Parallel Port is set to 1, the EPP mode cannot be enabled. Bit 0 of this register is always 0.

IT8700F**8.2.1 Logical Device Base Address**

The base I/O range of logical devices shown below is located in the base I/O address range of each logical device.

Table 8-11. Base Address of Logical Devices

Logical Devices	Address	Notes
LDN=0 FDC	Base + (2 - 5) and + 7	
LDN=1 SERIAL PORT 1	Base + (0 -7)	
LDN=2 SERIAL PORT 2	Base1 + (0 -7)	COM Port
LDN=3 PARALLEL PORT	Base1 + (0 -3) Base1 + (0 -7) Base1 + (0 -3) and Base2 + (0 -3) Base1 + (0 -7) and Base2 + (0 -3) Base3	SPP SPP+EPP SPP+ECP SPP+EPP+ECP POST Data Port
LDN=4 FAN Controller	Base1 + (0 -7) Base2 + (0 -3)	FAN Controller PME#
LDN=5 GPIO		-
LDN=6 Game Port	Base + (0 -1)	-
LDN=7 Consumer IR	Base + (0 -7)	-
LDN=8 MIDI Port	Base + (0 -1)	-



8.3 Global Configuration Registers (LDN: All)

8.3.1 Configure Control (Index=02h)

This register is **write only**. Its values are not sticky; that is, a hardware reset will automatically clear the bits, and does not require the software to clear them.

Bit	Description
7-2	Reserved
1	Return to the "Wait for Key" state. This bit is used when the configuration sequence is completed.
0	Reset all logical devices and restores configuration registers to their power-on states.

8.3.2 Logical Device Number (LDN, Index=07h)

This **read/write** register is used to select the current logical devices. By reading from or writing to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical devices can be accessed. In addition, the ACTIVATE command is only effective for the selected logical devices.

8.3.3 Chip ID Byte 1 (Index=20h, Default=87h)

This **read only** register is the Chip ID Byte 1. Bits [7:0]=87h when read.

8.3.4 Chip ID Byte 2 (Index=21h, Default=05h)

This **read only** register is the Chip ID Byte 2. Bits [7:0]=05h when read.

8.3.5 Configuration Select and Chip Version (Index=22h, Default=02h)

Bit	Description
7	Configuration Select This bit is used to select the chip, which needed to be configured. When there are two IT8700F chips in a system, to write "1" this bit will select JP6=1 (power-on strapping value of RTS2#) to be configured. The chip with JP6=0 will exit the configuration mode. To write "0", the chip with JP6=0 will be configured and the chip with JP6=1 will exit. If no write on this register, both chips will be configured.
6-4	Reserved
3-0	Version

8.3.6 Software Suspend (Index=23h, Default=00h)

Bit	Description
7-6	SCRPRES# Select 00: Pin 81 01: Pin 79 10: Pin 75 11: Pin 74
5-4	Reserved
0	Software Suspend This register is the Software Suspend register. When the bit 0 is set, the IT8700F enters the "Software Suspend" state. All the devices remain inactive until this bit is cleared or when the wake-up event occurs. The wake-up event occurs at any transition on signals R11# (pin 119) and R12# (pin 127).

IT8700F**8.3.7 Clock Selection and Flash ROM I/F Control Register (Index=24h, Default=sssss000b)**

The default values of bits 7-3 depend on the power-on strapping of JP1-5.

Bit	Description
7	Flash ROM Interface Address Segment 4 (000F0000h-000FFFFFFh, 000E0000h-000EFFFFFFh) Enable
6	Flash ROM Interface Address Segment 3 (FFF80000h-FFFDFFFFh, FFFE0000h-FFFEFFFFFFh) Enable
5	Flash ROM Interface Address Segment 2 (FFEF0000h-FFEFFFFFh, FFEE0000h-FFEEFFFFFFh) Enable
4	Flash ROM Interface Address Segment 1 (FFFF0000h-FFFFFFFFh, FFFE0000h-FFFEFFFFFFh) Enable
3	4M bits Flash ROM Enable (Pin 75 is selected as FA18)
2	Flash ROM I/F Writes Enable
1	Reserved
0	CLKIN Frequency 0: 48 MHz. 1: 24 MHz.

8.3.8 GPIO Set 1 Multi-Function Pin Selection Register (Index=25h, Default=00h)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	Perform the function selection of pin 14 0: Select the Flash ROM Interface Data 7. 1: Select the General Purpose I/O 17.
6	Perform the function selection of pin 13 0: Select the Flash ROM Interface Data 6. 1: Select the General Purpose I/O 16.
5	Perform the function selection of pin 12 0: Select the Flash ROM Interface Data 5. 1: Select the General Purpose I/O 15.
4	Perform the function selection of pin 11 0: Select the Flash ROM Interface Data 4. 1: Select the General Purpose I/O 14.
3	Perform the function selection of pin 10 0: Select the Flash ROM Interface Data 3. 1: Select the General Purpose I/O 13.
2	Perform the function selection of pin 9 0: Select the Flash ROM Interface Data 2. 1: Select the General Purpose I/O 12.
1	Perform the function selection of pin 8 0: Select the Flash ROM Interface Data 1. 1: Select the General Purpose I/O 11.
0	Perform the function selection of pin 7 0: Select the Flash ROM Interface Data 0. 1: Select the General Purpose I/O 10.



8.3.9 GPIO Set 2 Multi-Function Pin Selection Register (Index=26h, Default=00h)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	Perform the function selection of pin 23 0: Select the Flash ROM Interface Address 7. 1: Select the General Purpose I/O 27.
6	Perform the function selection of pin 22 0: Select the Flash ROM Interface Address 6. 1: Select the General Purpose I/O 26.
5	Perform the function selection of pin 21 0: Select the Flash ROM Interface Address 5. 1: Select the General Purpose I/O 25.
4	Perform the function selection of pin 20 0: Select the Flash ROM Interface Address 4. 1: Select the General Purpose I/O 24.
3	Perform the function selection of pin 19 0: Select the Flash ROM Interface Address 3. 1: Select the General Purpose I/O 23.
2	Perform the function selection of pin 18 0: Select the Flash ROM Interface Address 2. 1: Select the General Purpose I/O 22.
1	Perform the function selection of pin 17 0: Select the Flash ROM Interface Address 1. 1: Select the General Purpose I/O 21.
0	Perform the function selection of pin 16 0: Select the Flash ROM Interface Address 0. 1: Select the General Purpose I/O 20.

8.3.10 GPIO Set 3 Multi-Function Pin Selection Register (Index=27h, Default=00h)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	Perform the function selection of pin 31 0: Select the Flash ROM Interface Address15. 1: Select the General Purpose I/O 37.
6	Perform the function selection of pin 30 0: Select the Flash ROM Interface Address 14. 1: Select the General Purpose I/O 36.
5	Perform the function selection of pin 29 0: Select the Flash ROM Interface Address13. 1: Select the General Purpose I/O 35.



IT8700F

8.3.10 GPIO Set 3 Multi-Function Pin Selection Register (Index=27h, Default=00h) [cont' d]

Bit	Description
4	Perform the function selection of pin 28 0: Select the Flash ROM Interface Address 12. 1: Select the General Purpose I/O 34.
3	Perform the function selection of pin 27 0: Select the Flash ROM Interface Address 11. 1: Select the General Purpose I/O 33.
2	Perform the function selection of pin 26 0: Select the Flash ROM Interface Address 10. 1: Select the General Purpose I/O 32.
1	Perform the function selection of pin 25 0: Select the Flash ROM Interface Address 9. 1: Select the General Purpose I/O 31.
0	Perform the function selection of pin 24 0: Select the Flash ROM Interface Address 8. 1: Select the General Purpose I/O 30.

8.3.11 GPIO Set 4 Multi-Function Pin Selection Register (Index=28h, Default=FFh)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	Perform the function selection of pin 56 0: Select the Joystick B Button 2. 1: Select the General Purpose I/O 47.
6	Perform the function selection of pin 55 0: Select the Joystick B Button 1. 1: Select the General Purpose I/O 46.
5	Perform the function selection of pin 54 0: Select the Joystick B Coordinate Y. 1: Select the General Purpose I/O 45.
4	Perform the function selection of pin 53 0: Select the Joystick B Coordinate X. 1: Select the General Purpose I/O 44.
3	Perform the GP43 function of pin 52 0: Select the Joystick A Button 2. 1: Select the General Purpose I/O 43.
2	Perform the function selection of pin 51 0: Select the Joystick A Button 1. 1: Select the General Purpose I/O 42.
1	Perform the function selection of pin 50 0: Select the Joystick A Coordinate Y. 1: Select the General Purpose I/O 41.
0	Perform the function selection of pin 49 0: Select the Joystick A Coordinate X. 1: Select the General Purpose I/O 40.



8.3.12 GPIO Set 5 Multi-Function Pin Selection Register (Index=29h, Default=E0h)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	Perform the function selection of pin 75 If 4M bits Flash ROM (bit 3 of Index 24h register) is enabled, this bit is no used. 0: Select the Fan Tachometer Input 3. 1: Select the General Purpose I/O 57.
6	Perform the function selection of pin 74 0: Select the Fan Tachometer Input 2. 1: Select the General Purpose I/O 56.
5	Perform the function selection of pin 73 0: Select the Fan Tachometer Input 1. 1: Select the General Purpose I/O 55.
4	Perform the function selection of pin 48 0: Select the Flash ROM Interface Write Enable #. 1: Select the General Purpose I/O 54.
3	Perform the function selection of pin 47 0: Select the Flash ROM Interface Chip Select #. 1: Select the General Purpose I/O 53.
2	Perform the function selection of pin 34 0: Select the Flash ROM Interface Read Strobe #. 1: Select the General Purpose I/O 52.
1	Perform the function selection of pin 33 0: Select the Flash ROM Interface Address 17. 1: Select the General Purpose I/O 51.
0	Perform the function selection of pin 32 0: Select the Flash ROM Interface Address 16. 1: Select the General Purpose I/O 50.



IT8700F

8.3.13 GPIO Set 6 Multi-Function Pin Selection Register (Index=2Ah, Default=FFh)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	Perform the function selection of pin 85 0: Select the Consumer Infrared Receive Input (if bit 6 of PCR2 is low) or MIDI Input (if bit 6 of PCR2 is high). 1: Select the General Purpose I/O 67.
6	Perform the function selection of pin 84 0: Select the Consumer Infrared Transmit Output (if bit 6 of PCR2 is low) or MIDI Output (if bit 6 of PCR2 is high). 1: Select the General Purpose I/O 66.
5	Perform the function selection of pin 83 0: Select the Infrared Receive Input. 1: Select the General Purpose I/O 65.
4	Perform the function selection of pin 82 0: Select the Infrared Transmit Output. 1: Select the General Purpose I/O 64.
3	Perform the function selection of pin 81 0: Select the Power Management Event #. 1: Select the General Purpose I/O 63.
2	Perform the function selection of pin 80 0: Select the Fan Control Output 3. 1: Select the General Purpose I/O 62.
1	Perform the function selection of pin 79 0: Select the Fan Control Output 2. 1: Select the General Purpose I/O 61.
0	Perform the function selection of pin 78 0: Select the Fan Control Output 1. 1: Select the General Purpose I/O 60.

8.3.14 Test Mode Register 1 (Index=2Eh, Default=00h)

This register is the Test 1 Register and is reserved for ITE. It should not be set.

8.3.15 Test Mode Register 2 (Index=2Fh, Default=00h)

This register is the Test 2 Register and is reserved for ITE. It should not be set.



8.4 FDC Configuration Registers (LDN=00h)

8.4.1 FDC Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	FDC Enable 0: Disabled. 1: Enabled.

8.4.2 FDC Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	Read only, with "0h" for Base Address [15:12]
3-0	FDC Base Address MSB Mapped as Base Address [11:8].

8.4.3 FDC Base Address LSB Register (Index=61h, Default=F0h)

Bit	Description
7-3	FDC Base Address LSB Read/write, mapped as Base Address[7:3].
2-0	Read only as "000b".

8.4.4 FDC Interrupt Level Select (Index=70h, Default=06h)

Bit	Description
7-4	Reserved with default "0h".
3-0	FDC Interrupt Level Select Select the interrupt level ^{note1} for FDC.

8.4.5 FDC DMA Channel Select (Index=74h, Default=02h)

Bit	Description
7-3	Reserved with default "00h".
2-0	FDC DMA Channel Select Select the DMA channel ^{note2} for FDC.

IT8700F**8.4.6 FDC Special Configuration Register 1 (Index=F0h, Default=00h)**

Bit	Description
7-4	Reserved with default "00h".
3	FDC IRQ Sharing 1: IRQ sharing. 0: Normal IRQ.
2	Floppy A/B Swap 1: Swap Floppy Drives A, B. 0: Normal.
1	3 mode/AT Mode 1: 3-mode. 0: AT mode.
0	Software Write Protect 1: Software Write Protect. 0: Normal.

8.4.7 FDC Special Configuration Register 2 (Index=F1h, Default=00h)

Bit	Description
7-4	Reserved with default "0000b".
3-2	FDD B Data Rate Table Select (DRT1-0)
1-0	FDD A Data Rate Table Select (DRT1-0)

8.5 Serial Port 1 Configuration Registers (LDN=01h)**8.5.1 Serial Port 1 Activate (Index=30h, Default=00h)**

Bit	Description
7-1	Reserved
0	Serial Port 1 Enable 1: Enabled. 0: Disabled.

8.5.2 Serial Port 1 Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12].
3-0	Serial Port 1 Base Address MSB Read/write , mapped as Base Address[11:8].



8.5.3 Serial Port 1 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	Serial Port 1 Base Address LSB Read/write, mapped as Base Address[7:3].
2-0	Read only as "000b".

8.5.4 Serial Port 1 Interrupt Level Select (Index=70h, Default=04h)

Bit	Description
7-4	Reserved: default = "0h."
3-0	Serial Port 1 Interrupt Level Select Select the interrupt level ^{note1} for Serial Port 1.

8.5.5 Serial Port 1 Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-3	Reserved: default = "00h".
2-1	Clock Source 00: 24 MHz/13 (Standard). Others: Reserved.
0	IRQ Sharing Enable 1: IRQ sharing. 0: Normal.

8.6 Serial Port 2 Configuration Registers (LDN=02h)

8.6.1 Serial Port 2 Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Serial Port 2 Enable 1: Enabled. 0: Disabled.

8.6.2 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	Read only: with "0h" for Base Address[15:12].
3-0	Serial Port 2 Base Address MSB Read/write, mapped as Base Address[11:8].



IT8700F

8.6.3 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	Serial Port 2 Base Address LSB Read/write, mapped as Base Address[7:3].
2-0	Read only: as "000b".

8.6.4 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h)

Bit	Description
7-4	Reserved with default "0h".
3-0	Serial Port 2 Interrupt Level Select Select the interrupt level ^{note1} for Serial Port 2.

8.6.5 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-3	Reserved: with default "00h".
2-1	Clock Source 00: 24 MHz/13 (Standard). Others: Reserved.
0	IRQ Sharing Enable 1: IRQ sharing. 0: Normal.

8.6.6 Serial Port 2 Special Configuration Register 2 (Index=F1h, Default=50h)

Bit	Description
7	IR Rx2Tx Delay Mode 1: No transmission delays (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode. 0: Transmission delays (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode.
6	IR Tx2Rx Delay Mode 1: No reception delays (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode. 0: Reception delays (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode.
5	Reserved
4	Half Duplex Enable 1: Half Duplex (default). 0: Full Duplex.
3	Reserved
2-0	UART 2 Function Select 000: Standard 001: IrDA SIR 010: ASKIR 100 : Smart Card Reader (SCR) Others: Reserved



8.6.7 Serial Port 2 Special Configuration Register 3 (Index=F2h, Default=00h)

Bit	Description
7	COM_PNP_EN 0: Disable COM Port device Plug-and-Play operation (default). 1: Enable COM Port device Plug-and-Play operation.
6-5	Reserved
4	PNP_ID This bit is only available when bit 7=1. 0: PNP_ID Access mode (default). 1: Normal Plug-and-Play operation mode.
3	Reserved
2	SCPFET# Polarity 0: Active low (default). 1: Active high.
1-0	SCR Clock Select 00: Stop 01: 3.5 MHz 10: 7.1 MHz 11: Special Divisor (96 MHz/DIV96M)

8.6.8 Serial Port 2 Special Configuration Register 4 (Index=F3h, Default=7Fh)

Bit	Description
7	Reserved
6-0	SCR Clock Special Divisor (DIV96M) When the SCR Clock Select is 11b, the SCCLK output clock frequency is 96MHz / DIV96M.

8.7 Parallel Port Configuration Registers (LDN=03h)

8.7.1 Parallel Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Parallel Port Enable 1: Enabled. 0: Disabled.

8.7.2 Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12].
3-0	Base Address MSB Read/write , mapped as Base Address[11:8].

IT8700F



8.7.3 Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h)

If the bit 2 is set to 1, the EPP mode is disabled automatically.

Bit	Description
7-2	Base Address LSB Read/write, mapped as Base Address[7:2].
1-0	Read only as "00b".

8.7.4 Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12].
3-0	Secondary Base Address MSB Read/write, mapped as Base Address[11:8].

8.7.5 Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h)

Bit	Description
7-2	Secondary Base Address LSB Read/write, mapped as Base Address[7:2].
1-0	Read only as "00b".

8.7.6 POST Data Port Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12].
3-0	POST Data Port Base Address MSB Read/write, mapped as Base Address[11:8].

8.7.7 POST Data Port Base Address LSB Register (Index=65h, Default=80h)

Bit	Description
7-0	POST Data Port Base Address LSB Read/write, mapped as Base Address[7:0].

8.7.8 Parallel Port Interrupt Level Select (Index =70h, Default=07h)

Bit	Description
7-4	Reserved with default "0h".
3-0	Interrupt Level Select Select the interrupt level ^{note1} for Parallel Port.



8.7.9 Parallel Port DMA Channel Select (Index=74h, Default=03h)

Bit	Description
7-3	Reserved with default "00h".
2-0	DMA Channel Select Select the DMA channel ^{note2} for Parallel Port.

8.7.10 Parallel Port Special Configuration Register (Index=F0h, Default=03h)

Bit	Description
7-4	Reserved
3	POST Data Port Disable 1: POST Data Port Disable. 0: POST Data Port Enable.
2	IRQ Sharing Enable 1: IRQ sharing. 0: Normal.
1-0	Parallel Port Mode 00: SPP (Standard Parallel Port mode) 01: SPP & EPP (Enhanced Parallel Port) 10: SPP & ECP (Extended Capabilities Parallel Port) 11: SPP & EPP & ECP

If the bit 1 is set, ECP mode is enabled. If the bit 0 is set, EPP mode is enabled. These two bits are independent. However, according to the EPP spec., when Parallel Port Primary Base Address bit 2 is set to 1, the EPP mode cannot be enabled.

8.8 FAN Controller Configuration Registers (LDN=04h)

8.8.1 FAN Controller Activate Register (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	FAN Controller Enable 1: Enabled. 0: Disabled.

8.8.2 FAN Controller Primary Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12].
3-0	Read/write , mapped as Base Address[11:8].

8.8.3 FAN Controller Primary Base Address LSB Register (Index=61h, Default=90h)

Bit	Description
7-3	Read/write , mapped as Base Address[7:3].
2-0	Read only as "000b".



IT8700F

8.8.4 PME Direct Access Base Address MSB Register (Index=62h, Default=02h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12].
3-0	PME Base Address MSB Read/write , mapped as Base Address[11:8].

8.8.5 PME Direct Access Base Address LSB Register (Index=63h, Default=30h)

Bit	Description
7-3	PME Base Address LSB Read/write , mapped as Base Address[7:3].
2-0	Read only as "000b".

8.8.6 FAN Controller Interrupt Level Select (Index=70h, Default=09h)

Bit	Description
7-4	Reserved with default "0h".
3-0	Interrupt Level Select Select the interrupt level ^{note1} for FAN Controller.

8.8.7 PME Event Enable Register (Index=F0h, Default=00h)

Bit	Description
7	It is set to 1 when VCCH is OFF. Writing 1 to clear this bit. This bit is ineffective when a "0" is written to this bit.
6-3	Reserved
2	RI2# Event Enable 1: RI2# event enabled. 0: RI2# event disabled.
1	RI1# Event Enable 1: RI1# event enabled. 0: RI1# event disabled.
0	CIR Event Enable 1: CIR event enabled. 0: CIR event disabled.



8.8.8 PME Status Register (Index=F1h, Default=00h)

Bit	Description
7	It is set to 1 when VCC is ON during previous AC power failure, and 0 when VCC power is OFF.
6-3	Reserved
2	R12# Event Detected 1: R12# event detected. 0: R12# event undetected.
1	R11# Event Detected 1: R11# event detected. 0: R11# event undetected.
0	CIR Event Detected 1: CIR event detected. 0: CIR event undetected.

8.8.9 PME Control Register 1 (PCR 1) (Index=F2h, Default=00h)

Bit	Description
7	PER and PSR Normal Run Access Enable
6-0	Reserved

8.8.10 FAN Controller Special Configuration Register (Index=F3h, Default=00h)

Bit	Description
7-1	Reserved
0	IRQ Sharing Enable 1: IRQ sharing. 0: Normal.

8.8.11 PME Control Register 2 (PCR2) (Index=F4h, Default=00h)

Bit	Description
7	Reserved
6	This bit is active when the related pins are not selected as GPIO function. 1: SIR/ASKIR and CIR ports use the same pins (Pin 82 and Pin 83). Pins 84 and 85 are defined at MIDI port. 0: Pins 82 and 83 are defined at SIR/ASKIR port, and pins 84 and 85 are defined at CIR port.
5-0	Reserved

8.8.12 PME Special Code Index Register (Index=F5h)

Bit	Description
7-6	Reserved (should be filled "00b").
5-0	Indicate which Identification Key Code or CIR code register is to be read/written via 0xF6.

IT8700F



8.8.13 PME Special Code Data Register (Index=F6h)

There are 20 CIR event codes (Index 20h-32h) stored in this port. The index pointer is changed by PME Special Code Index Register. The first byte (Index 20h) is used to specify the pattern length in bytes. Bits[7:4] are used when VCC is ON, and bits[3:0] are used when VCC goes OFF. The minimum byte number is 3 (when bits[7:4] or bits[3:0]=0h), and the maximum byte number is 18 (when bits[7:4] or bits[3:0] =Fh).

8.9 GPIO Configuration Registers (LDN=05h)

8.9.1 Simple I/O Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address [15:12].
3-0	Simple IO Base Address MSB Read/write, mapped as Base Address [11:8].

8.9.2 Simple I/O Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-0	Simple IO Base Address LSB Read/write, mapped as Base Address[7:0].

8.9.3 Panel Button De-bounce Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address [15:12].
3-0	P.B.D Base Address MSB Read/write, mapped as Base Address [11:8].

8.9.4 Panel Button De-bounce Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-0	P.B.D Base Address LSB Read/write, mapped as Base Address[7:0].

8.9.5 SMI# Normal Run Access Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address [15:12].
3-0	SMI Base Address MSB Read/write, mapped as Base Address [11:8].

8.9.6 SMI# Normal Run Access Base Address LSB Register (Index=65h, Default=00h)

Bit	Description
7-0	SMI Base Address LSB Read/write, mapped as Base Address[7:0].



8.9.7 Panel Button De-bounce Interrupt Level Select Register (Index=70h, Default=00h)

Bit	Description
7-4	Reserved
3-0	P.B.D Interrupt Level Select Select the interrupt level ^{note1} for Panel Button De-bounce.

8.9.8 IRQ Routing Input 0 and 1 Interrupt Level Select Register (Index=71h, Default=00h)

Bit	Description
7-4	IRQIN1 Interrupt Level Select Select the interrupt level ^{note1} for IRQIN1.
3-0	IRQIN0 Interrupt Level Select Select the interrupt level ^{note1} for IRQIN0.

8.9.9 IRQ Routing Input 2 and 3 Interrupt Level Select Register (Index=72h, Default=00h)

Bit	Description
7-4	IRQIN3 Interrupt Level Select Select the interrupt level ^{note1} for IRQIN3.
3-0	IRQIN2 Interrupt Level Select Select the interrupt level ^{note1} for IRQIN2.

8.9.10 GPIO Pin Set 1, 2, 3, 4, 5 and 6 Polarity Registers (Index=B0h, B1h, B2h, B3h, B4h and B5h, Default=00h)

These registers are used to program the GPIO pin type as either polarity inverting or non-inverting.

Bit	Description
7-0	GPIO Polarity Inverting For each bit: 1: GPIO pin type is polarity inverting. 0: GPIO pin type is polarity non-inverting.



IT8700F

8.9.11 GPIO Pin Set 1, 2, 3, 4, 5 and 6 Pin Internal Pull-up Enable Registers (Index=B8h, B9h, BAh, BBh, BCh and BDh, Default=00h)

These registers are used to enable the GPIO pin internal pull-up.

Bit	Description
7-0	GPIO Pull-up Enable For each bit: 1: Enable GPIO pin internal pull-up. 0: Disable GPIO pin internal pull-up.

8.9.12 Simple I/O Set 1, 2, 3, 4, 5 and 6 Enable Registers (Index=C0h, C1h, C2h, C3h, C4h and C5h, Default=00h)

These registers are used to select the functions of either the Simple I/O or the Alternate function.

Bit	Description
7-0	Simple GPIO Enable For each bit: 1: Select the Simple I/O function. 0: Select the Alternate function.

8.9.13 Simple I/O Set 1, 2, 3, 4, 5 and 6 Output Enable Registers (Index=C8h, C9h, CAh, CBh, CCh and CDh, Default=00h)

These registers are used to determine the direction of the Simple I/O.

Bit	Description
7-0	GPIO Output Enable For each bit: 0: The direction of the Simple I/O is input mode. 1: The direction of the Simple I/O is output mode.

8.9.14 Panel Button De-bounce Control Register (Index=D0h, Default=00h)

Bit	Description
7-5	Reserved
4	IRQ Sharing 0: Disabled. 1: Enabled.
3	IRQ Output Type 0: Edge. 1: Level.
2	IRQ Output Enable 0: Disabled. 1: Enabled.
1-0	De-bounce Time Selection 00: 8 ms (6 ms ignored, 8 ms passed) 01: 16 ms (12 ms ignored, 16 ms passed) 10: 32 ms (24 ms ignored, 21 ms passed) 11: 64 ms (48 ms ignored, 64 ms passed)



8.9.15 Panel Button De-bounce Set 1, 2, 3, 4, 5 and 6 Enable Registers (Index=D1h, D2h, D3h, D4h, D5h and D6h, Default=00h)

These registers are used to enable Panel Button De-bounce for each pin.

Bit	Description
7-0	P.B.D Enable For each bit: 1: Enable Panel Button De-bounce. 0: Disable Panel Button De-bounce

8.9.16 SMI# Control Register (Index=F0h, Default=00h)

Bit	Description
7	Reserved
6	SMI# of MIDI IRQ Enable Enable the generation of an SMI# due to MIDI Port's IRQ (EN_CIRQ).
5	SMI# of CIR IRQ Enable Enable the generation of an SMI# due to CIR's IRQ (EN_CIRQ).
4	SMI# of FAN Controller IRQ Enable Enable the generation of an SMI# due to FAN Controller's IRQ (EN_ECIRQ).
3	SMI# of PPORT IRQ Enable Enable the generation of an SMI# due to Parallel Port's IRQ (EN_PIRQ).
2	SMI# of UART2 IRQ Enable Enable the generation of an SMI# due to Serial Port 2's IRQ (EN_S2IRQ).
1	SMI# of UART1 IRQ Enable Enable the generation of an SMI# due to Serial Port 1's IRQ (EN_S1IRQ).
0	SMI# of FDC IRQ Enable Enable the generation of an SMI# due to FDC's IRQ (EN_FIRQ).

8.9.17 SMI# Status Register (Index=F2h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7	Reserved
6	The generation of an SMI# due to MIDI Port's IRQ.
5	The generation of an SMI# due to CIR's IRQ.
4	The generation of an SMI# due to FAN Controller's IRQ.
3	The generation of an SMI# due to Parallel Port's IRQ.
2	The generation of an SMI# due to Serial Port 2's IRQ.
1	The generation of an SMI# due to Serial Port 1's IRQ.
0	The generation of an SMI# due to FDC's IRQ.



IT8700F

8.9.18 SMI# Pin Mapping Register (Index=F5h, Default=00h)

Bit	Description
7	Reserved
6	SMI# Direct Access Enable 0: Disable SMI# Direct Access (default) 1: Enable SMI# Direct Access.
5-0	SMI# Pin Location Please see Location mapping table ^{note3} .

8.9.19 FAN Controller Alert Beep Pin Mapping Register (Index=F6h, Default=00h)

Bit	Description
7-6	Reserved
5-0	FAN Controller Alert Beep Pin Location Please see Location mapping table ^{note3} .

8.9.20 GP LED Blinking 1 Pin Mapping Register (Index=F7h, Default=00h)

Bit	Description
7-6	Reserved
5-0	GP LED Blinking 1 Pin Location Please see Location mapping table ^{note3} .

8.9.21 GP LED Blinking 1 Control Register (Index=F8h, Default=00h)

Bit	Description
7-4	Reserved
3	GP LED Blinking 1 Active Pulse Control 0: 1/2 duty (default) 1: short active pulse.
2-1	GP LED Blinking 1 Frequency Select 00: 4 Hz (default) 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	GP LED Blinking 1 Active Mode 0: Blinking mode (default). 1: Always active.

8.9.22 GP LED Blinking 2 Pin Mapping Register (Index=F9h, Default=00h)

Bit	Description
7-6	Reserved
5-0	GP LED Blinking 2 Pin Location Please see Location mapping table ^{note3} .



8.9.23 GP LED Blinking 2 Control Register (Index=FAh, Default=00h)

Bit	Description
7-4	Reserved
3	GP LED Blinking 2 Active Pulse Control 0: 1/2 duty (default). 1: short active pulse.
2-1	GP LED Blinking 2 Frequency Select 00: 4 Hz (default) 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	GP LED Blinking 2 Active Mode 0: Blinking mode (default). 1: Always active.

8.9.24 Watch Dog Timer Control Register (Index=FBh, Default=00h)

Bit	Description
7	CIR Interrupt to Reset WDT Counter Enable 0: Disable a CIR Interrupt to reset WDT Counter (default). 1: Enable a CIR Interrupt to reset WDT Counter.
6-5	Reserved
4	A read from or write to the Game Port Base Address to Reset WDT Counter Enable 0: Disable a read from or write to Game port base address to reset WDT Counter (default). 1: Enable a read from or write to Game port base address to reset WDT Counter.
3	WDT Counter Unit Select 0: Minute (default). 1: Second.
2	Reserved
1	Direct Time Out Control This bit is self-clearing. 0: Normal (default). 1: Direct Time out regardless of the counter.
0	WDT Status 0: No time-out after last re-load counter value (default). 1: The timer was time-out.

8.9.25 Watch Dog Timer Time-out Output Pin Mapping Register (Index=FCh, Default=00h)

Bit	Description
7-6	Reserved
5-0	Watch Dog Timer Time-out Output Pin Location Please see Location mapping table ^{note3} .

8.9.26 Watch Dog Timer Time-out Value Register (Index=FDh, Default=00h)

Bit	Description
7-0	Watch Dog Timer Time-out Value Watch Dog Timer Counter Time-out value (1~256 unit(s)).

IT8700F**8.9.27 VID Input Register (Index=FEh, Default= --)**

Bit	Description
7-5	Reserved
4-0	VID_I[4:0] These bits are read-only. When read, they will perform the states of pins VID_I[4:0].

8.9.28 VID Output Register (Index=FFh, Default=00h)

Bit	Description
7	VID_O[4:0] Output Select 0: Translate VID_I[4:1] directly (default). 1: Output the desired value (bits [4:0] of this register).
6-5	Reserved
4-0	Output Value of VID_O[4:0] These bits are desired output value of VID_O[4:0].

8.10 Game Port Configuration Registers (LDN=06h)**8.10.1 Game Port Activate (Index=30h, Default=00h)**

Bit	Description
7-1	Reserved
0	Game Port Enable 1: Enabled. 0: Disabled.

8.10.2 Game Port Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	Read only with "0h" for Base Address[15:12].
3-0	Game Port Base Address MSB Read/write , mapped as Base Address[11:8].

8.10.3 Game Port Base Address LSB Register (Index=61h, Default=01h)

Bit	Description
7-0	Game Port Base Address LSB Read/write , mapped as Base Address[7:0].

8.11 Consumer IR Configuration Registers (LDN=07h)**8.11.1 Consumer IR Activate (Index=30h, Default=00h)**

Bit	Description
7-1	Reserved
0	Consumer IR Enable 1: Enabled. 0: Disabled.



8.11.2 Consumer IR Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	Read only with "0h" for Base Address[15:12].
3-0	CIR Base Address MSB Read/write , mapped as Base Address[11:8].

8.11.3 Consumer IR Base Address LSB Register (Index=61h, Default=10h)

Bit	Description
7-3	CIR Base Address LSB Read/write , mapped as Base Address[7:3].
2-0	Read only as "000b".

8.11.4 Consumer IR Interrupt Level Select (Index=70h, Default=0Bh)

Bit	Description
7-4	Reserved with default "0h".
3-0	CIR Interrupt Level Select Select the interrupt level ^{note1} for Consumer IR.

8.11.5 Consumer IR Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-1	Reserved with default "00h".
0	1: IRQ sharing. 0: Normal.

8.12 MIDI Port Configuration Registers (LDN=08h)

8.12.1 MIDI Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	MIDI Port Enable 1: Enabled. 0: Disabled.

8.12.2 MIDI Port Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	Read only with "0h" for Base Address[15:12].
3-0	MIDI Base Address MSB Read/write , mapped as Base Address[11:8].



IT8700F

8.12.3 MIDI Port Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-1	MIDI Base Address LSB Read/write, mapped as Base Address[7:3].
0	Read only as "000b".

8.12.4 MIDI Port Interrupt Level Select (Index=70h, Default=0Ah)

Bit	Description
7-4	Reserved with default "0h".
3-0	MIDI Port Interrupt Level Select Select the interrupt level ^{note1} for MIDI port.

8.12.5 MIDI Port Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-6	MID_IN Location Select 00: Pin 85. Please refer to Section 6 (default) 01: Pin 79 10: Pin 74 11: Pin 7
5-4	MID_OUT Location Select 00: Pin 84. Please refer to Section 6 (default) 01: Pin 78 10: Pin 73 11: Pin 8
3	FIFO Disable 0: Enabled (default). 1: Disabled.
2-1	Receive FIFO Trigger Level 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes
0	MIDI Port Interrupt Mode Select 0: Normal (default). 1: IRQ sharing.



Note 1: Interrupt Level Mapping

Fh-Dh: not valid
Ch: IRQ12

3h: IRQ3
2h: not valid
1h: IRQ1
0h: no interrupt selected

Note 2: DMA Channel Mapping

7h-5h: not valid
4h: no DMA channel selected
3h: DMA3
2h: DMA2
1h: DMA1
0h: DMA0

Note 3: Location Mapping Table

Location	Description
001 000	GP10 (pin 7)
001 001	GP11 (pin 8)
001 010	GP12 (pin 9)
001 011	GP13 (pin 10)
001 100	GP14 (pin 11)
001 101	GP15 (pin 12)
001 110	GP16 (pin 13)
001 111	GP17 (pin 14)
010 000	GP20 (pin 16)
010 001	GP21 (pin 17)
010 010	GP22 (pin 18)
010 011	GP23 (pin 19)
010 100	GP24 (pin 20)
010 101	GP25 (pin 21)
010 110	GP26 (pin 22)
010 111	GP27 (pin 23)
011 000	GP30 (pin 24)
011 001	GP31 (pin 25)
011 010	GP32 (pin 26)
011 011	GP33 (pin 27)
011 100	GP34 (pin 28)
011 101	GP35 (pin 29)

IT8700F**Note 3: Location Mapping Table [cont' d]**

Location	Description
011 110	GP36 (pin 30)
011 111	GP37 (pin 31)
100 000	GP40 (pin 49)
100 001	GP41 (pin 50)
100 010	GP42 (pin 51)
100 011	GP43 (pin 52)
100 100	GP44 (pin 53)
100 101	GP45 (pin 54)
100 110	GP46 (pin 55)
100 111	GP47 (pin 56)
101 000	GP50 (pin 32)
101 001	GP51 (pin 33)
101 010	GP52 (pin 34)
101 011	GP53 (pin 47)
101 100	GP54 (pin 48)
101 101	GP55 (pin 73)
101 110	GP56 (pin 74)
101 111	GP57 (pin 75)
110 000	GP60 (pin 78), powered by VCCH
110 001	GP61 (pin 79), powered by VCCH
110 010	GP62 (pin 80), powered by VCCH
110 011	GP63 (pin 81), powered by VCCH
110 100	GP64 (pin 82), powered by VCCH
110 101	GP65 (pin 83), powered by VCCH
110 110	GP66 (pin 84), powered by VCCH
110 111	GP67 (pin 85), powered by VCCH
else	Reserved