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IT8212F

IDE RAID Controller

Preliminary Specification V0.3

INTEGRATED TECHNOLOGY EXPRESS, INC.

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1. Features

- **RAID Function**
  - Compatible with the ATA/ATAPI-6 specification and supports two IDE channels with 4 drives
  - Supports ANSI ATA proposal PIO Modes 0, 1, 2, 3, 4 with flow control, DMA Modes 0, 1, 2 and Ultra DMA modes 0, 1, 2, 3, 4, 5, 6
  - Programmable active pulses and recovery time for data port access timing
  - 512 bytes FIFO for data transfer per IDE channel
  - Supports RAID 0/1/0+1 function
  - Supports JBOD function
  - Supports Scatter/Gather function for DMA/UDMA transfer
  - Supports pre-fetch and post-write function for PIO mode per IDE channel
  - Includes one embedded CPU and firmware on our chip to handle the RAID function. It can reduce the driver's loading and improve the system's stability
- **PCI Interface**
  - Host interface compiles with PCI local bus specification revision 2.2
  - Supports PCI Power Management v1.1 capability
  - Supports one Flash/ROM interface for expansion ROM of the PCI card
- **Miscellaney**
  - Supports the drivers for Windows 98SE/Me/XP, Windows NT 4.0, Windows 2000 and Linux
- **128-pin PQFP**

2. General Description

The IDE RAID controller, which is compatible with the ATA/ATAPI-6 specification and supports the IDE RAID 0/1/0+1 function, acts as an interface between the system and IDE device. It supports not only a Scatter/Gather DMA mechanism that complies with the Programming Interface for Bus Master IDE Controller Revision 1.0 but also 2 IDE channels and up to 4 IDE devices.

Different from using traditional software to handle the RAID function, IT8212F features one embedded CPU and firmware to handle it. The methodology is able to improve the system's stability and reduce the drivier's loading.

IT8212F is availabe in the 128-pin PQFP package.

3. System Block Diagram

3.1 Block Diagram

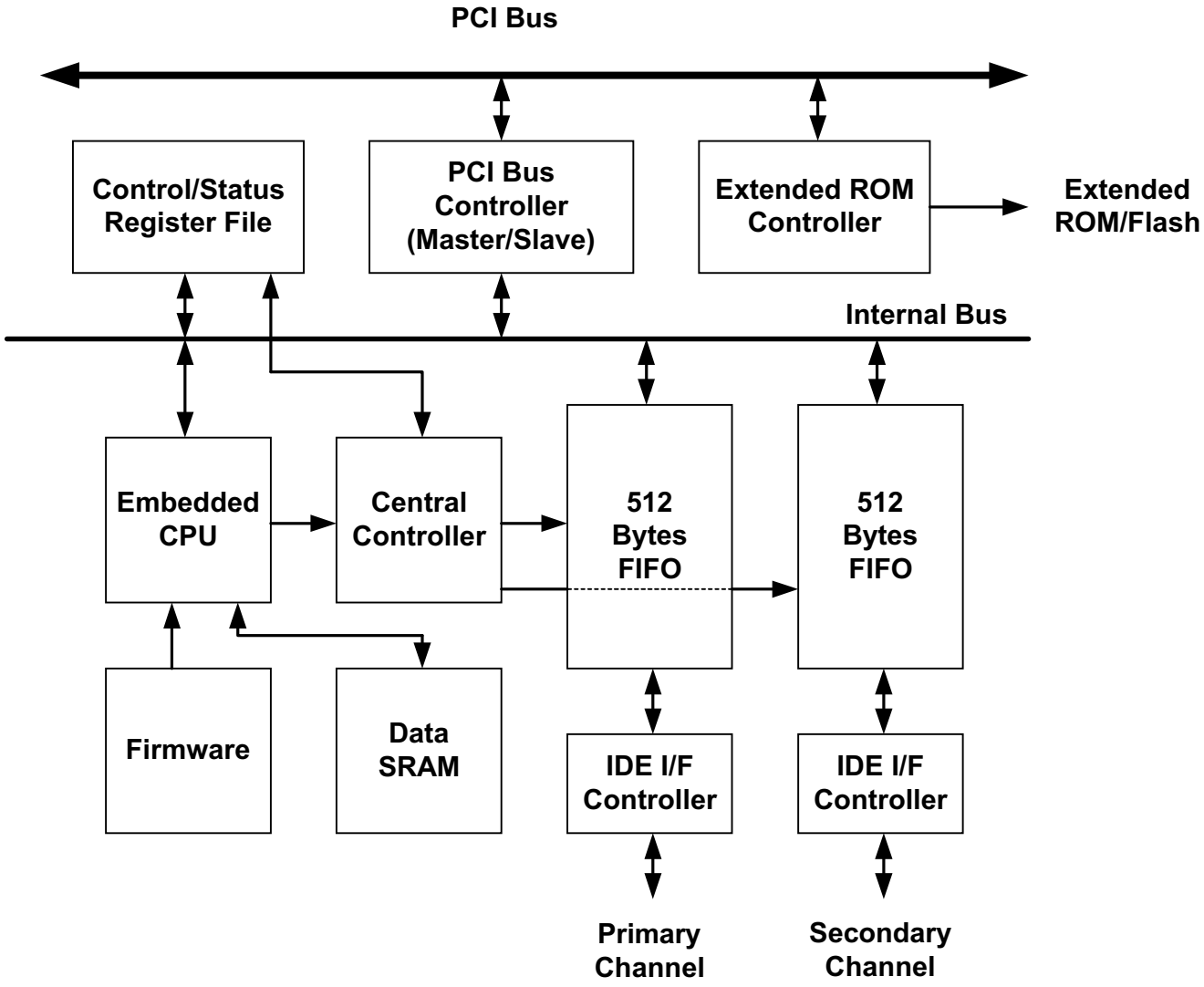


Figure 3-1. Block Diagram

3.2 System Address Space

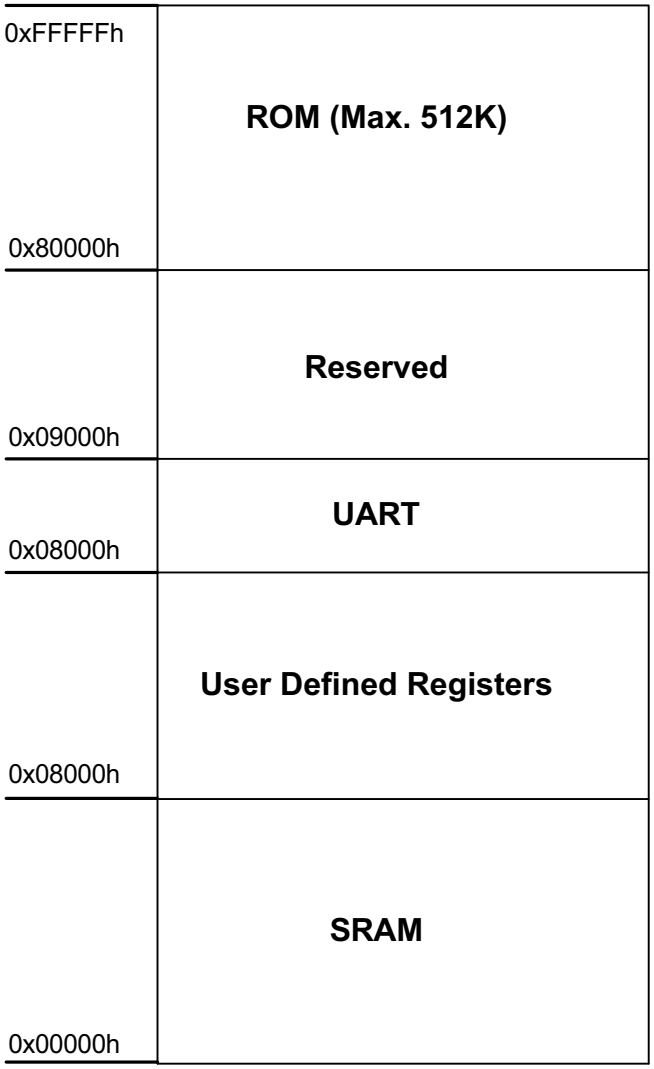


Figure 3-2. System Address Space

4. Pin Configuration

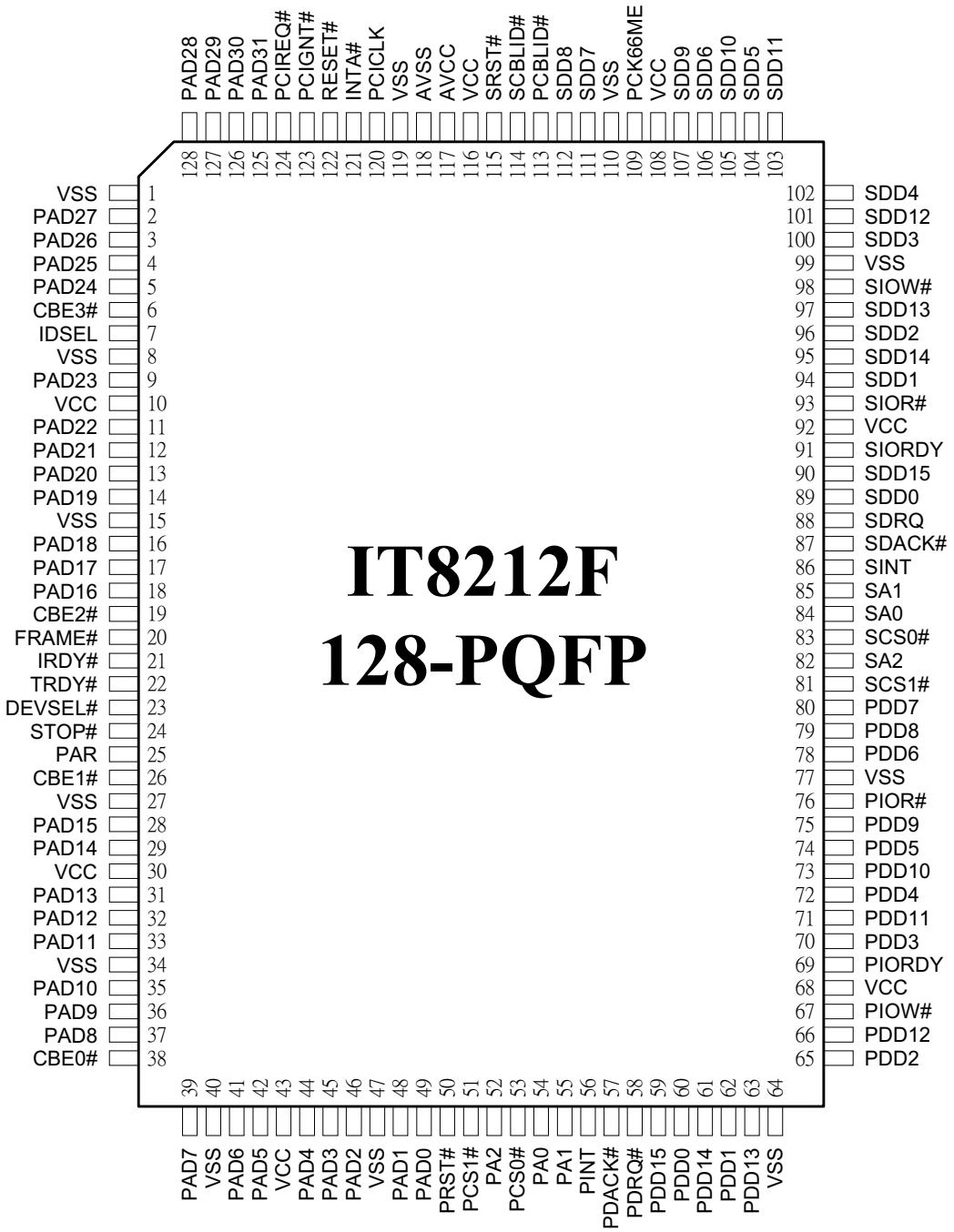


Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VSS	33	PAD11	65	PDD2 / FD2	97	SDD13
2	PAD27	34	VSS	66	PDD12 / FA4	98	SIOW#
3	PAD26	35	PAD10	67	PIOW#	99	VSS
4	PAD25	36	PAD9	68	VCC	100	SDD3
5	PAD24	37	PAD8	69	PIORDY	101	SDD12
6	CBE3#	38	CBE0#	70	PDD3 / FD3	102	SDD4
7	IDSEL	39	PAD7	71	PDD11 / FA3	103	SDD11
8	VSS	40	VSS	72	PDD4 / FD4	104	SDD5
9	PAD23	41	PAD6	73	PDD10 / FA2	105	SDD10
10	VCC	42	PAD5	74	PDD5 / FD5	106	SDD6
11	PAD22	43	VCC	75	PDD9 / FA1	107	SDD9
12	PAD21	44	PAD4	76	PIOR#	108	VCC
13	PAD20	45	PAD3	77	VSS	109	PCK66ME
14	PAD19	46	PAD2	78	PDD6 / FD6	110	VSS
15	VSS	47	VSS	79	PDD8 / FA0	111	SDD7
16	PAD18	48	PAD1	80	PDD7 / FD7	112	SDD8
17	PAD17	49	PAD0	81	SCS1# / FOE#	113	PCBLID#
18	PAD16	50	PRST#	82	SA2 / FA11	114	SCBLID#
19	CBE2#	51	PCS1# / FA13	83	SCS0# / FWE#	115	SRST#
20	FRAME#	52	PA2 / FA10	84	SA0 / FA16	116	VCC
21	IRDY#	53	PCS0# / FA12	85	SA1 / FA15	117	AVCC
22	TRDY#	54	PA0 / FA8	86	SINT	118	AVSS
23	DEVSEL#	55	PA1 / FA9	87	SDACK#	119	VSS
24	STOP#	56	PINT	88	SDRQ	120	PCICLK
25	PAR	57	PDACK#	89	SDD0	121	INTA#
26	CBE1#	58	PDRQ#	90	SDD15 / FA14	122	RESET#
27	VSS	59	PDD15 / FA7	91	SIORDY	123	PCIGNT#
28	PAD15	60	PDD0 / FD0	92	VCC	124	PCIREQ#
29	PAD14	61	PDD14 / FA6	93	SIOR#	125	PAD31
30	VCC	62	PDD1 / FD1	94	SDD1	126	PAD30
31	PAD13	63	PDD13 / FA5	95	SDD14	127	PAD29
32	PAD12	64	VSS	96	SDD2	128	PAD28

5. IT8212F Pin Descriptions

Table 5-1. Pin Descriptions of PCI Bus Interface

Signal	Pin(s) No.	Attribute	Description
PCI Bus Interface (3.3V CMOS I/F, 5V tolerant)			
RESET#	**122**	PI	***System Reset***
PCICLK	**120**	PI	***PCI Clock***
PAD31-0	**125-128, 2-5, 9, 11-14, 16-18, 28, 29, 31-33, 35-37, 39, 41, 42, 44-46, 48, 49**	PIO	***PCI Address Data***
CBE3-0#	**6, 19, 26, 38**	PIO	***PCI Command Byte Enable***
FRAME#	**20**	PIO	***PCI FRAME# Signal***
DEVSEL#	**23**	PIO	***PCI DEVSEL# Signal***
IRDY#	**21**	PIO	***PCI IRDY# Signal***
TRDY#	**22**	PIO	***PCI TRDY# Signal***
STOP#	**24**	PIO	***PCI STOP# Signal***
PAR	**25**	PIO	***PCI Parity***
IDSEL	**7**	PI	***PCI Initialization Device Select***
INTA#	**121**	PO	***PCI Interrupt A Output***
PCIREQ#	**124**	PO	***PCI Request Output***
PCIGNT#	**123**	PI	***PCI Grant Input***

Table 5-2. Pin Descriptions of IDE Primary Channel Interface

Signal	Pin(s) No.	Attribute	Description
IDE Primary Channel Interface (3.3V CMOS I/F, 5V tolerant)			
PDD15-0	**59, 61, 63, 66, 71, 73, 75, 79, 80, 78, 74, 72, 70, 65, 62, 60**	IOP	***IDE Primary Channel Data Bus***
PA2-0	**52, 55, 54**	OP	***IDE Primary Channel Device Address***
PCS1#	**51**	OP	***IDE Primary Channel Chip Select 1***
PCS0#	**53**	OP	***IDE Primary Channel Chip Select 0***
PIOW#	**67**	OP	***IDE Primary Channel IO Write Strobe***
PIOR#	**76**	OP	***IDE Primary Channel IO Read Strobe***
PDRQ	**58**	I	***IDE Primary Channel DMA Request***
PDACK#	**57**	OP	***IDE Primary Channel DMA Acknowledge***
PIORDY	**69**	I	***IDE Primary Channel IO Channel Ready***
PINT	**56**	I	***IDE Primary Channel Interrupt***
PCBLID#	**113**	I	***IDE Primary Channel Cable Assembly Type Identifier***
PRST#	**50**	OP	***IDE Primary Channel Reset***

Table 5-3. Pin Descriptions of IDE Secondary Channel Interface

Signal	Pin(s) No.	Attribute	Description
IDE Secondary Channel Interface (3.3V CMOS I/F, 5V tolerant)			
SDD15-0	**90, 95, 97, 101, 103, 105, 107, 112, 111, 106, 104, 102, 100, 96, 94, 89**	IOP	***IDE Secondary Channel Data Bus***
SA2-0	**82, 85, 84**	OP	***IDE Secondary Channel Device Address***
SCS1-0#	**81, 83**	OP	***IDE Secondary Channel Chip Select***
SIOW#	**98**	OP	***IDE Secondary Channel IO Write Strobe***
SIOR#	**93**	OP	***IDE Secondary Channel IO Read Strobe***
SDRQ	**88**	I	***IDE Secondary Channel DMA Request***
SDACK#	**87**	OP	***IDE Secondary Channel DMA Acknowledge***
SIORDY	**91**	I	***IDE Secondary Channel IO Channel Ready***
SINT	**86**	I	***IDE Secondary Channel Interrupt***
SCBLID#	**114**	I	***IDE Secondary Channel Cable Assembly Type Identifier***
SRST#	**115**	OP	***IDE Secondary Channel Reset***

Table 5-4. Pin Descriptions of Flash/ROM Interface*

Signal	Pin(s) No.	Attribute	Description
Flash/ROM Interface (3.3V CMOS I/F)			
FWE#	**83**	OP	***Flash/ROM Memory Write Enable*** This signal is multiplex with **SCS0#**.
FOE#	**81**	OP	***Flash/ROM Memory Output Enable*** This signal is multiplex with **SCS1#**.
FCS#	**109**	O8	***Flash/ROM Memory Chip Select*** This signal is multiplex with **PCK66ME**.
FA16-0	**84, 85, 90, 51, 53, 82, 52, 55, 54, 59, 61, 63, 66, 71, 73, 75, 79**	OP	***Flash/ROM Memory Address*** These signals are multiplex with the following signals (from MSB to LSB): **SA0, SA1, SDD15, PCS1#, PCS0#, SA2, PA2, PA1, PA0, PDD15-8**.
FD7-0	**80, 78, 74, 72, 70, 65, 62, 60**	IOP	***Flash/ROM Memory Output Enable*** These signals are multiplex with **PDD7-0**.

*: The above pins are multiplex function pins.

Table 5-5. Pin Descriptions of Miscellaneous Signal

Signal	Pin(s) No.	Attribute	Description
Miscellaneous Signal (3.3V CMOS I/F)			
PCK66ME	**109**	ID	***PCI Clock 66 MHz Input Enable*** This signal indicates the PCI clock frequency is 66 MHz or 33 MHz. The signal is only detected when the **RESET#** signal is changed from low to high. If the signal is high, the PCICLK frequency is 66 MHz; otherwise the frequency is 33 MHz. When the **RESET#** is high, the signal is used as **FCS#**.

Table 5-6. Pin Descriptions of Power/Ground Signals

Signal	Pin(s) No.	Attribute	Description
Power Ground Signals			
VSS	**1, 8, 15, 27, 34, 40, 47, 64, 77, 99, 110, 119**	I	***Ground***
VCC	**10, 30, 43, 68, 92, 108, 116**	I	***Power Supply of 3.3V***
AVSS	**118**	I	***Analog Ground for analog PLL***
AVCC	**117**	I	***Analog VCC for analog PLL***

Notes: IO cell types are described as below:

I: Input PAD.
ID: Input PAD (integrate a 75k-ohm pull-down resistor).
IK: Schmitt Trigger Input PAD.
PI: PCI Bus Specified Input PAD.
O8: 8mA Output PAD.
OP: Programming Output PAD, the output driving can be programmed to be 2~12mA, the default value is 8mA.
PO: PCI Bus Specified Ouput PAD.
PIO: PCI Bus Specified Input/Output PAD.
IOP: Programming Input/Output PAD, the output driving can be programmed to be 2~12mA, the default value is 8mA.

6. Functional Description

6.1 Register Description

6.1.1 Register List

6.1.2 List of PCI Configuration Registers

Table 6-1. List of PCI Configuration Registers

31 16	15 00	Index
Device ID (8212h)	Vendor ID (1283h)	00h-03h
Status (0230h)	Command (0000h)	04h-07h
Base Class Code (01h) / Sub-class code (04h)	Program Interface (00h) / Revision ID (10h)	08h-0Bh
Reserved / Header Type (00h)	Latency Timer (20h) / Cache Line Size (00h)	0Ch-0Fh
Primary Channel Command Block Register Base Address (1F1h)		10h-13h
Primary channel Control Block Register Base Address (3F5h)		14h-17h
Secondary Channel Command Block Register Base Address (171h)		18h-1Bh
Secondary Channel Control Block Register Base Address (375h)		1Ch-1Fh
Bus Master Base Address Register (0001h)		20h-23h
Reserved		24h-2Bh
Sub-system Device ID (0000h)	Sub-system Vendor ID (0000h)	2Ch-2Fh
Expansion ROM Base Address (0000h)		30h-33h
Reserved / Reserved	Reserved / Cap. Pointer (80h)	34h-37h
Reserved		38h-3Bh
MAX_LAT (08h) / MIN_GNT (08h)	INTERRUPT PIN (01h) / INTERRUPT LINE (00h)	3Ch-3Fh
IDE Virtual Channel Exist Register (01h) / IDE Pad Driving Current Register	IDE I/O Configuration Register	40h-43h
Reserved / PCI Burst Threshold (08h)	Reserved / Primary PCI Burst Threshold (08h)	44h-47h
Reserved / Reserved	PLL2 Control (02h) / PLL1 Control (02h)	48h-4Bh
IDE Bus Skew Control Register (40044004h)		4Ch-4Fh
RAID Transfer Sector Count (0000h)	RAID Control (00h) / PCI Mode (01h)	50h-53h
P-CH Device 1 Ultra DMA Timing (31h) / P-CH Device 0 Ultra DMA Timing (31h)	Reserved / P-CH PIO/MDMA Timing (A3h)	54h-57h
S-CH Device 1 Ultra DMA Timing (31h) / S-CH Device 0 Ultra DMA Timing (31h)	Reserved / S-CH PIO/MDMA Timing (A3h)	58h-5Bh
Reserved / CPU Control (00h)	CPU NMI Control (1Ah) / Test Mode (00h)	5Ch-5Fh
Reserved		60h-7Fh

List of PCI Configuration Registers [cont'd]

Power Management Capabilities (PMC) (02h)		Next Item Pointer (0h)	Capability ID (01h)	80h-83h
Data (00h)	PMCSR_BSE Bridge Support Extensions (00h)	Power Management Control/Status Register (PMCSR) (0000h)		84h-87h
Reserved				88h-FFh

6.1.3 List of PCI I/O Registers

Table 6-2. List of PCI I/O Register -- Bus Master IDE I/O Registers

Register Name	R/W	Offset (note)	Default	Register Size
Bus Master IDE Command Register for Primary Channel (BMICRP)	R/W	0x0	00h	8 bits
Bus Master IDE Status Register for Primary Channel (BMISRP)	R/WC	0x2	00h	8 bits
Bus Master Descriptor Table Pointer Register for Primary Channel (BMIDTPRP)	R/W	0x4	00000000h	32 bits
Bus Master IDE Command Register for Secondary Channel (BMICRS)	R/W	0x8	00h	8 bits
Bus Master IDE Status Register for Secondary Channel (BMISRS)	R/WC	0xA	00h	8 bits
Bus Master Descriptor Table Pointer Register for Secondary Channel (BMIDTPRS)	R/W	0xC	00000000h	32 bits

(Note)The Base Address depends on Bus Master Base Address Register (BMBA).

Table 6-3. List of PCI I/O Register From Local CPU View-- Bus Master IDE I/O Registers

Register Name	R/W	Address	Default	Register Size
Bus Master IDE Status Register for Primary Channel (BMISRP)	WO	0x08052h(Note)	00h	8 bits
Bus Master IDE Status Register for Secondary Channel (BMISRS)	WO	0x0805Ah(Note)	00h	8 bits

Note: Only Bit 2 (Interrupt bit) can be set by the local CPU.

Table 6-4. Virtual IDE Interface and Status Registers from PCI I/O View (PCI IO Space Mapping)

Register Name	R/W	Offset	Default	Register Size
Primary IDE Data Register (VPDR)	R/W	0x0 (Note 1)	0000h	16 bits
Primary IDE Error/Feature Register (VPEFR)	R/W	0x1(Note 1)	00h	8 bits
Primary IDE Sector Count (Ext) Register (VPSCR)	R/W	0x2 (Note 1, 5)	00h	8 bits
Primary IDE Sector Number (Ext) Register (VPSNR)	R/W	0x3 (Note 1, 5)	00h	8 bits
Primary IDE Cylinder Low (Ext) Register (VPCLR)	R/W	0x4 (Note 1, 5)	00h	8 bits
Primary IDE Cylinder High (Ext) Register (VPCHR)	R/W	0x5 (Note1, 5)	00h	8 bits
Primary IDE Device/Head Register (VPHDR)	R/W	0x6 (Note1)	00h	8 bits
Primary IDE Command/Status Register (VPCMR)	R/W	0x7 (Note1)	00h	8 bits
Primary IDE Device Control/Alternate Status Register (VPSTUR)	R/W	0x6 (Note2)	--	8 bits
Secondary IDE Data Register (VSDR)	R/W	0x0 (Note3)	0000h	16 bits
Secondary IDE Error/Feature Register (VSEFR)	R/W	0x1 (Note3)	00h	8 bits
Secondary IDE Sector Count (Ext) Register (VSSCR)	R/W	0x2 (Note 3, 5)	00h	8 bits
Secondary IDE Sector Number (Ext) Register (VSSNR)	R/W	0x3 (Note 3, 5)	00h	8 bits
Secondary IDE Cylinder Low (Ext) Register (VSCLR)	R/W	0x4 (Note 3, 5)	00h	8 bits
Secondary IDE Cylinder High (Ext) Register (VSCHR)	R/W	0x5 (Note 3, 5)	00h	8 bits
Secondary IDE Device/Head Register (VSHDR)	R/W	0x6 (Note 3)	00h	8 bits
Secondary IDE Command /Status Register (VSCMR)	R/W	0x7 (Note 3)	00h	8 bits
Secondary IDE Device Control/Alternate Status Register (VSSTUR)	R/W	0x6 (Note4)	--	8 bits

Definition of R/W Attributes:

RO **READ ONLY**. If a register is read only, writing will have no effect.

R/W **READ/WRITE**. A register with this attribute can be read and written.

R/WC READ/WRITE CLEAR. A register bit with this attribute can be read and written. However, a write of 1 clears the corresponding bit and a write of 0 will have no effect.

Notes:

1. The base address of the Primary IDE Command Registers is defined in PCI Configuration Register 10h~13h (Primary Channel Command Block Register)
2. The base address of the Primary IDE Control Register is defined in PCI Configuration Register 14h~17h (Primary Channel Control Block Register).
3. The base address of the Secondary IDE Command Register is defined in PCI Configuration Register 18h~1Bh (Secondary Channel Command Block Register).
4. The base address of the Secondary IDE Control Register is defined in PCI Configuration Register 1Ch~1Fh (Secondary Channel Control Block Register).
5. When the Primary/Secondary Device Control register bit 7 is set to 1, these registers are regarded as Extended registers, which are used for 48-bit address feature set.

6.1.4 List of Local CPU Access Registers

Table 6-5. Virtual IDE Interface and Status Registers from Local CPU View (CPU memory address mapping)

Register Name	R/W	Address	Default	Register Size
Primary IDE Data Register (PDR)	R/W	0x08000	0000h	16 bits
Primary IDE Error Register (PEFR)	R/W	0x08001	00h	8 bits
Primary IDE Sector Count Register (PSCR)	R/W	0x08002	00h	8 bits
Primary IDE Sector Number Register (PSNR)	R/W	0x08003	00h	8 bits
Primary IDE Cylinder Low Register (PCLR)	R/W	0x08004	00h	8 bits
Primary IDE Cylinder High Register (PCHR)	R/W	0x08005	00h	8 bits
Primary IDE Device/Head Register (PHDR)	R/W	0x08006	00h	8 bits
Primary IDE Status Register (PSTAR)	R/W	0x08007	00h	8 bits
Primary IDE Sector Counter Ext. Register (PSCEXR)	R/W	0x0800A	00h	8 bits
Primary IDE Sector Number Ext. Register (PSNEXR)	R/W	0x0800B	00h	8 bits
Primary IDE Cylinder Low Ext. Register (PCLEXR)	R/W	0x0800C	00h	8 bits
Primary IDE Cylinder High Ext. Register (PCHEXR)	R/W	0x0800D	00h	8 bits
Primary Feature Register (PFEAR)	R/W	0x0800E	00h	8 bits
Primary Command Register (PCMR)	R/W	0x0800F	00h	8 bits
Primary IDE Alternate Status Register (PSTUR)	R/W	0x08016	--	8 bits
Primary IDE Device Control Status Register (PDCR)	R/W	0x0801A	00h	8 bits
Secondary IDE Data Register (SDR)	R/W	0x08020	0000h	16 bits
Secondary IDE Error/Feature Register (SEFR)	R/W	0x08021	00h	8 bits
Secondary IDE Sector Count Register (SSCR)	R/W	0x08022	00h	8 bits
Secondary IDE Sector Number Register (SSNR)	R/W	0x08023	00h	8 bits
Secondary IDE Cylinder Low Register (SCLR)	R/W	0x08024	00h	8 bits
Secondary IDE Cylinder High Register (SCHR)	R/W	0x08025	00h	8 bits
Secondary IDE Device/Head Register (SHDR)	R/W	0x08026	00h	8 bits
Secondary IDE Status Register (SCMR)	R/W	0x08027	00h	8 bits
Secondary IDE Sector Counter Ext. Register (SSCEXR)	R/W	0x0802A	00h	8 bits
Secondary IDE Sector Number Ext. Register (SSNEXR)	R/W	0x0802B	00h	8 bits
Secondary IDE Cylinder Low Ext. Register (SCLEXR)	R/W	0x0802C	00h	8 bits

Table 6-5. Virtual IDE Interface and Status Registers from Local CPU View (CPU memory address mapping) [Cont'd]

Register Name	R/W	Address	Default	Register Size
Secondary IDE Cylinder High Ext. Register (SCHEXR)	R/W	0x0802D	00h	8 bits
Secondary Feature Register (SFEAR)	R/W	0x0802E	00h	8 bits
Secondary Command Register (SCMR)	R/W	0x0802F	00h	8 bits
Secondary IDE Alternate Status Register (SSTUR)	R/W	0x08036	--	8 bits
Secondary IDE Device Control Register (SDVR)	R/W	0x0803A	00h	8 bits

Note: The registers of Table 6-4 and Table 6-5 are the same. They just have different address mapping between the CPU and PCI access.

Table 6-6. List of IDE Control Registers for Local CPU

Register Name	R/W	Address	Default	Register Size
Primary IDE Transfer Counter Register (PIDETCR)	R/W	0x08100	0000h	16 bits
Primary IDE Operation Register (PIDEOPR)	R/W	0x08102	00h	8 bits
Primary IDE PIO and DMA Timing Register (PPIOTMR)	R/W	0x08103	00h	8 bits
Primary IDE Ultra DMA Timing Register (PUDMATMR)	R/W	0x08104	00h	8 bits
Primary FIFO Access Control Register (PFIFOCR)	R/W	0x08105	00h	8 bits
Primary FIFO Status Register (PFIFOSR)	RO	0x08106	80h	8 bits
Primary FIFO Low Word Access Register (PFIFOLR)	R/W	0x08108	0000h	16 bits
Primary FIFO High Word Access Register (PFIFOHR)	R/W	0x0810A	0000h	16 bits
Secondary IDE Transfer Counter Register (SIDETCR)	R/W	0x08110	0000h	16 bits
Secondary IDE Operation Register (SIDEOPR)	R/W	0x08112	00h	8 bits
Secondary IDE PIO and DMA Timing Register (SPIOTMR)	R/W	0x08113	00h	8 bits
Secondary IDE Ultra DMA Timing Register (PUDMATMR)	R/W	0x08114	00h	8 bits
Secondary FIFO Access Control Register (SFIFOCR)	R/W	0x08115	00h	8 bits
Secondary Status Control Register (SFIFOSR)	RO	0x08116	80h	8 bits
Secondary FIFO Low Word Access Register (SFIFOLR)	R/W	0x08118	0000h	16 bits

Table 6-6. List of IDE Control Registers for Local CPU[cont'd]

Register Name	R/W	Address	Default	Register Size
Secondary FIFO High Word Access Register (SFIFOHR)	R/W	0x0811A	0000h	16 bits
Primary IDE Data Register (PDR)	R/W	0x08120	0000h	16 bits
Primary IDE Error/Feature Register (PEFR)	R/W	0x08121	00h	8 bits
Primary IDE Sector Count Register (PSCR)	R/W	0x08122	00h	8 bits
Primary IDE Sector Number Register (PSNR)	R/W	0x08123	00h	8 bits
Primary IDE Cylinder Low Register (PCLR)	R/W	0x08124	00h	8 bits
Primary IDE Cylinder High Register (PCHR)	R/W	0x08125	00h	8 bits
Primary IDE Device/Head Register (PHDR)	R/W	0x08126	00h	8 bits
Primary IDE Command Register (PCMR)	R/W	0x08127	00h	8 bits
Primary IDE Alternate Status Register (PSTUR)	R/W	0x08136	--	8 bits
Secondary IDE Data Register (SDR)	R/W	0x08140	0000h	16 bits
Secondary IDE Error/Feature Register (SEFR)	R/W	0x08141	00h	8 bits
Secondary IDE Sector Count Register (SSCR)	R/W	0x08142	00h	8 bits
Secondary IDE Sector Number Register (SSNR)	R/W	0x08143	00h	8 bits
Secondary IDE Cylinder Low Register (SCLR)	R/W	0x08144	00h	8 bits
Secondary IDE Cylinder High Register (SCHR)	R/W	0x08145	00h	8 bits
Secondary IDE Device/Head Register (SHDR)	R/W	0x08146	00h	8 bits
Secondary IDE Command Register (SCMR)	R/W	0x08147	00h	8 bits
Secondary IDE Alternate Status Register (SSTUR)	R/W	0x08156	--	8 bits
Primary Channel Transfer Count Register (PTCR)	R/W	0x08200	0000h	16 bits
Primary Channel Operation Register (POPR)	R/W	0x08202	0000h	16 bits
Secondary Channel Transfer Count Register (STCR)	R/W	0x08208	0000h	16 bits
Secondary Channel Operation Register (SOPR)	R/W	0x0820A	0000h	16 bits
Rebuild Block Counter Register (RBCR)	R/W	0x08210	0000h	16 bits
Rebuild Operation Register (RBOPR)	R/W	0x08212	00h	8 bits
Interrupt Pending Register (INTPR)	R/W	0x08218	0000h	16 bits
Interrupt Mask Register (INTMSR)	R/W	0x0821A	FFF8h	16 bits
End of Interrupt Register (EOIR)	R/W	0x0821C	00h	8 bits
Timer 0 Control Register (T0CTLR)	R/W	0x08230	00h	8 bits
Timer 0 Count Register (T0CNTR)	RO	0x08232	0000h	16 bits
Timer 0 Max. Count Register (T0MAXR)	R/W	0x08234	FFFFh	16 bits
Timer 1 Control Register (T1CTLR)	R/W	0x08238	00h	8 bits
Timer 1 Count Register (T1CNTR)	RO	0x0823A	0000h	16 bits

Table 6-6. List of IDE Control Registers for Local CPU [cont'd]

Name	R/W	Address	Default	Register Size
Timer 1 Max. Count Register (T1MAXR)	R/W	0x0823C	FFFFh	16 bits
IDE Clock Frequency Register (IDECLKR)	R/W	0x08252	00h	8 bits
GPIO Register (GPIOR)	R/W	0x08254	00h	8 bits

6.1.5 List of UART Registers

Table 6-7. List of UART Registers

Register Name	R/W	Address	Default	Register Size
UART Receiver Buffer Register (URBR)	RO	0x09000 DLAB=0*Note1	-	8 bits
UART Transmitter Buffer Register (UTBR)	WO	0x09000 DLAB=0*Note1	-	8 bits
UART Interrupt Enable Register (UIER)	R/W	0x09002 DLAB=0*Note1	00h	8 bits
UART Interrupt Identification Register (UIIR)	RO	0x09004	01h	8 bits
UART FIFO Control Register (UFCR)	WO	0x09004	00h	8 bits
UART Line Control Register (ULCR)	R/W	0x09006	00h	8 bits
UART Line Status Register (ULSR)	R/W	0x0900A	60h	8 bits
UART Divisor Latch LSB Register (UDLL)	R/W	0x09000(Note 1)	00h	8 bits
UART Divisor Latch MSB Register (UDLM)	R/W	0x09002(Note1)	00h	8 bits

Definition of R/W Attributes:

RO **READ ONLY**. If a register is read only, writing will have no effect.
R/W **READ/WRITE**. A register with this attribute can be read and written.
WO **WRITE ONLY**. If a register is written only, the data written to this register cannot be read from this register.

Note: The registers are valuable when bit 7 (DLAB) of the UART Line Control Register is 1.

6.1.6 PCI Configuration Registers Definition

6.1.6.1 Vendor ID Register (VIDR) — Offset 0x0

Bit	R/W	Default	Description
15-0	RO	1283h	**Vendor ID (VID)** This is a 16-bit value assigned to the ITE IDE RAID Controller function.

6.1.6.2 Device ID Register (DIDR) — Offset 0x2

Bit	R/W	Default	Description
15-0	RO	8212h	**Device ID (DID)** This is a 16-bit value assigned to the ITE IDE RAID Controller function.

6.1.6.3 Command Register (CMDR) — Offset 0x4

Bit	R/W	Default	Description
15-7	-	0h	**Reserved**
6	RO	0h	**Parity Error Response (PER)** 1: Enabled 0: Disabled
5-3	-	0h	**Reserved**
2	R/W	0h	**DMA Bus Master Enable (DBME)** 1: Enabled 0: Disabled
1	R/W	0h	**Memory Access Enable** 1: Allow the chip to respond to I/O space accesses. 0: Disable I/O space accesses.
0	R/W	0h	**I/O Access Enable (IOAE)** 1: Allow the chip to respond to I/O space accesses. 0: Disable I/O space accesses.

6.1.6.4 Device Status Register (DSTR) — Offset 0x6

Bit	R/W	Default	Description
15-14	-	0h	**Reserved**
13	R/WC	0h	**Master Abort Status (MAST)** This bit is set to high when the IDE RAID Controller acts as a PCI master and has issued a Master-Abort. Write 1 to clear this bit.
12	R/WC	0h	**Received Target Abort (RTA)** This bit is set to high when the IDE RAID controller is a PCI master and the PCI transaction is terminated by receiving a Target-Abort. Write 1 to clear this bit.
11	R/WC	0h	**Signal Target Abort (STA)** This bit is set to high when the IDE RAID controller is a PCI target and has terminated the PCI transaction with a Target-Abort. Writing 1 to this bit to clear it.
10-9	RO	1h	**DEVSEL Timing (DEVT[1:0])** Medium timing is selected for DEVSEL# assertion when the PCI target performs the positive decode.
8	-	0h	**Reserved**
7	RO	0h	**Fast Back-to-Back Capable (FBC)** Always read as 0. Not supported
6	-	0h	**Reserved**
5	RO	1h	**66 MHz Capable** A “1” indicates that the function supports 66 MHz. A “0” indicates that the function just supports 33 MHz.
4	RO	1h	**Capabilities** This bit indicates whether this function implements a list of extended capabilities such as the PCI power management. When set, it indicates the presence of capabilities. The value of “0” means that this function does not implement capabilities.
3-0	-	0h	**Reserved**

6.1.6.5 Revision Register (RID) — Offset 0x8

Bit	R/W	Default	Description
7-0	RO	10h	**Revision ID (RID)** The revision number of the IDE RAID controller.

6.1.6.6 Program Interface (PIR) — Offset 0x9

Bit	R/W	Default	Description
7-0	RO	00h	**Program Interface (PI)** 00h for RAID Controller

6.1.6.7 Sub-class Code Register (SCC) — Offset 0xA

Bit	R/W	Default	Description
7-0	RO	04h	**Sub-class Code (SCC)** 04h for IDE RAID Controller.

6.1.6.8 Base Class Code Register (BCC) — Offset 0xB

Bit	R/W	Default	Description
7-0	RO	01h	**Base Class Code (SCC)** 01h for Mass storage device.

6.1.6.9 Cache Line Size Register (CLS) — Offset 0xC

Bit	R/W	Default	Description
7-0	RO	0h	**Cache Line Size (CLS)**

6.1.6.10 Master Latency Timer Register (MLT) — Offset 0xD

Bit	R/W	Default	Description
7-3	R/W	4h	**Master Latency Timer (MLT)** Indicates the PCI Bus master latency timer.
2-0	RO	000b	**Reserved**

6.1.6.11 Header Type Register (HTYPE) — Offset 0xE

Bit	R/W	Default	Description
7-0	RO	00h	**Head Type (HEADT)** Indicates the header type of the device.

6.1.6.12 Built-in Self Test Register (BISTR) — Offset 0xF

Bit	R/W	Default	Description
7	RO	0b	**Built-in Self-Test Capable (BC)** BIST is not supported.
6	RO	0b	**Built-in Self-Test Start (BS)** BIST start bit.
5-4	RO	00b	Reserved
3-0	RO	0h	**BIST Completion Code** Reserved

6.1.6.13 Primary Channel Command Block Register Base Address (PCMDBA) — Offset 0x10

Bit	R/W	Default	Description
31-3	R/W	3Eh	**Primary Channel Command Block Base Address (PCMDBA[28:0])** The base address of the command block register of the primary channel.
2-1	RO	00	**Reserved**
0	RO	1	**Resource Type (RT)** Hardwired to 1 to indicate that the base address field in this register has been mapped to the I/O space

This register is only used in the “Native-PCI” mode. The default value is 1F1h.

6.1.6.14 Primary Channel Control Block Base Address (PCNTBA) — Offset 0x14

Bit	R/W	Default	Description
31-2	R/W	FDh	**Primary Channel Control Block Base Address (PCNTLBA [29:0])** The base address of the control block register of the primary channel.
1	RO	0h	**Reserved**
0	RO	1	**Resource Type (RT)** Hardwired to 1 to indicate that the base address field in this register has been mapped to the I/O space.

This register is only used in the “Native-PCI” mode. The default value is 3F5h.

6.1.6.15 Secondary Channel Command Block Base Address (SCMDBA) — Offset 0x18

Bit	R/W	Default	Description
31-3	R/W	2Eh	**Secondary Channel Command Block Base Address (SCMDBA[28:0])** The base address of the command block register of the secondary channel.
2-1	RO	00	**Reserved**
0	RO	1	**Resource Type (RT)** Hardwired to 1 to indicate that the base address field in this register has been mapped to the I/O space.

This register is only used in the “Native-PCI” mode. The default value is 171h.

6.1.6.16 Secondary Channel Control Block Base Address (SCNTBA) — Offset 0x1C

Bit	R/W	Default	Description
31-2	R/W	DDh	**Secondary Channel Control Block Base Address (SCNTLBA[29:0])** The base address of the control block register of the secondary channel.
1	RO	0h	**Reserved**
0	RO	1	**Resource Type (RT)** Hardwired to 1 to indicate that the base address field in this register has been mapped to the I/O space.

This register is only used in the “Native-PCI” mode. The default value is 375h.

6.1.6.17 Bus Master Base Address Register (BMBA) — Offset 0x20

Bit	R/W	Default	Description
31-4	R/W	00h	**Bus Master Base Address (BMBA [27:0])** These bits provide the base address for the bus master interface register.
3-1	RO	000	**Reserved**
0	RO	1	**Resource Type (RT)** Hardwired to 1 to indicate that the base address field in this register has been mapped to the I/O space.

6.1.6.18 Sub-system Vendor ID Register (SVID) — Offset 0x2C

Bit	R/W	Default	Description
15-0	R/W	0h	**Sub-system Vendor ID (SVID [15:0]).**

6.1.6.19 Sub-system Device ID Register (SID) — Offset 0x2E

Bit	R/W	Default	Description
15-0	R/W	0h	**Sub-system Device ID (SVID [15:0]).**

6.1.6.20 Expansion ROM Base Address Register (ROMBAR) — Offset 0x30

Bit	R/W	Default	Description
31-17	R/W	0h	**Expansion ROM Base Address**
16-1	RO	0h	**Reserved** Read always as 0
0	R/W	0h	**ROM Address Decode Enable** 1: ROM address enables to decode. 0: ROM address disables to decode.

6.1.6.21 Capabilities Pointer Register (CPR) — Offset 0x34

Bit	R/W	Default	Description
7-0	RO	80h	**Capabilities Pointer (Cap_ptr)** The Cap_ptr provides an offset into the function’s PCI Configuration Space for the location of the first item in the Capabilities linked list. The Cap_ptr offset is Dword aligned so the two least significant bits are always “0”.

6.1.6.22 Interrupt Line Register (ILR) — Offset 0x3C

Bit	R/W	Default	Description
7-0	R/W	00h	**Interrupt Line (IL)** This is an 8-bit register used to communicate the interrupt line routing information. The value in the register tells which input of the system interrupt controller the device's interrupt pin is connected to.

6.1.6.23 Interrupt Pin Register (IPR) — Offset 0x3D

Bit	R/W	Default	Description
7-0	RO	01h	**Interrupt Pin (IP)** The register tells which interrupt pin the device uses. The device only uses the INTA#, so the value is 01h.

6.1.6.24 MIN_GNT Register (MGR) — Offset 0x3E

Bit	R/W	Default	Description
7-0	RO	08h	**MIN_GNT (MG)** The device has requirements for the setting of Latency Timers.

6.1.6.25 MAX_LAT Register (MLR) — Offset 0x3F

Bit	R/W	Default	Description
7-0	RO	08h	**MAX_LAT (ML)** The device has requirements for the setting of Latency Timers.

6.1.6.26 IDE I/O Configuration Register (IOCFG) — Offset 0x40

Bit	R/W	Default	Description
15	R/W	0h	**IDE Decode Enable for Primary Channel (PDE)** 1: Enabled. 0: Disabled.
14	RO	0b	**Reserved**
13	R/W	0h	**IDE Decode Enable for Secondary Channel (SDE)** 1: Enabled. 0: Disabled.
12-8	RO	00h	**Reserved**
7	R/W	0h	**Secondary Drive 1 Channel Cable Report (S1CR)** This bit is written by software. 1: 80 conductor cables are present. 0: 40 conductor cables are present.
6	R/W	0h	**Secondary Drive 0 Channel Cable Report (S0CR)** This bit is written by software. 1: 80 conductor cables are present. 0: 40 conductor cables are present.
5	R/W	0h	**Primary Drive 1 Channel Cable Report (P1CR)** This bit is written by software. 1: 80 conductor cables are present. 0: 40 conductor cables are present.
4	R/W	0h	**Primary drive 0 Channel Cable Report (P0CR)** This bit is written by software. 1: 80 conductor cables are present. 0: 40 conductor cables are present.
3	RO	-	**Secondary Channel SCBLID# Signal (SCCS)** CBLID# signal in the cable of the secondary channel.
2	RO	-	**Primary Channel PCBLID# Signal (PCCS)** PCBLID# signal in the cable of the primary channel.
1	R/W	0b	**Secondary Channel IORDY Sample Enable** 1 : Enable IORDY sample 0 : Disable IORDY sample
0	R/W	0b	**Primary Channel IORDY Sample Enable** 1 : Enable IORDY sample 0 : Disable IORDY sample

6.1.6.27 IDE Driving Current Register (DCR) — Offset 0x42

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5-3	R/W	3h	**Secondary Channel PAD Current Control (SPC)** When SPC[2:0]=000b, the driving current is 2 mA. When SPC[2:0]=001b, the driving current is 4 mA. When SPC[2:0]=010b, the driving current is 6 mA. When SPC[2:0]=011b, the driving current is 8 mA, When SPC[2:0]=100b, the driving current is 6 mA for SDD15-0; 2 mA for others. When SPC[2:0]=101b, the driving current is 8 mA for SDD15-0; 4 mA for others. When SPC[2:0]=110b, the driving current is 10 mA for SDD15-0; 6 mA for others. When SPC[2:0]=111b, the driving current is 12 mA for SDD15-0; 8 mA for others.
2-0	R/W	3h	**Primary Channel PAD Current Control (PPC)** When PPC[2:0]=000b, the driving current is 2 mA. When PPC[2:0]=001b, the driving current is 4 mA. When PPC[2:0]=010b, the driving current is 6 mA. When PPC[2:0]=011b, the driving current is 8 mA, When PPC[2:0]=100b, the driving current is 6 mA for SDD15-0; 2 mA for others. When PPC[2:0]=101b, the driving current is 8 mA for SDD15-0; 4 mA for others. When PPC[2:0]=110b, the driving current is 10 mA for SDD15-0; 6 mA for others. When PPC[2:0]=111b, the driving current is 12 mA for SDD15-0; 8 mA for others.

6.1.6.28 IDE Virtual Channel Exist Register (IDEENR) — Offset 0x43

Bit	R/W	Default	Description
7-4	RO	0h	**Reserved**
3	R/W	0b	**IDE Virtual Secondary Slave Exist** 0: Not Exist 1: Exist
2	R/W	0b	**IDE Virtual Secondary Master Exist** 0: Not Exist 1: Exist
1	R/W	0b	**IDE Virtual Primary Slave Exist** 0: Not Exist 1: Exist
0	R/W	1b	**IDE Virtual Primary Master Exist** 0: Not Exist 1: Exist Note: In order to make IDE Vender Specific Command access successfully, this bit must be set to 1 even though this device is not existed. After the vender command is finished, this bit must be cleared to 0 if the device is not existed.

6.1.6.29 PCI Burst Threshold Register (PCIBRSTR) — Offset 0x44

Bit	R/W	Default	Description
31-24	-	0h	**Reserved**
23-16	R/W	08h	**PCI Burst Threshold for Secondary Channel (SPCIBTHR)** This register decides the data size (Double Word Unit) must be satisfied before the PCI master can perform the burst cycle.
15-8	-	0h	**Reserved**
7-0	R/W	08h	**PCI Burst Threshold for Primary Channel (PPCIBTHR)** See bits 23-16.

6.1.6.30 PLL1 Control Register (PLL1CR) — Offset 0x48

Bit	R/W	Default	Description
7-2	RO	00h	**Reserved**
1	R/W	1b	**PLL1 Power Down (PLL1PD)** This bit is used to power down the PLL1 (66MHz). When this bit is set, the PLL operates normally. When this bit is cleared, the PLL is in the power down state.
0	R/W	0b	**PLL1 Bypass Enable (PLL1BE)** This bit is used to bypass the clock of the PLL1. When this bit is set, the PLL is bypassed. When this bit is cleared, the PLL is in the normal mode.

6.1.6.31 PLL2 Control Register (PLL2CR) — Offset 0x49

Bit	R/W	Default	Description
7-2	RO	00h	**Reserved**
1	R/W	1b	**PLL2 Power Down (PLL2PD)** This bit is used to power down the PLL2 (50MHz). When this bit is set, the PLL operates normally. When this bit is cleared, the PLL is in the power down state.
0	R/W	0b	**PLL2 Bypass Enable (PLL2BE)** This bit is used to bypass the clock of the PLL2. When this bit is set, the PLL is bypassed. When this bit is clear, the PLL is in the normal mode.

6.1.6.32 IDE Bus Skew Control Register (IDEBSCR) — Offset 0x4C

Bit	R/W	Default	Description
31-28	R/W	4h	**Secondary Channel Device Data Input Delay (PDDID)** These bits are used to control the DD input signal delay time.
27-24	R/W	0h	**Secondary Channel Device Strobe Delay (PDSBD)** These bits are used to control the DSTROBE (DIORDY) input signal delay time.
23-20	R/W	0h	**Secondary Channel Host Data Out Delay (PHDOD)** These bits are used to control the DD output signal delay time.
19-16	R/W	4h	**Secondary Channel Host Strobe Delay (PHSBD)** These bits are used to control the HSTROBE (DIOR) signal delay time.
15-12	R/W	4h	**Primary Channel Device Data Input Delay (PDDID)** These bits are used to control the DD input signal delay time.
11-8	R/W	0h	**Primary Channel Device Strobe Delay (PDSBD)** These bits are used to control the DSTROBE (DIORDY) input signal delay time.
7-4	R/W	0h	**Primary Channel Host Data Out Delay (PHDOD)** These bits are used to control the DD output signal delay time.
3-0	R/W	4h	**Primary Channel Host Strobe Delay (PHSBD)** These bits are used to control the HSTROBE (DIOR) signal delay time.

6.1.6.33 PCI Mode Control Register (PCICR) — Offset 0x50

Bit	R/W	Default	Description
7	R/W	0b	**PCI Mode Reset (PCIMR)** This bit is used to reset the related PCI circuit when IT8212F enters the PCI transparent mode. When it is set, the related PCI circuit will be reset. When it is cleared, the related PCI circuit will be in the normal mode.
6	R/W	0b	**Secondary Channel Device 1 Transfer Mode (SCHD1TM)** This bit is used to determine the transfer mode of IDE Bus. 1 : MultiWord DMA mode 0 : Ultra DMA mode
5	R/W	0b	**Secondary Channel Device 0 Transfer Mode (SCHD0TM)** This bit is used to determine the transfer mode of IDE Bus. 1 : MultiWord DMA mode 0 : Ultra DMA mode
4	R/W	0b	**Primary Channel Device 1 Transfer Mode (PCHD1TM)** This bit is used to determine the transfer mode of IDE Bus. 1 : MultiWord DMA mode 0 : Ultra DMA mode
3	R/W	0b	**Primary Channel Device 0 Transfer Mode (PCHD0TM)** This bit is used to determine the transfer mode of IDE Bus. 1 : MultiWord DMA mode 0 : Ultra DMA mode
2	R/W	0b	**Secondary Channel IDE Clock Frequency Select (SCHCLK)** This bit is used to select the IDE Clock Frequency. 1 : 50 MHz, 0 : 66 MHz

PCI Mode Control Register (PCICR) — Offset 0x50[cont'd]

Bit	R/W	Default	Description
1	R/W	0b	**Primary Channel IDE Clock Frequency Select (PCHCLK)** This bit is used to select the IDE Clock Frequency. 1 : 50 MHz, 0 : 66 MHz
0	R/W	1b	**PCI Mode Select (PCIMS)** This bit is used to select the PCI Transparent mode or CPU firmware mode. 1 : CPU firmware mode, 0 : PCI Transparent mode

6.1.6.34 RAID Function Control Registers (RAIDCR) — Offset 0x51

Bit	R/W	Default	Description
7	R/W	0b	**Rebuild Stop (RSTOP)** When the reconstruction is in the process, i.e. RBDS bit is 1. If this bit is set, the reconstruction process will be stopped. This bit is cleared by hardware itself.
6	RO	0b	**Reserved**
5	R/W	0b	**Rebuild Direction (RBDDT)** 1 : Secondary channel read and Primary channel write 0 : Primary channel read and Secondary channel write
4	R/W	0b	**Rebuild Start (RBDS)** When this bit is set, the reconstruction process will begin based on its direction (RBDDT). This bit is cleared by hardware when the reconstruction process is done.
3-1	RO	0h	**Reserved**
0	R/W	0b	**RAID 1 Enable (RAID1EN)** When this bit is set, the RAID 1 Function is enabled. Transfer data will be duplicated on both primary and secondary channels. This bit is cleared by hardware when the transfer is finished.

6.1.6.35 RAID Transfer Sector Count Register (RAIDTSCR) — Offset 0x52

Bit	R/W	Default	Description
15-0	R/W	0h	**Transfer Sector Count** This register is a sector count that can calculate how many sectors will be transferred in the reconstruction and RAID 1 function. The transfer sector count must be the same as the sector count of the IDE Command.

6.1.6.36 PCI Mode Primary PIO and DMA Timing Registers (PMPIOTR) — Offset 0x54

Bit	R/W	Default	Description
7-4	R/W	Ah	**IDE PIO and DMA Transfer Active Time** These bits define T2 or Td timing. The unit is two clock periods of the selected clock.
3-0	R/W	3h	**IDE PIO and DMA Transfer Recovery Time** These bits define the T2I or Tk timing. The unit is two clock periods of the selected clock.

Note: See more details in IDE PIO and DMA Timing Registers.

6.1.6.37 PCI Mode Primary Device 0 Ultra DMA Timing Registers (PMPD0UDTR) — Offset 0x56

Bit	R/W	Default	Description
7	R/W	0b	**Ultra DMA Mode 5, 6 Select** This bit defines the mode of Ultra DMA Mode. When this bit is set, the Ultra DMA Mode is mode 5 or 6. When this bit is cleared, the Ultra DMA Mode is mode 0,1,2,3 or 4.
6-4	R/W	3h	**Ultra DMA Data Setup Time** These bits define the Ultra DMA Tdvs timing. The unit is one clock period of the selected clock frequency for mode 0,1,2,3,4. The unit is half a clock period of the selected clock frequency for mode 5, 6.
3	R/W	0b	**Reserved**
2-0	R/W	1h	**Ultra DMA Data Hold Time** These bits define the Ultra DMA Tdvh timing. The unit is one clock period of the selected clock frequency for mode 0,1,2,3,4. The unit is half a clock period of the selected clock frequency for mode 5, 6.

Note: See more details in IDE Ultra DMA Timing Registers.

6.1.6.38 PCI Mode Primary Device 1 Ultra DMA Timing Registers (PMPD1UDTR) — Offset 0x57

Bit	R/W	Default	Description
7	R/W	0b	**Ultra DMA Mode 5, 6 Select** This bit defines the mode of Ultra DMA Mode. When this bit is set, the Ultra DMA Mode is mode 5 or 6. When this bit is cleared, the Ultra DMA Mode is mode 0,1,2,3 or 4.
6-4	R/W	3h	**Ultra DMA Data Setup Time** These bits define the Ultra DMA Tdvs timing. The unit is one clock period of the selected clock frequency for mode 0,1,2,3,4. The unit is half a clock period of the selected clock frequency for mode 5, 6.
3	R/W	0b	**Reserved**
2-0	R/W	1h	**Ultra DMA Data Hold Time** These bits define the Ultra DMA Tdvh timing. The unit is one clock period of the selected clock frequency for mode 0,1,2,3,4. The unit is half a clock period of the selected clock frequency for mode 5, 6.

Note: See more details in IDE Ultra DMA Timing Registers.

6.1.6.39 PCI Mode Secondary PIO and DMA Timing Registers (PMSPIOTR) — Offset 0x58

Bit	R/W	Default	Description
7-4	R/W	Ah	**IDE PIO and DMA Transfer Active Time** These bits define the T2 or Td timing. The unit is two clock periods of the selected clock.
3-0	R/W	3h	**IDE PIO and DMA Transfer Recovery Time** These bits define the T2I or Tk timing. The unit is two clock periods of the selected clock.

Note: See more details in IDE PIO and DMA Timing Registers

6.1.6.40 PCI Mode Secondary Device 0 Ultra DMA Timing Registers (PMSD0UDTR) — Offset 0x5A

Bit	R/W	Default	Description
7	R/W	0b	**Ultra DMA Mode 5, 6 Select** This bit defines the mode of Ultra DMA Mode. When this bit is set, the Ultra DMA Mode is mode 5 or 6. When this bit is cleared, the Ultra DMA Mode is mode 0,1,2,3 or 4.
6-4	R/W	3h	**Ultra DMA Data Setup Time** These bits define the Ultra DMA Tdvs timing. The unit is one clock period of the selected clock frequency for mode 0,1,2,3,4. The unit is half a clock period of the selected clock frequency for mode 5, 6.
3	R/W	0b	**Reserved**
2-0	R/W	1h	**Ultra DMA Data Hold Time** These bits define the Ultra DMA Tdvh timing. The unit is one clock period of the selected clock frequency for mode 0,1,2,3,4. The unit is half a clock period of the selected clock frequency for mode 5, 6.

Note: See more details in IDE Ultra DMA Timing Registers.

6.1.6.41 PCI Mode Secondary Device 1 Ultra DMA Timing Registers (PMSD1UDTR) — Offset 0x5B

Bit	R/W	Default	Description
7	R/W	0b	**Ultra DMA Mode 5, 6 Select** This bit defines the mode of Ultra DMA Mode. When this bit is set, the Ultra DMA Mode is mode 5 or 6. When this bit is cleared, the Ultra DMA Mode is mode 0,1,2,3 or 4.
6-4	R/W	3h	**Ultra DMA Data Setup Time** These bits define the Ultra DMA Tdvs timing. The unit is one clock period of the selected clock frequency for mode 0,1,2,3,4. The unit is half a clock period of the selected clock frequency for mode 5, 6.
3	R/W	0b	**Reserved**
2-0	R/W	1h	**Ultra DMA Data Hold Time** These bits define the Ultra DMA Tdvh timing. The unit is one clock period of the selected clock frequency for mode 0,1,2,3,4. The unit is half a clock period of the selected clock frequency for mode 5, 6.

Note: See more details in IDE Ultra DMA Timing Registers.

6.1.6.42 Test Mode Register (TMR) — Offset 0x5C

Bit	R/W	Default	Description
7-2	RO	0h	**Reserved**
1	R/W	0b	**PLL Output Test** When the bit is enabled, PRST# : 66 MHz, SRST# : 50 MHz
0	R/W	0b	**CPU Bus Watcher Enable** When the bit is enabled, the Internal CPU bus will output.

6.1.6.43 CPU NMI Control Register (CNMIR) — Offset 0x5D

Bit	R/W	Default	Description
7-0	R/W	1Ah	**NMI Delay ALE Number** These bits are used to control the delay to assert NMI to the local CPU

6.1.6.44 CPU Control Register (CCR) — Offset 0x5E

Bit	R/W	Default	Description
7-2	RO	0h	**Reserved**
1	R/W	0b	**BIOS ROM Ready** When this bit is set, the local CPU can do the IDE bus access.
0	R/W	0b	**CPU Software Reset** When this bit is set, the Internal CPU will be reset

6.1.6.45 Capability Identifier Register (CAPIDR) — Offset 0x80

Bit	R/W	Default	Description
7-0	RO	01h	**Capability Identifier (CAP_ID)** When this register is set to 01h, it identifies the linked capability list as the PCI Power Management Capability.

6.1.6.46 Next Item Pointer Register (NEXT_PTR) — Offset 0x81

Bit	R/W	Default	Description
7-0	RO	00h	**Next Item Pointer** This field provides an offset into the function's PCI Configuration Space pointing to the location of the next item on the function's Capability list. If there are no additional items on the Capability list, the register is set to 00h.

6.1.6.47 Power Management Capabilities Register (PMCR) — Offset 0x82

Bit	R/W	Default	Description
15-11	RO	0h	**PME_Support** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for every bit indicates that the function is not capable of asserting the PME# signal in the power state. bit(11) xxxx1b – PME# can be asserted from **D0.** bit(12) xxx1xb – PME# can be asserted from **D1.** bit(13) xx1xxb – PME# can be asserted from **D2.** bit(14) x1xxxb – PME# can be asserted from **$D3_{hot}$.** bit(15) 1xxxxb – PME# can be asserted from **$D3_{cold}$.**
10	RO	0h	**D2_Support** If this bit is a "1", this function supports the **D2** Power Management State. Not support
9	RO	0h	**D1_Support** If this bit is a "1", this function supports the **D1** Power Management State. Not support
8-6	RO	0h	**Reserved**
5	RO	0h	**Device Specific Initialization (DSI)** This bit indicates whether a special function initialization is required (beyond the PCI standard configuration header) before the generic class device driver is able to use it. A "1" indicates that the function requires a device specific initialization sequence following the transition to the D0 which is at the uninitialized state.

Power Management Capabilities Register (PMCR) — Offset 0x82[cont'd]

Bit	R/W	Default	Description
4	RO	0h	**Reserved**
3	RO	0h	**PME Clock** When this bit is a "1", it indicates that the function relies on the presence of the PCI clock for PME# operation. When this bit is a "0", it indicates that no PCI clock is required for the function to be generated. The function does not support PME# generation in any state. It must return "0" for this field.
2-0	RO	010b	**Version** A value of 010b indicates that this function complies with PCI Power Management Interface Specification Revision 1.1.

6.1.6.48 Power Management Control/Status Register (PMCSR) — Offset 0x84

Bit	R/W	Default	Description
15	RO	0h	**PME_Status** Do not support PME# generation from **$D3_{cold}$**.
14-13	RO	0h	**Data_Scale** Do not implement this field.
12-9	RO	0h	**Data_Select** Do not implement this field.
8	RO	0h	**PME_en** Do not support PME# generation from any D-state.
7-2	RO	0h	**Reserved**
1-0	R/W	0h	**Power State** This 2-bit field is used to determine the current power state of the function and set the function in a new power state. The definition of the field value is given below: 00b – **D0** 01b – **D1** 10b – **D2** 11b – **$D3_{hot}$** If software attempts to write an unsupported and optional state to this field, the writing operation must be completed normally on the bus; otherwise, data is discarded and the state won't change. So when a "01b" or "10b" is written to this register, data is discarded and the state won't change.

6.1.6.49 PMCSR PCI to PCI Bridge Support Extensions — Offset 0x86

Bit	R/W	Default	Description
7	RO	0h	**BPCC_En (Bus Power/Clock Control Enable)** A "1" indicates that the bus power/clock control mechanism defined in PCI Bus Power Management Interface Specification Revision 1.1 Section 4.7.1 is enabled. Otherwise, it is disabled. When it is disabled, the bridge's PMCSR Power State field cannot be used by software of the system to control the power or clock of the bridge's secondary bus.
6	RO	0h	**B2_B3# (B2/B3 Support for $D3_{hot}$)** The state of this bit determines the action that is to occur as a direct result of programming the function to $D3_{hot}$. A "1" indicates that when the bridge function is programmed to **$D3_{hot}$**, its secondary bus' PCI clock will be stopped (**B2**). A "0" indicates that when the bridge function is programmed to **$D3_{hot}$**, its secondary bus will have its power removed. This bit is only meaningful if bit 7 (BPCC_En) is a "1".
5-0	RO	0h	**Reserved**

6.1.6.50 Data Register (DR) — Offset 0x87

Bit	R/W	Default	Description
7-0	RO	0h	**Data** This register is used to report the state's dependent data requested by Data_Select field. The value of this register is scaled by the Data_Scale field.

6.1.7 PCI I/O Register -- Bus Master IDE I/O Registers

6.1.7.1 Bus Master IDE Command Registers (BMICR) — Offset 0x0 (Primary) / 08 (Secondary)

Bit	R/W	Default	Description
7-4	RO	0h	**Reserved** These bits must return 0h while being read.
3	R/W	0h	**Write or Read Control (WRC)** This bit sets the direction of the bus master transfer. 1: Bus master writes are performed. 0: Bus master reads are performed. This bit must not be changed when the bus master function is active.
2-1	RO	0h	**Reserved**
0	R/W	0h	**Start/Stop Bus Master (SBM)** Writing a “1” to this bit enables the bus master operation of the controller. A bus master operation begins when the value of this bit has changed from a “0” to a “1”. The controller transfers data between the IDE device and the memory only when this bit is set. Writing a “0” to this bit can halt the master operation and all the state information is lost. The master mode operation cannot be stopped and resumed. If this bit is reset while a bus master operation is still active (BMA=1) and the drive has not finished its data transfer (INT=0) yet, the bus master command is aborted, and data transferred from the drive may be discarded before being written to the system memory. This bit shall be reset after the data transfer is completed, as indicated by either BMA being reset or INT being set, or both.

6.1.7.2 Bus Master IDE Command and Status Registers (BMICSR) — Offset 0x2, 0xA

Bit	R/W	Default	Description
7	RO	0b	**Reserved**
6	R/W	0h	**Drive 1 DMA Capable (D1DMA)** This read/write bit is set by the device's dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transferring, and that the controller has been initialized for optimum performance.
5	R/W	0h	**Drive 0 DMA Capable (D0DMA)** This read/write bit is set by the device's dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transferring, and that the controller has been initialized for optimum performance.
4-3	RO	00b	**Reserved** These bits must return 0h when being read..
2	R/WC	0h	**Interrupt (INT)** This bit is set by the local CPU when an interrupt is required to inform the host. This bit is cleared when a "1" is written to it by host software. Software uses this bit to determine if an IDE device has asserted its interrupt line. When this bit is read as a "1," all data transferred from the drive is visible in the system memory.
1	R/WC	0h	**Error (ERR)** This bit is set when the controller encounters an error in the process of transferring data to or from the memory. This bit is cleared when a "1" is written to it via software.
0	RO	0h	**Bus Master IDE Active (BMA)** This bit is set when bit 0 of BMICR register is written by "1". This bit is cleared when the last transfer of the region is performed. EOT for that region is set in the region descriptor. It is also cleared when SBM is cleared. When this bit is read as a "0", all data transferred from the drive during the previous bus master command will be visible in the system memory, unless the bus master command has been aborted.

6.1.7.3 Bus Master IDE Descriptor Table Pointer Registers (BMIDTPR) — Offset 0x4, 0xCs

Bit	R/W	Default	Description
31-2	R/W	0	**Base Address of Descriptor Table (BADT)** This register provides the base memory address of the Descriptor Table.
1-0	-	0	**Reserved**

6.1.8 Virtual IDE Interface and Status Registers

The following registers are used to control the IDE channel action. These registers can also be R/W by the CPU. The content of these registers doesn't transfer directly to the IDE channel. The CPU will handle data to follow up the RAID mode setting.

1. The base address of primary IDE Command Registers (offset 0x0 ~0x7) is defined in PCI Configuration Register 10h~13h (Primary Channel Command Block Register) and these primary IDE Command Registers can be accessed by the CPU whose memory addresses are 0x8000h~0x08007h and 0x0800Ah~0x0800Fh.
2. The base address of primary IDE Alternate Status/Device Control Register is defined in PCI Configuration Register 14h~17h (Primary Channel Control Block Register) and the Primary IDE Alternate Status/Device Control Register can be accessed by the CPU whose memory addresses are 0x08016h and 0x0801Ah.
3. The base address of the secondary IDE Command Registers (offset 0x0~0x7) is defined in PCI Configuration Register 18h~1Bh (Secondary Channel Command Block Register) and these secondary IDE Command Registers can be accessed by the CPU whose memory addresses are 0x8020h~0x08027h and 0x0802Ah~0x2Fh.
4. The base address of Secondary IDE Alternate Status/Device Control Register is defined in PCI Configuration Register 1Ch~1Fh (Secondary Channel Control Block Register) and these Secondary IDE Alternate Status/Device Control Registers can be accessed by the CPU whose memory addresses are 0x08036h and 0x0803Ah.
5. For 6.1.4.3 ~ 6.1.4.6 registers, when IDE Device Control Register bit 7 (HOB) is set to 1, these registers are extended for 48-bit address feature setting for ATA-133 spec. The PCI shares the same IO space when HOB is 1 or 0. For the CPU address space, if HOB is set to 1, they are mapping from 0x0800A to 0x0800D for the primary IDE channel and 0x0802A to 0x0802D for the secondary channel. Please refer to the ATA specification for the detailed register definition.

6.1.8.1 Primary/Secondary IDE Data Registers — PCI IO Space: Offset 0x0, CPU Memory Space: 0x08000/0x08020

Bit	R/W	Default	Description
15-0	R/W	0	**IDE Data Register** This register is for PIO data access only.

6.1.8.2 Primary/Secondary IDE Error/Feature Registers — PCI IO Space: Offset 0x1, CPU Memory Space: 0x08001/0x08021 (0x0800E/0x0802E)

This is an IDE Error Register when it is read. It is an IDE Feature Register when written from the PCI access. However, the CPU can R/W these registers and the content will be mirrored to the PCI access. The CPU memory space 0x08001 and 0x08021 are assigned to Error registers for CPU accessing and 0x0800E and 0x0802E are assigned to Feature registers for CPU accessing.

Bit	R/W	Default	Description
7-0	R/W	0	**IDE Error/Feature Register** When this register is read, it is an IDE Error Register. When this register is written, it is an IDE Feature Register.

6.1.8.3 Primary/Secondary IDE Sector Count (Ext.) Registers — PCI IO Space: Offset 0x2, CPU Memory Space: 0x08002/0x08022 (0x0800A/0x0802A)

Bit	R/W	Default	Description
7-0	R/W	0	**IDE Sector Count Register** The content of this register becomes a command parameter when the Command register is written. The address is the same as Sector Count register in PCI space. If Device Control Register bit 7 HOB is set to 1, this register is Sector Count Ext. Register.

6.1.8.4 Primary/Secondary IDE Sector Number (Ext.) Registers — PCI IO Space: Offset 0x3, CPU Memory Space: 0x08003/0x08023 (0x0800B/0x0802B)

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Sector Number Register** The content of this register becomes a command parameter when the Command register is written. The address is the same as Sector Count register in PCI space. If Device Control Register bit 7 HOB is set to 1, this register is Sector Number Ext. Register.

6.1.8.5 Primary/Secondary IDE Cylinder Low (Ext.) Registers — PCI IO Space: Offset 0x4, CPU Memory Space: 0x08004/0x08024 (0x0800C/0x0802C)

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Cylinder Low Register** The content of this register becomes a command parameter when the Command register is written. The address is the same as Sector Count register in PCI space. If Device Control Register bit 7 HOB is set to 1, this register is Cylinder Low Ext. Register.

6.1.8.6 Primary/Secondary IDE Cylinder High (Ext.) Registers — PCI IO Space: Offset 0x5, CPU Memory Space: 0x08005/0x08025 (0x0800D/0x0802D)

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Cylinder High Register** The content of this register becomes a command parameter when the Command register is written. The address is the same as Sector Count register in PCI space. If Device Control Register bit 7 HOB is set to 1, this register is Cylinder High Ext. Register.

6.1.8.7 Primary/Secondary IDE Device/Head Registers — PCI IO Space: Offset 0x6, CPU Memory Space: 0x08006/0x08026

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Device/Head Register** Bit 4 DEV in this register selects the device. Other bits in this register are command dependent.

6.1.8.8 Primary/Secondary IDE Status/Command Registers — PCI IO Space: Offset 0x7, CPU Memory Space: 0x08007/0x08027 (0x0800F/0x0802F)

This is an IDE Status Register when it is read. It is an IDE Command Register when written from PCI access. However, the CPU can R/W these registers and the content will be mirrored to PCI access. The CPU memory space 0x08007 and 0x08027 are assigned to Status registers for CPU accessing and 0x0800F and 0x0802F are assigned to Command registers for CPU accessing.

Table 6-8. Status Register

Bit	R/W	Default	Description
7	RO	0h	**Busy** When this bit is set to 1, it indicates that the device is busy.
6	RO	0h	**Device Ready** When this bit is set to 1, it indicates that the device is ready and can accept and attempt to execute all implemented commands.
5-4	-	0h	**Reserved**
3	RO	0h	**Data Request** When this bit is set to 1, it indicates that the device is ready to transfer a word of data between the host and device.
2-1	-	0h	**Reserved**
0	RO	0h	**Error** When this bit is set to 1, it indicates that an error occurred during the execution of the previous command.

Table 6-9. Command Register

Bit	R/W	Default	Description
7-0	WO	-	**Command Code** This register contains the command code being sent to the device.

6.1.8.9 Primary/Secondary IDE Alternate Status/Device Control Registers — PCI IO Space: Offset 0x6, CPU Memory Space: 0x08016/0x08036 (0x0801A/0x0803A)

The base address of the Primary IDE Alternate Status/Device Control Register is defined in PCI Configuration Register 14h~17h (Primary Channel Control Block Register) and the base address of the Secondary IDE Alternate Status/Device Control Register is defined in PCI Configuration Register 1Ch~1Fh (Secondary Channel Control Block Register). When this register is read, it is Alternate Status Register, which contains the same information as the IDE Status Register. When this register is written, it is Device Control Register.

Bit	R/W	Default	Description
7	WO	-	**High Order Byte (HOB)** This bit is defined by the 48-bit address feature set. If this bit is on, extend register can be accessed.
6-3	-	-	**Reserved**
2	WO	-	**Software Reset (SRST)** This is a software reset bit. When it is written by 1, a software reset disk interrupt will occur.
1	WO	-	**nIEN** This is an enabled bit for the device assertion of interrupt to the host. When it is cleared to 0 and the device is selected, the device interrupt shall be enabled from itself. When it is set to 1 or the device is not selected, the device's interrupt is disabled by itself.
0	R/W	0	**Reserved** It must be 0

6.1.9 Local CPU Registers Definition

6.1.9.1 IDE Transfer Control Registers

6.1.9.1.1 IDE Transfer Counter Registers (PIDETCR/SIDETCR) — Address 0x08100, 0x08110

Bit	R/W	Default	Description
15-0	R/W	0h	**IDE Transfer Count Register (PIDETCR/SIDETCR)** This register is a counter that knows how many sectors will be transferred from IDE disk/FIFO to FIFO/IDE disk. t0 means 65536 sectors will be transferred.

6.1.9.1.2 IDE Operation Registers (PIDEOPR/SIDEOPR) — Address 0x08102, 0x08112

Bit	R/W	Default	Description
7	R/W	0h	**IDE DMA Transfer Start** When this bit is set, the IDE bus will start to transfer data. This bit is cleared by the chipset itself.
6	R/W	0h	**IDE Device Reset** When set to 1, this bit will cause the chipset to send a reset signal to the IDE device. This bit is cleared by writing a “0” to it via software.
5	R/W	0h	**IDE Status Reset** When set to 1, this bit will cause the chipset to reset the related circuit of its internal IDE bus interface and FIFO. This bit is cleared by the chipset itself.
4	RO	0h	**Disk Interrupt Pending Bit** When the interruption of the disk is active, this bit is set to 1. This bit will be cleared when users read the IDE status port.
3	R/W	0h	**Disk Interrupt Block Bit** When this bit is set, bit 4 will block the CPU.
2-0	R/W	0h	**Transfer Mode** These bits select the transfer modes of the disk. 000: PIO Read 001: PIO Write 010: DMA Read 011: DMA Write 100: Ultra DMA Read 101: Ultra DMA Write 111: NOP

6.1.9.1.3 IDE PIO and DMA Timing Registers (PPIOTMR/SPIOTMR) — Address 0x08103, 0x08113

The value is a two-clock cycle base.

Bit	R/W	Default	Description
7-4	R/W	Ah	**IDE PIO and DMA Transfer Active Time** These bits define the T2 or Td timing. The unit is two clock periods of the selected clock.
3-0	R/W	3h	**IDE PIO and DMA Transfer Recovery Time** These bits define the T2I or Tk timing. The unit is two clock periods of the selected clock.

Following tables are the reference values in different IDE transfer modes. The values in each field are calculated in the two-clock period of 50 MHz and 66 MHz. The value in the parenthesis is based on the 66 MHz IDE clock.

PIO Register & Data Transfer:

Mode	0	1	2	3	4
T_2	8(10*)	8(10*)	8(10*)	3(3*)	2(3)
T_{2i}	8(10*)	2(3*)	1(1*)	2(3*)	1(1)

MultiWord DMA Transfer:

Mode	0	1	2
T_d	6(8)	2(3*)	2(3)
T_k	6(8)	2(2*)	1(1)

Note:
1. The value in the parenthesis is calculated based on the 66 MHz IDE Clock.
2. The symbol * means the best programming value at that mode.

6.1.9.1.4 IDE Ultra DMA Timing Registers (PUDMATMR/SUDMATMR) — Address 0x08104, 0x08114

Bit	R/W	Default	Description
7	R/W	0b	**Ultra DMA Mode 5, 6 Select** This bit defines the mode of Ultra DMA Mode. When it is set, the Ultra DMA mode is mode 5 or 6. When it is cleared, the Ultra DMA mode is mode 0,1,2,3 or 4.
6-4	R/W	3h	**Ultra DMA Data Setup Time** These bits define the Ultra DMA Tdvs timing. The unit is one clock period of the selected clock frequency.
3	R/W	0b	**Reserved**
2-0	R/W	1h	**Ultra DMA Data Hold Time** These bits define the Ultra DMA Tdvh timing. The unit is one clock period of the selected clock frequency.

Note: Tdvs + Tdvh = Ultra DMA HSTROBE Tcyc value.

Mode	0	1	2	3	4	5	6
Tdvs	3(4)	3*(4)	2(3)	2(2*)	1(1*)	1*(2)	1(1*)
Tdvh	3(4)	1*(2)	1(1)	1(1*)	1(1*)	1*(2)	1(1*)

Note:
1. The value in the parenthesis is calculated based on the 66 MHz IDE Clock.
2. The symbol * means the best programming value at that mode.
3. To get the best performance of Ultra DMA Mode 1 and 5, 50 MHz IDE Clock Frequency should be select.

6.1.9.2 FIFO Access Control Registers (PFIFOCR/SFIFOCR) — Address 0x08105, 0x08115

Bit	R/W	Default	Description
7	R/W	0	**Write FIFO Action** When this bit is set to 1, it indicates FIFO Low Word /FIFO High Word registers will be FIFO data write ports.
6	R/W	0	**Read FIFO Action** When this bit is set to 1, it indicates 0x8108h~0x810Bh FIFO Low Word /FIFO High Word registers will be FIFO data read ports.
5-0	RO	0	**Reserved**

6.1.9.3 FIFO Status Registers (PFIFOSR/SFIFOSR) — Address 0x08106, 0x08116

Bit	R/W	Default	Description
7	RO	1	**FIFO Empty** When this bit is set to 1, it indicates the FIFO is empty.
6	RO	0	**FIFO Full** When this bit is set to 1, it indicates the FIFO is full.
5-0	RO	0	**Reserved**

6.1.9.4 FIFO Low Word Access Registers (PFIFOLR/SFIFOLR)— Address 0x08108, 0x08118

Bit	R/W	Default	Description
15-0	R/W	0h	**FIFO Low Word Access Register**

6.1.9.5 FIFO High Word Access Registers (PFIFOHR/SFIFOHR)— Address 0x0810A, 0x0811A

Bit	R/W	Default	Description
15-0	R/W	0h	**FIFO High Word Access Register**

6.1.9.6 IDE Interface Registers

These registers are mapped to the IDE Interface registers. When they are accessed, an IDE bus cycle will be generated to access the disk register. For detailed register information, please refer to the ATA specification.

Table 6-10. List of IDE I/O Port Primary Channel Address Mapping

CPU Memory Mapping Address (Note)	Device Address					Register Name		Register Size	Access Size
	DCS0#	DCS1#	DA2	DA1	DA0	Read	Write		
0x08120	A	N	0	0	0	Data	Data	16 bits	32/16 bits
0x08121	A	N	0	0	1	Error	Features	8 bits	8 bits
0x08122	A	N	0	1	0	Sector Count	Sector Count	8 bits	8 bits
0x08123	A	N	0	1	1	Sector Number LBA[7:0]	Sector Number LBA[7:0]	8 bits	8 bits
0x08124	A	N	1	0	0	Cylinder Low LBA[15:8]	Cylinder Low LBA[15:8]	8 bits	8 bits
00x08125	A	N	1	0	1	Cylinder High LBA[23:16]	Cylinder High LBA[23:16]	8 bits	8 bits
0x08126	A	N	1	1	0	Device/Head LBA[27:24]	Device/Head LBA[27:24]	8 bits	8 bits
0x08127	A	N	1	1	1	Status	Command	8 bits	8 bits
0x08136	N	A	1	1	0	Alternate Status	Device Control	8 bits	8 bits

Note: The address in the table is for the Primary IDE interface registers. For the Secondary IDE interface register, the address is ranged from 0x08140h to 0x08147h and 0x08156h.

6.1.9.6.1 IDE Data Registers (PDR/SDR) — Address 0x08120, 0x08140

Bit	R/W	Default	Description
15-0	R/W	0	**IDE Data Register** This register is for PIO data access only.

6.1.9.6.2 IDE Error/Feature Registers (PEFR/SEFR) — Address 0x08121, 0x08141

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Error/Feature Register** When read, this register is IDE Error Register. When written, it is IDE Feature Register.

6.1.9.6.3 IDE Sector Count Registers (PSCR/SSCR) — Address 0x08122, 0x08142

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Sector Count Register**

6.1.9.6.4 IDE Sector Number Registers (PSNR/SSNR) — Address 0x08123, 0x08143

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Sector Number Register**

6.1.9.6.5 IDE Cylinder Low Registers (PCLR/SCLR) — Address 0x08124, 0x08144

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Cylinder Low Register**

6.1.9.6.6 IDE Cylinder High Registers (PCHR/SCHR) — Address 0x08125, 0x08145

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Cylinder High Register**

6.1.9.6.7 IDE Device/Head Registers (PHDR/SHDR) — Address 0x08126, 0x08146

Bit	R/W	Default	Description
7-0	R/W	0	**IDE Device/Head Register**

6.1.9.6.8 IDE Status/Command Registers — Address 0x08127, 0x08147

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Status/Command Register** This register is IDE Status Register when read. It is IDE Command Register when written.

6.1.9.6.9 IDE Alternate Status/Device Control Registers (PSTUR/SSTUR) — Address 0x08136, 0x08156

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Alternate Status/Device Control Register** This register is IDE Alternate Status Register when read. It is IDE Device Control Register when written.

6.1.9.7 PCI Channel Control Registers

6.1.9.7.1 Channel Transfer Count Registers (PTCR/STCR) — Address 0x08200, 0x08208

Bit	R/W	Default	Description
15-0	R/W	0h	**Channel Transfer Count Register** This register defines how many sectors will be transferred on the PCI bus for a certain IDE channel.

6.1.9.7.2 Channel Operation Registers (POPR/SOPR) — Address 0x08202, 0x0820A

Bit	R/W	Default	Description
15	RO	-	**Channel CBLID# Signal** CBLID# signal in the cable of the primary channel.
14-11	RO	0	**Reserved**
10	R/W	0	**Channel Slave Device Enable** 1: Enable the slave device. 0: Disable the slave device. Bit 10 and bit 9 will affect the virtual status registers (PSTAR: 0x08007 and SSTAR: 0x08027) when PCI reads these two registers. There is no effect on the local CPU access. For the local CPU read operations, always return the status register value.
9	R/W	0	**Channel Master Device Enable** 1: Enable master device. 0: Disable master device. Bit 10 and 9 will affect the virtual status registers (PSTAR:0x08007 and SSTAR: 0x08027) when PCI reads these two registers. There is no effect on the local CPU access. When the virtual status register is read from the PCI bus, the read values are shown below. (bit 10, 9, device select): response value 0 0 0$^{\infty}$: 0x7f 0 0 1$^{\infty}$: 0x7f 0 1 0$^{\infty}$: status register value 0 1 1$^{\infty}$: 0x0 1 0 0$^{\infty}$: 0x7f 1 0 1$^{\infty}$: status register value 1 1 x$^{\infty}$: status register value For the local CPU read operations, always return the status register value.
8	R/W	0	**Channel Transfer Direction** When this bit is set to 1, data will be transferred from PCI to FIFO; otherwise, the data will be transferred from FIFO to PCI.
7	R/W	0	**Channel Transfer Start** When this bit is set to 1, the data will start to transfer between FIFO/PCI and PCI/FIFO. After the transfer is over (The last block transfer is finished.), it is cleared by the chipset itself.

Channel Operation Registers (POPR/SOPR) [cont'd]

Bit	R/W	Default	Description
6	R/W	0	**Last Transfer Bit** If this bit is set to 1, it indicates that the next block transfer will be the last one. After the last block transfer is over, it is cleared by the chipset itself, and a Channel Block Transfer Finished Interrupt occurs.
5	R/W	0	**Transfer Mode** This bit indicates which access operation will be active at the PCI bus. 0: PIO mode. 1: DMA mode. If the PIO mode is selected, PCI is in the PCI slave mode. If the DMA mode is selected, PCI is in the bus master mode.
4	R/W	0	**Reset Channel Operation** When this bit is set to 1, all PCI related circuits will be reset. This bit is set by software and cleared by the chipset itself. Always read as "0".
3-2	R/W	0h	**Next Access FIFO Number** This field defines which FIFO should be accessed by the PCI bus in the next PCI cycle. 01: Primary disk FIFO 10: Secondary disk FIFO 11: Dual FIFO 00: NOP When the current block transfer is finished, a reload interrupt will be sent to the CPU, and software will update this field and other bits in this register.
1-0	RO	0h	**Current Access FIFO Number** This field defines which FIFO is accessed in the current PCI cycle. 01: Primary disk FIFO 10: Secondary disk FIFO 11: Dual FIFO When the last transfer is completed, these two bits will be cleared to "0" by the chipset itself.

6.1.9.8 Rebuild Registers

6.1.9.8.1 Rebuild Block Counter Register (RBCTR) — Address 0x08210

Bit	R/W	Default	Description
15-0	R/W	0h	**Rebuild Block Counter Register** This register records how many sectors will be accessed in the reconstruction operation.

6.1.9.8.2 Rebuild Operation Register (RBOPR) — Address 0x08212

Bit	R/W	Default	Description
7	R/W	0h	**Rebuild Start** When this bit is set to 1, the disk's reconstruction operation will be started.
6	R/W	0h	**Reset Rebuild Operation** If this bit is set to 1, all reconstruction operations will be stopped. Disk channel reset must be done after this bit is set. This bit is cleared by the chipset itself. Always read as 0.
5-1	-	0h	**Reserved**
0	R/W	0h	**Rebuild Direction** 0: From the primary disk FIFO to the secondary disk FIFO. 1: From the secondary disk FIFO to the primary disk FIFO.

6.1.9.9 Interrupt Registers

6.1.9.9.1 Interrupt Pending Register (INTPR) — Address 0x08218

The CPU writes 1 to clear the relative bit.

Bit	R/W	Default	Description
15	R/W	0h	**Primary Disk Interrupt** This bit reflects the interrupt of the primary disk. Clear this bit by reading the primary disk register.
14	R/W	0h	**Secondary Disk Interrupt** This bit reflects the interrupt of the secondary disk. Clear this bit by reading the secondary disk register.
13	R/W	0h	**Primary Channel Block Transfer Finished Interrupt** This bit is set by the chipset itself to inform software that the primary channel transfer has been completed.
12	R/W	0h	**Secondary Channel Block Transfer Finished Interrupt** This bit is set by the chipset itself to inform software that the secondary channel transfer has been completed.
11	R/W	0h	**Primary Channel Next FIFO Reload Interrupt** This bit is set by the chipset itself to inform software to update the Primary Operation Register.
10	R/W	0h	**Secondary Channel Next FIFO Reload Interrupt** This bit is set by the chipset itself to inform software to update the Secondary Operation Register.
9	R/W	0h	**Primary Disk Software Reset Interrupt** When the primary IDE Device Control Register (in PCI IO address) is written and bit 2 (SRST) is set to 1, this interrupt bit is set to 1.
8	R/W	0h	**Secondary Disk Software Reset Interrupt** When the secondary IDE Device Control Register (in PCI IO address) is written and bit 2 (SRST) is set to 1, this interrupt bit is set to 1.
7	R/W	0	**Primary Command Write Interrupt** When the primary IDE Command Register (in PCI IO address) is written, this bit is set to 1.
6	R/W	0	**Secondary Command Write Interrupt** When the secondary IDE Command Register (in PCI IO address) is written, this bit is set to 1.
5	R/W	0	**Timer 0 Timeout Interrupt** When this bit is set to 1, it indicates the timer 1 timeout. Set Timer 0 Control Register bit 2 (MAX Count) to 0 to clear this bit.
4	R/W	0	**Timer 1 Timeout Interrupt** When this bit is set to 1, it indicates timer 2 timeout. Set Timer 1 Control Register bit 2 (MAX Count) to 0 to clear this bit.
3	R/W	0	**UART Interrupt** When this bit is set to 1, it indicates an UART interrupt occurred. To clear this bit, please refer to the UART Interrupt Identification Register.
2-1	-	0	**Reserved**
0	RO	0	**BIOS Ready** The local CPU must wait for this bit to be set to 1 then the CPU can access the IDE bus because the IDE bus is shared with BIOS ROM.

6.1.9.9.2 Interrupt Mask Register (INTMSR) — Address 0x0821A

Bit	R/W	Default	Description
15	R/W	1	**Primary Disk Interrupt Mask** 0: Enable the Primary Disk Interrupt. 1: Disabled.
14	R/W	1	**Secondary Disk Interrupt Mask** 0: Enable the Secondary Disk Interrupt. 1: Disabled.
13	R/W	1	**Primary Channel Block Transfer Finished Interrupt Mask** 0: Enable the Primary Channel Block Transfer Finished Interrupt. 1: Disabled.
12	R/W	1	**Secondary Channel Block Transfer Finished interrupt Mask** 0: Enable the Secondary Channel Block Transfer Finished Interrupt. 1: Disabled.
11	R/W	1	**Primary Channel Next FIFO Reload Interrupt Mask** 0: Enable the Primary Channel Next FIFO Reload Interrupt. 1: Disabled.
10	R/W	1	**Secondary Channel Next FIFO Reload Interrupt Mask** 0: Enable the Secondary Channel Next FIFO Reload Interrupt. 1: Disabled.
9	R/W	1	**Primary Disk Software Reset Interrupt Mask** 0: Enable the Primary Disk Software Reset Interrupt. 1: Disabled.
8	R/W	1	**Secondary Disk Software Reset Interrupt Mask** 0: Enable Secondary Disk Software Interrupt. 1: Disabled.
7	R/W	1	**Primary Command Write Interrupt Mask** 0: Enable the Primary Command Write Interrupt. 1: Disabled.
6	R/W	1	**Secondary Command Write Interrupt Mask** 0: Enable the Secondary Command Write Interrupt. 1: Disabled.
5	R/W	1	**Timer 0 Interrupt Mask** 0: Enable Timer 0 Interrupt. 1: Disabled.
4	R/W	1	**Timer 1 Interrupt Mask** 0: Enable Timer 1 Interrupt. 1: Disabled.
3	R/W	1	**UART Interrupt Mask** 0: Enable UART Interrupt. 1: Disabled.
2-0	-	-	**Reserved**

6.1.9.9.3 End of Interrupt Register (EOIR) — Address 0x0821C

Bit	R/W	Default	Description
7-0	R/W	0	**End of Interrupt Register** This register should be the last instruction in Interrupt Service Routine, and should be written only once in Interrupt Service Routine.

6.1.9.10 Timer Registers

6.1.9.10.1 Timer 0/1 Control Registers (T0CTLR/T1CTLR) — Address 0x08230, 0x08238

Bit	R/W	Default	Description
7	RO	0h	**Reserved**
6-4	R/W	0h	**Pre-Scaled Clock Frequency Select (PSCFS)** The timer's counting clock source (pre-scaled clock) can be selected by these 3 bits. 000: 66.6 MHz, 001: 33.3 MHz, 010: 16.65 MHz, 011: 8.325 MHz, 100: 4.163 MHz, 101: 2.082 MHz, 110: 1.041 MHz, 111: 0.52MHz
3	RO	0h	**Reserved**
2	R/W	0h	**MAX Count (MC)** This bit will be set whenever the counter reaches the maximum count value regardless of the timer's interrupting enabled bit. This bit gives users the ability to monitor the timer status through polling instead of through interrupting. When the interruption is enabled (IE=1) and MAX count (MC) bit is set, an interruption will be generated. When IE=0 and MC=1, no interruption will be generated. Note that this bit is the source of timer interrupted. This bit should be cleared by software before exiting the timer's interruption service routine. Otherwise, the interruption source will exist and the interrupt will be generated again after exiting the timer's ISR.
1	R/W	0h	**Interrupt Enable (IE)** When this bit is set, the interruption is enabled. The interruption will be generated at every terminal count (counter value = MAX count). When this bit is cleared, the interruption is disabled.
0	R/W	0h	**Count Enable (CE)** When this bit is set, the timer counter is increased by 1 every pre-scaled clock. When this bit is cleared, the timer counter value will be 0 and the counting is disabled.

6.1.9.10.2 Timer 0/1 Count Registers (T0CNTR/T1CNTR) — Address 0x08232, 0x0823A

Bit	R/W	Default	Description
15-0	RO	0h	**Current Count (CC)** The current count is the current contents of the timer counter. This register can be read at any time.

6.1.9.10.3 Timer 0 /1 Max. Count Registers (T0MAXR)/T1MAXR) — Address 0x08234, 0x0823C

Bit	R/W	Default	Description
15-0	R/W	FFFFh	**Maximum Count (MAXC)** This register is used to control the period of the interrupting generation. The counting source clock is the pre-scaled clock. The counter is increased by 1 every pre-scaled clock. When the current count is equal to the maximum count, the MC bit is set.

6.1.9.11 Miscellaneous Registers

6.1.9.11.1 IDE Clock Register (IDECLK) — Address 0x08252

Bit	R/W	Default	Description
7-3	-	0h	**Reserved**
2	R/W	0b	**Primary IDE Clock Frequency** 0: 66 MHz 1: 50 MHz There are two IDE clock frequencies in the chipset. Select a suitable clock to obtain the best performance. For example, the 66 MHz clock is selected in ATA133 mode, and 50 MHz is selected in ATA100 mode. Because the value of Timing Register is based on the clock cycle.
1	-	0b	**Reserved**
0	R/W	0b	**Secondary IDE Clock Frequency** 0: 66 MHz 1: 50 MHz There are two IDE clock frequencies in the chip. Select a suitable clock to obtain the best performance. For example, the 66 MHz clock is selected in ATA133 mode, and the 50 MHz one is selected in ATA100 mode. Because the value of Timing Register is based on the clock cycle.

6.1.9.11.2 GPIO Register (GPIOR) — Address 0x08254

Bit	R/W	Default	Description
7-0	R/W	0h	**GPIO[7:0]** This register is for the debugging purpose. Its value is output to PAD GPIO7-GPIO0.

6.1.10 UART Registers Definition

6.1.10.1 UART Receiver Buffer Register (URBR) — Address 0x09000

This register receives and holds the incoming data. It can hold from five to eight data bits. If the transmitted data is less than 8 bits, it aligns to the LSB. It contains a non-accessible shift register that converts the incoming serial data stream to a parallel 8-bit word. The bit 0 of this register is first received.

Bit	R/W	Default	Description
7-0	RO	-	**UART Receiver Buffer Register (URBR)** This register receives and holds the entering data.

6.1.10.2 UART Transmitter Buffer Register (UTBR) — Address 0x09000

This register holds and transmits the data via a non-accessible shift register. It converts the outgoing parallel data to a serial stream before transmission. It can hold from 5 to 8 data bits. If the transmitted data is less than 8 bits, it aligns to the LSB. The bit 0 of this register is first transmitted.

Bit	R/W	Default	Description
7-0	WO	-	**UART Transmitter Buffer Register (UTBR)** This register holds and transmits the data via a non-accessible shift register.

6.1.10.3 UART Interrupt Enable Register (UIER) — Address 0x09002

The UIER is used to enable (or disable) 3 active high interrupts that activate the interrupt outputs with its lower 3 bits: bit 0 to bit 2.

Bit	R/W	Default	Description
7-4	RO	0h	**Reserved** These bits are always “0”.
3	R/W	0	**Reserved.** The bit must be written to “0”.
2	R/W	0	**Enable Receiver Line Status Interrupt (ERLSI)** Set this bit high to enable the Receiver Line Status Interrupt, which is caused when Overrun, Parity, Framing or Break occurs.
1	R/W	0	**Enable Transmitter Buffer Register Empty Interrupt (ETBREI)** Set this bit high to enable the Transmitter Buffer Register Empty Interrupt.
0	R/W	0	**Enable Received Data Available Interrupt (ERDVI)** Set this bit high to enable the Received Data Available Interrupt and Time-out Interrupt in the FIFO mode.

6.1.10.4 UART Interrupt Identification Register (UIIR) — Address 0x09004

This register facilitates the host CPU to determine the interrupt priority and its source. The priority of the 4 existing interrupt levels is as follows:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Buffer Register Empty
4. Modem Status (lowest priority)

When a privileged interrupt is pending and the type of interrupt is stored in the UIIR which is accessed by the Host, the serial channel holds back all interrupts and indicates the highest priority pending interrupts to the Host. There are not any new interrupts acknowledged until the Host access finishes. The contents of the UIIR are described below. Table 6-11 lists the meaning of the interrupt identification.

Bit	R/W	Default	Description
7-6	RO	00b	**UART Interrupt Identification Register Bit 7, Bit 6 (UIIR7, UIIR6)** These two bits are set when UFCR(0)=1.
5-4	RO	00b	**Reserved** Always logic 0.
3	RO	0	**UART Interrupt Identification Register Bit 3 (UIIR3)** In the non-FIFO mode, this bit is logic 0. In the FIFO mode, this bit is set along with bit 2 when a time-out Interrupt is pending.
2-1	RO	00b	**UART Interrupt Identification Register Bit 2, Bit 1 (UIIR2, UIIR1)** These bits are used to identify the highest priority of the pending interrupt.
0	RO	1	**UART Interrupt Identification Register Bit 0 (UIIR0)** This bit is used to indicate a pending interrupt in either a hardwired priority or a polled environment in the logic 0 state. When the condition takes place, UIIR contents may be used as a pointer to the appropriate interrupt service routine.

Table 6-11. UART Interrupt Identification Register

FIFO Mode	UART Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt RESET Control
0	X	X	1	-	None	None	-
0	1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	ULSR READ
0	1	0	0	Second	Received Data Available	Received Data Available	URBR Read or FIFO drops below the trigger level
1	1	0	0	Second	Character Timer-out Indication	No characters have been removed from or input to the RCVR FIFO during the last 4 character times, and there is at least 1 character in it at this time.	URBR READ
0	0	1	0	Third	Transmitter Buffer Register Empty	Transmitter Buffer Register Empty	UIIR READ if TBRE is the Interrupt Source or TBR write

Note: X = Not Defined

6.1.10.5 UART FIFO Control Register (UFCR) — Address 0x09004

This register is used to enable and clear the FIFO, and set the RCVR FIFO trigger levels.

Bit	R/W	Default	Description
7-6	WO	00b	**UART FIFO Control Register Bit 7, Bit 6 (UFCR7,UFCR6)** These bits set the trigger levels for the RCVR FIFO interrupt. **UFCR7 UFCR6 RCVR FIFO Trigger Level** 0 0 1 byte 0 1 4 bytes 1 0 8 bytes 1 1 14 bytes
5-4	WO	00b	**Reserved**
3	WO	0	**Reserved** This bit does not affect the Serial Channel operation. RXRDY and TXRDY functions are not available in this controller.
2	WO	0	**XMIT FIFO Reset (XFRST)** This self-clearing bit clears all contents of the XMIT FIFO and resets its related counter to 0 by a logic “1”.
1	WO	0	**RCVR FIFO Reset (RFRST)** Setting this self-clearing bit to a logic “1” clears all contents of the RCVR FIFO and resets its related counter to 0 (except the shift register).
0	WO	0	**FIFO Enable (FEN)** XMIT and RCVR FIFOs are enabled when this bit is set high. The XMIT and RCVR FIFOs will be disabled and cleared when this bit is cleared to low. This bit has to be a logic “1” if the other bits of the UFCR are written or they will not be properly programmed. When this register changes to a non-FIFO mode, all contents will be cleared.

6.1.10.6 UART Divisor Latch LSB Register (UDLL) — Address 0x09000

UDLL and UDLM are combined to one 16-bit number when bit 7 (DLAB) of the Line Control Register is 1. It provides the divisor range from 1 to 2^{16} for the external reference clock to obtain the desired baud rate. Please refer to Table 6-12 for the baud rate values.

Bit	R/W	Default	Description
7-0	R/W	00h	**UART Divisor Latch LSB (UDLL)** This register stores the low byte of the divisor.

6.1.10.7 UART Divisor Latch MSB Register (UDLM) — Address 0x09002

Bit	R/W	Default	Description
7-0	R/W	00h	**UART Divisor Latch MSB (UDLM)** This register stores the high byte of the divisor.

Table 6-12. Baud Rates Using (1.8432 MHz) Clock

Desired Baud Rate	Divisor Used
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19200	6
38400	3
57600	2
115200	1

6.1.10.8 UART Line Control Register (ULCR) — Address 0x09006

ULCR controls the format of the data character and gives the information of the serial line.

Bit	R/W	Default	Description
7	R/W	0	**Divisor Latch Access Bit (DLAB)** This bit must be set high to access the Divisor Latches of the baud rate generator during read or write operations. It must be set low to access the Data Register URBR and UTBR or the Interrupt Enable Register.
6	R/W	0	**Break Control (BREAK)** Force the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, and this state will remain till a low level resets this bit and enables the serial port to alert the terminal in a communication system.
5	R/W	0	**Stick Parity Bit (SP)** When this bit and Parity Enable (PEN) bit are high at the same time, the parity bit is transmitted and then detected by the receiver. In the opposite state, the parity bit is detected by Even Parity Select (EPS) bit to force the parity to a known state and to check the parity bit in a known state.
4	R/W	0	**Even Parity Select (EPS)** When the parity is enabled (Parity Enable=1), EPS=0 selects the odd parity, and EPS=1 selects the even parity.
3	R/W	0	**Parity Enable (PEN)** The parity bit between the last data word bit and the stop bit will be generated or checked (transmit or receive data) when this bit is high.
2	R/W	0	**Stop Bit Select (STB)** Specify the number of stop bits in each serial character, which are summarized below: **STB** **Word Length** **No. of Stop Bits** 0 - 1 bit 1 5 1.5 bits 1 6 2 bits 1 7 2 bits 1 8 2 bits Note: The receiver will ignore all stop bits beyond the first bit regardless of the number used in transmission.
1-0	R/W	00b	**Word Length Select Bit 1, Bit 0 (WLS1, WLS0)** Specify the number of bits in each serial character, which are encoded below: **WLS1** **WLS0** **Word Length** 0 0 5 bits 0 1 6 bits 1 0 7 bits 1 1 8 bits

6.1.10.9 UART Line Status Register (ULSR) — Offset 0x0900A

This register indicates the status. It is usually the first one that is read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel. The contents of the ULSR are described below:

Bit	R/W	Default	Description
7	R/W	0	**Error In RCVR FIFO (ERF)** In the 16550 mode, this bit is always 0. In the FIFO mode, it is set high when there is at least one parity error and framing or break interrupt in the FIFO. This bit is cleared when the CPU reads the ULSR if there are no subsequent errors in the FIFO.
6	RO	1	**Transmitter Empty (TEMT)** This bit indicates that the Transmitter Buffer Register and Transmitter Shift Register are both empty; otherwise, this bit is “0”. It has the same function in the FIFO mode.
5	RO	1	**Transmitter Buffer Register Empty (TBRE)** This bit indicates that the UTBR is empty and is ready to accept a new character for transmission. It is set high when a character is transferred from the UTBR to the Transmitter Shift Register, causing a priority 3 UIIR interrupt which is cleared by a read of UIIR. In the FIFO mode, it is set when the XMIT FIFO is empty, and is cleared when at least 1 byte is written to the XMIT FIFO.
4	R/W	0	**Break Interrupt (BI)** This bit indicates that the last received character was a break character. The break interrupt status bit will be asserted only when the last received character, parity bits and stop bits are all break bits. When an error condition is detected from ULSR(1) to ULSR(3), a Receiver Line Status interrupt (priority 1) will be produced in the UIIR with the UIER(2) previously enabled.
3	R/W	0	**Framing Error (FE)** When this bit is a logic 1, it indicates that the stop bit in the received character was not valid. It is reset low when the CPU reads the contents of the ULSR.
2	R/W	0	**Parity Error (PE)** This bit is set to a logic “1”, representing that the received data character does not have the correct even or odd parity, as selected by bit 4 of the ULCR (Even Parity Select). It will be reset to “0” whenever the ULSR is read by the CPU.
1	R/W	0	**Overrun Error (OE)** This bit is set to a logic “1”, representing that the URBR had been overwritten by the next character before it was read by the CPU. In the FIFO mode, the OE occurs when the FIFO is full and the next character has been completely received by the Shift Register. It will be reset when the CPU reads the ULSR.
0	R/W	0	**Data Ready (DR)** This bit is set to a logic “1”, which indicates a character has been received by the URBR. A logic “0” indicates all data in the URBR or RCVR FIFO have been read.

Table 6-13. Line Status Register Bits

ULSR Bits	Logic 1	Logic 0
ULSR(7) PE/FE/BI (FIFO mode)	Error	No error
ULSR(6) Transmitter Empty(TEMT)	Empty	Not empty
ULSR(5) Transmitter Buffer Register Empty (TBRE)	Empty	Not empty
ULSR(4) Break Interrupt(BI)	Break	No break
ULSR(3) Framing Error(FE)	Error	No error
ULSR(2) Parity Error(PE)	Error	No error
ULSR(1) Overrun Error(OE)	Error	No error
ULSR(0) Data Ready(DR)	Ready	Not ready

6.2 UART Operation

6.2.1 Reset

Reset of UART should be held high and more than 500 ns until initialization, which causes the followings:

1. Initialization of internal clock counters of the transmitter and receiver.
2. Resetting all bits of the UBSR (except that TBRE and TEMT are set only by a hardware reset), memory and logic elements. Before the reset, UART remains in the idle mode until programmed.

Table 6-14. Reset Control of Register and Pinout Signals

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All bits Low
Interrupt Identification Register	Reset	Bit 0 is high and bits 1-7 are low
FIFO Control Register	Reset	All bits Low
Line Control Register	Reset	All bits Low
Line Status Register	Reset	Bits 5, 6 are high, others are low.
TXD	Reset	High

6.2.2 Programming

Each serial channel is programmed by control registers whose contents define the character length, number of stop bits, parity and baud rate. Although the control register can be written in every order, the UIER should be the last because it controls whether the interrupt is enabled or not. After the port is programmed, these registers can still be updated whenever the port is not transferring data.

6.2.2.1 Programming Sequence

UART module is compatible with standard 16550. Below is the standard 16550 compatible component register access sequence:
To access URBR/UTBR:
1. Set bit 7 of the ULCR register to “0”
2. Access URBR/UTBR

To access UIER:
1. Set bit 7 of the ULCR register to “0”
2. Access UIER

To access UDLL/UDLM:
1. Set bit 7 of the ULCR register to “1”
2. Access UDLL/UDLM

6.2.3 Software Reset

This method allows returning to a completely known state without a system reset. This is achieved by writing the required data to the ULCR, UDLL and UDLM. The ULSR and URBR must be read before enabling interrupts in order to clear every residual data or status bit that may be invalid for subsequent operations.

6.2.4 Clock Input Operation

The input frequency of the Serial Channel is 48 MHz/26, not exactly 1.8432 MHz.

6.2.5 FIFO Interrupt Mode Operation

6.2.5.1 RCVR Interrupt

When bit 0 of UFCR and bit 0 of UIER are set to 1, the RCVR FIFO and receiver interrupts are enabled. The RCVR interrupt occurs under the following conditions:

a. The received data available interrupt, UIIR and received data available indication will be issued only if the FIFO has reached its programmed trigger level. They will be cleared as soon as the FIFO drops below its trigger level.
b. The receiver line status interrupt has higher priority than the received data available interrupt.
c. The time-out timer will be reset after receiving a new character or after the Host reads the RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the Host reads one character from the RCVR FIFO.

RCVR FIFO time-out Interrupt: By enabling the RCVR FIFO and receiver interrupts, the RCVR FIFO time-out interrupt will occur under the following conditions:

a. It will occur only if there is at least one character in the FIFO whenever the period between the most recent received serial character and the most recent Host read from the FIFO is longer than four consecutive character times.
b. The time-out timer will be reset after receiving a new character or after the Host reads the RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the Host reads one character from the RCVR FIFO.

6.2.5.2 XMIT Interrupt

By setting the bit 0 of UFCR and the bit 1 of UIER to high, the XMIT FIFO and transmitter interrupts are enabled, and the XMIT interrupt will occur as follows:

a. The transmitter interrupt will occur when the XMIT FIFO is empty, and it will be reset if the TBR is written or the UIIR is read.
b. The transmitter FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following conditions occur: TBRE=1 and there have not been at least two bytes in the transmitter FIFO at the same time since the last TBRE=1. The transmitter interrupt will be immediate after the bit 0 of UFCR is changed, if it is enabled. Once it is enabled, the TBRE indication is delayed 1 character time minus the last stop bit time.

The character time-out and RCVR FIFO trigger level interrupts are in the same priority order as the received data available interrupt. The XMIT FIFO empty is in the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation (bit 0 of UFCR is 1, and bit 0, 1, 2, 3 of UIER or all are “0”.) Either or both XMIT and RCVR can be in this operation mode which can be programmed by users and is responsible for checking the RCVR and XMIT status via the ULSR described below:

ULSR(7): RCVR FIFO error indication.
ULSR(6): XMIT FIFO and Shift register empty.
ULSR(5): The XMIT FIFO empty indication.
ULSR(4) - ULSR(1): Specify that errors have occurred, Character error status is handled in the same way as in the interrupt mode. The UIIR is not affected since UIER(2)=0.
ULSR(0): This bit is high whenever the RCVR FIFO contains at least 1 byte.

There is no trigger level reached or time-out condition indicated in the FIFO Polled Mode.

7. DC Characteristics

(VCC3, AVCC =3.3V±0.3V, Ta=0°C to 70°C)

Absolute Maximum Ratings*

Applied Voltage of VCC3, AVCC1, AVCC2, AVCC3----------0.3 V to +3.6V

Input Voltage of 3.3V Interface ... -0.3V to VCC3 +0.3V

Input Voltage of 5.0V tolerant Interface .....-0.3V to 6.3V

Tcase .....0°C to +70°C

Storage Temperature.....-40°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Ta=0°C to 70°C)

Symbol	Parameter	Conditions	Typ.	Max.	Min.
3.3V CMOS Interface					
V_{IL}	Input Low Voltage	VCC=3.0 ~ 3.6V		VCC3 x 0.3	- 0.3V
V_{IH}	Input High Voltage	VCC=3.0 ~ 3.6V		VCC3+ 0.3V	VCC3 x 0.7
V_{IH}	Input High Voltage (5V tolerant pad)	VCC=3.0 ~ 3.6V		6.3V	VCC3 x 0.7
V_{OL}	Output Low Voltage	I_{OL}= -2, -4, -8, -12mA		0.4	
V_{OH}	Output High Voltage	I_{OH}= 2, 4, 8, 12mA			2.4
I_{IL}	Input Leakage Current	V_{IL}= V_{SS} no pull-up or pull-down		1µA	-1µA
I_{OZ}	Tri-state Leakage Current			1µA	-1µA
Cin	Input Capacitance		3.8pF		
Cout	Output Capacitance			6.5pF	3.5pF
Cbld	Bi-directional Buffer			6.5pF	3.5pF

8. AC Characteristics

Table 8-1. Register transfer to/from device

Symbol	Parameter	Mode4	Mode0	Unit
t_0	Cycle time	120	600	ns
t_1	Address valid to IOR#/IOW# setup	30	90	ns
t_2	IOR#/IOW# pulse width	90	300	ns
t_{2i}	IOR#/IOW# recovery time	30	300	ns
t_3	IOW# data setup	30	270	ns
t_4	IOW# data hold	20	270	ns
T_5	IOR# data setup	20	50	ns
T_6	IOR# data hold	5	5	ns
T_9	IOR#/IOW# to address valid hold	15	30	ns

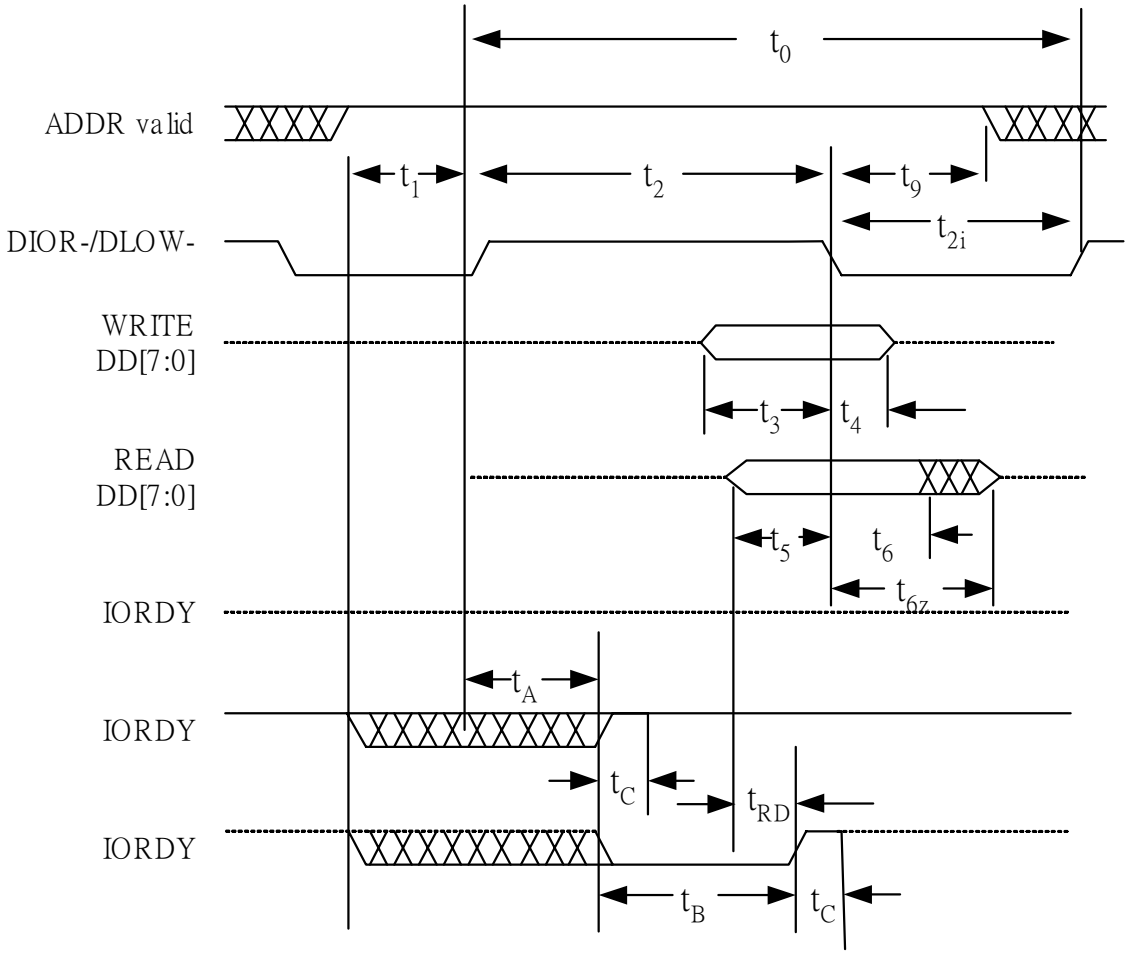


Figure 8-1.Register transfer to/from device

Table 8-2. Ultra DMA data burst timing requirements

Symbol	Parameter	Min	Max	Unit
$t_{2CYCTYP}$	Typical sustained average two cycle time	30_6-240_0	-	ns
t_{CYC}	Cycle time allowing for asymmetry and clock variations	13_6-112_0	-	ns
t_{UI}	Unlimited interlock time	0	-	ns
t_{ACK}	Setup and hold times for DACK#	30	-	ns
t_{ENV}	Envelope time	30	40	ns
t_{DVSIC}	Sender IC data valid setup time	6_6-100_0	-	ns
t_{DVHIC}	Sender IC data valid hold time	6_6-10_0	-	ns
t_{DSIC}	Recipient IC data valid setup time	2	-	ns
t_{DHIC}	Recipient IC data valid hold time	2	-	ns

Note: XX_6-XX_0 where the $_6$ indicates mode 6 and $_0$ indicates mode 0.

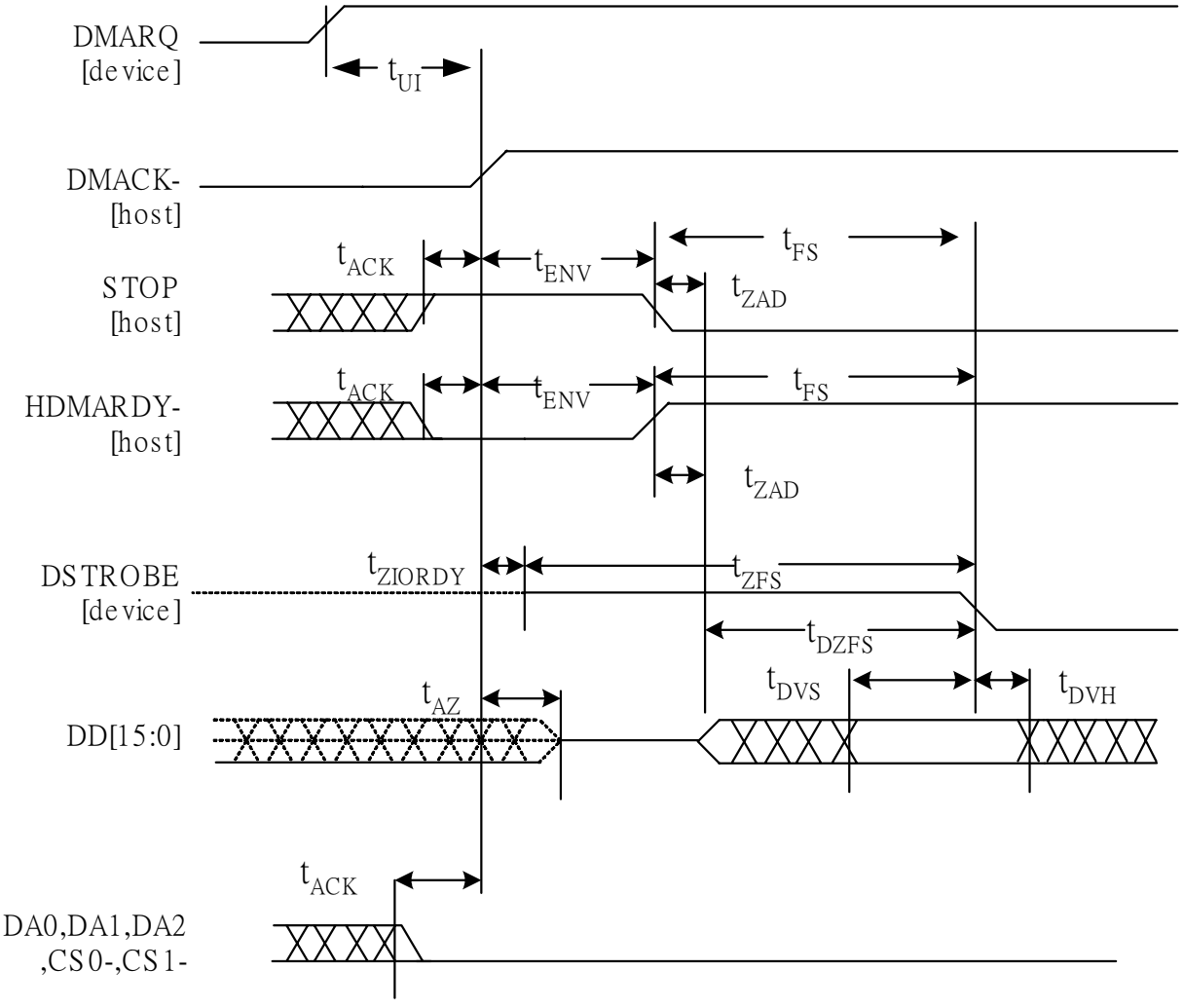


Figure 8-2.Initiating an Ultra DMA data-in burst

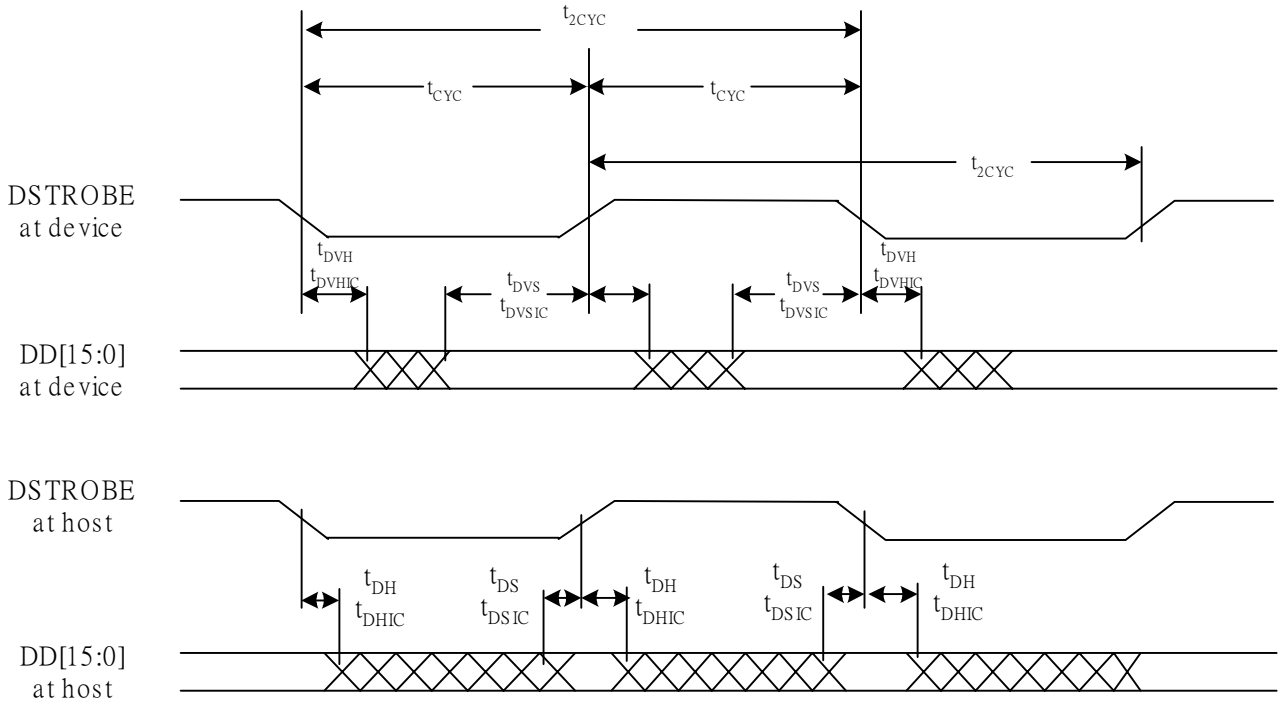


Figure 8-2. Sustained Ultra DMA data-in burst

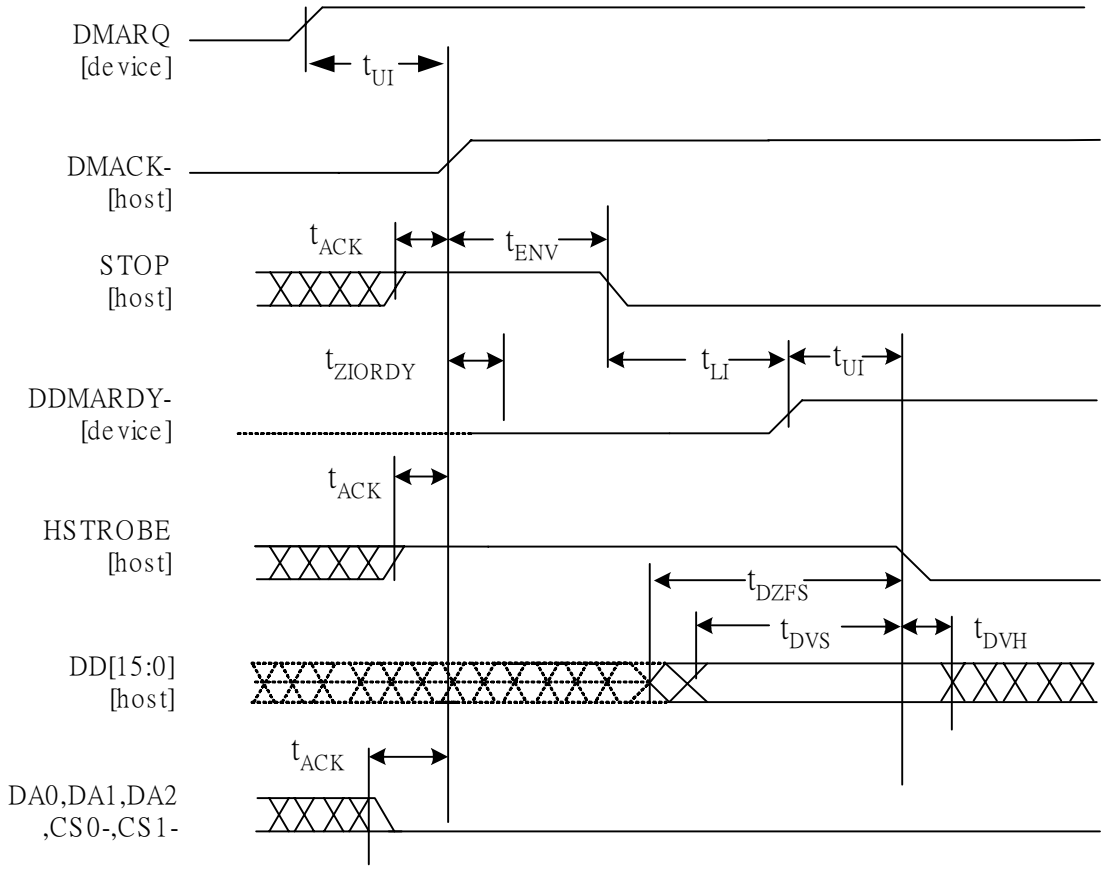


Figure 8-3. Initiating an Ultra DMA data-out burst

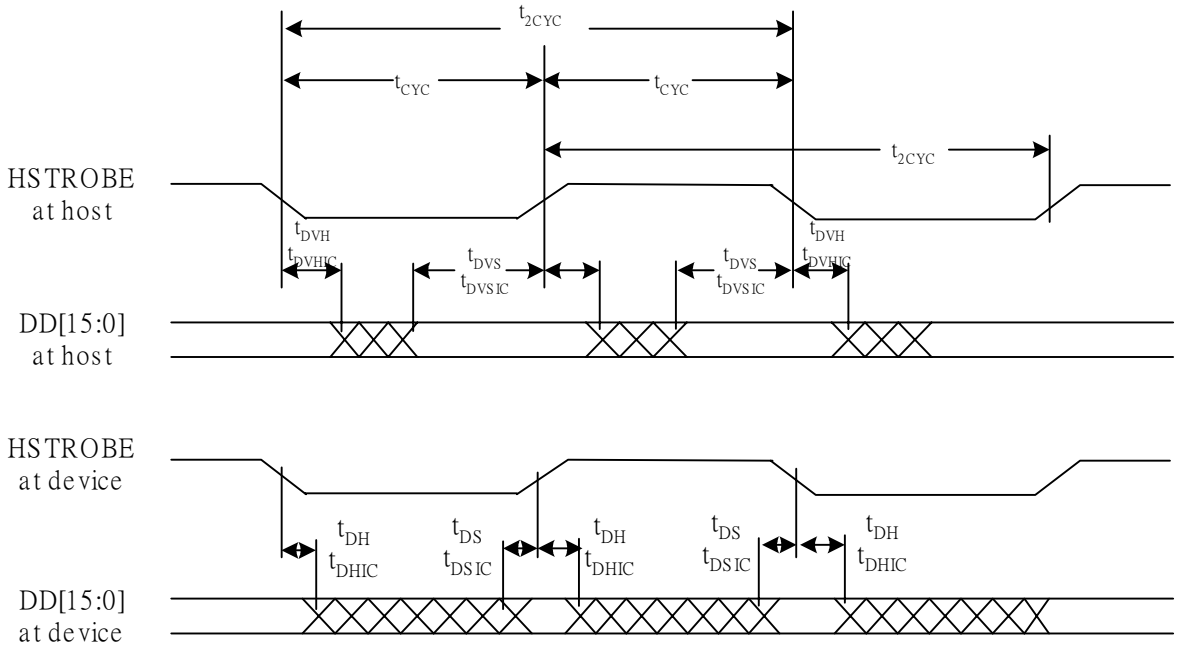
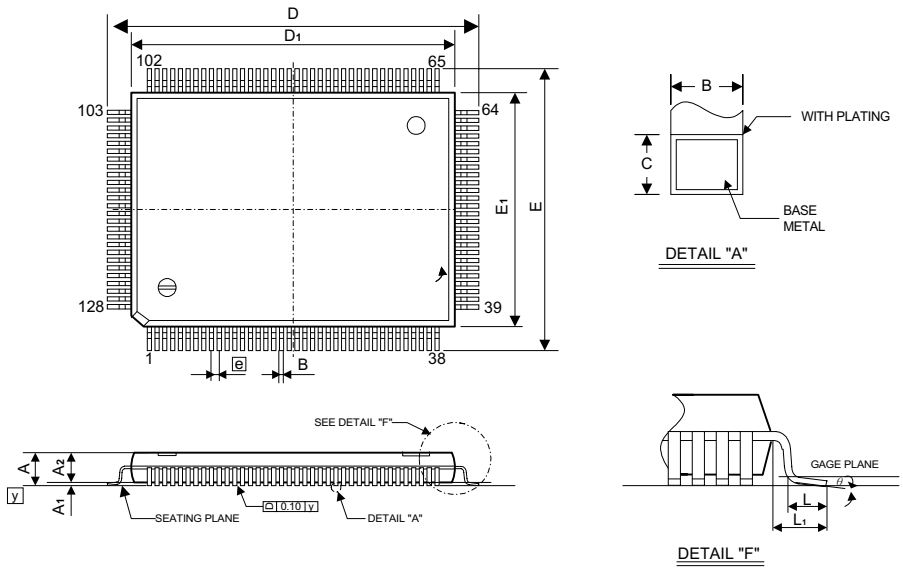


Figure 8-4. Sustained Ultra DMA data-out burst

9. Package Information

PQFP 128L Outline Dimensions **unit: inches/mm**



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.134	-	-	3.40
A1	0.010	-	-	0.25	-	-
A2	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

Notes:

1. Dimensions D_1 and E_1 do not include mold protrusion, but mold mismatch is included.
2. Dimension B does not include dambar protrusion.
3. Controlling dimension: millimeter.

10. Ordering Information

Part No.	Package
IT8212F	128-PQFP