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IT8211F

IDE Controller

Preliminary Specification V0.2

ITE TECH. INC.

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Revision History

Note: Words in bold typeface in the revisions below indicate the changes.

Section	Revision	Page No.
1	• Removed Flash/ROM interface in PCI Interface feature.	1
6	• PCI configure Register 0x2C~0x2F is writable. • ROM address decode enable bit (0x30, bit 0) was revised as read only.	20
	• Added Subsystem ID/System Vendor ID (0x2C~2F) write control bit (0x5C, bit 24).	28

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1. Features

- **IDE Function**
  - Compatible with the ATA/ATAPI-6 specification and supports two IDE channels with 4 drives
  - Supports ANSI ATA proposal PIO Modes 0, 1, 2, 3, 4 with flow control, DMA Modes 0, 1, 2 and Ultra DMA modes 0, 1, 2, 3, 4, 5, 6
  - Programmable active pulses and recovery time for data port access timing
  - 512 bytes FIFO for data transfer per IDE channel
  - Supports Scatter/Gather function for DMA/UDMA transfer
  - Supports pre-fetch and post-write function for PIO mode per IDE channel
- **PCI Interface**
  - Host interface compiles with PCI local bus specification revision 2.2
  - Supports PCI Power Management v1.1 capability
- **Miscellaney**
  - Supports the drivers for Windows 98SE/Me/XP, Windows NT 4.0, Windows 2000, Windows 2003 server and Linux
- **128 Pin QFP**

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2. General Description

The IDE controller, which is compatible with the ATA/ATAPI-6 specification .It supports not only a Scatter/Gather DMA mechanism that complies with the Programming Interface for Bus Master IDE Controller Revision 1.0 but also 2 IDE channels and up to 4 IDE devices.

IT8211F is availabe in the 128-pin QFP package.

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3. System Block Diagram

3.1 Block Diagram

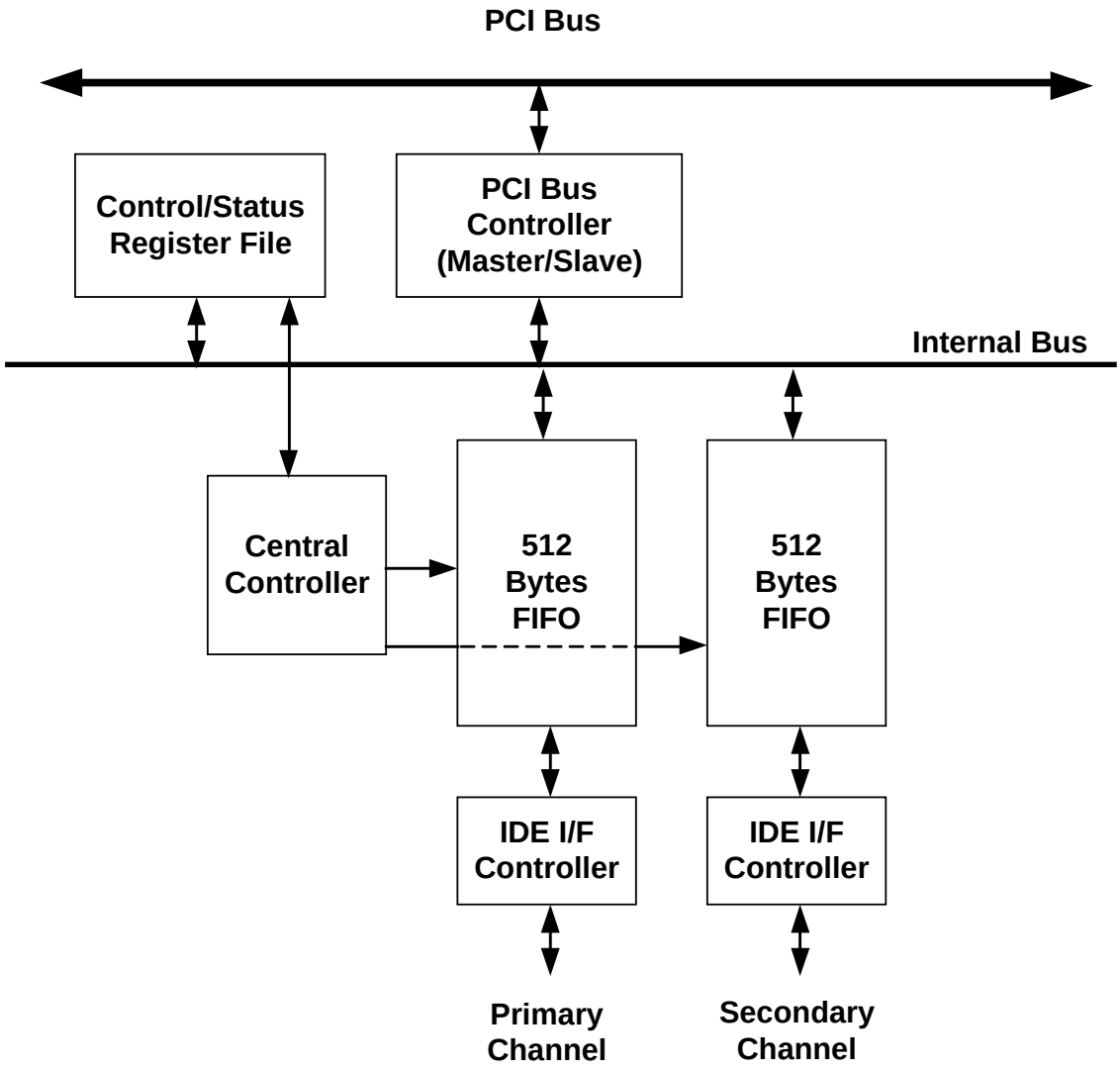

Figure 3-1. Block Diagram

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4. Pin Configuration

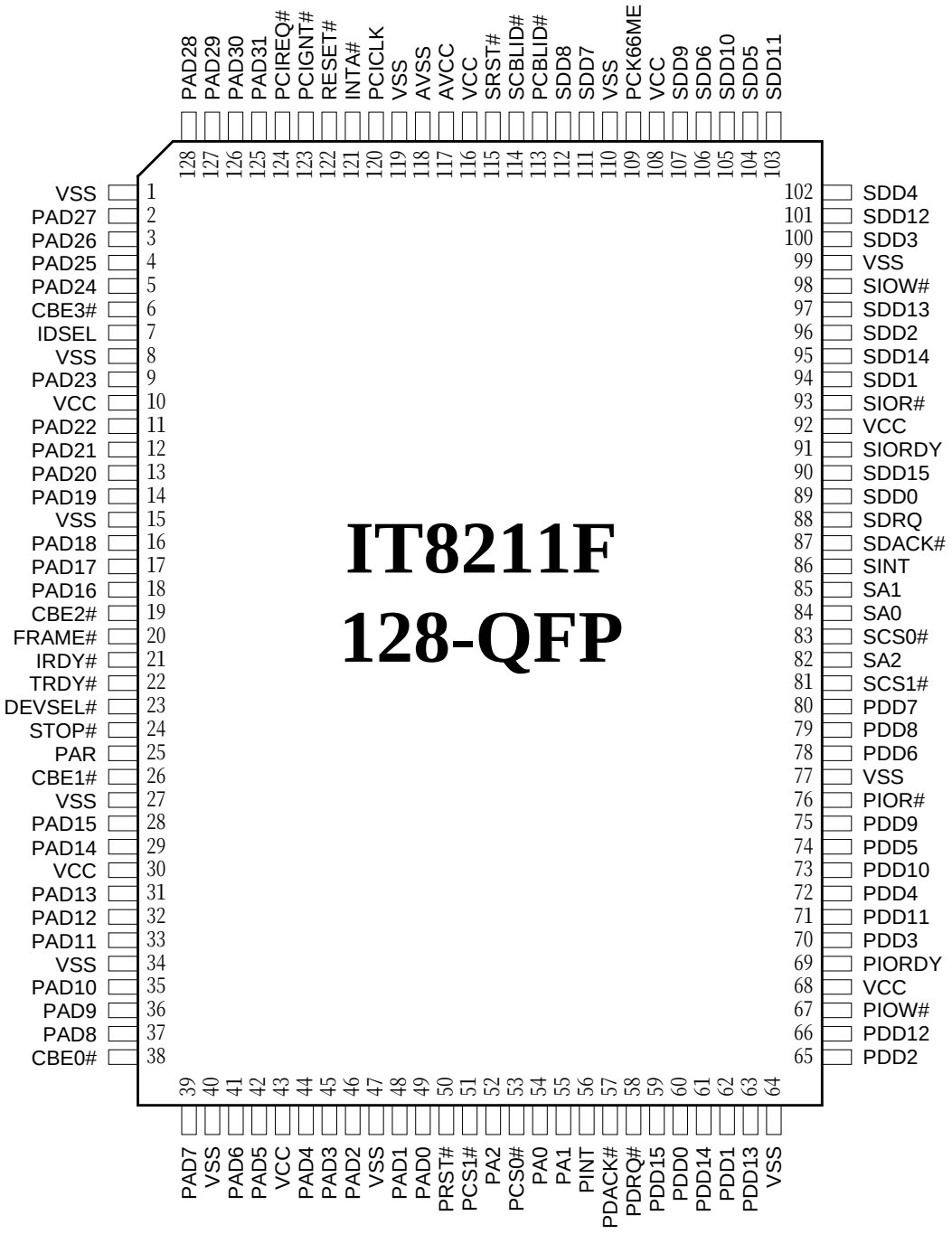

Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VSS	33	PAD11	65	PDD2	97	SDD13
2	PAD27	34	VSS	66	PDD12	98	SIOW#
3	PAD26	35	PAD10	67	PIOW#	99	VSS
4	PAD25	36	PAD9	68	VCC	100	SDD3
5	PAD24	37	PAD8	69	PIORDY	101	SDD12
6	CBE3#	38	CBE0#	70	PDD3	102	SDD4
7	IDSEL	39	PAD7	71	PDD11	103	SDD11
8	VSS	40	VSS	72	PDD4	104	SDD5
9	PAD23	41	PAD6	73	PDD10	105	SDD10
10	VCC	42	PAD5	74	PDD5	106	SDD6
11	PAD22	43	VCC	75	PDD9	107	SDD9
12	PAD21	44	PAD4	76	PIOR#	108	VCC
13	PAD20	45	PAD3	77	VSS	109	PCK66ME
14	PAD19	46	PAD2	78	PDD6	110	VSS
15	VSS	47	VSS	79	PDD8	111	SDD7
16	PAD18	48	PAD1	80	PDD7	112	SDD8
17	PAD17	49	PAD0	81	SCS1#	113	PCBLID#
18	PAD16	50	PRST#	82	SA2	114	SCBLID#
19	CBE2#	51	PCS1#	83	SCS0#	115	SRST#
20	FRAME#	52	PA2	84	SA0	116	VCC
21	IRDY#	53	PCS0#	85	SA1	117	AVCC
22	TRDY#	54	PA0	86	SINT	118	AVSS
23	DEVSEL#	55	PA1	87	SDACK#	119	VSS
24	STOP#	56	PINT	88	SDRQ	120	PCICLK
25	PAR	57	PDACK#	89	SDD0	121	INTA#
26	CBE1#	58	PDRQ#	90	SDD15	122	RESET#
27	VSS	59	PDD15	91	SIORDY	123	PCIGNT#
28	PAD15	60	PDD0	92	VCC	124	PCIREQ#
29	PAD14	61	PDD14	93	SIOR#	125	PAD31
30	VCC	62	PDD1	94	SDD1	126	PAD30
31	PAD13	63	PDD13	95	SDD14	127	PAD29
32	PAD12	64	VSS	96	SDD2	128	PAD28

5. IT8211F Pin Descriptions

Table 5-1. Pin Descriptions of PCI Bus Interface

Signal	Pin(s) No.	Attribute	Description
PCI Bus Interface (3.3V CMOS I/F, 5V tolerant)			
RESET#	122	PI	***System Reset***
PCICLK	120	PI	***PCI Clock***
PAD31-0	125-128, 2-5, 9, 11-14, 16-18, 28, 29, 31-33, 35-37, 39, 41, 42, 44-46, 48, 49	PIO	***PCI Address Data***
CBE3-0#	6, 19, 26, 38	PIO	***PCI Command Byte Enable***
FRAME#	20	PIO	***PCI FRAME# Signal***
DEVSEL#	23	PIO	***PCI DEVSEL# Signal***
IRDY#	21	PIO	***PCI IRDY# Signal***
TRDY#	22	PIO	***PCI TRDY# Signal***
STOP#	24	PIO	***PCI STOP# Signal***
PAR	25	PIO	***PCI Parity***
IDSEL	7	PI	***PCI Initialization Device Select***
INTA#	121	PO	***PCI Interrupt A Output***
PCIREQ#	124	PO	***PCI Request Output***
PCIGNT#	123	PI	***PCI Grant Input***

Table 5-2. Pin Descriptions of IDE Primary Channel Interface

Signal	Pin(s) No.	Attribute	Description
IDE Primary Channel Interface (3.3V CMOS I/F, 5V tolerant)			
PDD15-0	59, 61, 63, 66, 71, 73, 75, 79, 80, 78, 74, 72, 70, 65, 62, 60	IOP	***IDE Primary Channel Data Bus***
PA2-0	52, 55, 54	OP	***IDE Primary Channel Device Address***
PCS1#	51	OP	***IDE Primary Channel Chip Select 1***
PCS0#	53	OP	***IDE Primary Channel Chip Select 0***
PIOW#	67	OP	***IDE Primary Channel IO Write Strobe***
PIOR#	76	OP	***IDE Primary Channel IO Read Strobe***
PDRQ	58	I	***IDE Primary Channel DMA Request***
PDACK#	57	OP	***IDE Primary Channel DMA Acknowledge***
PIORDY	69	I	***IDE Primary Channel IO Channel Ready***
PINT	56	I	***IDE Primary Channel Interrupt***
PCBLID#	113	I	***IDE Primary Channel Cable Assembly Type Identifier***
PRST#	50	OP	***IDE Primary Channel Reset***

Table 5-3. Pin Descriptions of IDE Secondary Channel Interface

Signal	Pin(s) No.	Attribute	Description
IDE Secondary Channel Interface (3.3V CMOS I/F, 5V tolerant)			
SDD15-0	90, 95, 97, 101, 103, 105, 107, 112, 111, 106, 104, 102, 100, 96, 94, 89	IOP	***IDE Secondary Channel Data Bus***
SA2-0	82, 85, 84	OP	***IDE Secondary Channel Device Address***
SCS1-0#	81, 83	OP	***IDE Secondary Channel Chip Select***
SIOW#	98	OP	***IDE Secondary Channel IO Write Strobe***
SIOR#	93	OP	***IDE Secondary Channel IO Read Strobe***
SDRQ	88	I	***IDE Secondary Channel DMA Request***
SDACK#	87	OP	***IDE Secondary Channel DMA Acknowledge***
SIORDY	91	I	***IDE Secondary Channel IO Channel Ready***
SINT	86	I	***IDE Secondary Channel Interrupt***
SCBLID#	114	I	***IDE Secondary Channel Cable Assembly Type Identifier***
SRST#	115	OP	***IDE Secondary Channel Reset***

Table 5-4. Pin Descriptions of Miscellaneous Signal

Signal	Pin(s) No.	Attribute	Description
Miscellaneous Signal (3.3V CMOS I/F)			
PCK66ME	109	ID	***PCI Clock 66 MHz Input Enable*** This signal indicates the PCI clock frequency is 66 MHz or 33 MHz. The signal is only detected when the **RESET#** signal is changed from low to high. If the signal is high, the PCICLK frequency is 66 MHz; otherwise the frequency is 33 MHz.

Table 5-5. Pin Descriptions of Power/Ground Signals

Signal	Pin(s) No.	Attribute	Description
Power Ground Signals			
VSS	1, 8, 15, 27, 34, 40, 47, 64, 77, 99, 110, 119	I	***Ground***
VCC	10, 30, 43, 68, 92, 108, 116	I	***Power Supply of 3.3V***
AVSS	118	I	***Analog Ground for analog PLL***
AVCC	117	I	***Analog VCC for analog PLL***

Notes: IO cell types are described as follows:
I: Input PAD.
ID: Input PAD (integrate a 75k-ohm pull-down resistor).
IK: Schmitt Trigger Input PAD.
PI: PCI Bus Specified Input PAD.
O8: 8mA Output PAD.
OP: Programming Output PAD. The output driving can be programmed to be 2~12mA. The default value is 8mA.
PO: PCI Bus Specified Ouput PAD.
PIO: PCI Bus Specified Input/Output PAD.
IOP: Programming Input/Output PAD. The output driving can be programmed to be 2~12mA. The default value is 8mA.

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6. Functional Description

6.1 Register Description

6.1.1 Register List

6.1.2 List of PCI Configuration Registers

Table 6-1. List of PCI Configuration Registers

31	16	15	00	Index
Device ID (8211h)		Vendor ID (1283h)		00h-03h
Status (0230h)		Command (0000h)		04h-07h
Base Class Code (01h)	Sub-class code (80h)	Program Interface (00h)	Revision ID (11h)	08h-0Bh
Reserved	Header Type (00h)	Latency Timer (20h)	Cache Line Size (00h)	0Ch-0Fh
Primary Channel Command Block Register Base Address (1F1h)				10h-13h
Primary channel Control Block Register Base Address (3F5h)				14h-17h
Secondary Channel Command Block Register Base Address (171h)				18h-1Bh
Secondary Channel Control Block Register Base Address (375h)				1Ch-1Fh
Bus Master Base Address Register (0001h)				20h-23h
Reserved				24h-2Bh
Sub-system Device ID (8211h)		Sub-system Vendor ID (1283h)		2Ch-2Fh
Expansion ROM Base Address (0000h)				30h-33h
Reserved	Reserved	Reserved	Cap. Pointer (80h)	34h-37h
Reserved				38h-3Bh
MAX_LAT (08h)	MIN_GNT (08h)	INTERRUPT PIN (01h)	INTERRUPT LINE (00h)	3Ch-3Fh
IDE Channel Exist Register (01h)	IDE Pad Driving Current Register	IDE I/O Configuration Register		40h-43h
Reserved	PCI Burst Threshold (08h)	Reserved	Primary PCI Burst Threshold (08h)	44h-47h
Reserved	Reserved	PLL2 Control (02h)	PLL1 Control (02h)	48h-4Bh
IDE Bus Skew Control Register (40044004h)				4Ch-4Fh
Reserved		Reserved	PCI Mode (00h)	50h-53h
P-CH Device 1 Ultra DMA Timing (31h)	P-CH Device 0 Ultra DMA Timing (31h)	Reserved	P-CH PIO/MDMA Timing (A3h)	54h-57h
S-CH Device 1 Ultra DMA Timing (31h)	S-CH Device 0 Ultra DMA Timing (31h)	Reserved	S-CH PIO/MDMA Timing (A3h)	58h-5Bh
Test Mode (0000_0000h)				5Ch-5Fh
Reserved				60h-7Fh

List of PCI Configuration Registers [cont'd]

Power Management Capabilities (PMC) (02h)		Next Item Pointer (0h)	Capability ID (01h)	80h-83h
Data (00h)	PMCSR_BSE Bridge Support Extensions (00h)	Power Management Control/Status Register (PMCSR) (0000h)		84h-87h
Reserved				88h-FFh

6.1.3 List of PCI I/O Registers

Table 6-2. List of PCI I/O Register -- Bus Master IDE I/O Registers

Register Name	R/W	Offset (note)	Default	Register Size
Bus Master IDE Command Register for Primary Channel (BMICRP)	R/W	0x0	00h	8 bits
Bus Master IDE Status Register for Primary Channel (BMISRP)	R/WC	0x2	00h	8 bits
Bus Master Descriptor Table Pointer Register for Primary Channel (BMIDTPRP)	R/W	0x4	00000000h	32 bits
Bus Master IDE Command Register for Secondary Channel (BMICRS)	R/W	0x8	00h	8 bits
Bus Master IDE Status Register for Secondary Channel (BMISRS)	R/WC	0xA	00h	8 bits
Bus Master Descriptor Table Pointer Register for Secondary Channel (BMIDTPRS)	R/W	0xC	00000000h	32 bits

Note: The Base Address depends on Bus Master Base Address Register (BMBA).

Table 6-3. IDE Interface and Status Registers from PCI I/O View (PCI IO Space Mapping)

Register Name	R/W	Offset	Default	Register Size
Primary IDE Data Register (VPDR)	R/W	0x0 (Note 1)	0000h	16 bits
Primary IDE Error/Feature Register (VPEFR)	R/W	0x1(Note 1)	00h	8 bits
Primary IDE Sector Count (Ext) Register (VPSCR)	R/W	0x2 (Note 1, 5)	00h	8 bits
Primary IDE Sector Number (Ext) Register (VPSNR)	R/W	0x3 (Note 1, 5)	00h	8 bits
Primary IDE Cylinder Low (Ext) Register (VPCLR)	R/W	0x4 (Note 1, 5)	00h	8 bits
Primary IDE Cylinder High (Ext) Register (VPCHR)	R/W	0x5 (Note1, 5)	00h	8 bits
Primary IDE Device/Head Register (VPHDR)	R/W	0x6 (Note1)	00h	8 bits
Primary IDE Command/Status Register (VPCMR)	R/W	0x7 (Note1)	00h	8 bits
Primary IDE Device Control/Alternate Status Register (VPSTUR)	R/W	0x6 (Note2)	--	8 bits
Secondary IDE Data Register (VSDR)	R/W	0x0 (Note3)	0000h	16 bits
Secondary IDE Error/Feature Register (VSEFR)	R/W	0x1 (Note3)	00h	8 bits
Secondary IDE Sector Count (Ext) Register (VSSCR)	R/W	0x2 (Note 3, 5)	00h	8 bits
Secondary IDE Sector Number (Ext) Register (VSSNR)	R/W	0x3 (Note 3, 5)	00h	8 bits
Secondary IDE Cylinder Low (Ext) Register (VSCLR)	R/W	0x4 (Note 3, 5)	00h	8 bits
Secondary IDE Cylinder High (Ext) Register (VSCHR)	R/W	0x5 (Note 3, 5)	00h	8 bits
Secondary IDE Device/Head Register (VSHDR)	R/W	0x6 (Note 3)	00h	8 bits
Secondary IDE Command /Status Register (VSCMR)	R/W	0x7 (Note 3)	00h	8 bits
Secondary IDE Device Control/Alternate Status Register (VSSTUR)	R/W	0x6 (Note4)	--	8 bits

Definition of R/W Attributes:

RO **READ ONLY**. If a register is read only, writing will have no effect.
R/W **READ/WRITE**. A register with this attribute can be read and written.
R/WC READ/WRITE CLEAR. A register bit with this attribute can be read and written. However, a write of 1 clears the corresponding bit and a write of 0 will have no effect.

Notes:

1. The base address of the Primary IDE Command Registers is defined in PCI Configuration Register 10h~13h (Primary Channel Command Block Register)
2. The base address of the Primary IDE Control Register is defined in PCI Configuration Register 14h~17h (Primary Channel Control Block Register).
3. The base address of the Secondary IDE Command Register is defined in PCI Configuration Register 18h~1Bh (Secondary Channel Command Block Register).
4. The base address of the Secondary IDE Control Register is defined in PCI Configuration Register 1Ch~1Fh (Secondary Channel Control Block Register).
5. When the Primary/Secondary Device Control register bit 7 is set to 1, these registers are regarded as Extended registers, which are used for 48-bit address feature set.

6.1.4 PCI Configuration Registers Definition

6.1.4.1 Vendor ID Register (VIDR) — Offset 0x0

Bit	R/W	Default	Description
15-0	RO	1283h	**Vendor ID (VID)** This is a 16-bit value assigned to the ITE IDE Controller function.

6.1.4.2 Device ID Register (DIDR) — Offset 0x2

Bit	R/W	Default	Description
15-0	RO	8212h	**Device ID (DID)** This is a 16-bit value assigned to the ITE IDE Controller function.

6.1.4.3 Command Register (CMDR) — Offset 0x4

Bit	R/W	Default	Description
15-7	-	0h	**Reserved**
6	RO	0h	**Parity Error Response (PER)** 1: Enabled 0: Disabled
5-3	-	0h	**Reserved**
2	R/W	0h	**DMA Bus Master Enable (DBME)** 1: Enabled 0: Disabled
1	R/W	0h	**Memory Access Enable** 1: Allow the chip to respond to I/O space accesses. 0: Disable I/O space accesses.
0	R/W	0h	**I/O Access Enable (IOAE)** 1: Allow the chip to respond to I/O space accesses. 0: Disable I/O space accesses.

6.1.4.4 Device Status Register (DSTR) — Offset 0x6

Bit	R/W	Default	Description
15-14	-	0h	**Reserved**
13	R/WC	0h	**Master Abort Status (MAST)** This bit is set to high when the IDE Controller acts as a PCI master and has issued a Master-Abort. Write 1 to clear this bit.
12	R/WC	0h	**Received Target Abort (RTA)** This bit is set to high when the IDE controller is a PCI master and the PCI transaction is terminated by receiving a Target-Abort. Write 1 to clear this bit.
11	R/WC	0h	**Signal Target Abort (STA)** This bit is set to high when the IDE controller is a PCI target and has terminated the PCI transaction with a Target-Abort. Writing 1 to this bit to clear it.
10-9	RO	1h	**DEVSEL Timing (DEVT[1:0])** Medium timing is selected for DEVSEL# assertion when the PCI target performs the positive decode.
8	-	0h	**Reserved**
7	RO	0h	**Fast Back-to-Back Capable (FBC)** Always read as 0. Not supported.
6	-	0h	**Reserved**
5	RO	1h	**66 MHz Capable** A “1” indicates that the function supports 66 MHz. A “0” indicates that the function just supports 33 MHz.
4	RO	1h	**Capabilities** This bit indicates whether this function implements a list of extended capabilities such as the PCI power management. When being set, it indicates the presence of capabilities. The value of “0” means that this function does not implement capabilities.
3-0	-	0h	**Reserved**

6.1.4.5 Revision Register (RID) — Offset 0x8

Bit	R/W	Default	Description
7-0	RO	11h	**Revision ID (RID)** The revision number of the IDE controller.

6.1.4.6 Program Interface (PIR) — Offset 0x9

Bit	R/W	Default	Description
7-0	RO	00h	**Program Interface (PI)**

6.1.4.7 Sub-class Code Register (SCC) — Offset 0xA

Bit	R/W	Default	Description
7-0	RO	80h	**Sub-class Code (SCC)**

6.1.4.8 Base Class Code Register (BCC) — Offset 0xB

Bit	R/W	Default	Description
7-0	RO	01h	**Base Class Code (SCC)** 01h for Mass storage device.

6.1.4.9 Cache Line Size Register (CLS) — Offset 0xC

Bit	R/W	Default	Description
7-0	RO	0h	**Cache Line Size (CLS)**

6.1.4.10 Master Latency Timer Register (MLT) — Offset 0xD

Bit	R/W	Default	Description
7-3	R/W	4h	**Master Latency Timer (MLT)** These bits Indicate the PCI Bus master latency timer.
2-0	RO	000b	**Reserved**

6.1.4.11 Header Type Register (HTYPE) — Offset 0xE

Bit	R/W	Default	Description
7-0	RO	00h	**Head Type (HEADT)** These bits Indicate the header type of the device.

6.1.4.12 Built-in Self Test Register (BISTR) — Offset 0xF

Bit	R/W	Default	Description
7	RO	0b	**Built-in Self-Test Capable (BC)** BIST is not supported.
6	RO	0b	**Built-in Self-Test Start (BS)** BIST start bit.
5-4	RO	00b	**Reserved**
3-0	RO	0h	**BIST Completion Code** **Reserved**

6.1.4.13 Primary Channel Command Block Register Base Address (PCMDBA) — Offset 0x10

Bit	R/W	Default	Description
31-3	R/W	3Eh	**Primary Channel Command Block Base Address (PCMDBA[28:0])** The base address of the command block register of the primary channel.
2-1	RO	00	**Reserved**
0	RO	1	**Resource Type (RT)** Hardwired to 1 to indicate that the base address field in this register has been mapped to the I/O space.

This register is only used in the “Native-PCI” mode. The default value is 1F1h.

6.1.4.14 Primary Channel Control Block Base Address (PCNTBA) — Offset 0x14

Bit	R/W	Default	Description
31-2	R/W	FDh	**Primary Channel Control Block Base Address (PCNTLBA [29:0])** The base address of the control block register of the primary channel.
1	RO	0h	**Reserved**
0	RO	1	**Resource Type (RT)** Hardwired to 1 to indicate that the base address field in this register has been mapped to the I/O space.

This register is only used in the “Native-PCI” mode. The default value is 3F5h.

6.1.4.15 Secondary Channel Command Block Base Address (SCMDBA) — Offset 0x18

Bit	R/W	Default	Description
31-3	R/W	2Eh	**Secondary Channel Command Block Base Address (SCMDBA[28:0])** The base address of the command block register of the secondary channel.
2-1	RO	00	**Reserved**
0	RO	1	**Resource Type (RT)** Hardwired to 1 to indicate that the base address field in this register has been mapped to the I/O space.

This register is only used in the “Native-PCI” mode. The default value is 171h.

6.1.4.16 Secondary Channel Control Block Base Address (SCNTBA) — Offset 0x1C

Bit	R/W	Default	Description
31-2	R/W	DDh	**Secondary Channel Control Block Base Address (SCNTLBA[29:0])** The base address of the control block register of the secondary channel.
1	RO	0h	**Reserved**
0	RO	1	**Resource Type (RT)** Hardwired to 1 to indicate that the base address field in this register has been mapped to the I/O space.

This register is only used in the “Native-PCI” mode. The default value is 375h.

6.1.4.17 Bus Master Base Address Register (BMBA) — Offset 0x20

Bit	R/W	Default	Description
31-4	R/W	00h	**Bus Master Base Address (BMBA [27:0])** These bits provide the base address for the bus master interface register.
3-1	RO	000	**Reserved**
0	RO	1	**Resource Type (RT)** Hardwired to 1 to indicate that the base address field in this register has been mapped to the I/O space.

6.1.4.18 Sub-system Vendor ID Register (SVID) — Offset 0x2C

Bit	R/W	Default	Description
15-0	R/W	0h	**Sub-system Vendor ID (SVID [15:0]).** This bit is writable when test register (offset 0x5C) bit 24 is set to “1”.

6.1.4.19 Sub-system Device ID Register (SID) — Offset 0x2E

Bit	R/W	Default	Description
15-0	R/W	0h	**Sub-system Device ID (SVID [15:0]).** This bit is writable when test register (offset 0x5C) bit 24 is set to “1”.

6.1.4.20 Expansion ROM Base Address Register (ROMBAR) — Offset 0x30

Bit	R/W	Default	Description
31-17	R/W	0h	**Expansion ROM Base Address**
16-1	RO	0h	**Reserved** Read always as 0
0	RO	0h	**ROM Address Decode Enable** 1: ROM address enables to decode. 0: ROM address disables to decode.

6.1.4.21 Capabilities Pointer Register (CPR) — Offset 0x34

Bit	R/W	Default	Description
7-0	RO	80h	**Capabilities Pointer (Cap_ptr)** The Cap_ptr provides an offset into the function’s PCI Configuration Space for the location of the first item in the Capabilities linked list. The Cap_ptr offset is Dword aligned so the two least significant bits are always “0”.

6.1.4.22 Interrupt Line Register (ILR) — Offset 0x3C

Bit	R/W	Default	Description
7-0	R/W	00h	**Interrupt Line (IL)** This is an 8-bit register used to communicate the interrupt line routing information. The value in the register tells which input of the system interrupt controller the device’s interrupt pin is connected to.

6.1.4.23 Interrupt Pin Register (IPR) — Offset 0x3D

Bit	R/W	Default	Description
7-0	RO	01h	**Interrupt Pin (IP)** The register tells which interrupt pin the device uses. The device only uses the INTA#, so the value is 01h.

6.1.4.24 MIN_GNT Register (MGR) — Offset 0x3E

Bit	R/W	Default	Description
7-0	RO	08h	**MIN_GNT (MG)** The device has requirements for the setting of Latency Timers.

6.1.4.25 MAX_LAT Register (MLR) — Offset 0x3F

Bit	R/W	Default	Description
7-0	RO	08h	**MAX_LAT (ML)** The device has requirements for the setting of Latency Timers.

6.1.4.26 IDE I/O Configuration Register (IOCFG) — Offset 0x40

Bit	R/W	Default	Description
15	R/W	0h	**IDE Decode Enable for Primary Channel (PDE)** 1: Enabled. 0: Disabled.
14	RO	0b	**Reserved**
13	R/W	0h	**IDE Decode Enable for Secondary Channel (SDE)** 1: Enabled. 0: Disabled.
12-8	RO	00h	**Reserved**
7	R/W	0h	**Secondary Drive 1 Channel Cable Report (S1CR)** This bit is written by software. 1: 80 conductor cables are present. 0: 40 conductor cables are present.
6	R/W	0h	**Secondary Drive 0 Channel Cable Report (S0CR)** This bit is written by software. 1: 80 conductor cables are present. 0: 40 conductor cables are present.
5	R/W	0h	**Primary Drive 1 Channel Cable Report (P1CR)** This bit is written by software. 1: 80 conductor cables are present. 0: 40 conductor cables are present.
4	R/W	0h	**Primary drive 0 Channel Cable Report (P0CR)** This bit is written by software. 1: 80 conductor cables are present. 0: 40 conductor cables are present.
3	RO	-	**Secondary Channel SCBLID# Signal (SCCS)** CBLID# signal in the cable of the secondary channel.
2	RO	-	**Primary Channel PCBLID# Signal (PCCS)** PCBLID# signal in the cable of the primary channel.
1	R/W	0b	**Secondary Channel IORDY Sample Enable** 1: Enable IORDY sample 0: Disable IORDY sample
0	R/W	0b	**Primary Channel IORDY Sample Enable** 1: Enable IORDY sample 0: Disable IORDY sample

6.1.4.27 IDE Driving Current Register (DCR) — Offset 0x42

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5-3	R/W	3h	**Secondary Channel PAD Current Control (SPC)** When SPC[2:0]=000b, the driving current is 2 mA. When SPC[2:0]=001b, the driving current is 4 mA. When SPC[2:0]=010b, the driving current is 6 mA. When SPC[2:0]=011b, the driving current is 8 mA, When SPC[2:0]=100b, the driving current is 6 mA for SDD15-0; 2 mA for others. When SPC[2:0]=101b, the driving current is 8 mA for SDD15-0; 4 mA for others. When SPC[2:0]=110b, the driving current is 10 mA for SDD15-0; 6 mA for others. When SPC[2:0]=111b, the driving current is 12 mA for SDD15-0; 8 mA for others.
2-0	R/W	3h	**Primary Channel PAD Current Control (PPC)** When PPC[2:0]=000b, the driving current is 2 mA. When PPC[2:0]=001b, the driving current is 4 mA. When PPC[2:0]=010b, the driving current is 6 mA. When PPC[2:0]=011b, the driving current is 8 mA, When PPC[2:0]=100b, the driving current is 6 mA for SDD15-0; 2 mA for others. When PPC[2:0]=101b, the driving current is 8 mA for SDD15-0; 4 mA for others. When PPC[2:0]=110b, the driving current is 10 mA for SDD15-0; 6 mA for others. When PPC[2:0]=111b, the driving current is 12 mA for SDD15-0; 8 mA for others.

6.1.4.28 IDE Virtual Channel Exist Register (IDEENR) — Offset 0x43

Bit	R/W	Default	Description
7-4	RO	0h	**Reserved**
3	R/W	0b	**IDE Virtual Secondary Slave Exist** 0: Not Exist 1: Exist
2	R/W	0b	**IDE Virtual Secondary Master Exist** 0: Not Exist 1: Exist
1	R/W	0b	**IDE Virtual Primary Slave Exist** 0: Not Exist 1: Exist
0	R/W	1b	**IDE Virtual Primary Master Exist** 0: Not Exist 1: Exist **Note:** In order to make IDE Vender Specific Command access successfully, this bit must be set to 1 even though this device does not exist. After the vender command is finished, this bit must be cleared to 0 if the device does not exist.

6.1.4.29 PCI Burst Threshold Register (PCIBRSTR) — Offset 0x44

Bit	R/W	Default	Description
31-24	-	0h	**Reserved**
23-16	R/W	08h	**PCI Burst Threshold for Secondary Channel (SPCIBTHR)** This register decides that the data size (Double Word Unit) must be satisfied before the PCI master can perform the burst cycle.
15-8	-	0h	**Reserved**
7-0	R/W	08h	**PCI Burst Threshold for Primary Channel (PPCIBTHR)** See bits 23-16.

6.1.4.30 PLL1 Control Register (PLL1CR) — Offset 0x48

Bit	R/W	Default	Description
7-2	RO	00h	**Reserved**
1	R/W	1b	**PLL1 Power Down (PLL1PD)** This bit is used to power down the PLL1 (66MHz). When this bit is set, the PLL operates normally. When this bit is cleared, the PLL is in the power down state.
0	R/W	0b	**PLL1 Bypass Enable (PLL1BE)** This bit is used to bypass the clock of the PLL1. When this bit is set, the PLL is bypassed. When this bit is cleared, the PLL is in the normal mode.

6.1.4.31 PLL2 Control Register (PLL2CR) — Offset 0x49

Bit	R/W	Default	Description
7-2	RO	00h	**Reserved**
1	R/W	1b	**PLL2 Power Down (PLL2PD)** This bit is used to power down the PLL2 (50MHz). When this bit is set, the PLL operates normally. When this bit is cleared, the PLL is in the power down state.
0	R/W	0b	**PLL2 Bypass Enable (PLL2BE)** This bit is used to bypass the clock of the PLL2. When this bit is set, the PLL is bypassed. When this bit is cleared, the PLL is in the normal mode.

6.1.4.32 IDE Bus Skew Control Register (IDEBSCR) — Offset 0x4C

Bit	R/W	Default	Description
31-28	R/W	4h	**Secondary Channel Device Data Input Delay (PDDID)** These bits are used to control the DD input signal delay time.
27-24	R/W	0h	**Secondary Channel Device Strobe Delay (PDSBD)** These bits are used to control the DSTROBE (DIORDY) input signal delay time.
23-20	R/W	0h	**Secondary Channel Host Data Out Delay (PHDOD)** These bits are used to control the DD output signal delay time.
19-16	R/W	4h	**Secondary Channel Host Strobe Delay (PHSBD)** These bits are used to control the HSTROBE (DIOR) signal delay time.
15-12	R/W	4h	**Primary Channel Device Data Input Delay (PDDID)** These bits are used to control the DD input signal delay time.
11-8	R/W	0h	**Primary Channel Device Strobe Delay (PDSBD)** These bits are used to control the DSTROBE (DIORDY) input signal delay time.
7-4	R/W	0h	**Primary Channel Host Data Out Delay (PHDOD)** These bits are used to control the DD output signal delay time.
3-0	R/W	4h	**Primary Channel Host Strobe Delay (PHSBD)** These bits are used to control the HSTROBE (DIOR) signal delay time.

6.1.4.33 PCI Mode Control Register (PCICR) — Offset 0x50

Bit	R/W	Default	Description
7	R/W	0b	**PCI Mode Reset (PCIMR)** This bit is used to reset the related PCI circuit. When it is set, the related PCI circuit will be reset. When it is cleared, the related PCI circuit will be in the normal mode.
6	R/W	0b	**Secondary Channel Device 1 Transfer Mode (SCHD1TM)** This bit is used to determine the transfer mode of IDE Bus. 1 : MultiWord DMA mode 0 : Ultra DMA mode
5	R/W	0b	**Secondary Channel Device 0 Transfer Mode (SCHD0TM)** This bit is used to determine the transfer mode of IDE Bus. 1 : MultiWord DMA mode 0 : Ultra DMA mode
4	R/W	0b	**Primary Channel Device 1 Transfer Mode (PCHD1TM)** This bit is used to determine the transfer mode of IDE Bus. 1 : MultiWord DMA mode 0 : Ultra DMA mode
3	R/W	0b	**Primary Channel Device 0 Transfer Mode (PCHD0TM)** This bit is used to determine the transfer mode of IDE Bus. 1 : MultiWord DMA mode 0 : Ultra DMA mode
2	R/W	0b	**Secondary Channel IDE Clock Frequency Select (SCHCLK)** This bit is used to select the IDE Clock Frequency. 1 : 50 MHz, 0 : 66 MHz
1	R/W	0b	**Primary Channel IDE Clock Frequency Select (PCHCLK)** This bit is used to select the IDE Clock Frequency. 1 : 50 MHz, 0 : 66 MHz
0	R/W	1b	**PCI Mode Select (PCIMS)** This bit must be set to “0” before IDE operation.

6.1.4.34 PCI Mode Primary PIO and DMA Timing Registers (PMPIOTR) — Offset 0x54

Bit	R/W	Default	Description
7-4	R/W	Ah	**IDE PIO and DMA Transfer Active Time** These bits define T2 or Td timing. The unit is two-clock period of the selected clock.
3-0	R/W	3h	**IDE PIO and DMA Transfer Recovery Time** These bits define the T2I or Tk timing. The unit is two-clock period of the selected clock.

Note: See more details in IDE PIO and DMA Timing Registers.

6.1.4.35 PCI Mode Primary Device 0 Ultra DMA Timing Registers (PMPD0UDTR) — Offset 0x56

Bit	R/W	Default	Description
7	R/W	0b	**Ultra DMA Mode 5, 6 Select** This bit defines the mode of Ultra DMA Mode. When this bit is set, the Ultra DMA Mode is mode 5 or 6. When this bit is cleared, the Ultra DMA Mode is mode 0,1,2,3 or 4.
6-4	R/W	3h	**Ultra DMA Data Setup Time** These bits define the Ultra DMA Tdvs timing. The unit is one-clock period of the selected clock frequency for mode 0,1,2,3 and 4. The unit is half a clock period of the selected clock frequency for mode 5 and 6.
3	R/W	0b	**Reserved**
2-0	R/W	1h	**Ultra DMA Data Hold Time** These bits define the Ultra DMA Tdvh timing. The unit is one-clock period of the selected clock frequency for mode 0,1,2,3 and 4. The unit is half a clock period of the selected clock frequency for mode 5 and 6.

Note: See more details in IDE Ultra DMA Timing Registers.

6.1.4.36 PCI Mode Primary Device 1 Ultra DMA Timing Registers (PMPD1UDTR) — Offset 0x57

Bit	R/W	Default	Description
7	R/W	0b	**Ultra DMA Mode 5, 6 Select** This bit defines the mode of Ultra DMA Mode. When this bit is set, the Ultra DMA Mode is mode 5 or 6. When this bit is cleared, the Ultra DMA Mode is mode 0,1,2,3 or 4.
6-4	R/W	3h	**Ultra DMA Data Setup Time** These bits define the Ultra DMA Tdvs timing. The unit is one-clock period of the selected clock frequency for mode 0,1,2,3 and 4. The unit is half a clock period of the selected clock frequency for mode 5 and 6.
3	R/W	0b	**Reserved**
2-0	R/W	1h	**Ultra DMA Data Hold Time** These bits define the Ultra DMA Tdvh timing. The unit is one-clock period of the selected clock frequency for mode 0,1,2,3 and 4. The unit is half a clock period of the selected clock frequency for mode 5 and 6.

Note: See more details in IDE Ultra DMA Timing Registers.

6.1.4.37 PCI Mode Secondary PIO and DMA Timing Registers (PMSPIOTR) — Offset 0x58

Bit	R/W	Default	Description
7-4	R/W	Ah	**IDE PIO and DMA Transfer Active Time** These bits define the T2 or Td timing. The unit is two-clock period of the selected clock.
3-0	R/W	3h	**IDE PIO and DMA Transfer Recovery Time** These bits define the T2I or Tk timing. The unit is two-clock period of the selected clock.

Note: See more details in IDE PIO and DMA Timing Registers

6.1.4.38 PCI Mode Secondary Device 0 Ultra DMA Timing Registers (PMSD0UDTR) — Offset 0x5A

Bit	R/W	Default	Description
7	R/W	0b	**Ultra DMA Mode 5, 6 Select** This bit defines the mode of Ultra DMA Mode. When this bit is set, the Ultra DMA Mode is mode 5 or 6. When this bit is cleared, the Ultra DMA Mode is mode 0,1,2,3 or 4.
6-4	R/W	3h	**Ultra DMA Data Setup Time** These bits define the Ultra DMA Tdvs timing. The unit is one-clock period of the selected clock frequency for mode 0,1,2,3 and 4. The unit is half a clock period of the selected clock frequency for mode 5 and 6.
3	R/W	0b	**Reserved**
2-0	R/W	1h	**Ultra DMA Data Hold Time** These bits define the Ultra DMA Tdvh timing. The unit is one-clock period of the selected clock frequency for mode 0,1,2,3 and 4. The unit is half a clock period of the selected clock frequency for mode 5 and 6.

Note: See more details in IDE Ultra DMA Timing Registers.

6.1.4.39 PCI Mode Secondary Device 1 Ultra DMA Timing Registers (PMSD1UDTR) — Offset 0x5B

Bit	R/W	Default	Description
7	R/W	0b	**Ultra DMA Mode 5, 6 Select** This bit defines the mode of Ultra DMA Mode. When this bit is set, the Ultra DMA Mode is mode 5 or 6. When this bit is cleared, the Ultra DMA Mode is mode 0,1,2,3 or 4.
6-4	R/W	3h	**Ultra DMA Data Setup Time** These bits define the Ultra DMA Tdvs timing. The unit is one-clock period of the selected clock frequency for mode 0,1,2,3, and 4. The unit is half a clock period of the selected clock frequency for mode 5 and 6.
3	R/W	0b	**Reserved**
2-0	R/W	1h	**Ultra DMA Data Hold Time** These bits define the Ultra DMA Tdvh timing. The unit is one-clock period of the selected clock frequency for mode 0,1,2,3 and 4. The unit is half a clock period of the selected clock frequency for mode 5 and 6.

Note: See more details in IDE Ultra DMA Timing Registers.

6.1.4.40 Test Mode Register (TMR) — Offset 0x5C

Bit	R/W	Default	Description
31-25	-	0h	**Reserved**
24	R/W	0b	**Subsystem ID/System Vendor ID Write Enable** When this bit is set to “1”, Subsystem ID and subsystem vendor ID registers are writable, otherwise, they are read only
23-2	RO	0h	**Reserved**
1	R/W	0b	**PLL Output Test** When the bit is enabled, PRST# : 66 MHz, SRST# : 50 MHz.
0	-	0b	**Reserved**

6.1.4.41 Capability Identifier Register (CAPIDR) — Offset 0x80

Bit	R/W	Default	Description
7-0	RO	01h	**Capability Identifier (CAP_ID)** When this register is set to 01h, it identifies the linked capability list as the PCI Power Management Capability.

6.1.4.42 Next Item Pointer Register (NEXT_PTR) — Offset 0x81

Bit	R/W	Default	Description
7-0	RO	00h	**Next Item Pointer** This field provides an offset into the function's PCI Configuration Space pointing to the location of the next item on the function's Capability list. If there are no additional items on the Capability list, the register is set to 00h.

6.1.4.43 Power Management Capabilities Register (PMCR) — Offset 0x82

Bit	R/W	Default	Description
15-11	RO	0h	**PME_Support** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for every bit indicates that the function is not capable of asserting the PME# signal in the power state. bit(11) xxxx1b – PME# can be asserted from **D0.** bit(12) xxx1xb – PME# can be asserted from **D1.** bit(13) xx1xxb – PME# can be asserted from **D2.** bit(14) x1xxxb – PME# can be asserted from **$D3_{hot}$.** bit(15) 1xxxxb – PME# can be asserted from **$D3_{cold}$.**
10	RO	0h	**D2_Support** If this bit is a "1", this function supports the **D2** Power Management State. Not support
9	RO	0h	**D1_Support** If this bit is a "1", this function supports the **D1** Power Management State. Not supported.
8-6	RO	0h	**Reserved**
5	RO	0h	**Device Specific Initialization (DSI)** This bit indicates whether a special function initialization is required (beyond the PCI standard configuration header) before the generic class device driver is able to use it. A "1" indicates that the function requires a device specific initialization sequence following the transition to the D0 which is at the uninitialized state.
4	RO	0h	**Reserved**
3	RO	0h	**PME Clock** When this bit is a "1", it indicates that the function relies on the presence of the PCI clock for PME# operation. When this bit is a "0", it indicates that no PCI clock is required for the function to be generated. The function does not support PME# generation in any state. It must return "0" for this field.
2-0	RO	010b	**Version** A value of 010b indicates that this function complies with PCI Power Management Interface Specification Revision 1.1.

6.1.4.44 Power Management Control/Status Register (PMCSR) — Offset 0x84

Bit	R/W	Default	Description
15	RO	0h	**PME_Status** Do not support PME# generation from **D3**$_{cold}$.
14-13	RO	0h	**Data_Scale** Do not implement this field.
12-9	RO	0h	**Data_Select** Do not implement this field.
8	RO	0h	**PME_en** Do not support PME# generation from any D-state.
7-2	RO	0h	**Reserved**
1-0	R/W	0h	**Power State** This 2-bit field is used to determine the current power state of the function and set the function in a new power state. The definition of the field value is given below: 00b – **D0** 01b – **D1** 10b – **D2** 11b – **D3**$_{hot}$ If software attempts to write an unsupported and optional state to this field, the writing operation must be completed normally on the bus; otherwise, data are discarded and the state won't be changed. So, when a "01b" or "10b" is written to this register, data are discarded and the state won't be changed.

6.1.4.45 PMCSR PCI to PCI Bridge Support Extensions — Offset 0x86

Bit	R/W	Default	Description
7	RO	0h	**BPCC_En (Bus Power/Clock Control Enable)** A "1" indicates that the bus power/clock control mechanism defined in PCI Bus Power Management Interface Specification Revision 1.1 Section 4.7.1 is enabled. Otherwise, it is disabled. When it is disabled, the bridge's PMCSR Power State field cannot be used by software of the system to control the power or clock of the bridge's secondary bus.
6	RO	0h	**B2_B3# (B2/B3 Support for D3**$_{hot}$**)** The state of this bit determines the action that is to occur as a direct result of programming the function to D3$_{hot}$. A "1" indicates that when the bridge function is programmed to **D3**$_{hot}$, its secondary bus' PCI clock will be stopped (**B2**). A "0" indicates that when the bridge function is programmed to **D3**$_{hot}$, its secondary bus will have its power removed. This bit is only meaningful if bit 7 (BPCC_En) is a "1".
5-0	RO	0h	**Reserved**

6.1.4.46 Data Register (DR) — Offset 0x87

Bit	R/W	Default	Description
7-0	RO	0h	**Data** This register is used to report the state's dependent data requested by Data_Select field. The value of this register is scaled by the Data_Scale field.

6.1.5 PCI I/O Register -- Bus Master IDE I/O Registers

6.1.5.1 Bus Master IDE Command Registers (BMICR) — Offset 0x0 (Primary) / 08 (Secondary)

Bit	R/W	Default	Description
7-4	RO	0h	**Reserved** These bits must return 0h while being read.
3	R/W	0h	**Write or Read Control (WRC)** This bit sets the direction of the bus master transfer. 1: Bus master writes are performed. 0: Bus master reads are performed. This bit must not be changed when the bus master function is active.
2-1	RO	0h	**Reserved**
0	R/W	0h	**Start/Stop Bus Master (SBM)** Writing a "1" to this bit enables the bus master operation of the controller. A bus master operation begins when the value of this bit has changed from a "0" to a "1". The controller transfers data between the IDE device and the memory only when this bit is set. Writing a "0" to this bit can halt the master operation and all the state information is lost. The master mode operation cannot be stopped and resumed. If this bit is reset while a bus master operation is still active (BMA=1) and the drive has not finished its data transfer (INT=0) yet, the bus master command is aborted, and data transferred from the drive may be discarded before being written to the system memory. This bit shall be reset after the data transfer is completed, as indicated by either BMA being reset or INT being set, or both.

6.1.6 IDE Interface and Status Registers

The following registers are used to control the IDE channel action.

1. The base address of primary IDE Command Registers (offset 0x0 ~0x7) is defined in PCI Configuration Register 10h~13h (Primary Channel Command Block Register)
2. The base address of primary IDE Alternate Status/Device Control Register is defined in PCI Configuration Register 14h~17h (Primary Channel Control Block Register)
3. The base address of the secondary IDE Command Registers (offset 0x0~0x7) is defined in PCI Configuration Register 18h~1Bh (Secondary Channel Command Block Register)
4. The base address of Secondary IDE Alternate Status/Device Control Register is defined in PCI Configuration Register 1Ch~1Fh (Secondary Channel Control Block Register)
5. For 6.1.4.3 ~ 6.1.4.6 registers, when IDE Device Control Register bit 7 (HOB) is set to 1, these registers are extended for 48-bit address feature setting for ATA-133 spec. The PCI shares the same IO space when HOB is 1 or 0. Please refer to the ATA specification for the detailed register definition.

6.1.6.1 Primary/Secondary IDE Data Registers — PCI IO Space: Offset 0x0

Bit	R/W	Default	Description
15-0	R/W	0	**IDE Data Register** This register is for PIO data access only.

6.1.6.2 Primary/Secondary IDE Error/Feature Registers — PCI IO Space: Offset 0x1

This is an IDE Error Register when it is read. It is an IDE Feature Register when being written from the PCI access.

Bit	R/W	Default	Description
7-0	R/W	0	**IDE Error/Feature Register** When this register is read, it is an IDE Error Register. When this register is written, it is an IDE Feature Register.

6.1.6.3 Primary/Secondary IDE Sector Count (Ext.) Registers — PCI IO Space: Offset 0x2

Bit	R/W	Default	Description
7-0	R/W	0	**IDE Sector Count Register** The content of this register becomes a command parameter when the Command register is written. The address is the same as Sector Count register in PCI space. If Device Control Register bit 7 HOB is set to 1, this register is Sector Count Ext. Register.

6.1.6.4 Primary/Secondary IDE Sector Number (Ext.) Registers — PCI IO Space: Offset 0x3

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Sector Number Register** The content of this register becomes a command parameter when the Command register is written. The address is the same as Sector Count register in PCI space. If Device Control Register bit 7 HOB is set to 1, this register is Sector Number Ext. Register.

6.1.6.5 Primary/Secondary IDE Cylinder Low (Ext.) Registers — PCI IO Space: Offset 0x4

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Cylinder Low Register** The content of this register becomes a command parameter when the Command register is written. The address is the same as Sector Count register in PCI space. If Device Control Register bit 7 HOB is set to 1, this register is Cylinder Low Ext. Register.

6.1.6.6 Primary/Secondary IDE Cylinder High (Ext.) Registers — PCI IO Space: Offset 0x5

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Cylinder High Register** The content of this register becomes a command parameter when the Command register is written. The address is the same as Sector Count register in PCI space. If Device Control Register bit 7 HOB is set to 1, this register is Cylinder High Ext. Register.

6.1.6.7 Primary/Secondary IDE Device/Head Registers — PCI IO Space: Offset 0x6

Bit	R/W	Default	Description
7-0	R/W	0h	**IDE Device/Head Register** Bit 4 DEV in this register selects the device. Other bits in this register are command dependent.

6.1.6.8 Primary/Secondary IDE Status/Command Registers — PCI IO Space: Offset 0x7

This is an IDE Status Register when it is read. It is an IDE Command Register when being written from PCI access.

Table 6-4. Status Register

Bit	R/W	Default	Description
7	RO	0h	**Busy** When this bit is set to 1, it indicates that the device is busy.
6	RO	0h	**Device Ready** When this bit is set to 1, it indicates that the device is ready and can accept and attempt to execute all implemented commands.
5-4	-	0h	**Reserved**
3	RO	0h	**Data Request** When this bit is set to 1, it indicates that the device is ready to transfer a word of data between the host and device.
2-1	-	0h	**Reserved**
0	RO	0h	**Error** When this bit is set to 1, it indicates that an error occurred during the execution of the previous command.

Table 6-5. Command Register

Bit	R/W	Default	Description
7-0	WO	-	**Command Code** This register contains the command code being sent to the device.

6.1.6.9 Primary/Secondary IDE Alternate Status/Device Control Registers — PCI IO Space: Offset 0x6

The base address of the Primary IDE Alternate Status/Device Control Register is defined in PCI Configuration Register 14h~17h (Primary Channel Control Block Register) and the base address of the Secondary IDE Alternate Status/Device Control Register is defined in PCI Configuration Register 1Ch~1Fh (Secondary Channel Control Block Register). When this register is read, it is Alternate Status Register, which contains the same information as the IDE Status Register. When this register is written, it is Device Control Register.

Bit	R/W	Default	Description
7	WO	-	**High Order Byte (HOB)** This bit is defined by the 48-bit address feature set. If this bit is on, extend register can be accessed.
6-3	-	-	**Reserved**
2	WO	-	**Software Reset (SRST)** This is a software reset bit. When it is written by 1, a software reset disk interrupt will occur.
1	WO	-	**nIEN** This is an enabled bit for the device assertion of interrupt to the host. When it is cleared to 0 and the device is selected, the device interrupt shall be enabled from itself. When it is set to 1 or the device is not selected, the device's interrupt is disabled by itself.
0	R/W	0	**Reserved** It must be 0.

7. DC Characteristics

(VCC3, AVCC =3.3V±0.3V, Ta=0°C to 70°C)

Absolute Maximum Ratings

Power Supply (V_{CC}) ..... -0.3V to 3.6V

Input Voltage ..... -0.3V to VCC + 0.3V

Output Voltage ..... -0.3V to VCC + 0.3V

Storage Temperature ..... -55°C to 150°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Operation Condition Vcc=3.0V~3.6V, Tj=0°C~115°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	CMOS	-	-	0.3*Vcc	V
V_{IH}	Input High Voltage	CMOS	0.7*Vcc	-	-	V
Vt-	Schmitt trigger negative going threshold voltage	CMOS	-	1.20	-	V
Vt+	Schmitt trigger positive going threshold voltage	CMOS	-	2.10	-	V
V_{OL}	Output Low Voltage	I_{OL}=2mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}=2mA	2.4	-	-	V
R_I	Input Pull-up resistance	V_{IL}=0V or V_{IH}=Vcc	-	75	-	KΩ
I_{IL}	Input Leakage current	no pull-up	-1	-	1	uA
I_{OZ}	Tri-state leakage current		-1	-	1	mA
C_{IN}	Input capacity		-	10	-	pF
C_{OUT}	Output capacity		-	10	-	pF
C_{BID}	Bi-directional buffer capacity		-	10	-	pF

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8. AC Characteristics

Table 8-1. Register transfer to/from device

Symbol	Parameter	Mode4	Mode0	Unit
t_0	Cycle time	120	600	ns
t_1	Address valid to IOR#/IOW# setup	30	90	ns
t_2	IOR#/IOW# pulse width	90	300	ns
t_{2i}	IOR#/IOW# recovery time	30	300	ns
t_3	IOW# data setup	30	270	ns
t_4	IOW# data hold	20	270	ns
T_5	IOR# data setup	20	50	ns
T_6	IOR# data hold	5	5	ns
T_9	IOR#/IOW# to address valid hold	15	30	ns

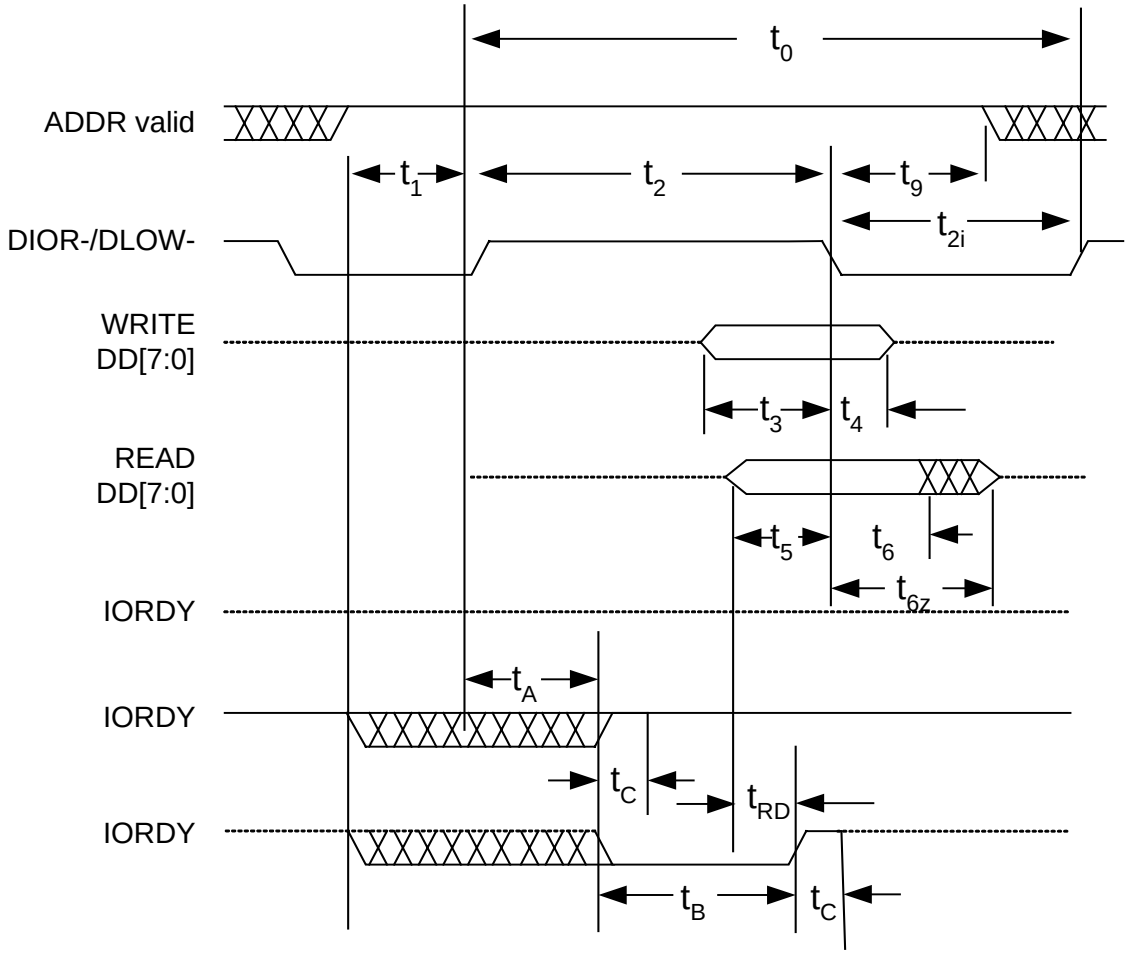


Figure 8-1.Register transfer to/from device

Table 8-2. Ultra DMA data burst timing requirements

Symbol	Parameter	Min	Max	Unit
$t_{2CYCTYP}$	Typical sustained average two cycle time	30_6-240_0	-	ns
t_{CYC}	Cycle time allowing for asymmetry and clock variations	13_6-112_0	-	ns
t_{UI}	Unlimited interlock time	0	-	ns
t_{ACK}	Setup and hold times for DACK#	30	-	ns
t_{ENV}	Envelope time	30	40	ns
t_{DVSIC}	Sender IC data valid setup time	6_6-100_0	-	ns
t_{DVHIC}	Sender IC data valid hold time	6_6-10_0	-	ns
t_{DSIC}	Recipient IC data valid setup time	2	-	ns
t_{DHIC}	Recipient IC data valid hold time	2	-	ns

Note: XX_6-XX_0 where the $_6$ indicates mode 6 and $_0$ indicates mode 0.

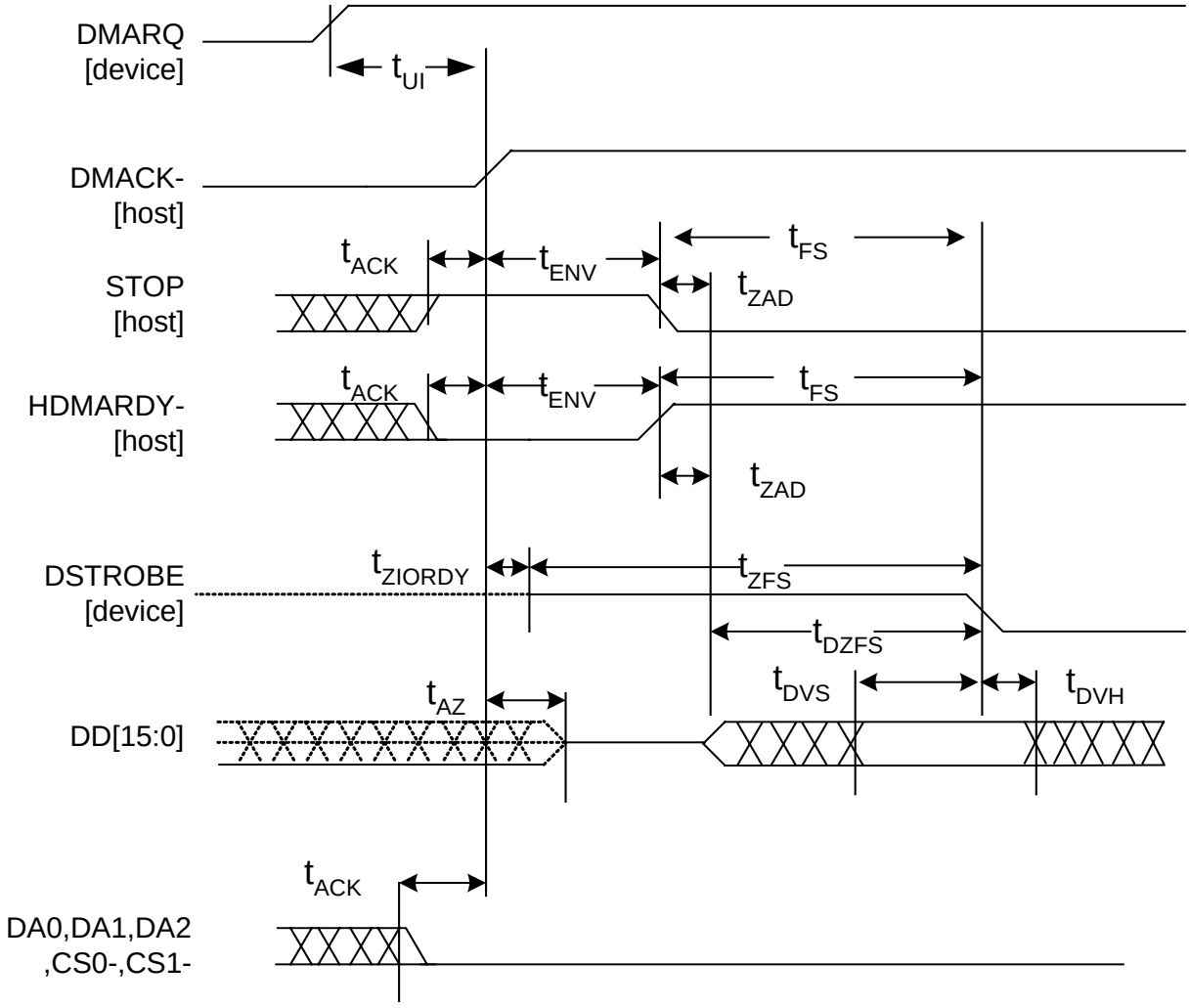


Figure 8-2.Initiating an Ultra DMA data-in burst

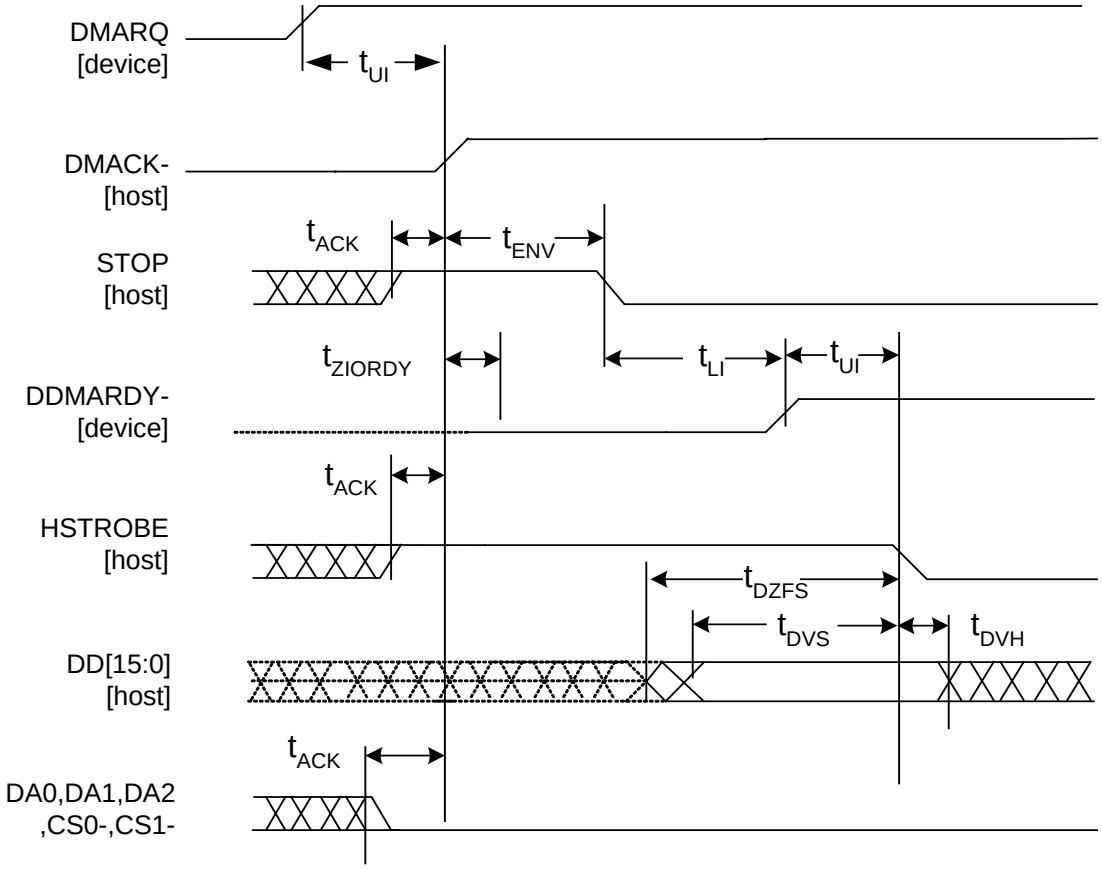


Figure 8-2. Initiating an Ultra DMA data-out burst

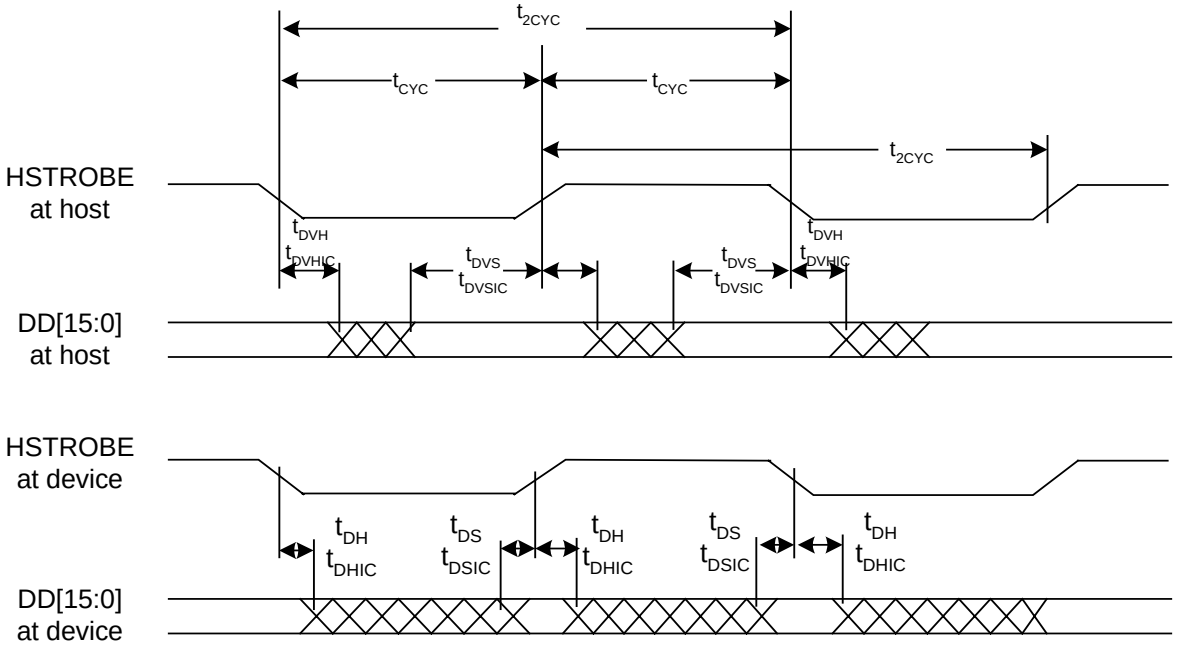
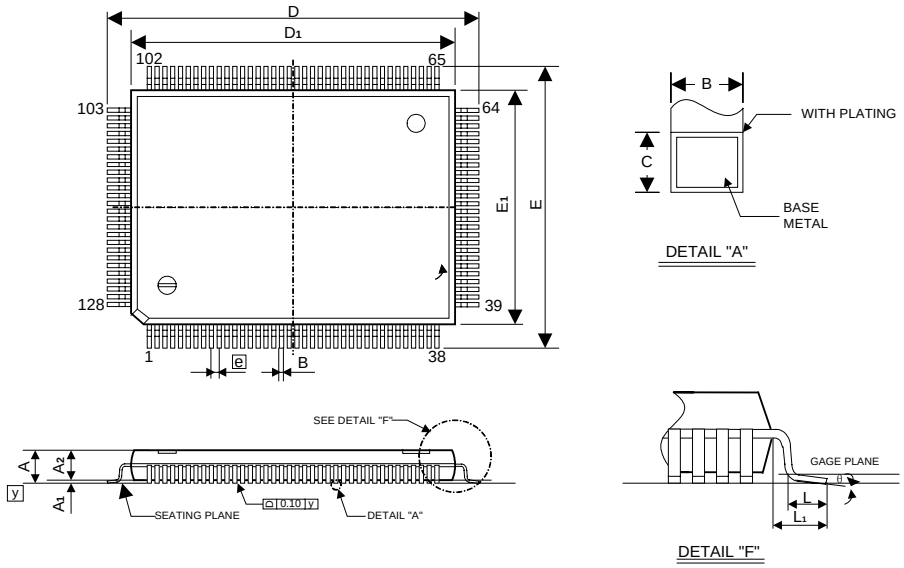


Figure 8-3. Sustained Ultra DMA data-out burst

9. Package Information

QFP 128L Outline Dimensions unit: inches/mm



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.134	-	-	3.40
A**1**	0.010	-	-	0.25	-	-
A**2**	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

Notes:

1. Dimensions D_1 and E_1 do not include mold protrusion, but mold mismatch is included.
2. Dimension B does not include dambar protrusion.
3. Controlling dimension: millimeter.

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10. Ordering Information

Part No.	Package
IT8211F	128 QFP