I^2C Clock Generator for 3 DIMM, Pentium™ II Designs

Approved Product

PRODUCT FEATURES

- Supports Pentium™, Pentium™ Pro and Cyrix CPUs.
- 4 CPU / AGP clocks
- Up to 12 SDRAM clocks for 3 DIMs.
- 7 PCI synchronous clocks.
- Optional common or mixed supply mode:
- (Vdd = Vddq3 = Vddq2 = 3.3V) or (Vdd = Vddq3 = 3.3V, Vddq2 = 2.5V)
- < 250ps skew among CPU or SDRAM clocks.
- < 250ps skew among PCI clocks.
- I^2C 2-Wire serial interface
- Programmable registers featuring:
  - Jumperless frequency selection
  - enable/disable each output pin
  - mode as tri-state, test, or normal
- Power Management Capability.
- IOAPIC clocks for multiprocessor support.
- 48 MHz for USB support
- 48-pin SSOP package

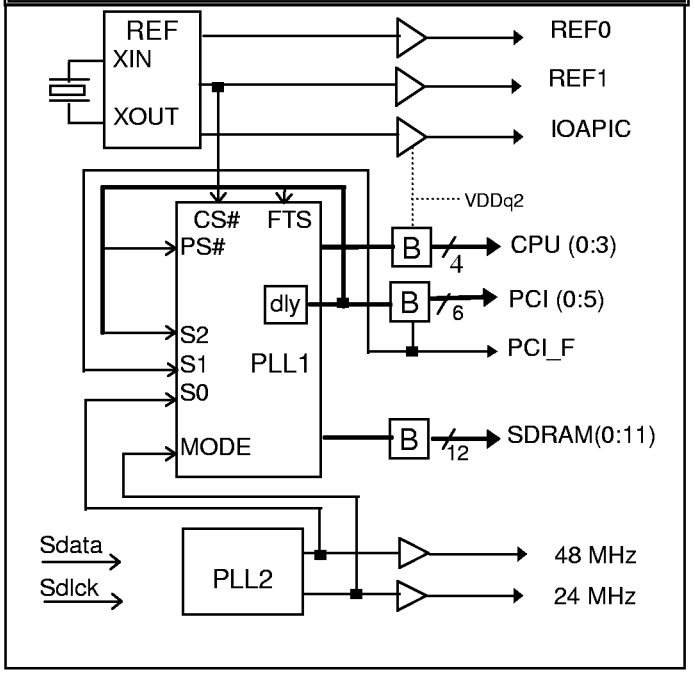
FREQUENCY TABLE (MHz)

			FTS = 1		FTS = 0	
S2	S1	S0	CPU	PCI	CPU	PCI
0	0	0	61.8	30.9	62.4	31.2
0	0	1	75	30	78**	39**
0	1	0	83.3**	33.3**	85.8**	42.8**
0	1	1	68.5	34.25	69.5	34.74
1	0	0	55	27.5	83.3**	41.7**
1	0	1	75	37.5	75	a.32
1	1	0	60	30	*	*
1	1	1	66.8	33.4	50	25

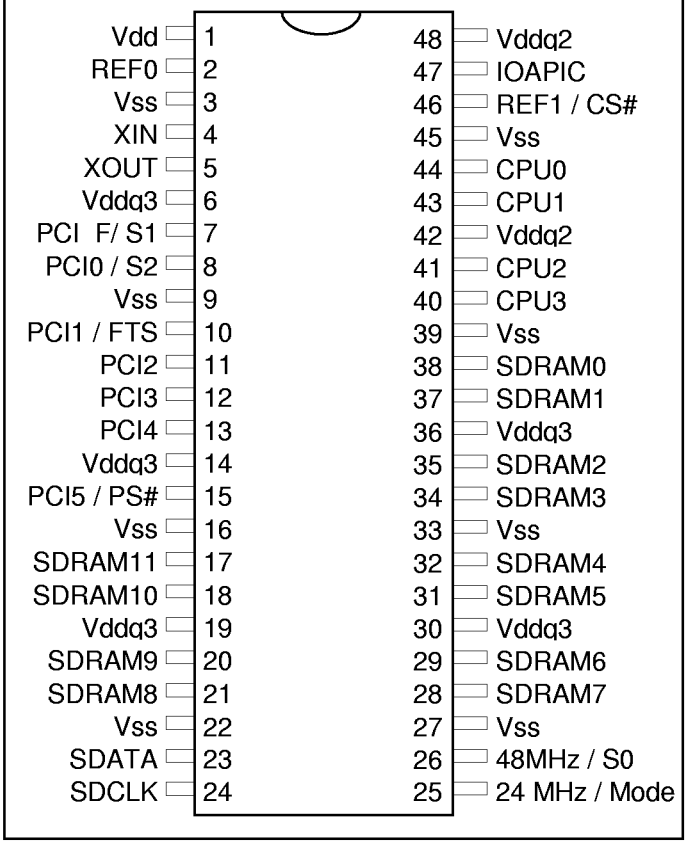
* Reserved for IMI use only

** Available for 3.3V @ ambient only

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

Xin, Xout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). Xin may also serve as input for an externally generated reference signal.

REF0 - Buffered output of the crystal.

REF1 / CS# - This pin is bidirectional. If pin 25, MODE = 1 (default), then this pin is a REF1 buffered output of the crystal. If pin 25, MODE = 0 then this pin is CS# and is used in power management mode for synchronously stopping the all CPU clocks (see page 4).

CPU (0:3) - Low skew (<250 pS) clock outputs for host frequencies such as CPU, Chipset, Cache. Vddq2 is the supply voltage for these outputs.

SDRAM(0:11) - Synchronous DRAM DIMs clocks, they have the same frequency as CPU clocks.

PCI (2:4) - Low skew (<250pS) PCI clock outputs.

PCI1 / FTS, PCI0 / S2, PCI_F / S1 - Low skew (<250pS) PCI clock outputs. These pins are bidirectional. During power-up, These pins are inputs (FTS, S2 and S1) and are used for HARD selecting the output frequency of CPU, SDRAM and PCI clocks, see Frequency table page1 and page 11, fig.3. When the power reaches the VDD rail (See Fig.1, page3), the selected data is latched internally to the IC and these pins become PCI1, PCI0 and PCI_F clock outputs.

PCI5 / PS# - PCI clock output. This pin is a bidirectional. If pin 25, MODE = 1 (default), then this pin is a PCI5 clock output. If pin 25, MODE = 0 then this pin is PS# and is used in power management mode for synchronously stopping the all PCI clocks (see page 4).

IOAPIC - This pin is a high drive buffered output of the crystal. This pin is powered by VDDq2.

48 MHz / S0 - This is a bidirectional pin. During power-up, This pin is in input mode and is used for selecting the output frequency of CPU and SDRAM clocks, see Frequency table page1 and page 11, fig.3 for jumper application; this pin has an internal pull-up. When the power reaches the VDD rail (See Fig.1, page3), the selected data is latched internally to the IC and this pin becomes a 48 Mhz output for USB clock.

24 MHz / MODE - This is a bidirectional pin. During power-up, This pin is an input and is used for enabling (0) or disabling (1, default) the power management pins 15 and 46. see page 4 and page 11, fig.3 for jumper application; this pin has an internal pull-up. When power reaches the VDD rail (See Fig.1, page 3), the selected data is latched internally to the IC and this pin becomes a 24 Mhz output for SIO clock.

SDATA - serial data of I^2C 2-wire control interface. Has internal pull-up resistor.

SDCLK - serial clock of I^2C 2-wire control interface. Has internal pull-up resistor.

Vss - Circuit Ground.

Vdd - Power supply for analog circuit and core logic.

Vddq3 - Power supply pins for 3.3V IO pins.

Vddq2 - Power supply pins for 2.5V/3.3V IO pins.

A bypass capacitor (0.1μF) should be placed as close as possible to each Vdd, Vddq2, and Vddq3 pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductances of the traces.

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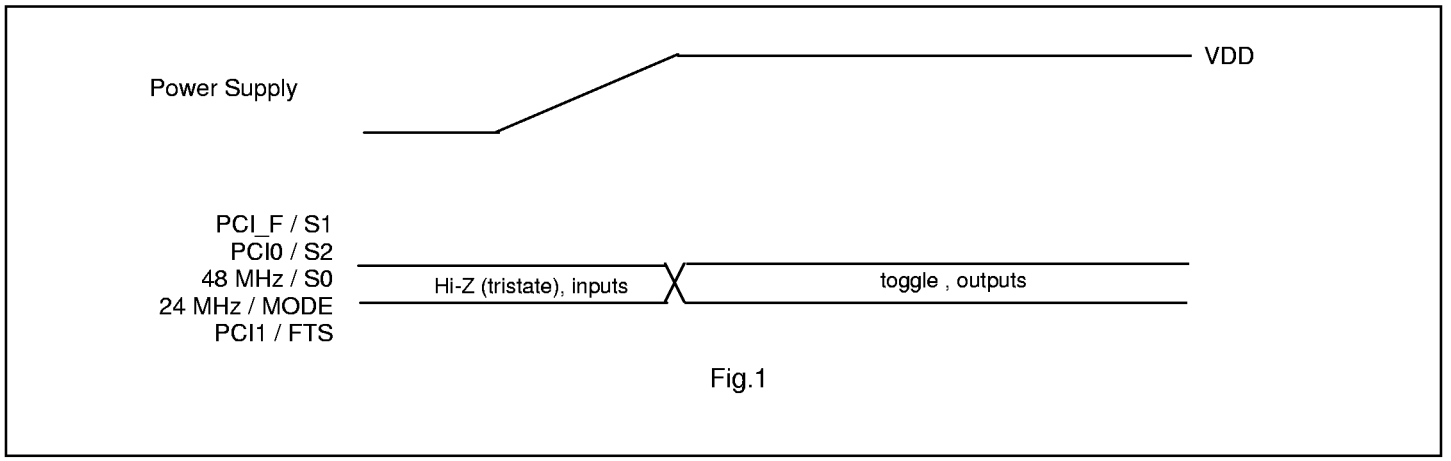

Fig.1

POWER MANAGEMENT FUNCTIONS

When MODE=0, pins 15 and 46 are inputs PS# (PCI_STOP#), and CS# (CPU_STOP#), respectively (when MODE=1, these functions are not available). A particular output is enabled only when both the serial interface and these pins indicate that it should be enabled. The IMISC643 clocks may be disabled according to the following table in order to reduce power consumption. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped. The CPU/AGP and PCI clocks transition between running and stopped by waiting for one positive edge on PCICLK_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	PCI_STOP#	CPU	PCI	OTHER CLKs	XTAL & VCOs
0	0	LOW	LOW	RUNNING	RUNNING
0	1	LOW	Frequency Table	RUNNING	RUNNING
1	0	Frequency Table	LOW	RUNNING	RUNNING
1	1	Frequency Table	Frequency Table	RUNNING	RUNNING

Please note that all clocks can be individually asynchronously enabled or stopped via the 2-wire I2C control interface. In this case all clocks are stopped in the low state.

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POWER MANAGEMENT TIMING

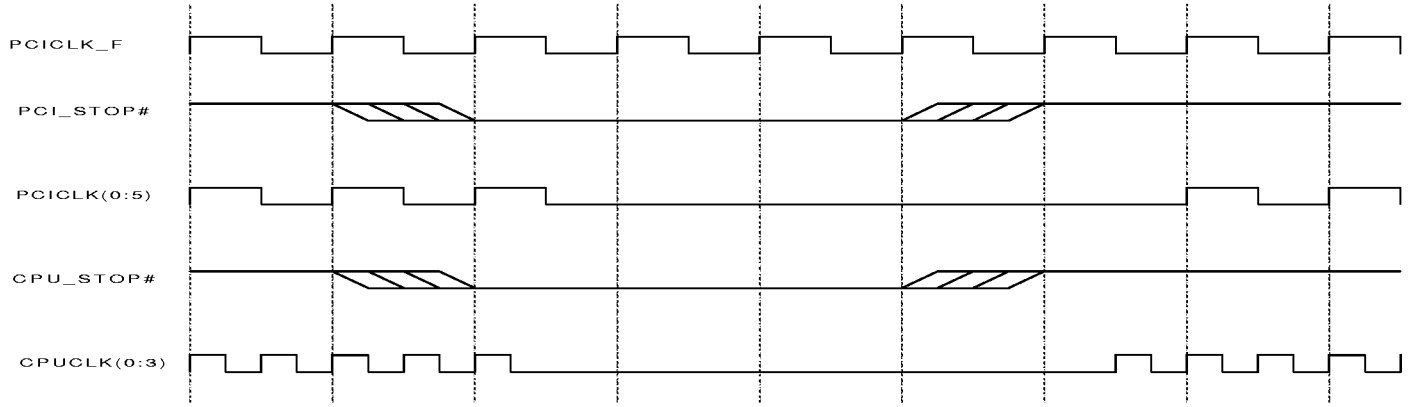

Fig. 2

2-WIRE I²C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The IMISC643 cannot be read back. Sub-addressing is not supported, thus all preceeding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The IMISC643 will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The IMISC643 will not respond to any other control interface conditions. Previously set control registers are retained.

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SERIAL CONTROL REGISTERS

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PWR_DWN# pin is activated.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below desrcibed sequence (Byte 0, Byte 1, Byte2, ...) will be valid and acknowledged.

Byte 0: Frequency, Function Select Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	*	FTS (for frequency table selection by software via I2C)
6	1	*	S2 (for frequency table selection by software via I2C)
5	1	*	S1 (for frequency table selection by software via I2C)
4	1	*	S0 (for frequency table selection by software via I2C)
3	0	*	enables freq. selection by hardware (set to 0) or software I2C (set to 1)
2	x	n/a	Reserved for future Spectrum Spread function
1 0	0 0	* *	Bit1 Bit0 1 1 Tri-State 1 0 Reserved for future Spectrum Spread function 0 1 Reserved for future Spectrum Spread function 0 0 Normal

Function Table

Function Description	Outputs				
	CPU	PCI	SDRAM	Ref	IOAPIC
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Normal	see table	see table	CPU	14.318	14.318

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SERIAL CONTROL REGISTERS (Cont.)

Byte 1: CPU, SIO, USB Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	26	48 Mhz enable/Stopped
6	1	25	24 Mhz enable/Stopped
5	1	-	0 = IC in TEST mode. 1 = normal operation.
4	x	-	Reserved
3	1	40	CPUCLK3 enable/Stopped
2	1	41	CPUCLK2 enable/Stopped
1	1	43	CPUCLK1 enable/Stopped
0	1	44	CPUCLK0 enable/Stopped

Byte 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	7	PCI_F / S1enable/Stopped
5	1	15	PCI5 / PS# enable/Stopped
4	1	13	PCI4 enable/Stopped
3	1	12	PCI3 enable/Stopped
2	1	11	PCI2 enable/Stopped
1	1	10	PCI1 / FTS enable/Stopped
0	1	8	PCI0 / S2 enable/Stopped

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	28	SDRAM7 enable/Stopped
6	1	29	SDRAM6 enable/Stopped
5	1	31	SDRAM5 enable/Stopped
4	1	32	SDRAM4 enable/Stopped
3	1	34	SDRAM3 enable/Stopped
2	1	35	SDRAM2 enable/Stopped
1	1	37	SDRAM1 enable/Stopped
0	1	38	SDRAM0 enable/Stopped

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SERIAL CONTROL REGISTERS (Cont.)

Byte 4: Additional SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	1	17	SDRAM11 enable/Stopped
2	1	18	SDRAM10 enable/Stopped
1	1	20	SDRAM9 enable/Stopped
0	1	21	SDRAM8 enable/Stopped

Byte 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	1	47	IOAPIC enable/Stopped
3	x	-	Reserved
2	x	-	Reserved
1	x	46	REF1 / CS# enable/Stopped
0	1	2	REF0 enable/Stopped

Byte 6: Reserved Register

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	x	-	Reserved

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Ambient Temperature:	-55ºC to +125ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	116	mA	CPU = 66.6 MHz, PCI = 33.3 Mhz Unloaded
Static Supply Current	Isdd	-	-	13	µA	-
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds
						VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5 ± 5%, TA = 0ºC to +70ºC

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM)	tSKEW1	-	-	250	ps	15 pf Load Measured at 1.5V
Skew (CPU-SDRAM)	tSKEW2	-	-	500	ps	15 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	-
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
Overshoot/Undershoot Beyond Power Rails	V_{over}	-	-	1.5	V	22 ohms @ source of 8 inch PCB run to 15 pf load
Ring Back Exclusion	V_{RBE}	0.7		2.1	V	note1
						VDD = VDDQ3 =3.3V ±5%, VDDQ2 =2.5 ± 5%, TA = 0ºC to +70ºC

note 1: Ring Back must not enter this range.

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TYPE 1 BUFFER CHARACTERISTICS FOR CPU (0:3)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH	-91	-131	-183	mA	Vout = 1.0 V
Pull-Up Current	IOH	-43	-62	-89	mA	Vout = 2.0V
Pull-Down Current	IOL	83	119	167	mA	Vout = 1.2 V
Pull-Down Current	IOL	26	38	53	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	2.0	nS	20 pF Load
						VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5 ± 5%, TA = 0ºC to +70ºC

TYPE 2 BUFFER CHARACTERISTICS FOR IOAPIC						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH	-91	-131	-183	mA	Vout = 1.0 V
Pull-Up Current	IOH	-43	-62	-87	mA	Vout = 2.0V
Pull-Down Current	IOL	83	119	167	mA	Vout = 1.2 V
Pull-Down Current	IOL	26	38	53	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	1.9	nS	20 pF Load
						VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5 ± 5%, TA = 0ºC to +70ºC

TYPE 3 BUFFER CHARACTERISTICS FOR REF0, REF1, 24MHZ, 48MHZ						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH	-40	-53	-69	mA	Vout = 1.0 V
Pull-Up Current	IOH	-32	-42	-53	mA	Vout = 2.0V
Pull-Down Current	IOL	37	47	58	mA	Vout = 1.2 V
Pull-Down Current	IOL	12	15	19	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	2.0	nS	20 pF Load
						VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5 ± 5%, TA = 0ºC to +70ºC

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TYPE 4 BUFFER CHARACTERISTICS FOR SDRAM(0:11)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH	-94	-134	-188	mA	Vout = 1.0 V
Pull-Up Current	IOH	-74	-106	-148	mA	Vout = 2.0 V
Pull-Down Current	IOL	83	119	167	mA	Vout = 1.2 V
Pull-Down Current	IOL	26	38	53	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	20 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	2.0	nS	30 pF Load
						VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5 ± 5%, TA = 0ºC to +70ºC

TYPE 5 BUFFER CHARACTERISTICS FOR PCICLK(0:5,F)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH	-94	-134	-188	mA	Vout = 1.0 V
Pull-Up Current	IOH	-74	-106	-148	mA	Vout = 2.0 V
Pull-Down Current	IOL	83	119	167	mA	Vout = 1.2 V
Pull-Down Current	IOL	26	38	53	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	15 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	2.0	nS	30 pF Load
						VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5 ± 5%, TA = 0ºC to +70ºC

APPLICATION NOTE FOR SELECTION ON BIDIRECTIONAL PINS

Pins 7, 8, 10, 25, and 26are bidirectional pins and are used for selecting different functions in this device (see Pin description, Pages 2&3). During power-up of the SC643, these pins are in input mode (see Fig1, page3), therefore, they are considered input select pins. Internal to the IC, these pins have a large value pull-up each (100KΩ), therefore, a selection "1" is the default. If a selection "0" is desired, then a direct connection to ground through a 10KΩ resistor should be implemented as shown in Fig.3. Please note the selection resistor (10KΩ) is placed before the Damping resistor (Rd) close to the pin.

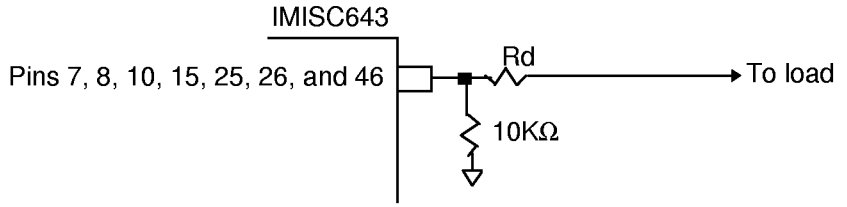

Fig. 3

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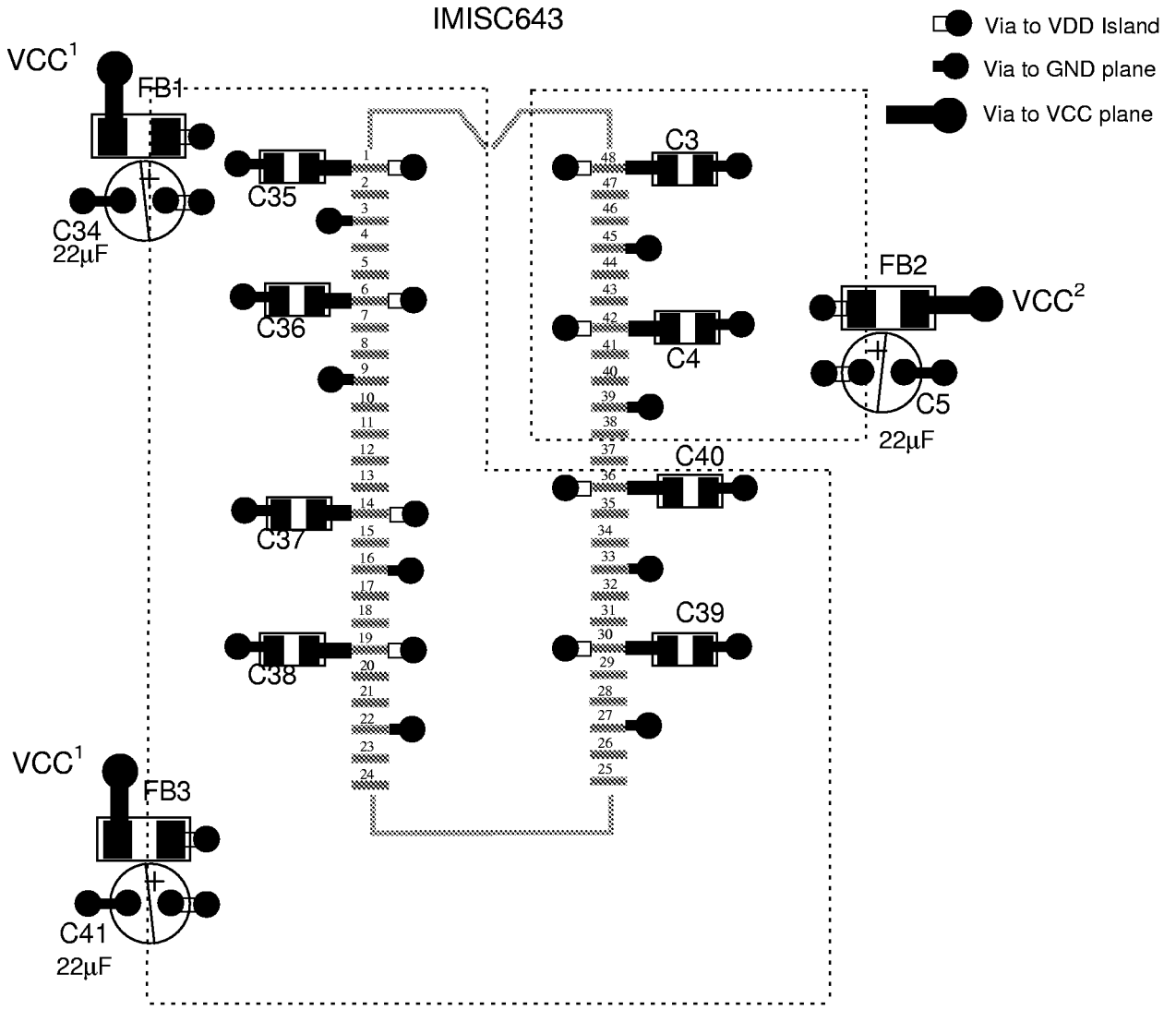
PCB LAYOUT SUGGESTION



This is only a layout recommendation for best performance and lower EMI. The designer may choose a different approach but C3, C4, C35, C36, C37, C38, C39and C40 (all are 0.1µf) should always be used and placed as close as possible to their VDD pins.

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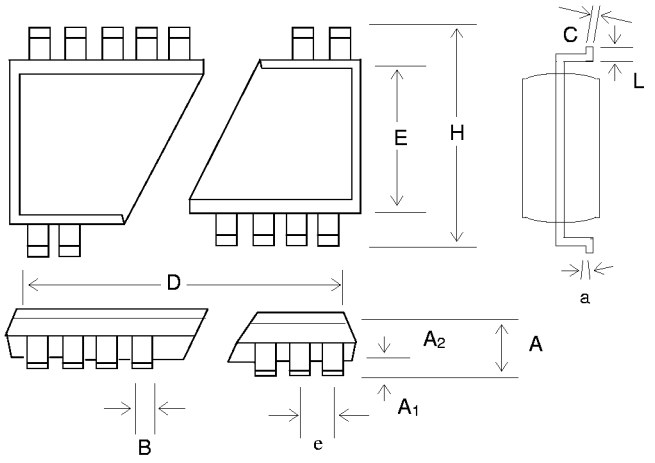
PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0º	5º	8º	0º	5º	8º

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC643AYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC643AYB
Date Code, Lot #

IMISC643AYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number

NOTE : Purchase of I^2C components of International Microcircuits, Inc. or one of its sublicensed Associated Companies conveys a license under the Phillips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Phillips.