100MHz Spread Spectrum Motherboard Frequency Generator

Features

- Maximized EMI suppression using IC WORKS' Spread Spectrum Technology
- Reduces measured EMI by as much as 10dB
- I^2C programmable
- Two skew-controlled copies of CPU output
- Seven copies of PCI output (synchronous w/CPU output)
- One copy of 14.31818 MHz IOAPIC output
- One copy of 48MHz USB output
- Selectable 24/48MHz output is determined by resistor straps on power up
- One high drive output buffer that produces a copy of the 14.318MHz reference
- Programmable to 133, 124, 112, 103, 100 MHz and below
- For 3 DIMM designs, see also the W40S11-23 buffer chip, for 4 DIMM designs see the W40S12-24 or W40S01-04

Key Specifications

Supply Voltages:

VDDQ3 = 3.3V±5%
VDDQ2 = 2.5V±5%

CPU Cycle to Cycle Jitter:	200ps
CPU, PCI Edge Rate:	≥1V/ns
CPU0:1 Skew:	175ps
PCI_F, PCI1:6 Skew:	500ps
CPU to PCI Skew:	1.5 - 4.0ns (CPU Leads)

Logic inputs and REF2X/SEL48# have 250Kohm pull-up resistors, except SEL100/66#

Figure 1 Block Diagram

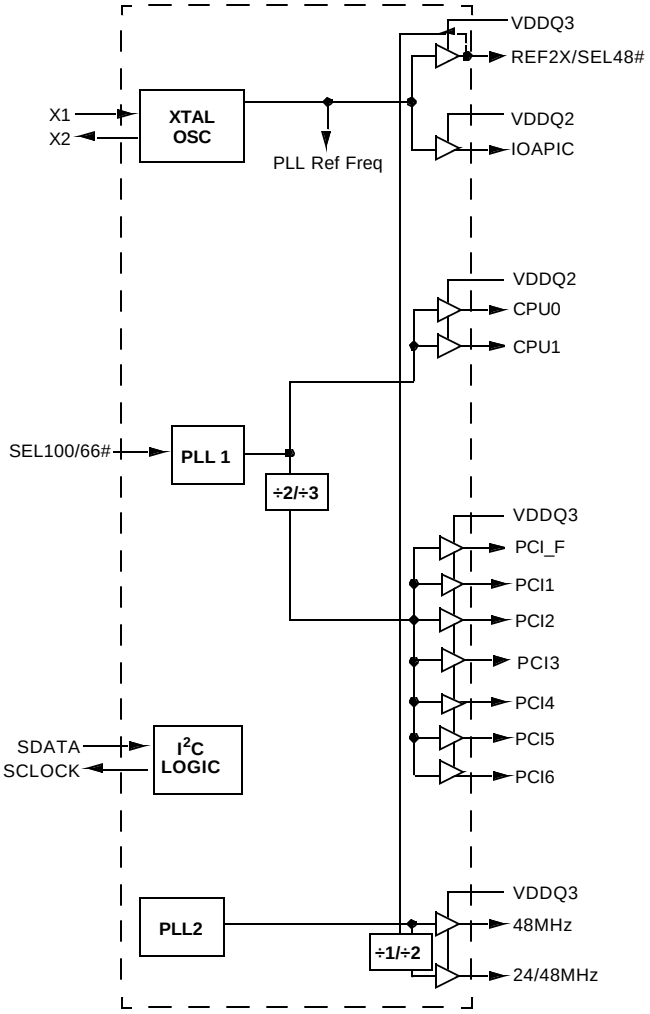


Table 1 Pin Selectable Frequency

SEL100/66#	CPU(0:1)	PCI
1	100MHz	33.3MHz
0	66.8MHz	33.4MHz

Figure 2 Pin Diagram

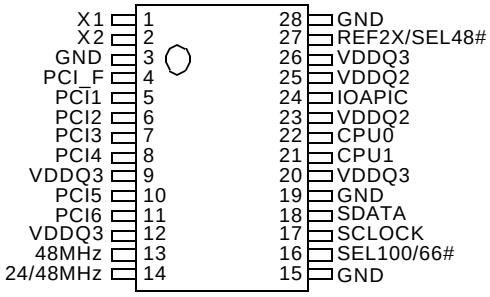


Table 2 Order Information

Part Number	Package
W124	G = SOIC (300 mils)

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:1	22, 21	O	***CPU Clock Outputs 0 through 1:*** These two CPU clocks run at a frequency set by SEL100/66#. Output voltage swing is set by the voltage applied to VDDQ2.
PCI1:6 PCI_F	5, 6, 7, 8, 10, 11, 4	O	***PCI Clock Outputs 1 through 6 and PCI_F:*** These seven PCI clock outputs run synchronously to the CPU clock. Voltage swing is set by the power connection to VDDQ3.
IOAPIC	24	O	***I/O APIC Clock Output:*** Provides 14.318MHz fixed frequency. The output voltage swing is set by the power connection to VDDQ2.
48MHz	13	O	***48MHz Output:*** Fixed 48MHz USB clock. Output voltage swing is controlled by voltage applied to VDDQ3.
24/48MHz	14	O	***24MHz or 48MHz Output:*** Frequency is set by the state of pin 27 on power up.
REF2X/ SEL48#	27	I/O	***I/O Dual Function REF2X and SEL48# pin:*** Upon power-up, the state of SEL48# is latched. The initial state is set by either a 10K resistor to GND or to VDD. A 10K resistor to GND causes pin 14 to output 48MHz. If the pin is strapped to VDD, pin 14 will output 24MHz. After 2ms, the pin becomes a high drive output that produces a copy of 14.318MHz.
SEL100/66#	16	I	***Frequency Selection Input:*** Selects CPU clock frequency as shown in Table1 on page1.
SDATA	18	I/O	***I^2C Data Pin:*** Data should be presented to this input as described in the I^2C section of this data sheet. Internal 250K ohm pull-up resistor.
SCLOCK	17	I	***I^2C clock Pin:*** The I^2C Data clock should be presented to this input as described in the I^2C section of this data sheet.
X1	1	I	***Crystal Connection or External Reference Frequency Input:*** Connect to either a 14.318MHz crystal or other reference signal.
X2	2	I	***Crystal Connection:*** An input connection for an external 14.318MHz crystal. If using an external reference, this pin must be left unconnected.
VDDQ3	9,12,20,26	P	***Power Connection:*** Power supply for PCI output buffers, 48MHz USB output buffers, Reference output buffer, core logic and PLL circuitry. Connect to 3.3V supply.
VDDQ2	23, 25	P	***Power Connection:*** Power supply for IOAPIC and CPU output buffers. Connect to 2.5V supply.
GND	3, 15, 19, 28	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Overview

The W124 a motherboard clock synthesizer, can provide either a 2.5V or 3.3V CPU clock swing making it suitable for a variety of CPU options. A fixed 48MHz clock is provided for other system functions. The device W124 supports spread spectrum clocking for reduced EMI.

Functional Description

I/O Pin Operation

Pin 27 is a dual purpose I/O pin. Upon power up this pin acts as a logic input, allowing the determination of assigned device functions. A short time after power up, the logic state of the pin is latched and the pin becomes a clock output. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10 kohm "strapping" resistor is connected between the I/O pin and ground or VDD. Connection to ground sets a latch to "0", connection to VDD sets a latch to "1'. Figure 3 and Figure 4 show two suggested methods for strapping resistor connections.

Upon W124 power up, the first 2ms of operation is used for input logic selection. During this period, the Reference clock output buffer is tristated, allowing the output strapping resistor on the I/O pin to pull the pin and its associated capacitive clock load to either a logic high or low state. At the end of the 2ms period, the established logic "0" or "1" condition of the I/O pin is then latched. Next the output buffer is enabled which converts the I/O pin into an operating clock output. The 2ms timer is started when VDD reaches 2.0V. The input bit can only be re-set by turning VDD off and then back on again.

It should be noted that the strapping resistor has no significant effect on clock output signal integrity. The drive impedance of clock output is 25 ohms (nominal) which is minimally affected by the 10 kohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock output is enabled following the 2ms input period, a 14.318MHz output frequency is delivered on the pin, assuming that VDD has stabilized. If VDD has not yet reached full value, output frequency initially may be below target but will increase to target once VDD voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

Figure 3 Input Logic Selection Through Resistor Load Option

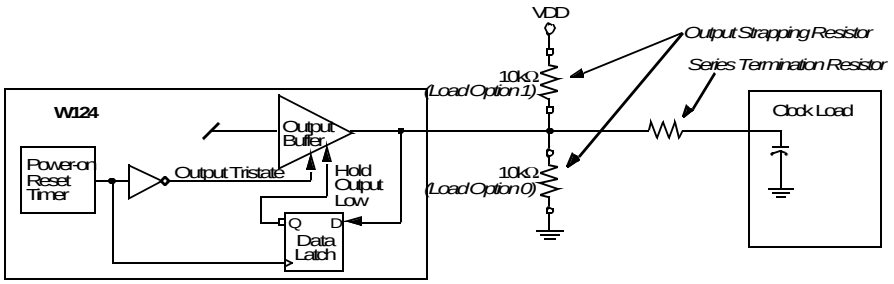
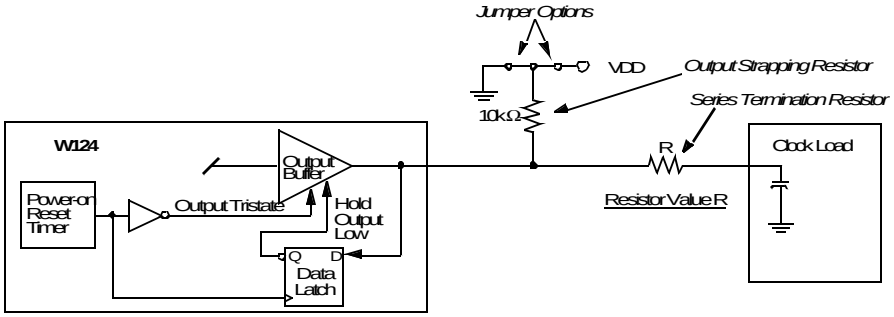


Figure 4 Input Logic Selection Through Jumper Option



Spread Spectrum Clocking

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in Figure 5.

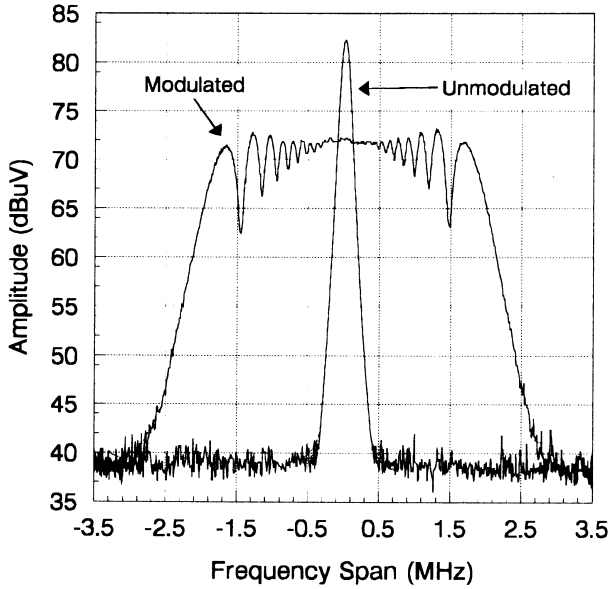
As shown in Figure 5, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

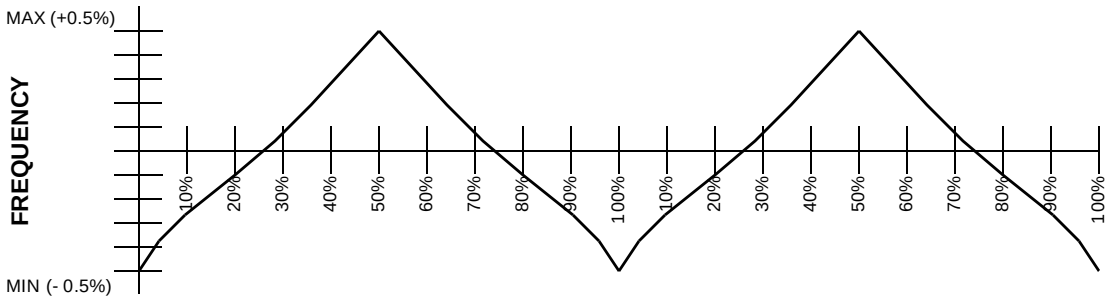
The output clock is modulated with a waveform depicted in Figure 6. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is ± 0.5% of the center frequency. Figure 6 details the IC WORKS spreading pattern. IC WORKS does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Figure 5 Clock Harmonic with and without SSCG Modulation Frequency Domain Representation



Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for bits 1-0 in data byte 0 of the I^2C data stream. Refer to Table 7 for more details.

Figure 6 Typical Modulation Profile



Serial Data Interface

The W124 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W124 initializes with default register settings. Therefore, the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if required. The interface can also be used during system operation for power management functions. Table 3 summarizes the control functions of the serial data interface.

Table 3 Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections beyond the 100 and 66.66MHz selections that are provided by the SEL100/66# pin. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Tristate	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to Table 5.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Operation

Data is written to the W124 in ten bytes of eight bits each. Bytes are written in the order shown in Table 4.

Table 4 Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W124 to accept the bits in Data Bytes 3-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W124 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the W124, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the W124, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Don't Care	Refer to IC WORKS SDRAM drivers (W40S11-23, W40S12-24, W40S01-04H).
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3	Refer to Table 5	The data bits in these bytes set internal W124 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 5, Data Byte Serial Configuration Map.
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit in the data bytes control a particular device function except for the "reserved" bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. Table 5 gives the bit formats for registers located in Data Bytes 3-6.

Table 6 details additional frequency selections that are available through the serial data interface.

Table 7 details the select functions for Byte 3, bits 1 and 0.

Table 5 Data Bytes 3-6 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 3						
7	--	--	(Reserved)	--	--	0
6	--	--	SEL_2	Refer to Table 6		0
5	--	--	SEL_1	Refer to Table 6		0
4	--	--	SEL_0	Refer to Table 6		0
3	--	--	BYT3 or SEL Pin	Frequency Controlled by external SEL100/ 66# pin	Frequency Controlled by BYT3 SEL (2:0)	0
2	--	--	(Reserved)	--	--	0
1-0	--	--	Bit 1 Bit 0 Function (See Table 7 for function details) 0 0 Normal Operation 0 1 Test Mode 1 0 Spread Spectrum on ± 0.5% Modulation 1 1 All Outputs Tristated			00
Data Byte 4						
7	--	--	(Reserved)	--	--	0
6	14	24/48MHz	Clock output disable	Low	Active	1
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	21	CPU1	Clock Output Disable	Low	Active	1
1	--	--	(Reserved)	--	--	0
0	22	CPU0	Clock Output Disable	Low	Active	1
Data Byte 5						
7	4	PCI_F	Clock Output Disable	Low	Active	1
6	11	PCI6	Clock Output Disable	Low	Active	1
5	10	PCI5	Clock Output Disable	Low	Active	1
4	-	--	(Reserved)	--	--	0
3	8	PCI4	Clock Output Disable	Low	Active	1
2	7	PCI3	Clock Output Disable	Low	Active	1
1	6	PCI2	Clock Output Disable	Low	Active	1
0	5	PCI1	Clock Output Disable	Low	Active	1
Data Byte 6						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	24	IOAPIC	Clock Output Disable	Low	Active	1
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	27	REF2X	Clock Output Disable	Low	Active	1 (Note 2)
0	27	REF2X	Clock Output Disable	Low	Active	1 (Note 2)

Table 6 Additional Frequency Selections through Serial Data Interface Data Bytes

Input Conditions			Output Frequency		If Spread Is On
Data Byte 3, Bit 3 = 1					
Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)	Spread Percentage
0	0	0	124	41.3	±0.5% Center
0	0	1	75	37.5	±0.5% Center
0	1	0	83.3	41.6	±0.5% Center
0	1	1	66.8	33.4	±0.5% Center
1	0	0	103	34.25	±0.5% Center
1	0	1	112	37.3	±0.5% Center
1	1	0	133.3	44.43	±0.5% Center
1	1	1	100	33.3	±0.5% Center

Table 7 Select Function for Data Byte 3, Bits 0:1

	Input Conditions		Output Conditions				
	Data Byte 3						
Function	Bit 1	Bit 0	CPU0:1	PCI_F, PCI1:6	REF2X, IOAPIC	48MHZ	24MHZ
Normal Operation	0	0	Note 1	Note 1	14.318MHz	48MHz	24MHz
Spread Spectrum Mode	1	0	±0.5%	±0.5%	14.318MHz	48MHz	24MHz
Test Mode	0	1	X1/2	CPU/2 or 3	X1	X1/2	X1/4
Tristate	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Notes: 1. CPU and PCI frequency selections are listed in Table 1 and Table 6.

2. Both Bits 0 &1 of Byte 6 in Table 5 MUST be set to the same value.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

DC Electrical Characteristics:

T_A = 0°C to +70°C; VDDQ3 = 3.3V±5%; VDDQ2 = 2.5V±5%

Symbol	Parameter		Min	Typ	Max	Unit	Test Condition
Supply Current							
I_{DDQ3}	Combined 3.3V Supply Current			85		mA	CPU0:1 = 100MHz Outputs Loaded (Note 1)
I_{DDQ2}	Combined 2.5V Supply Current			30		mA	CPU0:1 = 100MHz Outputs Loaded (Note 1)
Logic Inputs							
V_{IL}	Input Low Voltage		GND -.3		0.8	V	
V_{IH}	Input High Voltage		2.0		VDD +.3	V	
I_{IL}	Input Low Current (Note 2)				-25	µA	
I_{IH}	Input High Current (Note 2)				10	µA	
I_{IL}	Input Low Current (SEL100/66#)				-5	µA	
I_{IH}	Input High Current (SEL100/66#)				+5	µA	
Clock Outputs							
V_{OL}	Output Low Voltage				50	mV	I_{OL} = 1mA
V_{OH}	Output High Voltage		3.1			V	I_{OH} = -1mA
V_{OH}	Output High Voltage	CPU0:1/IOAPIC	2.2			V	I_{OH} = -1mA
I_{OL}	Output Low Current:	CPU0:1	38	57	97	mA	V_{OL} = 1.25V
		PCI_F, PCI1:6	74	96	200	mA	V_{OL} = 1.5V
		IOAPIC	55	85	165	mA	V_{OL} = 1.25V
		REF2X	50	74	152	mA	V_{OL} = 1.5V
		48MHz, 24MHz	50	60	120	mA	V_{OL} = 1.5V

DC Electrical Characteristics: (cont.)

T_A = 0°C to +70°C; VDDQ3 = 3.3V±5%; VDDQ2 = 2.5V±5%

Symbol	Parameter		Min	Typ	Max	Unit	Test Condition
I_{OH}	Output High Current	CPU0:1	38	55	97	mA	V_{OH} = 1.25V
		PCI_F, PCI1:6	74	96	200	mA	V_{OH} = 1.5V
		IOAPIC	55	85	165	mA	V_{OH} = 1.25V
		REF2X	50	74	152	mA	V_{OH} = 1.5V
		48MHz, 24MHz	50	60	120	mA	V_{OH} = 1.5V
Crystal Oscillator							
V_{TH}	X1 Input threshold Voltage (Note 3)			1.65		V	VDDQ3 = 3.3V
C_{LOAD}	Load Capacitance, As seen by External Crystal (Note 4)			14		pF	
$C_{IN,X1}$	X1 Input Capacitance (Note 5)			28		pF	Pin X2 unconnected
Pin Capacitance/Inductance							
C_{IN}	Input Pin Capacitance				5	pF	Except X1 and X2
C_{OUT}	Output Pin Capacitance				6	pF	
L_{IN}	Input Pin Inductance				7	nH	

Notes: 1. All clock outputs loaded with 6" 60 Ω transmission line, with 20pF capacitors .

2. W124 logic inputs have internal pull-up resistors, except SEL100/66# (pull-ups not CMOS level).
3. X1 input threshold voltage (typical) is VDDQ3/2.
4. The W124 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

AC Electrical Characteristics:

T_A = 0°C to +70°C; VDDQ3 = 3.3V±5%; VDDQ2 = 2.5V±5%; f_{XTL} = 14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs, CPU0:1 (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU = 66.8MHz			CPU = 100MHz			Unit	Test Condition/Comments
		Min	Typ	Max	Min	Typ	Max		
t_P	Period	15		15.5	10		10.5	ns	Measured on rising edge at 1.25.
t_H	High Time	5.2			3.0			ns	Duration of clock cycle above 2.0V.
t_L	Low Time	5.0			2.8			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	1		4	V/ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	1		4	1		4	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	45		55	%	Measured on rising and falling edge at 1.25V.
t_{JC}	Jitter, Cycle-to-Cycle			200			200	ps	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			175			175	ps	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		20			20		ohm	Average value during switching transition. Used for determining series termination value.

PCI Clock Outputs, PCI1:6 and PCI_F(Lump Capacitance Test Load = 30pF)

Symbol	Parameter	CPU = 66.8/100MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
t_P	Period	30			ns	Measured on rising edge at 1.5V.
t_H	High Time	12.0			ns	Duration of clock cycle above 2.4V.
t_L	Low Time	12.0			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			250	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			500	ps	Measured on rising edge at 1.5V.
t_O	CPU to PCI Clock Offset	1.5		4.0	ns	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		15		ohm	Average value during switching transition. Used for determining series termination value.

IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU = 66.8/100MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
f	Frequency, Actual		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.25V.
t_A	Jitter, Absolute			500	ps	Measured on rising edge at 1.25V. Maximum deviation of clock period.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		15		ohm	Average value during switching transition. Used for determining series termination value.

REF2X Clock Output (Lump Capacitance Test Load = 20pF)

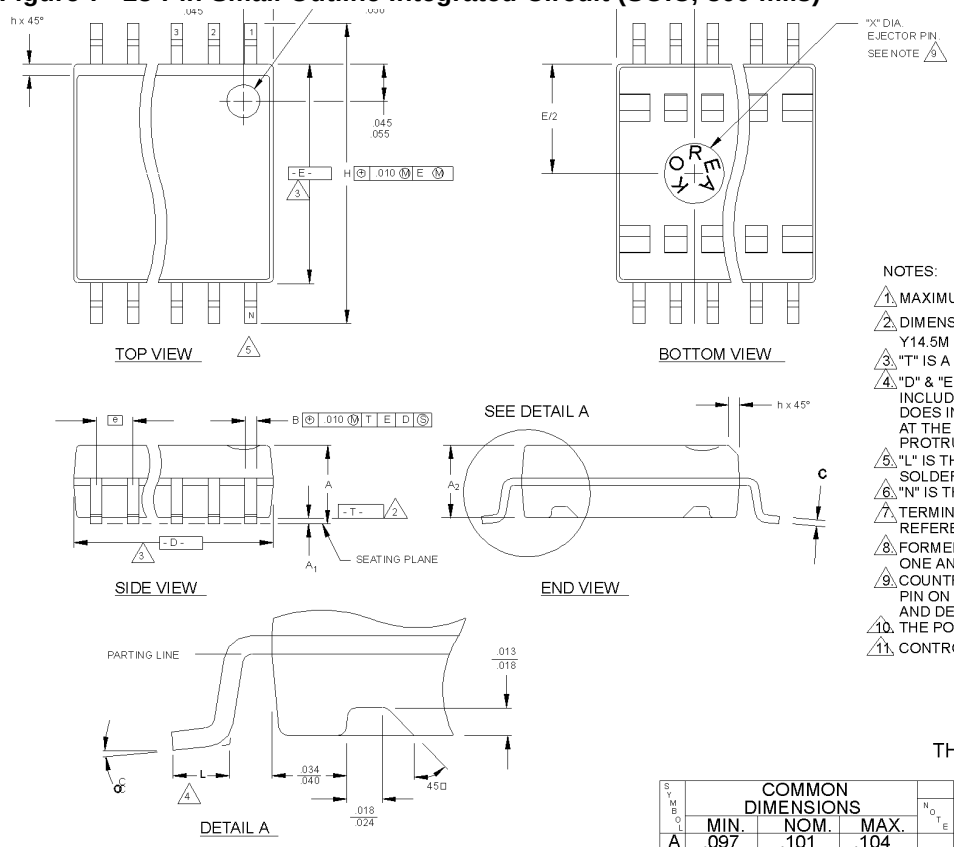
Symbol	Parameter	CPU =66.8/100MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
f	Frequency, Actual		14.318		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	0.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	0.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

48MHz and 24MHz Clock Output (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU = 66.8/100MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
f	Frequency, Actual		48.008 24.004		MHz	Determined by PLL divider ratio (see m/nbelow).
f_D	Deviation from 48MHz		+167		ppm	(48.008 – 48)/48
m/n	PLL Ratio		57/17, 57/34			(14.31818MHz x 57/17 = 48.008MHz)
t_R	Output Rise Edge Rate	0.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	0.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		25		ohm	Average value during switching transition. Used for determining series termination value.

Mechanical Package Outline

Figure 7 28-Pin Small Outline Integrated Circuit (SOIC, 300 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCES PER ANSI. Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
10. THE POCKETS ON THE BOTTOM ARE OPTIONAL.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.097	.101	.104		AA	.402	.407	.412	16
A_1	.0050	.009	.0115		AB	.451	.456	.461	18
A_2	.090	.092	.094		AC	.500	.505	.510	20
B	.014	.016	.019		AD	.602	.607	.612	24
C	.0091	.010	.0125		AE	.701	.706	.711	28
D	SEE VARIATIONS			3					
E	.292	.296	.299						
e	.050 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			5					
∝	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	2.46	2.56	2.64		AA	10.21	10.34	10.46	16
A_1	0.127	0.22	0.29		AB	11.46	11.58	11.71	18
A_2	2.29	2.34	2.39		AC	12.70	12.83	12.95	20
B	0.35	0.41	0.48		AD	15.29	15.42	15.54	24
C	0.23	0.25	0.32		AE	17.81	17.93	18.06	28
D	SEE VARIATIONS			3					
E	7.42	7.52	7.59						
e	1.27 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			5					
∝	0°	5°	8°						
X	2.16	2.36	2.54						