PC95 Enhanced Super I/O with IrDA Transmission

Features

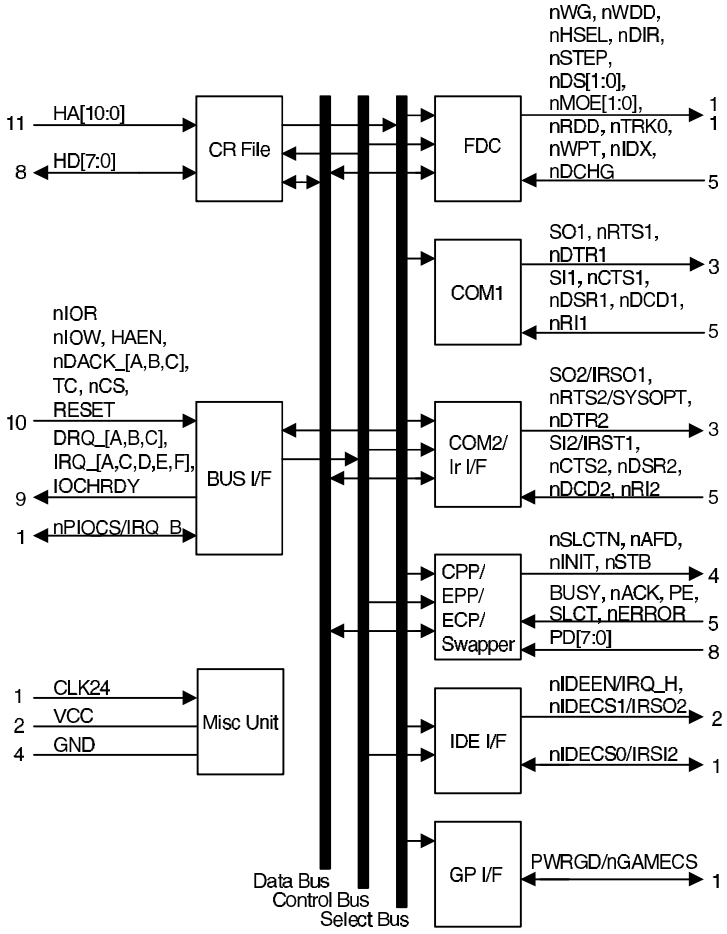
- On board Enhanced Super I/O Controller
- Provide Configurable area for each device on
  - Address mapping
  - IRQ channel routing
  - DMA channel routing
- Support the floppy disk upto 2.88MB
- FDD re-route to Parallel port
- Support 3-mode FDD
- Two high speed serial ports with the IrDA and ASKIr Supporting
- MIDI bit rate supporting on serial port
- Multi-mode parallel port supporting on ECP/EPP/SPP
- IDE/Game port interface decoder output
- Power Management supporting
- 100 PQFP

General Description

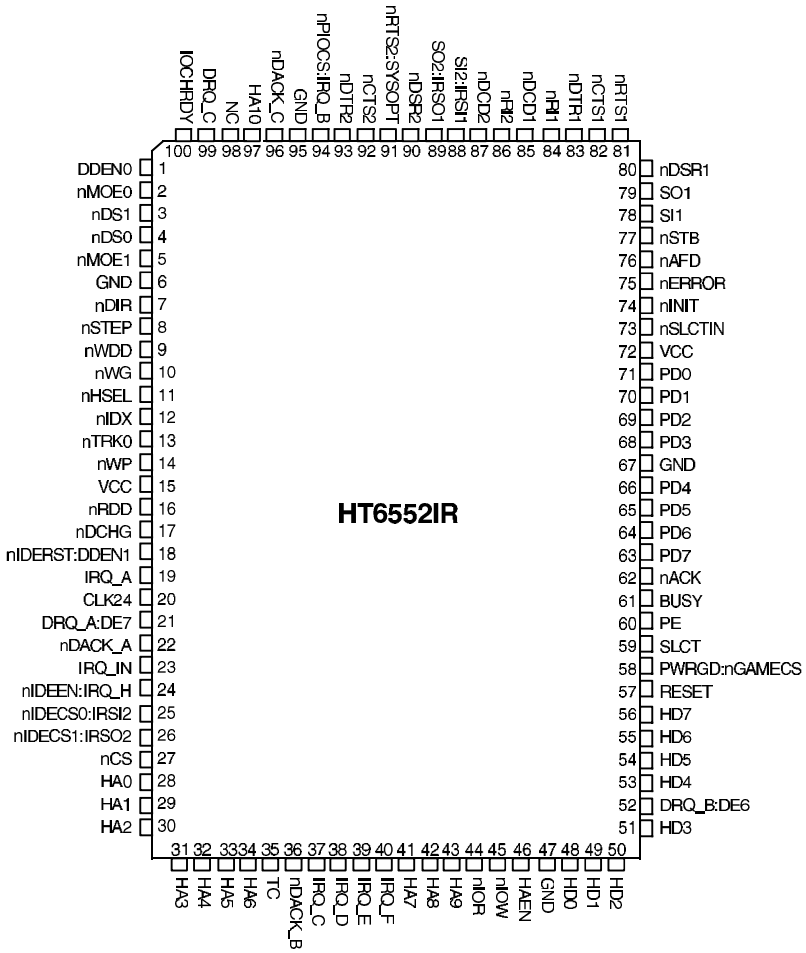
HT6552IR is a high integrated I/O device. It supports a floppy disk controller, a multi-mode printer port, two high speed serial communcation ports, one of which is enriched to support IrDA SIR and ASKIR transmission. By setting the different conf iguration, HT6552IR can also support IDE and game port interfaces.

There are some configuration register sets to reconfigure the ISA address, IRQ access channel, and DRQ channel for each device in order to support PC95 compatible function. The floppy disk controller supports the disk capacity upto 2.88MB with 3-mode floppy disk hardware interface. The disk interface can be re-routed to printer port for some specific applications. In the print port interface, it supports standard mode, PC/AT or PS/2 mode, Enhanced Parallel Port (EPP) 1.7/1.9, or Enhanced Capabilities Port (ECP). For the serial communication interface, there are two high speed ports for serial communication with the MIDI rate supports. One of which is expanded to support IrDA SIR or ASKIR transmission. By using the infrared interface, this device can support wireless communication easily.

Block Diagram



Pin Assignment



Pin Description

Host Interface

Pin No.	Pin Name	Type	Description
97,[43:41], [34:28]	HA[10:0]	I	Host I/O Address: For internal decoder use. The contents are latched internally by the leading edge of nIOR or nIOW.
[56:53], [51:48]	HD[7:0]	I/O24	Host I/O Data: For data accesses. These pins are Hi-Z when no output.
46	HAEN	I	Host Address Enable: For indicating DMA operation and internal address decode qualification.
44	nIOR	I	I/O Read: For host read operation.
45	nIOW	I	I/O Write: For host write operation.
100	IOCHRDY	OD8U	I/O Channel Ready: It is used to extend the host command in EPP mode. It is internal pull-up.
22 36 96	nDACK_A nDACK_B nDACK_C	I I I	DMA Acknowledgement: Host acknowledge the DMA request for transferring.
21 52 99	DRQ_A/ DRQ_B/ DRQ_C	O24ID O24ID O24	DMA Request: This pin is used to request host a DMA transferring. It will be cleared on the last data transfer by the nDACK/nIOR being low.
35	TC	I	Terminal Count: It indicates the DMA transfer is complete.
23	IRQ_IN	I	IRQ Input: An external IRQ input to the chip for IRQ router.
19 94 37 38 39 40 24	IRQ_A IRQ_B IRQ_C IRQ_D IRQ_E IRQ_F IRQ_H	O24 O24 O24 O24 O24 O24 O24	Interrupt Requests: The IRQ router outputs. Internal subsystems and IRQ_IN are connected to the router for re-configurable IRQ channels. When EPP or ECP mode is enable, the related IRQ output issues a low pulse for interrupt request.
27	nCS	I	Chip Select: External decoder input for selecting this device.
57	RESET	IS	System Reset: It is a reset input with a 500ns minimum active pulse for internal egisters reset. The configuration registers are unaffected.

FDD

Pin No.	Pin Name	Type	Description
16	nRDD	IS	Read Disk Data: Raw serial disk data coming from disk presents a flux transition on each falling edge.
9	nWDD	OD48	Write Disk Data: Encoded disk data stream for disk write.
10	nWG	OD48	Write Gate: For disk write head operation.
17	nDCHG	IS	Disk Changed: Indicate drive door is open.
14	nWP	IS	Write Protect: For disk status indication on write protection.
13	nTRK0	IS	Track 00: For disk status indication on track 0 being sensed.
12	nIDX	IS	Index Hole: For disk status indication on index hole being sensed.
11	nHSEL	OD48	Head Select: For disk head selection. A logic "1" means side 0 and a logic "0" means side 1.
7	nDIR	OD48	Direction Control: For disk head direction control. A logic "1" means inward motion and a logic "0" means outward motion.
8	nSTEP	OD48	Step Pulse: A pulse sequence output for track-to-track operation.
3,4	nDS[1:0]	OD48	Drive Selects: For disk driver selection.
5,2	nMOE[1:0]	OD48	Motor On: For disk motor control.
18 1	DDEN1 DDEN0	OD48 OD48	Driver Density(Reduce Write Current): Select drive and media. Refer to CR03, CR0B, and CR1F.

Serial port

Pin No.	Pin Name	Type	Description
78 88	SI1 SI2	I	Serial Data In: Received serial data input.
79 89	SO1 SO2	O4	Serial Data Out: Transmit serial data output.
81 91	nRTS1 nRTS2	O4 OT4	Request To Send: Handshake output signals notify modem that the UARTn is ready to transmit data. It can be programmed by writing to rts.CMn_MCR. It will be reset to inactive mode during hardware reset or forced to inactive during loop mode operation.
83 93	nDTR1 nDTR2	O4	Data Terminal Ready: Handshake output signals no tify modem that the UARTn is ready to setup data communication link. It can be programmed by writing to dtr.CMn_MCR. It will be reset to inactive mode during hardware reset or forced to inactive during loop mode operation.
82 92	nCTS1 nCTS2	I	Clear To Send: Han dshake input signals notify UARTn that the modem is ready to receive data. An nCTSn signal state change from low to high after the last CMn_MSR read will set dcts.CMn_MSR to "1". If emsi.CMn_IER is set, it will generate an interrupt when nCTSn changes sta te. The CPU can monitor the status of nCTSn by reading cts. CMn_MSR. The bit is the complement of nCTSn.
80 90	nDSR1 nDSR2	I	Data Send Ready: Handshake input signals notify UARTn that the modem is ready to setup the data communication link. An nDSRn signal stat change from low to high after the last CMn_MSR read will set ddsr. CMn_MSR to "1". If emsi.CMn_IER is set, it will generate an interrupt when nDSRn changes state. The CPU can monitor the status of nDSRn by reading dsr.CMn_MSR. The bit is the complement onDSRn.
85 87	nDCD1 nDCD2	I	Data Carrier Detect: Handshake input signals notify UARTn that carrier signal is detected by the modem. An nDCDn signal state change from low to high after the last CMn_MSR read will set ddcd.CMn_MSR to "1". If emsi.CMn_IER is set, i t will generate an interrupt when nDCDn changes state. The CPU can monitor the status of nDCDn by reading dcd.CMn_MSR. The bit is the complement of nDCDn.
84 86	nRI1 nRI2	I	Ring Indicator: Handshake input signals notify UARTn that the telephone ring signal is d etected by the modem. An nRIn signal state change from low to high after the last CMn_MSR read will set teri.CMn_MSR to "1". If emsi.CMn_IER is set, it will generate an interrupt when nRIn changes state. The CPU can monitor the status of nRIn by reading r i.CMn_MSR. The bit is the complement of nRIn.

Parallel port

Pin No.	Pin Name	Type	Description
[63:66], [68:71]	PD[7:0]	I/O24	Parallel Port Data I/O: The bi-directional parallel port data for data transfer between HOST and peripherals. It contents either address or data in EPP or ECP mode, the data may i nclude RLE data in ECP mode.
61	BUSY	I	Line Busy: A busy signal from printer to indicate printer is not available to receive the new data. The bit nbusy. SPP_SPR is the complement of this input. nWAIT(Wait): In EPP mode, it is active low to indicate the device is ready for the next transfer. BUSY/nPACK(Line Busy/Peripheral Acknowledge): In ECP mode, it is inactive low to indicate the peripheral is ready for the next transfer in the forward direction. It indicates the the data line is ECP command or data in the reverse direction.
62	nACK	I	Acknowledgment: A acknowledge signal from printer to indicate printer has received data and is ready to accept a new data. The bit nack. SPP_SPR directly reflects this signal. INTR(Interrupt): In EPP mode, it is active high with the positive edge triggered for the interrupt signal. nPACK(Peripheral Acknowledgment): In ECP mode, it is active low to indicate valid data being driven by peripheral.
60	PE	I	Paper End: A status signal from printer to indicate the printer is out of paper. The bit pe.SPP_SPR directly reflects this signal. (Same definition as SPP in EPP mode) PERROR/nACKR(PError/nAckReverse): In ECP mode, peripheral uses it to acknowledge a transfer direction change for nRREQ. The direction is forward when asserted, host is then permitted to drive the bus.
59	SLCT	I	Printer Selected Status: A status signal from p inter to indicate the printer has powered on. The bit slct. SPP_SPR directly reflects this signal. (Same definition as SPP in EPP mode) SLCT(Printer Selected Status): In ECP mode, A status signal from printer to indicate it is on-line.
75	nERROR	I	Printer Port Error: A status signal from printer to indicate an error status at the printer. The bit nerr.SPP_SPR directly reflects this signal. (Same definition as SPP in EPP mode) nFAULT/nPREQ(Fault/Peripheral Request): In ECP mode, peripheral uses it to indicate an error interrupt. It is valid only in forward mode. Occasionally, it can be used as a request for reverse transfer.

Pin No.	Pin Name	Type	Description
73	nSLCTIN	OD24 O24	Printer Select Input: This output is the complement of the bit slctin. SPP_CPR to select the printer. nASTB(Address Strobe): This output is used to indicate an address port access in EPP mode.nSLCTIN(Printer Select Input): In ECP mode, it is always deasserted.
74	nINIT	OD24 O24	Printer Initial Output: This output reflects the bit ninit.SPP_CPR to initiate the printer. (Same definition as SPP in EPP mode) nINIT/nRREQ(Initial Output/Reverse Request): In ECP mode, it sets the transfer direct ion. The transfer direction is reversed when it is asserted.
76	nAFD	OD24 O24	Printer Autofeed Output: This output is the complement of the bit autofd.SPP_CPR to control the printer for the auto line feed after each line is printed. nDSTB(Data Strobe): This output is used to indicate a data port access in EPP mode. nAFD/HACK(Autofeed Output/Host Acknowledge): In ECP mode, it is asserted to request a byte from the peripheral by the handshaking with nPACK in the reverse direction. In the forward direction, it indicates the data contents is address or data.
77	nSTB	OD24 O24	Printer Strobe Output: This output is the complement of the bit stb.SPP_CPR to strobe the data into printer. nWRITE(Write): In EPP mode, this output is used to indicate a write operation. nSTB(Strobe Output): In ECP mode, it is used to strobe the address or data into the peripheral on the asserting edge during write operation.

Infra-red interface

Pin No.	Pin Name	Type	Description
88	IRSI1	I	IR Receive Data In 1: IR Receive data input.
89	IRSO1	O4	IR Transmit Data Out 1: IR Transmit data output.
25	IRSI2	I	IR Receive Data In 2: An alternative IR Receive data input.
26	IRSO2	O24	IR Transmit Data Out 2: An alternative IR Transmit data output.

Game port interface

Pin No.	Pin Name	Type	Description
58	nGAMECS	O4	Game Port Select: This is a select signal for game port I/O address corresponding to the setup of CR1E when game port is enabled.

IDE interface

Pin No.	Pin Name	Type	Description
18	nIDERST	OD48	IDE Reset Output: An inverted RESET output for IDE interface.
24	nIDEEN	O24	IDE Enable: This signal is active when the IDE port is enabled and the system is accessing an IDE register.
25	nIDECS0	O24	IDE Chip Select 0: This is a select signal for IDE base address corresponding to the setup of CR21 when IDE port is enabled.
26	nIDECS1	O24P	IDE Chip Select 1: This is a select signal for IDE alternate base address corresponding to the setup of CR22 when IDE port is enabled.

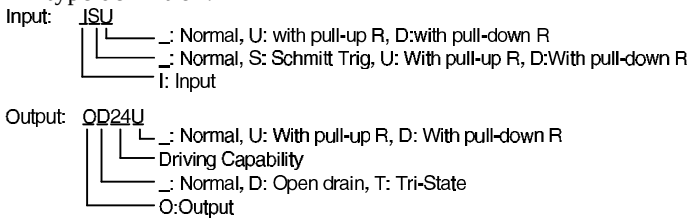
Misc

Pin No.	Pin Name	Type	Description
58	PWRGD	I	Power Good: This signal indicates the power (Vcc) is valid. When it is inactive, all inputs are disconnected, all outputs are tri-stated, and the contents of registers are kept if the Vcc is valid. It sets system into standby mode.
20	CLK24	ICLK	Clock 24MHz: A clock input for whole chip.
94	nPIOCS	OD24U	Programmable I/O Address Decode: This is a select signal for a 1, 8, or 16 byte I/O address corresponding to the setup of CR08 and CR09 when p94s[1:0].CR03 is set to decode mode.
52	DE6	ID	DE6: HT6552 supports an internal pull down input for ISA mode power on setup. System can use an external pull-up resistor to determine the operation mode. At the rising edge of PWRGD, the DE6 input is latched for the mode selection: 0: Normal mode, On-board with no device being active after hardware reset. 1: ISA mode, Adapter based design with default active value after hardware reset.
21	DE7	ID	DE7: HT6552 supports an internal pull down input for Ir mode power on setup. System can use an external pull-up resistor to determine the operation mode. At the rising edge of PWRGD, the DE7 input is latched for the mode selection: 0: Normal mode, polarity of IR receive signal is normal. 1: Inverted mode, polarity of IR receive signal is inverted.
91	SYSOPT	I	Index Base I/O Address Selection: HT6552 supports an input for configuration access setup. System can use an external pull-up/down resistor to determine the address. At the trailing edge of hardware reset, the SYSOPT input is latched for the address selection: 0: Index base I/O address is 3F0h. 1: Index base I/O address is 370h.

Power

Pin No.	Pin Name	Type	Description
15,72	VCC	Power	Vcc Power:
6,47,67,95	GND	Power	Ground:

Note: Pin type definition:



Register Definition

FDC register set

There are status registers, data register, and control registers being built in the FDC subsystem. The address map and the short form of these registers are shown below:

Base I/O Address	Attribute	Abbreviation	Description
fdc+00h			Reserved
fdc+01h			Reserved
fdc+02h	W/R	FDC_DOR	Digital output register
fdc+03h			Reserved
fdc+04h	W R	FDC_DSR FDC_MSR	Data rate select register Main status register
fdc+05h	W/R	FDC_MDR	Main data register
fdc+06h			Reserved
fdc+07h	W R	FDC_CCR FDC_DIR	Configuration control register Digital input register

Default	Reg	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
00	DOR	0	0	moten[1:0]		dmaen	nreset	dvsel[1:0]	
02	DSR	sreset	fdchpd	0	pcomp[2:0]			drsel[1:0]	
—	MSR	rqm	dio	nondma	cmdbsy	dubsy[3:0]			
—	MDR	hd[7:0]							
10b	CCR	—	—	—	—	—	—	drsel[1:0]	
–	DIR	dskchg	—	—	—	—	—	—	—

- Digital output register (FDC_DOR)

This register is used to control the driver Interface. It can not be affected by a software reset. The definition of the bits are:

FDC_DOR: Digital Output Register (fdc+02h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
fdc+02h	WR	0	0	moten1	moten0	dmaen	nreset	dvsel1	dvsel0
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7:6	0	Reserved.
5:4	moten[1:0]	Motor Enable [1:0]: These bits control the related nMOE disk interface. A logic "1" will cause the related output pin to go active.
3	dmaen	FDC DRQ Enable: Writing "0" can disable nDACK and TC inputs, and hold DRQ and IRQ outputs to Hi-Z state. Writing "1" will enable nDACK, TC, DRQ, and IRQ for DMA function.
2	nreset	FDC DOR Reset: A logic "0" written to this bit resets FDC. It will remain active until a logic "1" is written to this bit. The minimum reset duration for the software reset is 100ns. It does not affect FDC_DSR, FDC_CCR, and other bits of this register.
1:0	dvsel[1:0]	Drive Select: These bits are encoded selection bits to select DS0 - DS3. Therefore, only one drive can be accessed at one time.

The access of disk drive can be configured by programming FDC_DOR with the value as below:

Drive	DOR_FDC Value	Drive	DOR_FDC Value
0	1Ch	2	4Eh
1	2Dh	3	8Fh

- Data rate select register (FDC_DSR)

This register is a write-only register. It is used to program the write precompensation, low power mode, software reset, and data rate selection. In PC-AT system, data rate is programmed by using FDC_CCR instead of this register. But, the data rate is set by the recent programming of the FDC_CCR or FDC_DSR. This register is not affected by a software reset. The definition of the bits are:

FDC_DSR: Data Rate Select Register (fdc+04h.w)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
fdc+04h	W	sreset	fdclpd	0	pcomp2	pcomp1	pcomp0	drsel1	drsel0
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7	sreset	FDC Software Reset: This bit has the same function as nreset.FDC_DOR except the polarity. By the way, this bit is self clearing.
6	fdclpd	FDC Low Power Mode: Writing "1" can put FDC into Manual Low Power mode. In this mode, the FDC clock and data separator circuit will be turned off. FDC will leave this mode after software reset or access of the FDC_DR or FEC_MSR (and clear this bit).
5	0	Reserved and read only.
4:2	pcomp[2:0]	FDC Write Precompensation Select: These bits select the value of write precompensation for WDATA. Track 0 is the default starting track for precompensation and can be changed by the configuration command.
1:0	drsel[1:0]	Data Rate Select: These bits control the data rate of the FDC.

- Main status register (FDC_MSR)

This register is a read-only register. It reports the FDC status for the handshaking with system for FDC access. The definition of the bits are:

FDC_MSR: Main Status Register (fdc+04h.r)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
fdc+04h	R	rqm	dio	nondma	cmdbsy	dvbsy3	dvbsy2	dvbsy1	dvbsy0
Reset Default		—	—	—	—	—	—	—	—

Bit	Name	Description
7	rqm	FDC Ready for Access: FDC can be accessed if this bit is "1", otherwise the access is not allowed.
6	dio	FDC Data Transfer Direction: It indicates the data transfer direction when rqm is set. Reading "1" indicates a read operation. "0" is a write.
5	nondma	FDC Non-DMA Operation: It reflects the DMA setup in SPECIFY command and will be set "1" during execution phase of a command. It is for polled transfer and helps to distinguish between the data transfer phase and the reading of result bytes.
4	cmdbsy	FDC Command Progress: This bit indicates the command being processed. It is set after the command bytes being transfer and goes inactive at the end of result phase. If there is no result phase, it will return "0" after the last command byte being transferred.
3:0	dvbsy[3:0]	Drive x Busy: These bits are set to 1s when a driver is in the seek operation, including implied and overlapped seeks and recalibration.

- Main data register (FDC_MDR)

This register is a data I/O register for FDC. All commands, data, and result status are accessed from this register.

FDC_MDR: MainData Register (fdc+05h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
fdc+05h	WR	hd[7:0]							
Reset Default		—	—	—	—	—	—	—	—

- Configuration control register (FDC_CCR)

  This register is a write-only register. It is programmed for data rate selection as the function as drsel[1:0].FDC_DOR. The definition of the bits are:

FDC_CCR: Configuration Control Register (fdc+07h.w)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
fdc+07h	W	—	—	—	—	—	—	drsel1	drsel0
Reset Default		—	—	—	—	—	—	—	—

Bit	Name	Description
7:2	—	Reserved and could not be accessed.
1:0	drsel[1:0]	Data Rate Select: These bits control the data rate of the FDC.

- Digital input register (FDC_DIR)

  This register is a read-only register. It reports the FDC status for the disk changes. The definition of the bits are:

FDC_DIR: Digital Input Register (fdc+07h.r)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
fdc+07h	R	dskchg	—	—	—	—	—	—	—
Reset Default		—	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Bit	Name	Description
7	dskchg	FDD Disk Changed: This bit reflects the opposite value of the nDCHG input.
6:0	—	Reserved and tri-state during read access.

Serial port (UART) register set

There are status registers, data buffer registers, and control registers being built in the UART subsystem. The address map of these registers and the short form is shown below:

Base I/O Address	dlab	Attribute	Abbreviation	Description
cmn+0h	0	W R	CMn_THR CMn_RBR	Transmit Buffer Register Receive Buffer Register
cmn+0h	1	W/R	CMn_DLL	Divisor LSB (Baud Rate Generator)
cmn+1h	0	W/R	CMn_IER	Interrupt Enable Register
cmn+1h	1	W/R	CMn_DLH	Divisor MSB (Baud Rate Generator)
cmn+2h	x	W R	CMn_FCR CMn_IIR	FIFO Control Register Interrupt Identification Register
cmn+3h	x	W/R	CMn_LCR	Line Control Register
cmn+4h	x	W/R	CMn_MCR	Modem Control Register
cmn+5h	x	W/R	CMn_LSR	Line Status Register
cmn+6h	x	W/R	CMn_MSR	Modem Status Register
cmn+7h	x	W/R	CMn_SCR	Scratchpad Register

Note: dlab is the 7th bit of CMn_LCR.

Default	Reg	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
00	THR	Binary							
00	RBR	Binary							
00	IER	0	0	0	0	emsi	elsi	ethrei	erdai
00	DLL	Binary (LSB)							
00	DLH	Binary (MSB)							
02	DLL	sreset	fdclpd	0	pcomp[2:0]			drsel[1:0]	
00	FCR	thr[1:0]		0	0	0	xmtrst	rcvrst	fifoen
01	IIR	fifo		0	0	fifoto	intid1	intid0	noint
00	LCR	dlab	sbc	spb	eps	pen	stb	wls1	wls0
00	MCR	0	0	0	loop	out2	out1	rts	dtr
60	LSR	erfifo	temt	thre	bi	fe	pe	oe	dr
–0	MSR	dcd	ri	dsr	cts	ddcd	teri	ddsr	dcts
00	SCR	Binary							

- Transmit/Receive Buffer Register (CMn_THR/CMn_RBR)

  These registers are used to buffer the transmitting or received data. Bit 0 is transmitted and received first. The definition of the bits are:

CMn_THR: Transmit Buffer Register (com+0h.w/dlab=0)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
cmn+0h	W	Binary							
Reset Default		0	0	0	0	0	0	0	0

CMn_RBR: Receive Buffer Register (com+0h.r/dlab=0)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
cmn+0h	R	Binary							
Reset Default		0	0	0	0	0	0	0	0

- Interrupt enable register (CMn_IER)

  This register is used to control the attribute of interrupt. The definition of the bits are:

CMn_IER: Interrupt Enable Register (com+1h/dlab=0)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
cmn+1h	WR	0	0	0	0	emsi	elsi	ethrei	erdai
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7:4	0	None.
3	emsi	Enable MODEM Status Interrupt: Writing "1" can enable the function. This is caused when one of CMn_MSR bits changes state.
2	elsi	Enable Receiver Line Status Interrupt: Writing "1" can enable the function. The error sources for the interrupt are overrun, parity, framing and break. The CMn_LSR must be read to determine the source.
1	ethrei	Enable Transmit Buffer Register Empty Interrupt: Writing "1" can enable the function.
0	erdai	Enable Received Dtat Available Interrupt: Writing "1" can enable the function and timeout interrupts in the FIFO mode.

- Divisor MSB/LSB register (CMn_DLH/CMn_DLL)

These registers program the 16-bit divisor for baud rate generator. The definition are:

CMn_DLH/DLL: Divisor MSB/LSB Register (com+1/0h/dlab=1)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
cmn+1h	WR	Binary (MSB)							
cmn+0h	WR	Binary (LSB)							
Reset Default		0	0	0	0	0	0	0	0

Below shown is the programming reference table for some specific baud rates, the input clock is 1.8462MHz which is output from 24MHz with a divisor circuit of 13:

Desired Baud Rate	Divisor used to generate 16 x Clock	Percent Error Difference between Desired and Actual
50	2307	0.03
75	1538	0.03
110	1049	0.005
134.5	858	0.01
150	769	0.03
300	384	0.16
600	192	0.16
1200	96	0.16
1800	64	0.16
2000	58	0.5
2400	48	0.16
3600	32	0.16
4800	24	0.16
7200	16	0.16
9600	12	0.16
19200	6	0.16
38400	3	0.16
57600	2	1.6
115200	1	0.16

- FIFO control register (CMn_FCR)

This register is a write-only register and is used to control the FIFO operation. It is not supporting during the DMA operation. The definition of the bits are:

CMn_FCR: FIFO Control Register (com+2h.w)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
cmn+2h	W	thr1	thr0	0	0	0	xmtrst	rcvrst	fifoen
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7:6	thr[1:0]	FIFO Threshold Level: These bits are used to set the trigger level for the RCVR FIFO interrupt. Programming with "00" set 1 byte threshold, "01" for 4 bytes, "10" for 8 bytes, and "11" for 14 bytes.
5:3	0	Reserved and read only.
2	xmtrst	Transmit FIFO Reset: Writing "1" can clear all bytes in the XMIT FIFO and can reset its counter logic to 0. By the way, The shift register is not cleared. It is a self-cleared bit.
1	rcvrst	Receive FIFO Reset: Writing "1" can clear all bytes in the RCVR FIFO and can reset its counter logic to 0. It is a self-cleared bit.
0	fifoen	FIFO Enable: Writing "1" can enable both XMIT and RCVR FIFOs. When write "0" to this bit, it will disable the FIFOs and clear the contents automatically. It should be set to "1" if other bits in this register are set.

- Interrupt identification register (CMn_IIR)

This register is a read-only register and is used to determine the interrupt source and its priority. During CPU accessing the CMn_IIR, UART will freeze all interrupts and keep current status and pending new interrupts until CPU complete the access. The definition of the bits are:

CMn_IIR: Interrupt Identification Register (com+2h.r)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
cmn+2h	R	fifo	fifo	0	0	fifoto	intid1	intid0	noint
Reset Default		0	0	0	0	0	0	0	1

Bit	Name	Description
7:6	fifo	FIFO is Enabled: These bits are set when fifoen.CMn_FCR is set.
5:4	0	None.
3	fifoto	FIFO Time-Out: When in non-FIFO mode, this bit is always "0", In FIFO mode (fifoen.CMn_FCR is set), this bit is set along with bit 2 when a timeout interrupt is pending.
2:1	intid[1:0]	Interrupt Identification: These bits are used to identify the highest priority interrupt indicated below.
0	noint	No Interrupt Pending: There is no interrupt pending when this bit is "1". Otherwise, an interrupt is pending if the bit is "0". It can be used in either a hardwired prioritized or pulled environment.

Below shown is the Interrupt control table for the explanation of fifoto, intid[1:0], noint:

IIR[3:0]				Interrupt set and reset functions			
fifoto	**intid1**	**intid0**	**noint**	**Priority**	**Interrupt type**	**Interrupt source**	**Interrupt Reset Control**
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver line status	Overrun Error, Parity Error, Framing Error, or Break Interrupt.	Reading the CMn_LSR.
0	1	0	0	Second	Received Data Available	Received Data Available.	Read CMn_RBR or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Character have been removed from or input to the RCVR FIFO during the last 4 characters times and there is at least 1 character in it during this time.	Reading the CMn_RBR.
0	0	1	0	Third	CMn_THR Empty	CMn_THR empty.	Reading the CMn_IIR (if source of interrupt) or Writing the CMn_THR.
0	0	0	0	Lowest	MODEM Status	Clear to Send, or Data Set Ready, or Ring Indicator, or Data Carrier Detect	Reading the CMn_MSR.

- Line control register (CMn_LCR)

This register is used to determine the format of serial line. The definition of the bits are:

CMn_LCR: Line Control Register (com+3h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
cmn+3h	WR	dlab	sbc	spb	eps	pen	stb	wls1	wls0
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7	dlab	Divisor Latch Access Bit: It must be set to "1" to access the CMn_DLH/DLL and set to "0" for the access of CMn_RBR/THR/IER.
6	sbc	Set Break Control Bit: When this bit is set "1", the SO output is forced to the spacing or logic "0" state and remains there until the bit is reset. This feature enables the UART to alert a terminal in a communications system.
5	spb	Stick Parity Bit: When this bit is set "1" and pen is enabled, the parity bit is transmitted and then detected by the receiver in the opposite state indicated by eps.
4	eps	Even Parity Select Bit: When pen is set "1", it will generate or check the serial data with odd number of logic "1" if this bit is set to "0", or even parity check rule will be followed for the bit is set to "1".
3	pen	Parity Enable Bit: When it is set, a parity bit is generated for transmit or checked during receiving between the last data word bit and the first stop bit of the serial data.
2	stb	Number of Stop Bit: This bit defines the number of stop bits for transmitting or receiving data. The number of stop bits is depended to wls[1:0] too.
1:0	wls[1:0]	Word Length Select Bits: These bits defines the number of bits in each transmitted or received serial character. Below shown is the different types of character format.

stb	wls1	wls0	Word Length	Number of Stop Bits
0	0	0	5 Bits	1
0	0	1	6 Bits	1
0	1	0	7 Bits	1
0	1	1	8 Bits	1
1	0	0	5 Bits	1.5
1	0	1	6 Bits	2
1	1	0	7 Bits	2
1	1	1	8 Bits	2

- MODEM control register (CMn_MCR)

This register is used to control the interfaces of MODEM or data set or the emulated MODEM mode. The definition of the bits are:

CMn_MCR: MODEM Control Register (com+4h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
cmn+4h	WR	0	0	0	loop	out2	out1	rts	dtr
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7:5	0	None.
4	loop	Loopback Control Bit: When this bit is set "1", the UART will go into diagnostic test. First, SO is set to marking state (Logic "1") and SI is disconnected. Then, the output of Transmitter Shift Register is looped back into the Receiver Shift Register input. In this mode, all MODEM inputs (nCTS, nDSR, nRI, and nDCD) are disconnected, and the four MODEM Control output (nDTR, nRTS, OUT1, and OUT2) are internally connected to the four MODEM Control inputs (nCTS, nDSR, nRI, and nDCD) respectively. In addition, the MODEM control output pins are forced Hi-Z and the transmitted data is received immediately.
3	out2	Output 2: This bit sets to "1" to enable the serial port interrupt. When this bit is "0", the interrupt is disabled with a Hi-Z state.
2	out1	Output 1: For read/write access only.
1	rts	Request To Send: This bit controls the nRTS output. When it is set to "1", the nRTS output is forced to a logic "0", and nRTS will be "1" if the bit is "0".
0	dtr	Data Terminal Ready: This bit controls the nDTR output. If it is set to "1", the nDTR output is forced to a logic "0", and nDTR will be "1" if the bit is "0".

- Line status register (CMn_LSR):

This register reports the status of serial port interface. Bits 7 through 4 are the error conditions that produce a Receiver Line Status Interrupt when any of the corresponding conditions are detected and the interrupt is enabled. The definition of the bits are:

CMn_LSR: Line Status Register (com+5h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
cmn+5h	WR	erfifo	temt	thre	bi	fe	pe	oe	dr
Reset Default		0	1	1	0	0	0	0	0

Bit	Name	Description
7	erfifo	Error in RCVR FIFO: When in non-FIFO mode, this bit is permanently set to "0". In FIFO mode, this bit is set "1", when there is at least one parity error, frame error or break indication in the FIFO. This bit is cleared when this register is read if there are no subsequent errors in the FIFO.
6	temt	Transmitter Empty: This bit is set whenever CMn_THR and CMn_TSR are both empty, and will be reset whenever either CMn_THR or CMn_TSR contains a data character. In the FIFO mode, this bit is set when the CMn_THR and CMn_TSR are both empty. This is a read-only bit.
5	thre	Transmitter Holding Register Empty: This bit indicates the UART is ready to accept a new character for transmission. It is set when a character is transferred from CMn_THR into the CMn_TSR (Transmitter Shift Register), and will be reset whenever Host loads the CMn_THR. In addition, this bit causes the UART to issue an interrupt when ethrei.CMn_IER is set. In the FIFO mode, this bit is set when the XMIT FIFO is empty. It is cleared when at least 1 byte is written to the XMIT FIFO. This is a read-only bit.
4	bi	Break Interrupt: This bit is set whenever the received data is held in the Spacing state ("0") for longer than a full word transmission time (total time of the start bit + data bits + parity bit + stop bits). It is reset when this register is read. In FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received requires the serial data to be "1" for at least 1/2 bit time.
3	fe	Frame Error: This bit is set whenever the received character did not have a valid stop bit, i.e. a spacing level. It is reset when this register is read. In FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The UART will try to re-synchronize after a frame error. To do this, it assumes that the framing error was due to the next start bit, so it samples this "start" bit twice and then takes in the "data" field.
2	pe	Parity Error: This bit is set when the parity of the receive data is detected error, and is reset when this register is read. In FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.
1	oe	Overrun Error: This bit is set immediately to indicates the overrun condition that the data in the CMn_RBR was not read before the next character was transferred into the register. In FIFO mode, it will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred into the FIFO. It is reset when this register is read.
0	dr	Data Ready: This bit is set to "1" when a complete incoming character has been received and transferred into the CMn_RBR or the FIFO. It is reset to "0" by reading all of the data in the CMn_RBR or the FIFO.

- MODEM status register (CMn_MSR)

This register indicates the current state of the control lines from the MODEM (or peripheral device). In addition, there are 4 bits of this register provide change information. These bits are set to "1" when the corresponding control input from the MODEM changes state. Whenever bit 0, 1, 2, or 3 is set to "1", a MODEM Status Interrupt is generated. They are reset to "0" whenever this register is read. The definition of the bits are:

CMn_MSR: MODEM Status Register (com+6h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
cmn+6h	WR	dcd	ri	dsr	cts	ddcd	teri	ddsr	dcts
Reset Default		—	—	—	—	0	0	0	0

Bit	Name	Description
7	dcd	Data Carrier Detect: This bit reflects the complement of nDCD input. If loop.CMn_MCR is set, this bit is equivalent to out2.CMn_MCR.
6	ri	Ring Indicator: This bit reflects the complement of nRI input. If loop.CMn_MCR is set, this bit is equivalent to out1.CMn_MCR.
5	dsr	Data Set Ready: This bit reflects the complement of nDSR input. If loop.CMn_MCR is set, this bit is equivalent to dtr.CMn_MCR.
4	cts	Clear To Send: This bit reflects the complement of nCTS input. If loop.CMn_MCR is set, this bit is equivalent to rts.CMn_MCR.
3	ddcd	Delta Data Carrier Detect: This bit is set when the nDCD input to the chip has changed state. It will be cleared when it is read.
2	teri	Trailing Edge Ring Indicator: This bit is set when the nRI input to the chip has changed from "0" to "1". It will be cleared when it is read.
1	ddsr	Delta Data Set Ready: This bit is set when the nDSR input to the chip has changed state since the last time being read. It will be cleared when it is read.
0	dcts	Delta Clear To Send: This bit is set when the nCTS input to the chip has changed state since the last time being read. It will be cleared when it is read.

- Scratchpad register (CMn_SCR)

This register has no effect on the UART operation but just be a scratchpad register to be used by the programmer to hold data temporarily. The definition of the bits are:

CMn_MCR: Scratchpad Register (com+7h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
cmn+7h	WR	Binary							
Reset Default		0	0	0	0	0	0	0	0

Parallel port (SPP/EPP) register set

There are status registers, data buffer registers, and control registers being built in the parallel port subsystem. The registers, SPP_DPR, SPP_SPR, and SPP_CPR, are available in all modes of parallel port. The others, EPP_ADR, and EPP_DP[0:3], are only available in EPP mode. The address map and the short form of these registers are shown below:

Base I/O Address	Attribute	Abbreviation	Description
lpt+00h	W/R	SPP_DPR	Data Port Register - for all mode
lpt+01h	W/R	SPP_SPR	Status Port Register - for all mode
lpt+02h	W/R	SPP_CPR	Control Port Register - for all mode
lpt+03h	W/R	EPP_ADR	EPP Address Port Register - for EPP mode
lpt+04h	W/R	EPP_DP0	EPP Data Port 0 Register - for EPP mode
lpt+05h	W/R	EPP_DP1	EPP Data Port 1 Register - for EPP mode
lpt+06h	W/R	EPP_DP2	EPP Data Port 2 Register - for EPP mode
lpt+07h	W/R	EPP_DP3	EPP Data Port 3 Register - for EPP mode

Default	Reg	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
00	DPR	Binary							
00	SPR	nbusy	nack	pe	slct	nerr	0	0	tmout
00	CPR	0	0	pcd	irqe	slctin	ninit	autofd	stb
00	ADR	Binary							
00	DP0	Binary							
00	DP1	Binary							
00	DP2	Binary							
00	DP3	Binary							

In addition, there are more registers being defined for ECP operation. The address map and the short form of these registers are shown below:

Base I/O Address	Attribute	Abbreviation	Description
lpt+00h	W/R	ECP_DPR	Data Port Register - for ECP 000-001 mode
lpt+00h	W/R	ECP_AFF	ECP Address FIFO - for ECP 011 mode
lpt+01h	W/R	ECP_SPR	Status Port Register - for ECP all mode
lpt+02h	W/R	ECP_CPR	Control Port Register - for ECP all mode
lpt+400h	W/R	ECP_PDF	ECP Parallel Port Data FIFO - for ECP 010 mode
lpt+400h	W/R	ECP_DFF	ECP Data FIFO - for ECP 011 mode
lpt+400h	R	ECP_TFF	ECP Test FIFO - for ECP 110 mode
lpt+400h	W/R	ECP_CAR	ECP Configuration Register A - for ECP 111 mode
lpt+401h	W/R	ECP_CBR	ECP Configuration Register B - for ECP 111 mode
lpt+402h	W/R	ECP_ECR	ECP Extended Control Register - for ECP all mode

Default	Reg	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
00	DPR	Binary							
00	AFF	rle_a	Binary						
00	SPR	nbusy	nack	perror	slct	nfault	0	0	tmout
00	CPR	0	0	pcd	irqe	slctin	ninit	autofd	stb
00	PDF	Binary							
00	DFF	Binary							
00	TFF	Binary							
00	CAR	0	0	0	1	0	0	0	0
00	CBR	cpress	intvle	0	0	0	0	0	0
00	ECR	ecpm[2:0]			neiren	dmaen	sintr	full	empty

By the way, the pinout assignment of the port connector for each mode is defined below:

Host Connector	Chip Pin Number	Standard	EPP	ECP	
				Compatible	High Speed
1	77	nStrobe	nWrite	nStrobe	nStrobe
[9:2]	[63:66], [68:71]	PData[7:0]	PData[7:0]	PData[7:0]	PData[7:0]
10	62	nACK	Intr	nACK	nACK
11	61	Busy	nWait	Busy	PeriphAck
12	60	PE	(NU)	PError	nAckReverse
13	59	Select	(NU)	Select	Select
14	76	nAutofd	nDatastb	nAutofd	HostAck
15	75	nError	(NU)	nFault	nPeriphRequest
16	74	nInit	(NU)	nInit	nReverseRqst
17	73	nSelectin	nAddrstb	nSelectin	nSelectin

- Data port register (SPP_DPR)

  This register is used to latch the contents of output data bus with the rising edge of nIOW during the write operation. The contents of this register are buffered and output onto the PD[7:0] port. During a read operation in SPP mode, PD[7:0] ports are buffered without latch and output to the HOST. The definition of the bits are:

SPP_DPR: Data Port Register (lpt+0h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+0h	WR	Binary							
Reset Default		0	0	0	0	0	0	0	0

- Status port register (SPP_SPR)

This register is used to latch the status of printer port with the rising edge of nIOR during the read cycle. Most of the bits are read only, except the bit tmout can be written to clear the status in EPP mode. The definition of the bits are:

SPP_DPR: Data Port Register (lpt+0h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+1h	WR	nbusy	nack	pe	slct	nerr	0	0	tmout
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7	nbusy	BUSY Status: This bit reflects the complement of BUSY input. 0: The printer is busy and can not accept a new character. 1: It is ready to accept next new one.
6	nack	ACKNOWLEDGE Status: This bit reflects the nACK input. 0: The printer has received a character and can now accept a new one. 1: It is still processing the last character or has not received the data.
5	pe	Paper End Status: This bit reflects the PE input. 0: Paper present. 1: Paper end.
4	slct	Printer Selected Status: This bit reflects the SLCT input. 0: The printer is not selected. 1: The printer is on line.
3	nerr	ERROR Status: This bit reflects the nERROR input. 0: An error has been detected. 1: No error.
2:1	0	Reserved and read only.
0	tmout	Time Out: This bit is valid in EPP mode only and is set to "1" when a 10us time out has occurred and detected on the EPP bus. It is cleared by a RESET or writing a "1" to this bit. On a write, this bit is cleared by itself with writing a "1", but is no effect on writing a "0" to this bit.

- Control port register (SPP_CPR)

This register is used to control the printer port. The contents will be initialized by RESET. The definition of the bits are:

SPP_CPR: Status Port Register (lpt+2h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+2h	WR	0	0	pcd	irqe	slctin	ninit	autofd	stb
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7:6	0	Reserved and read only.
5	pcd	Parallel Control Direction: This bit is valid in extended mode only (ppmode.CR01 = 0). In printer mode, the direction is always out regardless the state of this bit. In bi-directional mode, "0" means the printer port is in output mode (write), and "1" means the printer port is in input mode (read).
4	irqe	Interrupt Request Enable: This bit enables or disables the interrupt request. When it is high, an interrupt request is generated on the IRQ port by a positive going nACK input. 0: Disable IRQ. 1: Enable IRQ.
3	slctin	Printer Select Input: This bit is inverted and output onto the nSLCTIN output. 0: The printer is not selected. 1: Select the printer.
2	ninit	nInitiate Output: This bit is output onto the nINIT output.
1	autofd	Autofeed: This bit is inverted and output onto the nAFD input. 0: No autofeed. 1: The printer will generate a line feed after each line is printed.
0	stb	Strobe: This bit is inverted and output onto the nSTB output.

- EPP address port register (EPP_ADR)

This register is used to buffer and output the contents onto PD[7:0] with no inverting, the leading edge of nIOW causes an EPP ADDRESS WRITE cycle to be performed, the trailing edge of nIOW latches the data for the duration of the EPP write cycle. During a read operation, PD[7:0] ports are read, the leading edge of nIOR causes an EPP ADDRESS READ cycle to be performed and the data output to the HOST, the deassertion of nAddrstb latches the data of PD[7:0] for the duration of the IOR cycle. This register is only available in EPP mode. It is cleared by RESET. The definition of the bits are:

SPP_CPR: Status Port Register (lpt+2h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+3h	WR	Binary							
Reset Default		0	0	0	0	0	0	0	0

- EPP DATA Port n Register (EPP_DP[0:3])

  These registers are used to buffer and output the contents onto PD[7:0] with no inverting, the leading edge of nIOW causes an EPP DATA WRITE cycle to be performed, the trailing edge of nIOW latches the data for the duration of the EPP write cycle. During a read operation, PD[7:0] ports are read, the leading edge of nIOR causes an EPP DATA READ cycle to be performed and the data output to the HOST, the deassertion of nDatastb latches the data of PD[7:0] for the duration of the IOR cycle. These registers are only available in EPP mode. They are cleared by RESET. The definition of the bits are:

EPP_DP[0:3]: EPP Data Port n Register (lpt+[4:7]h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
pt+[4:7]h	WR	Binary							
Reset Default		0	0	0	0	0	0	0	0

- Data port register-ECP 000 and 001 mode (ECP_DPR)

  This register is used to latch the contents of output data bus with the rising edge of nIOW during the write operation. The contents of this register are buffered and output onto the PD[7:0] port. During a read operation in ECP 000 and 001 mode, PD[7:0] ports are buffered without latch and output to the HOST. The definition of the bits are:

ECP_DPR: Data Port Register-ECP 000 and 001 (lpt+0h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+0h	WR	Binary							
Reset Default		0	0	0	0	0	0	0	0

- ECP address FIFO-ECP 011 mode (ECP_AFF)

  This FIFO is used to store the ECP Address/RLE contents. It will be sent automatically. This register is used only in forward direction. The definition of the bits are:

ECP_AFF: ECP Address FIFO-ECP 011 (lpt+0h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+0h	WR	rle_a	ecpa[6:0]						
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7	rle_a	RLE/Address: This bit defines the contents of ecpa[6:0] is the Run-Length count or ECP port Channel Address. 0: Run-Length Count in ecpa[6:0]. 1: Channel Address in ecpa[6:0].
6:0	ecpa[6:0]	RLE/Address Value: These bits present the RLE Count value or Channel Address Value for the ECP transmission.

- ECP status port register (ECP_SPR)

This register is used to latch the status of printer port with the rising edge of nIOR during the read cycle. Most of the bits are read only. The definition of the bits are:

ECP_SPR: ECP Status Port Register (lpt+1h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+1h	WR	nbusy	nack	perror	slct	nfault	0	0	0
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7	nbusy	nBUSY Status: This bit reflects the complement of BUSY input.
6	nack	nACKNOWLEDGE Status: This bit reflects the nACK input.
5	perror	Paper End Status: This bit reflects the PE input.
4	slct	Printer Selected Status: This bit reflects the SLCT input.
3	nfault	nERROR Status: This bit reflects the nERROR input.
2:0	0	Reserved and read only.

- Control port register (ECP_CPR)

This register is used to control the printer port. The contents will be initialized by RESET. The definition of the bits are:

ECP_CPR: ECP Status Port Register (lpt+2h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+2h	WR	0	0	pcd	irqe	slctin	ninit	autofd	stb
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7:6	0	Reserved and read only.
5	pcd	Parallel Control Direction: This bit is no effect in ECP 000 or 010 mode, and the direction is always out. In all other modes, it is valid and a logic "0" means the printer port is in output mode (write), and "1" means the printer port is in input mode (read).
4	irqe	Interrupt Request Enable: This bit enables or disables the interrupt request. When it is high, an interrupt request is generated on the IRQ port by a positive going nACK input. 0: Disable IRQ. 1: Enable IRQ.
3	slctin	Printer Select Input: This bit is inverted and output onto the nSLCTIN output. 0: The printer is not selected. 1: Select the printer.
2	ninit	nInitiate Output: This bit is output onto the nINIT output.
1	autofd	Autofeed: This bit is inverted and output onto the nAFD input. 0: No autofeed. 1: The printer will generate a line feed after each line is printed.
0	stb	Strobe: This bit is inverted and output onto the nSTB output.

- ECP parallel port data FIFO-ECP 010 mode (ECP_PDF)

  This FIFO is used store the bytes written or DMAed from the system in ECP 010 mode. It is defined only in the forward direction. The FIFO is shared with other FIFO accessing. The definition of the bits are:

ECP_PDF: ECP Parallel Port Data Register-ECP 010 (lpt+400h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+400h	WR	Binary							
Reset Default		0	0	0	0	0	0	0	0

- ECP data FIFO-ECP 011 mode (ECP_DFF):

  This FIFO is used store the bytes written or DMAed from the system or ECP port in ECP 011 mode. It is defined for bi-direction. The FIFO is shared with other FIFO accessing. The definition of the bits are:

ECP_DFF: ECP Data Register-ECP 011 (lpt+400h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+400h	WR	Binary							
Reset Default		0	0	0	0	0	0	0	0

- ECP test FIFO-ECP 110 mode (ECP_TFF)

  This FIFO is used store the bytes accessed or DMAed from the system in ECP 110 mode. It is defined for any direction. Data may not be transferred to printer port. The FIFO is shared with other FIFO accessing. The definition of the bits are:

ECP_TFF: ECP Test Register-ECP 110 (lpt+400h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+400h	WR	Binary							
Reset Default		0	0	0	0	0	0	0	0

- ECP configuration register A-ECP 111 mode (ECP_CAR)

  This register is read only. It is used to indicate this device is an 8-bit implementation. The definition of the bits are:

ECP_CAR: ECP Configuration Register A-ECP 111 (lpt+400h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+400h	R	0	0	0	1	0	0	0	0
Reset Default		0	0	0	1	0	0	0	0

- ECP configuration register B-ECP 111 mode (ECP_CBR)

  This register is used to indicate the compression mode and the IRQ status while system read it back. The definition of the bits are:

ECP_CBR: ECP Configuration Register B-ECP 111 (lpt+401h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+401h	WR	cpress	intvle	0	1	0	0	0	0
Reset Default		0	0	0	1	0	0	0	0

Bit	Name	Description
7	cpress	Compress: This bit is read only and response a low level to indicate this device can not support hardware RLE compression. By the way, hardware RLE decompression is supported.
6	intvle	Interrupt Value: This bit reflects the value on the ISA IRQ line to determine the possible conflicts.
5:0	0	Reserved and read only.

- ECP extended control register (ECP_ECR)

  This register is used to control the ECP extended functions. The definition of the bits are:

ECP_ECR: ECP Extended Control Register (lpt+402h)									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
lpt+402h	WR	ecpm[2:0]			neiren	dmaen	sintr	full	empty
Reset Default		0	0	0	1	0	0	0	0

Bit	Name	Description
7:5	ecpm[2:0]	ECP Mode: These bits are used to select the operation mode in ECP mode. The definition is shown below.
4	neiren	Error Interrupt Enable: This bit control the function of error interrupt. An interrupt will be generated on the falling edge of the nFAULT signal when it is set to "0". The interrupt will be disabled while it is set to "1". This device will still generate a interrupt when nFAULT is asserted and this bit is written from "1" to "0".
3	dmaen	DMA Enable: This bit control the function of DMA. It is set to "1" to enable the DMA function or is set to "0" to disable the DMA function.

Bit	Name	Description
2	sintr	Service Interrupt: This bit is set to "1" to disable the DMA and all of other interrupts, or to indicate the interrupt being serviced. When it is reset to "0", one of three conditions will set it to "1". One is terminal count being reached during DMA (dmaen is set). Second condition is Write Interrupt Threshold being reached or more bytes free in the FIFO when dmaen is "0" and the direction is "0". Last one is Read Interrupt Threshold being reached or more valid bytes to be read from the FIFO when dmaen is "0" and the direction is "1". It must be reset to service the next interrupt.
1	full	FIFO Full: This bit is read only. It indicates FIFO can not accept another data or the FIFO is full when it is "1". It is "0" to indicate the FIFO can accept one or more bytes of data.
0	empty	FIFO Empty: This bit is read only. It indicates FIFO is empty when it is "1". It is "0" to indicate the FIFO contains one or more bytes of data.

The following table shows the ECP mode being set by ecpm[2:0].ECP_ECR:

ecpm[2:0]	Mode Description
000	SPP mode: In this mode, it works like the standard Parallel Port. FIFO is disabled.
001	PS/2 mode: In this mode, it works like the standard PS/2 Parallel Port.
010	Parallel Port Data FIFO mode: In this mode, it works like the standard Parallel Port, but the FIFO is enabled. It can be enabled only when the direction is 0.
011	ECP mode: In this mode, it works in the ECP mode.
100	EPP mode: In this mode, it works like the EPP mode, if the option is set in ppem[1:0]. CR04.
101	Reserved.
110	Test mode: It is used to test FIFO in this mode.
111	Configuration mode: In this mode, ECP_CAR and ECP_CBR can be accessed via the offset address been set in adrp[9:2]. CR23.

Configuration register set

There are configuration registers for chip initial setup. These registers can be accessed via indexed mapping by using index base I/O address 3F0/3F1h or 370/371h after the configuration cycle being enabled. The configuration index address is selected via the external pull-up or pull-down resistor on the pin SYSOPT. In order to enter the configuration cycle system has to write the index I/O port 3F0h or 370h with the data 55h twice consecutively. When the configuration cycle is enabled, system can access these configuration registers via index I/O port 3F0h/3F1h or 370h/371h. When the configuration is completed, system should write the index I/O port with the data AAh to exit the configuration cycle. The address map of these registers is shown below:

Default	Reg	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
28/2A	CR00	valid	0	1	0	fdcpwr	0	ideen[1:0]	
9C	CR01	crlock	0	0	1	ppmode	lptpwr	0	0
88	CR02	cm2pwr	0	0	0	cm1pwr	0	0	0
70	CR03	p94s1	ident	1	p18s	0	p94s0	efdc	p58s
00	CR04	altir	epprev	0	0	00ppfdc[1:0]		ppem[1:0]	
04	CR05	0	0	abswp	dens[1:0]		1	0	0
FF	CR06	1	1	1	1	fd1id[1:0]		fd0id[1:0]	
00	CR07	fdcapd	cm1apd	cm2apd	lptapd	0	0	fboot[1:0]	
00	CR08	adra[7:4]				0	0	0	0
00	CR09	sizea[1:0]		0	0	0	adra[10:8]		
00	CR0A	0	0	0	0	pthr[3:0]			
00	CR0B	0	0	0	0	fd1drt[1:0]		fd0drt[1:0]	
00/01	CR0C	0	0	irmod[2:0]			irdpx	irtxp	irrxp
03	CR0D	Device ID							
00	CR0E	Revision ID							
00	CR0F	0	0	0	0	0	0	0	0
00	CR10	0	0	0	0	0	0	0	0
00	CR11	0	0	0	0	0	0	0	0
00	CR[12:1D]	0	0	0	0	0	0	0	0
80/82	CR1E	adrg[9:4]						sizeg[1:0]	
00	CR1F	0	0	0	0	fd1dt[0:1]		fd0dt[0:1]	
3C/FC	CR20	adrf[9:4]						0	0
3C/7C	CR21	adri[9:4]						0	0
3D/FD	CR22	adre[9:4]						0	1
00/DE	CR23	adrp[9:2]							
00/FE	CR24	adru[9:3]							0
00/BE	CR25	adrv[9:3]							0
00/20	CR26	dmaf[3:0]				dmap[3:0]			
00/65	CR27	irqf[3:0]				irqp[3:0]			
00/43	CR28	irqu[3:0]				irqv[3:0]			
00/01	CR29	0	0	0	0	irqi[3:0]			
—	CR[2A:3F]	Reserved							
00	CR40	regdef	isadef	0	0	0	0	0	0

- Configuration register 00 (CR00)

It is used to control the parallel port power and mode. The definition of the bits are:

CR00: Configuration Register 00 (CSR(00h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(00h)	WR	valid	0	1	0	fdcpwr	0	ideen1	ideen0
Reset Default		0	0	1	0	1	0	0/1	0

Bit	Name	Description
7	valid	Configuration Valid: Control software need to set this bit in the proper time to indicate a valid configuration cycle has occurred. It will be cleared after power up. This bit is used for a status report and do not affect any circuit.
6	0	Reserved and read only.
5	1	Reserved and read only.
4	0	Reserved and read only.
3	fdcpwr	FDC Power Down: This bit is set to "1" to enable the FDC operation. Setting this bit low will force the FDC into low power mode.
2	0	Reserved and read only.
1:0	ideen[1:0]	IDE Enable: These bits control alternate function of the IDE interface as below: 00: IDE, IRSI2, IRSO2, IRQ_H disabled (Default) 01: Reserved (IDE, IRSI2, IRSO2, IRQ_H disabled). 10: IDE enabled (set as default via DRQ_B being pulled up externally). 11: IRSI2, IRSO2, IRQ_H Enabled.

- Configuration register 01 (CR01)

It is used to control the parallel port power and mode. The definition of the bits are:

CR01: Configuration Register 01 (CSR(01h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(01h)	WR	crlock	0	0	1	ppmode	lptpwr	0	0
Reset Default		1	0	0	1	1	1	0	0

Bit	Name	Description
7	crlock	Lock CRx: This bit is set "1" after the power on to enable the accessibility of configuration registers of CR00-CR17. When it is set to "0", those registers can not be accessed and this bit can only be set back to "1" via a hardware reset or power-up reset.
6:5	0	Reserved and read only.
4	1	Reserved and read only.
3	ppmode	Parallel Port Mode: This bit is "1" as the default in the reset and sets the parallel port for Standard Printer Mode. The parallel port is set to Extended Parallel Port Modes when this bit is set to "0".
2	lptpwr	Parallel Port Power Down: This bit is "1" as the default in the reset and sets the parallel port in normal operation mode. A "0" sets the port being in low power mode.
1:0	0	Reserved and read only.

- Configuration register 02 (CR02)

It is used to control the serial port power mode. The definition of the bits are:

CR02: Configuration Register 02 (CSR(02h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(02h)	WR	cm2pwr	0	0	0	cm1pwr	0	0	0
Reset Default		1	0	0	0	1	0	0	0

Bit	Name	Description
7	cm2pwr	UART2 Power Down: This bit is "1" as the default in the reset and sets the Secondary UART port in normal operation mode. A "0" sets the port being in low power mode.
6:4	0	Reserved and read only.
3	cm1pwr	UART1 Power Down: This bit is "1" as the default in the reset and sets the Primary UART port in normal operation mode. A "0" sets the port being in low power mode.
2:0	0	Reserved and read only.

- Configuration register 03 (CR03)

It is used to control the FDC media setup and game port selection. The definition of the bits are:

CR03: Configuration Register 03 (CSR(03h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(03h)	WR	p94s1	ident	mfm	p18s	0	p94s0	efdc	p58s
Reset Default		0	1	1	1	0	0	0	0

Bit	Name	Description
7,2	p94s[1:0]	nPIOCS/IRQ_B Selection: These bits select the function of pin 94 as below: 0x: Tri-state. 10: nPIOCS. 11: IRQ_B.
6	ident	IDENT Selection: This bit is used in conjunction with mfm to select the interface mode of FDC as below: x0: reserved. 01: PS/2 mode(3.5" FDD). 11: AT mode(5.25" FDD).
5	mfm	Fixed to "1" as AT mode, read only.
4	p18s	DDEN1/nIDERST Selection: This bit selects the function of pin 18: 0: DDEN1. 1: nIDERST.
3	0	Reserved and read only.
1	efdc	Enhanced Floppy Mode: This bit is "0" as the default in the reset and sets the FDC to operate as normal mode. An "1" sets the FDC being in enhance mode and will set FDC_TDR to report additional information.
0	p58s	PWRGD/nGAMECS Selection: This bit selects the function of pin 58 as below: 0: PWRGD. 1: nGAMECS.

- Configuration Register 04 (CR04)

It is used to control the parallel port setup and IR port selection. The definition of the bits are:

CR04: Configuration Register 04 (CSR(04h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(04h)	WR	altir	epprev	midi2	midi1	ppfdc1	ppfdc0	ppem1	ppem0
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7	altir	IR ALT I/O: This bit selects the IR output to alter in/out pins as below: 0: use IRSI1/IRSO1. 1: use IRSI2/IRSO2. When it sets "1", it should be combined with ideen[1:0].CR00 being set to "11".
6	epprev	EPP Revision Control: This bit selects the revision of EPP as below: 0: EPP 1.9. 1: EPP 1.7.
5	midi2	UART2 MIDI Clock Control: This bit selects the divisor of UART2 input clock as below: 0: Clock derived by a divisor of 13, normal operation. 1: Clock derived by a divisor of 12, MIDI operation.
4	midi1	UART1 MIDI Clock Control: This bit selects the divisor of UART1 input clock as below: 0: Clock derived by a divisor of 13, normal operation. 1: Clock derived by a divisor of 12, MIDI operation.
3:2	ppfdc[1:0]	Parallel Port FDC Control: These bits control the swap logic of the FDD interface to Printer interface as below: 00: Normal, printer I/F. 01: PPFD1 - one FDD. 10: PPFD2 - two FDD. 11: Reserved.
1:0	ppem[1:0]	Parallel Port Extended Modes Selection: These bits select the extended mode function as below when ppmode.CR01 is set to extended mode. 00: Standard and Bi-directional Modes(SPP, IBM PS/2). 01: EPP mode and SPP. 10: ECP mode (SPP can be selected via ECP_ECR as mode 000) 11: ECP&EPP mode (SPP/EPP can be selected via ECP_ECR as mode 000/100)

- Configuration register 05 (CR05)

It is used to control the FDC swap and density selection. The definition of the bits are:

CR05: Configuration Register 05 (CSR(05h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(05h)	WR	0	0	abswp	dens1	dens0	1	0	0
Reset Default		0	0	0	0	0	1	0	0

Bit	Name	Description
7:6	0	Reserved and read only.
5	abswp	FDD A/B Swap: This bit controls the swap function of drives and nMOE[1:0] of FDC. A high will enable the function.
4:3	dens[1:0]	DENSEL Output Control: These bits control the output of DENSEL as below: 00: Normal, followed with data rate control and drive type control. 01: Reserved. 10: Fixed high. 11: Fixed low.
2	1	Reserved and read only.
1:0	0	Reserved and read only.

- Configuration register 06 (CR06)

It is used to hold the floppy disk drive types. The definition of the bits are:

CR06: Configuration Register 06 (CSR(06h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(06h)	WR	1	1	1	1	fd1id1	fd1id0	fd0id1	fd0id0
Reset Default		1	1	1	1	1	1	1	1

Bit	Name	Description
7:4	1	Reserved and read only.
3:2	fd1id[1:0]	FDD1 type: These bits hold the FDD1 floppy disk drive type.
1:0	fd0id[1:0]	FDD0 type: These bits hold the FDD0 floppy disk drive type.

- Configuration register 07 (CR07)

It is used to control the auto powerdown feature for each subsystem. The definition of the bits are:

CR07: Configuration Register 07 (CSR(07h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(07h)	WR	fdcapd	cm1apd	cm2apd	lptapd	0	0	fboot1	fboot0
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7	fdcapd	FDC Auto Powerdown Mode: This bit enables the FDC auto powerdown feature when sets to high, and disables the feature when low. It is reset by power on reset and hardware reset both.
6	cm1apd	COM1 Auto Powerdown Mode: This bit enables the COM1 auto powerdown feature when sets to high, and disables the feature when low. It is reset by power on reset and hardware reset both.
5	cm2apd	COM2 Auto Powerdown Mode: This bit enables the COM2 auto powerdown feature when sets to high, and disables the feature when low. It is reset by power on reset and hardware reset both.
4	lptapd	Parallel Port Auto Powerdown Mode: This bit enables the parallel port auto powerdown feature when sets to high, and disables the feature when low. It is reset by power on reset and hardware reset both.
3:2	0	Reserved and read only.
1:0	fboot[1:0]	Boot Floppy: These bits defines the boot floppy as below. 0: Drive A. 1: Drive B.

- Configuration register 08 (CR08)

It is the address input of Programmable I/O decoder. The definition of the bits are:

CR08: Configuration Register 08 (CSR(08h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(08h)	WR	adra7	adra6	adra5	adra4	0	0	0	0
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7:4	adra[7:4]	Programmable I/O Address Bit [7:4]: These bits are the lower 4 bits of addresses for the Programmable I/O decoder.
3:0	0	Reserved and read only.

- Configuration register 09 (CR09)

It is the address input and size control of Programmable I/O decoder. The definition of the bits are:

CR09: Configuration Register 09 (CSR(09h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(09h)	WR	sizea1	sizea0	0	0	0	adra10	adra9	adra8
Reset Default		0	0	0	1	0	0	0	0

Bit	Name	Description
7:6	sizea[1:0]	Programmable I/O Configuration Control: These bits control the function and the decode size of Programmable I/O decoder as below:00: Programmable I/O disabled. 01: 1 Byte decode, A[3:0] = 0000b. 10: 8 Byte block decode, A[3:0] = 0xxxb. 11: 16 Byte block decode, A[3:0] = xxxxb.
5:3	0	Reserved and read only.
2:0	adra[10:8]	Programmable I/O Address Bit [10:8]: These bits are the upper 3 bits of addresses for the Programmable I/O decoder.

- Configuration register 0A (CR0A)

It is the address input and size control of Programmable I/O decoder. The definition of the bits are:

CR0A: Configuration Register 0A (CSR(0Ah))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(0Ah)	WR	0	0	0	0	pthr3	pthr2	pthr1	pthr0
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7:4	0	Reserved and read only.
3:0	pthr[3:0]	ECP FIFO Threshold: These bits define the FIFO threshold value for the ECP mode parallel port.

- Configuration register 0B (CR0B)

It is used to hold the floppy disk data rate. The definition of the bits are:

CR0B: Configuration Register 0B (CSR(0Bh))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(0Bh)	WR	0	0	0	0	fd1drt1	fd1drt0	fd0drt1	fd0drt0
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7:4	0	Reserved and read only.
3:2	fd1drt[1:0]	FDD1 Data Rate: These bits hold the FDD1 data rate.
1:0	fd0drt[1:0]	FDD0 Data Rate: These bits hold the FDD0 data rate.

- Configuration register 0C (CR0C)

It is used to define the Ir interface. In addition, this register is reset by the power on reset or a hardware reset. The definition of the bits are:

CR0C: Configuration Register 0C (CSR(0Ch))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(0Ch)	WR	0	0	irmod2	irmod1	irmod0	irdpx	irtxp	irrxp
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7:6	0	Reserved and read only.
5:3	irmod [2:0]	Ir Mode Selection: These bits define Ir mode for UART2 as below:000: Standard (No Ir). 001: IrDA (HP-SIR). 010: ASK-IR@500K. 011: Reserved. 1xx: Reserved.
2	irdpx	Ir Duplex Selection: This bit selects the duplex mode of Ir interface (UART2). 0: Full Duplex. 1: Half Duplex.
1	irtxp	Ir Transmit Polarity: This bit selects the polarity of Ir transmitting (UART2). 0: IRSO output non-inverted. (default) 1: IRSO output inverted.
0	irrxp	Ir Receive Polarity: This bit selects the polarity of Ir Receiving (UART2). 0: IRSI output non-inverted. (default) 1: IRSI output inverted.(default by DRQ_A pull up)

- Configuration register 0D (CR0D)

  It is read only for device ID identification. The definition of the bits are:

CR0D: Configuration Register 0D (CSR(0Dh))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(0Dh)	R	Device ID							
Reset Default		0	0	0	0	0	0	0	0

- Configuration register 0E (CR0E)

  It is read only for revision ID identification. The definition of the bits are:

CR0E: Configuration Register 0E (CSR(0Eh))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(0Eh)	R	Revision ID							
Reset Default		0	0	0	0	0	0	0	0

- Configuration register F-1D (CR[0F:1D])

  These registers are reserved and read as 00h.

- Configuration register 1E (CR1E)

  It is used to define the GAME port address selection. The address can be set to 48 locations with 16-byte boundaries from 100h-3F0h. By the way, nCS = 0 and A10 = 0 are required to qualify the nGAMECS output, and the bit p58s.CR03 can override this register if it selects another output function, PWRGD. The definition of the bits are:

CR1E: Configuration Register 1E (CSR(1Eh))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(1Eh)	WR	adrg9	adrg8	adrg7	adrg6	adrg5	adrg4	sizeg1	sizeg0
Reset Default		1	0	0	0	0	0	0/1	0

Bit	Name	Description
7:2	adrg[9:4]	nGAMECS Address Bit [9:4]: These bits are the upper 6 bits of addresses for the nGAMECS decoder.
1:0	sizea[1:0]	nGAMECS Configuration Control: These bits control the function and the decode size of nGAMECS decoder as below: 00: nGAMECS disabled. 01: 1 Byte decode, A[3:0] = 0001b. 10: 8 Byte block decode, A[3:0] = 0xxxb. 11: 16 Byte block decode, A[3:0] = xxxxb.

- Configuration register 1F (CR1F)

It is used to select the drive type. The definition of the bits are:

CR1F: Configuration Register 1F (CSR(1Fh))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(1Fh)	WR	0	0	0	0	fd1dt0	fd1dt1	fd0dt0	fd0dt1
Reset Default		1	0	0	0	0	0	0/1	0

Bit	Name	Description
7:4	0	Reserved and read only.
3:2	d1dt[0:1]	fFDD1 Drive Type: These bits hold the FDD1 drive type.
1:0	fd0dt[0:1]	FDD0 Drive Type: These bits hold the FDD0 drive type.

- Configuration Register 20 (CR20)

It is used to define the FDC address selection. The address can be set to 48 locations with 16-byte boundaries from 100h-3F0h. By the way, nCS = 0 and A10 = 0 are required to qualify for the registers accesses of FDC. A[3:0] are decoded as 0xxxb. The definition of the bits are:

CR20: Configuration Register 20 (CSR(20h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(20h)	WR	adrf9	adrf8	adrf7	adrf6	adrf5	adrf4	0	0
Reset Default		0/1	0/1	1	1	1	1	0	0

Bit	Name	Description
7:2	adrf[9:4]	FDC Address Bit [9:4]: These bits are the upper 6 bits of addresses for the FDC decoder. It can be set to ISA mode default by pull-up DRQ_B.
1:0	0	Reserved and read only.

- Configuration register 21 (CR21)

It is used to define the IDE interface base address for the control registers (0-7). The address can be set to 48 locations with 16-byte boundaries from 100h-3F0h. System can set adri[9:8] as "00" to disable the decoder. By the way, nCS = 0 and A10 = 0 are required to qualify for the registers accesses of IDE interface. A[3:0] are decoded as 0xxxb. The definition of the bits are:

CR21: Configuration Register 21 (CSR(21h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(21h)	WR	adri9	adri8	adri7	adri6	adri5	adri4	0	0
Reset Default		0	0/1	1	1	1	1	0	0

Bit	Name	Description
7:2	adri[9:4]	IDE Base Address Bit [9:4]: These bits are the upper 6 bits of addresses for the IDE decoder. It can be set to ISA mode default by pull-up DRQ_B.
1:0		Reserved and read only.

- Configuration register 22 (CR22)

It is used to define the alternate IDE interface base address for the control registers (0-7). The address can be set to 48 locations with 16-byte boundaries from 106h-3F6h. System can set adre[9:8] as "00" to disable the decoder. By the way, nCS = 0 and A10 = 0 are required to qualify for the registers accesses of IDE interface. A[3:0] must be decoded as 0110b. The definition of the bits are:

CR22: Configuration Register 22 (CSR(22h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(22h)	WR	adre9	adre8	adre7	adre6	adre5	adre4	0	1
Reset Default		0/1	0/1	1	1	1	1	0	1

Bit	Name	Description
7:2	adri[9:4]	IDE Alternate Base Address Bit [9:4]: These bits are the upper 6 bits of addresses for the IDE decoder. It can be set to ISA mode default by pull-up DRQ_B.
1	0	Reserved and read only.
0	1	Reserved and read only.

- Configuration register 23 (CR23)

It is used to define the parallel port address. When EPP mode is not enabled, the address can be set to 192 locations with 4-byte boundaries from 100h-3FCh. When EPP mode is enabled, it can be set to 96 locations with 8-byte boundaries from 100h-3F8h. System can set adrp[9:8] as "00" to disable the decoder. By the way, nCS = 0 and A10 = 0 are required to qualify for the registers accesses of parallel port when in compatible, bi-directional, or EPP modes (A10 is active when in ECP mode). It can be set to ISA mode default by pull-up DRQ_B. The definition of the bits are:

CR23: Configuration Register 23 (CSR(23h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(23h)	WR	adrp[9:2]							
Reset Default		0/1	0/1	0	0/1	0/1	0/1	0/1	0

- Configuration register 24 (CR24)

It is used to define the UART1 base address. The address can be set to 96 locations with 8-byte boundaries from 100h-3F8h. System can set adru[9:8] as "00" to disable the decoder. By the way, nCS = 0 and A10 = 0 are required to qualify for the registers accesses of UART1. The definition of the bits are:

CR24: Configuration Register 24 (CSR(24h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(24h)	WR	adru9	adru8	adru7	adru6	adru5	adru4	adru3	0
Reset Default		0/1	0/1	0/1	0/1	0/1	0/1	0/1	0

Bit	Name	Description
7:1	adru[9:3]	UART1 Base Address Bit [9:3]: These bits are the upper 7 bits of addresses for the UART1 decoder. It can be set to ISA mode default by pull-up DRQ_B.
0	0	Reserved and read only.

- Configuration register 25 (CR25)

It is used to define the UART2 base address. The address can be set to 96 locations with 8-byte boundaries from 100h-3F8h. System can set adru[9:8] as "00" to disable the decoder. By the way, nCS = 0 and A10 = 0 are required to qualify for the registers accesses of UART2. The definition of the bits are:

CR25: Configuration Register 25 (CSR(25h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(25h)	WR	adrv9	adrv8	adrv7	adrv6	adrv5	adrv4	adrv3	0
Reset Default		0/1	0	0/1	0/1	0/1	0/1	0/1	0

Bit	Name	Description
7:1	adrv[9:3]	UART2 Base Address Bit [9:3]: These bits are the upper 7 bits of addresses for the UART2 decoder. It can be set to ISA mode default by pull-up DRQ_B.
0	0	Reserved and read only.

- Configuration register 26 (CR26)

It is used to define the DMA channels for FDC and parallel port. Any unselected DMA acknowledge output is in tri-state. The definition of the bits are:

CR26: Configuration Register 26 (CSR(26h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(26h)	WR	dmaf3	dmaf2	dmaf1	dmaf0	dmap3	dmap2	dmap1	dmap0
Reset Default		0	0	0	1	0	0	0	0

Bit	Name	Description
7:4	dmaf[3:0]	FDC DMA Channel: These bits defines the selection of DMA channel for FDC as the table shown below. It can be set to ISA mode default by pull-up DRQ_B.
3:0	dmap[3:0]	Parallel Port DMA Channel: These bits defines the selection of DMA channel for parallel port as the table shown below.

dmax[3:0]	DMA Selection
0000	None
0001	DMA_A
0010	DMA_B
0011	DMA_C
Others	Reserved

- Configuration register 2[7:9] (CR2[7:9])

These registers are used to define the IRQ channels for FDC, parallel port, UART1, UART2, and IRQIN. Any unselected IRQ output is in tri-state. The definition of the bits are:

CR27: Configuration Register 27 (CSR(27h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(27h)	WR	irqf3	irqf2	irqf1	irqf0	irqp3	irqp2	irqp1	irqp0
Reset Default		0	0	0	1	0	0	0	0

Bit	Name	Description
7:4	irqf[3:0]	FDC IRQ Channel: These bits defines the selection of IRQ channel for FDC as the table shown below. It can be set to ISA mode default by pull-up DRQ_B.
3:0	irqp[3:0]	Parallel Port IRQ Channel: These bits defines the selection of IRQ channel for parallel port as the table shown below. It can be set to ISA mode default by pull-up DRQ_B.

CR28: Configuration Register 28 (CSR(28h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(28h)	WR	irqu3	irqu2	irqu1	irqu0	irqv3	irqv2	irqv1	irqv0
Reset Default		0	0/1	0	0	0	0	0/1	0/1

Bit	Name	Description
7:4	irqu[3:0]	UART1 IRQ Channel: These bits defines the selection of IRQ channel for UART1 as the table shown below. It can be set to ISA mode default by pull-up DRQ_B.
3:0	irqv[3:0]	UART2 IRQ Channel: These bits defines the selection of IRQ channel for UART2 as the table shown below. It can be set to ISA mode default by pull-up DRQ_B.

CR29: Configuration Register 29 (CSR(29h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(29h)	WR	0	0	0	0	irqi3	irqi2	irqi1	irqi0
Reset Default		0	0	0	0	0	0	0	0/1

Bit	Name	Description
7:4	0	Reserved and read only.
3:0	irqi[3:0]	IRQIN IRQ Channel: These bits defines the selection of IRQ channel for IRQIN as the table shown below. It can be set to ISA mode default by pull-up DRQ_B.

irqx[3:0].CR2[7:9]	IRQ Selection
0000	None
0001	IRQ_A
0010	IRQ_B
0011	IRQ_C
0100	IRQ_D
0101	IRQ_E
0110	IRQ_F
0111	Reserved
1000	IRQ_H
Others	Reserved

- Configuration register 40 (CR40)

  This register is used to indicate the default setup for some specific pins or registers. The terminal status of the pins will reflect to these bits. By setting the external pull-up or not will change the value of this resistors to the ISA default value. The definition of the bits are:

CR40: Configuration Register 40 (CSR(40h))									
Address	Type	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
csr(27h)	R	regdef	isadef	0	0	0	0	0	0
Reset Default		0	0	0	0	0	0	0	0

Bit	Name	Description
7	regdef	Register Definition: This bit defines the power on default of irrxp.CR0C via DRQ_A being pulled up externally or not. The definition is: 0: (Internal pull-down), power-on default of irrxp.CR0C is 0. 1: (External pull-up), power-on default of irrxp.CR0C is 1.
6	isadef	ISA Definitivn: This bit defines the power on default of ideen1.CR00 and CR[20:29] via DRQ_B being pulled up externally or not. The definition is: 0: (Internal pull-down), power-on defaults are set to Normal mode. 1: (External pull-up), power-on defaults are set to ISA mode.
5:0	0	Reserved and read only.

Advanced Information

Definition of DDEN[1:0]

The pins are controlled by several registers and defined as following:

Pin Name	Register					
	p18s.CR03		fdndt[0:1].CR1F			
	0	1	(0,0)	(0,1)	(1,0)	(1,1)
DDEN1	DDEN1	nIDERST	DRATE0	DRATE0	DRATE0	DRATE1
DDEN0	DDEN0	DDEN0	DENSEL	DRATE1	nDENSEL	DRATE0
Note	DDEN[1:0] is defined by fdndt[0:1].CR1F	DDEN1 is set to nIDERST in this mode.	4/2/1MB 3.5" 2/1MB 5.25" 2/1.6/1MB 3.5"		PS/2,	

When the pins are defined as nIDERST and DDEN0, the pin nIDERST is always driven as negated RESET signal of ISA-bus. The pin DDEN0 is then followed with the assignment defined by fdndt[0:1].CR1F as similar as the other case that the pins are defined as DDEN1 and DDEN0. By the way, the assignments of these pins are depended on the value of fdndt[0:1].CR1F being selected currently.

In addition, the functions of DRATE[1:0] and DENSEL are controlled by several registers and defined as following:

* for DENSEL

dens[1:0].CR05		ident.CR03	drate[1:0].DSR/CCR		DENSEL	Definitions
dens1	dens0		drate1	drate0		
0	0	0	1 0 0 1	1 0 1 0	0 0 1 1	PS/2 mode (3.5" FDD).
		1	1 0 0 1	1 0 1 0	1 1 0 0	AT mode (5.25" FDD).
0	1	x	x	x	—	Reserved.
1	0	x	x	x	1	Fixed high output.
1	1	x	x	x	0	Fixed low output.

* for DRATE[1:0]

drate1.DSR/CCR	drate0.DSR/CCR	DRATE1	DRATE0
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Normally, when ident.CR03 is configured as AT mode (5.25" FDD), DENSEL output is high when the data rate is 500Kbps or above, and is low when the data rate is 300Kbps or 250Kbps. If the bit is configured as PS/2 mode (3.5" FDD), DENSEL output is then driven in opposite of the definition in the AT-mode depended on the data rate defined in drate[1:0].DSR/CCR. When the system supports 2MB tape driver or 3-mode FDD, the definition of the data rate is different and is controlled by drt[1:0].CR0B.

The definition of data rate is configured by drt[1:0].CR0B and drate[1:0].DSR/CCR as following:

drt[1:0].CR0B		drate[1:0].DSR/CCR		Data Rate		Note
drt1	drt0	drate1	drate0	MFM	FM	
0	0	1	1	1Mbps	—	360K, 1.2M, 720K, 1.44M, and 00500Kbps250Kbps2.88M Vertical Format
		0	0	500Kbps	250Kbps	
		0	1	300Kbps	150Kbps	
		1	0	250Kbps	125Kbps	
0	1	1	1	1Mbps	—	3-Mode Drive
		0	0	500Kbps	250Kbps	
		0	1	500Kbps	250Kbps	
		1	0	250Kbps	125Kbps	
1	0	1	1	1Mbps	—	2 Mbps Tape
		0	0	500Kbps	250Kbps	
		0	1	2Mbps	—	
		1	0	250Kbps	125Kbps	
1	1	x	x	—	—	Reserved

When system is set to AT mode, 3-mode drive supporting, i.e. drt[1:0].CR0B= (0,1), the FDD can be configured as 300 rpm, 500Kbps, 2/1MB mode (traditional 3.5" FDD) by setting DENSEL to high. In this case, drate[1:0].DSR/CCR need to be set to (0,0). In the other case, 360rpm, 500Kbps, 1.6MB mode, DENSEL must be low and drate[1:0].DSR/CCR need to be set to (0,1). Below shown is the format control of the 3-mode FDD:

FD Type	Formatted	Density	Motor Speed	Data Rate	DENSEL	HD
2MB	1.44MB	2HD	300rpm	500Kbps	1	1
1.6MB	1.2MB	2HD	360rpm	500Kbps	0	1
1MB	720KB	2DD	300rpm	250Kbps	—	0

Note: HD input is unused on the FDD interface.

FDC port swapping

Programming ppfdcits of CR04 with 01/10 will swap the FDD I/F to parallel port. There are two kinds of swap mode. One is B-disk swap only (PPFD1 mode), the other one is two disk swap (PPFD2 mode). When the swap is enabled, parallel port can not be used as normal until the mode has been reset. Write of SPP_CPR is inhibited, but SPP_DPR can be accessible with no meaning. In addition, the status lines of LPT are stuck on the specific value for read back and the read back of SPP_CPR will be bypassed to a guided register for responding "Cable not connected". In PPFD1 mode, nSTB and PD6 signal are set as input for dummy, and the FDC status inputs from both connectors (FDD and LPT) are combined internally. In PPFD2 mode, nSTB and PD6 are changed to output for the second disk, and the pins of FDC interface are tri-stated for disable. The related system pinouts or registers for parallel port during swap mode are defined as no operation (inactive) as following:

Pinout	Assignment	Register	Assignment (On Read)
nDACK_lpt	Keep the same status	SPP_DPRData Reg	last SPP_DPR(write)
DRQ_lpt	! ECP: Hi-ZECP & dmaen: 0ECP & ! dmaen:Hi-Z	SPP_CPRControl Reg	"Cable not connected", means: strobe, autofd, slc= 0 ninit= 1
IRQ_lpt	Hi-Z or 0, depending on setting	SPP_SPRStatus Reg	nbusy, pe, slct= 0nack, nerr =1

The interface pinouts of FDD as reassigned as following:

Connector Pin No.	Chip Pin No.	Spp Mode Pin Name	Pin Attribute	FDC Swap Pin Name	Pin Attribute
1	77	nSROTBE	I/O	(nDS0)	I/(O)
2	71	PD0	I/O	nIDX	I
3	70	PD1	I/O	nTRK0	I
4	69	PD2	I/O	nWP	I
5	68	PD3	I/O	nRDD	I
6	66	PD4	I/O	nDCHG	I
7	65	PD5	I/O		I
8	64	PD6	I/O	(nMOE0)	I/(O)
9	63	PD7	I/O		I
10	62	nACK	I	nDS1	O
11	61	BUSY	I	nMOE1	O
12	60	PE	I	nWDD	O
13	59	SLCT	I	nWG	O
14	76	nAFD	I/O	DENSEL	O
15	75	nERROR	I	nHSEL	O
16	74	nINIT	I/O	nDIR	O
17	73	nSLCTIN	I/O	nSTEP	O

( ): additional assignment in PPFD2 mode.

Power management

There are two kinds of power management. The first one is auto-powerdown mode, the other one is direct power down mode.

Using auto-powerdown mode can save power during the normal operation. In this mode each subsystem can monitor the system accesses and the status from target interface to decide to enter the powerdown mode and can be recovered immediately while system accesses the subsystem or some specific status from target interfaces. The status of each subsystem is software transparency for system power management. In addition, the register sets are unchanged, and most of the related interface are still active except some control pins.

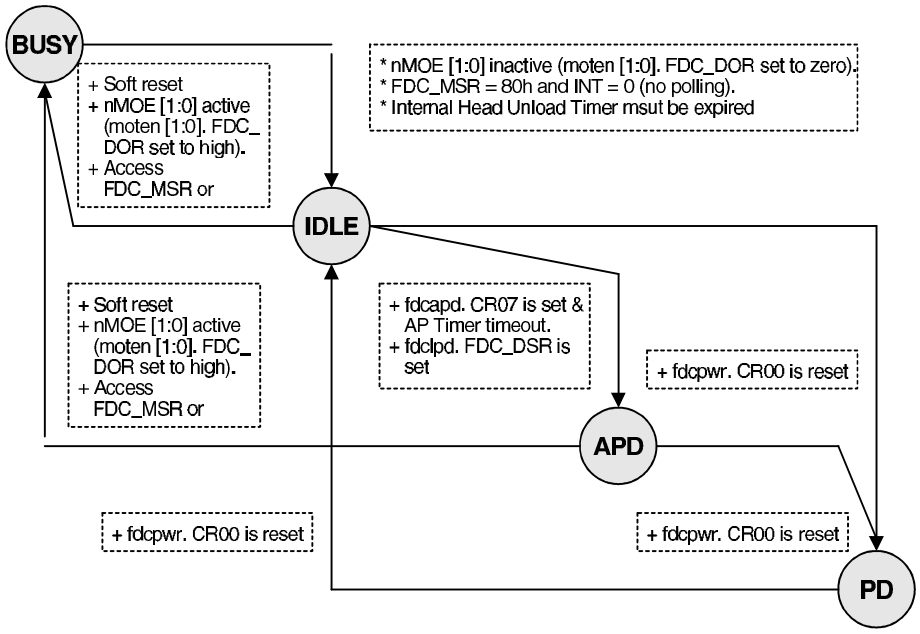
For the implementation of system power management, direct powerdown mode can be used for the control transparency by system power management unit. In the direct power down mode, subsystems are controlled via setting or clearing the related registers for function disabling or enabling. Eventually, the register contents are keep unchanged. But for the consistency of the system setting for reconfigurable subsystem function, we recommend system should configure the related subsystem again after the subsystem being set to exit direct power down mode, except the configuration is the same as the previous setting and the chip power is still available during the mode changes. In addition, the related interface pins are mostly being turned off, except some status signals.

- FDC power management
  - Description:

Mode	Entry	Pri	Functions	Exit	Functions
Direct	Reset fdcpwr.CR00 then monitor the status of FDC till IDLE or APD.	H	- Set status to PD. - Disable clock, DDS and most of block. - Registers set to RO and keep the same contents. - Input: All inactive. - Output: All tri-state.	Set fdcpwr.CR00	- Set status back to IDLE. - All functions recovery. - Recover the auto power down mode if the mode is set before. But reset the fdclpd.FDC_DSR if the mode is set before.

Mode	Entry	Pri	Functions	Exit	Functions
DSR	Set fdclpd. FDC_DSR then monitor the status of FDC till IDLE or APD.	M	- Set status to APD. - Disable the APD mode if the mode is set. - Disable clock and DDS. - Registers keeps the same contents. - Input: All active - Output: Tri-state: nWE, nMOE[0:1], nWRDATA, DS[0:1]. Active: nHSEL, nSTEP, nDIR, DDEN0.	Access FDC_MSR or FDC_DR, or doing a software reset via FDC_DOR/ FDC_DSR, or enable one of the moten[1:0].FDC _DOR	- Set status to BUSY. - All functions recovery. - Recover the auto power down mode if the mode is set before. But reset the fdclpd. FDC_DSR if the mode is set before.
Auto	Set fdcapd.CR07 then monitor the IDLE state: - nMOE[1:0] inactive, moten[1:0]. FDC_DOR set to zero. - State machine is idle, FDC_MSR= 80h and INT=0 (no polling). - Internal Head Unload Timer must be expired. Then check APD Timer (10 ms) is timeout. The timer is reset for any accesses of FDC_MSR or FDC_DR during the count down.	L	- Set status to APD. - Disable clock and DDS. - Registers keeps the same contents. - Input: All active - Output: Tri-state: nWE, nMOE[0:1], nWRDATA, DS[0:1]. Active: nHSEL, nSTEP, nDIR, DDEN0.	Access FDC_MSR or FDC_DR, or doing a software reset via FDC_DOR/ FDC_DSR, or enable one of the moten[1:0]. FDC_DOR	- Set status back to IDLE. - All functions recovery.

* State diagram



Notice:

While system changes the state from APD state to BUSY state, fdclpd.FDC_DSR will be reset automatically. Eventually, fdcapd.CR07 is keep unchanged during the changes.

The status of state will be output to the power management for the power control.

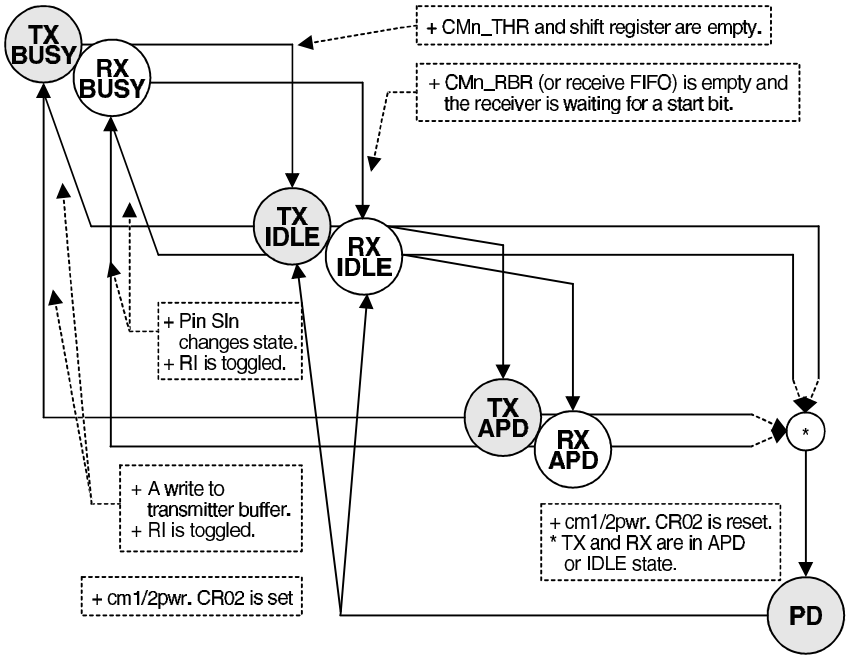
In the APD state, system interface input pins are kept unchanged, output pins are kept unchanged with no operation (i.e. IRQ_FDC and DRQ_FDC are low). In the PD state, system interface input pins are the same as APD state, but IRQ_FDC and DRQ_FDC is floated.

- Serial port power management

  * Description

Mode	Entry	Pri	Functions	Exit	Functions
Direct	Reset cm1/2pwr. CR02 then monitor the status of COM1/2 till transmitter and receiver are all be in IDLE or APD state.	H	- Set status to PD. - Disable clock and most of block. - Registers set to RO and keep the same contents. - Input: All inactive. - Output: Inactive.	Set cm1/2pwr.CR02	- Set status back to IDLE. - All functions recovery. - Recover the auto power down mode if the mode is set before.
Auto	Set cm1/2apd.CR07 then monitor the IDLE state of transmitter or receiver: a. Transmitter: - CMn_THR and shift register are empty. b. Receiver: - CMn_RBR (or receive FIFO) is empty, and the receiver is waiting for a start bit.	L	- Set status to APD. - Disable clock. - Registers keeps the same contents. - Input: All active but gated, except RI and SIn. - Output: Inactive.	a. A write to the transmitter buffer. b. Pin SIn changes state. c. RI input is toggled.	a. Transmit recovery: - Set transmit status to BUSY. - Recover transmitter b. Receive recovery: - Set receive status to BUSY. - Recover receiver. c. All recovery: - Set status back to BUSY. - All functions recovery.

* State diagram



Notice:

System does not change the output pins to tri-state during the power down mode in order to avoid the harzad state on buffer chip.

RI interrupts are kept valid and transitions when nRIn inputs changes during auto powerdown mode.

- Parallel Port power management

  * Description

Mode	Entry	Pri	Functions	Exit	Functions
Direct	Reset lptpwr.CR01.	H	- Disable clock and most of block. - Registers set to RO and keep the same contents. - Input: All inactive. - Output: All tri-state.	Set lptpwr.CR01	- All functions recovery. - Recover the auto power down mode if the mode is set before.
Auto	Set lptapd.CR07 then check the configuration status of EPP and ECP: a. EPP: + EPP is not enabled in the configuration registers. + EPP is not selected through ecr while in ECP mode. b. ECP: + ECP is not enabled in the configuration registers. + SPP, PS/2 Parallel port or EPP mode is selected through ecr while in ECP mode.	L	- Disable EPP or ECP clock. - Registers keeps the same contents. - Input: Active. - Output: Active.	+ Reset lptapd. CR07 + ECP mode is changed through ecr register. + The parallel port mode is changed via the configuration register.	+ All functions recovered if reset lptapd. CR07 + Recover related block if it is activated via the reconfiguration.

Notice:

This block does not support status outputs for system request. The power status can be identified via reading back lptpwr.CR01 or lptapd.CR07

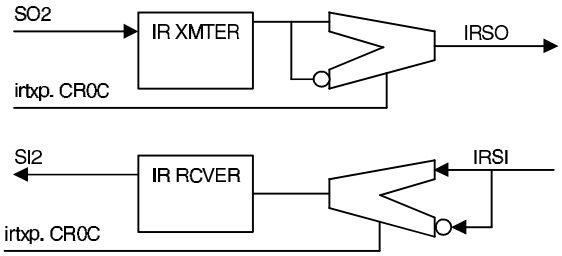
MISC

- Application notice:

  For the completion of power on initialization, PWRGD should be connected to system power good signal correctly. If the pin is failed to connect with power good signal, the power on initialization will be configured incorrectly. In such case, we recommend that using BIOS reconfiguration with the default value for all of the configuration registers is the best way to avoid the potential conflictions.

- The polarity control of Ir-DA interface

  For the ease of IR setup, we can use an external pull up resistor to put on the DRQ_A pin. It will reflect to the bit 7 of Holtek private setup register, regdef.CR40, for cold start setup and enable the internal control logic for the polarity of Ir-DA interface. When it is enabled, the default value of irrxp.CR0C is changed from 0 to 1 after cold reset, and the polarity of IR receiver is changed.



Operational Descriptions

DC characteristics

Buffer Type	Symbol	Min.	Typ.	Max.	Unit	Parameter	Test Condition
Power	V_{CC}	4.75		5.25	V	Power Supply,	
I Normal Input	V_{IL}	-0.5		0.8	V	Low level input	TTL level
	V_{IH}	2.0		5.5	V	High level input	TTL level
	I_{IL}	-10		+10	μA	Low input leakage	Vin= GND
	I_{IH}	-10		+10	μA	High input leakage	Vin= V_{CC}
ID Input with pull-down	V_{IL}	-0.5		0.8	V	Low level input	TTL level
	V_{IH}	2.0		5.5	V	High level input	TTL level
	I_{IL}	-10		+10	μA	Low input leakage	Vin= GND
	I_{IH}	-10		+10	μA	High input leakage	Vin= V_{CC}
IS Input schmitt- trigger	V_{IL}	-0.5		0.8	V	Low level input	TTL level
	V_{IH}	2.0		5.5	V	High level input	TTL level
	I_{IL}	-10		+10	μA	Low input leakage	Vin= GND
	I_{IH}	-10		+10	μA	High input leakage	Vin= V_{CC}
O4 4mA output	V_{OL}			0.4	V	Low level output	I_{OL}=4mA
	V_{OH}	2.4			V	High level output	I_{OH}=4mA
	I_{OL}	-10		+10	μA	Low output leakage	Vin= GND
	I_{OH}	-10		+10	μA	High output leakage	Vin= V_{CC}
OT4 4mA output with Tri-state	V_{OL}			0.4	V	Low level output	I_{OL}=4mA
	V_{OH}	2.4			V	High level output	I_{OH}=4mA
	I_{OL}	-10		+10	μA	Low output leakage	Vin= GND
	I_{OH}	-10		+10	μA	High output leakage	Vin= V_{CC}
OD8U 8mA output open-drain with pull-up	V_{OL}			0.4	V	Low level output	I_{OL}=8mA
						,	
	I_{OL}	-10		+10	μA	Low output leakage	Vin= GND
	I_{OH}	-10		+10	μA	High output leakage	Vin= V_{CC}
O24 24mA output	V_{OL}			0.4	V	Low level output	I_{OL}=24mA
	V_{OH}	2.4			V	High level output	I_{OH}=24mA
	I_{OL}	-10		+10	μA	Low output leakage	Vin= GND
	I_{OH}	-10		+10	μA	High output leakage	Vin= V_{CC}

Buffer Type	Symbol	Min.	Typ.	Max.	Unit	Parameter	Test Condition
O24P 24mA output	V_{OL}			0.4	V	Low level output	I_{OL}=24mA
	V_{OH}	2.4			V	High level output	I_{OH}=24mA
	I_{OL}	–10		+10	μA	Low output leakage	Vin= GND
	I_{OH}	–10		+10	μA	High output leakage	Vin= V_{CC}
OD24 24mA output open-drain	V_{OL}			0.4	V	Low level output	I_{OL}=24mA
	I_{OL}	–10		+10	μA	Low output leakage	Vin= GND
	I_{OH}	–10		+10	μA	High output leakage	Vin= V_{CC}
OD24U 24mA output open-drain	V_{OL}			0.4	V	Low level output	I_{OL}=24mA
	I_{OL}	–10		+10	μA	Low output leakage	Vin= GND
	I_{OH}	–10		+10	μA	High output leakage	Vin= V_{CC}
OD48 48mA output open-drain	V_{OL}			0.5	V	Low level output	I_{OL}=48mA
	I_{OL}	–10		+10	μA	Low output leakage	Vin= GND
	I_{OH}	–10		+10	μA	High output leakage	Vin= V_{CC}

AC Characteristics

FDC: Data rate=1000/500/300/250 KB/SEC

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
T_{AR}	HA[10:0], AEN, nDACK Setup time to nIOR ↓	—	25	—	—	ns
T_{RA}	HA[10:0], AEN, nDACK hold time from nIOR ↑	100pf Loading	0	—	—	ns
T_{RR}	nIOR width	100pf Loading	200	—	—	ns
T_{FD}	Data access time from nIOR ↓	100pf Loading	—	—	80	ns
T_{DH}	Data hold time from nIOR ↓	—	10	—		ns
T_{DF}	HD to float from nIOR ↑	—	10	—	50	ns
T_{RI}	IRQ Delay from nIOR ↑	—	—	—	360/ 570/ 675	ns
T_{AW}	HA[10:0], AEN, nDACK setup time to nIOW ↓	—	25	—	—	ns
T_{WA}	HA[10:0], AEN, nDACK hold time from nIOW ↑	—	0	—	—	ns
T_{WW}	nIOW width	—	200	—	—	ns
T_{DW}	Data setup time to nIOW ↑	—	60	—	—	ns
T_{WD}	Data hold time from nIOW ↑	—	0	—	—	ns
T_{WI}	IRQ delay from nIOW ↑	—	—	—	360/ 570/ 675	ns
T_{MCY}	DMA cycle time	—	27	—	—	μs
T_{AM}	DMA reset delay time from nDACK ↓	—	—	—	50	ns
T_{MA}	DRQ to nDACK delay	—	0	—	—	ns
T_{AA}	nDACK width	—	260/ 430/ 510	—	—	ns
T_{MR}	nIOR delay from DRQ	—	0	—	—	ns
T_{MW}	nIOW dleay from DRQ	—	0	—	—	ns
T_{MRW}	nIOW or nIOR response time from DRQ	—	—	—	12/ 20 24	μs
T_{TC}	TC width	—	135/ 220/ 260	—	—	ns

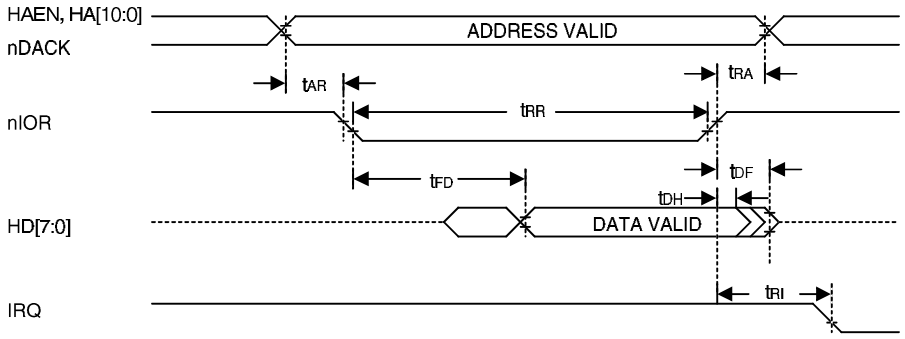
Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
T_{RST}	RESET width	—	1.8/ 3.0/ 3.5	—	—	µs
T_{IDX}	nIDX width	—	0.5/ 0.9/ 1.0	—	—	µs
T_{DST}	nDIR setup time to nSTEP	—	1.0/ 1.6/ 2.0	—	—	µs
T_{STD}	nDIR hold time from nSTEP	—	24/ 40/ 48	—	—	µs
T_{STP}	nSTEP pulse width	—	6.8/ 11.5/ 13.8	7.0/ 11.7/ 14	7.2/ 11.9/ 14.2	µs
T_{SC}	nSTEP cycle time	—	**	**	**	µs
T_{WDD}	nWDD pulse width	—	37/ 100/ 188/ 225	62/ 125/ 210/ 250	87/ 150/ 235/ 275	ns
T_{WPC}	Write Precompensation	—	37/ 100/ 188/ 225	62/ 125/ 210/ 250	87/ 150/ 235/ 275	µs

Notes:

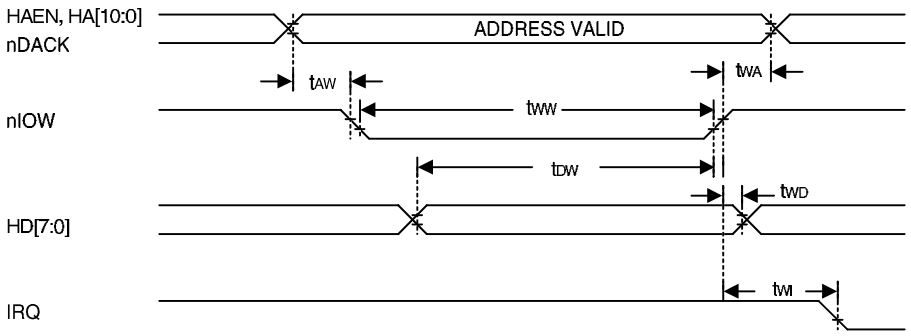
* Typical nsvalues for TA=25°C and nominal value for supply voltage.

** Programmable from 2ms to 32ms in 2ms increments.

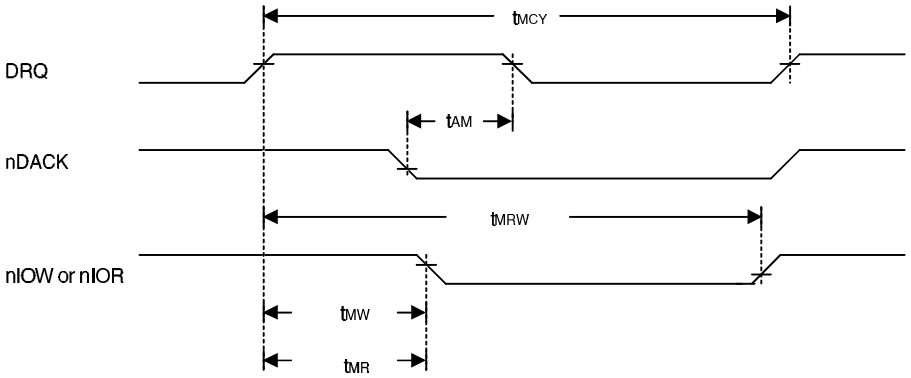
• Processor read operation



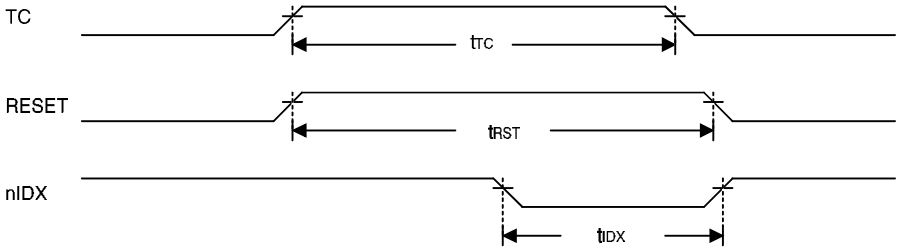
• Processor write operation



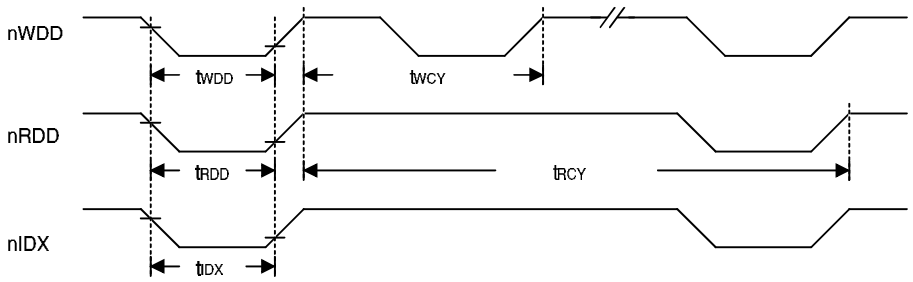
• DMA operation



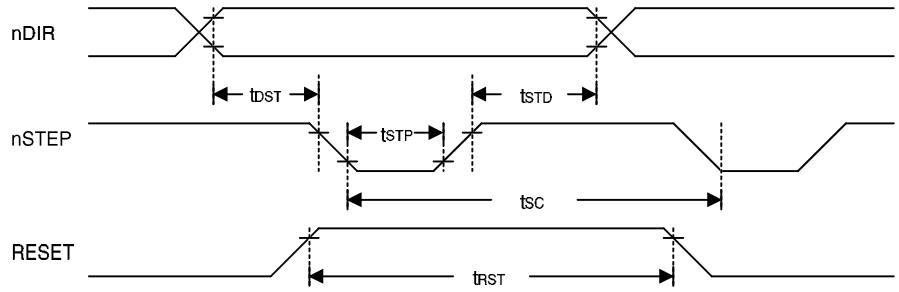
• Terminal count



• FDD write/read operation



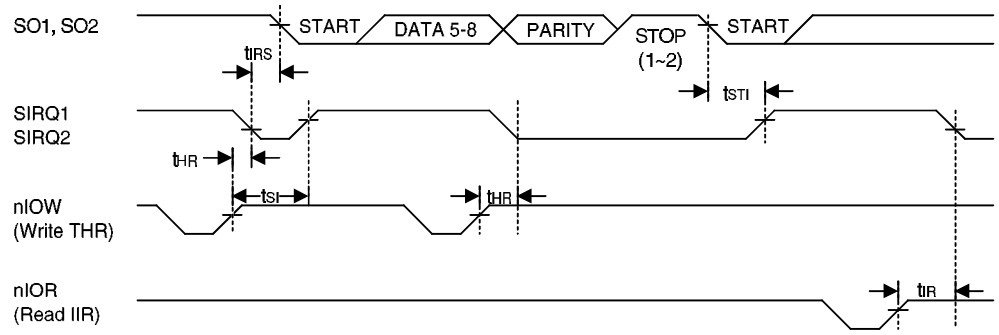
• Seek operation



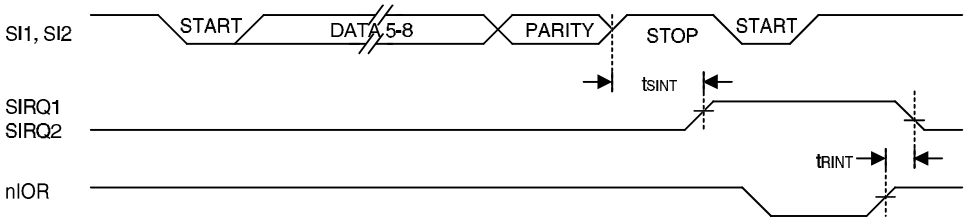
UART

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{IRS}	Delay from initial IRQ reset to transmit start	—	1/16	—	8/16	Baud Rate
T_{STI}	Delay from stop to interrupt	—	9/16	—	—	Baud Rate
T_{HR}	Delay from nIOW to reset interrupt	100pf Loading	—	—	175	ns
T_{SI}	Delay from initial nIOW to interrupt	—	9/16	—	16/16	Baud Rate
T_{IR}	Delay from nIOR to reset	100pf Loading	—	—	1	ns
T_{SINT}	Delay from stop to set interrupt	—	—	—	1/2	Baud Rate
T_{RINT}	Delay form nIOR reset interrupt	100pf Loading	—	—	250	ns
T_{MWO}	Delay from nIOW to output	100pf Loading	—	—	200	ns
T_{SIM}	Set interrupt delay from MODEM input	100pf Loading	—	—	250	ns
T_{RIM}	Reset interrupt Delay from nIOR	100pf Loading	—	—	250	ns
N	Baud rate divisor	100pf Loading	—	—	$2^{16}-1$	unit

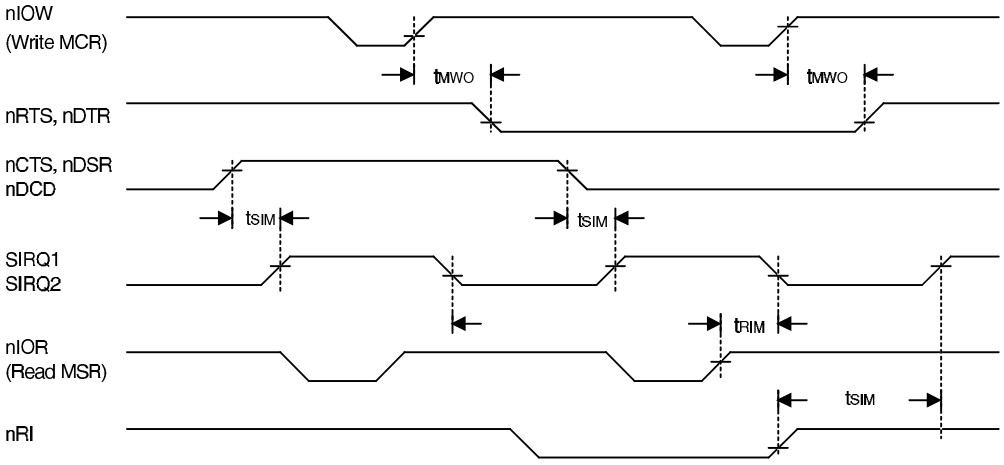
• Transmitter timing



• Receiver timing



• MODEM control timing

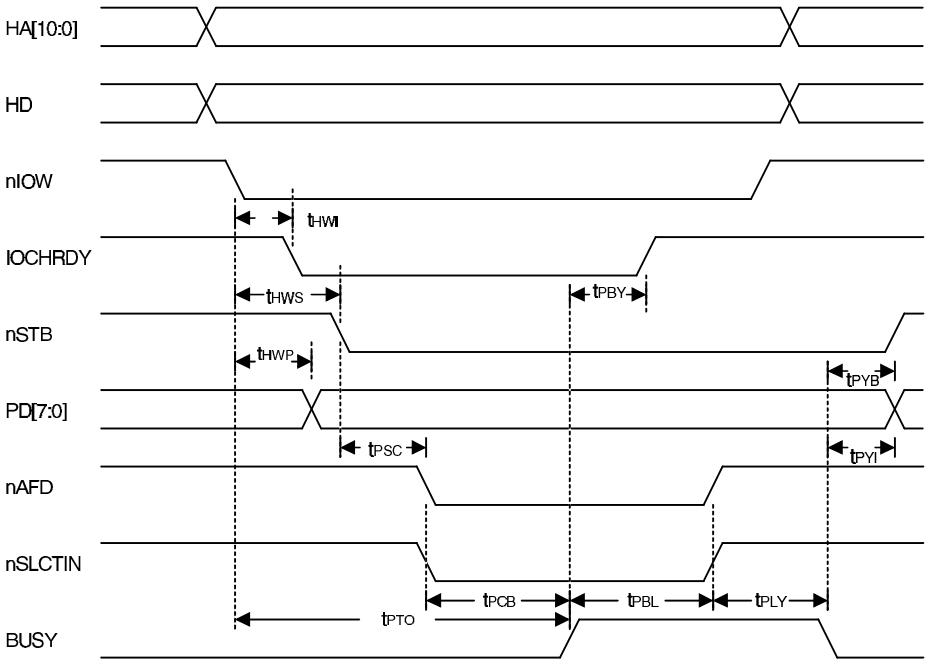


Print

- EPP address or data write cycle timing

	Parameter	Min.	Max.	Units	Notes
t_{HWI}	nIOW asserted to IOCHRDY asserted	10	80	ns	
t_{HWS}	nIOW asserted to nSTB asserted	140	240	ns	
t_{HWP}	nIOW asserted to PD [7:0] valid		210	ns	
t_{PTO}	time out	10	12	μs	
t_{PSC}	nSTB asserted to nAFD, nSLCTIN asserted	70	80	ns	
t_{PCB}	nAFD, nSLCTIN asserted to BUSY asserted	0	10	μs	
t_{PBY}	BUSY asserted to IOCHRDY deasserted	220	290	ns	1
t_{PBL}	BUSY asserted to nAFD, nSLCTIN deasserted	280	350	ns	1
t_{PLY}	nAFD, nSLCTIN deasserted to BUSY deasserted	0			
t_{PYB}	BUSY deasserted to nSTB deasserted	280	350	ns	1
t_{PYI}	BUSY deasserted to PD [7:0] invalid		350	ns	1

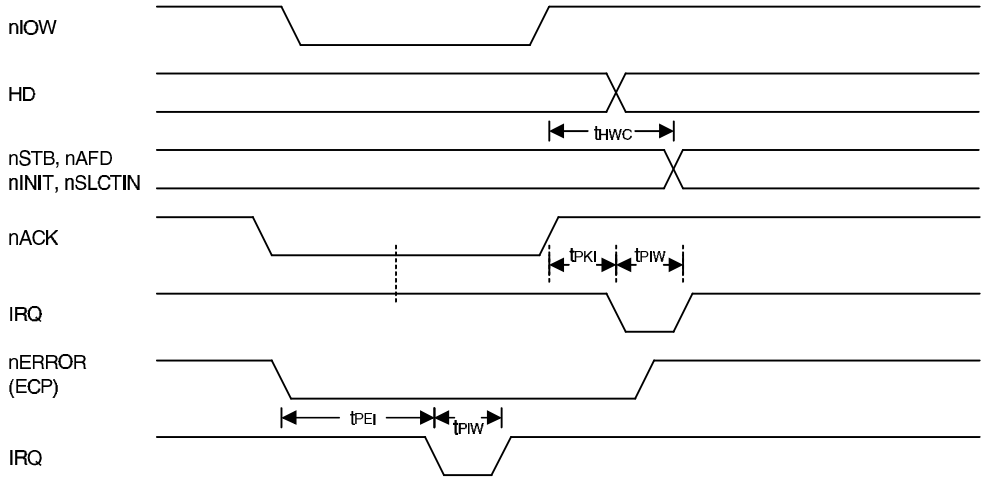
BUSY must be filtered to compensate for ringing on the parallel bus cable. BUSY is considered to have settle after it does not transition for a minimum of 210 μs.



• Parallel port timing

	Parameter	Min.	Max.	Units	Notes
t_{HWC}	nSTB, nAFD, nINIT, nSLCTIN delay from nIOW inactive		400	ns	
t_{PKI}	IRQ delay from nACK		1.25	μs	
t_{PIW}	IRQ active low pulse width	100	200	ns	1
t_{PEI}	IRQ delay from nERROR		140	ns	

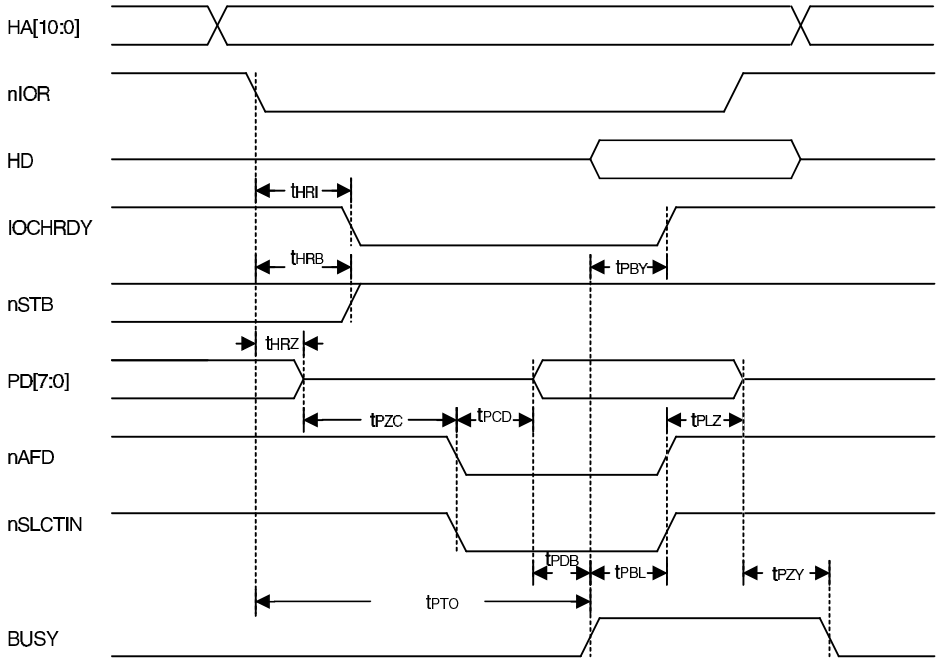
The IRQ pulse width is in the range: 300~400ns when operating in ECP interrupt I/O or DMA I/O.



• EPP address or data READ cycle timing

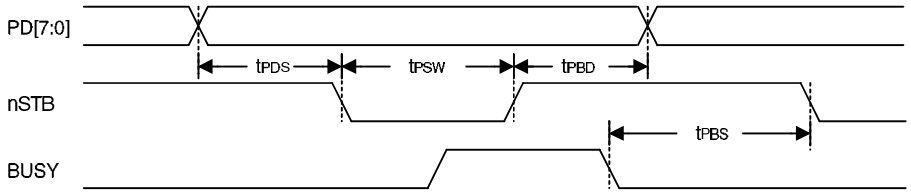
	Parameter	Min.	Max.	Units	Notes
t_{HRI}	nIOR asserted to IOCHRDY asserted	0	80	ns	
t_{HRB}	nIOR asserted to nSTB deasserted	0		ns	2
t_{HRZ}	nIOR asserted to PD[7:0] Hi-Z	0	70	ns	
t_{PTO}	time out	10	12	μs	
t_{PZC}	PD[7:0] Hi-Z to nAFD, nSLCTIN asserted	140	210	ns	
t_{PCD}	nAFD, nSLCTIN to PD[7:0] valid	0		ns	
t_{PDB}	PD[7:0] valid to BUSY asserted	0		ns	
t_{PBY}	BUSY asserted to IOCHRDY deasserted	280	350	ns	1
t_{PBL}	BUSY asserted to nAFD, nSLTIN deasserted	350	420	ns	1
t_{PLZ}	nAFD, nSLCTIN deasserted to PD[7:0] Hi-Z	0		ns	
t_{PZY}	PD[7:0] Hi-Z to BUSY deasserted	0		ns	

BUSY is considered to have settled after it does not transition for a minimum of 210 μs.



• ECP parallel port FIFO mode timing

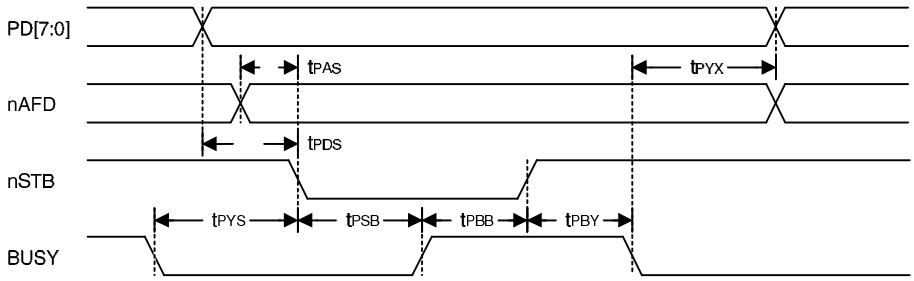
	Parameter	Min.	Max.	Units	Notes
t_{PDS}	PD[7:0] valid to nSTB active	500		ns	
t_{PSW}	nSTB active pulse width	500		ns	
t_{PBD}	PD[7:0] hold from nSTB inactive	500		ns	
t_{PBS}	BUSY inactive to nSTB active	900		ns	



• ECP parallel port forward timing

	Parameter	Min.	Max.	Units	Notes
t_{PDS}	PD[7:0] valid to nSTB asserted	0	180	ns	
t_{PAS}	nAFD valid to nSTB asserted	0	70	ns	
t_{PSB}	nSTB asserted to BUSY asserted	0		ns	
t_{PBB}	BUSY asserted to nSTB deasserted	280	360	ns	2
t_{PBY}	nSTB deasserted to BUSY deasserted	0		ns	
t_{PYX}	BUSY deasserted to PD[7:0] changed	210	350	ns	1, 2
t_{PYS}	BUSY deasserted to nSTB asserted	560	850	ns	1, 2

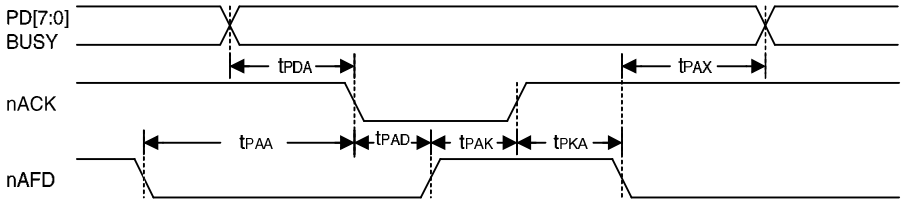
Maximum value only applies if there is data in the FIFO waiting to be written out.
Busy in not considered asserted or deasserted nutil it is stable for minimum of 280~350 μs.



• ECP parallel port reverse timing

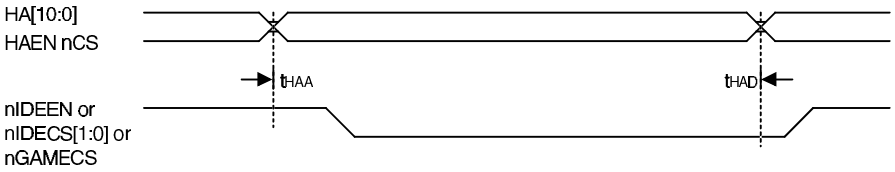
	Parameter	Min.	Max.	Units	Notes
t_{PDA}	PD[7:0], BUSY valid to nACK asserted	0		ns	
t_{PAD}	nACK asserted to nAFD deasserted	280	450	ns	1, 2
t_{PAK}	nAFD asserted to nACK deasserted	0		ns	
t_{PKA}	nACK deasserted to nAFD asserted	350	500	ns	2
t_{PAX}	nAFD asserted to PD[7:0] changed	0		ns	
t_{PAA}	nAFD asserted to nACK asserted	0		ns	

Maximum value only applies if there is room in FIFO and a terminal count has not been received. ACKZ is not considered asserted or deasserted until it is stable for minimum of 280~350 μs.

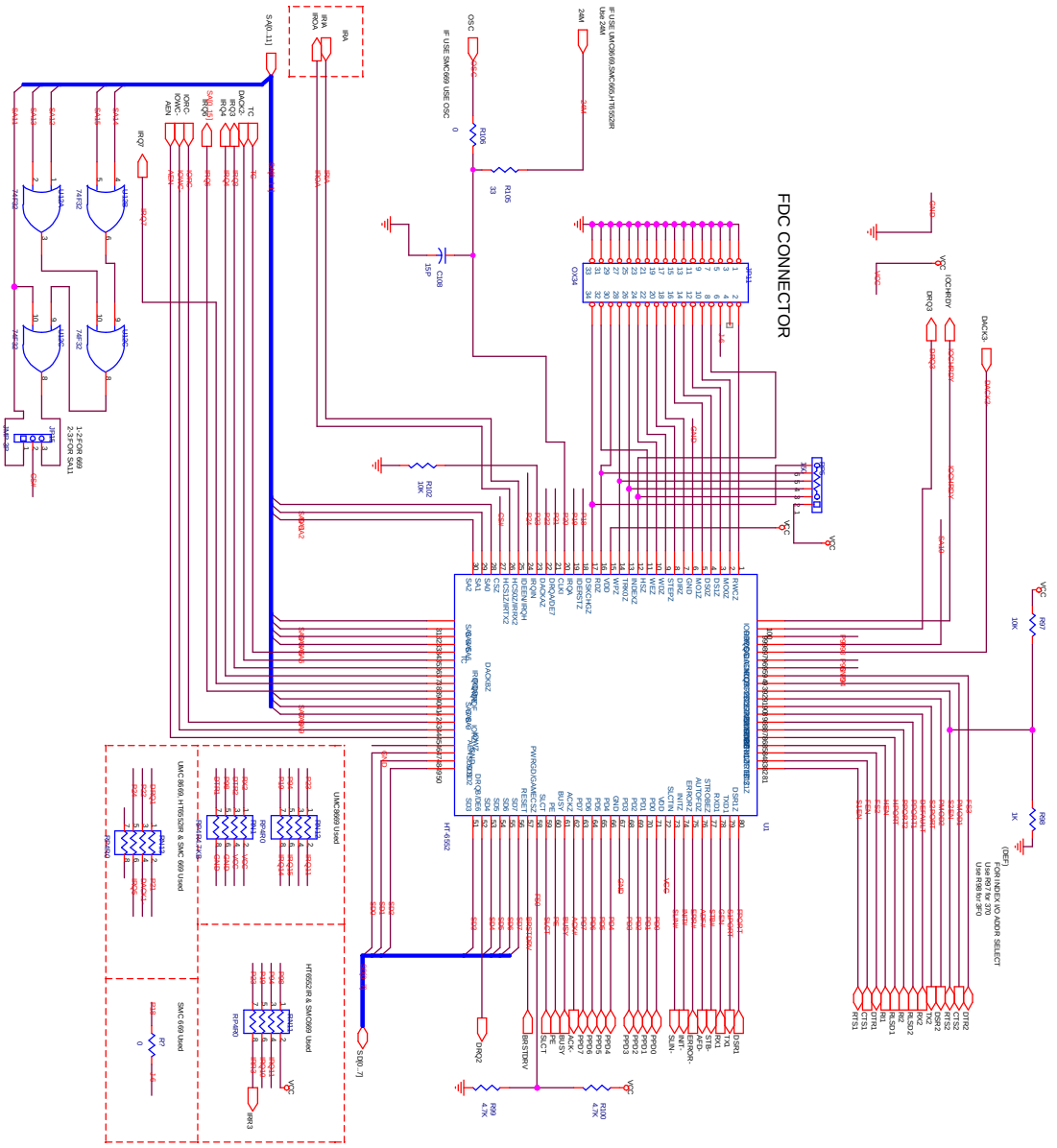


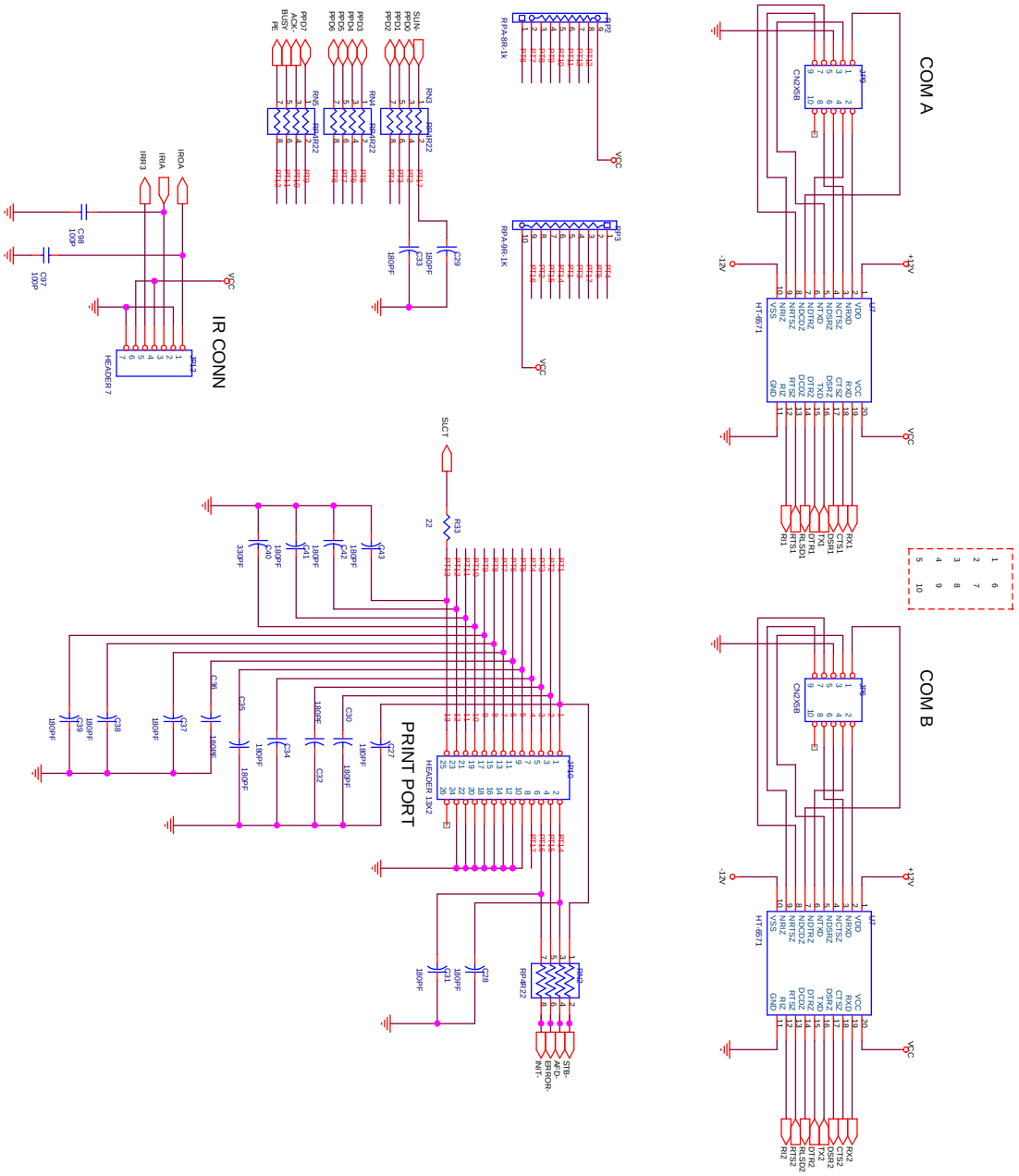
• MISC

	Parameter	Min.	Max.	Units	Notes
t_{HAA}	HA[10:0], HAEN and nCS valid to nIDEEN, nIDECS1, nIDECS2, nGAMECS assented.		29	ns	
t_{HAD}	HA[10:0], HAEN and nCS invalid to nIDEEN, nIDECS1, nIDECS2, nGAMECS deassented.		25	ns	



Application Diagram




COM A
COM B
IR CONN
PRINT PORT
HEADER 7
HEADER 13X2
CN2X5B
HT-6571
RPA4R-1K
RPA4R22
SLCT
VCC
+12V
-12V