Headland
Technology
Product Group

LSI LOGIC

T-52-33-05

HT25
3V Core Logic for 386SX

Features

- 25MHz operation at 2.7V to 3.6V
- Extensive power management features
- SMI support
- Local Bus Interface
- CPU clock control
- 16 general purpose I/O pins
- 2 programmable chip selects
- 44 event activity monitor
- ISA bus refresh control
- Up to 4 banks of 512Kb, 1Mb and 4Mb DRAM
- Flexible DRAM controller
- Slow and Self refresh DRAM modes
- Page mode DRAM accesses
- DRAM page interleaving
- 4 register EMS
- BIOS shadowing
- Relocation for unused DRAM segments
- PROM Write Enable for FLASH support
- 208 pin PQFP
- 0.7 Micron HCMOS

The HT25 is the industry's first 3-Volt single chip core logic with integrated power management for 386SX based 3-Volt systems. Programmable power management features give system manufacturers the flexibility of offering customized system solutions.

HT25 Based System Implementation

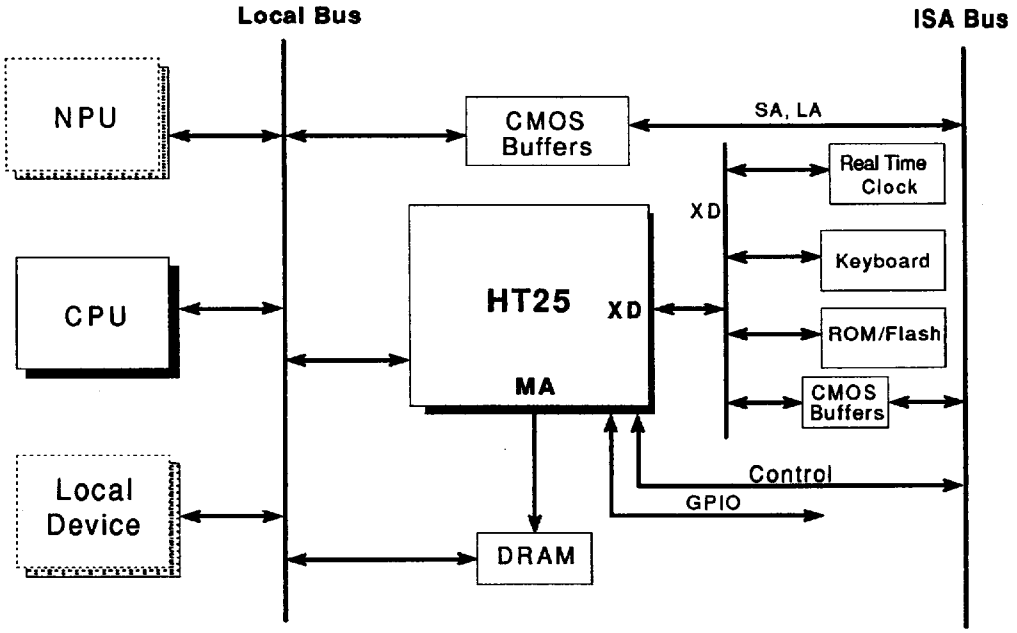


Figure 1 - HT25 Based System Implementation

HT25
3V Single Chip 386SX Controller

Internal Block Diagram

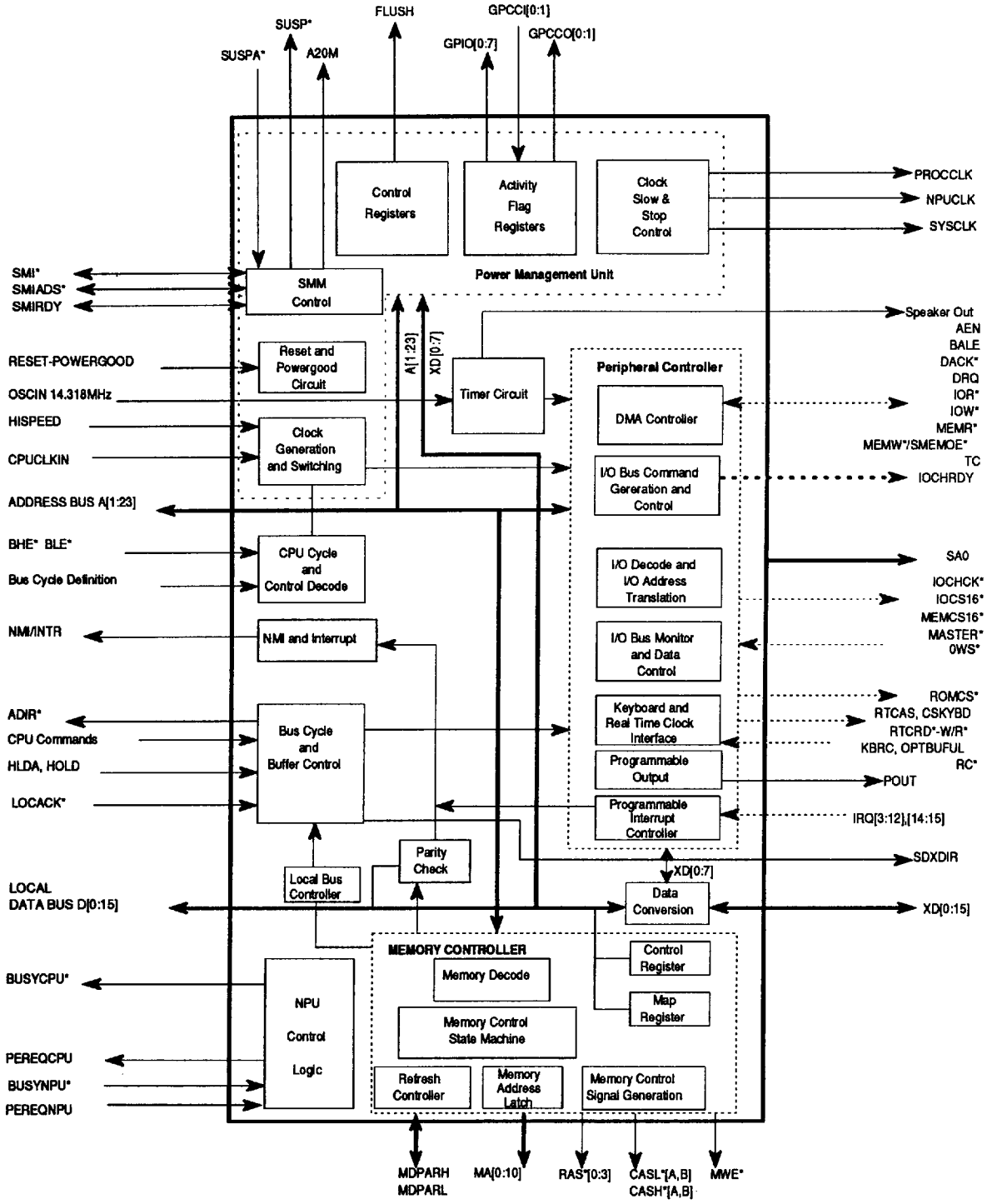


Figure 2 - Internal Block Diagram

GENERAL DESCRIPTION

The HT25 is a PC/AT™ compatible single-chip solution with integrated power management designed to operate in a 3-Volt system environment. This highly integrated chip facilitates the design of low power, high performance portable systems. The HT25 supports 3-Volt 386SX CPUs at clock speeds up to 25MHz at 2.7V to 3.6V. It supports power management functions using the System Management Mode (SMM).

Flexible power management is the cornerstone of the HT25. This approach provides power saving features that can be customized for product differentiation. Power management features include system activity monitors and general purpose I/O pins. The HT25 generates System Management Interrupt (SMI) to process activity information or when access to powered down peripherals is detected. Further power savings are achieved through the HT25's ability to control CPU and NPU clocks and support for slow refresh and self refresh DRAMs.

The HT25 Memory Controller features BIOS Shadowing, Memory Relocation, EMS, Page Mode Memory Access and Interleaving. The memory controller allows memory banks to be reordered to allow more efficient memory interleaving. The HT25 supports 512Kb, 1Mb, and 4Mb DRAMs.

The HT25 architecture is optimized for 3-Volt system designs, the SD bus acknowledge input provides a flexible I/O bus architecture and the XD bus is buffered directly from the HT25. Further, no external data bus buffers are required for a closed 3V system.

FUNCTIONAL DESCRIPTION

CPU Interface

The HT25 supports the AM386™SXLV and Cx486SLCTM CPUs including the system management mode (SMM). Interface diagrams are shown in figure 3a and 3b.

The HT25 supports the Cyrix CPU suspend mode in two ways:

1. SUSP* and SUSPA* handshake sequence.
2. CPU executing a HALT instruction.

The HT25 requests suspend mode by asserting SUSP* and when SUSPA* is received from the CPU, the HT25 asserts HOLD and upon receiving the HLDA from the CPU, self refresh is initiated if it was enabled, then the CPU clock is stopped (ISA refresh continues to run while CPU clock is stopped).

To restart the CPU clock, the HT25 normally terminates self refresh, starts the clock, waits for at least 10 clock cycles and then releases the HOLD request. The CPU resumes execution when it exits the hold acknowledge state.

If SUSPA* was requested by the HT25, the HT25 releases SUSPA* when it releases the hold request. If on the other hand, the SUSPA* was initiated by the CPU on a HALT instruction the HT25 restarts the clock on the deassertion of SUSPA*. The SUSP* is controlled by bit 7 of register 98H.

The internal Cyrix CPU cache needs to be FLUSHED to maintain coherency for non-CPU initiated cycles such as MASTER write and DMA write. The HT25 provides a FLUSH signal that goes active when the CPU generates HLDA and there is an ISA memory write.

The FLUSH signal can also be directly controlled by a bit in the System Configuration Register B (index 11H). This allows software such as EMS drivers to flush the cache when the memory mapping is changed.

The Cyrix processor does not have a dedicated SMI READY* pin. All Cyrix Bus cycles are terminated by READY*.

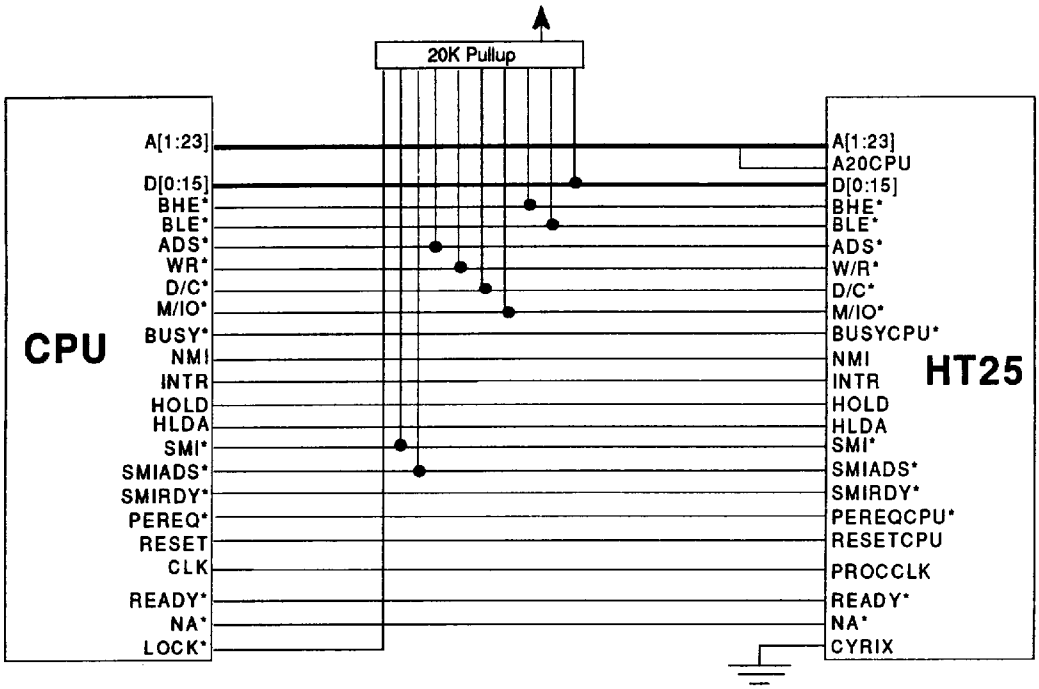


Figure 3a - HT25 AM386™ SXLV CPU Interface

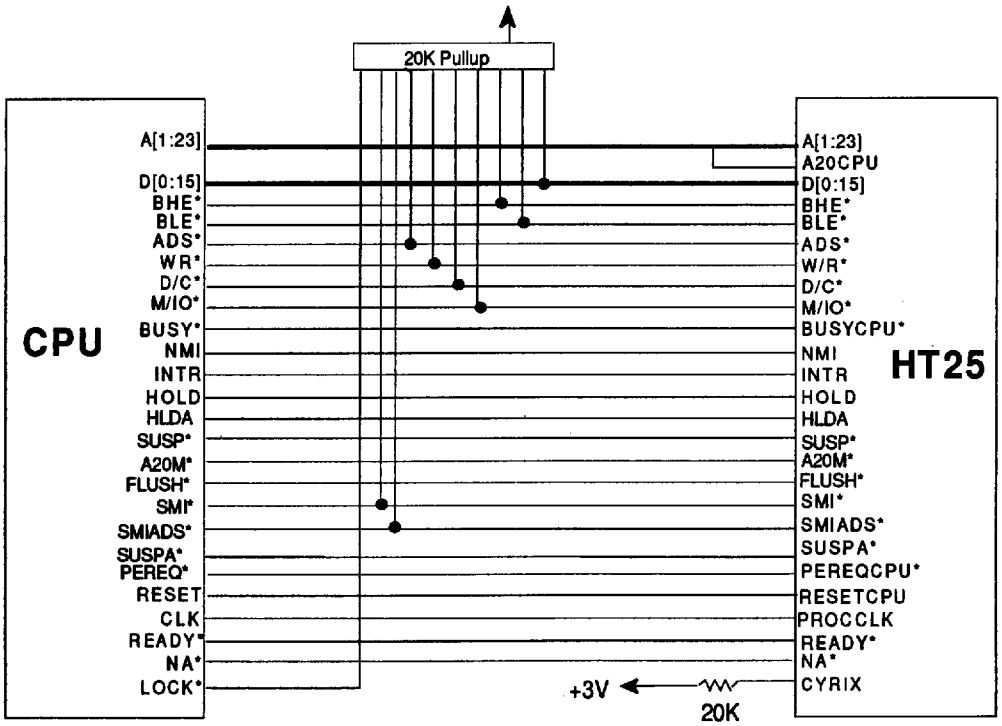


Figure 3b - HT25 Cyrix CX486SLC™ CPU Interface

The CPU is operated in pipeline mode during non-SMM local memory cycles and local bus cycles. During SMM code execution, I/O cycles or memory cycles outside the local memory address range, the CPU is operated in non-pipeline mode. This provides addresses to system peripheral devices for the entire CPU cycle without the need for address latches.

CPU Clock Control

The CPU clock (PROCCLK) is generated from the CPUCLKIN input to the HT25. The clock may be controlled by the CPU Speed Control Register (Index 98h) or be slowed or stopped under various conditions. The CPU Speed Control Register contains two CPU clock speed settings. The clock speed is also controlled by the HISPEED input on the HT25. The clock speed is derived by dividing the input clock by 1, 2, 4, 8, 16 or 32. See Figure 4 for the clock generator diagram.

The CPU Speed Control Register contains a clock stop control. The clock may be stopped by setting the CPU Clock Stop Control bit (bit 7). The CPU is first put into a HOLD state then the clock is stopped. The clock is restarted by an interrupt (INTR, NMI or SMI) or reset. It is recommended that the NPU clock be stopped while the CPU clock is stopped.

The Interrupt Control Register (index 96) controls the way that interrupts re-start the CPU clock. The CPU clock will re-start for interrupts if bit 7 of this control register is set to 1.

If an interrupt occurs while the CPU clock is stopped the CPU clock is restored, for a set amount of time, to the mode it was in when the clock was stopped. The amount of time that

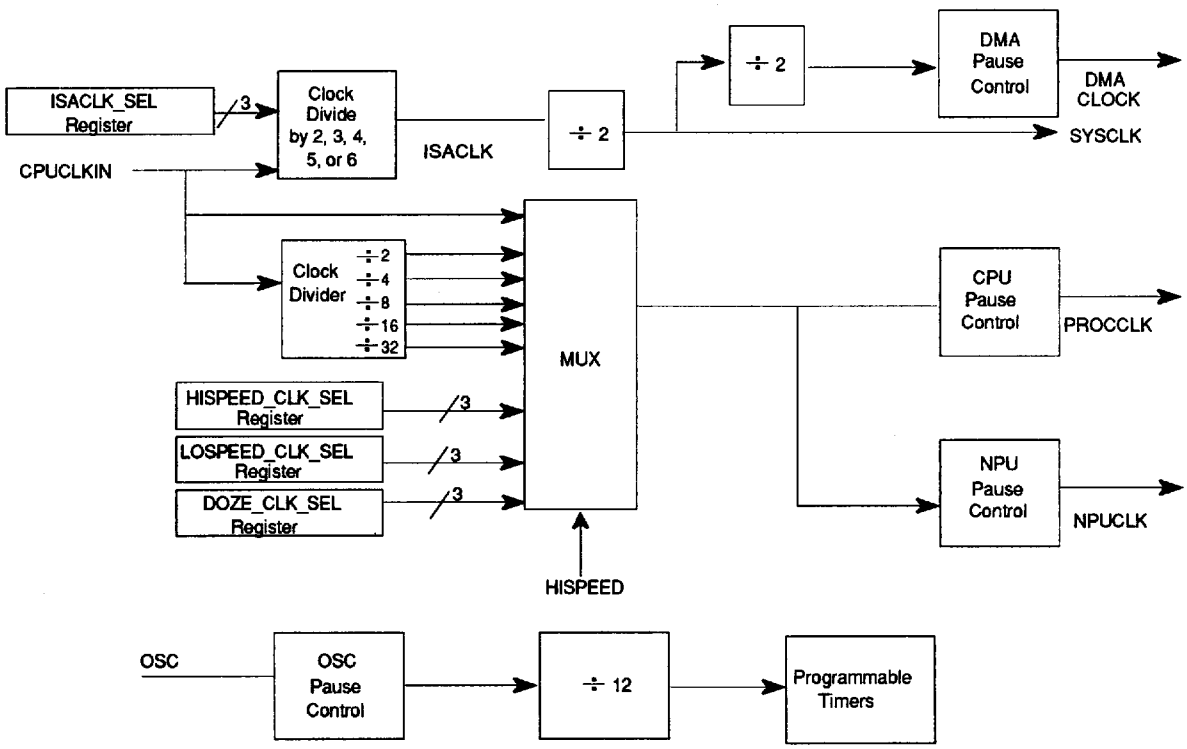


Figure 4 - Clock Control Diagram

the CPU clock remains active to allow for servicing the interrupt is controlled by the Interrupt Control Register if bit 7 is a 1. This allows housekeeping interrupts (SMI is not set to occur) to be handled and quickly stop the clock again. If the SMI enable bit is on for an interrupt, the SMM code will usually clear the CPU stop clock bit to keep the clock running when that interrupt occurs. If bit 7 is set to 0 the CPU clock will restart only for interrupts which have their SMI enable bit set.

The CPU clock may also be stopped during ISA bus cycles and during CPU hold cycles. These functions are controlled by CPU Doze Control Register C (Index 92h). Setting bit 2 will cause the CPU clock to stop during accesses to the ISA bus. Setting bit 3 will cause the CPU clock to be stopped during CPU hold cycles.

The CPU clock may be slowed when the CPU is not performing certain tasks. This mode, Doze, is controlled by CPU Doze Control Registers A and B (Index 90h and 91h). The tasks to be monitored are programmable and can be one or more of the following:

- I/O operations to address 100h - 3FFh
- Keyboard controller output buffer read (I/O address 060h)
- Video memory writes (memory address 0A0000h - 0BFFFFh)
- Local bus peripheral cycles
- Non-periodic SMI cycles

If the selected tasks have not occurred by the amount of time specified in the control registers then the CPU clock will be reduced to its doze speed. The doze speed is derived by dividing the normal CPU speed by 2, 4, 8 or 16. The doze speed is selected in CPU Doze Control Register B (Index 91h). The CPU clock speed resumes at its programmed normal speed upon detection of one of the programmed activities.

CPU Reset

PWRGOOD signal is the main reset for the HT25. When it is low RESETCPU and RESETBUS will be active. RESETCPU is generated for several conditions. RESETCPU is always active for at least 16 PROCCLK cycles. When the RC* pin is low the RESETCPU is active. RESETCPU will be active 6.72 microsec. after port 92H bit 0 is set to a 1. RESETCPU will be active for 16 PROCCLK cycles after detection of a CPU SHUTDOWN condition is detected.

System Management Interrupt

The HT25 supports the SMM as described in the AMD Am386SXLV Technical Reference Manual. The SMI*, SMIADS* and SMIRDY* are used as described in the AMD document. The SMI can be disabled independently or can be masked with the NMI mask using the SMI Control Register (Index 80h).

The SMI pin can be activated either by a periodic timer or by IO and interrupt activity monitors. Normally when the SMM is used the periodic SMI is always active and the activity monitor SMI's are disabled. The appropriate activity monitor SMI is normally activated when the SMM code disables a peripheral. After the SMI pin is active the system will be in SMM. The state of the system can be checked in a status register at Index 98. Bit 2 is set while the system is in SMM by the first SMIADS* and cleared when the CPU releases the SMI pin.

When the CPU is in SMM the SMM memory space at 06XXXXh is mapped to system memory at physical address 0AXXXXh. If SMI is not used the SMM memory size can be set to 0 (SMI Control Register bits 0,1) and the 0A0000h segment made available for remapping. Memory accesses to the PROM address range during SMM are directed to the PROM space. The SMM PROM address space can be made larger than the normal system BIOS space as programmed in PROM Configuration Register 2 (Index 17h).

Periodic SMI

System Management Interrupts can be generated periodically by programming an SMI interval into the SMI Control Register (Index 80h), bits [2:5].

Activity Initiated SMI

The HT25 provides for activity monitoring and SMI generation on certain events. The event flags are contained in the Activity Flag Registers (Index 84h - 89h). Each flag is set on the occurrence of its associated event and reset on a read of the register. The events that are monitored are shown in Table 1.

Each activity monitor has an associated SMI Enable Bit. The SMI enable control bits for the activity monitors are contained in the Activity Monitor SMI Enable Registers (Index 8Ah - 8Fh). If the SMI Enable Bit for a given activity is set when the activity occurs then an SMI is generated and the activiy flag is set. If a the CPU is currently servicing an SMI when an activity occurs then another SMI request will be issued when the current one completes.

The address range for SMI generation is expanded for Keyboard controller, Floppy disk and Hard disk activities to include all accesses to these peripherals. This allows for SMI generation to trap attempted accesses to peripherals that may be powered down. An activity

Activity	Command	Address
ISA bus	IOR/IOW	100h-3FFh
Video memory	MEMW	0A0000h-0BFFFFh
Keyboard controller	IOR/IOW	060h
	IOW	064h
Serial ports	IOR/IOW	38Fh-3FFh
	IOR/IOW	2F8h-2FFh
	IOR/IOW	3E8h-3EFh
	IOR/IOW	2E8h-2EFh
Parallel ports	IOR/IOW	378h-37Fh
	IOR/IOW	278h-27Fh
	IOR/IOW	3BCh-3BFh
Floppy disk	IOR/IOW	3F5h
Hard disk	IOR/IOW	1F0h-1F7h
System interrupts (IRQ)	IRQ 0,1,3-15	
ISA bus I/O Channel Check	IOCHCK*	
Programmable I/O space 1 and 2	Programmable	Programmable
Local Bus Device		
NPU Cycle	IOR/IOW	A23=1
General Purpose I/O [0:7]		
General Purpose Input [0:3]		

Table 1 - HT25 Activity Monitors

flag is generated for the expanded address range when the SMI Enable Bit is set.

The activity monitor addresses exclude status registers so that these peripherals can be interrogated without setting an activity flag when the SMI Enable Bit is off. Table 2 shows the address ranges for these devices when the SMI Enable Bit is set.

When an SMI request is generated due to an IRQ then INTR is not issued to the CPU until the SMI is acknowledged (by the assertion of SMIADS*). This insures that the IRQ is handled under control of the system SMI routine. If the CPU is already in SMI mode then the INTR is not issued until after the completion of the current SMI and the start of the IRQ initiated SMI. The same is true of NMI. The HT25 does not send an NMI to the CPU until the SMI request for NMI has been sent.

On reset, all Activity Flags and SMI Enable Bits are cleared.

NPU Interface

The HT25 supports 80387SX or compatible Numeric Co-Processors (NPU). The NPU is connected to the HT25 as shown in Figure 5. The BUSYNPU*, ERRNPU* and PEREQNPU signals from the NPU are intercepted and used to generate BUSYCPU* and PEREQCPU signals to the CPU.

Activity	Command	Address
Keyboard controller	IOR/IOW	60, 64
Floppy controller	IOR/IOW	3F0-3F5, 3F7
Hard disk controller	IOR/IOW	170-177, 1F0-1F7, 3F6-3F7

Table 2 - HT25 Expanded Activity Monitor SMI Addresses

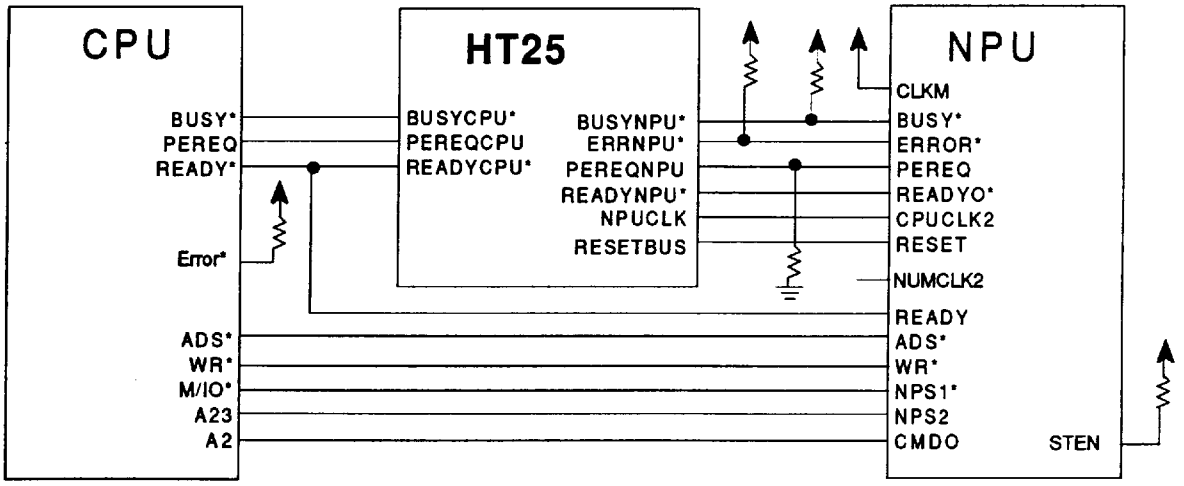


Figure 5. NPU Interface Diagram

The presence of an NPU is determined by checking the state of the ERRNPU* after PWRGOOD input to the HT25 goes high. If the input is asserted (LOW) then bit 3 of the Miscellaneous Status Register (Index 1Fh) will be set.

When ERRNPU* is asserted, indicating an unmasked exception, the HT25 generates an internal interrupt, IRQ13, and asserts INTR to the CPU. The PEREQCPU output to the CPU is then asserted after the BUSYNPU* input becomes inactive (HIGH). PEREQCPU will remain active until it is cleared upon a write to I/O Port 0F0. This allows unmasked exceptions to be handled under interrupt control as in standard ISA systems.

BUSYNPU* is passed to the co-processor as BUSYCPU*. On occurrence of an ERRNPU* signal, BUSYNPU* is latched and held until an I/O write to F0H. If it is determined that a co-processor is not present then the BUSYCPU* signal to the CPU is toggled low during REFRESH*. This prevents the CPU from waiting for a BUSY* when an NPU is not installed.

The READYNPU* input to the HT25 is used to generate the READYCPU* output to the CPU. NPU cycles may be 0 wait states for certain operations when READYNPU* is used. All other NPU cycles will be 1 wait state.

The NPUCLK output has the same frequency as the PROCCLK output, but it can be stopped independently. The NPU clock may be stopped by setting bit 0 of the NPU Speed Control Register (Index9Ah). There should be software support in the interrupt 7 handler to transparently re-start the NPUCLK, if an NPU is installed and the clock was stopped while the CPUCLK is left running The NPU must operate in the synchronous mode.

Local Bus Interface

Devices that interface directly to the CPU local bus are supported by the HT25. These devices gain control of the CPU cycle by asserting the LOCACK* signal. This pin can be programmed to be sampled at one of four points in the CPU cycle. The point at which LOCACK* is sampled is selected using bits [0:1] in the Local Bus Control Register (Index 20h). The timing options for LOCACK* are shown in Figure 6.

Local bus devices that gain control of the CPU bus are responsible for completing the CPU cycle by asserting the READY* pin on the processor. The HT25 releases the READYCPU* pin upon recognizing a local bus device. It is recommended that the LOCACK* signal be driven high before the local bus device releases the signal. If LOCACK* is allowed to transition to a high using a pull up resistor, it

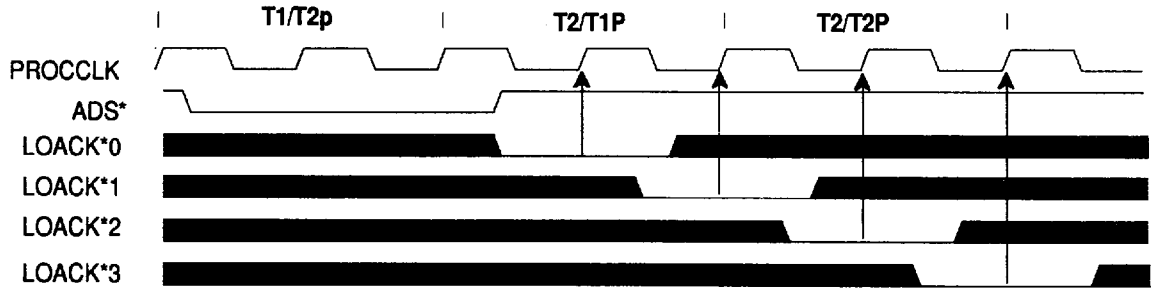


Figure 6 - LOCACK* Sample Points

may not have attained the minimum level required for a high by the time that it is sampled again.

The HT25 will not recognize local bus device requests for system memory or I/O addresses that are under the control of the HT25.

Local bus devices cannot be accessed through the HT25 by devices on the ISA bus. In addition, ISA bus devices cannot be accessed by local bus devices via the HT25. Local bus device access to the ISA bus and ISA bus accesses via master mode or DMA cycles to local bus devices must be accomplished directly without HT25 support.

MEMORY CONTROLLER

The HT25 supports up to 4 banks of 512K, 1M and 4M byte memory devices in combination with a maximum total memory size of 20M bytes. HT25 memory controller performs page/interleaving, memory relocation, BIOS shadowing, EMS paging and provides various refresh options. The memory controller runs in page mode during CPU accesses. Memory bank pairs 0,1 and 2,3 are interleaved whenever they contain memory of the same size.

DRAM Interface

The HT25 provides row and column address select, multiplexed memory address, memory write and parity signals to the DRAM devices. The interface is shown in Figure 7.

Memory Configuration

The memory configuration is selected using DRAM Configuration Register A (Index 10h). The available configurations are listed in the Register Description section of this document.

In several memory configurations the memory banks are reordered to produce a more efficient interleaving configuration. The banks with the largest page size are remapped to the more frequently used low memory area as shown in Table 3.

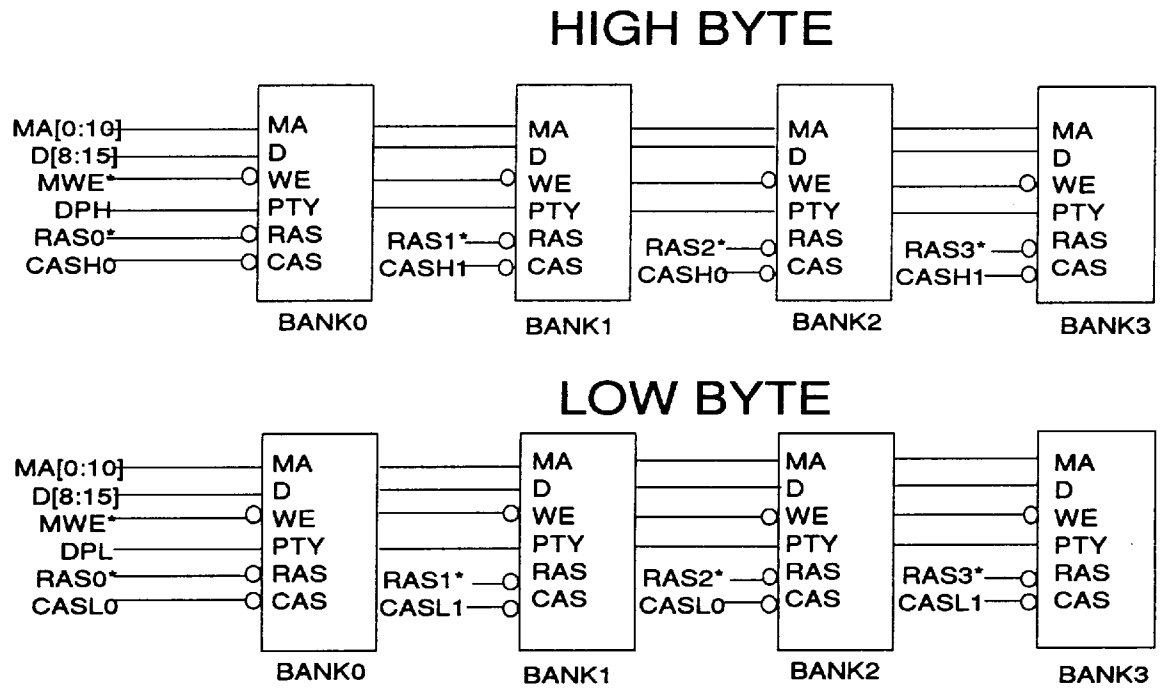


Figure 7 - HT25 DRAM Interface

	Physical Bank				Logical Bank				Mem Size
Config	0	1	2	3	0	1	2	3	
6	512K	1M	1M	-	1M	1M	512K	-	5M
7	512K	1M	1M	1M	1M	1M	512K	1M	7M
9	512K	4M	4M	-	4M	4M	512K	-	17M
11	512K	512K	1M	1M	1M	1M	512K	512K	6M
13	512K	512K	4M	4M	4M	4M	512K	512K	18M
17	512K	1M	4M	4M	4M	4M	512K	1M	19M
25	1M	4M	4M	-	4M	4M	1M	-	18M
26	1M	1M	4M	4M	4M	4M	1M	1M	20M

Table 3 - Remapped Memory Configurations

The Memory Controller is disabled when programmed into the 0K configuration. RAM control signals are not generated and the HT25 relinquishes control of the CPU (generation of READYCPU*) to a local bus device.

The BIOS address space at the top of the CPU address range (FF0000h-FFFFFFh or FE0000h-FFFFFFh) is reserved for the ROM BIOS. For configurations with a total memory size of 16M or greater, that area of memory is accessible via EMS only.

BIOS Shadowing

BIOS instructions that are located in the ROM space can be relocated to DRAM (shadowed) to reduce the instruction fetch time and enhance system performance. Address space from 0C0000h to 0FFFFFh can be selected for shadowing in 16K blocks. The blocks are selected in Shadow RAM Configuration Registers A and B (Index 14h and 15h). Shadow mode is enabled in DRAM Configuration Register B (Index 11h), bit 0.

With shadow mode disabled and no memory blocks selected for shadowing, all reads from the BIOS space are directed to the ROMs (ROMCS* active) and all writes to the BIOS space are directed to the ISA bus. To shadow the BIOS the space to be shadowed is first selected in 16K blocks. This will direct all writes to the selected blocks to DRAM and allow the BIOS to be transferred. Shadow mode is then enabled by setting bit 0 of System Configuration Register B and all read operations from the selected blocks are directed to the DRAM. All write operations to the selected blocks are directed to the ISA bus.

Memory Relocation

DRAM in the 0A0000h to 0FFFFFh address space that is not used for SMI memory or Shadow RAM can be remapped to occupy the area above the top of memory. This feature is enabled using System Configuration Register B (Index 11h), bit 1. DRAM is relocated in 64K blocks as shown in Table 4.

An additional wait state can be added during accesses to DRAM that is relocated. This may be necessary due to additional address translation time required for relocated memory spaces.

Block	Relocated if relocation enabled and
0AXXXXh	SMI is disabled
0BXXXXh	Always relocated
0CXXXXh	0C0000h - 0CFFFFh not shadowed
0DXXXXh	0C0000h - 0DFFFFh not shadowed OR 0CXXXXh and 0FXXXXh shadowed
0EXXXXh	0C0000h - 0EFFFFh not shadowed OR 0CXXXXh and 0FXXXXh shadowed
0FXXXXh	Shadowing disabled

Table 4 - DRAM Memory Relocation

EMS

The HT25 supports LIM EMS 4.0 with an EMS Configuration Register (Index 60h) and four pairs of EMS Page Registers (Index 64h - 6Bh). Expanded memory is accessed through a 64K window residing in memory address range 0C0000h - 0DFFFFh. The 64K window is divided into four 16K contiguous pages as shown in Figure 8. EMS is enabled and the location of the EMS window is programmed using the EMS Configuration Register.

Each EMS page has a two page registers that specify the physical memory space to which the EMS page is mapped. The mapping information consists of a nine bit address (T[14:22]) and two bits for bank select. The nine bit address is used directly in the access of the DRAMs as described in the following section on memory addressing. The bank select bits are used to select the logical DRAM bank to which the EMS page is mapped.

The EMS driver must flush the cache (System Configuration Register B, index 11H) when the memory mapping is changed and a CPU with internal cache is being used.

Memory Interleaving

The HT25 Memory Controller interleaves logical memory banks 0 and 1 or 2 and 3 whenever a logical bank pair contains DRAMs of the

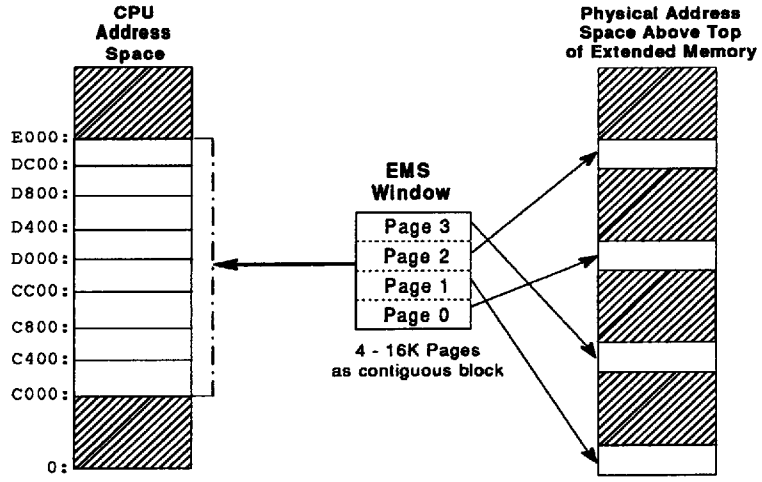


Figure 8 - EMS Memory Mapping

same configuration. The interleaving is done on page boundaries such that one bank (bank 0 or 2) of a bank pair contains even pages and the other bank (bank 1 or 3) contains odd pages.

See the following section on DRAM addressing for further details.

DRAM Addressing

The Memory Address (MA[0:10]), Row Address Select (RAS0* - RAS3*) and Column Address Select (CASL0*, CASL1*, CASH0*, CASH1*) signals are used by the HT25 to address the system DRAM. These signals are derived from the CPU address (or master/DMA device) using bank remapping, shadowing, SMM, relocation and EMS configurations.

The translation of the CPU address is performed on A[14:23] to produce the Translated addresses T[14:23]. See the descriptions of bank and EMS for more details. Address bits A[1:13] are used directly, without translation, to produce the memory address.

The column address (MA[0:10] on the falling edge of CAS) for the various DRAM sizes is shown in Table 5.

The active CAS signals are determined by the translated address and the interleave mode. First the logical bank is determined using the translated address and memory configuration. For non-interleave mode, CASL0* and CASH0* are active for logical banks 0 and 2, while CASL1* and CASH1* are active for logical banks 1 and 3.

MA	0	1	2	3	4	5	6	7	8	9	10
Col-512K	A1	A2	A3	A4	A5	A6	A7	A8	A9	-	-
Col-1M	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	-
Col-4M	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11

Table 5 - DRAM Column Address

LOGICAL BANK	512K A(10)	1M A(11)	4M A(12)	ACTIVE CAS
0	0	0	0	CASL0*, CASH0*
0	1	1	1	CASL1*, CASH1*
1	0	0	0	CASL0*, CASH0*
1	1	1	1	CASL1*, CASH1*
2	0	0	0	CASL0*, CAS0H*
2	1	1	1	CASL1*, CASH1
3	0	0	0	CASL0*, CASH0*
3	1	1	1	CASL1*, CASH1*

Table 6 - Active CAS in Interleave mode.

In interleave mode, the active CAS signals are determined using the logical bank, DRAM size and A[10:12] as shown in Table 6. For banks that are relocated for interleaving (see table 3).

The row address (MA[0:10] on the falling edge of RAS) in non-interleave mode for the various DRAM sizes is shown in Table 7.

The DRAM row address for interleave mode is shown in Table 8. BK0 is 0 for logical banks 0 and 2. BK0 is 1 for logical banks 1 and 3.

The active RAS signal is determined by the translated address and the interleave mode. First the logical bank is determined using the translated address and memory configuration. For non-interleave mode, RAS0*, RAS1*, RAS2* and RAS3* are active for logical banks 0, 1, 2 and 3 respectively.

In interleave mode, the active RAS signals are determined using the logical bank, DRAM size, bank relocation mode and A[10:12] as shown in Table 9.

MA	0	1	2	3	4	5	6	7	8	9	10
Row-512K	A10	A11	A12	A13	T14	T15	T16	T17	T18	T19	-
Row-1M	T20	A11	A12	A13	T14	T15	T16	T17	T18	T19	-
Row-4M	T20	T21	A12	A13	T14	T15	T16	T17	T18	T19	T22

Table 7 - DRAM Row Address in Non-interleave mode

MA	0	1	2	3	4	5	6	7	8	9	10
Row-512K	BK0	A11	A12	A13	T14	T15	T16	T17	T18	T19	-
Row-1M	T20	BK0	A12	A13	T14	T15	T16	T17	T18	T19	-
Row-4M	T20	T21	BK0	A13	T14	T15	T16	T17	T18	T19	T22

Table 8 - DRAM Row Address in Interleave mode

LOGICAL BANK	512K A(10)	1M A(11)	4M A(12)	ACTIVE RAS
0	0	0	0	RAS0
0	1	1	1	RAS1
1	0	0	0	RAS0
1	1	1	1	RAS1
2	0	0	0	RAS2
2	1	1	1	RAS3
3	0	0	0	RAS2
3	1	1	1	RAS3

Table 9 - Active RAS in Interleave mode.

Refresh

The HT25 Memory Controller generates CAS-before-RAS refresh cycles to the system DRAM and ISA compatible refresh cycles to the ISA bus. Self Refresh Mode can be enabled for system DRAM when the CPU clock is stopped. Refresh is controlled by the Refresh Control Register (Index 37h).

The normal refresh rate is determined by 8254 compatible Programmable Interval Timer, Channel 1 (see description in the ISA Controller section). The refresh rate is typically programmed for 15.6uS. The refresh rate may be slowed, without altering the PIT registers, by using the Refresh Rate Control (Refresh Control Register bits 0:2).

Refresh cycles to the ISA bus are controlled by Refresh Control Register bit 7. When enabled, refresh cycles on the ISA bus are compatible with the ISA standard and a 2 way staggered CAS-before-RAS refresh cycle is performed on the system DRAM.

When the ISA bus refresh is disabled a 4 way staggered CAS-before-RAS refresh cycle is performed on the system DRAM and the refresh cycle operates at full CPU speed. Also, the CPU is not put on HOLD during these refresh cycles. If a CPU cycle is pending during refresh the CPU cycle is extended using READYCPU*.

Automatic Self Refresh (Refresh Control Register bit 6) places the DRAM into Self Refresh mode when the CPU clock is stopped by the CPU Speed Control Register (index 98). When Automatic Self Refresh is disabled the refresh mode is unchanged when the CPU clock is stopped.

Before exiting self-refresh mode, a 2048 cycle CAS-before-RAS burst refresh is performed to refresh all rows.

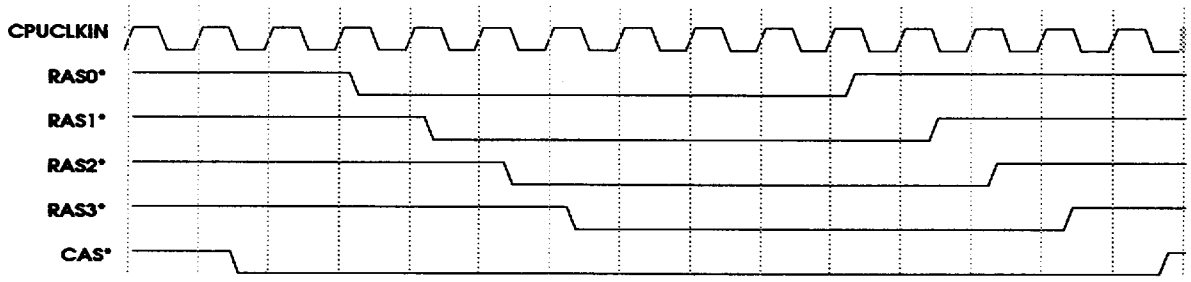


Figure 9a - ISA Bus refresh enabled

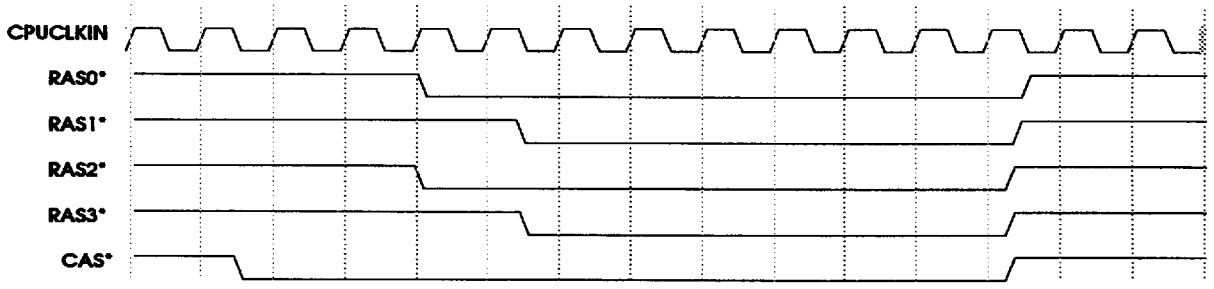


Figure 9b - ISA Bus refresh disabled

Figure 9 - System DRAM Refresh Cycles.

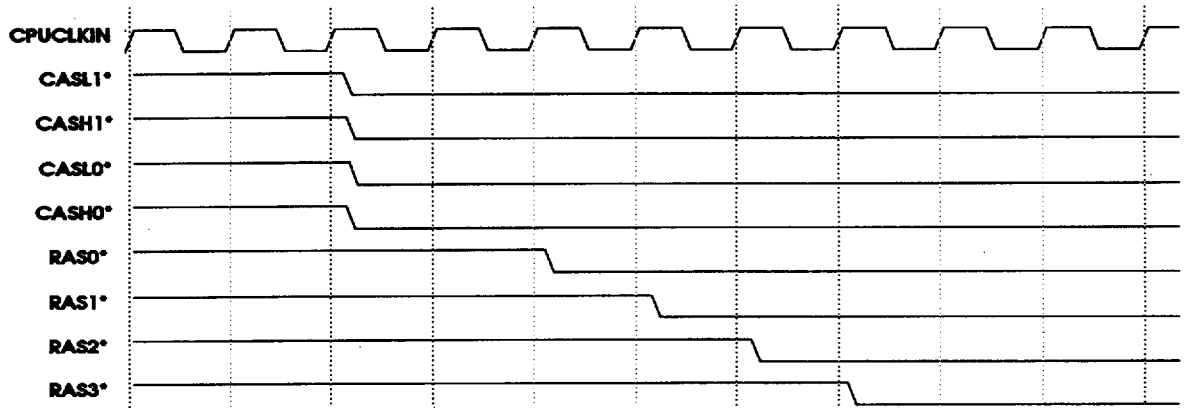


Figure 9c - Self Refresh Start

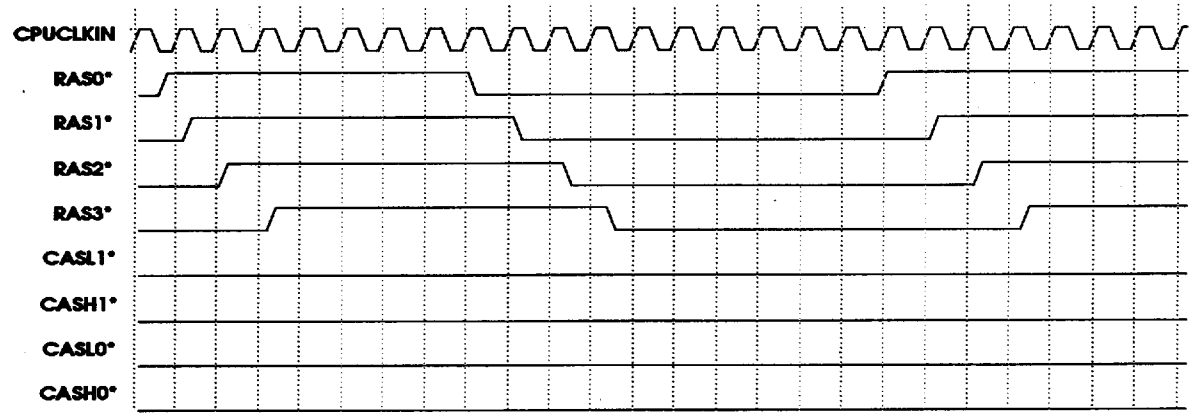


Figure 9d - Self Refresh Exit

Figure 9 - System DRAM Refresh Cycles

When the memory is in self refresh mode, the memory is not available. DMA or master devices must wake up the CPU first to take the memory out of self refresh mode before accessing memory.

The system DRAM refresh cycles are shown in Figure 9.

Parity Checking

System board memory write cycles generate two parity bits, one for each byte of a bank. These bits are written out coincident with the data write. On a CPU read, DRAM read data is latched and feeds the parity generator. The read, DRAM parity bits are latched and compared with the generated parity bits and the NMI signal is generated in the case of a parity error detection. The NMI can be masked by bits in control register at port 61H and 70H. The HT25 control register index 11H can override port 61H and disable parity checking for the on-board dram.

Page Mode

The HT25 CPU memory controller always operates in page mode memory timing. There are 4 RAS lines, one for each bank, and 2 pairs of high and low CAS lines. Each pair of CAS lines is shared between 2 banks.

This means only 2 RAS lines can be active at any time. RAS0 and RAS2 are mutually exclusive and so are RAS1 and RAS3. When a RAS line is asserted, the paired RAS must be deasserted.

Bank 0	RAS0	CASL0	CASH0
Bank 1	RAS1	CASL1	CASH1
Bank 2	RAS2	CASL0	CASH0
Bank 3	RAS3	CASL1	CASH1

Table 10 - Page Mode

The HT25 supports 2 sets of DRAM timing, Extended mode and Standard mode. Standard timing is the highest performance with 0 wait states for a page hit, pipeline cycle.

Extended timing has 1 wait state for a page hit, pipeline cycle. The memory controller state machines always operate at the CPUCLKIN frequency even when the PROCCLK is at a slower frequency. Table 11 shows the number of wait states for the memory cycles.

Write cycles are partially posted by starting CAS late in the cycle and keeping it active into the next CPU cycle. As a result, back to back write cycles can be 0 wait state, but a read hit following a write has an extra wait state in standard timing.

Cycle Type	Wait States
read, hit	0
read, hit after a write	1
read, miss	3
1st read to page	2
write, hit	0
write, miss	2
1st write to page	1

Table 11A - Standard mode timing wait states

Cycle Type	Wait States
read, hit	1
read, miss	4
1st read to page	3
write, hit	1
write, miss	4
1st write to page	3

Table 11B - Extended mode timing wait states

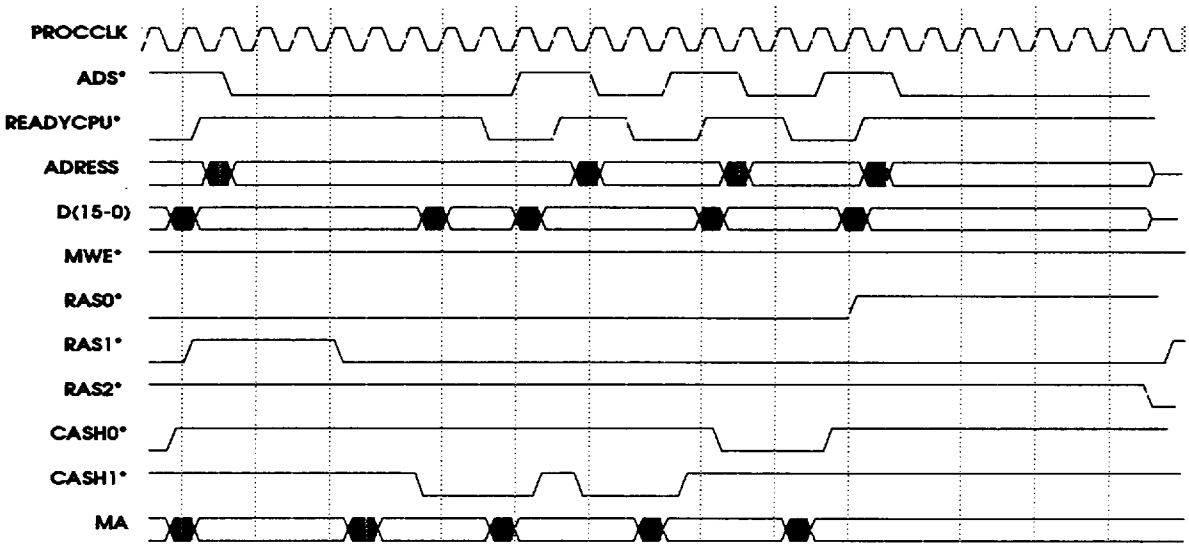


Figure 10a - Standard Timing (Read) Page Miss/Hit

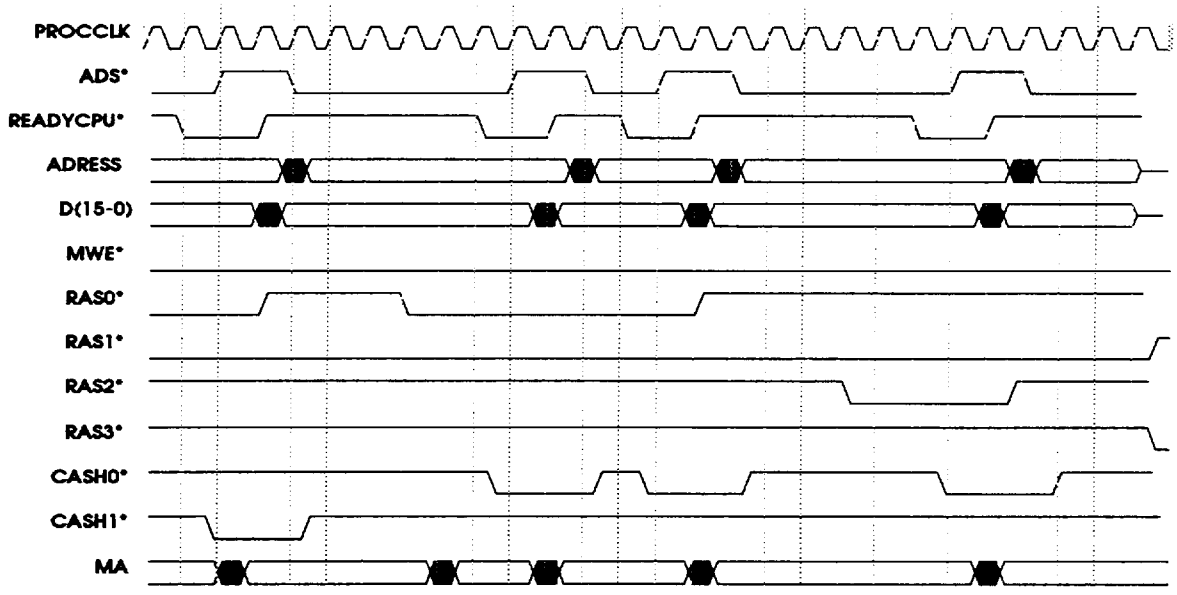


Figure 10b - Standard Timing (Write) Page Miss/Hit

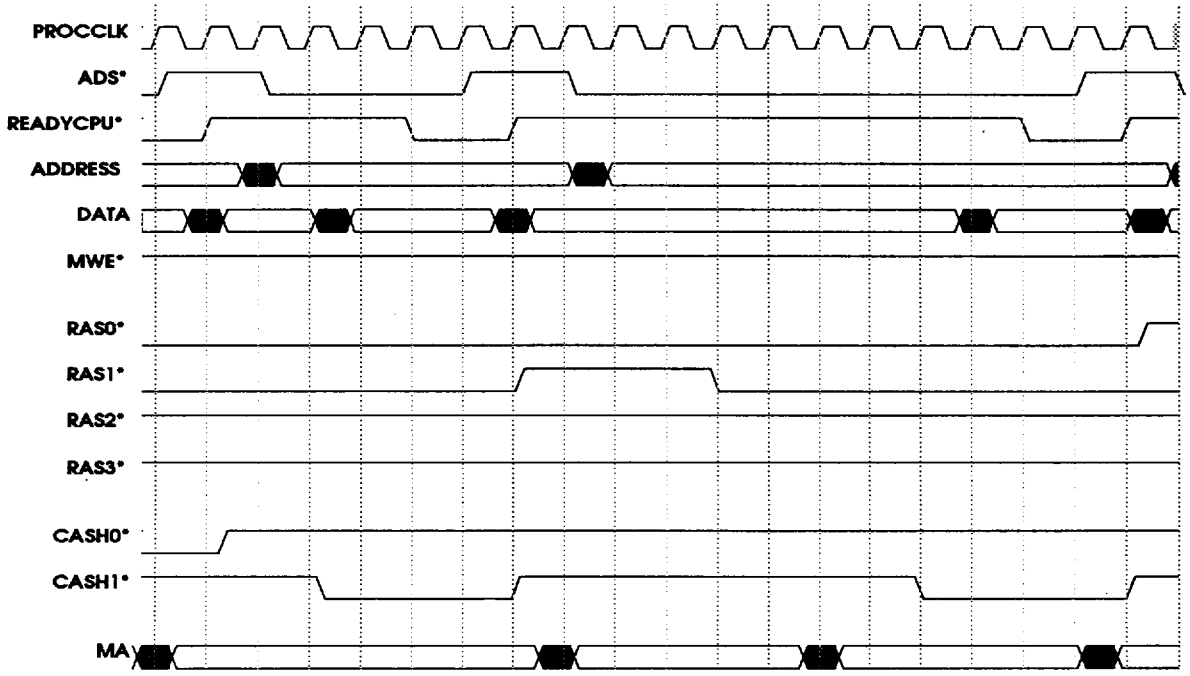


Figure 10c - Extended Timing (Read) Page Hit/Miss

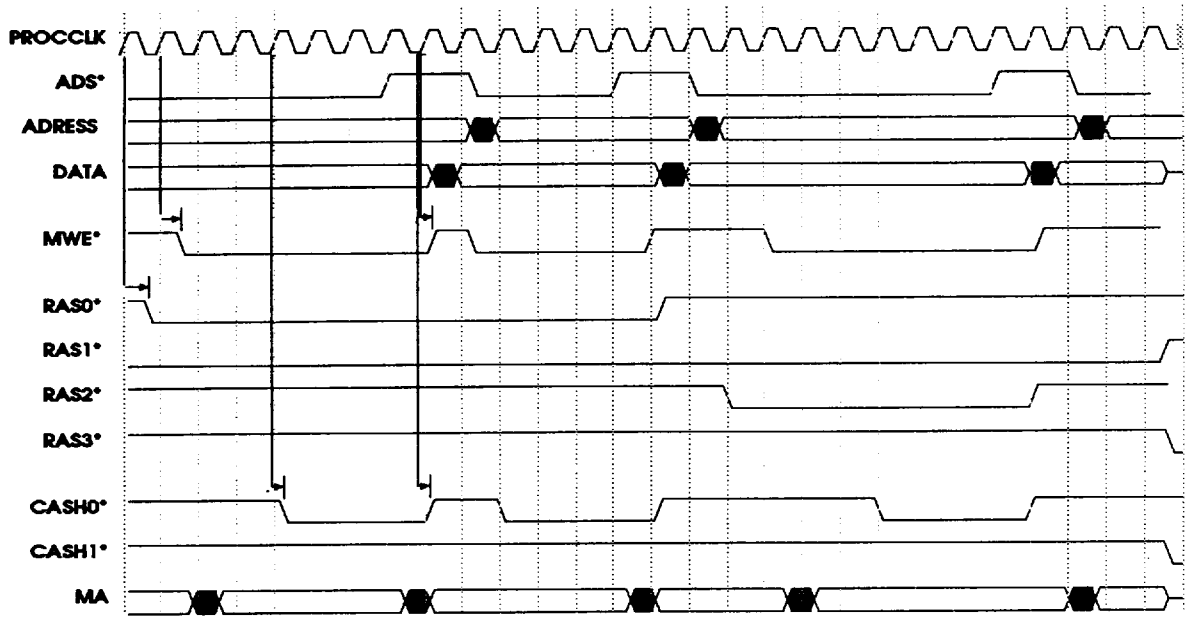


Figure 10d - Extended Timing (Write), Page Miss/Hit

ISA SYSTEM CONTROLLER

The HT25 ISA bus controller provides all of the signals necessary to produce a fully ISA compatible bus. This system bus may be a simple 3 volt 8 bit bus for system peripherals or a full 5 volt 16 bit ISA bus with Master Mode support. The bus speed is programmable using the ISA Bus Speed Control Register (Index 22h) and is a derivative of the CPU clock. See the ISA Bus Speed Control Register description for ISA bus speed programming.

Address and Data Busses

CPU cycles are run in non-pipeline mode during ISA bus cycles. This allows the CPU address bus to be used directly by system peripherals or to be buffered to create an SA bus without the need for latches. The ADIR* signal, which is derived from HLDA and MASTER*, is provided as the direction control for the SA bus buffers. (ADIR* would also control the direction of a buffer on IOR*, IOW*, MEMR*, MEMW* , if these signals require buffering.)

The HT25 provides SA0 directly. During CPU cycles, SA0 is derived from the CPU control signals. The DMA controller provides SA0 during DMA operations. When a master mode device asserts control on the system the SA0 pin on the HT25 in an input pin.

The HT25 supplies a 16 bit data bus, XD, which is compatible with the ISA system architecture. The HT25 provides for the proper byte steering for accessing 8 bit devices on the bus and converts 16 bit accesses into 2 cycles for 8 bit devices. Read data from the XD bus is latched in the HT25 for proper synchronization to the CPU bus. All CPU cycles which are not system memory, NPU, Local Bus or internal HT25 register accesses are directed to this data bus.

For systems which need to buffer the XD bus or support a 5V ISA I/O bus (SD data bus) three signals, BUFE*, SDLDIR and SDHDIR, are provided. These signals are used to control buffers or 3V to 5V translators as shown in Figure 11. BUFE* is used to disable the buffers/translators when not in use to save power. SDLDIR and SDHDIR are used as direction controls for the buffers/translators. BUFE* can also be used to disable any buffers on the SA and control signals. BUFE* is always low unless the ISA Bus Speed Control register (index 22) has bit 7 set to 1. When the BUFE* function is enabled, the BUFE* signal is high for local bus cycles, local memory cycles, and any XD bus devices.

I/O devices with addresses 100h and above and all memory devices on the ISA bus are normally on the SD portion of the bus. The RTC and Keyboard Controller may be programmed, using the XD Bus Control Register (Index 24), to reside on the SD bus.

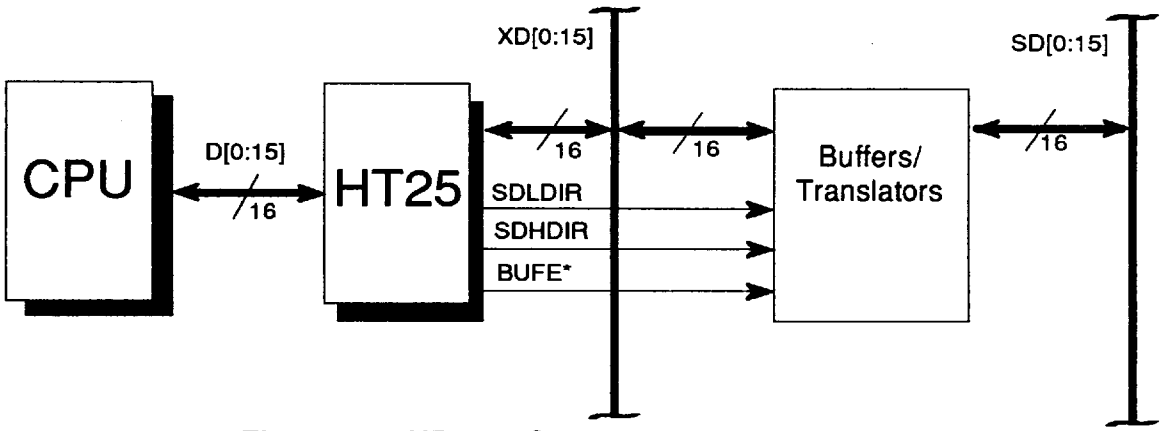


Figure 11 - XD and SD data bus architecture.

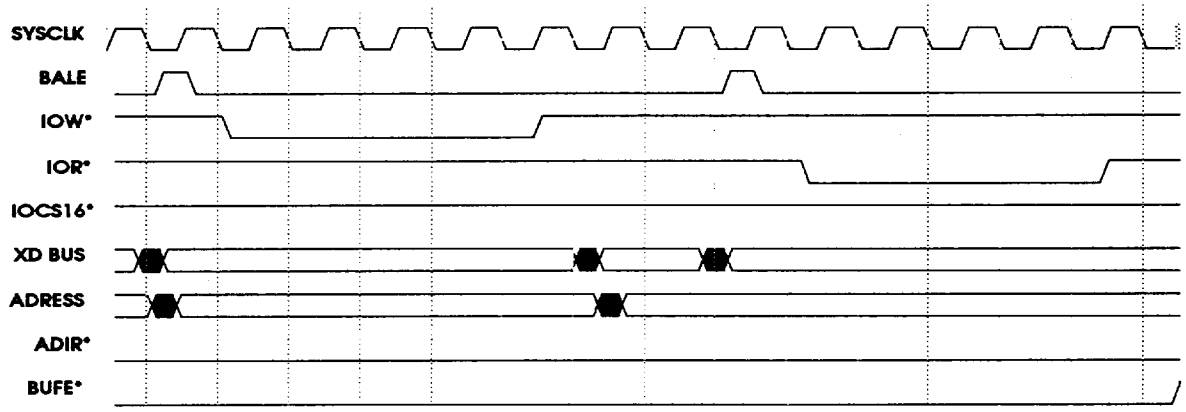


Figure 12a - ISA 8 Bit I/O Cycle

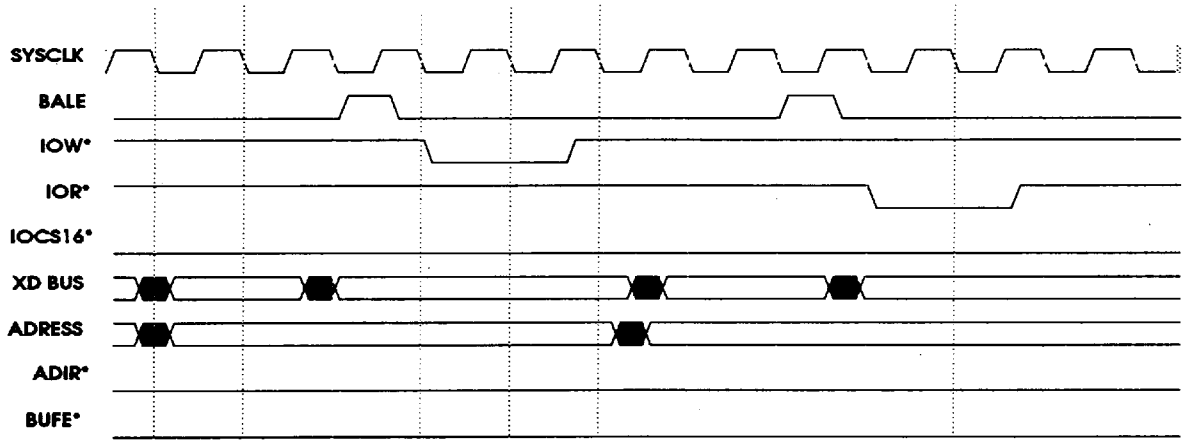


Figure 12b - ISA 16 Bit I/O Cycle

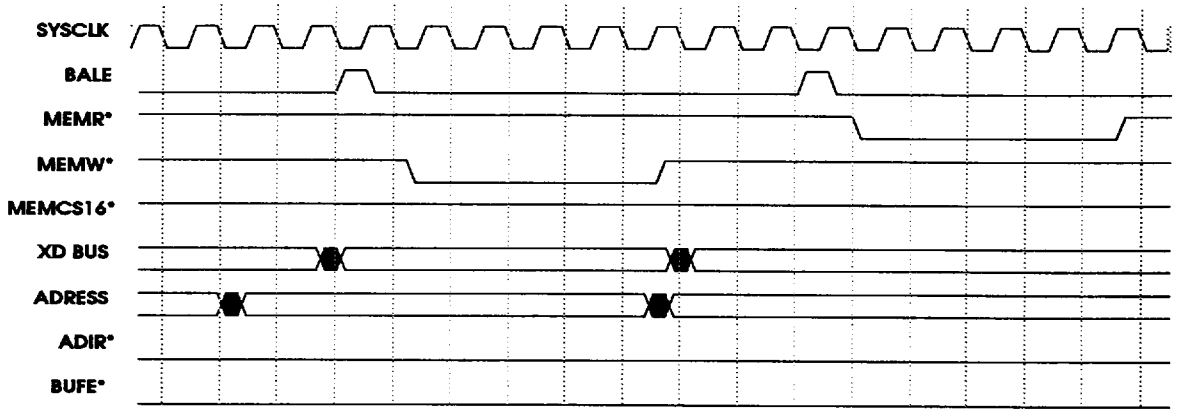


Figure 12c - ISA 8 Bit Memory Cycle

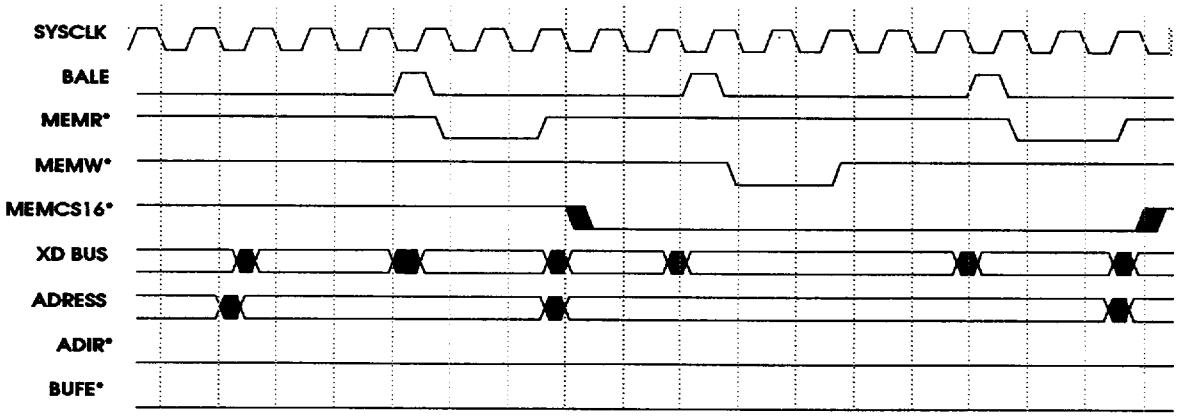


Figure 12d - ISA 16 Bit Memory Cycle

Any device which normally resides on the SD bus may acknowledge its presence on the XD bus by using the XDBUS* input pin on the HT25. This pin must be asserted by the device when it recognizes its address and command signal(s).

ISA Bus Control Signals

In addition to the signals for data and address bus buffering, the standard ISA system controls are provided. These are: AEN, BALE, DACK(0-3,5-7), DRQ(0-3,5-7), IOCHCK*, IOCHRDY, IOCS16*, IOR*, IOW*, IRQ(3-7, 9-7, 14, 15), MASTER*, MEMCS16*, MEMR*, MEMW*, REFRESH*, RESET, SMEMR*, SMEMW*, SYSCLK, TC. These signals are described in the Pin Description section of this document.

BIOS ROM Interface

The BIOS ROM resides on the XD bus and is connected to the HT25 as shown in Figure 13. ROMCS* is asserted when the HT25 decodes a memory read in the ROM address range.

The ROM address is programmable and consists of System/User BIOS (0E0000h - 0FFFFFh), SMM BIOS (0E0000h - 0FFFFFh) and Video/User BIOS (0C0000h - 0DFFFFh) ranges. ROM Configuration Registers A and B (Index 16h and 17h) are used to program the ROM address ranges. ROM Configuration Register B is also used to select the number of wait states during a ROM access and the bus to which write commands to the ROM address range is directed. Refer to the Register Description section of this document for more details.

The HT25 supports the use of 16 bit or 8 bit BIOS ROMs on the XD bus. On power on reset, the HT25 defaults to the 16 bit ROM mode. When the CPU performs its initial ROM read at location FFFFF0h, the HT25 performs a 16 bit read and checks the data on the high byte of the XD bus (byte location FFFFF1h). If the value is not equal to FFh the HT25 completes the CPU read cycle (by asserting READY) and the HT25 remains in 16 bit ROM mode.

If, on the first ROM read, the data on the XD bus high byte is equal to FFh it is assumed that the data lines are not driven and pulled high. The HT25 then holds the CPU read cycle, switches into the 8-bit ROM mode and restarts the read cycle. Instruction fetches will be per-

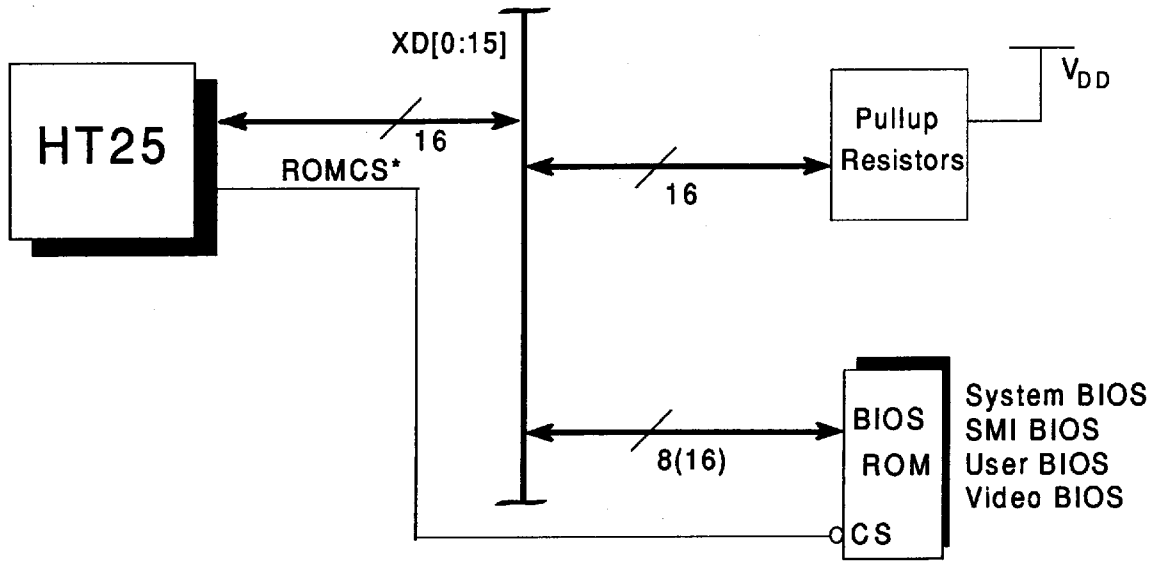


Figure 13 - HT25 BIOS ROM Interface

formed by the HT25 two bytes at a time from the XD bus low byte with the even byte (SA[0] = 0) being read first. The two bytes will then be presented to the CPU as 16 bit information.

Using this method, the information stored in location FFFFF1h cannot be FFh. Since, in an ISA environment, there is a far jump starting at location FFFFF0h there should not be a problem.

The ROM mode detected by the HT25 will be stored in the Miscellaneous Status Register (Index 1Fh), bit 2.

RTC/CMOS RAM Interface

The HT25 provides three command signals and an active low interrupt request input for a Motorola™ 146818 or compatible RTC. RTCAS, RTCRD* and RTCWR* are generated to control the AS, DS and R/W* inputs to the RTC. The IRQ8* input pin is inverted and connected to interrupt channel 8 of the HT25 interrupt controller.

RTCAS is an active high signal which is asserted during I/O writes to address 070h. In standard PC/AT systems it is used to access the index register in the RTC. RTCRD* is an active low signal which is asserted during I/O reads from address 071h. RTCWR* is an active low signal which is asserted during I/O writes to address 071h. RTCRD* and RTCWR* are intended to be used, in standard PC/AT systems, as the I/O read and write commands to the RTC.

Keyboard Controller Interface

The HT25 Keyboard Controller Interface consists of one command signal, one interrupt request signal and two input signals. This interface is designed to interact with a 8042 slave micro-controller which serves as the PC/AT system keyboard controller.

The command signal KBDCS*, is active during I/O operations to address 060h and 064h. It is intended to be used as the chip select for the keyboard controller.

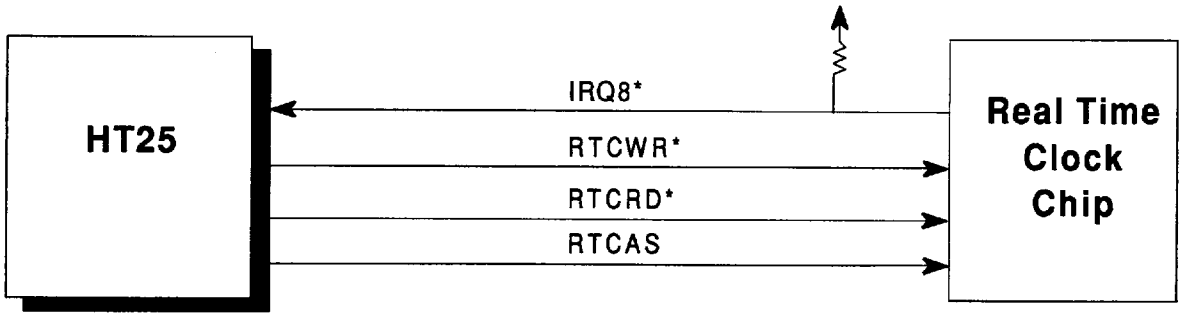


Figure 14 - Real Time Clock Interface

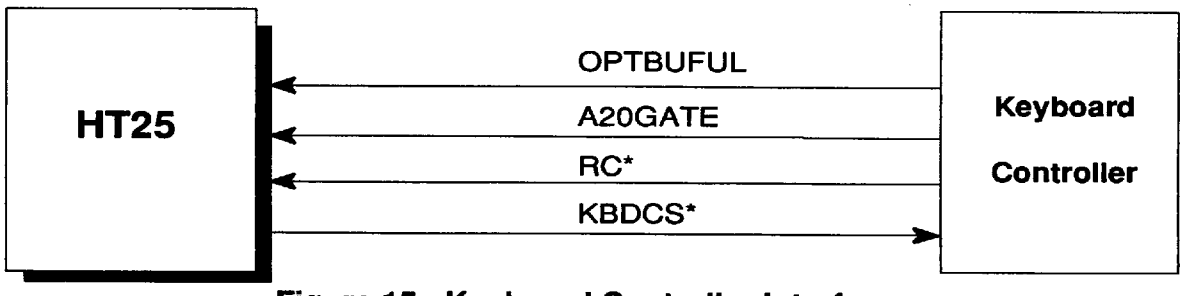


Figure 15 - Keyboard Controller Interface

OPTBUFUL furnishes the interrupt request number one to the HT25's interrupt controller. This signal is normally used to indicate that there is keyboard information in the keyboard controller for the system to read.

The input signal RC* is used by the HT25 to generate a reset to the system CPU. A20GATE is used by the HT25 to mask CPU address bit 20.

DMA Controller

The HT25 DMA controller is based on two 8237 compatible DMA controller modules. Each of the DMA modules generates a 16 bit address and control signals for DMA operations. The two DMA modules, DMA1 and DMA2, are cascaded resulting in seven usable DMA channels. Figure 16 shows a block diagram of the HT25 DMA controller.

DMA1 controls DMA channels 0-3 and its hold request is cascaded into DMA2. DMA1 is used for 8 bit DMA cycles. During DMA cycles on channels 0-3 the DMA controller module supplies address bits [0:15]. The DMA page registers for channels 0-3 provide address bits [16:23].

DMA2 controls DMA channels 5-7 with channel 4 being used for the hold request input from DMA1. DMA2 is used for 16 bit DMA cycles. Devices that are accessed during DMA cycles on channels 5-7 are assumed to be 16 bit devices. IOCS16* and MEMCS16* have no effect. During DMA cycles on channels 5-7 the DMA controller module supplies address bits [1:16]. The DMA page registers for channels 5-7 provide address bits [17:23]. Address bit 0 remains low during 16 bit DMA cycles.

The DMA modules operate as described in the Intel 8237™ Data Sheet with the following exceptions:

1. During DMA cycles the start of MEMR*is delayed by one clock cycle.
2. IOR* and MEMR* commands are extended by one SYSCLK cycle.
3. DMA cycles may be extended by use of IOCHRDY.

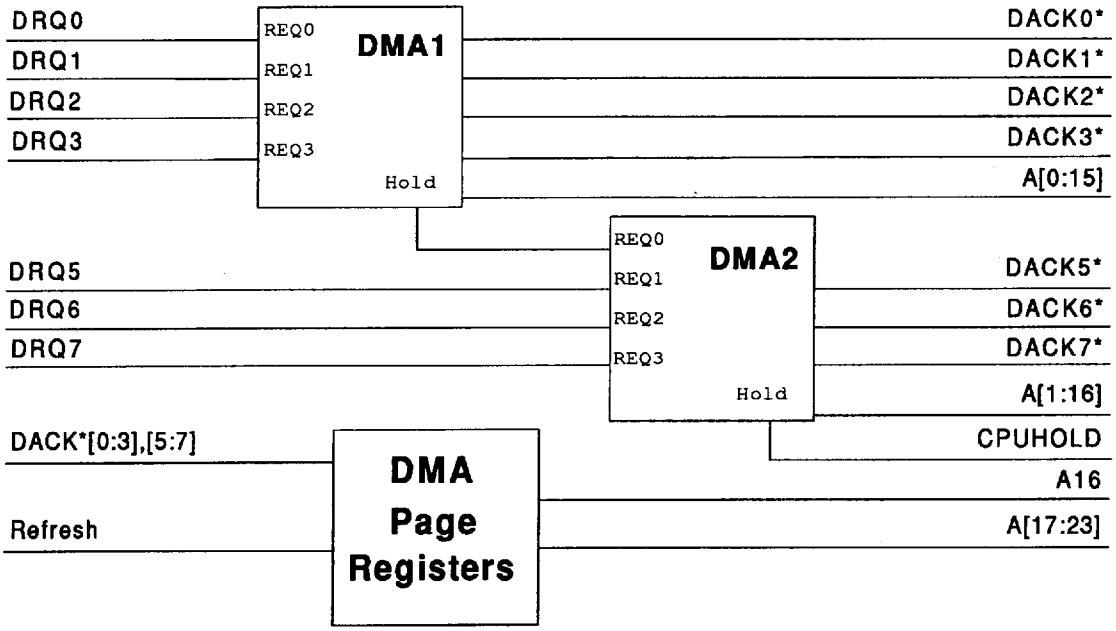


Figure 16 - HT25 DMA Controller

4. Memory-to-memory transfers are not supported.

A typical DMA cycle is shown in Figure 17.

DMA 1 is mapped into I/O address range 000h - 01Fh. DMA 1 is connected to A(0:3) for addressing of the internal registers. Since A(4) is not used I/O addresses 000h - 00Fh are duplicated in 010h - 01Fh.

DMA 2 is mapped into I/O address range 0C0h - 0DFh. The four bits used to address the internal registers in DMA 2 are connected to A(1:4). Since A(0) is not used the even and odd addresses in the 0C0h - 0DFh range access the same locations. The addresses for the DMA controller registers are shown in Table 12.

Addr Port	Read/ Write	Description
DMA Controller #1		
0000H	R/W	Channel 0 current address
0001H	R/W	Channel 0 current word count
0002H	R/W	Channel 1 current address
0003H	R/W	Channel 1 current word count
0004H	R/W	Channel 2 current address
0005H	R/W	Channel 2 current word count
0006H	R/W	Channel 3 current address
0007H	R/W	Channel 3 current word count
0008H	R/W	Command/Status Register
0009H	R/W	Request Register
000AH	R/W	Single Bit Mask Register
000BH	R/W	Mode Register
000CH	R/W	Clear Byte Pointer
000DH	R/W	Master Clear
000EH	R/W	Clear Mask Register
000FH	R/W	Write All Mask Register Bit

Table 12A - DMA Controller Register Addresses

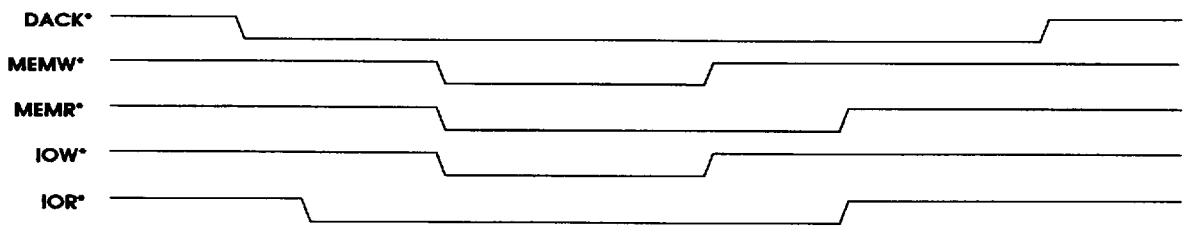


Figure 17 - DMA Functional Timing

Addr Port	Read/ Write	Description
DMA Controller #2		
00C0H	R/W	Channel 0 current address
00C4H	R/W	Channel 0 current word count
00C6H	R/W	Channel 1 current address
00C8H	R/W	Channel 1 current word count
00CAH	R/W	Channel 2 current address
00CCH	R/W	Channel 2 current word count
00CEH	R/W	Channel 3 current address
00CFH	R/W	Channel 3 current word count
00D0H	R/W	Command/Status Register
00D2H	R/W	Request Register
00D4H	R/W	Single Bit Mask Register
00D6H	R/W	Mode Register
00D8H	R/W	Clear Byte Pointer
00DAH	R/W	Master Clear
00DCH	R/W	Clear Mask Register
00DEH	R/W	Write All Mask Register Bit
000DFH-00EFH		Reserved

Table 12B - DMA Controller Register Addresses

The DMA Page Registers are mapped into I/O addresses 080h - 08Fh. The page registers for the DMA channels are shown in Table 13.

I/O Address	Page Register
080h	Not used
081h	DMA Channel 2
082h	DMA Channel 3
083h	DMA Channel 1
084h-086h	Not used
087h	DMA Channel 0
088h	Not used
089h	DMA Channel 6
08Ah	DMA Channel 7
08Bh	DMA Channel 5
08Ch-08Eh	Not used
08Fh	A[17:23] during Refresh cycles

Table 13 - DMA Page Register Addresses

Interrupt Controller

The HT25 Interrupt Controller is based on two 8259TM compatible Interrupt Controller Modules. Each of the Interrupt Controller Modules handles eight interrupt levels. The two interrupt controller modules, INT1 and INT2, are cascaded as shown in Figure 18. INT1 is configured as the master controller and INT2 as the slave controller. INT 1 provides interrupt levels 0-7 while INT2 provides interrupt levels 8-15. The interrupt generated by INT2 is cascaded into the Interrupt Request 2 (IRQ2) input of INT1.

The Interrupt Controller Modules operate as described in the Intel 8259 Data Sheet. INT1 is mapped into I/O addresses 020h and 021h. INT2 is mapped into I/O addresses 0A0h and 0A1h. The addresses for the interrupt controller registers is shown in Table 14.

Addr Port	Read/ Write	Description
Programmable Interrupt Controller #1		
0020H	W	ICW1
	W	OCW2
	W	OCW3
	R	Interrupt Request Register (IRR)
	R	In-Service Register (ISR)
	R	Polling Data Byte
0021H	W	ICW2
	W	ICW3
	W	ICW4
	W	OCW1
	R	Interrupt Mask Register (IMR)
0023H		Reserved
0024H	R/W	Configuration Data Port
0028H	R/W	Configuration Address Port
0029H-003FH		Reserved

Table 14A- Interrupt Controller Addresses

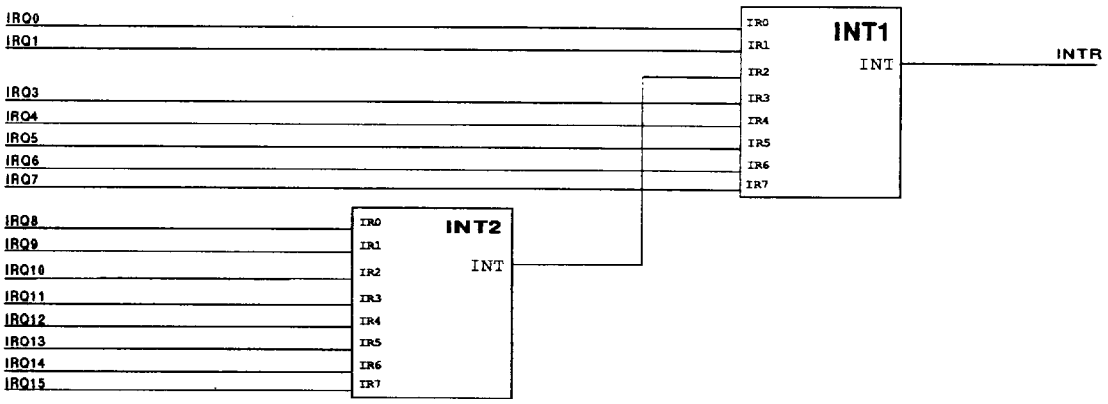


Figure 18 - HT25 Interrupt Controller

Addr Port	Read/ Write	Description
Programmable Interrupt Controller #2		
00A0H	W	ICW1
	W	OCW2
	W	OCW3
	R	Interrupt Request Register (IRR)
	R	In-Service Register (ISR)
	R	Polling Data Byte
00A1H	W	ICW2
	W	ICW3
	W	ICW4
	W	OCW1
	R	Interrupt Mask Register (IMR)

Table 14B - Interrupt Controller Addresses

Interrupt acknowledge cycles are performed at the CPU speed rather than at the ISA bus I/O speed.

The interrupt request inputs to INT1 and INT2 are connected as shown in Table 15.

Interrupt Request	Source
0	Programmable Interval Timer, output 0
1	OUTBUFUL input
2	Cascade input from INT2 to INT1
3-7	IRQ[3:7] inputs
8	Inverted IRQ8* input
9-12	IRQ[9:12] inputs
13	NPU error logic
14-15	IRQ[14:15]

Table 15 - Interrupt Requests

Programmable Interval Timer

The Programmable Interval Timer (PIT) is based on an 8254TM compatible Programmable Interval Timer module. The PIT contains three programmable 16-bit counters. A block diagram of the HT25 PIT is shown in Figure 19.

The PIT operates as described in the Intel 8254TM Data Sheet. It is mapped into I/O locations 040h-043h.

The output of counter 0 is connected to IRQ0 of the Interrupt Controller, counter 1 is used to generate the memory refresh requests. The output of counter 2 is gated by bit 1 of I/O port 061h (Port B register) to produce the SPKR output signal.

The gate inputs for counters 0 and 1 are high allowing the counters to run continuously. The gate input for counter 2 is bit 0 of I/O port 061h (Port B register).

The clock for the PIT is 1.19MHz generated by dividing the 14.318 MHz OSC input by 12. See Table 16 for the timer register addresses.

Addr Port	Read/ Write	Description
Timer/Counter		
0040H	R/W	Timer 0 Count Load/Read
0041H	R/W	Timer 1 Count Load/Read
0042H	R/W	Timer 2 Count Load/Read
0043H	W	Timer Control Word
0044H-005FH		Reserved

Table 16 - Timer Register Addresses

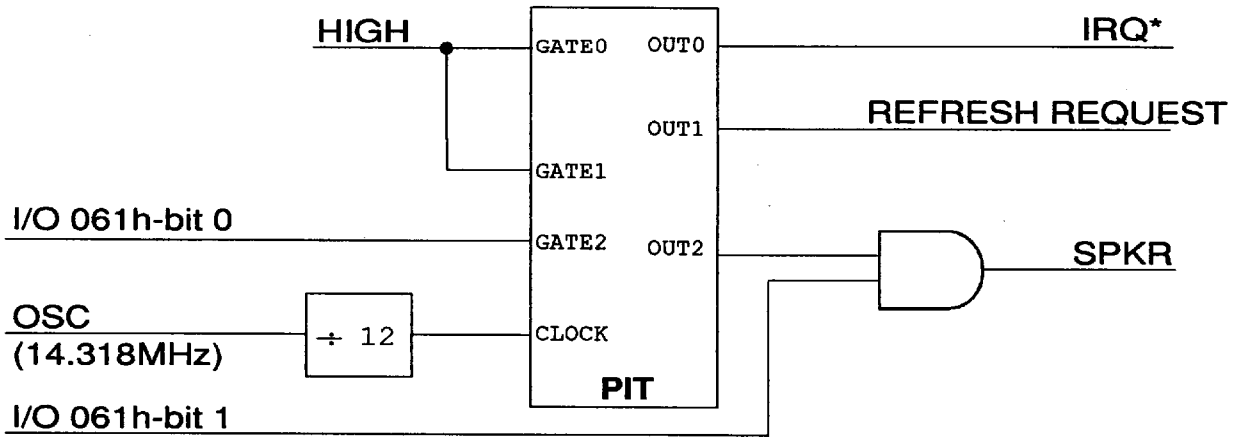


Figure 19 - HT25 Programmable Interval Timer

Master Mode

A device on the ISA bus can assume control of the system by requesting a DMA cycle and asserting the MASTER* signal when acknowledged. The HT25 will then respond to addresses and commands from the ISA bus master. All I/O and memory operations will be carried out by the HT25 with all bus buffer directions altered to support the ISA bus master.

An ISA bus master must manage the memory refresh for the system if MASTER* is asserted for more than 15uS. Refresh cycles in master mode are performed by asserting REFRESH* and holding it low until the end of the resulting MEMR* signal.

General Purpose I/O Ports

The HT25 provides programmable General Purpose I/O (GPIO), General Purpose Input (GPI) and General Purpose Output (GPO) ports.

There are eight GPIO pins (GPIO[0:7]) available on the HT25. They are independently programmable as input, output or I/O. The configurations for GPIO[0:7] are programmed using the GPIO Control Registers (Index B0h-B7h).

The state of the GPIO pins is available in the GPIO Control Registers. They can be programmed to set activity flags and generate an SMI on rising and/or falling edges. The inputs can also be debounced.

Each GPIO output pin has an output control. When disabled the GPIO pin is input only. GPIO0 and GPIO1 can serve as chip select outputs active for the Programmable Activity I/O Monitor 1 and 2 address range register at index A0H - A3H. The address range can be programmed from 1 to 16 sequential addresses.

DMA Request inputs 3 and 5-7 (DRQ3, DRQ[5:7]) can be programmed to be used as General Purpose Inputs (GPI[0:3]). When enabled, the GPI function replaces the DMA channel function. GPI[0:3] are programmed using GPI Control Registers 0-3 (Index B8h-BBh).

The state of the GPI pins is available in the GPI Control Registers. They can be programmed to set activity flags and generate an SMI on rising and/or falling edges. The inputs can also be debounced.

DMA Acknowledge outputs 3 and 5-7 (DACK3, DACK[5:7]) can be programmed to be used as General Purpose Outputs (GPO[0:3]). When enabled, the GPO function replaces the DMA channel function. GPO[0:3] are programmed using GPO Control Register 0-3 (Index BCh-BFh). Each GPO pin may be high, low or high impedance.

General Purpose Clock Channels (GPCC)

The HT25 provides four General Purpose Clock Channels (GPCC) to control peripheral clocks. They are controlled by the GPCC Control Registers (Index C0h-C3h). Each GPCC channel can buffer a clock without altering its frequency, divide by 2, 4, 8, 16, 32 or stop the clock completely.

General Purpose Clock Channels 0 and 1 have dedicated input (GPCCI0 and GPCCI1) and output (GPCCO0 and GPCCO1) pins. GPCC input pins for channels 2 and 3 are shared with DRQ0 and DRQ1. The output pins are shared with DACK0 and DACK1. When enabled, GPCC input and output pins for channels 2 and 3 replace DMA channel 0 and 1 control pins.

REGISTER DESCRIPTIONS

The HT25 contains three ISA compatible registers for system control, 74 indexed configuration registers and registers contained in the DMA Controller, Interrupt Controller, and Programmable Interval Timer. The I/O address map for the internal registers is shown in Table 16.

For a description of the DMA Controller, Interrupt Controller and Programmable Interval Timer see the ISA Controller section of this document.

Address	Register
000h-01Fh	DMA Controller Module 1
020h-02Fh	Interrupt Controller Module 1
040h-05Fh	Programmable Interval Timer
061h	Port B
070h	RTC Index and NMI Mask
080h-08Fh	DMA Page Registers
092h	Hot Reset/GATE A20
0A0h-0BFh	Interrupt Controller Module 2
0C0h-0DFh	DMA Controller Module 2
F0H	Clear BUSYCPU and PEREQCPU Latch
1EDh	Configuration Register Index
1EFh	Configuration Register Data

Table 17 - HT25 Register Address Map

ISA System Control Registers

Port B

I/O Address 061h

7	6	5	4	3	2	1	0
PTYCHK	IOCHK	TIM2OUT	REFDET	CHKMSK	PARMSK	SPKDAT	TIM2GT

Bit(s)	Access	Default	Description
7	R	0	Parity Error Status 0 = no error 1 = Parity Error has occurred in the DRAM.
6	R	0	I/O Channel Check error. 0 = no error occurred. 1 = I/O Channel Check on the ISA Bus is asserted.
5	R	-	This bit returns the state of Timer channel 2 output.
4	R	-	Refresh Detect. This bit toggles for each refresh Cycle.
3	R/W	0	I/O Channel Check Mask. 0 = enables I/O Channel Check error. 1 = disables I/O Channel Check error.
2	R/W	0	Memory parity error Mask. 0 = enable parity error generation. May be overridden by System Configuration Register (Index11h, bit 2). 1 = disable parity error generation.
1	R/W	0	This bit gates the output of timer channel 2 to produce the SPKR output signal. 0 = output disabled 1 = output enabled
0	R/W	0	This bit controls the operation of timer channel 2. 0 = operation disabled 1 = operation enabled

RTC Index and NMI Mask

I/O Address 070h

7	6	5	4	3	2	1	0
NMIMSK	XD(6)	XD(5)	XD(4)	XD(3)	XD(2)	XD(1)	XD(0)

Bit(s)	Access	Default	Description
7	W	1	NMI Mask 0 = NMI enabled 1 = NMI disabled
[6:0]	W	-	XD[6:0] - These bits are presented on the XD bus when the CPU writes to Address 070h. They are intended to be used for the index register in an external 146818 compatible Real Time Clock.

Note: The contents of this register may be read from the RTC Index and NMI Mask Shadow Register (Configuration Register Index D0h).

Fast Reset/Gate A20

I/O Address 092h

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	RES	A20GT	RCPU

Bits	Access	Default	Description
[7:2]	--		Reserved
1	R/W		Alternate A20 Gate. 0 = Forces A20 to a 0. 1 = A20CPU input is passed to A20.
0	R/W		Alternate CPU Reset 0 to 1 transition causes the CPU to be reset.RESETCPU to Pulse High.

Configuration Registers

The configuration registers are accessed through the two I/O ports at locations 1EDh and 1EFh. Port 1EDh serves as an index register in determining which configuration register is accessed at Port 1EFh. To access a configuration register, the corresponding index must first be written into the index register at location 1EDh. The register is then accessed at location 1EFh. The Configuration Registers are shown in Table 18.

Configuration Register — I/O Address 1EDh

7	6	5	4	3	2	1	0
INDX7	INDX6	INDX5	INDX4	INDX3	INDX2	INDX1	INDX0

Bit(s)	Access	Default	Description
[7:0]	R/W		Pointer for HT25 Configuration registers

Configuration Register Data — I/O Address 1EFh

7	6	5	4	3	2	1	0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0

Bit(s)	Access	Default	Description
[7:0]	-		Configuration register data to/from register at 1EDh pointer.

Index	Register
00h-01h	Revision Information Registers
10h-11h	DRAM Configuration Registers
14h-15h	Shadow RAM Configuration Registers
16h-17h	PROM Configuration Registers
1Fh	Miscellaneous Status Register
20h	LOCAL BUS Control Register
22h	ISA BUS Control Register
24h	XD BUS Control Register
28h-2Bh	Programmable Memory Control Registers
30h-31h	DRAM Control Registers
37h	Refresh Control Register
60h	EMS Configuration Register
62h	Top of Extended Memory Register
64h-6Bh	EMS Page Registers
80h	SMI Control Register
84h-89h	Activity Flag Registers
8Ah-8Fh	Activity Monitor SMI Enable Registers
90h-92h	CPU Doze Control Registers
94h	CPU Doze Status Register
96h	Doze Mode Interrupt Control Register
98h	CPU SPEED Control Register
9Ah	NPU SPEED Control Register
A0h-A3h	Programmable I/O Control Registers
B0h-B7h	GPIO Control Registers
B8h-BBh	GPI Control Registers
BCh-BFh	GPO Control Registers
C0h-C3h	GPCC Control Registers

Table 18 - HT25 Configuration Registers

Revision Information Register A — Index 00h

7	6	5	4	3	2	1	0
CHIP ID11	CHIP ID10	CHIP ID9	CHIP ID8	CHIP ID7	CHIP ID6	CHIP ID5	CHIP ID4

Bits	Access	Default	Description
[7:0]	R	-	Product Identification

Revision Information Register B — Index 01h

7	6	5	4	3	2	1	0
CHIP ID3	CHIP ID2	CHIP ID1	CHIP ID0	REV 3	REV 2	REV 1	REV 0

Bits	Access	Default	Description
[3:0]	R	01	Revision B
[7:4]	R	0	Identification

DRAM Configuration Register A — Index 10h

7	6	5	4	3	2	1	0
RAM TYPE1	RAM TYPE0	RES	RAM SEL4	RAM SEL3	RAM SEL2	RAM SEL1	RAM SEL0

Bits	Access	Default	Description
[4:0]	R/W	0	RAM Configuration (See Table 13)
5			Reserved
[7:6]	R/W	0	Memory Type 00 = DRAM 01 = Reserved 10 = Reserved 11 = Reserved

Configuration [4:0]		Banks 0	1	2	3	Total
00000	0	-	-	-	-	0K
00001	1	512K	-	-	-	1M
00010	2	512K	512K	-	-	2M
00011	3	512K	512K	512K	-	3M
00100	4	512K	512K	512K	512K	4M
00101	5	512K	1M	-	-	3M
00110	6	512K	1M	1M	-	5M
00111	7	512K	1M	1M	1M	7M
01000	8	512K	4M	-	-	9M
01001	9	512K	4M	4M	-	17M
01010	10	512K	512K	1M	-	4M
01011	11	512K	512K	1M	1M	6M
01100	12	512K	512K	4M	-	10M
01101	13	512K	512K	4M	4M	18M
01110	14	512K	512K	512K	1M	5M
01111	15	512K	512K	512K	4M	11M
10000	16	512K	1M	4M	-	11M
10001	17	512K	1M	4M	4M	19M
10010	18	1M	-	-	-	2M
10011	19	1M	1M	-	4M	
10100	20	1M	1M	1M	-	6M
10101	21	1M	1M	1M	1M	8M
10110	22	1M	4M	-	-	10M
10111	23	1M	1M	4M	-	12M
11000	24	1M	1M	1M	4M	14M
11001	25	1M	4M	4M	-	18M
11010	26	1M	1M	4M	4M	20M
11011	27	4M	-	-	-	8M
11100	28	4M	4M	-	-	16M
11101	29	-	-	-	-	Reserved
11110	30	-	-	-	-	Reserved
11111	31	-	-	-	-	Reserved

Table 19 - DRAM Configuration

DRAM Configuration Register B — Index 11h

7	6	5	4	3	2	1	0
RES	RES	RES	FLUSH	RES	PAR DIS	RELOC EN	SHAD EN

Bits	Access	Default	Description
[7:5]			Reserved
4	R/W	O	Flush Enable 0 = Disable 1 = Enable CPU cache flush. Forces FLUSH*, Pin 72 low.
3			Reserved
2	R/W	0	Memory Parity Control 0 = Enable Parity 1 = Disable parity - Overrides Port B (I/O Address 061h), bit 2.
1	R/W	0	Relocation Control 0 = Relocation Disabled 1 = Relocation Enabled 0A0000h-0FFFFh is relocated to the top of memory.
0	R/W	0	Master Shadow Control 0 = Shadowing Disabled 1 = Shadowing Enabled

Shadow RAM Configuration Register A — Index 14h

7	6	5	4	3	2	1	0
DC000h DFFFFh	D8000h DBFFFh	D4000h D7FFFh	D0000h D3FFFh	CC000h CFFFFh	C8000h CBFFFh	C4000h C7FFFh	C0000h C3FFFh

Bits	Access	Default	Description
7	R/W	0	DC000h-DFFFFh Shadow Control 0 = Disable Shadow 1 = Enable Shadow
6	R/W	0	D8000h-DBFFFh Shadow Control 0 = Disable Shadow 1 = Enable Shadow
5	R/W	0	D4000h-D7FFFh Shadow Control 0 = Disable Shadow 1 = Enable Shadow
4	R/W	0	D0000h-D3FFFh Shadow Control 0 = Disable Shadow 1 = Enable Shadow
3	R/W	0	CC000h-CFFFFh Shadow Control 0 = Disable Shadow 1 = Enable Shadow
2	R/W	0	C8000h-CBFFFh Shadow Control 0 = Disable Shadow 1 = Enable Shadow
1	R/W	0	C4000h-C7FFFh Shadow Control 0 = Disable Shadow 1 = Enable Shadow
0	R/W	0	C0000h-C3FFFh Shadow Control 0 = Disable Shadow 1 = Enable Shadow

Shadow RAM Configuration Register B — Index 15h

7	6	5	4	3	2	1	0
FC000h FFFFFh	F8000h FBFFFh	F4000h F7FFFh	F0000h F3FFFh	EC000h EFFFFh	E8000h EBFFFh	E4000h E7FFFh	E0000h E3FFFh

Bits	Access	Default	Description
7	R/W	0	FC000h-FFFFFh Shadow Control 0 = Disable 1 = Enable
6	R/W	0	F8000h-FBFFFh Shadow Control 0 = Disable 1 = Enable
5	R/W	0	F4000h-F7FFFh Shadow Control 0 = Disable 1 = Enable
4	R/W	0	F0000h-F3FFFh Shadow Control 0 = Disable 1 = Enable
3	R/W	0	EC000h-EFFFFh Shadow Control 0 = Disable 1 = Enable
2	R/W	0	E8000h-EBFFFh Shadow Control 0 = Disable 1 = Enable
1	R/W	0	E4000h-E7FFFh Shadow Control 0 = Disable 1 = Enable
0	R/W	0	E0000h-E3FFFh Shadow Control 0 = Disable 1 = Enable

PROM Configuration Register A

Index 16h

7	6	5	4	3	2	1	0
DC000h DFFFFh	D8000h DBFFFh	D4000h D7FFFh	D0000h D3FFFh	CC000h CFFFFh	C8000h CBFFFh	C4000h C7FFFh	C0000h C3FFFh

Bits	Access	Default	Description
7	R/W	0	Local ROM DC000h-DFFFFh Control 0 = Disable 1 = Enable
6	R/W	0	Local ROM D8000h-DBFFFh Control 0 = Disable 1 = Enable
5	R/W	0	Local ROM D4000h-D7FFFh Control 0 = Disable 1 = Enable
4	R/W	0	Local ROM D0000h-D3FFFh Control 0 = Disable 1 = Enable
3	R/W	0	Local ROM CC000h-CFFFFh Control 0 = Disable 1 = Enable
2	R/W	0	Local ROM C8000h-CBFFFh Control 0 = Disable 1 = Enable
1	R/W	0	Local ROM C4000h-C7FFFh Control 0 = Disable 1 = Enable
0	R/W	0	Local ROM C0000h-C3FFFh Control 0 = Disable 1 = Enable

PROM Configuration Register B — Index 17h

7	6	5	4	3	2	1	0
ROM WE	BIOS SIZE	SMI SIZE	RES	RES	RES	ROM WS1	ROM WS0

Bits	Access	Default	Description
7	R/W	0	ROM Write Address Bus Control 0 = Write to PROM space on SD bus 1 = Write to PROM space on XD bus
6	R/W	0	System BIOS Address Space 0 = 0E0000h-0FFFFFh 1 = 0F0000h-0FFFFFh
5	R/W	0	SMI ROM Address Space 0 = Same as System BIOS Address Space 1 = 0E0000h-0FFFFFh
[4:2]			Reserved
[1:0]	R/W	0	ROM Wait State Control 00 = 1 wait state 01 = 2 wait state 10 = 3 wait state 11 = 4 wait state

Miscellaneous Status Register

Index 1Fh

7	6	5	4	3	2	1	0
RES	RES	RES	RES	NPU INS	PROM WIDTH	NMI EN	8042 GA20

Bits	Access	Default	Description
[7:4]	R	-	Reserved
3	R		NPU Installed 0 = NPU not installed 1 = NPU installed
2	R	-	ROM Width 0 = 8 bit ROM 1 = 16 bit ROM
1	R	-	NMI Enable Status Shows the status of the Port 70 NMI Mask. 0 = NMI disabled 1 = NMI enabled
0	R	-	8042 Gate A20 Status Shows the status of the A20GATE Pin. 0 = A20 forced low 1 = A20 enabled

Local Bus Control Register

Index 20h

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	RES	LOCSP1	LOCSP0

Bits	Access	Default	Description
[7:2]			Reserved
[1:0]	R/W	00	LOCACK* Sampling Point. See Figure 16. 00 = Middle of first T2/T_{1P} 01 = End of first T2/T_{1P} 10 = Middle of second T2/T_{2P} 11 = End of second T2/T_{2P}

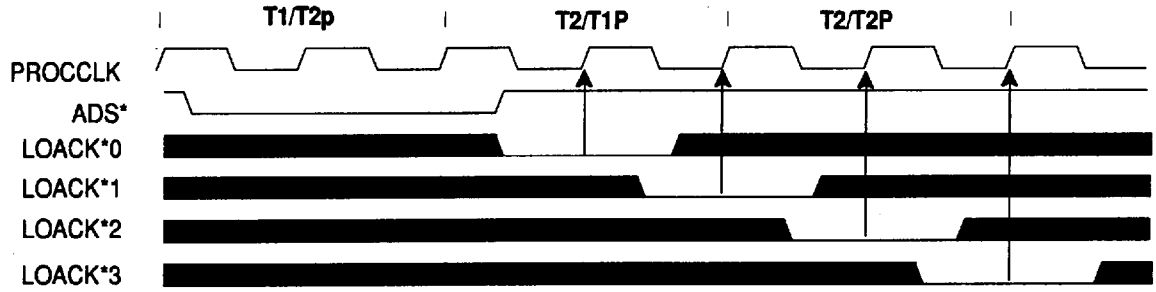


Figure 20 - LOCACK* Sampling Point

ISA Bus Speed Control Register

Index 22h

7	6	5	4	3	2	1	0
BUFEN	RES	RES	RES	RES	ISA SP2	ISA SP1	ISA SP0

Bits	Access	Default	Description
7	R/W	0	Buffer Enable Control 0 = BUFE* output (Pin 88) always asserted (LOW). 1 = BUFE* function enabled.BUFE* is high for local bus cycles, local memory cycles and XD bus cycles.
[6:3]			Reserved
[2:0]	R/W	100	ISA Clock Divider. The Sysclk frequency will be 1/2 of the ISA Clock frequency. Normally, select a divisor to make the ISA Clock close to 16MHz. 000 = CPUCLKIN/2 001 = CPUCLKIN/3 010 = CPUCLKIN/4 011 = CPUCLKIN/5 100 = CPUCLKIN/6 101 = Reserved 110 = Reserved 111 = Reserved

XD Bus Control Register — Index 24h

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	RES	KBCTL	RTC

Bits	Access	Default	Description
[7:2]			Reserved
1	R/W	0	Keyboard Controller Data Bus (IOR/IOW 60h, 62h-6Fh) 0 = XD 1 = SD
0	R/W	0	RTC Data Bus (IOR/IOW 70h-7Fh) 0 = XD 1 = SD

These bits allow the Real Time Clock or Keyboard Controller to be placed on either the XD or SD bus.

DRAM Control Register A

Index 30h

7	6	5	4	3	2	1	0
RTO EN	RES	RES	RES	RES	RES	RES	DRAM MODE

Bits	Access	Default	Description
7	R/W	0	RAS Timeout Control. 0 = Disable 1 = Enable The RAS signals will be forced high after the number of clocks programmed below. This saves power at the expense of performance.
[6:1]			Reserved
0	R/W	0	DRAM Timing Mode. 0 = Extended Timing Mode 1 = Standard Timing Mode

DRAM Control Register B

Index 31h

7	6	5	4	3	2	1	0
RTCC 4	RTCC 3	RTCC 2	RTCC 1	RTCC 0	RTOP 2	RTOP 1	RTOP 0

Bits	Access	Default	Description
[7:3]	R/W	0	RAS Timeout Count (RTCC) RAS Timeout = (RTCC + 1) x RAS Timeout Counter Period
[2:0]	R/W	0	RAS Timeout Counter Period 000 = 8 CPUCLKIN 001 = 16 CPUCLKIN 010 = 32 CPUCLKIN 011 = 64 CPUCLKIN 100 = 128 CPUCLKIN 101 = 256 CPUCLKIN 110 = 512 CPUCLKIN 111 = 1024 CPUCLKIN

Refresh Control Register — Index 37h

7	6	5	4	3	2	1	0
ISA REF	SELF REF	RES	RES	RES	RATE 2	RATE 1	RATE 0

Bits	Access	Default	Description
7	R/W	0	ISA Bus Refresh Control Only Local DRAM is refreshed when ISA Refresh is off. 0 = ISA Bus Refresh on 1 = ISA Bus Refresh off
6	R/W	0	Automatic Self Refresh Control Requires special DRAMs with self-refresh mode. Self-refresh will be started when the CPU Clock is stopped by Control Register Index 98h. 0 = Refresh mode unchanged during CPU clock stop 1 = Self-refresh mode selected during CPU clock stop
[5:3]	R/W		Reserved
[2:0]	R/W	0	Refresh Rate The output of the programmable timer is further divided to change the Refresh Rate without reprogramming the timer. 000 = Standard rate - as set by programmable timer output 1. 001 = Standard rate/2 010 = Standard rate/4 011 = Standard rate/8 100 = Standard rate/16 101 = Standard rate/32 110 = Standard rate/64 111 = Reserved
		Note:	Standard rate = 216/OSCIN = 15.6us (typical)

EMS Configuration Register

Index 60h

7	6	5	4	3	2	1	0
EMS EN	PAGE ADRR2	PAGE ADDR1	PAGE ADDR0	PAGE3 EN	PAGE2 EN	PAGE1 EN	PAGE0 EN

Bits	Access	Default	Description
7	R/W	0	Global EMS Control 0 = Disable EMS. All EMS pages are disabled. Over rides bits [0:3]. 1 = Enable EMS. EMS pages are enabled by bits [3:0].
[6:4]	R/W	0	EMS Page 0 Starting Address 000 = 0C0000h 001 = 0C4000h 010 = 0C8000h 011 = 0CC000h 100 = 0D0000h
3	R/W	0	EMS Page 3 Control 0 = Disable 1 = Enable
2	R/W	0	EMS Page 2 Control 0 = Disable 1 = Enable
1	R/W	0	EMS Page 1 Control 0 = Disable 1 = Enable
0	R/W	0	EMS Page 0 Control 0 = Disable 1 = Enable

Top Of Extended Memory Register — Index 62h

7	6	5	4	3	2	1	0
TA 23	TA 22	TA 21	TA 20	TA 19	TA 18	TA 17	TA 16

Bits	Access	Default	Description
[7:0]	R/W	00	Top of Extended Memory

This register specifies the top of extended memory. Extended memory address must be less than or equal to the Top of Memory setting. The memory above the Top of Extended Memory and below the total available memory can be used for EMS.

EMS Page 0 Register A

Index 64h

7	6	5	4	3	2	1	0
PA 21	PA 20	PA 19	PA 18	PA 17	PA 16	PA 15	PA 14

Bits	Access	Default	Description
[7:0]	R/W	-	Translated EMS address bits.

EMS Page 0 Register B

Index 65h

7	6	5	4	3	2	1	0
RES	RES	P0BK 1	P0BK 0	RES	RES	RES	PA 22

Bits	Access	Default	Description
[7:6]			Reserved.
[5:4]	R/W	-	EMS Page 0 Bank Select 00 = Logical Bank 0 01 = Logical Bank 1 10 = Logical Bank 2 10 = Logical Bank 3
[3:1]			Reserved.
0	R/W	-	Translated EMS address bit 22.

EMS Page 1 Register A

Index 66h

7	6	5	4	3	2	1	0
PA 21	PA 20	PA 19	PA 18	PA 17	PA 16	PA 15	PA 14

Bits	Access	Default	Description
[7:0]	R/W	-	Translated EMS address bits.

EMS Page 1 Register B

Index 67h

7	6	5	4	3	2	1	0
RES	RES	P1BK 1	P1BK 0	RES	RES	RES	PA 22

Bits	Access	Default	Description
[7:6]			Reserved.
[5:4]	R/W	-	EMS Page 1 Bank Select 00 = Logical Bank 0 01 = Logical Bank 1 10 = Logical Bank 2 11 = Logical Bank 3
[3:1]			Reserved.
0	R/W	-	Translated EMS address bit 22.

EMS Page 2 Register A

Index 68h

7	6	5	4	3	2	1	0
PA 21	PA 20	PA 19	PA 18	PA 17	PA 16	PA 15	PA 14

Bits	Access	Default	Description
[7:0]	R/W	-	Translated EMS address bits.

EMS Page 2 Register B

Index 69h

7	6	5	4	3	2	1	0
RES	RES	P2BK 1	P2BK 0	RES	RES	RES	PA 22

Bits	Access	Default	Description
[7:6]			Reserved.
[5:4]	R/W	-	EMS Page 2 Bank Select 00 = Logical Bank 0 01 = Logical Bank 1 10 = Logical Bank 2 11 = Logical Bank 3
[3:1]			Reserved.
0	R/W	-	Translated EMS address bit 22.

EMS Page 3 Register A — Index 6Ah

7	6	5	4	3	2	1	0
PA 21	PA 20	PA 19	PA 18	PA 17	PA 16	PA 15	PA 14

Bits	Access	Default	Description
[7:0]	R/W	-	Translated EMS address bits

EMS Page 3 Register B — Index 6Bh

7	6	5	4	3	2	1	0
RES	RES	P3BK 1	P3BK 0	RES	RES	RES	PA 22

Bits	Access	Default	Description
[7:6]			Reserved.
[5:4]	R/W	-	EMS Page 2 Bank Select 00 = Logical Bank 0 01 = Logical Bank 1 10 = Logical Bank 2 11 = Logical Bank 3
[3:1]			Reserved.
0	R/W	-	Translated EMS address bit 22.

SMI Control Register

Index 80h

7	6	5	4	3	2	1	0
SMI MASK	SMI EN	SMI INT3	SMI INT2	SMI INT1	SMI INT0	SMI SIZE1	SMI SIZE0

Bits	Access	Default	Description
7	R/W	0	SMI/NMI Mask Control 0 = SMI Mask is unaffected when NMI is masked. 1 = SMI is masked whenever NMI is masked.
6	R/W	0	SMI Control 0 = SMI disabled. SMI can only be cleared by enabling SMI. 1 = SMI Enabled.
[5:2]	R/W	0	Periodic SMI Interval 0000 = 9.15ms 1000 = 2.34 sec 0001 = 18.3ms 1001 = 4.69 sec 0010 = 36.6ms 1010 = 9.37 sec 0011 = 73.2ms 1011 = Reserved 0100 = 146ms 1100 = Reserved 0101 = 293ms 1101 = Reserved 0110 = 586ms 1110 = Reserved 0111 = 1.17 sec 1111 = Off
		Note:	Periodic SMI Interval = $\frac{2^{17} \times 2^{\text{SMI Interval [Bit2:5]}}}{\text{OSCIN}}$ Above intervals given for OSCIN = 14.318Mhz
[1:0]	R/W	0	SMI Memory Size 00 = 0K 01 = Reserved 10 = Reserved 11 = 64K

Activity Flag Register A — Index 84h

7	6	5	4	3	2	1	0
ISA	LPT3	LPT2	LPT1	COM4	COM3	COM2	COM1

Bits	Access	Default	Description
7	R	0	ISA Bus I/O Accesses (100h-3FFh) 0 = No activity 1 = Activity
6	R	0	Parallel Port I/O (3BCh-3BFh) 0 = No activity 1 = Activity
5	R	0	Parallel Port I/O (278h-27Fh) 0 = No activity 1 = Activity
4	R	0	Parallel Port I/O (378h-37Fh) 0 = No activity 1 = Activity
3	R	0	Serial Port I/O (2E8h-2EFh) 0 = No activity 1 = Activity
2	R	0	Serial Port I/O (3E8h-3EhF) 0 = No activity 1 = Activity
1	R	0	Serial Port I/O (2F8h-2FFh) 0 = No activity 1 = Activity
0	R	0	Serial Port I/O (3F8h-3FFh) 0 = No activity 1 = Activity

These registers are cleared when read.

Activity Flag Register B

Index 85h

7	6	5	4	3	2	1	0
IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	RES	IRQ1	IRQ0

Bits	Access	Default	Description
7	R	0	IRQ7
6	R	0	IRQ6
5	R	0	IRQ5
4	R	0	IRQ4
3	R	0	IRQ3
2	R	0	Reserved
1	R	0	IRQ1
0	R	0	IRQ0

Activity Flag Register C

Index 86h

7	6	5	4	3	2	1	0
IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8

Bits	Access	Default	Description
7	R	0	IRQ15
6	R	0	IRQ14
5	R	0	IRQ13
4	R	0	IRQ12
3	R	0	IRQ11
2	R	0	IRQ10
1	R	0	IRQ9
0	R	0	IRQ8

Activity Flag Register D

Index 87h

7	6	5	4	3	2	1	0
RES	NPU	LOCAL	IOCHK	HD	FD	VIDEO	KBCTL

Bits	Access	Default	Description
7	R	0	Reserved
6	R	0	NPU Cycle
5	R	0	Local Bus Device Cycle
4	R	0	IOCHCK*
3	R	0	Hard Disk Access (I/O1F0h-1F7h)
2	R	0	Floppy Access (I/O 3F5h)
1	R	0	Video Memory Space (MEMW A0000h-BFFFFh)
0	R	0	Keyboard Controller I/O (060h R/W, 064h W)

Activity Flag Register E

Index 88h

7	6	5	4	3	2	1	0
GPI3	GPI2	GPI1	GPI0	RES	RES	PIO2	PIO1

Bits	Access	Default	Description
7	R		GPI3 This activity flag is set when there is activity on GPI3 (See Index BBh)
6	R		GPI2 This activity flag is set when there is activity on GPI2 (See Index BAh)
5	R		GPI1 This activity flag is set when there is activity on GPI1 (See Index B9h)
4	R		GPI0 This activity flag is set when there is activity on GPI0 (See Index B8h)
[3:2]	R		Reserved
1	R		Programmable I/O 2 This activity flag is set when Programmable I/O Monitor 2 is active. (See Index A2h, A3h)
0	R		Programmable I/O 1 This activity flag is set when Programmable I/O Monitor 1 is active. (See Index A0h, A1h)

Activity Flag Register F

Index 89h

7	6	5	4	3	2	1	0
GPIO 7	GPIO 6	GPIO 5	GPIO 4	GPIO 3	GPIO 2	GPIO 1	GPIO 0

Bits	Access	Default	Description
7	R	0	GPIO 7 Activity
6	R	0	GPIO 6 Activity
5	R	0	GPIO 5 Activity
4	R	0	GPIO 4 Activity
3	R	0	GPIO 3 Activity
2	R	0	GPIO 2 Activity
1	R	0	GPIO 1 Activity
0	R	0	GPIO 0 Activity

Activity Monitor SMI Enable Register A — Index 8Ah

7	6	5	4	3	2	1	0
ISA SMI	LPT3 SMI	LPT2 SMI	LPT1 SMI	COM4 SMI	COM3 SMI	COM2 SMI	COM1 SMI

Bits	Access	Default	Description
7	R/W	0	ISA Bus I/O Accesses (100h-3FFh) SMI Control 0 = Disable 1 = Enable
6	R/W	0	Parallel Ports I/O (3BCh-3BFh) SMI Control 0 = Disable 1 = Enable
5	R/W	0	Parallel Ports I/O (278h-27Fh) SMI Control 0 = Disable 1 = Enable
4	R/W	0	Parallel Ports I/O (378h-37Fh) SMI Control 0 = Disable 1 = Enable
3	R/W	0	Serial Port I/O (2E8h-2EFh) SMI Control 0 = Disable 1 = Enable
2	R/W	0	Serial Port I/O (3E8h-3EFh) SMI Control 0 = Disable 1 = Enable
1	R/W	0	Serial Port I/O (2F8h-2FFh) SMI Control 0 = Disable 1 = Enable
0	R/W	0	Serial Port I/O(3F8h-3FFh) SMI Control 0 = Disable 1 = Enable

Activity Monitor SMI Enable Register B — Index 8Bh

7	6	5	4	3	2	1	0
IRQ7 SMI	IRQ6 SMI	IRQ5 SMI	IRQ4 SMI	IRQ3 SMI	RES	IRQ1 SMI	IRQ0 SMI

Bits	Access	Default	Description
7	R/W	0	IRQ7 SMI Control 0 = Disable 1 = Enable
6	R/W	0	IRQ6 SMI Control 0 = Disable 1 = Enable
5	R/W	0	IRQ5 SMI Control 0 = Disable 1 = Enable
4	R/W	0	IRQ4 SMI Control 0 = Disable 1 = Enable
3	R/W	0	IRQ3 SMI Control 0 = Disable 1 = Enable
2	R	0	Reserved
1	R/W	0	IRQ1 SMI Control 0 = Disable 1 = Enable
0	R/W	0	IRQ0 SMI Control 0 = Disable 1 = Enable

Activity Monitor SMI Enable Register C — Index 8Ch

7	6	5	4	3	2	1	0
IRQ15 SMI	IRQ14 SMI	IRQ13 SMI	IRQ12 SMI	IRQ11 SMI	IRQ10 SMI	IRQ9 SMI	IRQ8 SMI

Bits	Access	Default	Description
7	R/W	0	IRQ15 SMI Control 0 = Disable 1 = Enable
6	R/W	0	IRQ14 SMI Control 0 = Disable 1 = Enable
5	R/W	0	IRQ13 SMI Control 0 = Disable 1 = Enable
4	R/W	0	IRQ12 SMI Control 0 = Disable 1 = Enable
3	R/W	0	IRQ11 SMI Control 0 = Disable 1 = Enable
2	R/W	0	IRQ10 SMI Control 0 = Disable 1 = Enable
1	R/W	0	IRQ9 SMI Control 0 = Disable 1 = Enable
0	R/W	0	IRQ8 SMI Control 0 = Disable 1 = Enable

Activity Monitor SMI Enable Register D

Index 8Dh

7	6	5	4	3	2	1	0
RES	RES	RES	IOCHK SMI	HD SMI	FD SMI	VIDEO SMI	KBCTL SMI

Bits	Access	Default	Description
[7:5]			Reserved
4	R/W	0	IOCHCK* SMI Control 0 = Disable 1 = Enable
3	R/W	0	Hard Disk Access SMI Control 1F0h-1FFh, 3F6h-3F7h 0 = Disable 1 = Enable
2	R/W	0	Floppy Access SMI Control (3F0h-3F7h) 0 = Disable 1 = Enable
1	R/W	0	Video Memory Space (MEMW A0000h-BFFFFh) SMI Control 0 = Disable 1 = Enable
0	R/W	0	Keyboard controller output buffer (60h) read SMI Control 0 = Disable 1 = Enable

Activity Monitor SMI Enable Register E

Index 8Eh

7	6	5	4	3	2	1	0
GPI3 SMI	GPI2 SMI	GPI1 SMI	GPI0 SMI	RES	RES	PIO2 SMI	PIO1 SMI

Bits	Access	Default	Description
7	R/W	0	GPI3 SMI Control 0 = Disable 1 = Enable
6	R/W	0	GPI2 SMI Control 0 = Disable 1 = Enable
5	R/W	0	GPI1 SMI Control 0 = Disable 1 = Enable
4	R/W	0	GPI0 SMI Control 0 = Disable 1 = Enable
[3:2]			Reserved
1	R/W	0	Programmable I/O Range 2 SMI Control 0 = Disable 1 = Enable
0	R/W	0	Programmable I/O Range 1 SMI Control 0 = Disable 1 = Enable

Activity Monitor SMI Enable Register F — Index 8Fh

7	6	5	4	3	2	1	0
GPIO 7 SMI	GPIO 6 SMI	GPIO 5 SMI	GPIO 4 SMI	GPIO 3 SMI	GPIO 2 SMI	GPIO 1 SMI	GPIO 0 SMI

Bits	Access	Default	Description
7	R/W	0	GPIO 7 SMI Control 0 = Disable 1 = Enable
6	R/W	0	GPIO 6 SMI Control 0 = Disable 1 = Enable
5	R/W	0	GPIO 5 SMI Control 0 = Disable 1 = Enable
4	R/W	0	GPIO 4 SMI Control 0 = Disable 1 = Enable
3	R/W	0	GPIO 3 SMI Control 0 = Disable 1 = Enable
2	R/W	0	GPIO 2 SMI Control 0 = Disable 1 = Enable
1	R/W	0	GPIO 1 SMI Control 0 = Disable 1 = Enable
0	R/W	0	GPIO 0 SMI Control 0 = Disable 1 = Enable

CPU Doze Control Register A — Index 90h

7	6	5	4	3	2	1	0
CPM EN	RES	RES	SMI SEL	LOCAL SEL	VIDEO SEL	KB SEL	ISA SEL

Bits	Access	Default	Description
7	R/W	0	CPU Doze Control 0 = Disable 1 = Enable
[6:5]	R/W		Reserved
4	R/W	0	Non-Periodic SMI 0 = Select 1 = Deselect When selected non-periodic SMI are considered activities and the CPU would not go into doze speed.
3	R/W	0	Local Bus Peripheral Cycles 0 = Select 1 = Deselect When selected local bus peripheral cycles are considered activities and the CPU would not go into doze speed.
2	R/W	0	Video Writes 0 = Select 1 = Deselect When selected video writes are considered activities and the CPU would not go into doze speed.
1	R/W	0	Keyboard Controller Output Buffer Reads 0 = Select 1 = Deselect When selected keyboard controller output buffer reads are considered activities and the CPU would not go into doze speed.
0	R/W	0	ISA Bus I/O (100h-3FFh) 0 = Select 1 = Deselect When selected ISA bus I/O accesses to 100h-3FFh are considered activities and the CPU would not go into doze speed.

CPU Doze Control Register B

Index 91h

7	6	5	4	3	2	1	0
RES	RES	DOZE SP1	DOZE SP0	RES	CPU IDLE2	CPU IDLE1	CPU IDLE0

Bits	Access	Default	Description
[7:6]	R/W	0	Reserved
[5:4]	R/W	0	Doze Speed 00 = Doze speed = Normal Speed / 2 01 = Doze speed = Normal Speed / 4 10 = Doze speed = Normal Speed / 8 11 = Doze speed = Normal Speed / 16
3			Reserved
[2:0]	R/W	0	CPU Doze Timeout 000 = 73.2ms 001 = 146ms 010 = 293ms 011 = 586ms 100 = 1.17 sec 101 = 2.34 sec 110 = 4.69 sec 111 = 9.37 sec

Note: $\text{CPU Doze Timeout} = \frac{2^{20} \times 2^{\text{CPU Doze Timeout [Bit0:2]}}}{\text{OSCIN}}$

Above intervals given for OSCIN = 14.318MHz

CPU Doze Control Register C — Index 92h

7	6	5	4	3	2	1	0
RES	RES	SUSP CLK	HALT CLK	HLDA CLK	IO CLK	DMA CLK	OSC CLK

Bits	Access	Default	Description
[7:6]	R/W		Reserved
5	R/W	O	Stop CPU Clock enable on SUSP* initiated suspend cycles (This bit works together with bit 7 of Register 98h for Cyrix CPU only) 0 = Disable 1 = Enable
4	R/W	O	Stop CPU Clock enable on halt cycles 0 = Disable 1 = Enable
3	R/W	O	Stop CPU Clock on HLDA cycles 0 = Disable 1 = Enable
2	R/W	0	Stop CPU Clock Control during ISA Bus I/O Cycles. 0 = Disable 1 = Enable
1	R/W	0	DMA Clock Control (Stop DMA Clock on non-DMA cycles) 0 = Disable 1 = Enable
0	R/W	0	OSC (14.318MHz) Clock Control 0 = Disable 1 = Enable When enabled OSC stopped when CPU clock stop bit (Index 98h, bit 7) is set.

CPU Doze Status Register

Index 94h

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	SMI CYC	CPM ACT	DOZE

Bits	Access	Default	Description
[7:3]	R		Reserved
2	R		SMI Cycle Status 0 = CPU in normal mode 1 = CPU in SMI mode This bit is set when the CPU returns and SMIADS* and remains set until the CPU completes its state restore and the SMI* signal returns high.
1	R		CPU Activity Status 0 = No CPU Activity since last read. 1 = CPU Activity detected since last read. Note:This bit is cleared when read.
0	R		Doze Status 0 = Normal State 1 = Doze State

Interrupt Clock Control Register — Index 96h

7	6	5	4	3	2	1	0
IPM EN	RES	RES	RES	RES	INT TIME2	INT TIME1	INT TIME0

Bits	Access	Default	Description
7	R/W	0	Doze Mode Interrupt Control When enabled the CPU clock will restart after an interrupt for the time programmed below then the CPU Clock will stop. This register has no effect if Control Register Index 98h, Bit 7 is 0. 0 = Disable 1 = Enable
[6:3]		0	Reserved - Must be set 000.
[2:0]	R/W	0	Interrupt Service Time 000 = 1.14ms 001 = 2.29ms 010 = 4.58ms 011 = 9.15ms 100 = 18.3ms 101 = 36.6ms 110 = 73.2ms 111 = Reserved

CPU Speed Control Register

Index 98h

7	6	5	4	3	2	1	0
CPU STOP	RES	CPU LSP2	CPU LSP1	CPU LSP0	CPU HSP2	CPU HSP1	CPU HSP0

Bits	Access	Default	Description
7	R/W	0	CPU Clock Stop Control 0 = Run 1 = Stop
6			Reserved
[5:3]	R/W	0	Normal CPU and NPU Speed when HISPEED (Pin 76) input is low 000 = PROCCLK = CPUCLKIN 001 = PROCCLK = CPUCLKIN/2 010 = PROCCLK = CPUCLKIN/4 011 = PROCCLK = CPUCLKIN/8 100 = PROCCLK = CPUCLKIN/16 101 = PROCCLK = CPUCLKIN/32 110 = Reserved 111 = Reserved
[2:0]	R/W	0	Normal CPU and NPU Speed when HISPEED (Pin 76) input is high 000 = PROCCLK = CPUCLKIN 001 = PROCCLK = CPUCLKIN/2 010 = PROCCLK = CPUCLKIN/4 011 = PROCCLK = CPUCLKIN/8 100 = PROCCLK = CPUCLKIN/16 101 = PROCCLK = CPUCLKIN/32 110 = Reserved 111 = Reserved

NPU Speed Control Register — Index 9Ah

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	RES	RES	NPU STOP

Bits	Access	Default	Description
[7:1]			Reserved
0	R/W	0	NPU Clock Stop Control 0 = Run 1 = Stop

Programmable I/O 1 Control Register A

Index A0h

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Bits	Access	Default	Description
[7:0]	R/W		I/O Address

Programmable I/O 1 Control Register B

Index A1h

7	6	5	4	3	2	1	0
A9	A8	IOW EN	IOR EN	MASKA3	MASKA2	MASKA1	MASKA0

Bits	Access	Default	Description
[7:6]	R/W		I/O Address
5	R/W	0	I/O Write Control 0 = Disable write monitoring 1 = Set activity flag or chip select on write
4	R/W	0	I/O Read Control 0 = Disable read monitoring 1 = Set activity flag or chip select on read
3 2 1 0	R/W		I/O Address Mask 0 = Address Bit must match 1 = Address Bit will not be compared.

Programmable I/O 2 Control Register A — Index A2h

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Bits	Access	Default	Description
[7:0]	R/W		I/O Address

Programmable I/O 2 Control Register B — Index A3h

7	6	5	4	3	2	1	0
A9	A8	IOW EN	IOR EN	MASKA3	MASKA2	MASKA1	MASKA0

Bits	Access	Default	Description
[7:6]	R/W		I/O Address
5	R/W	0	I/O Write Control 0 = Disable write monitoring 1 = Set activity flag or chip select on write
4	R/W	0	I/O Read Control 0 = Disable read monitoring 1 = Set activity flag or chip select on read
3 2 1 0	R/W		I/O Address Mask 0 = Address Bit must match 1 = Address Bit will not be compared.

GPIOx Control Register

Index B0h - B1h

7	6	5	4	3	2	1	0
PCS SENSE	PCS EN	DBNC EN	SMI FALL	SMI RISE	OUT EN	DATA OUT	DATA IN

Bits	Access	Default	Description
7	R/W	O	Chip Select Sense 0 = Active low 1 = Active high
6	R/W	O	Programmable Chip Select 0 = Disable 1 = Programmable chip select output. GPIOx is asserted when the CPU accesses addresses in the range specified in the Programmable I/O Control Register x, when bit 2 is set. The active state of the chip select is defined in bit 7.
5	R/W	0	Debounce Control 0 = No debounce (Disable) 1 = 18.3ms debounce (Enable)
4	R/W	0	SMI on Falling Edge 0 = Disable 1 = Generate SMI on GPIOx input rising edge. SMI Control Register (Index 80h), bit 6 and Activity Monitor SMI Enable Register F (Index 8Fh), bit x.
		Note:	Must be set to generate an SMI.
3	R/W	0	SMI on Rising Edge 0 = Disable 1 = Generate SMI on GPIOx input rising edge. SMI Control Register (Index 80h), bit 6 and Activity Monitor SMI Enable Register F (Index 8Fh), bit x must be set to generate an SMI
2	R/W	0	Output Control 0 = High impedance 1 = Enable output for data or chip select

Bits	Access	Default	Description
1	R/W	-	Data Output This bit contains the data presented on the GPIOx pin when bit 2 is set.
		Note:	must be set to generate an SMI
0	R	-	Data Input This bit contains the data present at the GPIOx pin.

GPIO2-7

Index B2h-B7h

7	6	5	4	3	2	1	0
RES	RES	DBNC EN	SMI FALL	SMI RISE	OUT EN	DATA OUT	DATA IN

Bits	Access	Default	Description
[7:6]			Reserved
5	R/W	O	Debounce Control (when enabled, HT25 debounced switching noise of 18.3ms or shorter 0 = Disable 1 = Enable
4	R/W	O	SMI on Falling Edge (SMI generated only if the SMI enable bit is set) 0 = Disable 1 = Enable
3	R/W	O	SMI on Rising Edge (SMI is generated only if the SMI enable bit is set) 0 = Disable 1 = Enable
2	R/W	O	Port output Control 0 = Disable 1 = Enable
1	R/W	-	Data output (This bit contains the data on the pin when port is configured as an output port.)
0	R	-	Data input (This bit contains the data present at the pin when the port is configured as an input port.)

GPI0 Control Register — Index B8h
GPI1 Control Register — Index B9h
GPI2 Control Register — Index BAh
GPI3 Control Register — Index BBh

7	6	5	4	3	2	1	0
GPI EN	RES	DBNC EN	SMI FALL	SMI RISE	RES	RES	DATA IN

Bits	Access	Default	Description
7	R/W	0	GPI Enable When enabled, the corresponding DMA pin is used as a GPI pin. The pin mapping is as the follows 0 = Disable DRQ3 GPI0 1 = Enable DRQ5 GPI1 DRQ6 GPI2 DRQ7 GPI3
6			Reserved
5	R/W	0	Debounce Control When enabled, the HT25 debounces switching noise of 18.3ms or shorter. 0 = Disable 1 = Enable
4	R/W	0	SMI on Falling Edge An SMI is generated only if the SMI Enable bit is set. 0 = Disable 1 = Enable
3	R/W	0	SMI on Rising Edge An SMI is generated only if the SMI Enable bit is set. 0 = Disable 1 = Enable
[2:1]			Reserved
0	R	-	Data Input This bit contains the data present at the pin when the port is configured as an input port.

GPO0 Control Register — Index BCh
GPO1 Control Register — Index BDh
GPO2 Control Register — Index BEh
GPO3 Control Register — Index BFh

7	6	5	4	3	2	1	0
GPO EN	RES	RES	RES	RES	OUT EN	DATA OUT	RES

Bits	Access	Default	Description
7	R/W	0	GPO Enable When enabled, the corresponding DMA pin is used as a GPO pin. 0 = Disable 1 = Enable The pin mapping is as the follows DACK3 GPO0 DACK5 GPO1 DACK6 GPO2 DACK7 GPO3
[6:3]			Reserved
2	R/W	0	Port Output Logic Control 0 = Disable 1 = Enable When the output logic is disabled the pin is tri-stated.
1	R/W	-	Data Output This bit contains the data on the pin when the port is configured as an output port.
0			Reserved

GPCC0 Control Register — Index C0h
GPCC1 Control Register — Index C1h
GPCC2 Control Register — Index C2h
GPCC3 Control Register — Index C3h

7	6	5	4	3	2	1	0
GPCCEN	RES	RES	RES	GPCC3	GPCC2	GPCC1	GPCC0

Bits	Access	Default	Description
7	R/W	0	GPCC0-GPCC1 Reserved GPCC2 0 = disabled - pin 138 is DRQ0 pin 139 is DACK0* 1 = enabled - pin 138 is GPCCI2 pin 139 is GPCCO2 GPCC3 0 = disabled - pin 140 is DRQ1 pin 141 is DACK1* 1 = enabled - pin 140 is GPCCI3 pin 141 is GPCCO3
[6:4]			Reserved
[3:0]	R/W	0	Output Clock Control 0000 = Output = Input 1000 = Reserved 0001 = Output = Input/2 1001 = Reserved 0010 = Output = Input/4 1010 = Reserved 0011 = Output = Input/8 1011 = Reserved 0100 = Output = Input/16 1100 = Reserved 0101 = Output = Input/32 1101 = Reserved 0110 = Reserved 1110 = Reserved 0111 = Reserved 1111 = Output = 0

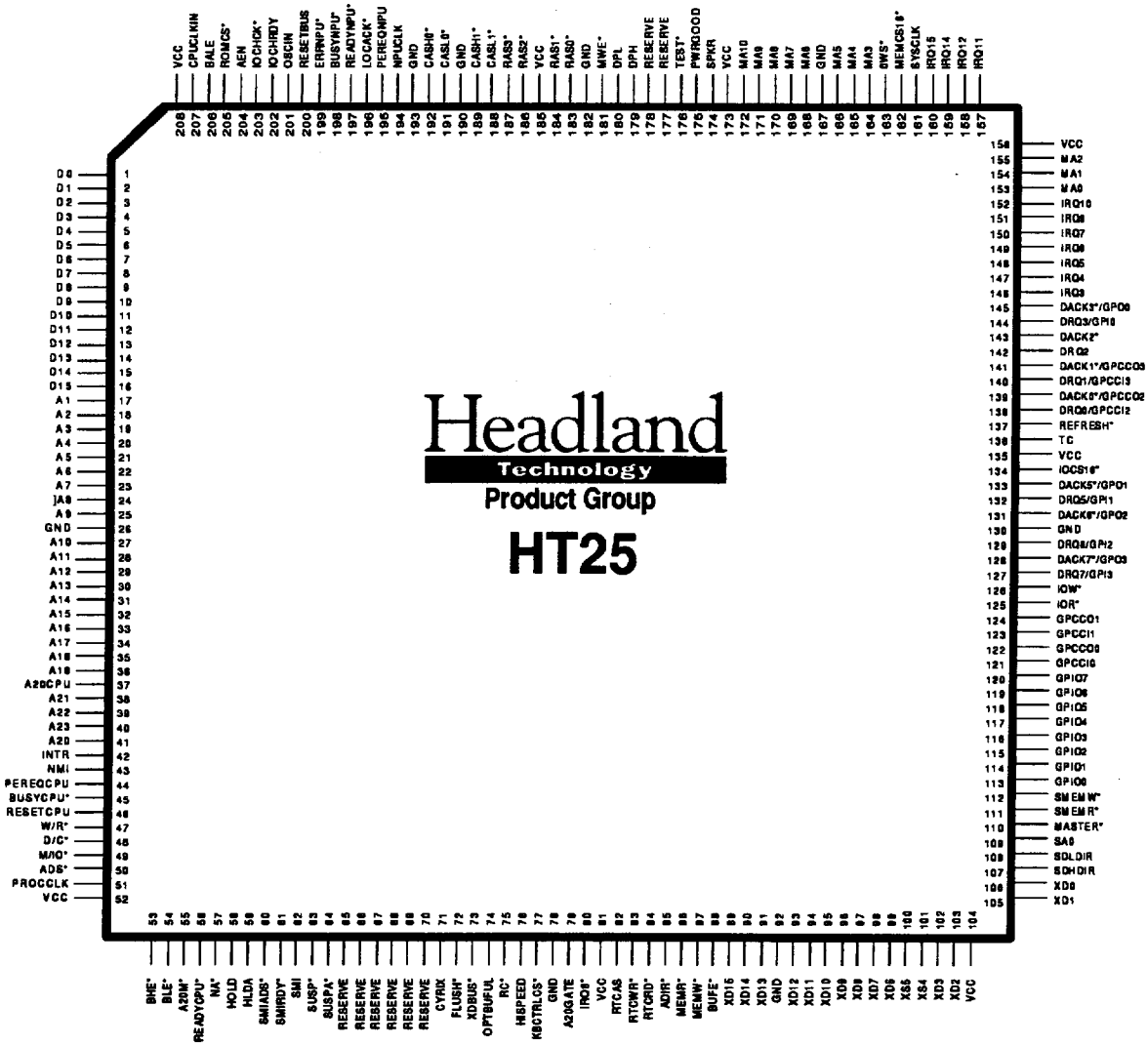
Port 92H Hot Reset and GATEA20 — Port 92h

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	RES	GATE A20	HOT RESET

Bits	Access	Default	Description
[7:2]			Reserved
1	R/W	O	Gate A20 0 = A20 forced low if A20GATE is low. 1 = A20 will follow A20CPU
0	R/W	O	Hot Reset (The reset occurs after a minimum of 6.72us when the Hot Reset bit is set to 1, it remains set until cleared by the BIOS.) 0 = Clear reset 1 = Reset - RESETCPU Pin will go high for 16 Clocks.

HT25
3V Single Chip 386SX Controller

Pin Diagram



Pins Alphabetically

17	+	A1	13	+	D12	147	+	IRQ4	70		RESERVE
18	+	A2	14	+	D13	148	+	IRQ5	177		RESERVE
19	+	A3	15	+	D14	149	+	IRQ6	178		RESERVE
20	+	A4	16	+	D15	150	+	IRQ7	200		RESETBUS
21	+	A5	48	+	D/C*	80	+	IRQ8*	46		RESETCPU
22	+	A6	139		DACK0*	151	+	IRQ9	205		ROMCS*
23	+	A7	141		DACK1*	152	+	IRQ10	82		RTCAS
24	+	A8	143		DACK2*	157	+	IRQ11	84		RTCRD*
25	+	A9	145		DACK3*	158	+	IRQ12	83		RTCWR*
27	+	A10	133		DACK5*	159	+	IRQ14	109	+	SA0
28	+	A11	131		DACK6*	160	+	IRQ15	107		SDHDIR
29	+	A12	128		DACK7*	77		KBCTRLCS*	108		SDLDIR
30	+	A13	179	+	DPH	196	+	LOCACK*	111		SMEMR*
31	+	A14	180	+	DPL	49	+	M/IO*	112		SMEMW*
32	+	A15	138	x	DRQ0	153		MA0	62	+	SMI
33	+	A16	140	x	DRQ1	154		MA1	60	+	SMIADS*
34	+	A17	142	x	DRQ2	155		MA2	61		SMIRDY*
35	+	A18	144	x	DRQ3	164		MA3	174		SPKR
36	+	A19	132	x	DRQ5	165		MA4	63		SUSP*
41	+	A20	129	x	DRQ6	166		MA5	64	+	SUSPA*
38	+	A21	127	x	DRQ7	168		MA6	161		SYSCLK
39	+	A22	199	+	ERRNPU*	169		MA7	136		TC
40	+	A23	72		FLUSH*	170		MA8	176		TEST*
55		A20M*	26		GND	171		MA9	52		VCC
37	+	A20CPU	78		GND	172		MA10	81		VCC
79	+	A20GATE	92		GND	110	+	MASTER*	104		VCC
85		ADIR*	130		GND	162	+	MEMCS16*	135		VCC
50	+	ADS*	167		GND	86	+	MEMR*	156		VCC
104		AEN	182		GND	87	+	MEMW*	173		VCC
206		BALE	190		GND	181		MWE*	185		VCC
53	+	BHE*	193		GND	57		NA*	208		VCC
54	+	BLE*	121	+	GPCCI0	43		NMI	47	+	W/R*
88		BUFE*	123	+	GPCCI1	194		NPUCLK	106	+	XD0
45		BUSYCPU*	122	+	GPCCO0	74	x	OPTBUFUL	105	+	XD1
198	+	BUSYNPU*	124	+	GPCCO1	201		OSCIN	103	+	XD2
192		CASH0*	113	+	GPIO0	44		PEREQCPU	102	+	XD3
189		CASH1*	114	+	GPIO1	195	x	PEREQNPU	101	+	XD4
191		CASL0*	115	+	GPIO2	51		PROCCLK	100	+	XD5
188		CASL1*	116	+	GPIO3	175		PWRGOOD	99	+	XD6
207	+	CPUCLKIN	117	+	GPIO4	183		RAS0*	98	+	XD7
71	+	CYRIX	118	+	GPIO5	184		RAS1*	97	+	XD8
1	+	D0	119	+	GPIO6	186		RAS2*	96	+	XD9
2	+	D1	120	+	GPIO7	187		RAS3*	95	+	XD10
3	+	D2	76	+	HISPEED	75	+	RC*	94	+	XD11
4	+	D3	59	x	HLDA	56	+	READYCPU*	93	+	XD12
5	+	D4	58		HOLD	197	+	READYNPU*	91	+	XD13
6	+	D5	42		INTR	137	+	REFRESH*	90	+	XD14
7	+	D6	203	+	IOCHCK*	65		RESERVE	89	+	XD15
8	+	D7	202	+	IOCHRDY	66		RESERVE	73	+	XDBUS*
9	+	D8	134	+	IOCS16*	67		RESERVE	163	+	0WS*
10	+	D9	125	+	IOR*	68		RESERVE			
11	+	D10	126	+	IOW*	69		RESERVE			
12	+	D11	146	+	IRQ3						

\+ These pins have internal pullup Resistors
x These pins have internal pulldown Resistors

HT25
3V Single Chip 386SX Controller

Pins Numerically

1	D0	53	BHE*	105	XD1	157	IRQ11
2	D1	54	BLE*	106	XD0	158	IRQ12
3	D2	55	A20M*	107	SDHDIR	159	IRQ14
4	D3	56	READYCPU*	108	SDLDIR	160	IRQ15
5	D4	57	NA*	109	SA0	161	SYSCLK
6	D5	58	HOLD	110	MASTER*	162	MEMCS16*
7	D6	59	HLDA	111	SMEMR*	163	0WS*
8	D7	60	SMIADS*	112	SMEMW*	164	MA3
9	D8	61	SMIRDY*	113	GPIO0	165	MA4
10	D9	62	SMI	114	GPIO1	166	MA5
11	D10	63	SUSP*	115	GPIO2	167	GND
12	D11	64	SUSPA*	116	GPIO3	168	MA6
13	D12	65	RESERVE	117	GPIO4	169	MA7
14	D13	66	RESERVE	118	GPIO5	170	MA8
15	D14	67	RESERVE	119	GPIO6	171	MA9
16	D15	68	RESERVE	120	GPIO7	172	MA10
17	A1	69	RESERVE	121	GPCCI0	173	VCC
18	A2	70	RESERVE	122	GPCCO0	174	SPKR
19	A3	71	CYRIX	123	GPCCI1	175	PWRGOOD
20	A4	72	FLUSH*	124	GPCCO1	176	TEST*
21	A5	73	XDBUS*	125	IOR*	177	RESERVE
22	A6	74	OPTBUFUL	126	IOW*	178	RESERVE
23	A7	75	RC*	127	DRQ7	179	DPH
24	A8	76	HISPEED	128	DACK7*	180	DPL
25	A9	77	KBCTRLCS*	129	DRQ6	181	MWE*
26	GND	78	GND	130	GND	182	GND
27	A10	79	A20GATE	131	DACK6*	183	RAS0*
28	A11	80	IRQ8*	132	DRQ5	184	RAS1*
29	A12	81	VCC	133	DACK5*	185	VCC
30	A13	82	RTCAS	134	IOCS16*	186	RAS2*
31	A14	83	RTCWR*	135	VCC	187	RAS3*
32	A15	84	RTCRD*	136	TC	188	CASL1*
33	A16	85	ADIR*	137	REFRESH*	189	CASH1*
34	A17	86	MEMR*	138	DRQ0	190	GND
35	A18	87	MEMW*	139	DACK0*	191	CASL0*
36	A19	88	BUFE*	140	DRQ1	192	CASH0*
37	A20CPU	89	XD15	141	DACK1*	193	GND
38	A21	90	XD14	142	DRQ2	194	NPUCLK
39	A22	91	XD13	143	DACK2*	195	PEREQNPU
40	A23	92	GND	144	DRQ3	196	LOCACK*
41	A20	93	XD12	145	DACK3*	197	READYNPU*
42	INTR	94	XD11	146	IRQ3	198	BUSYNPU*
43	NMI	95	XD10	147	IRQ4	199	ERRNPU*
44	PEREQCPU	96	XD9	148	IRQ5	200	RESETBUS
45	BUSYCPU*	97	XD8	149	IRQ6	201	OSCIN
46	RESETCPU	98	XD7	150	IRQ7	202	IOCHRDY
47	W/R*	99	XD6	151	IRQ9	203	IOCHCK*
48	D/C*	100	XD5	152	IRQ10	204	AEN
49	M/IO*	101	XD4	153	MA0	205	ROMCS*
50	ADS*	102	XD3	154	MA1	206	BALE
51	PROCCLK	103	XD2	155	MA2	207	CPUCLKIN
52	VCC	104	VCC	156	VCC	208	VCC

Pin Descriptions

Pin Symbol	Pin Number	Pin Type	Description
A[1:19] A[21:23]	17-25, 27-36, 38-40	I/O	During CPU cycles and Master Mode cycles, A[1:19] and A[21:23] are inputs. During non-master mode HLDA cycles, A[1:19] and A[21:23] are outputs.
A20	41	I/O	During CPU cycles and non-ISA Master Mode cycles A20 is an output. During ISA Master Mode cycles A20 is an input.
A20CPU	37	I	Address bit 20 from the CPU. This signal is gated with A20GATE (pin 79) and Alternate A20Gate (I/O Port 92, bit 1) to produce A20 (pin 41).
A20GATE	79	I	A20 gating control input.When low, A20 is low.
A20M*	55		A20 Masking for Cyrix CPU. Low when A20GATE is low and Port 92 Bit 1 is low.
ADIR*	85	O	SA & LA Address buffers direction control.High during ISA Master Mode. Low otherwise.
ADS*	50	I	Address status input from the CPU.
AEN	204	O	Address Enable. High during a DMA cycle.
BALE	206	O	Bus Address Latch Enable. Latch Enable (LE) for latching the address bus with external latches. High during MASTER, Refresh and DMA cycles.
BHE*	53	I/O	Byte High Enable. Indicates data transfer on the ISA bus high byte (bits 8-15). Input during Master Mode, output otherwise.
BLE*	54	I/O	Byte Low Enable. Indicates data transfer on the ISA bus low byte (bits 0-7). Input during Master Mode, output otherwise.
BUFE*	88	O	Buffer/Level Shifter Enable. Asserted (low) during ISA bus cycles. May be programmed to be always asserted.
BUSYCPU*	45	O	BUSYCPU* output connects to the BUSY* input of the CPU.

Pin Symbol	Pin Number	Pin Type	Description
BUSYNPU*	198	I	BUSYNPU* is connected to the BUSY* output of the NPU.
CASH0* CASH1*	192,189	O	Column Address Strobe High order byte.
CASL0* CASL1*	191,188	O	Column Address Strobe Low order byte.
CPUCLKIN	207	I	CPU Clock Input. This clock is also used to generate the bus clock.
CYRIX	71	I	For Cyrix CPU support if high.
D[0:15]	1-16	I/O	Local CPU Data Bus.
D/C*	48	I	Data/Control signal from the CPU.
DACK2*, DACK0*/GPCCO2 DACK1*/GPCCO3 DACK3*/GPO0 DACK5*/GPO1 DACK6*/GPO2 DACK7*/GPO3	143, 139, 141, 145, 133, 131, 128	O	DMA Acknowledges. This signals are the respective Bus Grant Signals to DRQ requests. May function as Clock Channels and inputs under control of Registers BCh through C3h.
DPL, DPH	179,180	I/O	Data Parity Low and Data Parity High for System DRAM.
DRQ2 DRQ0/GPCCI2 DRQ1/GPCCI3 DRQ3/GPI0 DRQ5/GPI1 DRQ6/GPI2 DRQ7/GPI3	142, 138, 140, 144, 132, 129 127	I	DMA Channel Requests/General Purpose Clock Channel Input/General Purpose Input.
ERRNPU*	199	I	Error signal from the NPU.
FLUSH*	72	O	Cyrix processor cache flush.Configuration Register Index 11h, Bit 4.
GND	26,78,92, 130,167,182,190 193		Ground

Pin Descriptions

Pin Symbol	Pin Number	Pin Type	Description
GPCCI0 GPCCI1	121, 123	I	General Purpose Clock Channel Inputs
GPCCO0 GPCCO1	122, 124	O	General Purpose Clock Channel Outputs
GPIO[0:7]	113-120	I/O	General Purpose I/O
HISPEED	76	I	HISPEED controls PROCCLK switching on high to low speed operations, as programmed by Control Register Index 98h.
HLDA	59	I	Hold Acknowledge from the CPU. The CPU drives this input high to indicate that it has released control of the buses.
HOLD	58	O	Hold request to the CPU.
INTR	42	O	Interrupt Request signal to the CPU.
IOCHCK*	203	I	I/O Channel check, active low, causes NMI when enabled.
IOCHRDY	202	I	I/O Channel Ready, active high.
IOCS16*	134	I	I/O Chip Select 16 bits. Asserted by the respondant Backplane Device, it indicates acceptance of a 16 bit transfer for the current I/O Cycle.
IOR*,	125	I/O	I/O Read, active low. This signal indicates an I/O read operation is in progress on the ISA Bus. For CPU and DMA cycles, this signal is an output; for Master Mode cycles it is an input.
IOW*	126	I/O	I/O Write, active low. This signal indicates an I/O write operation is in progress on the ISA Bus. For CPU and DMA cycles, this signal is an output; for Master Mode cycles it is an input.

Pin Symbol	Pin Number	Pin Type	Description
IRQ3-IRQ7, IRQ9-IRQ12, IRQ14-IRQ15	146-150, 151,152, 157,158 159,160	I	Interrupt Requests. Interrupts from the I/O Channel indicate that a peripheral on the Backplane is requesting service by the CPU. An interrupt request is generated on the rising edge of an IRQ which must be maintained high until acknowledged by the INTR cycle.
IRQ8*	80	I	Interrupt Request 8. Real Time Clock interrupt. Needs 10K Ohm external pullup for 146818 type devices.
KBCTRLCS*	77	O	Keyboard Controller Chip Select. Asserted during I/O operations to addresses 060h and 064h.
LOCACK*	196	I	Local bus device cycle acknowledge
M/IO*	49	I	Memory I/O signals from the CPU bus.
MA[0:10]	153-155, 164-166, 168-172	O	DRAM Address bus.
MASTER*	110	I	The ISA Backplane Master cycle indicator, active low. When active at the DRQ/DACK exchange, it indicates that a Backplane Master device owns the local bus using the HT25 as a Synchronizer/Interface chip between the ISA and Local Bus.
MEMCS16*	162	I	Memory Chip Select is 16 bits. Asserted by the respondant Backplane Device, it indicates acceptance of a 16 bit transfer for the current cycle.
MEMR*	86	I/O	Memory Read. Asserted during memory reads from the ISA bus. Normally an output, during a Master Mode cycle this signal will be an input. This signal will be active for all Backplane accesses below 16MB.
MEMW*	87	I/O	Memory Write, active low. When active, this signal indicates that a Memory Write Cycle is in progress on the Backplane. This signal will be active for all Backplane accesses below 16MB. Normally an Output, during a Master Mode Cycle this signal will be an Input.

Pin Descriptions

Pin Symbol	Pin Number	Pin Type	Description
MWE*	181	O	DRAM Write Enable.
NA*	57	O	Next Address signal to the CPU.
NMI	43	O	Non-Maskable Interrupt to the CPU. Active for local RAM parity error or IOCHCK* low.
NPUCLK	194	O	NPU Clock to the co-processor.
OPTBUFUL	74	I	Keyboard Output Buffer Full interrupt. Connects to IRQ1 of Interrupt Controller 1.
OSCIN	201	I	14.318MHz input
PEREQCPU	44	O	NPU Request passed on to CPU. Also, output Pin for NAND Tree Test Mode.
PEREQNPU	195	I	Processor Extension Request from NPU.
PROCCLK	51	O	Clock Output to the CPU.
PWRGOOD	175	I	Power Good signal. Indicates that system power is stable.
RAS0* RAS1* RAS2* RAS3*	183, 184, 186, 187	O	Row Address Select signals.
RC*	75	I	Reset CPU signal . When driven low RESETCPU will go high.
READYCPU*	56	O	Ready signal to the CPU.
READYNPU*	197	I	Ready signal from the Co-processor.
REFRESH*	137	I/O	Refresh signal active low.
RESERVED	65-70		Unused. Leave Open.
RESETBUS	200	O	Reset output to the System.

Pin Symbol	Pin Number	Pin Type	Description
RESETCPU	46	O	Reset to the CPU.
ROMCS*	205	O	ROM Chip Select. This signal is MEMR* qualified by the ROM address range decode.
RTCAS	82	O	Real Time Clock Address Select signal. Asserted during I/O writes to address 070h.
RTCRD*	84	O	Real Time Clock Read command. Asserted during I/O reads from I/O address 071h.
RTCWR*	83	O	Real Time Clock Write command. Asserted during I/O writes to address 071h.
SA0	109	I/O	ISA Bus Address bit 0.
SDHDIR	107	O	SD Bus High byte buffer direction control. High for SD Bus write.
SDLDIR	108	O	SD Low byte buffer direction control. High for SD Bus write.
SMEMR*	111	O	SMEMR*. Asserted during memory reads from ISA bus address below 1Mb.
SMEMW*	112	O	SMEMW*. Asserted during memory writes to ISA bus addresses below 1Mb.
SMI	62	I/O	System Management Interrupt to the CPU.
SMIADS*	60	I	System Management Interrupt Address Status from the CPU.
SMIRDY*	61	O	Ready signal to the CPU during SMI Memory cycles. (For AMD CPU only)
SPKR	174	O	Speaker output signal.
SUSP*	63	O	Cyrix processor suspend request.
SUSPA*	64	I	Cyrix processor suspend acknowledge.
SYSCLK	161	O	System clock signal to the ISA Bus.

Pin Descriptions

Pin Symbol	Pin Number	Pin Type	Description
TC	136	O	DMA Terminal count.
TEST*	176	I	A low on this pin puts the chip in test mode
VCC	52, 81, 104, 135, 156, 173, 185, 208		Power Input Pins
W/R*	47	I	Write/Read signal from the CPU.
XD[0:15]	106, 105, 103-93, 91-89	I/O	16-bit XD data bus
XDBUS*	73	I	XD Bus Transfer. A Low on this signal indicates that the current bus tranfer is to/from a peripheral on the XD bus.
0WS*	163	I	Zero Wait State, active low. Asserted by the respondant Backplane Device. This signal indicates that the slave device requests early termination of the Backplane cycle or is capable of a Zero Wait State Cycle.

The following pins need external pullups when used in a standard ISA bus configuration. The suggested values are for standard ISA compatibility.

SIGNAL	RESISTOR VALUE
0WS*	300
IOCS16*	300
MASTER*	300
MEMCS16*	300
IOCHRDY	1K
IRQ (all)	10K
IOCHCK*	4.7K
REFRESH*	300
IOR*	10k (place on ISA side of any buffers)
IOW*	10k (place on ISA side of any buffers)
MEMR*	10k (place on ISA side of any buffers)
MEMW*	10k (place on ISA side of any buffers)
SMEMR*	10k (place on ISA side of any buffers)
SMEMW*	10k (place on ISA side of any buffers)

HT25
3V Single Chip 386SX Controller

DC Specifications

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	-0.3 to +5.5	V
Input Voltage	VIN	-0.3 to VDD +0.3	V
DC input Current	IIN	10	mA
Strorage Temperature Range(Plastic)	TSTG	-40 to +125	C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	2.7 to 3.6	V
Operating Ambient Temperature Range (Commercial)	TA	0 to +70	C

DC Characteristics: **VDD = 2.7 to 3.6V** **TA = 0C to 70C**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input Low	VIL		-0.3		VDD 0.3	V
Voltage Input High	VIH		0.7 VDD		VDD +0.3	V
Input Current, Cmos	IIN	VIN = VDD or VSS	- 10	± 1	10	
Input with pulldown Resister		VIN = VDD		99		uA
Inputs with pullup		VIN = VSS		-85		uA
Voltage OutPut High	VOH					V
PROCCLK		IOH = 6mA	VDD -0.4			
AEN,CAS*(0:3),RAS*(0:3), IOW/R,MA(0:10),MWE*,SA0, SMEMW*, SMEMR*,MEMR*,		IOH = 8mA	2.1			
REFRESH*		IOH = 8mA				
BALE,DACK(0:3,5:7),MDPH/L, SPKR, SYSCLK, TC, BUFE*, RESETBUS, READYCPU*, GPIO[7:0]		IOH = 6mA				
A[1:23],ADIR,BHE*,INTR,NA, ROMCS*, RTCRD*, PEREQCPU, RTCAS*, NPUCLK, ADIR*, RTCAS, RTCWR*, SDH/LDIR, XD[0:15], RESETCPU*, BUSYCPU*, SMIREADY*, HOLD, NMI, KBCTRLCS*, GPCC0, GPCC1, D[0:15]		IOL = 4mA				

DC Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage output Low	VOL					
PROCCLK		IOL = 6mA			0.4	V
AEN,CAS*(0:3),RAS*(0:3), IOW/R,MA(0:10),MWE*,SA0, SMEMW*, SMEMR*,MEMR*,		IOL = 8mA			0.5	
REFRESH*		IOL = 15mA				
BALE,DACK(0:3,5:7),MDPH/L, SPKR, SYSCLK, TC, BUFE*, RESETBUS, READYCPU*, GPIO[7:0]		IOL = 6mA				V
A[1:23],ADIR,BHE*,INTR,NA, ROMCS*, RTCRD*, PEREQCPU, RTCAS*, NPUCLK, ADIR*, RTCAS, RTCWR*, SDH/LDIR, XD[0:15], RESETCPU*, BUSYCPU*, SMIREADY*, HOLD, NMI, KBCTRLCS*, GPCC0, GPCC1, D[0:15]		IOL = 4mA				
3-State output leakage current	IOZ	VOH = VSS or VDD	-10	1	10	uA
Output short circuit current	IOS	VDD = Max, V0 = VDD VCC = Max, V0 = 0V		28.4 -21.8		mA mA
Supply Current	IDD	CLK = 25 MHz, CL = 50pf		76		mA
Hysteresis, Schmitt Trigger		CMOS VIL to VIH	1	1.5		V

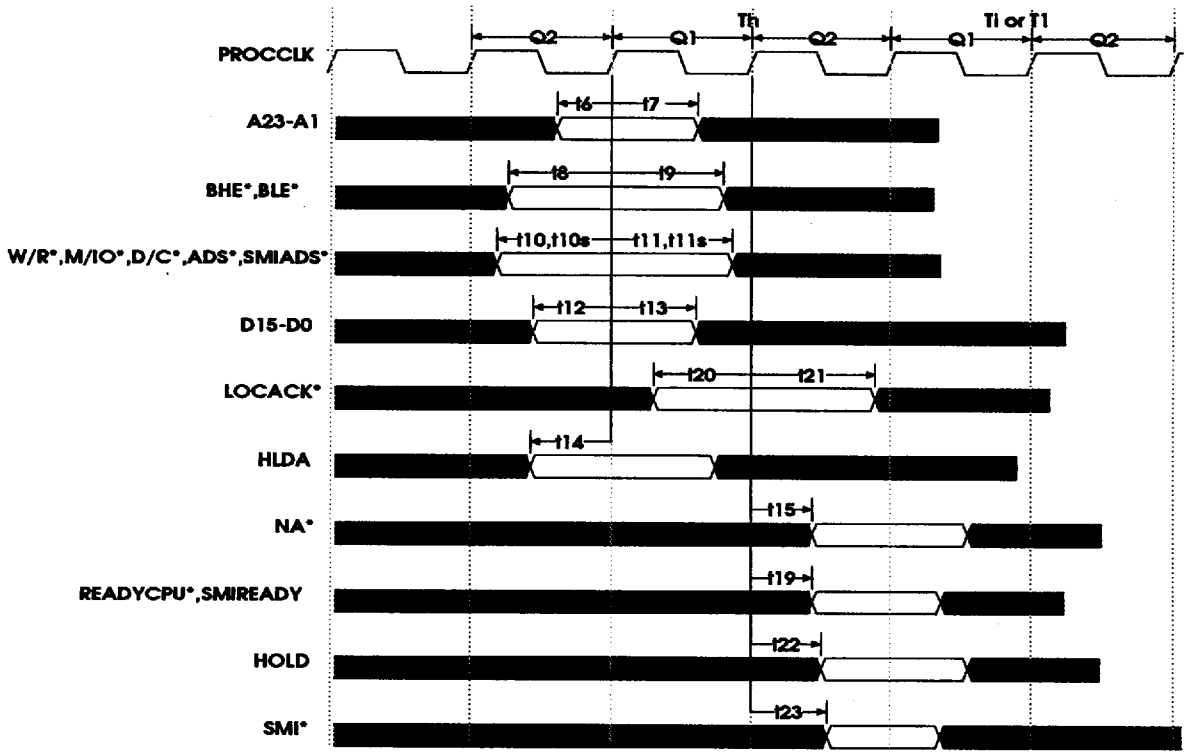
Pullup/Pulldown Resistor Values		Internal Resistor Type			Resistance Range	
HT25		PU/PD			Min	Max
					15K	143K

All timing parameters are specified under capacitive load of 50 pf, TA=0 to 70 degree C, VDD=3.3V +/- 10%, VSS=0. All AC specifications listed in this document are subject to change.

CPU Interface

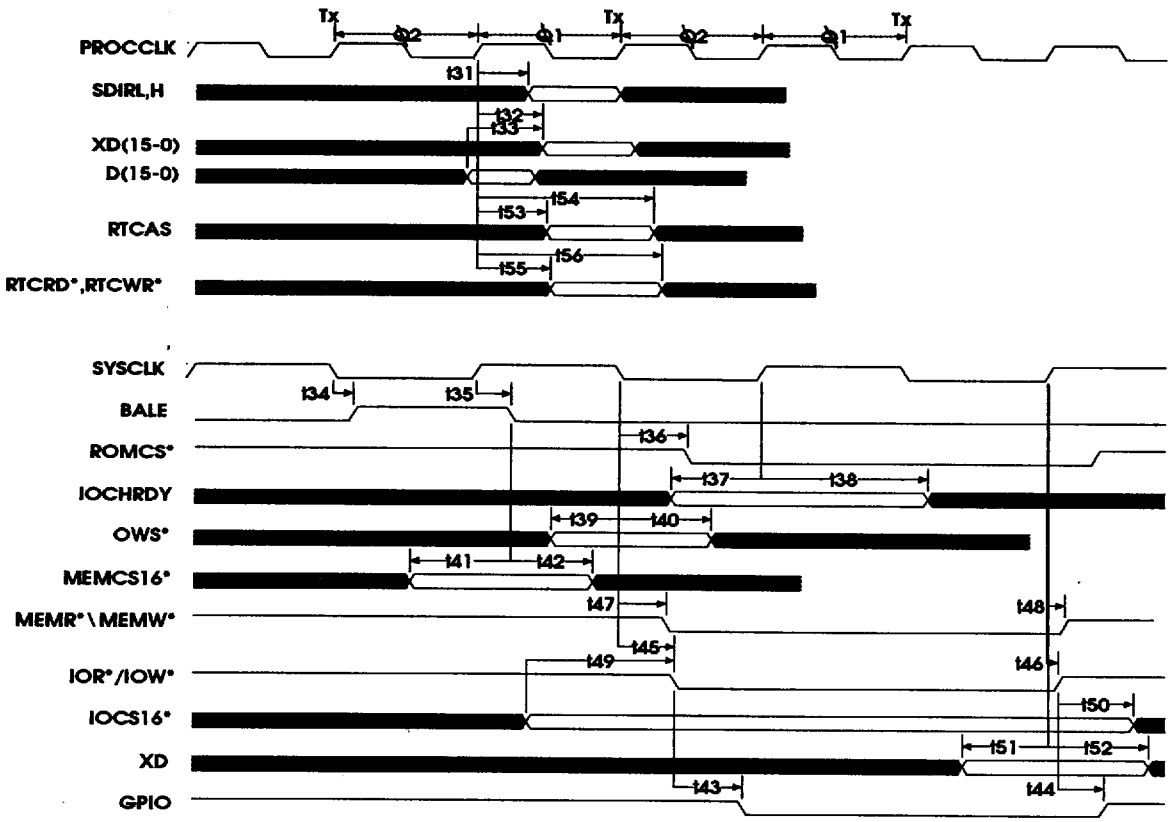
		Min	Max	Unit
	CPUCLKIN cycle time		25	MHz
	CPUCLKIN high time	7		ns
	CPUCLKIN low time	7		ns
	PROCCLK rise from CPUCLKIN rise		6.5	ns
	PROCCLK fall from CPUCLKIN fall		5.5	ns
	OSCIN Input frequency		14.318	MHz
t6	A(23:1) setup to PROCCLK	10		ns
t7	A(23:1) hold from PROCCLK	6		ns
t8	BHE*, BLE* setup to PROCCLK	10		ns
t9	BHE*, BLE* hold from PROCCLK	6		ns
t10	M/IO*, D/C*, W/R*, ADS* setup to PROCCLK	10		ns
t10s	SMIADS*, setup to PROCCLK	10		ns
t11	W/R*, M/IO*, D/C*, ADS* hold from PROCCLK	6		ns
t11s	SMIADS* hold from PROCCLK	6		ns
t12	D[15:0] setup to PROCCLK	10		ns
t13	D[15:0] hold from PROCCLK	6		ns
t14	HLDA setup to PROCCLK	10		ns
t15	NA* delay from PROCCLK		10	ns
t19	READYCPU*, SMIRDY* delay from PROCCLK		12	ns
t20	LOCACK* setup time to PROCCLK	10		ns
t21	LOCACK* hold time from PROCCLK	6		ns
t22	HOLD delay from PROCCLK		11	ns
t23	SMI* delay from PROCCLK		12	ns

AC Specifications



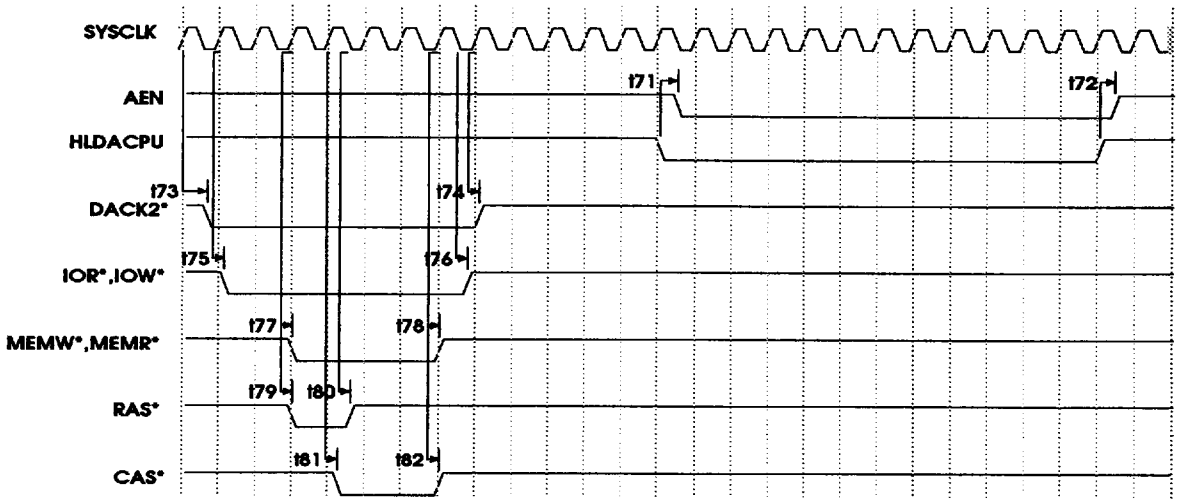
ISA Bus Timing

		Min	Max	Unit
t31	SDIRL,H delay from PROCCLK		20	ns
t32	XD(15-0) delay from PROCCLK		20	ns
t33	XD(15-0) delay from D(15-0)		15	ns
t34	BALE rise from SYSCLK		10	ns
t35	BALE fall from SYSCLK		10	ns
t36	ROMCS* active from SYSCLK		10	ns
t37	IOCHRDY setup time from SYSCLK	10		ns
t38	IOCHRDY hold from SYSCLK	10		ns
t39	0WS setup from SYSCLK	10		ns
t40	0WS hold from SYSCLK	7		ns
t41	MEMCS16* setup from BALE	10		ns
t42	MEMCS16* hold from BALE	7		ns
t43	GPIO active delay from IOR*\IOW*	12		ns
t44	GPIO inactive delay from IOR*\IOW*	7		ns
t45	IOR*/IOW* active delay from SYSCLK	10		ns
t46	IOR*/IOW* inactive delay from SYSCLK	12		ns
t47	MEMR*/MEMW* active delay from SYSCLK	7		ns
t48	MEMR*/MEMW* inactive delay from SYSCLK	10		ns
t49	IOCS16* setup to IOR*/IOW*	15		ns
t50	IOCS16* hold from IOR*/IOW*	7		ns
t51	XD bus setup to SYSCLK		20	ns
t52	XD bus float from SYSCLK		10	ns



DMA Timing

		Min	Max	Units
t71	AEN active delay from HLDA	12		ns
t72	AEN inactive delay from HLDA	15		ns
t73	DACK2* active delay from SYSCLK	6		ns
t74	DACK2* inactive delay from SYSCLK	6		ns
t75	IOR*, IOW* active delay from SYSCLK	15		ns
t76	IOR*, IOW* inactive delay from SYSCLK	9		ns
t77	MEMW*, MEMR* active delay from SYSCLK	15		ns
t78	MEMW*, MEMR* inactive delay from SYSCLK	20		ns
t79	RAS* active delay from SYSCLK	20		ns
t80	RAS* inactive delay from SYSCLK	5		ns
t81	CAS* active delay from SYSCLK	15		ns
t82	CAS* inactive delay from SYSCLK	20		ns

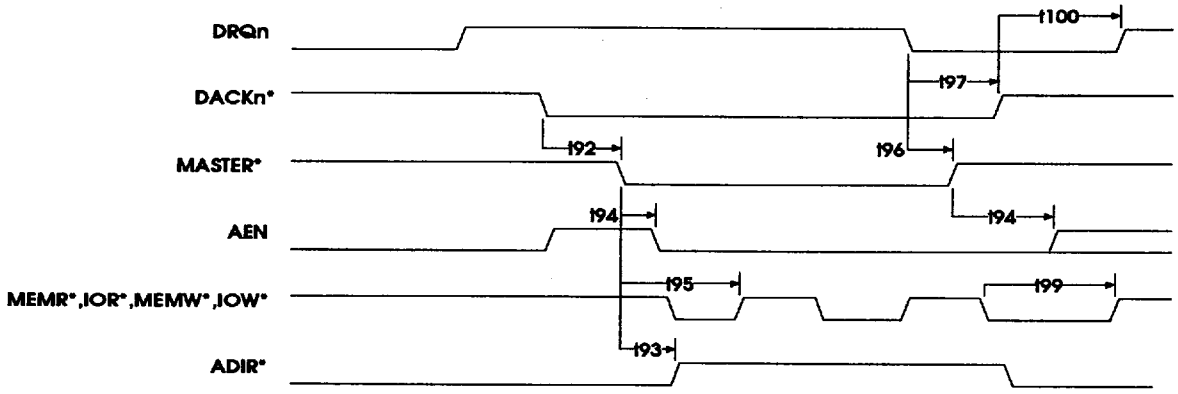


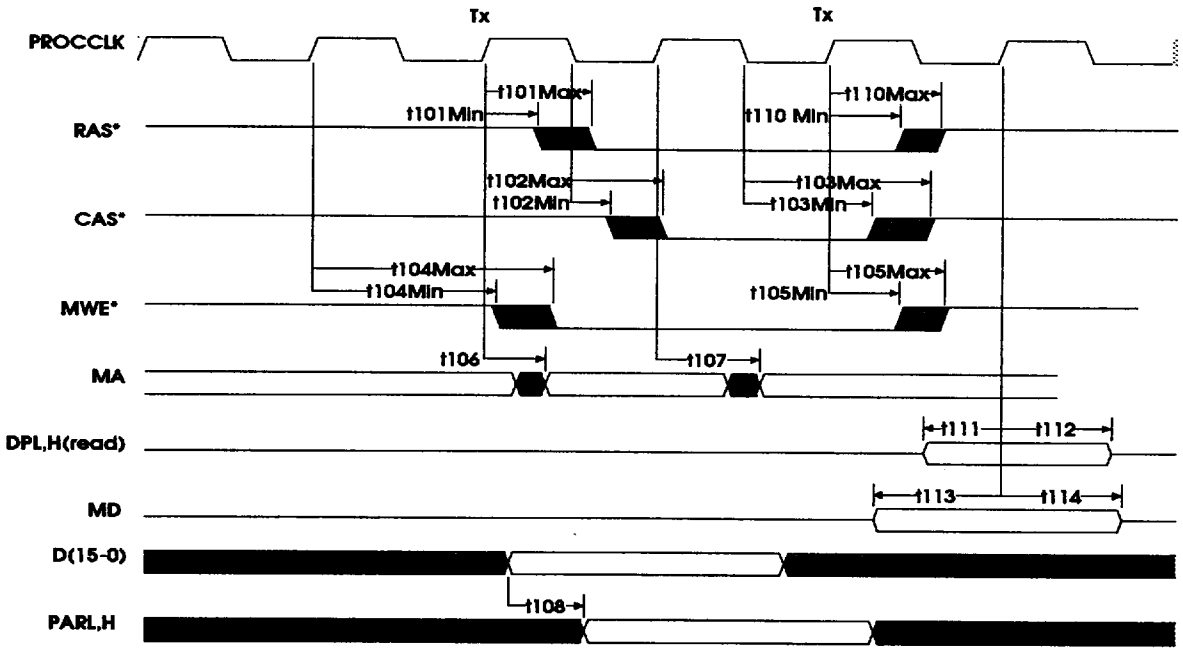
BUS Arbitration Timing:

		Min	Max	Units
t92	DACKn* to MASTER* delay	0		
t93	ADIR* delay from MASTER	10		ns
t94	AEN delay from MASTER*		49	ns
t95	Alternate MASTER drives address/data		125	ns
t96	MASTER* delay from DRQn inactive		100	ns
t97	DACKn* inactive from DRQn inactive	375		ns
t99	Permanent MASTER drives bus signals	49		ns
t100	DRQn inactive hold from DACKn*	0		

DRAM Interface

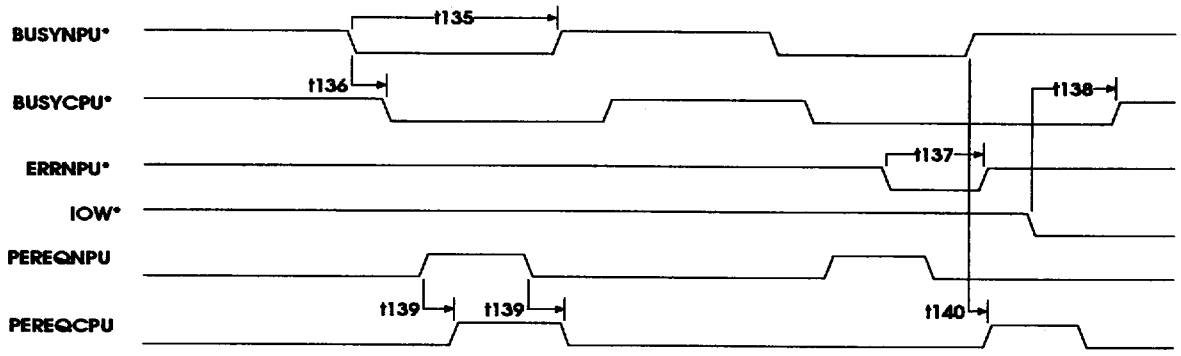
		Standard Mode		Extended mode		
		Min	Max	Min	Max	Units
t101	RAS active delay	4	12		13	ns
t102	CAS active delay	5	15		15	ns
t103	Cas inactive delay	6	17		17	ns
t104	Write enable active delay	11	32		33	ns
t105	Write enable inactive delay	13	38		39	ns
t106	MA row address delay	10	29		29	ns
t107	MA column address delay	11	32		32	ns
t108	DPL,H valid from D(0-15)		18		18	ns
t110	RAS inactive delay	5	14		14	ns
t111	Memory parity setup time	10				ns
t112	Memory parity hold time	6				ns
t113	MD read setup time	8				ns
t114	MD read hold time	19				ns

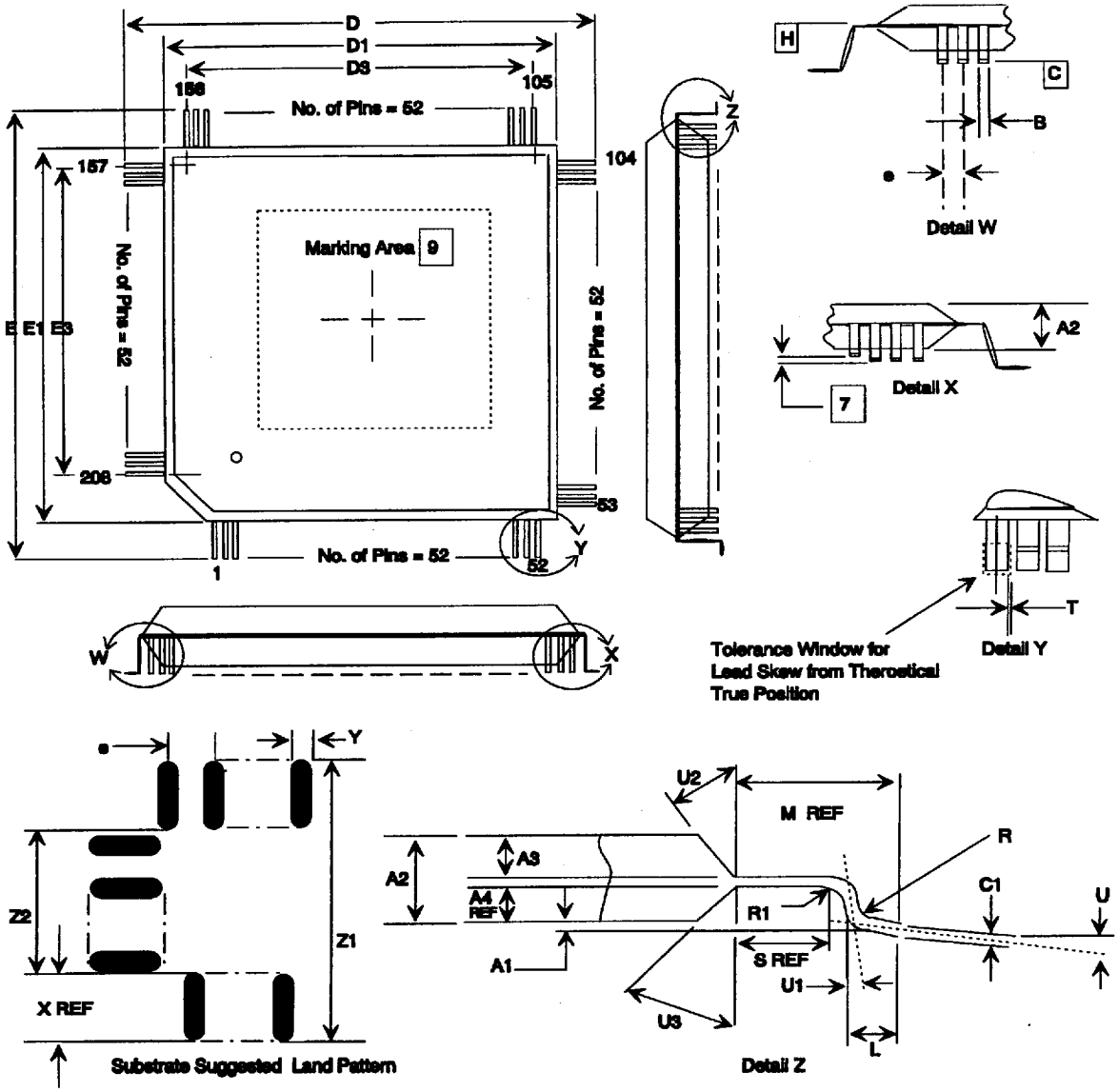




NPU Timings

		Min	Max	Units
t135	BUSYNPU* active pulse width	15		ns
t136	BUSYCPU* active delay from BUSYNPU*	10		ns
t137	ERRNPU* active pulse width	15		ns
t138	BUSYCPU inactive delay from IOW*	7		ns
t139	PEREQNPU to PEREQCPU	7		ns
t140	BUSYNPU* high to PEREQCPU high	7		ns





See Notes on next page.

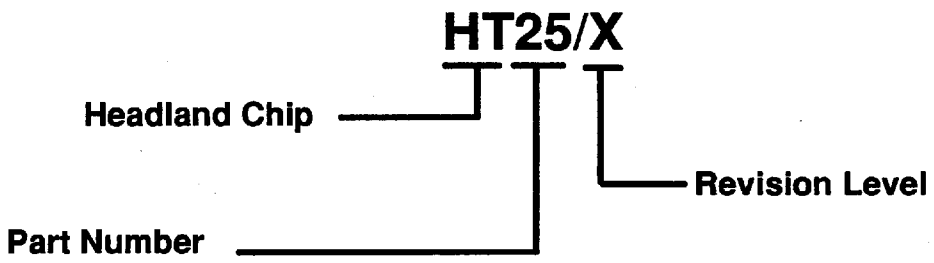
Package Outline

Dimensions in MM			
Symbol	Minimum	Maximum	Note
A1	0.25	0.36	
A2	3.40 +/- 0.10		
A3	1.60 +/- 0.05		
A4	1.60 Ref.		
B	0.23 +/- 0.05		6, 10
C1	015 +/- 0.03		10
D	30.60 +/- 0.20		2
D1	28.00 +/- 0.10		3
D3	25.5 Ref.		11
E	30.60 +/- 0.20		2
E1	28.00 +/- 0.10		3
E3	25.5 Ref.		11
e	0.5 Basc.		8
L	0.50 +/-		
M	1.30 Ref.		
R	0.19 +/- 0.06		
R1	0.13	-	
S	0.40	-	
T	-	0.1	12
U	2.5 +/- 2.5 Deg.		
U1	4 +/- 4 Deg.		
U2	10 +/- 2 Deg.		
U3	10 +/- 2 Deg.		
208 PQFP Recommended land Pattern			
X	2.0 Ref.		
Y	0.3 +/- 0.1		
Z1	32.0 +/- 0.1		
Z2	28.0 +/- 0>1		
# of Pins	208		

Notes: Unless otherwise specified

1. Datum plane - H - located at mold parting line is coincident with the bottom of lead, where the lead exits the plastic body.
2. To be determined at seating plane - C -.
3. Dimension D1 and E1 do not include mold protusion. Allowable protusion is .25mm per side.
4. These dimensions to be determined at datum plane - H -.
5. All dimensions in milimeters. Controlling dimension in milmeters.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm. Total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot minimum space between adjacent leads to be 0.07.
7. Coplanarity of all leads shall be within 0.076mm. Difference between highest and lowest lead with seating plane - C - as reference.
8. Lead pitch determined at datum - H -.
9. Marking area free of protrusion and intrusion.
10. Plating thickness included. Plating thickness to be 0.005mm Min. 0.020mm Max.
11. Dimension D3 and E3 to centered relative to Dimension D1 and E1 within +/- 0.15mm respectively.
12. From true lead location measured at seating plane - C -.

Product Order Information



IMPORTANT: Contact your local sales office for the current Order Code/Part Number