CONEXANT™

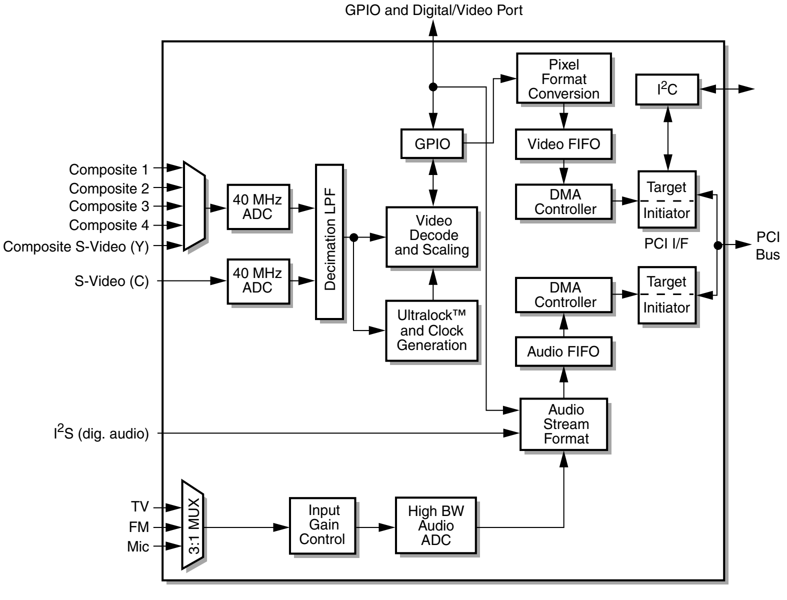
Fusion™ 878A

PCI Video Decoder

The Fusion 878A is a complete, low cost, single-chip solution for analog broadcast signal capture on the PCI bus. The Fusion 878A takes advantage of the PCI-based system's high bandwidth and inherent multimedia capability. It is designed to be interoperable with any other PCI multimedia device at the component or board level.

The Fusion 878A has all the video and audio capture features of the Bt878, plus a whole lot more. Designed to address the demanding requirements of the Personal Computing and digital video industry, Fusion 878A meets PC98/PC99 requirements as well as being fully PCI 2.2 compliant. Fusion 878A addresses the current analog PC TV requirements since it is pin for pin compatible and software compatible with the current Bt878. But, Fusion 878A can also be used in an array of MPEG digital transport stream products as well. The world is turning digital, with new standards in Television – ATSC and COFDM – and Television recording technologies using MPEG compression. Fusion 878A can be used as the hub into the PC connecting the multiple analog and digital video formats in the PC via a single PCI connection.

Functional Block Diagram



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Distinguishing Features

- NTSC/PAL/SECAM video decoding
- Supports capture resolutions up to 768 x 576 (full PAL)
- On-chip PCI bus mastering and bridge functionality
- Supports HDTV/audio/MPEG2 transport data across PCI bus
- High-speed serial port support MPEG transport stream up to rates of 40 Mbps
- High-speed parallel port supports MPEG transport streams up to 20 Mbps
- Flexible 24-bit wide GPIO
- CCIR656 interface
- Interfaces to a Digital TV data stream from a VSB or OFDM demodulator
- Multiple YCrCb and RGB pixel formats and YUV planar formats supported on output
- Selectable pixel density: 8, 16, 24, and 32 bits per pixel
- Performs complex clipping of video source and VGA video overlay
- Permits different program control and color space/scaling for even and odd fields
- Executes Windows 98 "Scatter and Gather"
- Integrates advanced chroma and luma comb filters/scalers
- Image scaleable in X and Y direction
- Y/C, 6-tap luma/2-tap chroma polyphase filter
- Receives Digital audio via I2S serial port
- Includes VBI data capture (closed captioning, teletext, and Intercast data decoding)
- 100% PCI Rev. 2.2 compliant
- PC 98/PC 99 compliant
- WHQL-certifiable
- Accepts Mono audio input
- Packaged in compact 128-pin plastic QFP

Fusion 878A Specific Features

- Full stereo decoding for both TV audio (BTSC) and FM radio
- Enhanced GPIO/I^{2}S
- ACPI support
- Byte alignment
- Vital product data
- High speed serial port
- High speed parallel port

Applications

- PC television
- Digital television
- Digital VCR
- Desktop video phone
- Still frame capture
- VBI data service capture

Ordering Information

Model Number	Package	Operating Temperature
Fusion 878A	128-pin PQFP	0 °C to + 70 °C

Related Documents

Fusion Technical Reference Manual
Fusion Programmers Guide

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1.0 Product Overview

1.1 Functional Overview

The Fusion 878A video and audio capture chip is a multi-function peripheral component interconnect (PCI) device intended for +5 V only operation. The video function features a direct memory access (DMA)/PCI bus master for analog NTSC/PAL/SECAM composite, S-Video, and digital CCIR 656 video capture. The audio function features a completely independent DMA/PCI bus master for FM radio or TV sound capture.

The Fusion 878A is based on the Bt848A video capture chip. The Fusion 878A is a Bt848A upgraded to include various audio capture capabilities. The main features of the Bt848A are: NTSC/PAL/SECAM video decoding, multiple YCrCb and RGB pixel formats supported on the output, vertical blanking interval (VBI) data capture for closed captioning, teletext, and intercast data decoding. The complete set of video and audio capture features are documented in this data sheet.

Table 1-1 indicates which audio capture features are added to the Bt848A to produce the Fusion 878A.

Table 1-1. Audio/Video Capture Product Family

All Features of the Bt848A, Plus:	CN878A
Mono line level and MIC level audio capture	x
Mono TV audio	x
ACPI Support	x

Figure 1-1 illustrates a block diagram of the Fusion 878A, and Figure 1-2 illustrates a detailed block diagram of the decoder and scaler sections of the Fusion 878A.

Figure 1-1. Fusion 878A Detailed Block Diagram

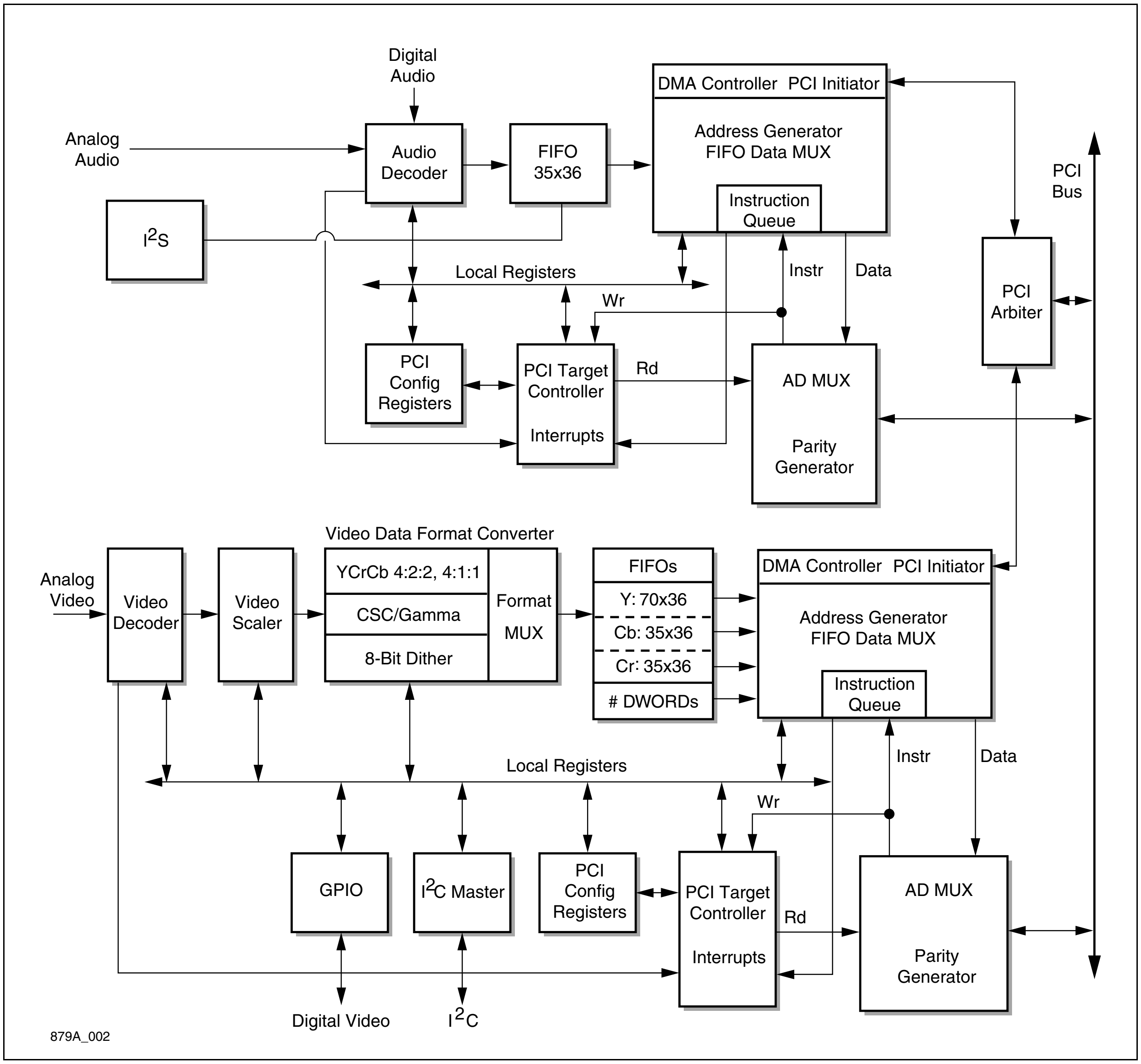
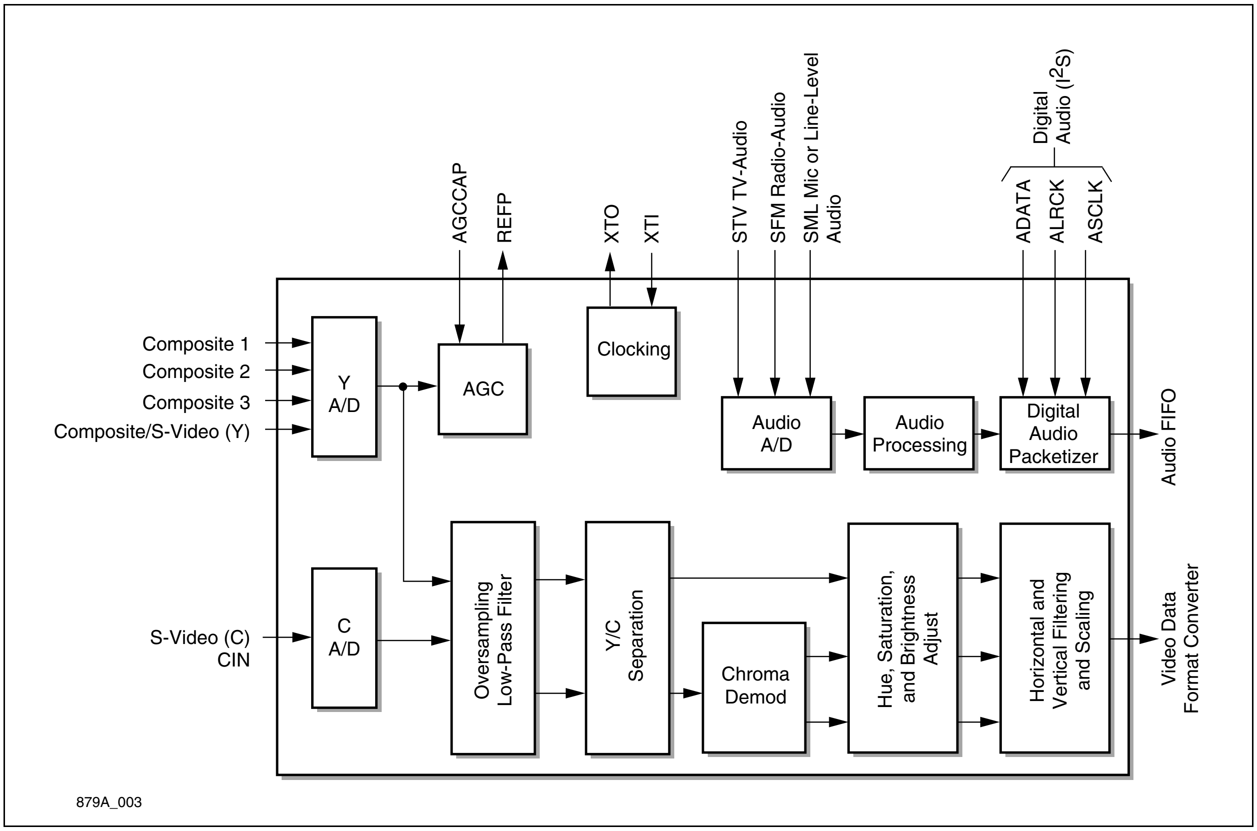


Figure 1-2. Fusion 878A Audio/Video Decoder and Scaler Block Diagram



1.2 Detailed Features

1.2.1 Video Capture

The Fusion 878A integrates an NTSC/PAL/SECAM composite and S-Video decoder, scaler, DMA controller, and PCI Bus master on a single device. The Fusion 878A can place video data directly into host memory for video capture applications and into a target video display frame buffer for video overlay applications. As a PCI initiator, the Fusion 878A can take control of the PCI bus as soon as it is available, thereby avoiding the need for on-board frame buffers. The Fusion 878A contains a pixel data FIFO to decouple the high speed PCI bus from the continuous video data stream.

The video data input may be scaled, color translated, and burst-transferred to a target location on a field basis. This allows for simultaneous preview of one field and capture of the other field. Alternatively, the Fusion 878A is able to capture both fields simultaneously or preview both fields simultaneously. The fields may be interlaced into memory or sent to separate field buffers.

1.2.2 Audio Capture

The Fusion 878A can also capture the broadcast audio spectrum over the PCI bus. This enables system solutions without the use of an analog audio cable. In addition, the audio capture can be used to implement microphone audio capture for complete videoconferencing applications.

1.2.3 Analog Video and Digital Camera Capture

The Fusion 878A includes a digital camera port to support digital video capture. This specification defines the registers and functionality required for implementing analog video capture support. Most of the analog and digital video register settings are identical.

In addition to the standard CCIR 656 digital interface, the Fusion 878A can accept digital video from digital cameras such as the Conexant Quartsight™, Silicon Vision™, and Logitech™. Internally the digital stream is routed to the high-quality down-scaler and color adjustment processing. It is then bus-mastered into system memory or displayed via the graphics frame buffer.

1.2.4 Intel Intercast™ Support

The Fusion 878A fully supports the Intel Intercast technology. Intel Intercast technology combines the programming of television and the Internet on the PC.

1.2.5 Video DMA Channels

The Fusion 878A enables separate destinations for the odd and even fields, each controlled by a pixel RISC instruction list. This instruction list is created by the Fusion 878A device driver and placed in the host memory. The instructions control the transfer of pixels to target memory locations on a byte resolution basis. Complex clipping can be accomplished by the instruction list, blocking the generation of PCI bus cycles for pixels that are not to be seen on the display.

The DMA channels can be programmed on a field basis to deliver the video data in packed or planar format. In packed mode, YCrCb data is stored in a single continuous block of memory. In planar mode, the YCrCb data is separated into three streams which are burst to different target memory blocks. Having the video data in planar format is useful for applications where the data compression is accomplished via software and the CPU.

1.2.6 Audio DMA Channels

The audio channel delivers 8-bit or 16-bit digital samples of a digital frequency-multiplexed analog signal to system memory in packets of DWORDs. A RISC program controls the audio DMA Program Initiator. The flow of audio data and audio RISC instructions is completely independent and asynchronous to the flow of video data and video RISC instructions.

Since the audio data path operates in continuous transfer mode (no sync gaps), both the analog and the digital audio inputs can be used for other data capture applications. The analog input offers 360 kHz usable BW at 8 effective bits or 100 kHz usable BW at 12 effective bits. The digital input offers up to 20 Mbps for the parallel mode and 40 Mbps for the serial mode.

The audio DMA channel controller is similar to the video DMA controller in that it supports packed mode RISC instructions. It also only interfaces to one 35 x 36 FIFO and its associated 6-bit DWORD counter.

The audio PCI initiator is identical to the video PCI initiator; they have the same DMA controller interface and the same support for interrupts and configuration space. Since the video and audio initiators are independent, each can handle retries without inhibiting the other. Thus, the audio function can initiate transfers to the host bridge even when a GFX target is retrying the video function.

The audio PCI target is similar to the video PCI target with respect to interrupts, configuration space, memory-mapped registers, and parity error checking. The main difference in audio is that all of the memory-mapped registers remain within the PCI clock and 32-bit interface domain. There is no register interface to the audio clock domain. Thus, this target never issues a disconnect or a retry.

1.2.7 Data Transport Engine

The Fusion 878A data transport engine operates in instruction mode. Video data and audio data are delivered over the PCI bus under independent control.

1.2.8 PCI Bus Interface

The Fusion 878A is designed to efficiently utilize the available 132 Mbps PCI bus. The 32-bit DWORDs are output on the PCI bus with the appropriate image data under the control of the DMA channels. The video stream consumes bus bandwidth with average data rates varying from 44 Mbps for full size 768 x 576 PAL RGB32, to 4.6 Mbps for NTSC CIF 320 x 240 RGB16, to 0.14 Mbps for NTSC ICON 80 x 60 8-bit mode.

The pixel instruction stream for the DMA channels consumes a minimum of 0.1 Mbps. The Fusion 878A provides the means for handling the bandwidth bottlenecks caused by slow targets and long bus access latencies that can occur in some system configurations. To overcome these system bottlenecks, the Fusion 878A gracefully degrades and recovers from FIFO overruns to the nearest pixel in real time.

1.2.9 UltraLock™

The Fusion 878A employs a proprietary technique known as UltraLock to lock to the incoming analog video signal. It always generates the required number of pixels per line from an analog source in which line length can vary by as much as a few microseconds. UltraLock's digital locking circuitry enables the VideoStream decoders to lock on to video signals quickly and accurately, regardless of their source. Since the technique is completely digital, UltraLock can recognize unstable signals caused by VCR head switches or any other deviation and adapt the locking mechanism to accommodate the source. UltraLock uses nonlinear techniques that are difficult, if not impossible, to implement in genlock systems. And unlike linear techniques, it adapts the locking mechanism automatically.

1.2.10 Scaling and Cropping

The Fusion 878A can reduce the video image size in both horizontal and vertical directions independently, using arbitrarily selected scaling ratios. The X and Y dimensions can be scaled down to one-sixteenth of the full resolution. Horizontal scaling is implemented with a 6-tap interpolation filter, while up to 5-tap interpolation is used for vertical scaling with a line store.

The video image can be arbitrarily cropped by reducing the number of active scan lines and active horizontal pixels per line.

The Fusion 878A supports a temporal decimation feature that reduces video bandwidth. This is accomplished by allowing frames or fields to be dropped from a video sequence at fixed but arbitrarily selected intervals.

1.2.11 Input Interface

Analog video signals are input to the Fusion 878A via a four-input multiplexer. The multiplexer can select between four composite source inputs or between three composite and a single S-Video input source. When an S-Video source is input to the Fusion 878A, the luma component is fed through the input analog multiplexer, and the chroma component feeds directly into the C input pin. An AGC circuit enables the Fusion 878A to compensate for non-standard amplitudes in the analog signal input.

The clock signal interface consists of a pair of pins that connect to a 28.63636 MHz (8 × NTSC Fsc) crystal. Either fundamental or third harmonic crystals may be used. Alternatively, CMOS oscillators may be used.

1.2.12 GPIO Port

The Fusion 878A provides a 24-bit GPIO bus. This interface can be used to input or output up to 24 general purpose I/O signals. Alternatively, the GPIO port can be used as a means to input video data. For example, the Fusion 878A can input the video data from an external digital camera and bypass the Fusion 878A's internal video decoder block.

1.2.13 Vertical Blanking Interval Data Capture

The Fusion 878A provides a complete solution for capturing and decoding VBI data. The Fusion 878A can operate in a VBI Line Output Mode, in which the VBI data is only captured during select lines. This mode of operation enables concurrent capture of VBI lines containing ancillary data and normal video image data.

In addition, the Fusion 878A supports a VBI Frame Output Mode in which every line in the video frame istreated as if it were a VBI line. This mode of operation is designed for use with still frame capture/processing applications.

1.2.14 I^{2}C Interface

The Fusion 878As I^{2}C interface supports both 99.2 kHz timing transactions and 396.8 kHz, repeated start, multi-byte sequential transactions. As an I^{2}C master, Fusion 878A can program other devices on the video card, such as a TV tuner as long as the device address is known. The Fusion 878A supports multi-byte sequential reads (more than one transaction) and multi-byte write transactions (greater than three transactions), which enable communication to devices that support auto-incremental internal addressing.

1.2.15 HDTV Support

Fusion 878A has the ability to accept either serial or parellel HDTV data and deliver that data to the host. Serial and parellel inputs both use the audio DMA channel to transfer the HDTV MPEG packets to the host.

Serial HDTV streams may be input to the high speed serial port, which shares pins with the digital audio (I^{2}S) port. Fusion 878A will accept serial HDTV streams at up to 40 Mbps.

Parellel HDTV data may be input to the GPIO port in asychronous parallel mode at up to 20 Mbps.

1.3 Pin Descriptions

Figure 1-3 displays the pinout diagram. Table 1-2 provides a description of pin functions grouped by common function.

Figure 1-3. Fusion 878A Pinout Diagram

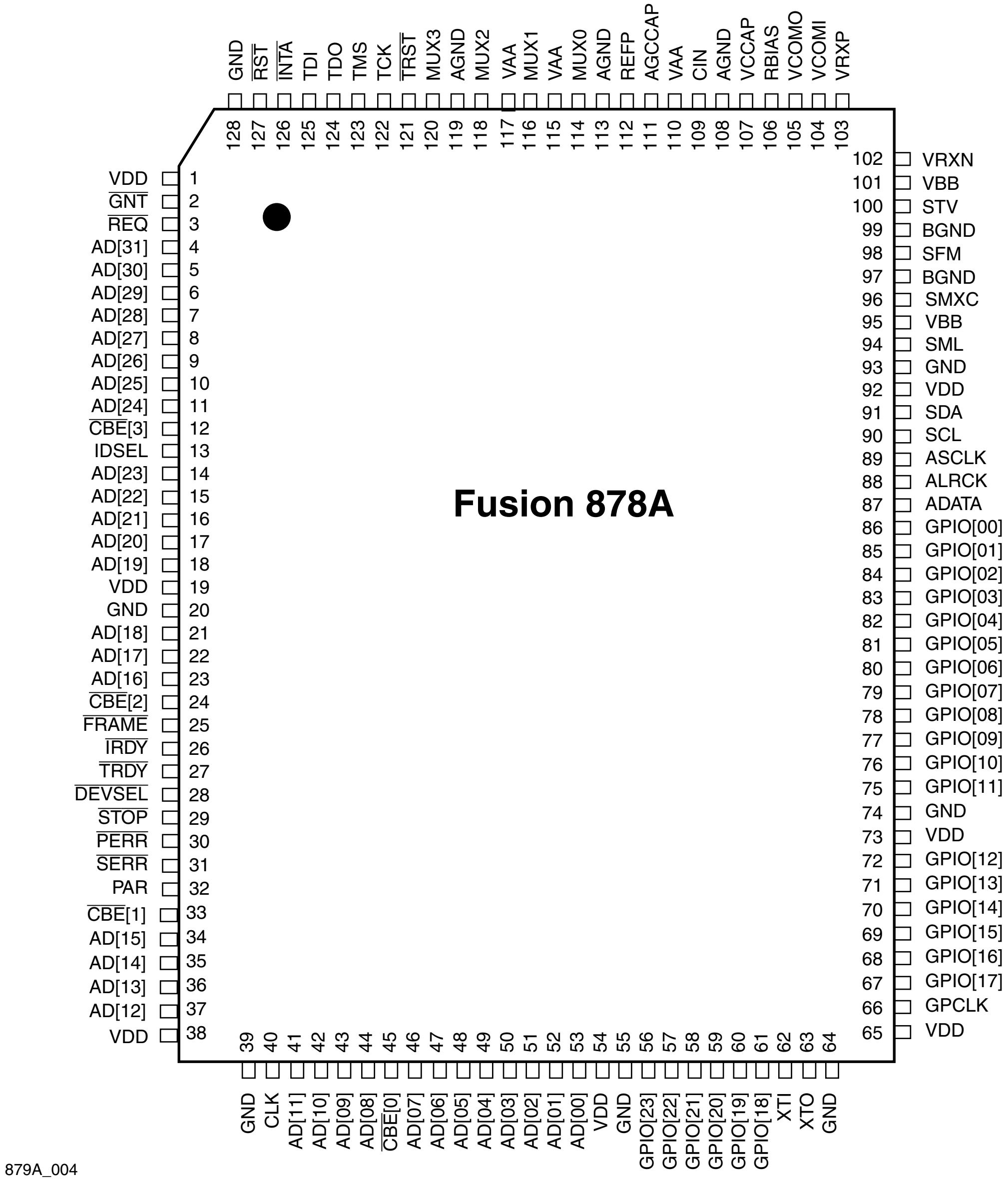


Table 1-2. Pin Descriptions Grouped by Pin Function *(1 of 4)*

Pin #	Pin Name	I/O	Signal	Description
PCI Interface (50 Pins) [1]				
40	CLK	I	Clock	This input provides timing for all PCI transactions. All PCI signals except $\overline{\text{RST}}$ and $\overline{\text{INTA}}$ are sampled on the rising edge of CLK, and all other timing parameters are defined with respect to this edge. The Fusion 878A supports a PCI clock of up to 33.3333 MHz.
127	$\overline{\text{RST}}$	I	Reset	This input three-states all PCI signals asynchronous to the CLK signal.
3	$\overline{\text{REQ}}$	O	Request	Agent desires bus.
2	$\overline{\text{GNT}}$	I	Grant	Agent granted bus.
13	IDSEL	I	Initialization Device Select	This input is used to select the Fusion 878A during configuration read and write transactions.
4–11, 14–18, 21–23, 34–37, 41–44, 46–53	AD[31:0]	I/O	Address/Data	These three-state, bidirectional I/O pins transfer both address and data information. A bus transaction consists of an address phase followed by one or more data phases for either read or write operations. The address phase is the clock cycle in which $\overline{\text{FRAME}}$ is first asserted. During the address phase, AD[31:0] contains a byte address for I/O operations and a DWORD address for configuration and memory operations. During data phases, AD[7:0] contains the least significant byte and AD[31:24] contains the most significant byte. Read data is stable and valid when $\overline{\text{TRDY}}$ is asserted and write data is stable and valid when $\overline{\text{IRDY}}$ is asserted. Data is transferred during the clocks when both $\overline{\text{TRDY}}$ and $\overline{\text{IRDY}}$ are asserted.
12, 24, 33, 45	$\overline{\text{CBE}}$[3:0]	I/O	Bus Command/Byte Enable	These three-state, bidirectional I/O pins transfer both bus command and byte enable information. During the address phase of a transaction, $\overline{\text{CBE}}$[3:0] signals contain the bus command. During the data phase, $\overline{\text{CBE}}$[3:0] are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data. $\overline{\text{CBE}}$[3] refers to the most significant byte and $\overline{\text{CBE}}$[0] refers to the least significant byte.
32	PAR	I/O	Parity	This three-state, bidirectional I/O pin provides even parity across AD[31:0] and $\overline{\text{CBE}}$[3:0]. This means that the number of 1s on PAR, AD[31:0], and $\overline{\text{CBE}}$[3:0] equals an even number. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either $\overline{\text{TRDY}}$ is asserted on a read, or $\overline{\text{IRDY}}$ is asserted on a write. Once valid, PAR remains valid until one clock after the completion of the current data phase. PAR and AD[31:0] have the same timing, but PAR is delayed by one clock. The target drives PAR for read data phases; the master drives PAR for address and write data phases.

Table 1-2. Pin Descriptions Grouped by Pin Function (2 of 4)

Pin #	Pin Name	I/O	Signal	Description
25	$\overline{\text{FRAME}}$	I/O	Cycle Frame	This sustained, three-state signal is driven by the current master to indicate the beginning and duration of an access. $\overline{\text{FRAME}}$ is asserted to signal the beginning of a bus transaction. Data transfer continues throughout assertion. At de-assertion, the transaction is in the final data phase.
26	$\overline{\text{IRDY}}$	I/O	Initiator Ready	This sustained, three-state signal indicates the bus master's readiness to complete the current data phase. $\overline{\text{IRDY}}$ is used in conjunction with $\overline{\text{TRDY}}$. When both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted, a data phase is completed on that clock. During a read, $\overline{\text{IRDY}}$ indicates when the initiator is ready to accept data. During a write, $\overline{\text{IRDY}}$ indicates when the initiator has placed valid data on AD[31:0]. Wait cycles are inserted until both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted together.
28	$\overline{\text{DEVSEL}}$	I/O	Device Select	This sustained, three-state signal indicates device selection. When actively driven, $\overline{\text{DEVSEL}}$ indicates the driving device has decoded its address as the target of the current access.
27	$\overline{\text{TRDY}}$	I/O	Target Ready	This sustained, three-state signal indicates the target's readiness to complete the current data phase. $\overline{\text{IRDY}}$ is used in conjunction with $\overline{\text{TRDY}}$. When both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted, a data phase is completed on that clock. During a read, $\overline{\text{TRDY}}$ indicates when the target is presenting data. During a write, $\overline{\text{TRDY}}$ indicates when the target is ready to accept the data. Wait cycles are inserted until both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted together.
29	$\overline{\text{STOP}}$	I/O	Stop	This sustained, three-state signal indicates the target is requesting the master to stop the current transaction.
30	$\overline{\text{PERR}}$	I/O	Parity Error	Report data parity error.
31	$\overline{\text{SERR}}$	O	System Error	Report address parity error. Open drain.
126	$\overline{\text{INTA}}$	O	Interrupt A	This signal is an open drain interrupt output.
JTAG (5 Pins)				
122	TCK	I	Test Clock	Used to synchronize all JTAG test structures. When JTAG operations are not being performed, this pin must be driven to a logical low.
123	TMS	I	Test Mode Select	JTAG input pin whose transitions drive the JTAG state machine through its sequences. When JTAG operations are not being performed, this pin must be left floating or tied high.
125	TDI	I	Test Data Input	JTAG pin used for loading instructions to the TAP controller or for loading test vector data for boundary-scan operation. When JTAG operations are not being performed, this pin must be left floating or tied high.
124	TDO	O	Test Data Output	JTAG pin used for verifying test results of all JTAG sampling operations. This output pin is active for certain JTAG operations and will be three-stated at all other times.
121	$\overline{\text{TRST}}$	I	Test Reset	JTAG pin used to initialize the JTAG controller. When JTAG operations are not being performed, this pin must be driven to a logical low.

Table 1-2. Pin Descriptions Grouped by Pin Function (3 of 4)

Pin #	Pin Name	I/O	Signal	Description
I^2C Interface (2 Pins)				
90	SCL	I/O	Serial Clock	Bus clock, output open drain.
91	SDA	I/O	Serial Data	Bit Data or Acknowledge, output open drain.
General Purpose I/O (25 Pins)				
66	GPCLK	I/O	GP Clock	Video clock. Internally pulled up to VDD.
56–61, 67–72, 75–86	GPIO[23:0]	I/O	General Purpose I/O	Fusion 878A pin decoding in normal mode. Pins pulled up to VDD. For additional information, see Tables 3-3 and 3-5.
Digital Audio Input/Audio Test Signals (3 Pins)				
87	ADATA	I/O	Audio Data	Bit serial data.
88	ALRCK	I/O	Audio Clock	Left/right framing clock.
89	ASCLK	I/O	Audio Serial Clock	Bit serial clock.
Reference Timing Interface Signals (2 Pins)				
62	XTI	I		A 28.63636 MHz crystal can be tied directly to these pins, or a single-ended oscillator can be connected to XTI.
63	XTO	O		
Video Input Signals (7 Pins)				
114, 116, 118, 120	MUX[0:3]	I		Analog composite video inputs to the on-chip 4:1 analog multiplexer. Unused inputs should be tied to AGND. The output of the MUX is direct-coupled to Y-A/D.
112	REFP	A		The top of the reference ladder for the video A/Ds. Connect to a 0.1 µF decoupling capacitor to AGND.
111	AGCCAP	A		The AGC time-constant control capacitor node. Must be connected to a 0.1µF capacitor to AGND.
109	CIN	I		Analog chroma input to the C-A/D.
TV/Radio Audio Input Signals (10 Pins)				
100	STV	I		TV sound input from TV tuner.
98	SFM	I		FM sound input from FM tuner.
94	SML	I		MIC/line input.
96	SMXC	A		Audio MUX anti-alias filter RC node. Connect through 68 pF capacitor to BGND.
106	RBIAS	A		Connection point for external bias 9.53 kΩ 1% resistor.
105	VCOMO	A		Common mode voltage for the audio analog circuitry. This pin should be connected to an external filtering 0.1 µF capacitor.
104	VCOMI	A		Common mode voltage for the audio analog circuitry. This pin should be connected to an external filtering 0.1 µF capacitor.
107	VCCAP	A		Audio analog voltage compensation capacitor. This pin should be connected to an external filtering 0.1 µF capacitor.

Table 1-2. Pin Descriptions Grouped by Pin Function (4 of 4)

Pin #	Pin Name	I/O	Signal	Description
103	VRXP	A		Audio input circuitry reference voltage. This pin should be connected to an external filtering 0.1 μF capacitor.
102	VRXN	A		Audio input circuitry reference voltage. This pin should be connected to an external filtering 0.1 μF capacitor.
I/O and Core Power and Ground (14 Pins)				
1, 19, 38, 54, 65 73, 92	VDD	P		Digital outputs power supply.
20, 39, 55, 64, 74, 93, 128	GND	G		Digital outputs ground.
Analog Video Power and Ground (6 Pins)				
108	AGND	A		C video A/D ground and CREFN. Connect to analog ground AGND.
110	VAA	A		Charge pump power supply and C video A/D power. Connect to analog power VAA and a 0.1μF decoupling capacitor to AGND.
113	AGND	A		Charge pump ground return.
115	VAA	A		Y video A/D power. Connect to analog power VAA and a 0.1μF decoupling capacitor to AGND.
117	VAA	A		Y video A/D power. Connect to analog power VAA and a 0.1μF decoupling capacitor to AGND.
119	AGND	A		Y video A/D ground. Connect to analog ground AGND.
Analog Audio Power and Ground (4 Pins)				
95, 101	VBB	P		Audio A/D power supply.
97, 99	BGND	G		Ground for audio A/D.

NOTE(S):

[1] See *PCI Specification 2.2* for further documentation.

2. I/O Column Legend:

I = Digital Input
O = Digital Output
I/O= Digital Bidirectional
A = Analog
G = Ground
P = Power

2.0 Functional Description

2.1 UltraLock^{TM} Functionality

2.1.1 The Challenge

The line length (the interval between the midpoints of the falling edges of succeeding horizontal sync pulses) of analog video sources is not constant. For a stable source such as studio quality source or test signal generators, this variation is very small: ±2 ns. However, for an unstable source such as a VCR, laser disk player, or TV tuner, line length variation is as much as a few microseconds.

Digital display systems require a fixed number of pixels per line despite these variations. The Fusion 878A employs a technique known as UltraLock to implement locking the horizontal sync and the subcarrier of the incoming analog video signal, generating the required number of pixels per line.

2.1.2 Operating Principles of UltraLock

UltraLock is based on sampling using a fixed-frequency, stable clock. Since the video line length will vary, the number of samples generated using a fixed-frequency sample clock will also vary from line to line. If the number of generated samples per line is always greater than the number of samples per line required by the particular video format, the number of acquired samples can be reduced to fit the required number of pixels per line.

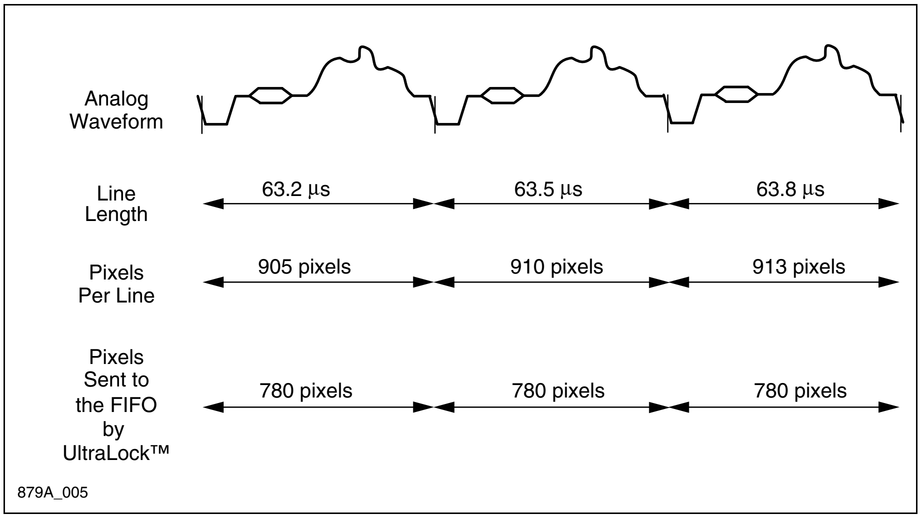
The Fusion 878A requires an 8 × Fsc (28.63636 MHz for NTSC and 35.46895 MHz for PAL) reference time source. The 8 × Fsc clock signal, or CLK x 2, is divided down to CLK x 1 internally (14.31818 MHz for NTSC and 17.73 MHz for PAL). CLK x 2 and CLK x 1 are internal signals and are not made available to the system. UltraLock operates at CLK x 1 although the input waveform is sampled at CLK x 2 then low-pass filtered and decimated to CLK x 1 sample rate.

At a 4 × Fsc (CLK x 1) sample rate there are 910 pixels for NTSC and 1,135 pixels for PAL/SECAM within a nominal line time interval (63.5 µs for NTSC and 64 µs for PAL/SECAM). For square pixel NTSC and PAL/SECAM formats, there should only be 780 and 944 pixels per video line, respectively. This is because the square pixel clock rates are slower than a 4 × Fsc clock rate; for example, 12.27 MHz for NTSC and 14.75 MHz for PAL.

UltraLock accommodates line length variations from nominal in the incoming video by always acquiring more samples, at an effective 4 × Fsc rate, than are required by the particular video format and outputting the correct number of pixels per line. UltraLock then interpolates the required number of pixels in a way that maintains the stability of the original image despite variation in the line length of the incoming analog waveform.

Figure 2-1 illustrates an example of three successive lines of video being decoded for square pixel NTSC output. The first line is shorter than the nominal NTSC line time interval of 63.5 µs. On this line, a line time of 63.2 µs sampled at 4 × Fsc (14.31831 MHz) generates only 905 pixels. The second line matches the nominal line time of 63.5 µs and provides the expected 910 pixels. Finally, the third line is too long at 63.8 µs within which 913 pixels are generated. In all three cases, UltraLock outputs only 780 pixels.

Figure 2-1. UltraLock Behavior for NTSC Square Pixel Output



UltraLock can be used to extract any programmable number of pixels from the original video stream as long as the sum of the nominal pixel line length (910 for NTSC and 1,135 for PAL/SECAM) and the worst case line length validation from nominal in the active region is greater than or equal to the required number of output pixels per line; i.e.,

$$P_{Nom} + P_{Var} \geq P_{Desired}$$

where: P_{Nom} = Nominal number of pixels per line at 4 × Fsc sample rate (910 for NTSC, 1,135 for PAL/SECAM)

P_{Var} = Variation of pixel count from nominal at 4 × Fsc (can be a positive or negative number)

$P_{Desired}$ = Desired number of output pixels per line

NOTE: With stable inputs, UltraLock guarantees the time between the falling edges of HRESET to within only one pixel. UltraLock does, however, guarantee the number of active pixels in a line as long as the above relationship holds.

2.2 Composite Video Input Formats

Fusion 878A supports several composite video input formats. Table 2-1 shows the video formats and some of the countries in which each format is used.

Table 2-1. Video Input Formats Supported by the Fusion 878A

Format	Lines	Fields	F_{SC}	Country
NTSC-M	525	60	3.58 MHz	U.S., many others
NTSC-Japan[1]	525	60	3.58 MHz	Japan
PAL-B, G, H	625	50	4.43 MHz	Western/Central Europe, others
PAL-D	625	50	4.43 MHz	China
PAL-I	625	50	4.43 MHz	U.K., Ireland, South Africa
PAL-M	525	60	3.58 MHz	Brazil
PAL-N$_C$	625	50	3.58 MHz	Argentina
PAL-N	625	50	3.58 MHz	Paraguay, Uruguay
SECAM	625	50	4.406 MHz, 4.250 MHz	Eastern Europe, France, Middle East

NOTE(S):
[1] NTSC—Japan has 0 IRE setup.

The video decoder must be programmed appropriately for each of the composite video input formats. Table 2-2 lists the register values that need to be programmed for each input format.

Table 2-2. Register Values for Square Pixel Video Input Formats

Register	Bit	NTSC-M	NTSC-Japan	PAL-B, D, G, H, I	PAL-M	PAL-N	PAL-N Combination	SECAM
IFORM (0x01)	FORMAT [2:0]	001	010	011	100	101	111	110
Cropping: HDELAY VDELAY VACTIVE CROP HACTIVE	[7:0] in all five registers	Set to desired cropping values in registers	Set to NTSC-M square pixel values	Set to desired cropping values in registers	Set to NTSC-M square pixel values	Set to PAL-B, D, G, H, I square pixel values		
HSCALE	[15:0]	0x02AC	0x02AC	0x033C	0x02AC	0x033C	0x033C[1]	0x033C
ADELAY	[7:0]	0x70	0x70	0x7F	0x70	0x7F	0x7F	0x7F
BDELAY	[7:0]	0x5D	0x5D	0x72	0x5D	0x72	0x72	0xA0

NOTE(S):
[1] The Fusion 878A will not output square pixel resolution for PAL N-combination. A smaller number of pixels must be output.

2.3 Y/C Separation and Chroma Demodulation

Figure 2-2 illustrates Y/C separation and chroma decoding. Band-pass and notch filters are implemented to separate the composite video stream. The filter responses are illustrated in Figure 2-3. The optional chroma comb filter is implemented in the vertical scaling block. See Section 2.4.

Figure 2-4 schematically describes the filtering and scaling operations.

In addition to the Y/C separation and chroma demodulation illustrated in Figure 2-2, the Fusion 878A also supports chrominance comb filtering as an optional filtering stage after chroma demodulation. The chroma demodulation generates baseband I and Q (NTSC) or U and V (PAL/SECAM) color difference signals.

For S-Video operation, the digitized luma data bypasses the Y/C separation block completely and the digitized chrominance is passed directly to the chroma demodulator.

For monochrome operation, the Y/C separation block must be disabled and the saturation registers (SAT_U and SAT_V) are set to 0.

Figure 2-2. Y/C Separation and Chroma Demodulation for Composite Video

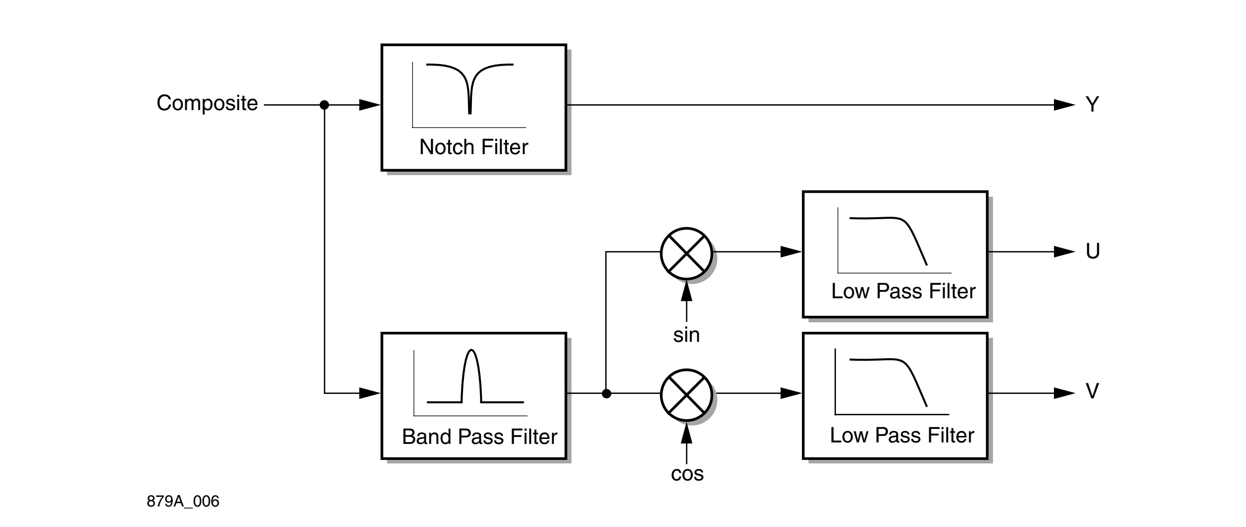


Figure 2-3. Y/C Separation Filter Responses

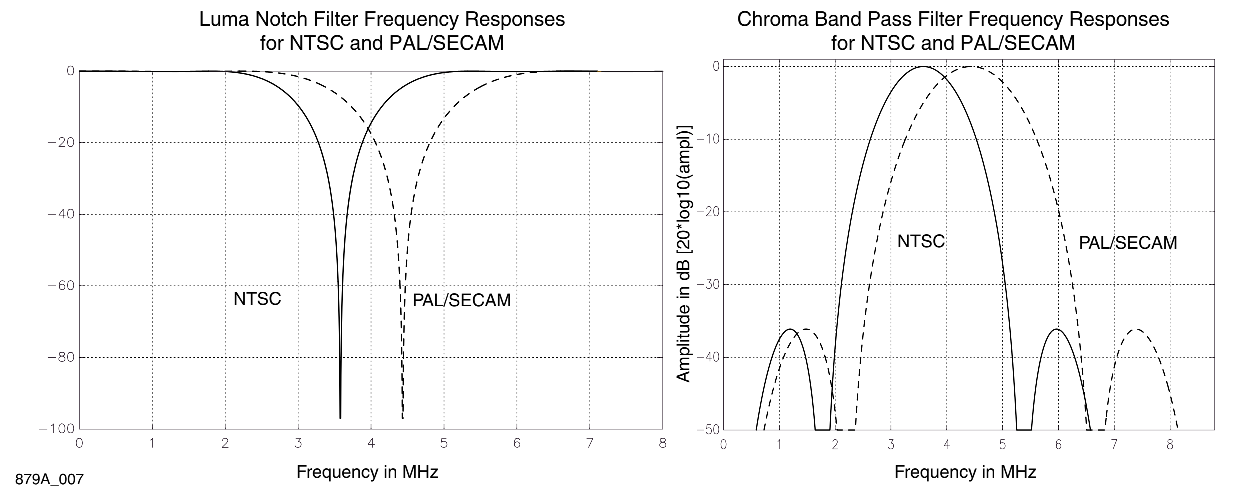
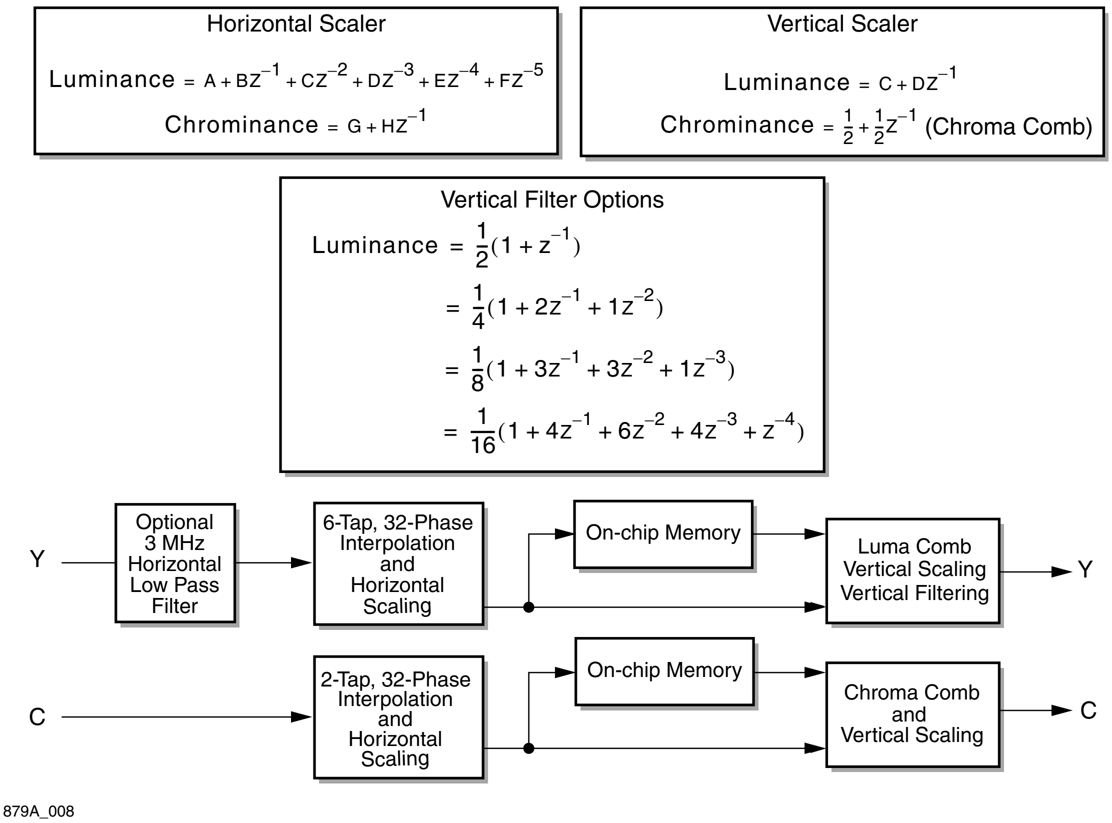


Figure 2-4. Filtering and Scaling


Horizontal Scaler
Luminance = $A + BZ^{-1} + CZ^{-2} + DZ^{-3} + EZ^{-4} + FZ^{-5}$
Chrominance = $G + HZ^{-1}$
Vertical Scaler
Luminance = $C + DZ^{-1}$
Chrominance = $\frac{1}{2} + \frac{1}{2}Z^{-1}$ (Chroma Comb)
Vertical Filter Options
Luminance = $\frac{1}{2}(1 + z^{-1})$
= $\frac{1}{4}(1 + 2z^{-1} + 1z^{-2})$
= $\frac{1}{8}(1 + 3z^{-1} + 3z^{-2} + 1z^{-3})$
= $\frac{1}{16}(1 + 4z^{-1} + 6z^{-2} + 4z^{-3} + z^{-4})$
Y
Optional 3 MHz Horizontal Low Pass Filter
6-Tap, 32-Phase Interpolation and Horizontal Scaling
On-chip Memory
Luma Comb Vertical Scaling Vertical Filtering
Y
C
2-Tap, 32-Phase Interpolation and Horizontal Scaling
On-chip Memory
Chroma Comb and Vertical Scaling
C
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NOTE(S): Z^{-1} refers to a pixel delay in the horizontal direction, and a line delay in the vertical direction. The coefficients are determined by UltraLock and the scaling algorithm.

2.4 Video Scaling, Cropping, and Temporal Decimation

The Fusion 878A provides three mechanisms to reduce the amount of video pixel data in its output stream: down-scaling, cropping, and temporal decimation. All three can be controlled independently.

2.4.1 Down-Scaling

2.4.1.1 Horizontal and Vertical Scaling

The Fusion 878A provides independent and arbitrary horizontal and vertical down- scaling. The maximum scaling ratio is 16:1 in both X and Y dimensions. The maximum vertical scaling ratio is reduced from 16:1 (when using frames) to 8:1 (when using fields). The different methods used for scaling luminance and chrominance are described in the following sections.

2.4.1.2 Field Aligned Vertical Scaling

If Common Interchange Format (CIF) resolution video is viewed at 60/50 Hz rates, then the video fields must be field-aligned for proper overlay (sequenced on top of each other successively). This could be done in interlaced Vertical Scaling mode (INT set) which group delays (filters) only one field by one line. The two fields are vertically aligned for overlay, but the two fields have different frequency responses. One has not been filtered, while the other has been line-averaged. A new option exists to filter both fields in a similar manner yet maintain proper field alignment. This mode is selected by setting VSFLDALIGN and resetting the INT bit to non-interlaced Vertical Scaling mode.

2.4.1.3 Luminance Scaling

Horizontal Scaling

The first stage in horizontal luminance scaling is an optional pre-filter which provides the capability to reduce anti-aliasing artifacts. It is generally desirable to limit the bandwidth of the luminance spectrum prior to performing horizontal scaling because the scaling of high-frequency components may create image artifacts in the resized image. The optional low pass filters illustrated in Figure 2-5 reduce the horizontal high-frequency spectrum in the luminance signal. Figure 2-6 and Figure 2-7 illustrates the combined results of the optional low-pass filters, the luma notch filter and the 2x oversampling filter. Figure 2-8 illustrates the combined responses of the luma notch filter and the 2x oversampling filter.

The Fusion 878A implements horizontal scaling through poly-phase interpolation. The Fusion 878A uses 32 different phases to accurately interpolate the value of a pixel. This provides an effective pixel jitter of less than 6 ns.

In simple pixel- and line-dropping algorithms, non-integer scaling ratios introduce a step function in the video signal that effectively introduces high-frequency spectral components. Poly-phase interpolation accurately interpolates to the correct pixel and line position providing more accurate information. This results in aesthetically pleasing video as well as higher compression ratios in bandwidth limited applications.

Figure 2-5. Optional Horizontal Luma Low-Pass Filter Responses

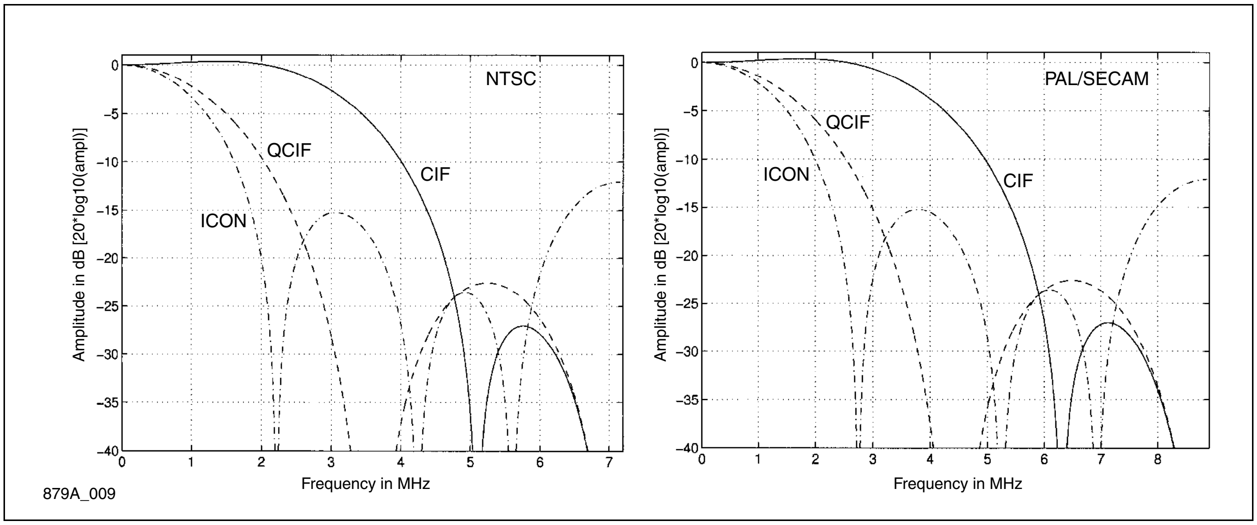


Figure 2-6. Combined Luma Notch, 2x Oversampling and Optional Low-Pass Filter Response (NTSC)

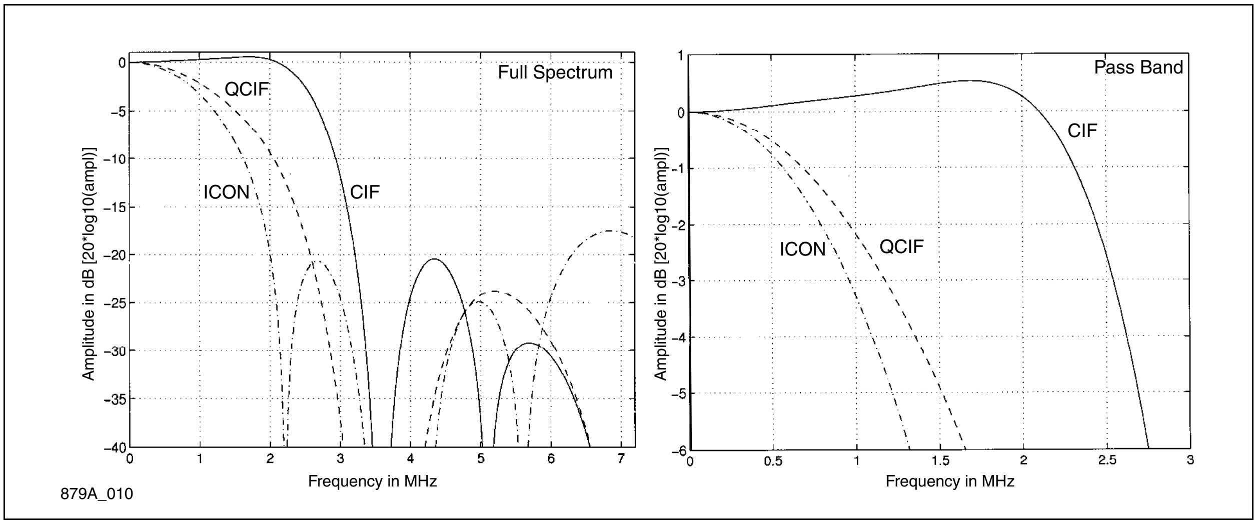


Figure 2-7. Combined Luma Notch, 2x Oversampling and Optional Low-Pass Filter Response (PAL/SECAM)

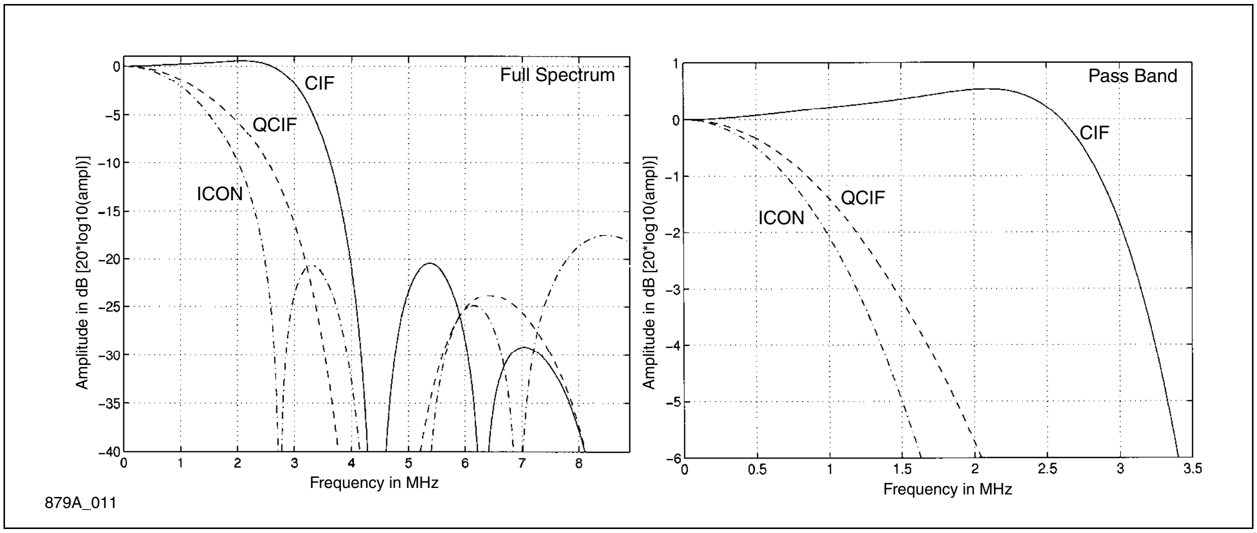
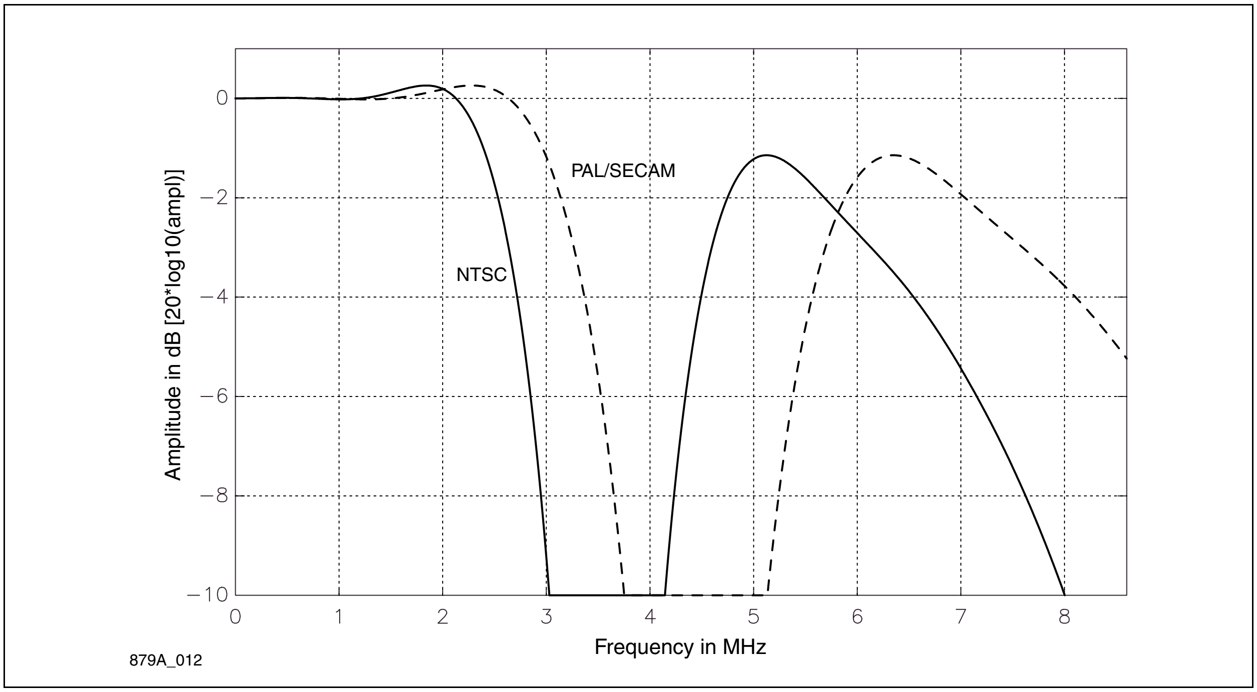


Figure 2-8. Combined Luma Notch and 2x Oversampling Filter Response

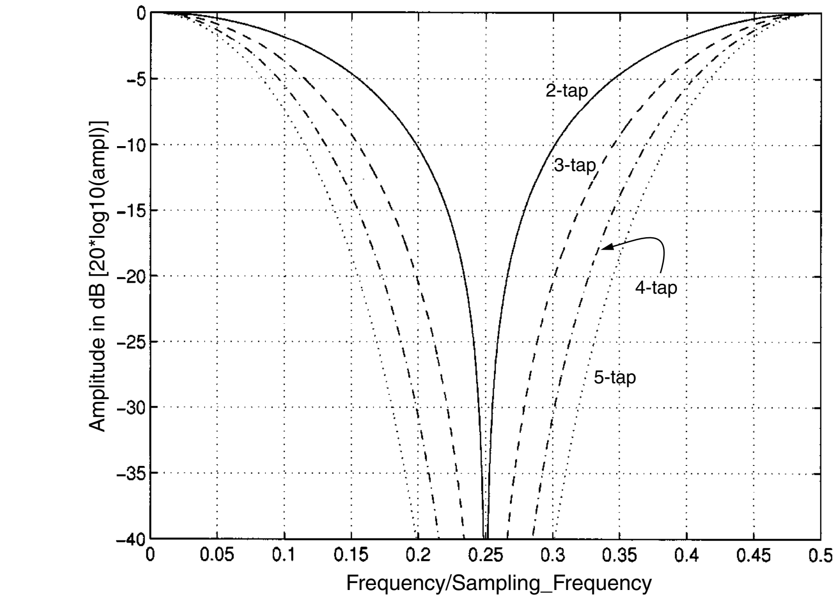


Vertical Scaling

For vertical scaling, the Fusion 878A uses a line store to implement four different filtering options. The filter characteristics are illustrated in Figure 2-9. The Fusion 878A provides up to 5-tap filtering to ensure removal of aliasing artifacts.

The Video Timing Control (VTC) register sets the number of taps in the vertical filter. The user may select 2, 3, 4 or 5 taps. The number of taps must be chosen in conjunction with the horizontal scale factor in order to ensure the needed data fits in the internal FIFO (see the VFILT bits in the VTC register for limitations). As the scaling ratio is increased, the number of taps available for vertical scaling increases. In addition to low-pass filtering, vertical interpolation is also employed to minimize artifacts when scaling to non-integer scaling ratios.

Figure 2-9. Frequency Responses for the Four Optional Vertical Luma Low-Pass Filters



2.4.1.4 Peaking

The Fusion 878A enables four different peaking levels by programming the PEAK bit and HFILT bits in the SCLOOP register. The filters are illustrated in Figure 2-10 and Figure 2-11. For more information, refer to *SC Loop Control Register*.

Figure 2-10. Peaking Filters

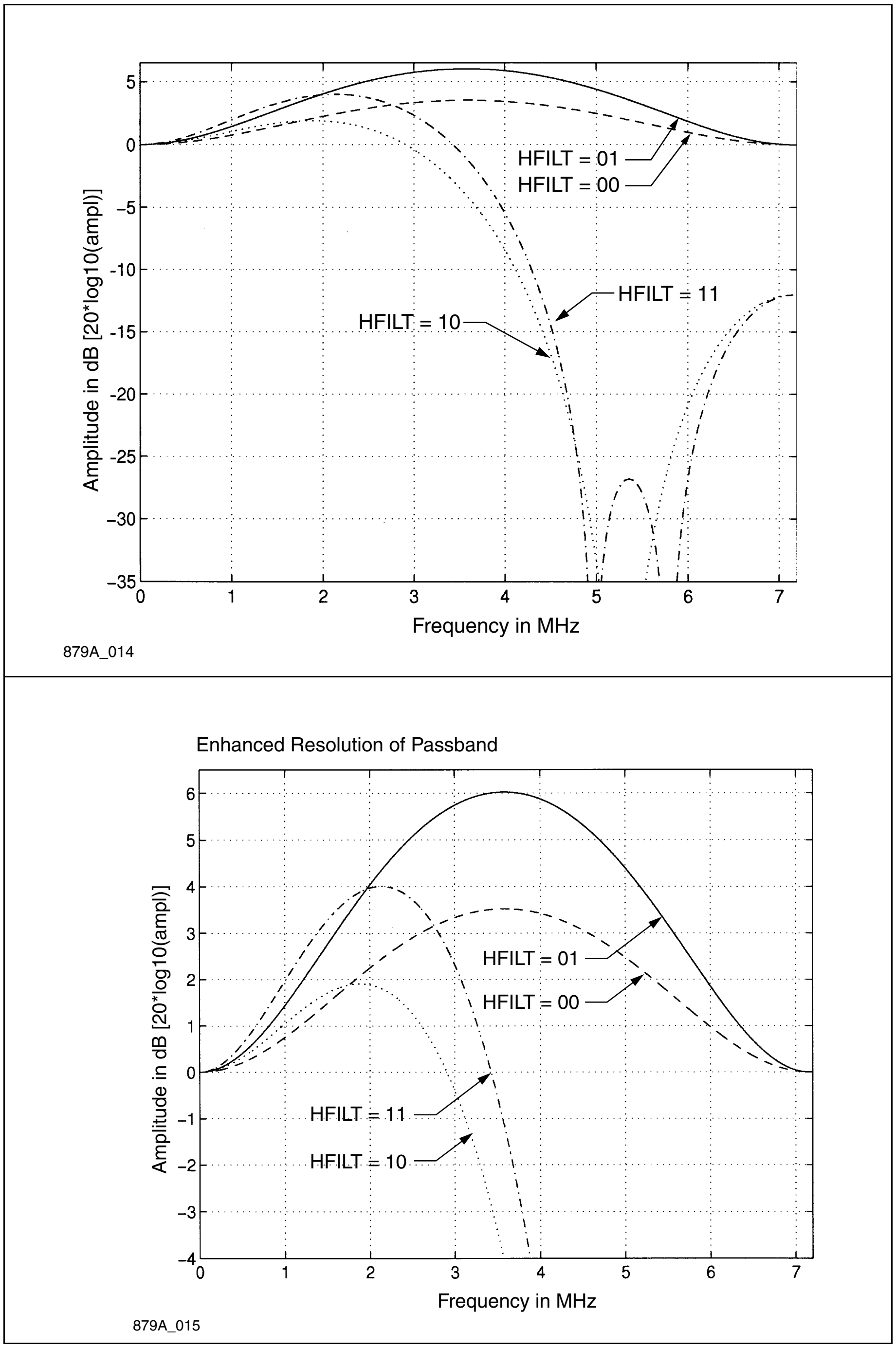
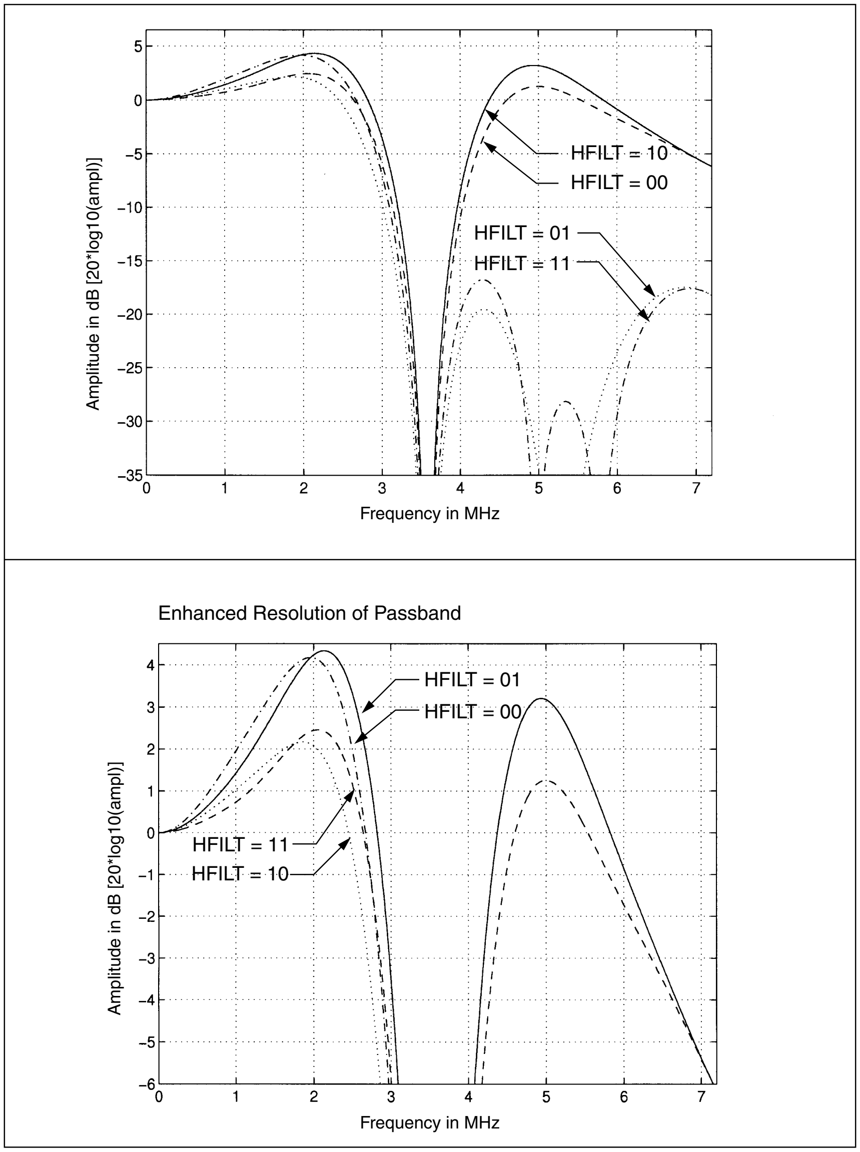


Figure 2-11. Luma Peaking Filters with 2x Oversampling Filter and Luma Notch (1 of 2)



Enhanced Resolution of Passband

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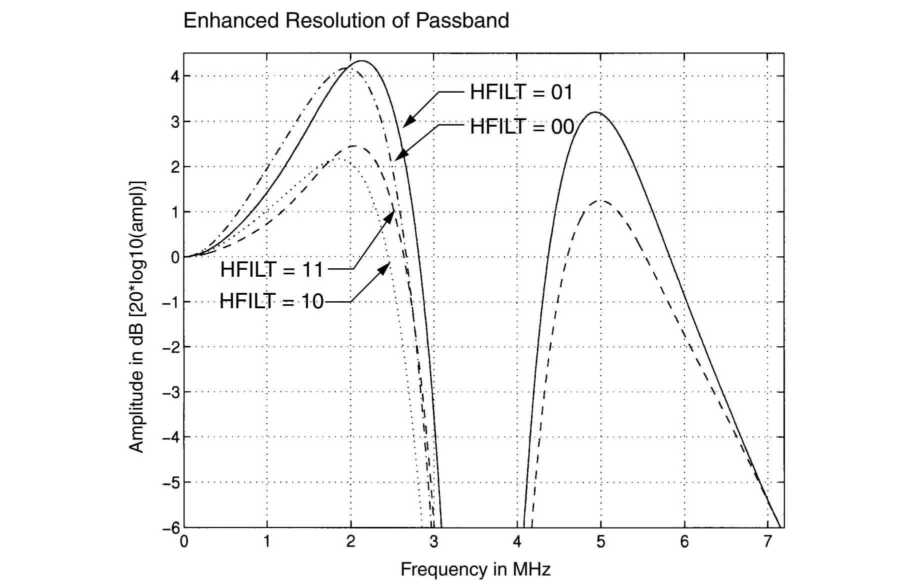
Figure 2-11. Luma Peaking Filters with 2x Oversampling Filter and Luma Notch *(2 of 2)*



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2.4.1.5 Chrominance Scaling

A 2-tap, 32-phase interpolation filter is used for horizontal scaling of chrominance. Vertical scaling of chrominance is implemented through chrominance comb filtering using a line store, followed by simple decimation or line dropping.

2.4.1.6 Scaling Registers

The Horizontal Scaling Ratio Register (HSCALE)

HSCALE is programmed with the horizontal scaling ratio. When outputting unscaled video (in NTSC), the Fusion 878A produces 910 pixels per line. This corresponds to the pixel rate at fCLK x 1 (4 × Fsc). This register is the control for scaling the video to the desired size. For example, square pixel NTSC requires 780 samples per line, while CCIR 601 requires 858 samples per line. HSCALE_HI and HSCALE_LO are two 8-bit registers that, when concatenated, form the 16-bit HSCALE register. The method below uses pixel ratios to determine the scaling ratio. The following formula should be used to determine the scaling ratio to be entered into the 16-bit register:

$$\text{NTSC:} \quad \text{HSCALE} = [\,(910/P_{\text{desired}}) - 1] \times 4096$$

$$\text{PAL/SECAM:} \quad \text{HSCALE} = [\,(1135/P_{\text{desired}}) - 1] \times 4096$$

where: $P_{desired}$ = Desired number of pixels per line of video, including active, sync and blanking.

For example, to scale PAL/SECAM input to square pixel QCIF, the total number of horizontal pixels desired is 236:

$$\begin{aligned} \text{HSCALE} &= [\,(1135/236) - 1\,] \times 4096 \\ &= 12331 \\ &= 0 \times 3\text{CF2} \end{aligned}$$

An alternative method for determining the HSCALE value uses the ratio of the scaled active region to the unscaled active region as shown below:

$$\begin{aligned} &\text{NTSC:} && \text{HSCALE} = [\,(754 / \text{HACTIVE}) - 1] \times 4096 \\ &\text{PAL/SECAM:} && \text{HSCALE} = [\,(922 / \text{HACTIVE}) - 1] \times 4096 \end{aligned}$$

where: HACTIVE = Desired number of pixels per line of video, not including sync or blanking.

In this equation, the HACTIVE value cannot be cropped; it represents the total active region of the video line. This equation produces roughly the same result as using the full line length ratio shown in the first example. However, due to truncation, the HSCALE values determined using the active pixel ratio method will be slightly different from those obtained using the total line length pixel ratio method. The values in Table 2-3, were calculated using the full line length ratio.

The Vertical Scaling Ratio Register (VSCALE)

VSCALE is programmed with the vertical scaling ratio. It defines the number of vertical lines output by the Fusion 878A. The following formula should be used to determine the value to be entered into this 13-bit register. The loaded value is a two's-complement, negative value.

$$\text{VSCALE} = (\,0\text{x}10000 - \{\,[\,(\,\text{scaling\_ratio}\,) - 1] \times 512\,\}\,) + 0\text{x1FFF}$$

For example, to scale PAL/SECAM input to square pixel QCIF, the total number of vertical lines is 156:

$$\begin{aligned} \text{VSCALE} &= (\,0\text{x}10000 - \{\,[\,(4/1) - 1\,] \times 512\,\}\,) + 0\text{x1FFF} \\ &= 0\text{x1A00} \end{aligned}$$

Only the 13 LSBs of the VSCALE value are used; the five LSBs of VSCALE_HI and the 8-bit VSCALE_LO register form the 13-bit VSCALE register. The three MSBs of VSCALE_HI are used to control other functions. The user must take care not to alter the values of the three MSBs when writing a vertical scaling value.

The following C-code fragment illustrates changing the vertical scaling value:

```
#define VSCALE_HI 0x13
#define VSCALE_LO 0x14
typedef unsigned char BYTE;
typedef unsigned int WORD;

BYTE ReadFromFusion878A(BYTE regAddress);
void WriteToFusion878A(BYTE regAddress, BYTE regValue);

void SetFusion878AVScaling(WORD VSCALE)
{
   BYTE oldVscaleMSByte, newVscaleMSByte;

   /* get existing VscaleMSByte value from */
   /* Fusion878A VSCALE_HI register */
   oldVscaleMSByte = ReadFromFusion878A(VSCALE_HI);

   /* create a new VscaleMSByte, preserving top 3 bits */
   newVscaleMSByte = (oldVscaleMSByte & 0xE0)|(VSCALE >>
         8);

   /* send the new VscaleMSByte to the VSCALE_HI reg */
   WriteToFusion878A(VSCALE_HI, newVscaleMSByte);

   /* send the new VscaleLSByte to the VSCALE_LO reg */
   WriteToFusion878A(VSCALE_LO, (BYTE) VSCALE);
}
```

where:	&	= bitwise AND
	|	= bitwise OR
	>>	= bit shift, MSB to LSB

If your target machine has sufficient memory to statically store the scaling values locally, the READ operation can be eliminated.

NOTE: When scaling below CIF resolution, it may be useful to use a single field as opposed to using both fields. Using a single field will ensure there are no inter-field motion artifacts on the scaled output. When performing single field scaling, the vertical scaling ratio will be twice as large as when scaling with both fields. For example, CIF scaling from one field does not require any vertical scaling, but when scaling from both fields, the scaling ratio is 50%. Also, the non-interlaced bit should be reset when scaling from a single field (INT=0 in the VSCALE_HI register).

Table 2-3 lists scaling ratios for various video formats and the register values required.

Table 2-3. Scaling Ratios for Popular Formats Using Frequency Values

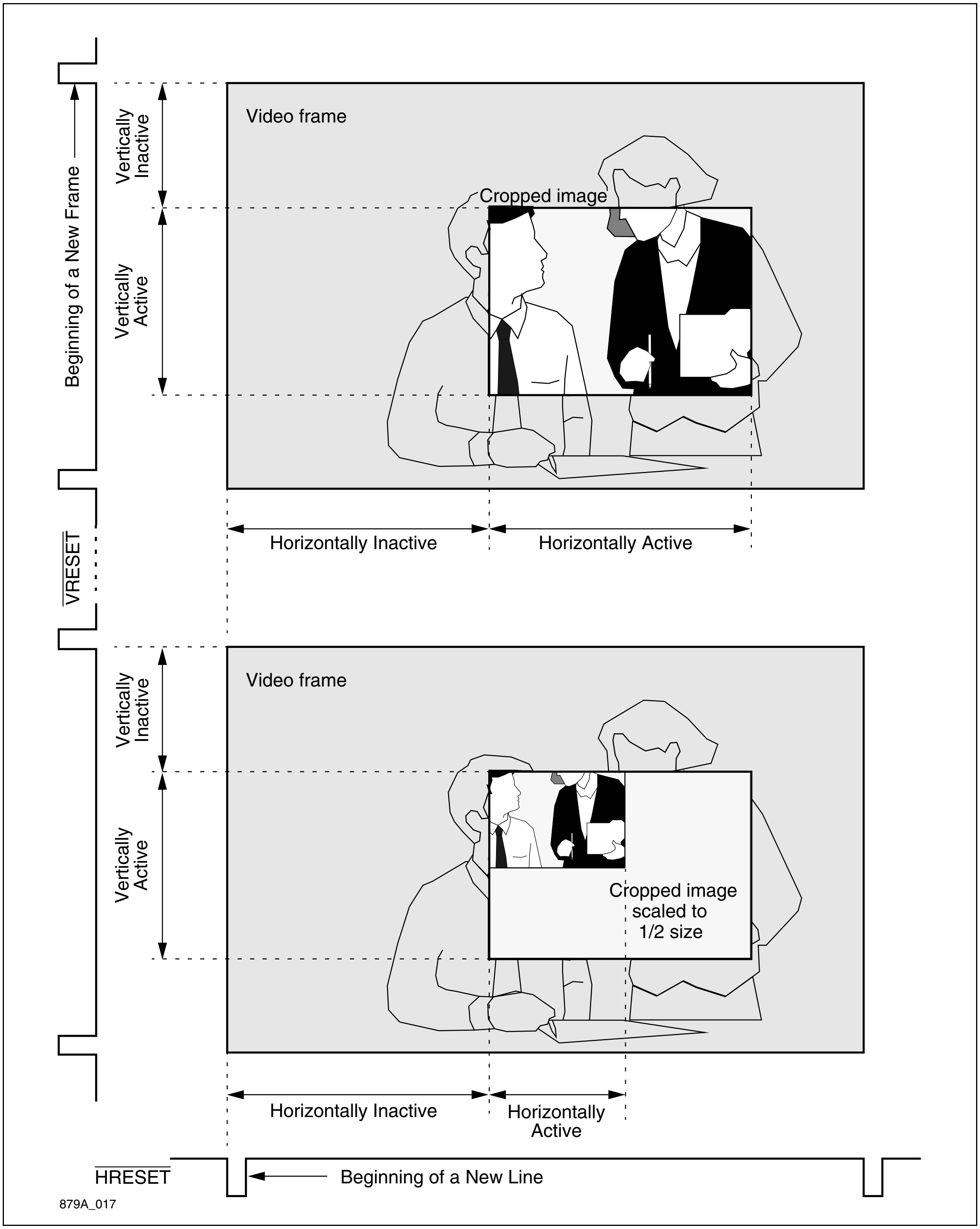
Scaling Ratio	Format	Total Resolution[1]	Output Resolution (Active Pixels)	HSCALE Register Values	VSCALE Register Values	
					Use Both Fields	Single Field
Full Resolution 1:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR 601 PAL SQ Pixel	780x525 858x525 864x625 944x625	640x480 720x480 720x576 768x576	0x02AA 0x00F8 0x0504 0x033C	0x0000 0x0000 0x0000 0x0000	N/A N/A N/A N/A
CIF 2:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR 601 PAL SQ Pixel	390x262 429x262 432x312 472x312	320x240 360x240 360x288 384x288	0x1555 0x11F0 0x1A09 0x1679	0x1E00 0x1E00 0x1E00 0x1E00	0x0000 0x0000 0x0000 0x0000
QCIF 4:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR 601 PAL SQ Pixel	195x131 214x131 216x156 236x156	160x120 180x120 180x144 192x144	0x3AAA 0x3409 0x4412 0x3CF2	0x1A00 0x1A00 0x1A00 0x1A00	0x1E00 0x1E00 0x1E00 0x1E00
ICON 8:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR 601 PAL SQ Pixel	97x65 107x65 108x78 118x78	80x60 90x60 90x72 96x72	0x861A 0x7813 0x9825 0x89E5	0x1200 0x1200 0x1200 0x1200	0x1A00 0x1A00 0x1A00 0x1A00

NOTE(S):
[1] Including sync and blanking interval.

2.4.2 Image Cropping

Cropping enables the user to output any subsection of the video image. The start of the active area in the vertical direction is referenced to $\overline{\text{VRESET}}$ (beginning of a new field). In the horizontal direction it is referenced to $\overline{\text{HRESET}}$ (beginning of a new line). The dimensions of the active video region are defined by HDELAY, HACTIVE, VDELAY, and VACTIVE. All four registers are 10-bit values. The CROP register contains two MSBs of each register, while the lower eight bits are in the respective HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO registers. The vertical and horizontal delay values determine the position of the cropped image within a frame while the horizontal and vertical active values set the pixel dimensions of the cropped image as illustrated in Figure 2-12.

Figure 2-12. Effect of the Cropping and Active Registers



2.4.2.1 Cropping Registers

Horizontal Delay Register (HDELAY)

For video decoding, HDELAY is programmed with the number of pixels between horizontal sync and the first pixel of each line to be displayed or captured. For GPIO SPIOUT, the HDELAY is programmed with the number of pixels between the falling edge of HRESET and the rising edge of HACTIVE. HDELAY should be an even number to get Cb as the first pixel, an odd number to get Cr.

The register value is programmed with respect to the scaled frequency clock.

Horizontal Active Register (HACTIVE)

For video decoding, HACTIVE is programmed with the actual number of displayed or captured pixels per line. For GPIO SPIOUT, HACTIVE is programmed with the number of pixels that HACTIVE signal is high after the HACTIVE signal goes high.

The register value is programmed with respect to the scaled frequency clock. The video line can be considered a combination of three components:

1. Back porch and Sync: defined by HDELAY
2. Active Video: defined by HACTIVE
3. Front Porch: total scaled pixels—HDELAY through HACTIVE

For uncropped images, the square pixel values for these components at 4 × Fsc are displayed in Table 2-4.

Table 2-4. Square Pixel Values

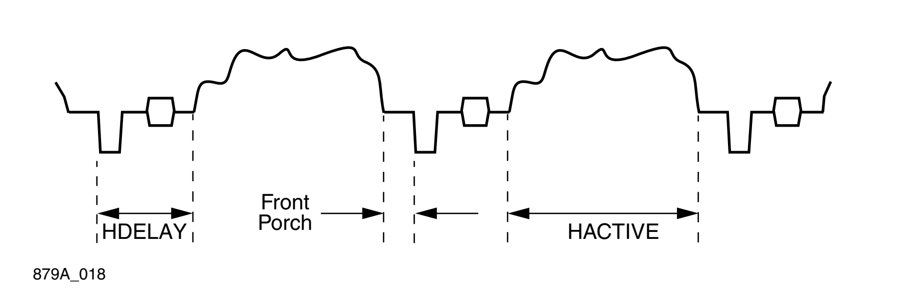
Video Standard	CLK x 1 Front Porch	CLK x 1 HDELAY	CLK x 1 HACTIVE	CLK x 1 Total
NTSC	21	135	754	910
PAL/SECAM	27	186	922	1135

Therefore, for uncropped images the values are:

HDELAY (NTSC) = (135/754 × HACTIVE) & 0x3FE
HDELAY(PAL) = (186/922 × HACTIVE) & 0x3FE

For cropped images, HDELAY can be increased and HACTIVE decreased so that HDELAY + HACTIVE ≤ 889 × HSCALE for NTSC and ≤ 1108 × HSCALE for PAL. If HDELAY + HACTIVE is too much, then you will see front or back porch pixels. Regions of the video signal are illustrated in Table 2-13.

Figure 2-13. Regions of the Video Signal



The Vertical Delay Register (VDELAY)

For video decoding, VDELAY is programmed with the number of half lines between the end of the serration pulses and the first line to be displayed or captured.

For GPIO SPIOUT, VDELAY is programmed with the number of half lines between the rising edge of $\overline{\text{VRESET}}$ and the rising edge of VACTIVE.

The register value is programmed with respect to the unscaled input signal. VDELAY must be programmed to an even number to avoid apparent field reversal.

The Vertical Active Register (VACTIVE)

For video decoding and GPIO SPIOUT, VACTIVE is programmed with the number of lines in one frame for the source video.

NOTE: It is important to note the difference between the implementation of the horizontal registers (HSCALE, HDELAY, and HACTIVE) and the vertical registers (VSCALE, VDELAY, and VACTIVE). Horizontally, HDELAY and HACTIVE are programmed with respect to the scaled pixels defined by HSCALE. Vertically, VDELAY and VACTIVE are programmed with respect to the number of lines before scaling (before VSCALE is applied).

For GPIO SPIIN, the registers HDELAY, HACTIVE, VDELAY, and VACTIVE are not used.

2.4.3 Temporal Decimation

Temporal decimation provides a solution for video synchronization during periods when full frame rate cannot be supported due to bandwidth and system restrictions.

For example, when capturing live video for storage, system limitations such as hard disk transfer rates or system bus bandwidth may limit the frame capture rate. If these restrictions limit the frame rate to 15 frames per second, the Fusion 878As time scaling operation enables the system to capture every other frame instead of allowing hard disk timing restrictions to dictate which frame to capture. This maintains an even distribution of captured frames and alleviates the “jerky” effect caused by systems that simply burst in data when the bandwidth becomes available.

The Fusion 878A provides temporal decimation on either a field or frame basis. The temporal decimation register (TDEC) is loaded with a value from 1 to 60 (NTSC) or 1 to 50 (PAL/SECAM). This value is the number of fields or frames skipped by the chip during a sequence of 60 for NTSC or 50 for PAL/SECAM. Skipped fields and frames are considered inactive, which is indicated by the ACTIVE pin remaining low.

Examples:

TDEC = 0x02 Decimation is performed by frames. Two frames are skipped per 60 frames of video, assuming NTSC decoding.

Frames 1–29 are output normally, then ACTIVE remains low for one frame. Frames 31–59 are then output followed by another frame of inactive video.

TDEC = 0x9E Decimation is performed by fields. Thirty fields are output per 60 fields of video, assuming NTSC decoding.

This value outputs every other field (every odd field) of video starting with field 1 in frame 1.

TDEC = 0x01 Decimation is performed by frames. One frame per 50 frames of video is skipped, assuming PAL/SECAM decoding.

TDEC = 0x00 Decimation is not performed. Full frame rate video is output by the Fusion 878A.

When changing the programming in the temporal decimation register, 0x00 should be loaded first, and then the decimation value. This ensures that the decimation counter is reset to 0. If 0 is not loaded first, the decimation may start on any field or frame in the sequence of 60 (or 50 for PAL/SECAM). On power-up, this preload is not necessary because the counter is internally reset.

When decimating fields, the FLDALIGN bit in the TDEC register can be programmed to choose whether the decimation starts with an odd field or an even field. If the FLDALIGN bit is set to logical 0, the first field dropped during the decimation process will be an odd field. Conversely, setting the FLDALIGN bit to logical 1 causes the even field to be dropped first in the decimation process.

2.5 Video Adjustments

The Fusion 878A provides programmable hue, contrast, saturation, and brightness.

2.5.1 The Hue Adjust Register

The Hue Adjust Register (HUE) is used to offset the hue of the decoded signal. In NTSC, the hue of the video signal is defined as the phase of the subcarrier with reference to the burst. The value programmed in this register is added to or subtracted from the phase of the subcarrier, which effectively changes the hue of the video. The hue can be shifted by ±90 degrees. Because of the nature of PAL/SECAM encoding, hue adjustments can not be made when decoding PAL/SECAM.

2.5.2 The Contrast Adjust Register

The Contrast Adjust Register (CONTRAST) (also called the luma gain) provides the ability to change the contrast from approximately 0% to 200% of the original value. The decoded luma value is multiplied by the 9-bit coefficient loaded into this register.

2.5.3 The Saturation Adjust Registers

The Saturation Adjust Registers (SAT_U, SAT_V) are additional color adjustment registers. It is a multiplicative gain of the U and V signals. The value programmed in these registers are the coefficients for the multiplication. The saturation range is from approximately 0% to 200% of the original value.

2.5.4 The Brightness Register

The Brightness Register (BRIGHT) is simply an offset for the decoded luma value. The programmed value is added to or subtracted from the original luma value which changes the brightness of the video output. The luma output is in the range of 0 to 255. Brightness adjustment can be made over a range of –128 to +127.

2.6 Automatic Chrominance Gain Control

The Automatic Chrominance Gain Control (ACGC) compensates for reduced chrominance and color-burst amplitudes. Here, the color-burst amplitude is calculated and compared to nominal. The color-difference signals are then increased or decreased in amplitude according to the color-burst amplitude difference from nominal. The range of chrominance gain is 0.5–2 times the original amplitude. This compensation coefficient is then multiplied by the saturation adjust value for a total chrominance gain range of 0–2 times the original signal. Automatic chrominance gain control may be disabled.

2.7 Low Color Detection and Removal

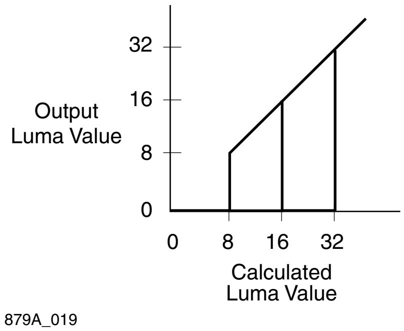
If a color-burst of 25 percent (NTSC) or 35 percent (PAL/SECAM) or less of the nominal amplitude is detected for 127 consecutive scan lines, the color-difference signals U and V are set to 0. When the low color detection is active, the reduced chrominance signal is still separated from the composite signal to generate the luminance portion of the signal. The resulting Cr and Cb values are 128. Output of the chrominance signal is re-enabled when a color-burst of 43 percent (NTSC) or 60 percent (PAL/SECAM) or greater of nominal amplitude is detected for 127 consecutive scan lines. Low color detection and removal may be disabled.

2.8 Coring

The Fusion 878A video decoder can perform a coring function, in which it forces all values below a programmed level to be 0. This is useful as the human eye is more sensitive to variations in black images. By taking near-black images and turning them into black, the image appears clearer to the eye.

Four coring values can be selected: 0, 8, 16, or 32 above black. If the total luminance level is below the selected limit, the luminance signal is truncated to the black value. If the luma range is limited (i.e., black is 16), then the coring circuitry automatically takes this into account and references the appropriate value for black. Coring is illustrated in Figure 2-14.

Figure 2-14. Coring Map



2.9 VBI Data Output Interface

A frame of video is composed of 525 lines for NSTC and 625 for PAL/SECAM. Figure 2-15 illustrates an NTSC video frame, in which there are a number of distinct regions. The video image or picture data is contained in the odd and even fields within lines 21 to 263 and lines 283 to 525, respectively. Each field of video also contains a region for vertical synchronization (lines 1 through 9 and 264 through 272) as well as a region which can contain non-video ancillary data (lines 10 through 20 and 273 through 283). These regions between the vertical synchronization region and the video picture region are referred to as the VBI portion of the video signal. Figure 2-16 illustrates the PAL video frame.

Figure 2-15. Regions of the NTSC Video Frame

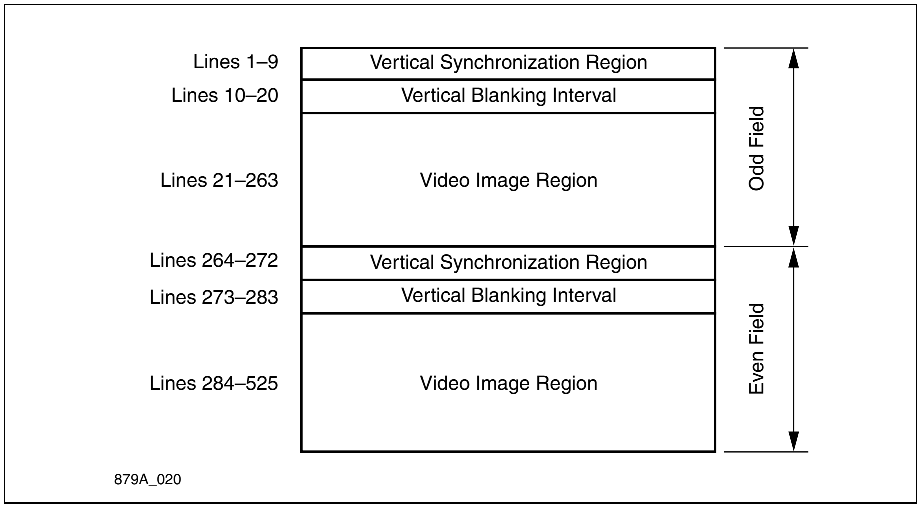
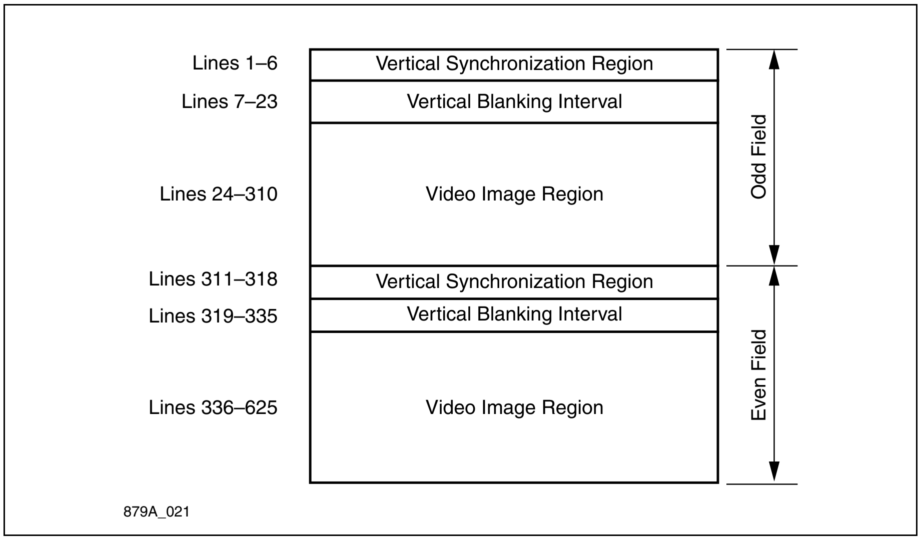


Figure 2-16. Regions of the PAL Video Frame (Fields 1, 2, 5, and 6)



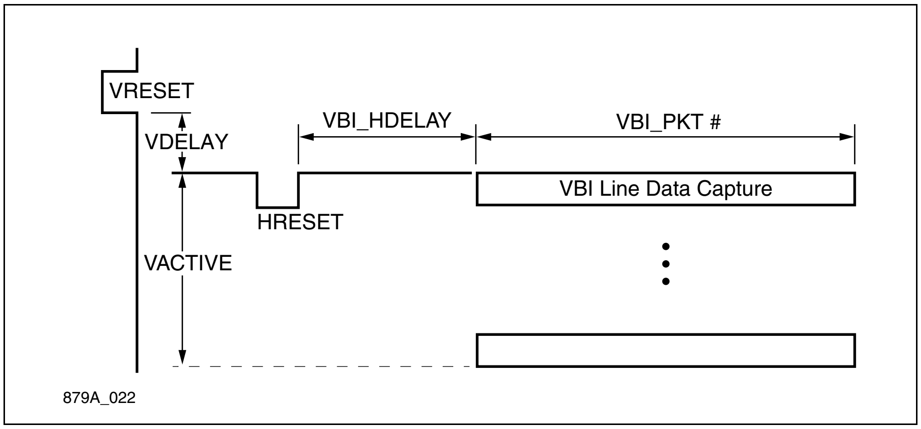
The Fusion 878A is able to capture VBI data and store it in the host memory for later processing by the Fusion 878A VBI decoder software. Two modes of VBI capture exist: VBI line output mode and VBI frame output mode. Both types of data may be captured during the same field.

2.9.1 VBI Line Output Mode

In the VBI line output mode, VBI capture occurs during the vertical blanking interval. The start of VBI data capture is set by the VBI_HDELAY bit in the VBI Packet Size/Delay register, and is in reference to the trailing edge of the HRESET signal. The number of DWORDs of VBI data is selected by the user. Each DWORD contains 4 VBI bytes, and each VBI pixel consists of two VBI samples. For example, for a given 800 pixel line in the VBI region, there exist 1600 VBI samples, which are equivalent to 400 DWORDs of VBI data. The VBI_PKT_HI and VBI_PKT_LO register bits are concatenated to create the 9-bit value for the number of DWORDs to be captured.

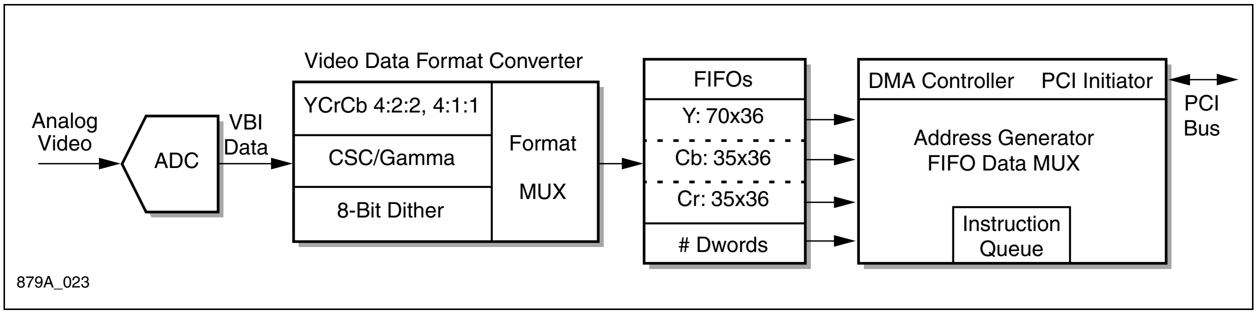
VBI line data capture occurs when the CAPTURE_VBI_EVEN register bit is enabled for the even field, and CAPTURE_VBI_ODD register bit is enabled for the odd field. The VBI data is sampled at a rate of 8 × Fsc and is stored in the FIFO as a sequence of 8-bit samples. Line mode VBI data starts horizontally beginning at VBI_HDELAY pixels from the trailing edge of HRESET and ending after the VBI_PKT number of DWORDs. Line mode VBI data starts vertically beginning at the first line following VRESET and ending at VACTIVE. VBI register settings can be changed only on a per-frame basis. The VBI timing is illustrated in Figure 2-17.

Figure 2-17. VBI Timing



Once the VBI data has been captured and stored in the Fusion 878A FIFO, it is treated as any other type of data. It is output over the PCI bus via RISC instructions. If the number of VBI lines desired by the user is smaller than the entire vertical blanking region, the extra data will be discarded by the use of the SKIP RISC instruction. Alternatively, if the user desires a larger VBI region in the VBI line output mode, the vertical blanking region can be extended by setting the VDELAY register to the appropriate value. The VBI line output mode can in effect extend the VBI region to the entire field. Figure 2-18 illustrates a block diagram of the VBI section.

Figure 2-18. VBI Section Block Diagram



In the VBI frame output mode, VBI data capture occurs in the active video region and includes all the horizontal blank/sync information in the data stream. This feature can be used to provide a high quality still-capture of video. The data is vertically bound beginning at the first line during VACTIVE and ending after a fixed number of packets. The data stream is packetized into a series of 256-DWORD blocks.

A fixed number of DWORD blocks (434 for NTSC and 650 for PAL) are captured during each field. This is equivalent to 111,104 DWORDs for NTSC (434 × 256 DWORDs) and 166,400 DWORDs for PAL (650 × 256 DWORDs) per field. The VBI frame capture region can be extended to include the 10 lines prior to the default VACTIVE region by setting the EXT_FRAME register bit. VDELAY must also be set to its minimum value of 2. The extended DWORD block size is 450 DWORD blocks for NTSC and 674 DWORD blocks for PAL.

The VBI frame data capture occurs during the even field when the CAPTURE_EVEN register bit is set and the COLOR_EVEN bit is set to raw mode, and during the odd field when the CAPTURE_ODD register bit is set and the COLOR_ODD bit is set to raw mode. The captured data stream is continuous and not aligned with HSYNC.

2.10 Video Data Format Conversion

2.10.1 Pixel Data Path

The video decoder/scaler portion of the Fusion 878A generates a video data stream in packed 4:2:2 YCrCb format. The video data is then color space-converted and formatted in a 32-bit wide DWORD. Figure 2-19 illustrates the steps in converting the video data from packed 4:2:2 YCrCb to the desired format. The YCrCb 4:2:2 data is up-sampled to 4:4:4 format prior to conversion to RGB. It can then be dithered, have gamma correction removed, or be presented directly to the byte swap circuit.

In the case where 4:1:1 data is desired, the 4:2:2 data is first down-sampled, then packed into BtYUV format (see Table 2-6) or converted to planar format and vertically sub-sampled to achieve the YUV9 format. Alternatively, packed 4:2:2 data may be converted to planar 4:2:2 and vertically sub-sampled to YUV12 format. The vertical sub-sampling is achieved via the appropriate DMA instructions (see Section 2.12).

Fusion 878A also offers a Y8 color format, in which the chroma component of the packed 4:2:2 data is stripped and the luma component is packed into 8 bits. This format is otherwise known as gray scale. Table 2-5 lists the various color formats supported by the Fusion 878A and the mapping of the bytes onto 32-bit DWORDs.

2.10.2 Video Control Code Status Data

In addition to the pixel information, the Fusion 878A's Video Data Format Converter provides four bits of video control status code to the FIFO. These four bits of status code STATUS[3:0] are based on inputs from the video decoder/scaler block of the Fusion 878A and convey information about the pixel data and the state of the video timing (see Figure 2-19). STATUS[3:0] bits have four uses:

1. To specify the FIFO mode (packed or planar)
2. To provide information regarding the pixel data (respective position of the pixel and number of valid bytes)
3. To indicate whether the pixel data is valid
4. To signal the end of a capture enabled field

Figure 2-19. Video Data Format Converter

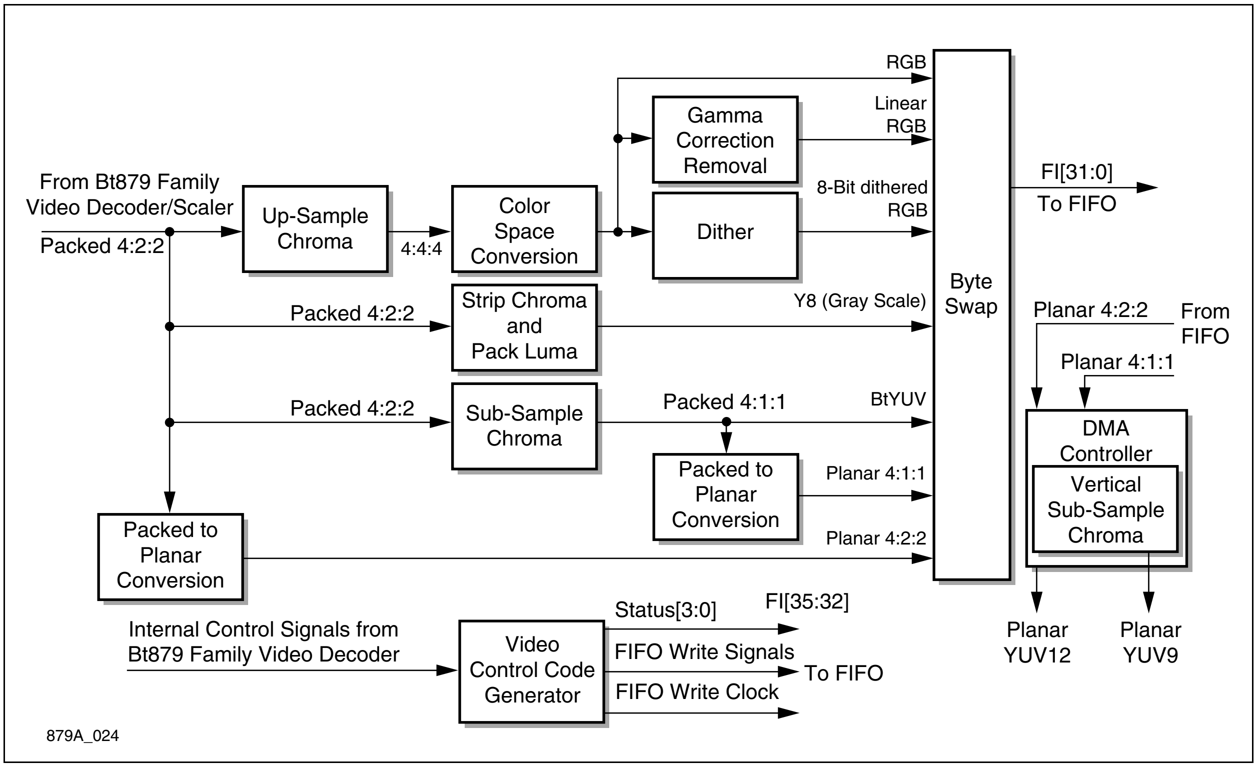


Table 2-5. Color Formats

Format	DWORD	Pixel Data [31:0]			
		Byte Lane 3 [31:24]	Byte Lane 2 [23:16]	Byte Lane 1 [15:8]	Byte Lane 0 [7:0]
RGB32[(1)]	dw0	Alpha	R	G	B
RGB24	dw0	B1	R0	G0	B0
	dw1	G2	B2	R1	G1
	dw2	R3	G3	B3	R2
RGB16	dw0	{R1[7:3],G1[7:2],B1[7:3]}		{R0[7:3],G0[7:2],B0[7:3]}	
RGB15	dw0	{0,R1[7:3],G1[7:3],B1[7:3]}		{0,R0[7:3],G0[7:3],B0[7:3]}	
YUY2—YCrCb 4:2:2[(2)]	dw0	Cr0	Y1	Cb0	Y0
	dw1	Cr2	Y3	Cb2	Y2
BtYUV—YCrCb 4:1:1	dw0	Y1	Cr0	Y0	Cb0
	dw1	Y3	Cr4	Y2	Cb4
	dw2	Y7	Y6	Y5	Y4
Y8 (Gray Scale)	dw0	Y3	Y2	Y1	Y0
8 Bit Dithered	dw0	B3	B2	B1	B0
VBI Data	dw0	D3	D2	D1	D0
YCrCb 4:2:2 Planar	dw0 FIFO1	Y3	Y2	Y1	Y0
	dw1 FIFO1	Y7	Y6	Y5	Y4
	dw0 FIFO2	Cb6	Cb4	Cb2	Cb0
	dw0 FIFO3	Cr6	Cr4	Cr2	Cr0
YUV12 Planar	Vertically sub-sampled to 4:2:2 by the DMA controller				
YCrCb 4:1:1 Planar	dw0 FIFO1	Y3	Y2	Y1	Y0
	dw1 FIFO1	Y7	Y6	Y5	Y4
	dw2 FIFO1	Y11	Y10	Y9	Y8
	dw3 FIFO1	Y15	Y14	Y13	Y12
	dw0 FIFO2	Cb12	Cb8	Cb4	Cb0
	dw0 FIFO3	Cr12	Cr8	Cr4	Cr0
YUV9 Planar	Vertically sub-sampled to 4:1:1 by the DMA controller				

NOTE(S):

[(1)] The alpha byte can be written as 0 data, or not written.

[(2)] UYVY can be achieved by byte swapping.

3. All planar modes require the HACTIVE register to be multiple of 16 pixels.

2.10.3 YCrCb to RGB Conversion

The 4:2:2 YCrCb data stream from the video decoder portion of the Fusion 878A must be converted to 4:4:4 YCrCb before the RGB conversion occurs, using an interpolation filter on the chroma data path. The even valid chroma data passes through unmodified, while the odd data is generated by averaging adjacent even data. The chroma component is up-sampled using the following equations:

For n = 0, 2, 4, etc.

$$Cb_n = Cb_n$$
$$Cr_n = Cr_n$$
$$Cb_{n+1} = (Cb_n + Cb_{n+2})/2$$
$$Cr_{n+1} = (Cr_n + Cr_{n+2})/2$$

RGB Conversion:

$$R = 1.164(Y–16) + 1.596(Cr–128)$$
$$G = 1.164(Y–16) – 0.813(Cr–128) – 0.391(Cb–128)$$
$$B = 1.164(Y–16) + 2.018(Cb–128)$$

Y range = [16,235]
Cr/Cb range = [16,240]
RGB range = [0,255]

2.10.4 Gamma Correction Removal

Fusion 878A provides gamma correction removal capability. The available gamma values are:

NTSC: $RGBout = RGBin^{2.2}$
PAL: $RGBout = RGBin^{2.8}$

Gamma correction removal capability is not programmable on a field basis. Furthermore, gamma correction removal is not available when YCrCb data is output.

2.10.5 YCrCb Sub-sampling

The 4:2:2 data stream is horizontally sub-sampled to 4:1:1 using the following equations:

For n = 0, 4, 8, etc.:

$$Cb_n = (Cb_n + Cb_{n+2})$$
$$Cr_n = (Cr_n + Cr_{n+2})$$

Vertical sub-sampling is supported by Fusion 878As YUV9 and YUV12 planar modes. In these modes, the video data is first planarized and placed in the FIFO as 4:2:2 planar or 4:1:1 planar data. The FIFO data is then vertically sub-sampled to 4:1:1 for YUV9 and 4:2:2 for YUV12 formats. The vertical sub-sampling is performed via RISC instructions that are executed by the DMA controller.

Table 2-5, shows an example of a 4-pixel line for YUV9 and YUV12 formats. In the YUV12 format, line 2 of Cr/Cb data is discarded, and hence 4:2:2 vertical sub-sampling is achieved. In the YUV9 format, lines 2–4 of Cr/Cb data are discarded, and hence 4:1:1 vertical sub-sampling is achieved.

2.10.6 Byte Swapping

Before the data enters the FIFO it passes through a 4-way MUX to allow swapping of the bytes to support Macintosh (big endian) color data formats. The pixel DWORD PD[31:0] maps onto the FIFO input FI[31:0]. The byte-swap MUX remaps the data bytes, but byte lane 0 or bits[7:0] will still be considered the first byte of the scan line. See Table 2-6.

Table 2-6. Byte Swapping Map

Word Swap	**0**		**1**	
Byte Swap	**0**	**1**	**0**	**1**
FIFO Inputs	**Outputs of FIFO Data Formatter**			
FI[31:24]	PD[31:24]	PD[23:16]	PD[15:8]	PD[7:0]
FI[23:16]	PD[23:16]	PD[31:24]	PD[7:0]	PD[15:8]
FI[15:8]	PD[15:8]	PD[7:0]	PD[31:24]	PD[23:16]
FI[7:0]	PD[7:0]	PD[15:8]	PD[23:16]	PD[31:24]
NOTE(S): The byte swapping mode is disabled during VBI data.				

2.11 Video and Control Data FIFO

The FIFO block accepts data from the video data format conversion process, buffers the data in FIFO memory, then outputs DWORDs to the DMA Controller to be burst onto the PCI bus.

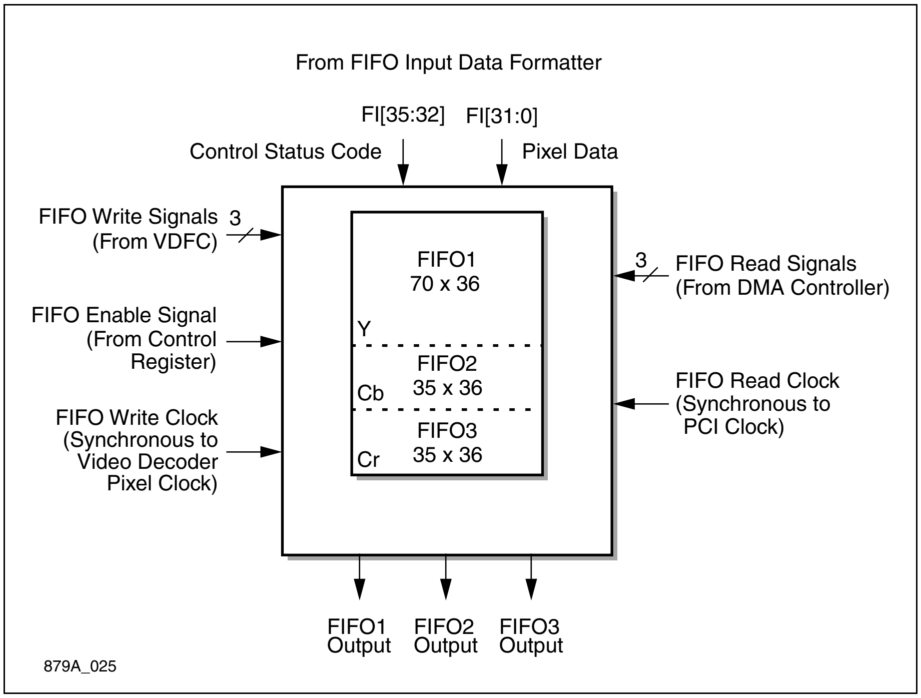
2.11.1 Logical Organization

The 630-byte data FIFO is logically organized into three segments:

1. FIFO1 = 70 words deep by 36 bits wide
2. FIFO2 = 35 × 36 bits
3. FIFO3 = 35 × 36 bits

Each of the 140 FIFO data words provide for one DWORD of pixel data and four bits of video control code status. This is illustrated in Figure 2-20. The FIFOs are large enough to support efficient size burst transfers (16 to 32 data phases) in planar as well as packed mode.

Figure 2-20. Data FIFO Block Diagram


From FIFO Input Data Formatter
FI[35:32]
FI[31:0]
Control Status Code
Pixel Data
FIFO Write Signals (From VDFC)
3
FIFO Enable Signal (From Control Register)
FIFO Write Clock (Synchronous to Video Decoder Pixel Clock)
FIFO1 70 x 36
Y
FIFO2 35 x 36
Cb
FIFO3 35 x 36
Cr
3
FIFO Read Signals (From DMA Controller)
FIFO Read Clock (Synchronous to PCI Clock)
FIFO1 Output
FIFO2 Output
FIFO3 Output
879A_025

2.11.2 FIFO Data Interface

Loading data into the FIFO can begin only when valid pixels are present during the even or the odd field. The pixel DWORD Pixel Data (PD) [31:0] is stored in FI[31:0], and the video control code STATUS[3:0] is stored in FI[35:32]. The VBI data will be included in the captured sequence if VBI capture capability is enabled.

Four bits of STATUS are used to encode information about the pixel data and the state of video timing unit (see Table 2-7). Video timing and control information, along with the data stream, passes through the FIFO. The FIFO buffer isolates the asynchronous video input and PCI output domains. Control of the input stream can occur only from the video timing unit of the video decoder and from the configured registers. The interaction and synchronization of the DMA controller and the RISC instruction sequence relies solely on the output side of the FIFO.

Table 2-7. Status Bits

Status[3:0]	Code	Description
0110	FM1	FIFO Mode: packed data to follow
1110	FM3	FIFO Mode: planar data to follow
0010	SOL	First active pixel/data DWORD of scan line
0001	EOL	Last active pixel/data DWORD of scan line, 4 valid bytes
1101	EOL	Last active pixel/data DWORD of scan line, 3 valid bytes
1001	EOL	Last active pixel/data DWORD of scan line, 2 valid bytes
0101	EOL	Last active pixel/data DWORD of scan line, 1 valid byte
0100	VRE	VRESET following an even field–falling edge of FIELD
1100	VRO	VRESET following an odd field–rising edge of FIELD
0000	PXV	Valid pixel/data DWORD

Capturing data to the FIFO always begins with a FIFO mode indicator code followed by pixel data. The FIFO mode indicator is stored in the FIFOs at the beginning of every capture-enabled field, when the data format is changed mid-field such as transitioning from packed VBI data to planar mode, and when video capture of a field is asynchronously enabled. The mode status codes are always stored in planar format. FIFO1 receives two copies of the status code, while FIFO2 and FIFO3 each receive one copy.

The SOL code is packed in the FIFO with the first valid pixel data byte, which is the first pixel DWORD for the scan line. The EOL code is packed in the FIFO with the last valid pixel data byte, which is the last DWORD location written to the FIFO for the scan line. The EOL code indicates 1–4 valid bytes. The VRE/VRO code is stored in the FIFO at the end of a capture-enabled field. The DMA controller activates the appropriate PCI byte-enable by the time a given DWORD arrives on the output side of the FIFO.

The DMA controller guarantees that the FIFO does not fill; therefore the VDFC has no responsibility for FIFO overruns. The DMA Controller will be able to resynchronize to data streams that are shorter or longer than expected.

Planar mode and packed mode data can be present in the FIFOs at the same time if a bus access latency persists across a FIELD transition, or if packed VBI data proceeds planar YCrCb data.

2.11.3 Physical Implementation

The three FIFO outputs are delivered in parallel so that the DMA controller can monitor the FIFOs and perform skipping (reading and discarding data), if necessary, on all three simultaneously.

Due to the latency in determining the number of DWORDs placed in each FIFO, a FIFO Full (FFULL) condition is indicated prior to the FIFO count reaching the maximum FIFO Size. The FIFO is considered FFULL when the FIFO Count (FCNT) value equals or exceeds the FFULL value. Table 2-8 indicates the FIFO size and FIFO Full/Almost Full counts in units of DWORDs.

Table 2-8. FIFO Full/Almost Full Counts

FIFO	Size	FFULL	FAFULL
FIFO1	70	68	64
FIFO2	35	34	32
FIFO3	35	34	32
Total	140	136	128

A read must occur on the same cycle as FFULL, otherwise data will overflow and will be overwritten. The maximum bus latencies for various video formats and modes are shown in Table 2-9.

In planar mode the three FIFOs operate concurrently and independently. In packed mode, however, the three FIFOs operate in a merged mode to provide the maximum size buffer. FSIZE1, 2, and 3 indicate the physical size of each FIFO. FSIZET represents the total buffer size when the FIFOs work together in packed mode.

2.11.4 FIFO Input/Output Rates

The input and output ports of the Fusion 878A's FIFO can operate simultaneously and are asynchronous to one another.

The maximum FIFO input rate is for consecutive writes of PAL video at 17.73 MHz. However, there are never consecutive-pixel-cycle writes to the same FIFO. The fastest FIFO write sequence is F1, F2, F1, F3. Therefore, the fastest write rate to any FIFO is less than or equal to half of the pixel rate.

The maximum FIFO output read rate is one FIFO word at the PCI clock rate (33 MHz). All three FIFOs can be read simultaneously. Some bus systems may be designed with PCI clocks slower than 33 MHz. The Fusion 878A data FIFO only supports systems where the maximum input data rate is less than the output data rate. It can support a input video clock (17.73 MHz) faster than the PCI clock (16 MHz) as long as the video data rate does not exceed the available PCI burst rate.

Table 2-9. Table of PCI Bus Access Latencies

Video Format	Resolution	Mode	Max Bus Latency Before FIFO Overflow (μs)
NTSC 30 fps	640 x 480	RGB32	10
		RGB24	13
		RGB16/YCrCb 4:2:2	20
		YCrCb 4:1:1	27
		Y8, 8-bit dithered, VBI	41
NTSC 30 fps	320 x 240	RGB32	20
		RGB24	27
		RGB16/YCrCb 4:2:2	41
		YCrCb 4:1:1	55
		Y8, 8-bit dithered, VBI	83
PAL/SECAM 25 fps	768 x 576	RGB32	8
		RGB24	11
		RGB16/YCrCb 4:2:2	17
		YCrCb 4:1:1	23
		Y8, 8-bit dithered, VBI	34
PAL/SECAM 25 fps	384 x 288	RGB32	17
		RGB24	23
		RGB16/YCrCb 4:2:2	34
		YCrCb 4:1:1	46
		Y8, 8-bit dithered, VBI	69

Effective Rate		M Pixels/Sec
NTSC	640 x 480	12.27
NTSC	320 x 240	6.14
NTSC	720 x 480	13.50
PAL	768 x 576	14.75
PAL	384 x 288	7.38

NOTE(S):

1. The above figures are based on a 33.33 MHz PCI bus.
2. Maximum bus latency before FIFO Overflow (μs) = FIFO FAFULL Limit (Effective Rate × Number of Bytes/Pixel)

2.12 DMA Controller

The Fusion 878A incorporates a unique DMA controller architecture that gives the capture system great flexibility in its ability to deliver data to memory. It is designed as a small RISC engine that runs on a set of instructions generated and maintained in host system memory by the Fusion 878A device driver software. The video and audio DMA controllers are identical except that the audio DMA controller does not support planar mode instructions.

In this architecture, the DMA can dynamically change target memory address from one video line to the next. This enables multiple memory targets to be established for various components of each video frame. For example, an NTSC video frame contains four discrete components which require separate target memory locations:

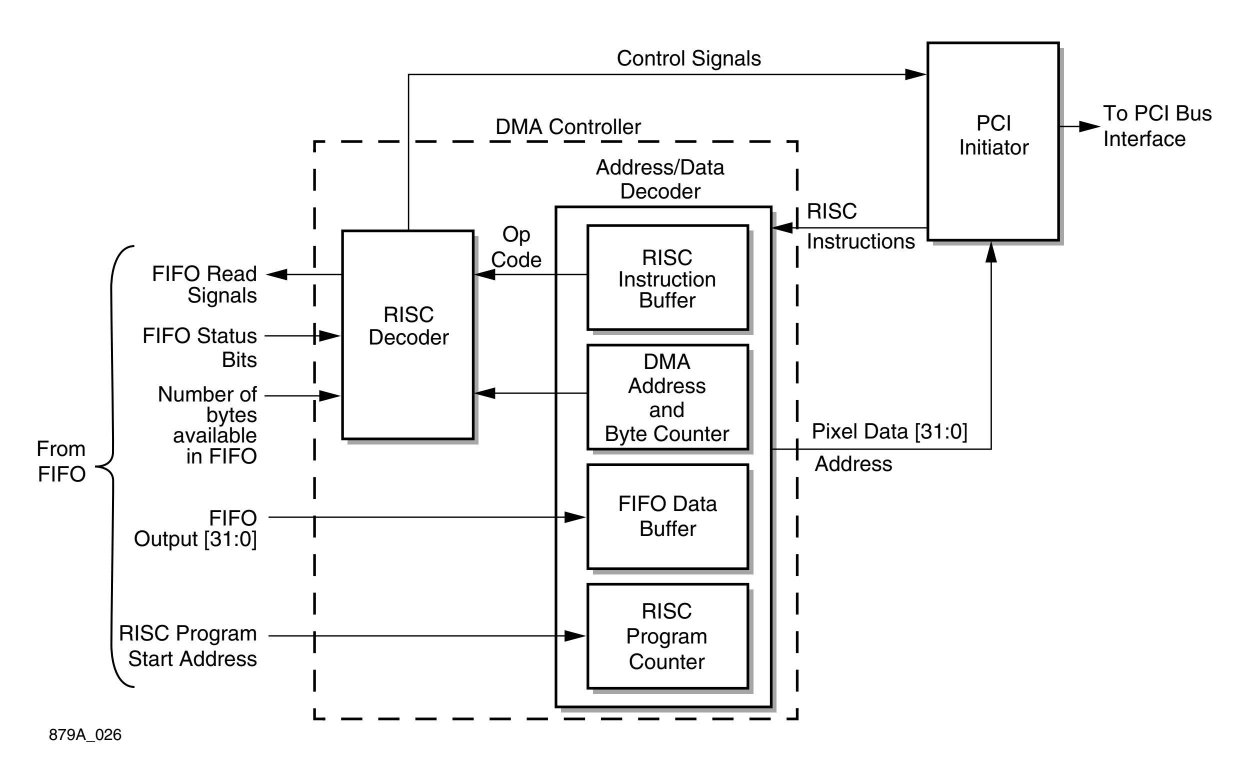
- Even-field video image data
- Odd-field video image data
- Line 21 closed captioning data
- Line 15 teletext data

The Fusion 878A DMA can concurrently support a display memory target for the even-field image and three separate system memory targets for the odd-field image, line 21 data, and line 15 data images respectively.

The Fusion 878A device driver software creates a RISC program which runs the DMA controller. The RISC program resides in host system memory. Through the use of the PCI target, the RISC program puts its own starting address in a Fusion 878A register and makes it available to the DMA controller. The DMA controller then requests the PCI initiator to fetch an instruction. The RISC instructions available are WRITE, SKIP, SYNC, and JUMP.

Decoded composite video data is stored in the Fusion 878A FIFO. The DMA controller then presents the data to the PCI initiator and requests that the data be output to the target memory. The PCI initiator outputs the pixel data on the PCI bus after gaining access to the PCI bus. It is the responsibility of the DMA controller to prevent and manage the overflow of the Fusion 878A FIFOs. This process is illustrated in Figure 2-21.

Figure 2-21. Audio/Video RISC Block Diagram



2.12.1 Target Memory

The Fusion 878A's FIFO DWORDs are perfectly aligned to the PCI bus: i.e., bit 0 of the FIFO DWORDs lines up with bit AD[0] on the PCI bus. Thus, video scan line data is aligned to target memory locations, and data path combinational logic between the FIFO and the PCI bus is not required.

The target memory for a given scan line of data is assumed to be linear, incrementing, and contiguous. For a 1024-pixel scan line, a maximum of 4 kB of contiguous physical memory is required. Each scan line can be stored anywhere in the 32-bit address space. A scan line can be broken into segments with each segment sent to a different target area. An image buffer can be allocated to line fragments anywhere in the physical memory, because the line sequence is arbitrary.

2.12.2 RISC Program Setup and Synchronization

There are two independent sets of RISC instructions in the host memory: one for the odd field and the other for the even field. The first field begins with a synchronization instruction (See SYNC in Table 2-10) indicating packed or planar data from the FIFO (STATUS[3:0] = FM1 or FM3). The first field ends with a SYNC instruction indicating an even or an odd field to follow (STATUS[3:0] = VRE or VRO). The second field begins with a SYNC instruction and ends with a SYNC instruction followed by a JUMP instruction back to the first field. The SYNC instructions allow the synchronization of the FIFO output and the RISC program start/end points.

The software will set up a pixel data flow by creating a RISC instruction sequence in the host memory for the odd and even fields. The DMA controller normally branches through the RISC instruction sequence via JUMP instructions. The RISC program sequence needs to be changed only when the parameters of the video capture/preview mode change. Otherwise, the DMA controller continuously cycles through the same program, which is set up once for control of an entire frame.

2.12.3 RISC Instructions

There are five types of packed mode RISC instructions—WRITE, WRITEC, SKIP, SYNC, and JUMP—that control the data stored in the FIFO. Three additional planar mode instructions exist, which replace the simple packed mode WRITE/SKIP instructions. Instruction details are listed in Table 2-10. The DMA controller switches from packed mode to planar mode or vice versa based on the status codes flowing through the FIFOs along with the pixel data.

***Table 2-10. RISC Instructions** (1 of 5)*

Instruction	Opcode	DWORDs	Description		
WRITE	0001	2	Write packed mode pixels to memory from the FIFO beginning at the specified target address.		
			DWORD0:		
			[11:0]	Byte count + Byte offset	
			[15:12]	Byte enables	
			[23:16]	Reset/Set RISC_STATUS	
			[24]	IRQ	
			[25]	Reserved	
			[26]	EOL	
			[27]	SOL	
			[31:28]	Opcode	
			DWORD1:[1]		
			[31:0]	32-bit target address	Byte address of first pixel byte.

NOTE(S):
[1] [1:0] is the Byte offset.

Table 2-10. RISC Instructions (2 of 5)

Instruction	Opcode	DWORDs	Description		
WRITE123	1001	5	Write pixels to memory in planar mode from the FIFOs beginning at the specified target addresses.		
			DWORD0:		
			[11:0]	Byte count #1	Byte transfer count from FIFO1
			[15:12]	Byte enables	
			[23:16]	Reset/Set RISC_STATUS	
			[24]	IRQ	
			[25]	Reserved	
			[26]	EOL	
			[27]	SOL	
			[31:28]	Opcode	
			DWORD1:		
			[11:0]	Byte count #2	Byte transfer count from FIFO2
			[27:16]	Byte count #3	Byte transfer count from FIFO3
			DWORD2:		
			[31:0]	32-bit target address	Byte address for Y data from FIFO1
			DWORD3:		
			[31:0]	32-bit target address	Byte address for Cb data from FIFO2
			DWORD4:		
			[31:0]	32-bit target address	Byte address for Cr data from FIFO3

Table 2-10. RISC Instructions (3 of 5)

Instruction	Opcode	DWORDs	Description		
WRITE1S23	1011	3	Write pixels to memory in planar mode from the FIFO1 beginning at the specified target addresses. Skip pixels from FIFO2 and FIFO3. This instruction is used to achieve the YUV9 and YUV12 color modes, where the chroma components are sub-sampled.		
			DWORD0:		
			[11:0]	Byte count #1	Byte transfer count from FIFO1
			[15:12]	Byte enables	
			[23:16]	Reset/Set RISC_STATUS	
			[24]	IRQ	
			[25]	Reserved	
			[26]	EOL	
			[27]	SOL	
			[31:28]	Opcode	
			DWORD1:		
			[11:0]	Byte count #2	Byte skip count from FIFO2
			[27:16]	Byte count #3	Byte skip count from FIFO3
			DWORD2:		
			[31:0]	32-bit target address	Byte address for Y data from FIFO1
WRITEC	0101	1	Write packed mode pixels to memory from the FIFO continuing from the current target address.		
			DWORD0:		
			[11:0]	Byte count	
			[15:12]	Byte enables	
			[23:16]	Reset/Set RISC_STATUS	
			[24]	IRQ	
			[25]	Reserved	
			[26]	EOL	
			[27]	SOL	Cannot be set
			[31:28]	Opcode	

***Table 2-10. RISC Instructions** (4 of 5)*

Instruction	Opcode	DWORDs	Description		
SKIP	0010	1	Skip pixels by discarding byte-count number of bytes from the FIFO. This may start and stop in the middle of a DWORD.		
			DWORD0:		
			[11:0]	Byte Count	
			[13:12]	Byte Offset	
			[15:14]	Reserved	
			[23:16]	Reset/Set RISC_STATUS	
			[24]	IRQ	
			[25]	Reserved	
			[26]	EOL	
			[27]	SOL	
			[31:28]	Opcode	
SKIP123	1010	2	Skip pixels in planar mode by discarding byte count #1 of bytes from the FIFO1 and byte count #2 from FIFO2 and FIFO3. This may start and stop in the middle of a DWORD.		
			DWORD0:		
			[11:0]	Byte Count #1	
			[15:12]	Reserved	
			[23:16]	Reset/Set RISC_STATUS	
			[24]	IRQ	
			[25]	Reserved	
			[26]	EOL	
			[27]	SOL	
			[31:28]	Opcode	
			DWORD1:		
			[11:0]	Byte count #2	
			[27:16]	Byte count #3	

Table 2-10. RISC Instructions *(5 of 5)*

Instruction	Opcode	DWORDs	Description		
JUMP	0111	2	Jump the RISC program counter to the jump address. This allows unconditional branching of the sequencer program.		
			DWORD0:		
			[15:0]	Reserved	
			[23:16]	Reset/Set RISC_STATUS	
			[24]	IRQ	
			[27:25]	Reserved	
			[31:28]	Opcode	
			DWORD1:		
			[31:0]	Jump address	DWORD-aligned
SYNC	1000	2	Synchronize all data in FIFO until the RISC instruction status bits equal the FIFO status bits.		
			DWORD0:		
			[3:0]	Status	
			[14:4]	Reserved	
			[15]	RESYNC	A value of 1 disables FDSR errors
			[23:16]	Reset/Set RISC_STATUS	
			[24]	IRQ	
			[27:25]	Reserved	
			[31:28]	Opcode	
			DWORD1:		
			[31:0]	Reserved	

Each RISC instruction consists of 1 to 5 DWORDs. The 32-bits in the DWORDs relay information such as the opcode, target address, status codes, synchronization codes, byte count/enables, and start/end of line codes.

The SOL bit in the WRITE and SKIP instructions indicates that this particular instruction is the first instruction of the scan line. The EOL bit in the WRITE and SKIP instructions indicates that this particular instruction is the last instruction of the scan line. An EOL flag from the FIFO and the last DWORD for the scan line coincide with finishing the last instruction of the scan line. If the FIFO EOL condition occurs early, the current instruction and all instructions leading up to the one that contains the EOL flag will be aborted. If there is only one instruction to process the line, both SOL and EOL bits will be set.

WRITE, WRITEC, and SKIP control the processing of active pixel data stored in the FIFO. These three instructions alone control the sequence of *packed mode* data written to target memory on a byte resolution basis. The WRITEC instruction does not supply a target address. Instead, it relies on continuing from the current DMA pointer contained in the target address counter. This value is updated and kept current even during SKIP mode or FIFO overruns. However, WRITEC cannot be used to begin a new line; i.e., this instruction cannot have the SOL bit set.

WRITE123, WRITE1S23, and SKIP123 control the processing of active pixel data stored in the FIFOs. These three instructions alone control the sequence of *planar mode* data written to target memory on a byte resolution basis. The WRITE1S23 instruction supports further decimation of chroma on a line basis. For each of these instructions, the same number of bytes will be processed from FIFO2 and FIFO3.

The JUMP instruction is useful for repeating the same even/odd program for every frame, or for switching to a new program when the sequence needs to be changed without interrupting the pixel flow.

The SYNC instruction is used to synchronize the RISC program and the pixel data stream. The DMA controller achieves this by using the status bits in DWORD0 of the SYNC instruction and matching them to the four FIFO status bits provided along with the pixel data. Once the DMA controller has matched the status bits between the FIFO and the RISC instruction, it proceeds with outputting data. Prior to establishing synchronization, the DMA controller reads and discards the FIFO data.

Opcodes 0000 and 1111 are reserved to detect instruction errors. If these opcodes or the other unused opcodes are detected, an interrupt will be set. The DMA controller will stop processing until the RISC program is re-enabled. This also applies to SYNC instructions specifying unused or reserved status codes. Detecting RISC instruction errors is useful for detecting software errors in programming, or ensuring that the DMA controller is following a valid RISC sequence. In other words, it ensures that the program counter is not pointing to the wrong location.

All unused/reserved bits in the instruction DWORDs must be set to 0.

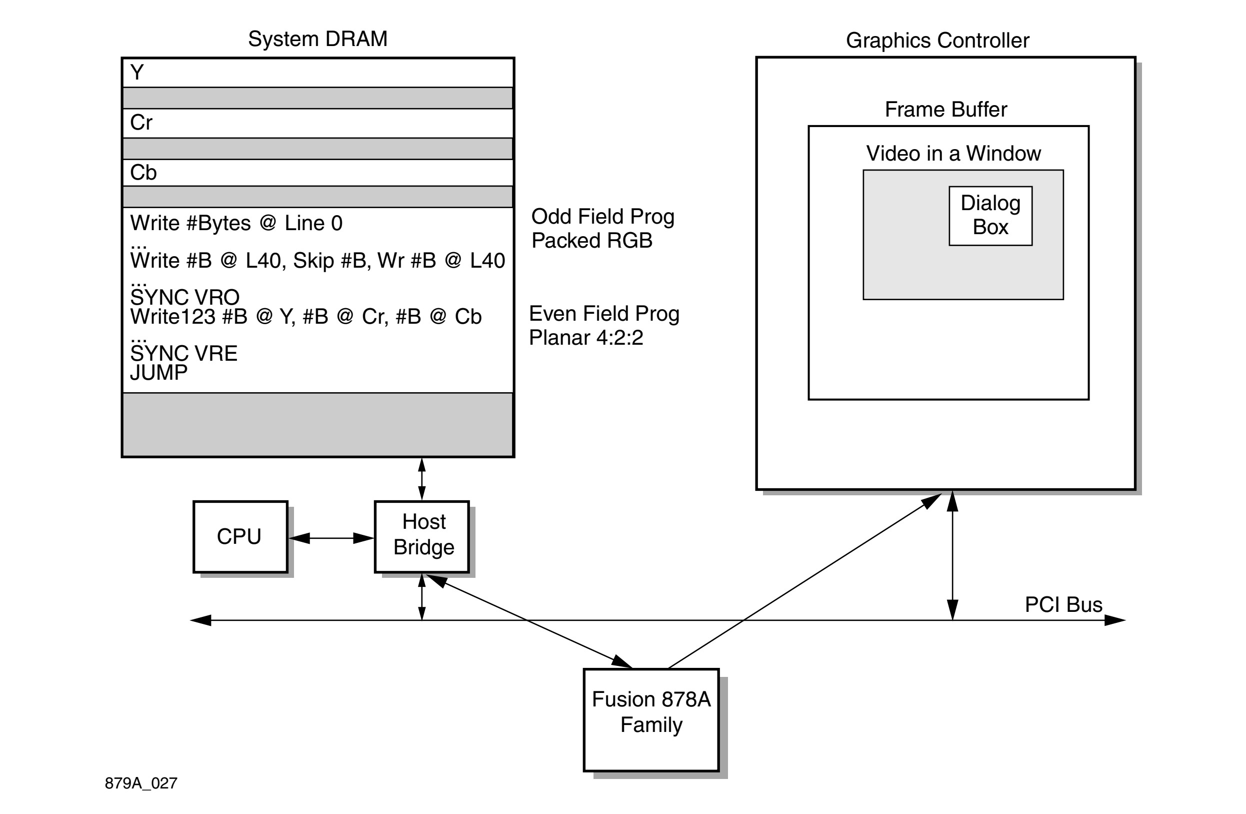
2.12.4 Complex Clipping

When writing video data directly into on-screen display memory, it is necessary to be able to clip the video image before it is put onto the PCI bus. The Fusion 878A supports complex clipping of the video image for those applications which require the displayed video picture to be occluded by graphics objects such as a pull-down menu, an overlaying graphics window, etc. Typically, a target graphics frame buffer controller cannot provide overlay control for the video pixel data stream when it is provided by a PCI bus master peripheral to the graphics PCI host interface.

The Fusion 878A implements clipping by blocking the video image as it is being put onto the PCI bus in the areas where graphics are to be displayed, that is, where graphics objects are “overlaying” the video image. The Fusion 878A cuts out portions of the video image so that it can “inlay” or fit around the displayed graphics objects

A clip list is provided through the graphics system DirectDRAW Interface^{TM} provider to the Fusion 878A device driver software. This indicates the areas of the display where the video image is to be occluded. The Fusion 878A driver software interprets the clip list and generates a RISC program that blocks writing video pixels that are to be occluded, as illustrated in Figure 2-22.

Figure 2-22. Example of Complex Clipping



2.12.5 Executing Instructions

Once the DMA controller has achieved synchronization between the FIFO and the RISC program, it starts executing the RISC instructions. The data in the FIFO will be aligned with the data bytes expected by the RISC instructions. The DMA controller reads RISC instructions and performs burst writes from the FIFO.

The DMA controller can be programmed to wait for 4, 8, 16, or 32 DWORDs in the FIFO before executing a WRITE instruction. Setting this FIFO trigger point optimizes the bus efficiency by not allowing the DMA controller to access the bus every time a DWORD enters the FIFO. However, the FIFO trigger point is ignored when the DMA controller is near the end of an instruction and the number of DWORDs left to transfer is less than the number of DWORDS in the FIFO. By allowing the instruction to complete, even if the FIFO is below its trigger point, the RISC instructions can be flushed sooner for every scan line. Otherwise, the DMA controller may have to wait for many scan lines before the required number of DWORDs are present in the FIFO, especially when capturing highly scaled down images. There may be several horizontal lines before another DWORD enters the FIFO.

The FIFO trigger point is ignored by the DMA controller during all SKIP instructions. In the planar mode, the trigger points for the FIFOs should be set to the same level, even though the luma data is being stored in the Y FIFO at least twice as fast the chroma data is being stored in the Cr and Cb FIFOs. This ensures that the Y FIFO will be selected first to burst data onto the PCI bus.

When the initiator is disconnected from the PCI bus while in the planar mode, it is essential to regain control of the bus as soon as possible and to deliver any queued DWORDs. The DMA controller will ignore the FIFO trigger point because it needs to empty the FIFO immediately. Otherwise it may not have a chance to empty the rest of the FIFOs before it has to relinquish the bus. This is not a concern in the packed mode because all three FIFOs are treated as one large FIFO.

When the PCI target detects a parity error while the PCI initiator is reading the instruction data, the DMA controller immediately stops burst data writes and RISC instruction reads. This condition also causes an interrupt.

2.12.6 FIFO Overrun Conditions

There are cases where the Fusion 878A PCI initiator cannot gain control of the PCI bus, and the DMA controller is not able to execute the necessary WRITE instructions. Instead of writing data to the bus, the DMA controller reads data out of the FIFO and discards the data. To the FIFO, it appears as if the DMA controller is outputting to the bus. This allows the FIFO overruns to be handled gracefully, with minimal loss of data. The Fusion 878A is not required to abort a whole scan during FIFO overruns. The DMA controller keeps track of the data to the nearest byte, and is able to deliver the rest of the scan line in case the FIFO overrun condition is cleared.

The Fusion 878A DMA controller normally monitors the FIFO Full (FFULL) counters to determine how full the FIFOs are. However, before the DMA controller begins a burst write operation to process a WRITE instruction, it is desirable to have some headroom in the FIFO allowing for more data to enter while the PCI initiator is waiting for the target to respond. Hence, the Fusion 878A monitors the FIFO Almost Full (FAFULL) counters. The difference between FFULL and FAFULL provides the necessary headroom to handle target latency.

Before the DMA controller executes the address phase of a PCI write transaction to process a WRITE instruction, the FIFO count value must be below the FAFULL level. At all other times, the FIFOs must be maintained below the FFULL level. The FIFO counters for all three FIFOs are monitored for full/almost full conditions in both planar and packed modes.

Once the DMA controller begins the PCI bus transaction, it has committed to a target DMA start address. If the FIFO overflows while it is waiting for the target to respond, the initiator must terminate the transaction just after the target responds. This is because the DMA controller has to start discarding the FIFO data, since the target pointer and the data are out of sync. This terminating condition will be communicated to the Fusion 878A device driver by setting an interrupt bit that indicates interfacing to unreasonably slow targets (FBUS).

If an instruction is exhausted while the FIFO is in an overrun condition, the Fusion 878A DMA controller will continue discarding the FIFO data during the next pre-fetched instruction as well. If the DMA controller runs out of RISC instructions and the FIFO continues to fill up, then PCI bus access is still denied. The DMA controller continues discarding FIFO data for the remainder of that scan line. Once the Fusion 878A DMA controller detects the EOL control bits from the FIFO, it will attempt to gain access to the PCI bus and resynchronize itself with the RISC instruction EOL status bits. However, if the DMA controller is not successful in getting control of the bus, it will keep track of the number of scan lines discarded out of the FIFO and will resynchronize itself with the RISC program based on the number of EOL control signals detected.

The planar mode requires that the DMA controller give priority to the Y FIFO to be emptied first. If there is a very long latency in getting access to the PCI bus, all three FIFOs will be almost full when the bus is finally granted. While bursting the Y data, the CrCb data is likely to overflow. Attempting to deliver data from each FIFO to the bus will yield poor bus performance. Preference is given to the Y FIFO to finish the burst write operation, and if Cr or Cb FIFOs each reach a full condition, the DMA controller will discard their data in parallel to delivering the Y data.

2.12.7 FIFO Data Stream Resynchronization

The Fusion 878A DMA controller is constantly monitoring whether there is a mismatch between the amount of data expected by the RISC instruction and the amount of data being provided by the FIFO. The DMA controller then corrects for the mismatches and realigns the RISC program and the FIFO data stream.

For example, if the FIFO contains a shorter video line than expected by the RISC instruction, the DMA controller detects the EOL control code from the FIFO earlier than expected. The DMA controller then aborts the rest of the RISC instructions until it detects the EOL control code from the RISC program.

If the FIFO contains a longer video line than expected by the RISC instruction, the DMA controller will not detect the EOL control code from the FIFO at the expected time. The DMA controller will continue reading the FIFO data; however it will discard the additional FIFO data until it reaches the EOL control code from the FIFO.

Similarly, if the FIFO provides a smaller number of scan lines per field than expected by the RISC program, the end of field control codes from the FIFO (VRE/VRO) will arrive early. The DMA controller then aborts all RISC instructions until the SYNC status codes from the RISC instruction match the end of field status codes from the FIFO.

If the FIFO provides a larger number of scan lines per field than expected by the RISC program, the end of field control codes from the FIFO (VRE/VRO) will not arrive at the expected time. Again, the FIFO data is read by the DMA controller and discarded until the SYNC status codes from the RISC instruction match the end of field status codes from the FIFO.

The DMA controller manages all of the above error conditions, but the FIFO Data Stream Resynchronization (FDSR) interrupt bit will be set as well.

2.13 Byte Alignment

The video function DMA controllers and PCI initiators are enhanced for byte resolution on target addresses in packed color modes. The FIFO DWORD-aligned data is realigned with the correct byte lanes according to the target address.

Byte alignment in the Fusion 878A, which applies only to packed modes, disables the PCI byte and enables C/BE# during the initial part of a line transfer. Since the disabled bytes are transferred but not written, they must still be included in the total byte count. For example, if a non-DWORD aligned target address begins the line with an offset of 3, then the first byte (byte 0) from the FIFO is shifted to byte lane 3 and transferred in the first PCI DWORD data with byte lanes 0–2 disabled. The remaining FIFO bytes (bytes 1–3) are combined with the following FIFO byte (byte 4) to form the next DWORD transfer. Again, since the RISC instruction’s byte count represents the number of bytes transferred, not the number written, the byte count must be increased by 3 in order to account for the 3 disabled bytes that were transferred in the first DWORD.

Table 2-11. Write 640 Pixels in RGB8 Mode

RISC Instruction	Byte Count	Target Address	Pixel/Byte Offset
WRITE	640	F0040004	0
WRITE	641	F0040005	1
WRITE	642	F0040006	2
WRITE	643	F0040007	3

The target address used is a byte lane offset (relative address), as opposed to an absolute byte address. So if multiple WRITE instructions are used per video line, each would have the same byte offset no matter which byte lane SKIP starts or stops at. Formerly reserved bits [13:12] of the SKIP instruction must contain the byte offset (two LSB’s of the target address) if they are using byte aligned addresses.

Byte alignment applies only to video packed mode, and only one byte alignment may occur per line. A video line may not be transferred to two segments with byte alignments.

One notable case arises when combining a SKIP and a WRITE with a byte alignment offset. This may produce a PCI bus WRITE transaction with no byte enables active. For example, if the first two bytes are skipped combined with a WRITE and an address offset of 3, the first PCI data phase will have no byte enables active. The bus master will not prevent the null data transaction because the DMA will not advance the address. The reason for this is the SKIP consumes only two bytes, and the address gets advanced only if the entire DWORD is consumed by going to the bus. The second data phase then consists of 3 bytes with byte lane 0 disabled.

2.14 Multifunction Arbiter

An internal arbiter is necessary to determine whether the video or audio DMA controller claims the PCI bus when a $\overline{\text{GNT}}$ is issued to the Fusion 878A. Only one of the two functions may actually see the $\overline{\text{GNT}}$ active during any one PCI clock cycle. This also ensures that only one function can park on the bus. The following rules outline the arbitration algorithm. Internal signals $\overline{\text{REQ}}$[0:1] and $\overline{\text{GNT}}$[0:1] are for the video Function 0 and the audio Function 1 respectively.

2.14.1 Normal PCI Mode

The PCI $\overline{\text{REQ}}$ signal is the logical OR of the incoming function requests. The internal $\overline{\text{GNT}}$[0:1] signals are gated asynchronously with $\overline{\text{GNT}}$ and demultiplexed by the audio request signal. Thus the arbiter defaults to the video function at power-up and parks there during no requests for bus access. This is desirable since the video will request the bus more often. However, the audio will have highest bus access priority. Thus, the audio will have first access to the bus even when issuing a request after the video request but before the PCI external arbiter has granted access to the Fusion 878A. Neither function can preempt the other once on the bus. Emptying the entire video PCI FIFO onto the PCI bus is of very short duration compared to the bus access latency that the audio PCI FIFO can tolerate.

2.14.2 430FX Compatibility Mode

When using the 430FX PCI, the following rules will ensure compatibility:

1. De assert $\overline{\text{REQ}}$ at the same time as asserting $\overline{\text{FRAME}}$.
2. Do not reassert $\overline{\text{REQ}}$ to request another bus transaction until after finishing the previous transaction.

Since individual bus masters do not have direct control of $\overline{\text{REQ}}$, a simple logical OR of video and audio requests would violate the rules. Thus, both the arbiter and the initiator contain 430FX compatibility mode logic. To enable 430FX mode, set the EN_TBFX bit as indicated in *0x40—Device Control Register*.

When EN_TBFX is enabled, the arbiter ensures that the two compatibility rules are satisfied. Before $\overline{\text{GNT}}$ is asserted by the PCI arbiter, this internal arbiter may still logical OR the two requests. However, once the $\overline{\text{GNT}}$ is issued, this arbiter must lock in its decision and now route only the granted request to the $\overline{\text{REQ}}$ pin. The arbiter decision lock happens regardless of the state of $\overline{\text{FRAME}}$ because it does not know when $\overline{\text{FRAME}}$ will be asserted. (Typically, each initiator will assert $\overline{\text{FRAME}}$ on the cycle following $\overline{\text{GNT}}$.)

When $\overline{\text{FRAME}}$ is asserted, the initiator's responsibility is to remove its request at the same time. The arbiter's responsibility is to allow this request to flow through to $\overline{\text{REQ}}$ and not allow the other request to hold $\overline{\text{REQ}}$ asserted. The decision lock may be removed at the end of the transaction: for example, when the bus is idle ($\overline{\text{FRAME}}$ and $\overline{\text{IRDY}}$). The arbiter decision may then continue asynchronously until $\overline{\text{GNT}}$ is again asserted.

2.14.3 Interfacing with Non-PCI 2.1 Compliant Core Logic

A small percentage of core logic devices may start a bus transaction during the same cycle that $\overline{\text{GNT}}$ is de-asserted. This is non PCI 2.1 compliant. To ensure compatibility when using PCs with these PCI controllers, the EN_VSFX bit must be enabled (refer to *0x40—Device Control Register*). When in this mode, the arbiter does not pass $\overline{\text{GNT}}$ to the internal functions unless $\overline{\text{REQ}}$ is asserted. This prevents a bus transaction from starting the same cycle when $\overline{\text{GNT}}$ is de asserted. This also has the side effect of not being able to take advantage of bus parking, thus lowering arbitration performance. The Fusion 878A drivers must query for these non-compliant devices, and set the EN_VSFX bit only if required.

2.15 Audio A/D

2.15.1 Muxing and Anti-aliasing Filtering

Before entering the audio A/D, the TV, FM, and microphone/line audio inputs are selected by A_SEL and multiplexed. The MUX selects are break-before-make. If A_SEL is set to 3, no mux is enabled. Thus the SMXC pin can be used as a direct connect to the pre-amp (bypass MUX) if only one analog input is required. Refer to *0x10C—Audio Control Register (GPIO_DMA_CTL)* in Chapter 6.0 for register information.

The SMXC pad leads directly to the single-ended differential converter. The resistive load seen by the audio inputs is approximately 20 kΩ.

2.15.2 Input Gain Control

The audio frequency (AF) output level from the TV tuners ranges from 250 mV_{RMS} to 750 mV_{RMS}, typically riding on a 2 VDC offset. If the A/D nominal operating point is 0.5 V_{RMS} (1.414 V_{p-p}), then the input gain needs to vary from –3.5 dB to +6.0 dB.

The input signal is gained in discrete linear steps via A_GAIN[3:0]. Table 2-12 shows the calculated gain values. The A_GAIN value is set in *0x10C—Audio Control Register (GPIO_DMA_CTL)* in Chapter 6.0.

Table 2-12. Gain Control *(1 of 2)*

A_GAIN	Input GAIN	dB	Nominal Input V_{rms}	V_{p-p}
0	0.500	–6.02	1.000	2.828
1	0.667	–3.52	0.750	2.121
2	0.833	–1.58	0.600	1.697
3	1.000	0.00	0.500	1.414
4	1.167	1.34	0.429	1.212
5	1.333	2.50	0.375	1.061
6	1.500	3.52	0.333	0.943
7	1.667	4.44	0.300	0.849
8	1.833	5.26	0.273	0.771
9	2.000	6.02	0.250	0.707
10	2.167	6.72	0.231	0.653
11	2.333	7.36	0.214	0.606
12	2.500	7.96	0.200	0.566

Table 2-12. Gain Control (2 of 2)

A_GAIN	Input GAIN	dB	Nominal Input V_{rms}	V_{p-p}
13	2.667	8.52	0.188	0.530
14	2.833	9.05	0.176	0.499
15	3.000	9.54	0.167	0.471

In addition to the switched capacitor gain control, there is a +6 dB switch in the pre-amp. This additional amplification is enabled if A_G2X is set high. Thus, when A_GAIN equals 3 and A_G2X equals 1, the maximum signal input would be 0.25 V_{RMS}. The 6 dB boost is useful for very small input signals.

2.16 High Speed Serial Interface Mode

The same interface used for digital audio may be used for other types of digital serial data. With default settings, the maximum data rate into the serial interface is 16.6 MHz, due to PCI clock resampling of the ASCLK. Changing the DA_APP bit to 1 and the DA_IOM bits to 01 allows direct ASCLK sampling and increases the maximum speed of the interface to 40 Mbps. The DA_SBR bit must also be set to 1 for proper transfer to serial byte packets.

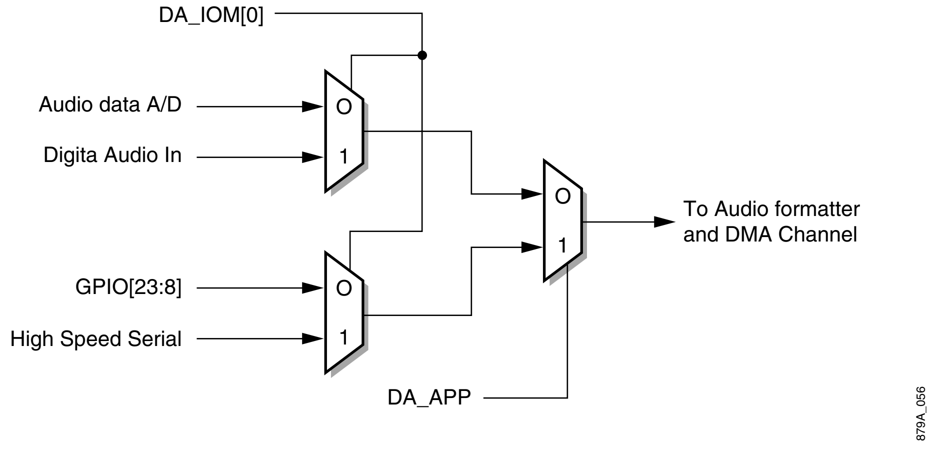
The ADATA input is clocked into an 8-bit shift register. The basic timing relationship between the ASCLK and ADATA pins is identical to the timing in Digital Audio input mode (refer to Figure 3-3). The DA_SCE bit determines whether the data is clocked in on the rising edge or the falling edge of ASCLK. When DA_SCE is low (default) data is clocked in on the rising edge. If falling-edge clocking is desired, DA_SCE must be changed to 1. The DA_MLB bit determines the bit order. When DA_MLB is low (default), the "MSB first" format is used. If DA_MLB is high, the "LSB first" format is used.

There are two ways of getting the registered data into the audio path for packetization. If the DA_DPM bit is low, the ALRCK signal must transition every eighth bit to signal the input byte boundaries. (Both rising and falling edges of ALRCK are used to clock bytes.) Alternatively, if DA_DPM is high, a 4-bit counter is provided to eliminate the need for a continuos ALRCK. In this case, it is recommended that ALRCK still be used to synchronized the counter, but on a less frequent basis.

2.17 Asynchronous Data Parallel Mode: Raw Data Capture

The asynchronous data parallel port interface allows the user to multiplex raw data from the GPIO port into the audio packetizer. Normally, the audio processor selects the 16-bit digitized analog data from the audio A/D and from the 16-bit digital audio input data. By setting the DA_APP bit in Bit 5 of the Audio Control Register (0x10C), the user may configure the part to disregard the 16-bit digital audio data, and use either the information on GPIO [23:8] or high speed serial mode input from the I^2S data port, as illustrated in Figure 2-23.

Figure 2-23. Asynchronous Data Parallel Input Multiplexer Block



In Asynchronous Data Parallel mode, the DA_APP bit switches the functionality of the ALRCK pin. When DA_APP is high, use ALRCK to clock in the data on GPIO [23:8]. This interface is dubbed *asynchronous*, because the clock is not required to be continuous or fixed-rate. From the point where it is multiplexed into the Digital Audio Packetizer, the GPIO data is treated the same as normal audio data. From the Packetizer, data goes into a 35 × 36 FIFO, and from the FIFO, to the PCI initiator. This mode supports input frequencies of up to 20 MBps.

This data rate is achieved by inputting 16-bit data at a frequency of 10 MHz. Both rising and falling clock edges are used to clock in data. Thus, the maximum allowable clock frequency on the ALRCK pin is 5 MHz. When DA_SBR is set, only data from GPIO[15:8] will be used.

2.18 Digital Audio Packetizer

The Digital Audio Packetizer (DAP) block can packetize data input on ASCLK, ALRCK, and ADATA in two additional modes besides normal I^2S mode. It can also packetize asynchronous parallel data from the GPIO pins (Asychronous Data Parallel Port). This mode is described in the Electrical Interfaces Asychronous Data Parallel mode section. Table 2-13 displays the DAP programming map.

Table 2-13. Digital Audio Packetizer Programming Map

Audio Control Registers	I^2S Mode	Asynchronous Data Parallel Port	Data Packet Mode	High Speed Serial Interface[1]
DA_APP	0	1	0	1
DA_IOM[0]	1	0	1	1
DA_DPM	0	0	1	See Section 2.16

NOTE(S):
[1] Set DA_SBR to 1 for High Speed Serial Interface Mode.

2.18.1 Audio FIFO Memory and Status Codes

The audio FIFO is identical to the video 36 × 35 FIFO memory block. The 36 bits allow for two 16-bit samples (or four 8-bit samples) and a 4-bit status nibble. The planar mode FM3 code and the VRE code are not generated from the audio packetizer. The SOL/EOL (1-4) codes bound the finite size audio packets (number of bytes indicated by ALP_LEN). The size of the data byte buffers may typically be set to the system memory page sizes. The FM1 and VRO codes bound a finite number of packets. These delimiter codes are useful for providing data delivery checks, RISC program loop checks, and synchronization. The PXV code is used for all valid audio samples between the packetizing codes SOL/EOL.

Both the input and output sides of the FIFO run off the PCI clock.

2.18.2 PCI Bus Latency Tolerance for Audio Buffer

The latency-effective size of the audio FIFO is essentially 32 DWORDs or 64 samples of 16-bit audio. This allows for a maximum PCI bus latency of 286 µs at 224 kHz (381 µs at 149 kHz) sample rate before overflow will occur. This latency drops to 143 µs when in 8-bit mode, because the rate is 4X and the number of bits is half. The digital audio input tolerates a maximum latency of 667 µs at 48 kHz 16-bit L,R or 122 µs at 1 MBps data before FIFO overflow.

2.18.3 FIFO Interface

The audio FIFO de couples the high-speed PCI interface from the slow audio data packetizer. The size chosen provides for efficient PCI bursts and effective PCI bus latency tolerance:

FSIZE = 35　　FFULL = 34　　FAFULL = 32

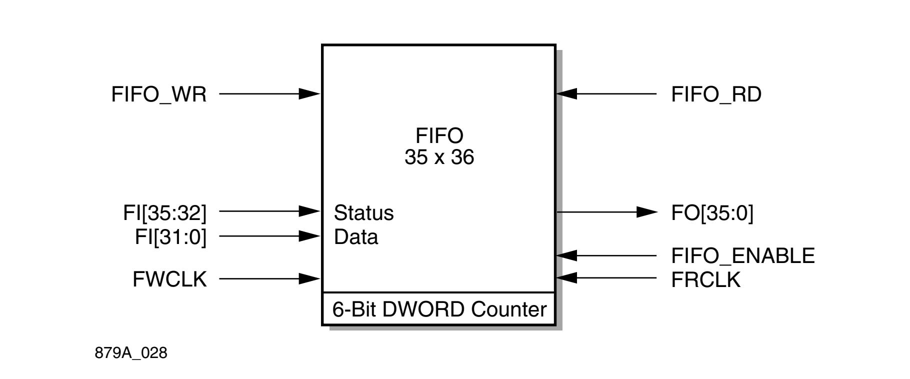
FIFO_WR must not be active for two consecutive FWCLK cycles. Thus, each word write must be followed by at least one dead cycle. FIFO_WR write data rate must also be less than the FRCLK rate. Since FWCLK = FRCLK = PCI-CLK for this instance, the write rate is not an issue.

The 6-bit DWORD counter indicates the number of DWORDs stored in the FIFO. It is cleared when FIFO_ENABLE is reset to 0. Otherwise, FIFO_WR –> cntr++, and FIFO_RD –> cntr--. This counter is part of the DAP block.

The 6-bit DWORD counter will be available for monitoring on GPIO[13:8] during debug mode (similar to the video DWORD counter monitor on GPIO[7:0]).

Figure 2-24 illustrates the FIFO interface.

Figure 2-24. FIFO Interface



2.18.4 Audio Packets and Data Capture

Audio samples are grouped into a line packet of length ALP_LEN bytes. The audio line packets are grouped to form an audio field packet of length AFP_LEN audio lines. Thus, the number of data bytes in an audio field is ALP_LEN × AFP_LEN. The line and field concept applied to audio only serves to delimit the real-time continuous data stream, into packets, that can be monitored for error conditions. The FIFO status and data flow is below.

```
FIFO Status                     FIFO Data

begin Audio Field
    FM1                         Don't Care
    begin Audio Line                              //repeat (AFP_LEN)
            SOL                 audio DWORD
            PXV                 audio DWORD       //repeat (AFP_LEN)
            EOL(1–4)            audio DWORD or sub-DWORD
    end Audio Line
    VRO                         Don't Care
end Audio Field
```

When ACAP_EN is set high, the audio capture sequence begins. The first 36-bit word written to the FIFO contains the FM1 packet-mode status code (DWORD data portion = Don't Care). The next word written contains 1 DWORD of audio samples and the SOL status code. Then ALP_LEN/4–2 words are written with the PXV status code and one audio data DWORD, followed by one more word of one audio data DWORD and the EOL status code. Each line of audio data always begins DWORD aligned. Since ALP_LEN has byte resolution, the last audio data DWORD of the line may contain less than 4 valid bytes as indicated by the proper EOL(1-4) code. This data is right-justified. The next line starts DWORD aligned again.

Regardless of where the audio is sourced (A/D, Digital Audio, or Packet Data), ALP_LEN always controls the proper usage of EOL codes. Thus in the case of A/D interface where data is presented as 16-bit words, an odd number of bytes used for ALP_LEN would cause one byte to be lost since this byte would not be carried into the next line. Similarly for the digital audio interface, which consists of L,R word pairs, an ALP_LEN not a multiple of four would cause data to be lost. So it is recommended that ALP_LEN be used with byte resolution for Data Packet mode, word resolution for A/D mode, and DWORD resolution for Digital Audio mode.

The audio data samples from the DDF are presented to the DAP as 16-bit words or 8-bit bytes as determined by DA_SBR. The DAP packs words or bytes together into DWORDs for writing into the FIFO. Usually, two words are packed together (little-endian format) into a DWORD to be written into the audio FIFO. If ALP_LENmod4 equals 2, then the last word of the line for the FIFO will contain only 2 valid bytes (EOL2). The next 16-bit audio sample will begin the next line (right-justified, DWORD aligned). Similarly, L,R digital audio word pairs are packed together (always a DWORD) and written to a common FIFO location. Data bytes from the packet mode interface are, collected into DWORDs also, except for the last DWORD of the line which may have fewer than four valid bytes. The data following one line of length ALP_LEN will begin the next line (no data lost).

The ALP_LEN sequence is repeated AFP_LEN times. The last 36-bit word written to the FIFO contains the VRO end-of-audio-field status code (DWORD data portion = don't care). This whole field sequence repeats until ACAP_EN is reset low. The end of data capture will be synchronized with the VRO code DWORD. FIFO_ENABLE should be set high during audio capture to enable the FIFO. If FIFO_ENABLE is reset, capture is immediately (asynchronously) stopped, and the capture state machine begins its sequence from the start of the next frame (FM1...).

2.18.5 Digital Audio Input

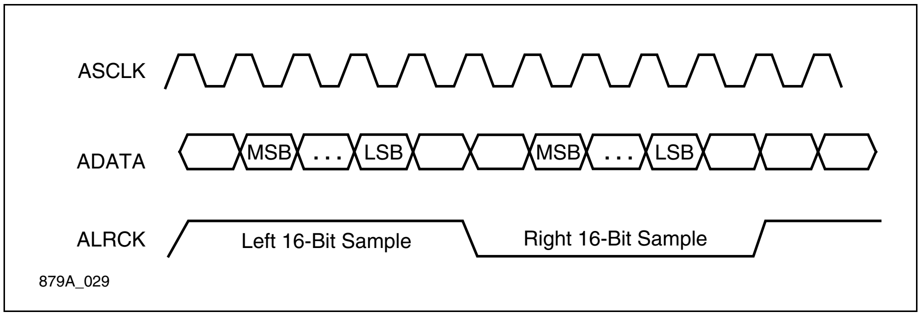
The digital audio interface consists of three input pins: ADATA, ALRCK, and ASCLK. This three-wire interface can be used to capture 16-bit I^{2}S style digital audio (DA_DPM = 0) or more generic non-continuous packet synchronized data bytes (DA_DPM = 1). The PCI clock will be used to re-sample the asynchronous clock ASCLK, since it is at a much higher rate. The ALRCK and ADATA signals are sampled with respect to this re-synchronized clock. Refer to the *0x10C—Audio Control Register (GPIO_DMA_CTL)*.

2.18.5.1 Digital Audio Input Mode

The digital audio is a serial bit stream where the highest ASCLK allowed is 64 x 48 kHz = 3.072 MHz. ADATA must supply at least 16 bits per left and 16 bits per right audio sample. The framing ALRCK clock is a square wave usually aligned with the start of each sample.

The universal interface can be configured by several register values. The bit DA_SCE (0 = rising, 1 = falling) chooses the edge of ASCLK used to sample the bit stream on ADATA. The bit DA_LRI (0 = left, 1 = right) is used to determine the left/right sample synchronized with the rising edge of ALRCK. It is assumed that the left sample will lead and be paired with the following right sample. Thus DA_LRI can be used to indicate which ALRCK edge points to start of the sample coincident pair. (If a particular format is R then L oriented, then this will reverse the order of data presented to memory, i.e., the right sample will be at the lower address.) The 5-bit value DA_LRD is used to delay from each ALRCK edge, DA_LRD ASCLKs before transferring the left or right shift-register data to a parallel register. The value DA_LRD indicates the number of ASCLKs following the edge of ALRCK where the first bit of the 16-bit data (regardless of serial transfer order) can be found. The bit DA_MLB (0 = MSB 1st, 1 = LSB 1st) determines the order that the data comes in so that the 16-bit samples delivered to the packetizer can be properly aligned. Figure 2-25 illustrates an example of audio input timing

Figure 2-25. Audio Input Timing



There can be any number of ASCLKs ≥ 16 (usually 16–32 between ALRCK edges. Thus there may be extra ASCLKs versus collected data bits. There is no requirement for ASCLK (or ALRCK or ADATA)) to be continuous. A specified edge of ASCLK is used to sample the other two signals. Each 16-bit sample is sampled a specified number of ASCLK edges from the edge of ALRCK, which serves as a word sync.

The Number of Bytes/AudioLine ALP_LEN should be DWORD aligned so a whole number of L, R sample pairs can be delivered to memory. The start of audio L, R data capture is asynchronous and is enabled with ACAP_EN. The end of data capture is synchronized to the VRO code DWORD after ACAP_EN is disabled.

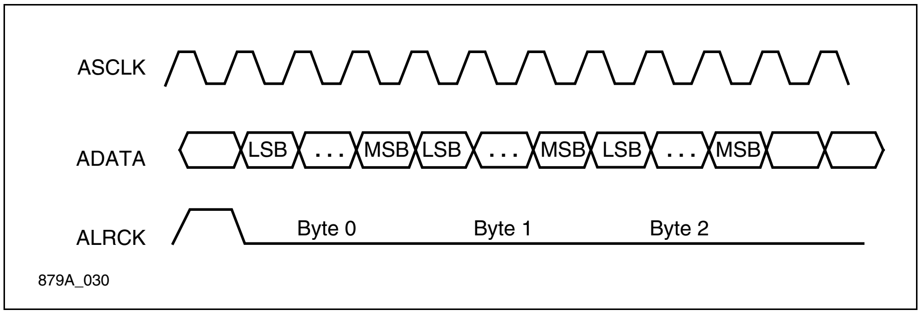
2.18.6 Data Packet Mode

The serial data on ADATA is again sampled with a programmable ASCLK edge. Data is collected in bytes (shift-register bit order programmable via DA_MLB). There are no extra ASCLKs between bytes, but there can be extra ASCLKs between packets (frames of data bytes). The maximum data rate allowed is 1 MBps or 8 MHz for ASCLK. There is no requirement for the interface signals to be continuous. The signal ALRCK is used for byte alignment and packet framing. DA_LRD will be used again to delay sampling of the shift-register to output packet data bytes (DA_LRD ASCLKs after the leading edge of ALRCK indicates the first bit of the first byte. Successive bytes are transferred every 8 ASCLKs). DA_LRI will be used to indicate the edge (0 = rising, 1 = falling) of ALRCK to use for synchronization.

The Number of Bytes/AudioLine ALP_LEN used here indicates the number of bytes to collect/count per ALRCK sync/framing signal. There can be extra ASCLKs or data following this count which will be ignored. The FIFO will only be sent data that belongs to the packet as specified by ALP_LEN bytes from the start of each ALRCK frame sync. The start of data capture is enabled via ACAP_EN and then synchronized to the start of a packet. Thus, the byte synchronized to ALRCK will be the first data byte in the audio line buffer. The end of data capture is synchronized to the VRO code DWORD after ACAP_EN is disabled.

Figure 2-26 illustrates the data packet mode signals.

Figure 2-26. Data Packet Mode Timing



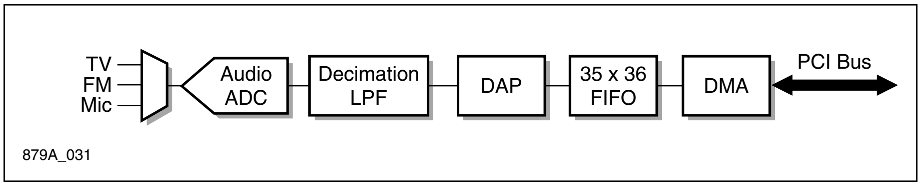
2.18.7 Audio Data Formats

Table 2-14 provides a summary of audio data formats (signed integer 16/8-bit) flowing through the audio FIFO. The audio data path is illustrated in Figure 2-27.

Table 2-14. Audio Data Formats

Format	F[35:32]	F[31:24]	F[23:16]	F[15:8]	F[7:0]
8-bit Samples	Status	S3[7:0]	S2[7:0]	S1[7:0]	S0[7:0]
16-bit Samples	Status	S1[15:8]	S1[7:0]	S0[15:8]	S0[7:0]
L,R Digital Audio	Status	R[15:8]	R[7:0]	L[15:8]	L[7:0]
Data	Status	D3[7:0]	D2[7:0]	D1[7:0]	D0[7:0]

Figure 2-27. Audio Data Path



2.18.8 Audio Dropout Detection

When a FIFO overflow occurs due to long bus access latencies, some data will not be written to the targeted memory buffer. When the DMA resumes, data writing begins at the address, as if all the skipped data were written. Thus, there would exist a hole or gap in the memory buffer containing old or stale data. By initializing the buffer DWORDs to 0x80008000 (0x808080) it is possible to detect words or bytes of audio not delivered (down to a single sample resolution level).

Enabling DA_LMT will cause the audio DMA to exclude writing 0x8000 words or 0x80 bytes (mode determined by DA_SBR) to the memory buffer. When the DAP detects 0x8000, it replaces this code with 0x8001 while in 16-bit mode. The 0x8000 sample is usually not present since it represents the most negative value of a 2’s complement 16-bit integer. While in 8-bit mode, 0x80 samples will be replaced by 0x81.

2.19 Digital Television Support

Digital television support will be available through upcoming application notes. Please contact the local sales office for availability.

3.0 Electrical Interfaces

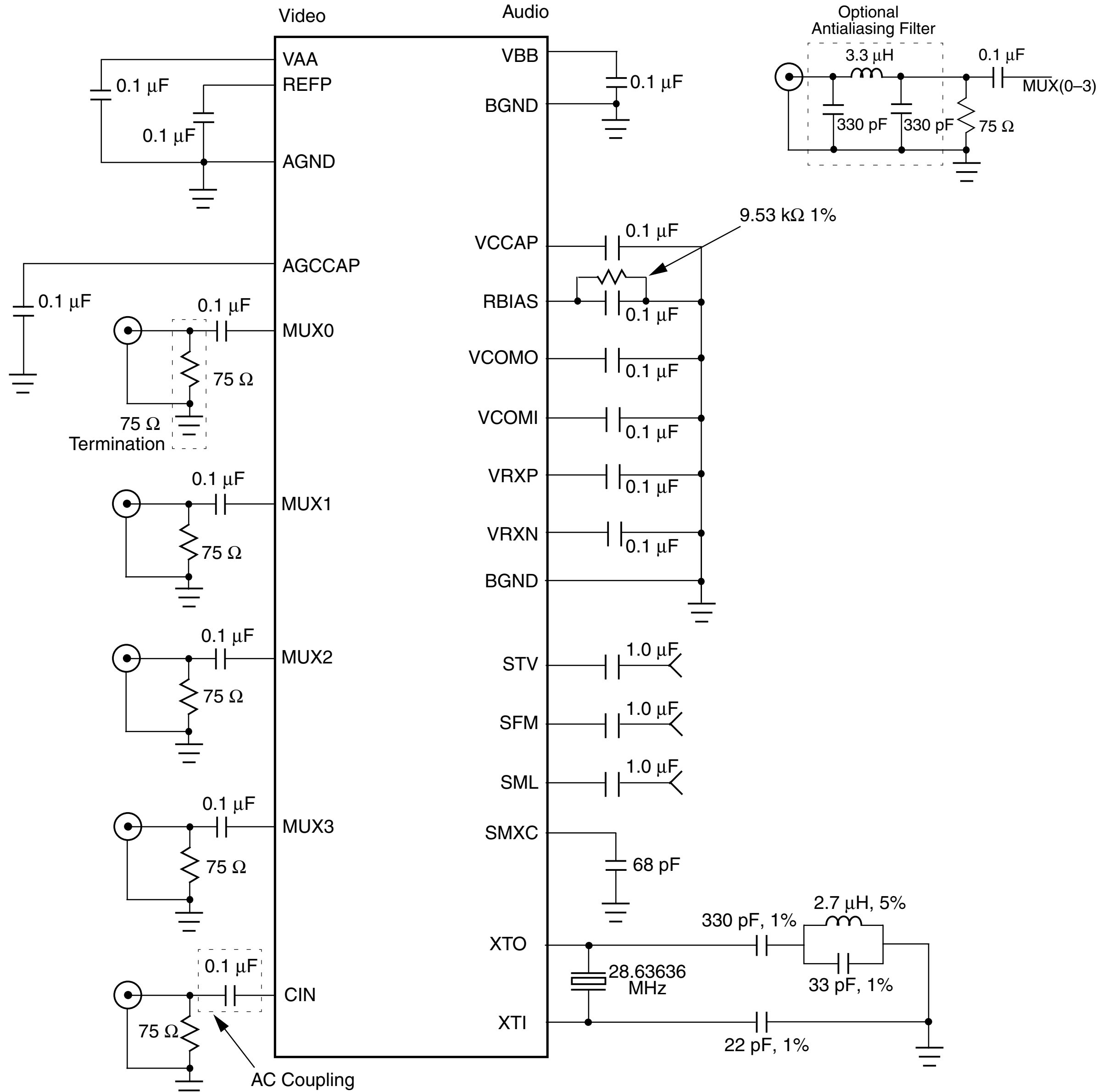
3.1 Input Interface

3.1.1 Analog Signal Selection

The Fusion 878A contains an on-chip 4:1 multiplexer (MUX[3:0]) that can be used to switch between four composite sources or three composite sources and one S-Video source. In the first configuration, connect the inputs of the MUX to the four composite sources. In the second configuration, connect three inputs to the composite sources and the other input to the luma component of the S-Video connector. When an S-Video source is input to the Fusion 878A, the luma component feeds through the input analog multiplexer, and the chroma component feeds directly into the C input pin. An automatic gain control circuit enables the Fusion 878A to compensate for nonstandard amplitudes in the analog signal input.

Figure 3-1 illustrates the Fusion 878A's typical external circuitry.

Figure 3-1. Typical External Circuitry



For recommended crystals, please see Table 3-1.

3.1.2 Multiplexer Considerations

The video multiplexer is not a break-before-make design. Therefore, during multiplexer switching time, it is possible for the input video signals to be momentarily connected together through the equivalent of 200 Ω. In addition, the multiplexers cannot be switched on a real-time, pixel-by-pixel basis.

3.1.3 Flash A/D Converters

The Fusion 878A uses two on-chip flash A/D converters to digitize the video signals. YREF+, CREF+ and YREF–, CREF– are the respective top and bottom of the internal resistor ladders.

The input video is always AC-coupled to the decoder. CREF– and YREF– are connected to analog ground. Voltage levels for YREF+ and CREF+ are controlled by the gain control circuitry. If the input video momentarily exceeds the corresponding REF+ voltage, it is indicated by LOF and COF in the DSTATUS register.

YREF+ and CREF+ are internally connected to REFP. CREF– is internally connected to AGND. YREF– is externally connected to AGND via YREFN.

3.1.4 A/D Clamping

An internally generated clamp control signal clamps the inputs of the A/D converter for DC restoration of the video signals. Clamping for both the Y and C analog inputs occurs within the horizontal sync tip. The Y input is always restored to ground while the C input is always restored to REFP/2.

3.1.5 Power-up Operation

Upon power-up, the status of the Fusion 878A's registers is indeterminate. The $\overline{\text{RST}}$ signal must be asserted to set the register bits to their default values. Upon reset, the Fusion 878A defaults to NTSC-M format.

3.1.6 Automatic Gain Controls

The Fusion 878A controls the voltage for the top of the reference ladder for each A/D. The automatic gain control adjusts the REFP, YREF+, and CREF+ voltage levels until the back porch sampling of the Y video input, as controlled by ADELAY, generates a digital code 0x38 from the A/D.

3.1.7 Crystal Inputs and Clock Generation

The Fusion 878A includes an internal phase lock loop (PLL) that may be used to decode NTSC and PAL using only a single crystal. The clock signal interface consists of a pair of I/O pins (XTI and XTO) connected to a 28.63636 MHz (8 × NTSC Fsc) crystal. Either fundamental or third harmonic crystals may be used. When using the PLL, a 28.63636 MHz, 50 ppm, fundamental (or third overtone) crystal must be connected across XTI and XT0. Alternately, a single-ended oscillator can be connected to XTI.

This clock is used to generate the CLKx2 frequency via the following equation:

Frequency = (F_input ÷ PLL_X) × PLL_I.PLL_F ÷ PLL_C
where F_input = 28.63636 MHz (50 ppm)
PLL_X = Reference pre-divider (divide by 2)
PLL_I = Integer input
PLL_F = Fractional input
PLL_C = Post divider (divide by 6)

These values should be programmed as follows to generate PAL frequencies:

PAL (CLKx2 = 35.46895 MHz)
PLL_X = 1
PLL_I = 0x0E
PLL_F = 0xDCF9
PLL_C = 0

The PLL can be put into low power mode by setting PLL_I to 0. For NTSC operation, PLL_I should be set to 0 to disable PLL. In this mode, the correct clock frequency is already input to the system, and the PLL is shut down. An out-of-lock or error condition is indicated by the PLOCK bit in the DSTATUS register.

When using the PLL to generate the required NTSC and PAL clock frequencies, the following sequence must be followed:

1. Initially, TGCKI bits in the TGCTRL register must be programmed for normal operation of the XTAL ports.
2. After the PLL registers are programmed, the PLOCK bit in the DSTATUS register must be polled until it has been verified that the PLL has attained lock (approximately 500 ms).
3. At that point the TGCKI bits are set to select operation via the PLL.

Crystals are specified as follows:

- 28.63636 MHz
- Third overtone or fundamental
- Parallel resonant
- 30 pF load capacitance
- 50 ppm
- Series resistance 40 Ω or less

Recommended crystals for use with the Fusion 878A are listed in Table 3-1.

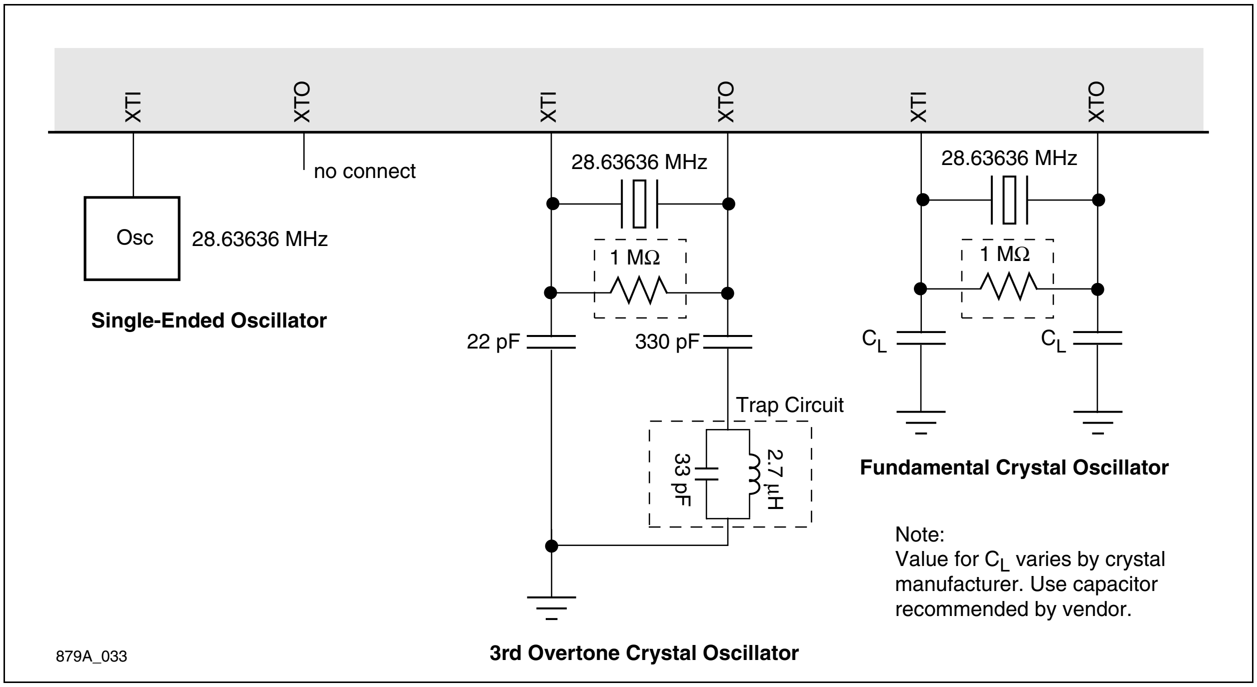
Table 3-1. Recommended Crystals

Crystal Manufacturer	Part Number
Standard Crystal (El Monte, CA) Phone: (626) 443-2121 Fax: (626) 443-9049 EMail: stdxtl@worldnet.att.net Web: www.standardcrystalcorp.com	2BAK28M636363GLE30A, 3rd Overtone 2AAK28M636363GLE30A, Fundamental
MMD Components (Irvine, CA) Phone: (949) 753-5888 Fax: (949) 753-5889 EMail: www.mmd.com info@mmdcomp.com	A30BA3-28.63636, 3rd Overtone A30BA1-28.63636, Fundamental
General Electronics (San Marcos, CA) Phone: (760) 591-4170 Fax: (760) 591-4164 EMail: gedlm@4dcomm.com Web: www.gedlm.com	PKHC49-28.63636-.030-005-40R, 3rd Overtone PKHC49/U-28.63636-.030-005-15R(F), Fundamental
M-Tron Industries (Yankton, SD) Phone: (605) 665-9321 Fax: (605) 665-1709 EMail: jkerg@mtron.com Web: www.mtron.com	MP - 1 28.63636, 3rd Overtone
Bomar (Middlesex, NJ) Phone: (732) 356-7787 Fax: (732) 356-7362 EMail: sales@bomarcrystal.com Web: www.bomarcrystal.com	BC1FFA330–28.63636 MHz, 3rd Overtone BC1FFA130–28.63636 MHz, Fundamental
CTS Frequency Controls (Sandwich, IL) Phone: (815) 786-8411 Fax: (815) 786-3600 EMail: kstone@ctsreeves.com Web: www.ctscorp.com	R3B55A30-28.63636, 3rd Overtone
Fox Electronics (Fort Myers, FL) Phone: (941) 693-0099 Fax: (941) 693-1554 EMail: sales@foxonline.com Web: www.foxonline.com	HC49U-FOX286, 3rd Overtone

The clock source tolerance should be 50 ppm or less. Devices that output CMOS voltage levels are required. The load capacitance in the crystal configurations may vary depending on the magnitude of board parasitic capacitance. The Fusion 878A is dynamic, and to ensure proper operation, the clocks must always be running with a minimum frequency of 28.63636 MHz.

Figure 3-2 illustrates the Fusion 878A clock options.

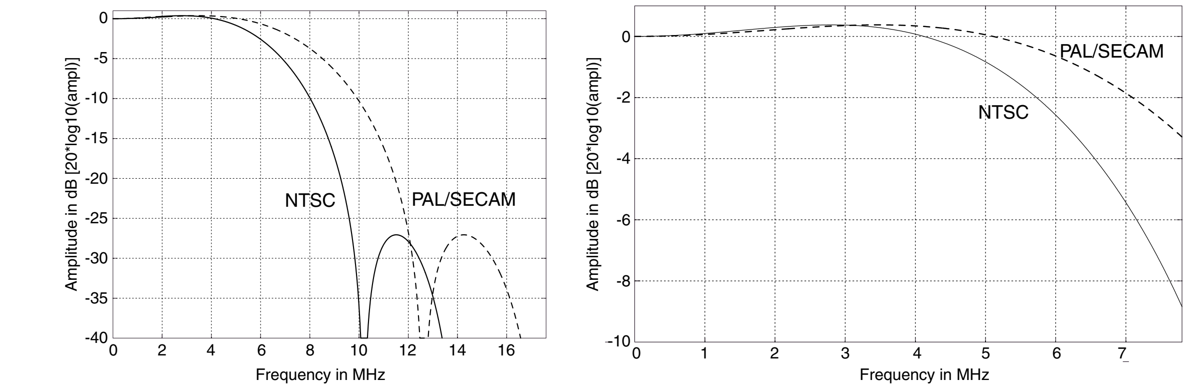
Figure 3-2. Clock Options



3.1.8 2X Oversampling and Input Filtering

Digitized video needs to be band-limited in order to avoid aliasing artifacts. Because the Fusion 878A samples the video data at 8 × Fsc (over twice the normal rate), no filtering is required at the input to the A/Ds. The analog video needs to be band-limited to 14.32 MHz in NTSC and 17.73 MHz in PAL/SECAM mode. Normal video signals do not require additional external filtering. After digitalization, the samples are digitally low-pass filtered and then decimated to 4 × Fsc. The response of the digital low pass filter is illustrated in Figure 3-3. The digital low pass filter provides the digital bandwidth reduction to limit the video to 6 MHz.

Figure 3-3. Luma and Chroma 2x Oversampling Filter



879A_034

3.2 PCI Bus Interface

The PCI local bus is an architectural, timing, electrical, and physical interface that allows the Fusion 878A to interface to the local bus of a host CPU. The Fusion 878A is fully compliant with PCI Rev. 2.2 specifications.

The supported bus cycles for the PCI initiator and target are:

- Memory read
- Memory write

The supported bus cycles for the PCI target only are:

- Configuration read
- Configuration write
- Memory read multiple
- Memory read line
- Memory write and invalidate

Memory write and invalidate is treated in the same manner as Memory write. Memory read multiple and Memory read line are treated in the same manner as Memory read.

The unsupported PCI bus features are:

- 64-bit bus extension
- I/O transactions
- Special, interrupt acknowledge, dual address cycles
- Locked transactions
- Caching protocol
- Initiator fast back-to-back transactions to different targets

As a PCI master, the Fusion 878A supports agent parking, AD[31:0], $\overline{\text{CBE}}$[3:0], and PAR driven if $\overline{\text{GNT}}$ is asserted and follows an idle cycle (regardless of the state of bus master).

All bus commands accepted by the Fusion 878A as a target require a minimum of three clock cycles. This allows for a full internal clock cycle address decode time (medium DEVSEL timing) and a registered state machine interface. Write burst transactions can continue with zero wait state performance on the fourth clock cycle and onward (unless writing to video decoder/scaler registers). All read burst transactions contain one wait-state per data phase. Figure 3-4 provides a block diagram of the PCI video interface. Figure 3-5 provides a block diagram of the PCI audio interface.

Figure 3-4. PCI Video Block Diagram

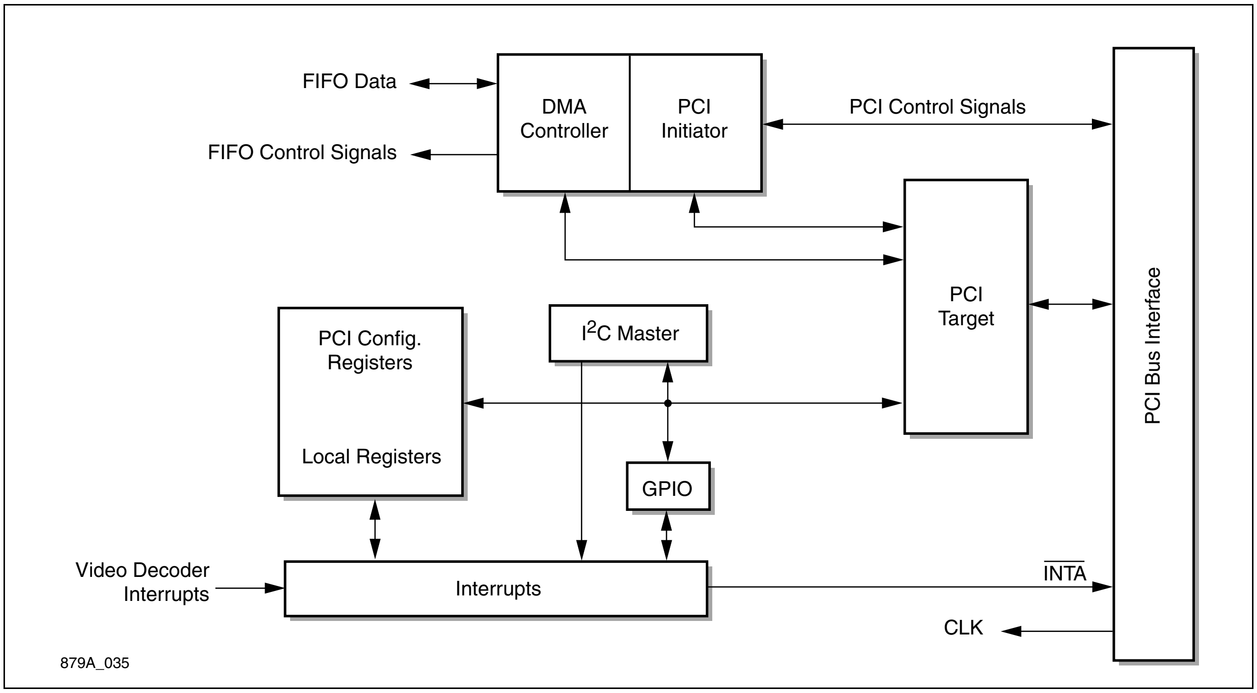
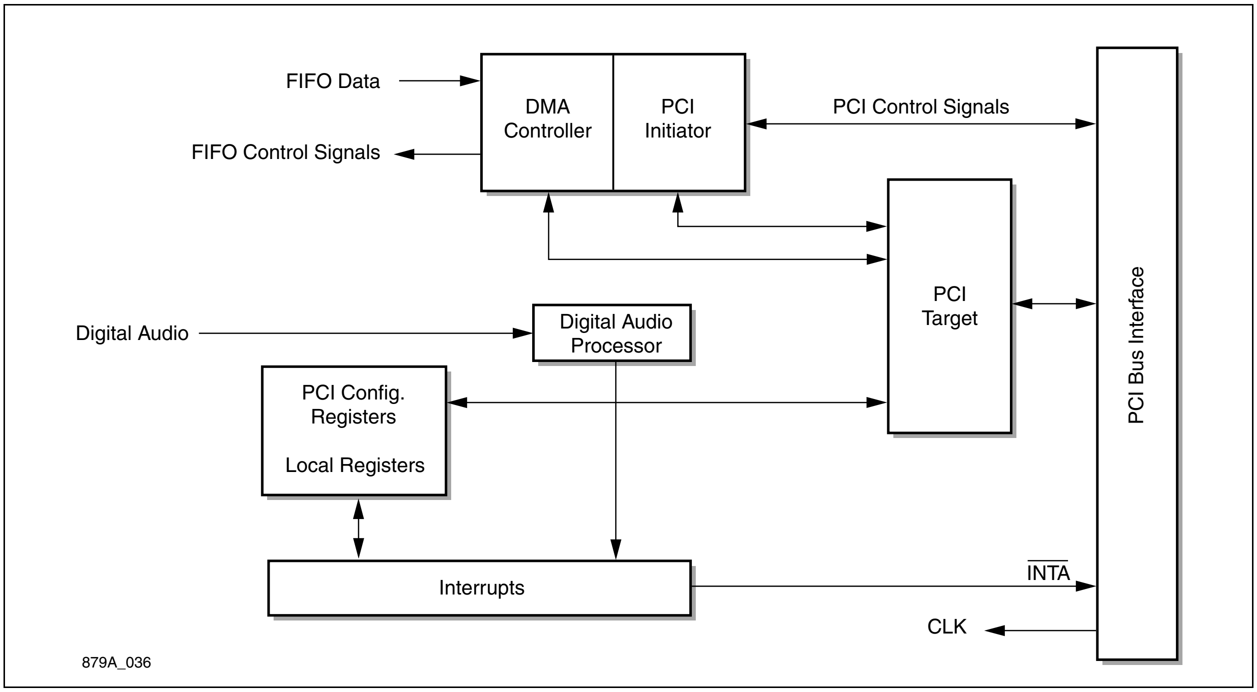


Figure 3-5. PCI Audio Block Diagram

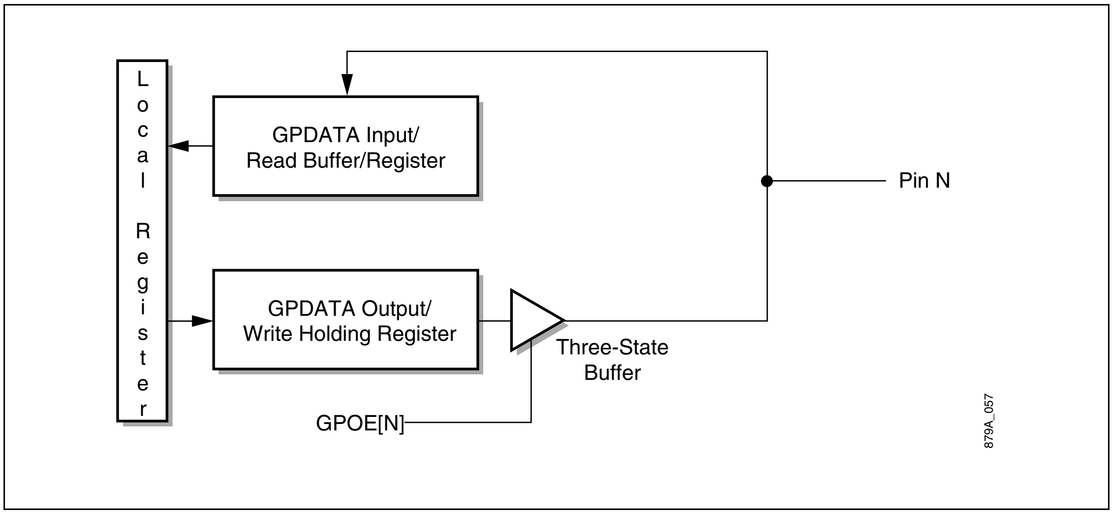


3.3 General Purpose I/O Port

3.3.1 GPIO Pin Architecture

Each GPIO pin is set up as a basic input/output buffer, with each bit of the GPOE register used to enable an individual pin's output driver (refer to Figure 3-6).

Figure 3-6. GPIO Pin Architecture


Local Register
GPDATA Input/ Read Buffer/Register
GPDATA Output/ Write Holding Register
Pin N
Three-State Buffer
GPOE[N]
879A_057

3.3.2 GPIO Modes in Fusion 878A

The GPIO port operates in five designated modes:

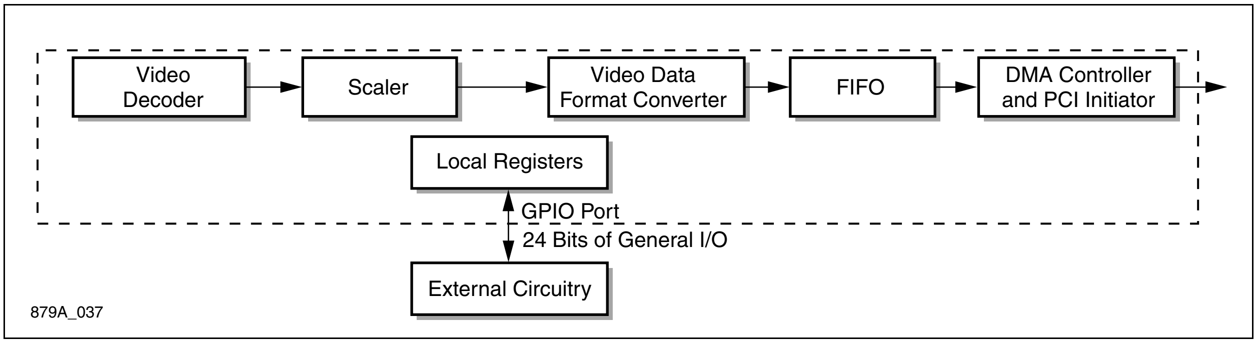
- Normal mode
- Synchronous Pixel Interface (SPI) Input mode
- SPI Output mode
- Digital Video Input mode
- Asynchronous Data Parallel mode

The GPIOMODE bits determine the port's mode of operation. Each GPIO pin can be individually configured, but GPIOMODE affects the entire port.

3.3.3 GPIO Normal Mode

The Normal mode of the GPIO port can be used to input or output general board-level signals to or from the PCI interface in the Fusion 878A. The GPIOMODE bits are in the default state of 00 during Normal mode. The GPIO port in Normal mode was not designed to support a high-speed interface for video data or other types of data. The functionality of the GPIO in Normal mode is illustrated in Figure 3-7.

Figure 3-7. GPIO Normal Mode



Data is written to and read from the GPIO pins through the GPDATA signal. When configured to output signals through the GPIO, information is written to a GPDATA holding register, which is output to the pin. When configured to input data from the GPIO, buffered data is read directly from the pin. Illustrated in Figure 3-6.

Each GPIO pin must be configured either as an input or an output according to the 24-bit GPOE register. Each bit in the register corresponds to an output driver for a GPIO pin. A value of 1 in the register enables the output buffer, making the pin an output pin. A value of 0 in the register disables the output buffer, making the pin an input pin.

To avoid any conflicts, parts will power-up with the GPOE register set to 0x000000, which means all pins are three-stated and configured as inputs.

Any information written to GPDATA[n] while GPOE[n] is low will be lost. Take care not to enable the GPOE bits for GPIO pins, set up on the board as input pins. If you read GPDATA[n] while GPOE[n] is enabled, the value read back will echo what was last written to the GPDATA holding register. This will likely create contention on the signal. Avoid enabling GPOE[n] when expecting to read an external value on GPIO[n].

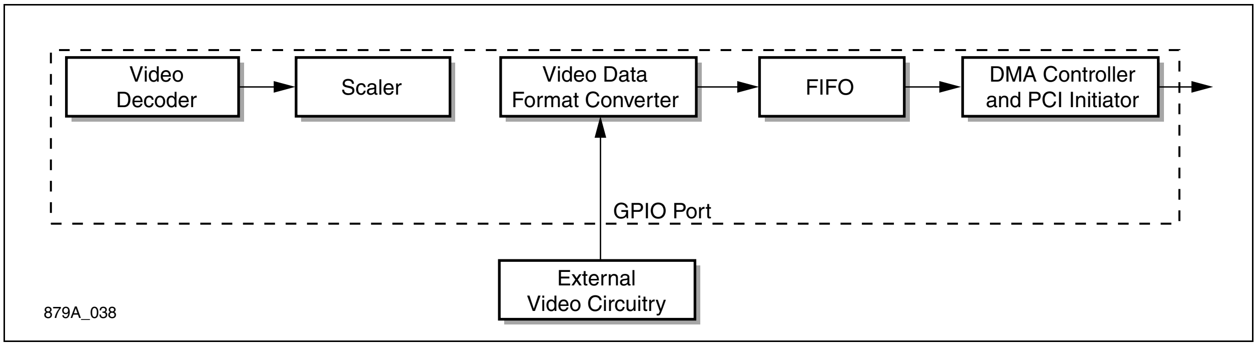
Normal mode permits PCI burst transfers by providing a 64-DWORD contiguous address space. Only the lower 24 bits of the 32-bit PCI DWORD are sent over the GPIO port. An interrupt may be requested through the GPIO[8] pin. The GPINTR pin is linked to the Interrupt Status Register within the part, and controls the GPINT bit of that register. The GPINTI and GPINTC bits provide options for the GPINT bit. The GPINTI bit, when set, inverts the value of the GPINTR signal immediately after the input buffer. The GPINTC bit provides a means of registering the GPINTR input. If the GPINTC bit is low, the GPINTR non-inverted/inverted input will go straight to the GPINT register. If GPINTC is high, the GPINT bit changes on the rising edge of the non-inverted or inverted GPINTR input.

Theoretically, the GPIO port can output (write) at a maximum of 11.1 MHz, and input (read) at a maximum of 8.3 MHz. Normal mode is asynchronous, and it is therefore difficult to ascertain a definite maximum frequency of operation. Real world maximum frequencies will be lower than theoretical frequencies because system configuration and PCI bus availability are limiting factors.

3.3.4 SPI Input Mode

SPI Input mode is used to input Synchronous Pixel Interface video information into the part. The interface accepts 16-bit YCrCb video data. Because the incoming video is inserted after the decoder and scaler, no adjustments can be made on hue, contrast, saturation, or brightness. Similarly, horizontal or vertical filtering or scaling also cannot be performed. Figure 3-8 illustrates the architecture of the SPI input mode.

Figure 3-8. GPIO SPI Input Mode



The GPCLK signal is used to input an external clock signal. The video data and related signals are accepted over the GPIO pins, defined in Table 3-2.

Table 3-2. SPI Input GPIO Signals (1 of 2)

GPIO	Signal	Description	Pin Number
[23]	$\overline{\text{HRESET}}$	A 1 to 64-GPCLK-long active low pulse. It is accepted on the rising edge of GPCLK. The falling edge of $\overline{\text{HRESET}}$ indicates the beginning of a new video line.	56
[22]	$\overline{\text{VRESET}}$	A 1 clock to 6 lines long active low pulse. It is accepted on the rising edge of GPCLK. The falling edge of $\overline{\text{VRESET}}$ indicates the beginning of a new field of video output.	57
[21]	HACTIVE	An active high signal that indicates the beginning of the active video and is accepted on the rising edge of GPCLK. The HACTIVE flag is used to indicate where nonblanking pixels are present.	58
[20]	DVALID	An active high pixel qualifier that indicates whether or not the associated pixel is valid. For continuous valid data, this signal can be connected to HACTIVE or VACTIVE.	59
[19]	CBFLAG	An active high pulse that indicates when Cb data is being output on the chroma stream. Only required for YCrCb input, otherwise connect to ground.	60
[18]	FIELD	When high, indicates that an even field (field 2) is being input; when low, it indicates that an odd field (field 1) is being output. The transition of FIELD should occur prior to the rising edge of $\overline{\text{VRESET}}$.	61

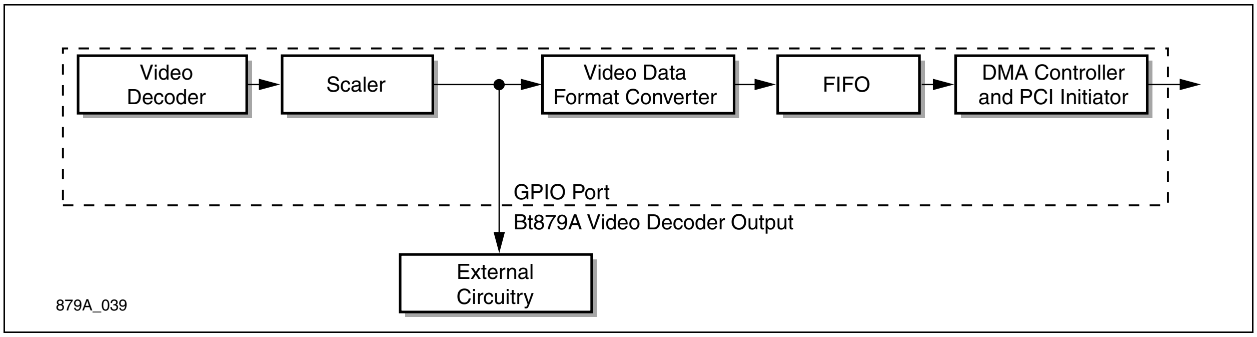
Table 3-2. SPI Input GPIO Signals (2 of 2)

GPIO	Signal	Description	Pin Number
[17]	VACTIVE	An active high signal that indicates the beginning of the active video and is accepted on the rising edge of GPCLK. The VACTIVE flag is used to indicate where nonblanking pixels are present.	67
[16]	GROUND	—	68
[15:8]	Y[7:0]	Digital pins for the luminance component of the video data stream, or for 8-bit transfers.	69–72 75–78
[7:0]	CrCb[7:0]	Digital pins for the chrominance component of the video data stream.	79–86

3.3.5 SPI Output Mode

SPI Output mode is used to output data from the decoder/scaler block of the part. This does not change the regular output of the part. Refer to Figure 3-9.

Figure 3-9. GPIO SPI Output Mode


Video Decoder
Scaler
Video Data Format Converter
FIFO
DMA Controller and PCI Initiator
GPIO Port
Bt879A Video Decoder Output
External Circuitry
879A_039

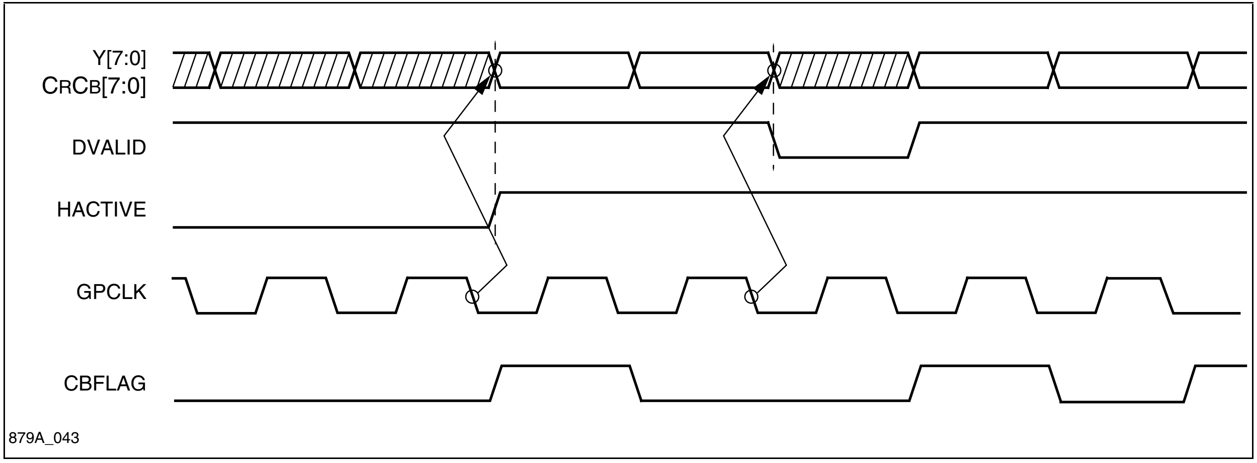
When running the GPIO port in SPI Output mode, the GPCLK is configured to output CLKx1 (4 × Fsc). CCIR601 is followed when the RANGE bit is set to 0. The GPIO pins are mapped as described in Table 3-3.

Table 3-3. SPI GPIO Output Signals

GPIO	Signal	Description	Pin Number
[23]	$\overline{\text{HRESET}}$	A 64-clock-long active low pulse, output following the rising edge of CLKx1. The falling edge of $\overline{\text{HRESET}}$ indicates the beginning of a new video line.	56
[22]	$\overline{\text{VRESET}}$	An active low signal that is at least two lines long (for non-VCR sources, $\overline{\text{VRESET}}$ is normally six lines long). It is output following the rising edge of CLKx1. The falling edge of $\overline{\text{VRESET}}$ indicates the beginning of a new field of video output. The falling edge of $\overline{\text{VRESET}}$ lags the falling edge of $\overline{\text{HRESET}}$ by two clock cycles at the start of an odd field. At the start of even fields, the falling edge of $\overline{\text{VRESET}}$ is in the middle of a scan line, horizontal count (HPIXEL/2)+1, on scan line 263 for NTSC and scan line 313 for PAL.	57
[21]	HACTIVE	An active high signal that indicates the beginning of the active video and is output following the rising edge of CLKx1. The HACTIVE flag is used to indicate where nonblanking pixels are present. The start and the end of the HACTIVE signal can be adjusted by programming the HDELAY and HACTIVE registers.	58
[20]	DVALID	An active high pixel qualifier that indicates whether or not the associated pixel is valid. DVALID is independent of the HACTIVE and VACTIVE signals. DVALID indicates which pixels are valid. DVALID will toggle high outside of the active window, indicating a valid pixel outside the programmed active region.	59
[19]	CBFLAG	An active high pulse that indicates when Cb data is being output on the chroma stream. During invalid pixels, CBFLAG holds the value of the last valid pixel.	60
[18]	FIELD	When high, indicates that an even field (field 2) is being output; when low it indicates that an odd field (field 1) is being output. The transition of FIELD is synchronous with the end of active video (i.e. the trailing edge of ACTIVE). The same information can also be derived by latching the $\overline{\text{HRESET}}$ signal with $\overline{\text{VRESET}}$.	61
[17]	VACTIVE	An active high signal that indicates the beginning of the active video and is output following the rising edge of CLKx1. The VACTIVE flag is used to indicate where nonblanking pixels are present. The start and the end of the VACTIVE signal can be adjusted by programming the VDELAY and VACTIVE registers.	67
[16]	VBISEL	An active high signal that indicates the beginning and end of the VBI. The end of VBISEL will adjust accordingly when VDELAY is changed.	68
[15:8]	Y[7:0]	Digital pins for the luminance component of the video data stream.	72–69, 78–75
[7:0]	CrCb[7:0]	Digital pins for the chrominance component of the video data stream.	79–86

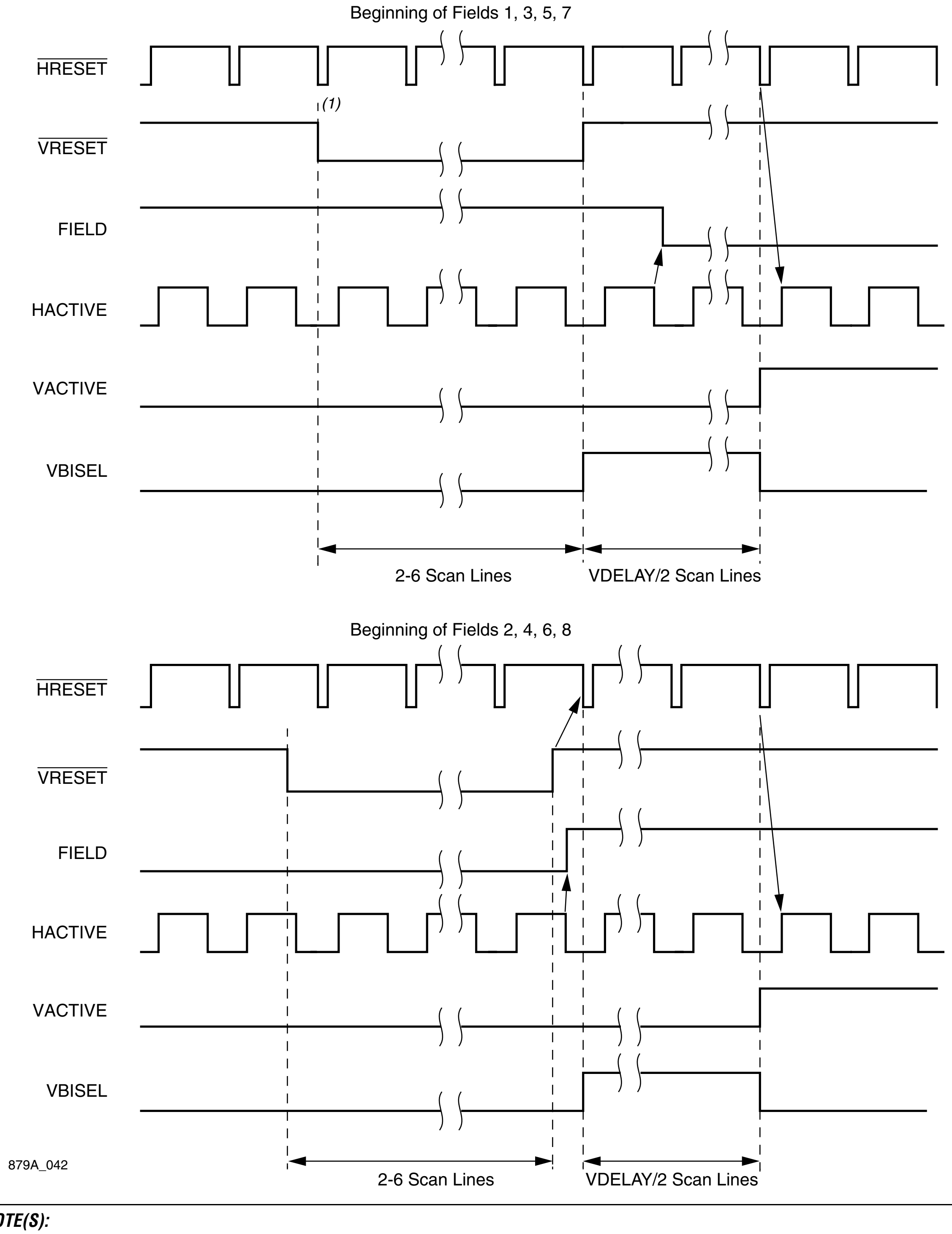
Figure 3-10 illustrates SPI output clock-data timing information. The falling edge of the output GPCLK triggers the change in video data. This should allow for ample setup and hold times for any device accepting the data.

Figure 3-10. Basic Timing Relationships for SPI Output Mode



Related video timing signals for both fields are illustrated in Figure 3-11. Note that in Fields 1, 3, 5, and 7 the falling edge of HRESET is two clock cycles ahead of the falling edge of VRESET.

Figure 3-11. Video Timing in SPI Output Mode



NOTE(S):

[1] HRESET precedes VRESET by two clock cycles at the beginning of fields 1, 3, 5 and 7 to facilitate external field generation.

2. FIELD transitions with the end of horizontal active video defined by HDELAY and HACTIVE.

3.3.6 GPIO SPI Mode Timing Parameters

For the timing parameters of GPIO SP1 mode, refer to Table 3-4.

Table 3-4. GPIO SPI Mode Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
NTSC: 4 × F_{SC} Rate	F_{S1}	14.31746	14.31818	14.31889	MHz
PAL: 4 × F_{SC} Rate	F_{S1}	17.73358	17.73447	17.73535	MHz
GPCLK Duty Cycle		45	—	55	%
GPCLK (falling edge) to Data Delay	4	0		15	ns
Data/Control Setup to GPCLK (falling edge)	5	5			ns
Data/Control Hold to GPCLK (falling edge)	6	5			ns
GPCLK Input:					
Cycle Time	7	56	—	10,000	ns
Low Time	8	22			ns
High Time	9	22			ns

3.3.7 Digital Video Input Mode

The GPIO port can be configured to accept general digital data streams. The parts contain a TG_RAM-based state machine that isolates the digital video input events from the internal decoder timing. This allows the digital video input H and V events to synchronize the sequencer, and allows the programmable output events to be positioned where needed to synchronize the decoder.

The digital input port provides flexibility for interfacing to various video standards. Software for programming the parts is included in the development kit for interfacing to the supported video standards. Table 3-5 provides the alternate pin definitions when using the digital video-in mode. Additional digital interfaces may be implemented by changing the TG_RAM contents. Contact your local Conexant sales office for more information.

Table 3-5. Pin Definition of GPIO Port When Using Digital Video-In Mode

GPIO	Signal	Description	Pin Number
[23]	CLKx1	Output signals for synchronizing to input video.	56
[22]	FIELD		57
[21]	VACTIVE		58
[20]	VSYNC		59
[19]	HACTIVE		60
[18]	HSYNC		61
[17]	Composite ACTIVE		67
[16]	Composite SYNC		68
[20]	VSYNC/FIELD	Input signals for synchronizing to input video.	59
[18]	HSYNC		61
[7:0]	DATA	Cb0, Y0, Cr0, Y1 ... Video data input at GPCLK = CLK × 2 rate.	79–86

3.3.7.1 CCIR656

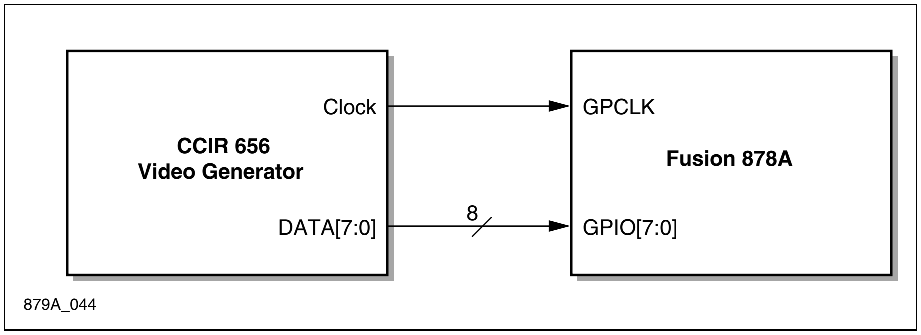
CCIR656 is a 27 MBps interface in the form of Cb, Y, Cr, Y, Cb, etc. In this sequence, the word sequence Cb, Y, Cr, refers to co-sited and color-difference samples, and the following word, Y, corresponds to the next luminance sample.

In this interface, two timing reference codes, SAV and EAV occur at the start and end of active video, respectively. These 4-byte codes occur at the outside boundaries of the active video. In the active video line, 720 pixels correspond to 1440 samples; 1448 bytes comprise a video data block (one line of video with reference codes).

The full video line consists of 1716 bytes (in 525 line systems) and 1728 bytes (in 625 line systems). The line breaks into two parts. The first part is blanking, which consists of the front porch, HSYNC, back porch, and 276 bytes (288 in 635 line systems) from EAV through SAV. The leading edge of HSYNC occurs 32-bytes (24 in 625 line systems) after the start of the digital line. The field interval is aligned to this leading edge of HSYNC.

Figure 3-12 illustrates a diagram of the interface. For a full reference on this standard, please refer to the International Telecommunications Union (ITU) specification, ITU-R-BT656. This can be obtained from the ITU Web Site at http://www.itu.int/publications/.

Figure 3-12. CCIR 656 Interface to Digital Input Port



3.3.7.2 Modified SMPTE-125

The Modified SMPTE-125 interface is the same as CCIR656, but the clock runs at 24.54 MHz, with 640 active pixels on a 780 pixel line. This clock rate difference provides simple interface for digital cameras from Silicon Vision and Logitech.

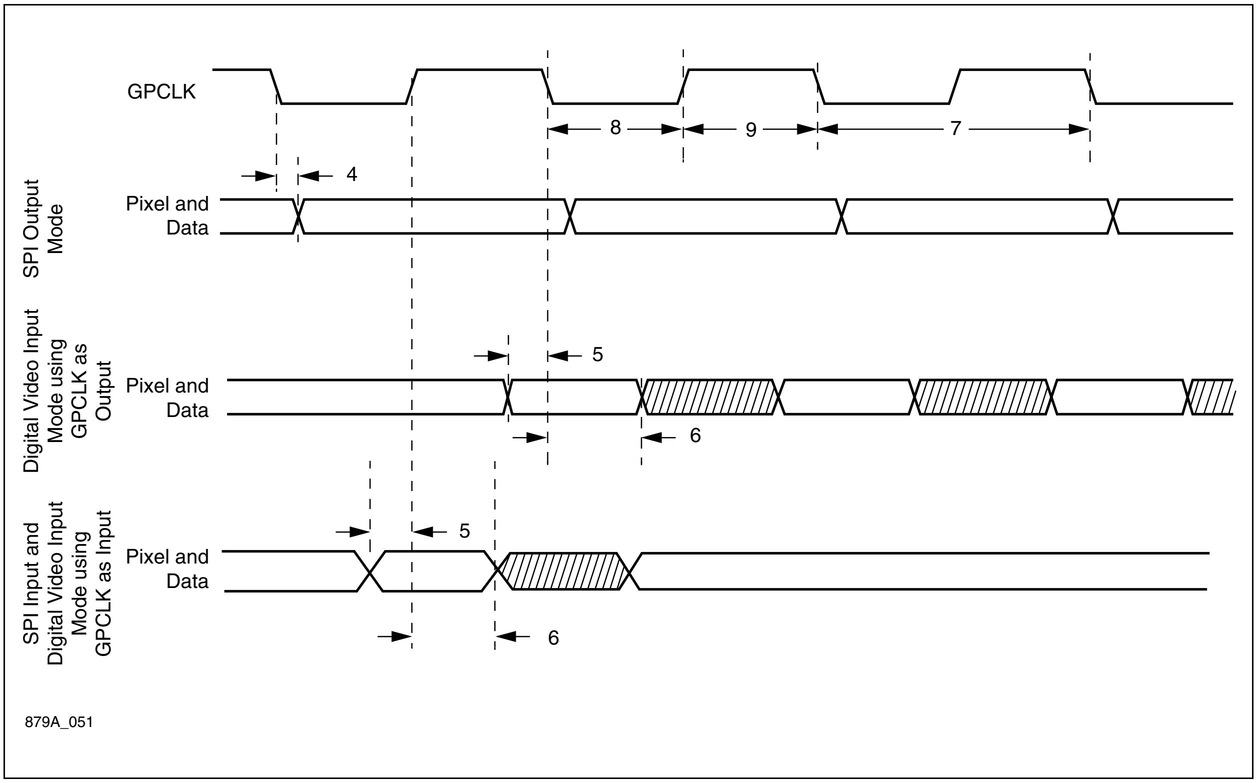
To properly implement a digital video input mode with CCIR656 incoming data, several steps must be taken to set the part up to accept data:

1. Set the signal format to CCIR656 (VSFMT[2:0] in the DVSIF register).
2. Set the sync video reference to align with Cb, Cr, Y1, or Y0 (SVREF bits in DVSIF register).
3. Disable the sync output register (VSIF-ESO in the DVSIF register).
4. Load the TG_RAM table. Place the Timing Generator Video mode into Read/Write mode (TGC_VM bit in the TGCNTRL register). Reset the Timing Generator Address (GPC_AR in the TGCNTRL register. Write the LSB of the TG_RAM table first. The address will be incremented automatically. TG_RAM maps may be obtained from your local FAE.
5. Set the desired PLL frequency. (This is not necessary, but will provide the correct blue screen output in the event the input is disconnected. If the input clock is disconnected, the decoder will run off the PLL, or the XTAL if the PLL is sleeping.)
6. Select GPCLK as the decoder input clock. Set the GPIO_DMA_CTL register bits [12:10] to 100 to select the SPI Input mode. The entire decoder will now be run by the external clock.
7. Enable the Timing Generator Video mode, by setting bit 0 of the TGCTRL register to a logical 1.

3.3.8 GPIO Timing Diagram for SPI and Digital Video Input Modes

Figure 3-13 illustrates an overview of the GPIO timing for SPI Input and Digital Video Input modes.

Figure 3-13. GPIO Timing Diagram

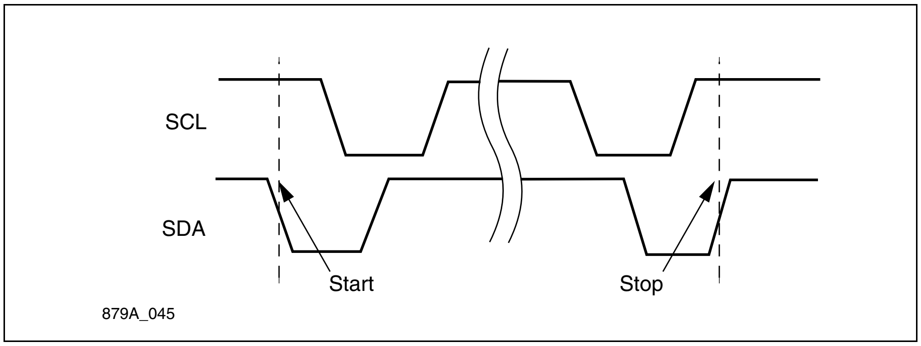

GPCLK
8
9
7
4
SPI Output Mode
Pixel and Data
Digital Video Input Mode using GPCLK as Output
Pixel and Data
5
6
SPI Input and Digital Video Input Mode using GPCLK as Input
Pixel and Data
5
6
879A_051

3.4 I^{2}C Interface

The I^{2}C bus is a two-wire serial interface. Serial clock and data lines, SCL, and SDA transfer data between the bus master and the slave device. The I^{2}C bus within the Fusion 878A supports repeated starts, up to 396.8 kHz timing, and multi-byte sequential transactions. The I2CRATE signal specifies either 99.2 kHz or 396.8 kHz timing rate. If the PCI clock runs at less than the maximum rate, these rates will slow down proportionately. For details on the I^{2}C register, see *0x110—I2C Data/Control Register* in Chapter 5.0.

The relationship between SCL and SDA is decoded to provide both a start and stop condition on the bus. To initiate a transfer on the I^{2}C bus, the master must transmit a start pulse to the slave device. This is accomplished by taking the SDA line low while the SCL line is held high. The master should generate a start pulse only at the beginning of the cycle, or after the transfer of a data byte to or from the slave. To terminate a transfer, the master must take the SDA line high while the SCL line is held high. The master may issue a stop pulse at any time during an I^{2}C cycle. Since the I^{2}C bus interprets any transition on the SDA line during the high phase of the SCL line as a start or stop pulse, care must be taken to ensure that data is stable during the high phase of the clock. This is illustrated in Figure 3-14.

Figure 3-14. The Relationship Between SCL and SDA



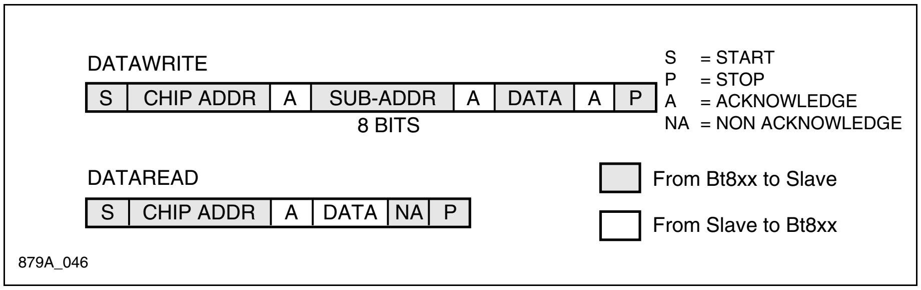
An I^{2}C write transaction consists of sending a START signal, 2 or 3 bytes of data (checking for a receiver acknowledge after each byte), and a STOP signal. The write data is supplied from a 24-bit register with bytes I2CDB0, I2CDB1, and I2CDB2. This 24-bit register is shifted left to provide data serially, with the MSB as the first bit. An I^{2}C write occurs when the R/$\overline{W}$ bit in the I2CDB0[0] is set to a logical low. The system driver can write 2 or 3 bytes of data by selecting the appropriate value for I2CW3BRA bit.

An I^{2}C read transaction consists of sending a START signal, 1 byte of data (checking for a receiver acknowledge), reading 1 data byte from the slave, sending the master NACK, and sending the STOP signal. The data read is shifted into the I2CDB2 register. An I^{2}C read occurs when the R/$\overline{W}$ bit in the I2CDB0[0] is set to a logical 1, illustrated in Figure 3-15.

When the read or write operation is completed, the Fusion 878A sends an interrupt over the PCI bus to the host controller. The status bit RACK will indicate if the operation completed successfully with the correct number of slave acknowledges.

In the case where direct control of the I^2C bus lines is desired, the Fusion 878A device driver can disable the I^2C hardware control and can take software control of the SCL and SDA pins. This is useful in applications where the I^2C bus is used for general purpose I/O or if a special type of I^2C operation (such as multi-mastering) needs to be implemented.

Figure 3-15. I^2C Typical Protocol Diagram



A transaction sequence involving a repeated START usually occurs after setting up a slave read address using a 2-byte write transaction, then following with a 1-byte read (with 1-byte slave address write) transaction. The STOP can be disabled for the first transaction by setting I2CNOSTOP high only for the first register write. I2CNOSTOP should be reset during the second register write because every set of I^2C transactions should begin with a START and end with a STOP. (This rule is applicable to the overall transaction set or sequence).

Multi-byte (> 3) write transactions enable communication to devices that support auto-increment internal addressing. To avoid reset of the internal address sequencer in some devices, a STOP is not transmitted until the very end of the sequence. The first register write should enable a 2-byte write transaction with START. I2CNOSTOP should be set to disable STOPs temporarily. The SCL signal will be held in the active low state while the I2CDONE interrupt is processed. The second and successive register writes will enable 1-byte writes to be transmitted without START and without STOP (I2CNOS1B, I2CNOSTOP both high). The last register write should enable the final STOP to be sent to end the sequential write transaction set. The 1-byte write data is sent from I2CDB0. The R/W mode was saved from the first register write when the START was transmitted.

For multi-byte (>1) sequential reads, the first register write enables the START and slave address to be transmitted. The first read byte is received into I2CDB2. The STOP is disabled via I2CNOSTOP. Since the reading continues, the master should acknowledge at the end of the first read (set I2CW3BRA high). The SCL signal will be held in the active low state while the I2CDONE interrupt is processed.

The second and successive register writes will enable 1-byte reads to be received without sending START or STOP (I2CNOS1B, I2CNOSTOP both high). The last register write should reset I2CW3BRA low to master NACK. This will indicate final read from slave, and enable the final STOP to be sent to end the sequential read transaction set. The 1-byte read data is also read from I2CDB2. The R/W mode was saved from the first register write when the START was transmitted, so I2CDB0 is a Don't Care during 1-byte reads.

For detailed information on the I^2C bus, refer to *The I^2C-Bus Reference Guide,* reprinted by Conexant.

3.5 I^2C Serial EEPROM Interface

The external EEPROM must reside on the I^2C bus (SDA, SCL). This interface supports the IC's equivalent to the 24C02 or 24C02A 2 k bit 5 V CMOS Serial EEPROM. The 7-bit slave device address is 1010000. The EEPROM can be read anytime using the I^2C hardware or software modes. The read transaction sequence is:

1. START
2. 0xA0
3. 8-bit byte address
4. START
5. 0xA1
6. 8-bit read data, followed by (master NACK &) STOP

Thus, a normal 2-byte write transaction without STOP followed by a 2-byte read transaction allows random access to a data byte.

3.5.1 EEPROM Address Mapping

Fusion 878A can support one EEPROM (max 256 B), typically a single 24C02. Re-map the 8-bit addressable physical memory space to an 8-bit logical address space by inverting the address A[7:0], and subtracting 4. The 7-bit slave device address is 1010_xxx where the xxx bits are (normally used for A[10:8]) set to zero. The A2, A1, A0 pins on the 24C02 device should be tied low to match.

Table 3-6. External EEPROM Memory Map

Logical Address	Physical Address	24C02
251	0x00	Read/Write
...	...	
124	0x7F	
123	0x80	Read-Only
...	...	
–4	0xFF	

Re-mapping the address space in this way allows the subsystem IDs to be stored at a fixed physical base address and have the read-only section precede the read-writable section. The entire address range (rather than some sub-portion) is inverted to maintain physical address continuity. The address translation applies only when the hardware accesses subsystem IDs or vital product data. If SW uses the I^2C function to directly address the EEPROM, the actual physical address must be used.

3.5.2 Subsystem Vendor ID

PCI Configuration Header Location 0x2C specifies the subsystem vendor ID and the subsystem ID. If an external EEPROM is present, the subsystem vendor ID and subsystem ID and vital product data are uploaded. If an external EEPROM is not present, the 32 bits of the header register default to 0x0000, and the register can be programmed using BIOS.

This chapter defines the subsystem vendor ID configuration with and without an EEPROM present. For more details on the Function 1 definition, refer to Section 6.1. The Function 0 subsystem vendor ID registers are defined starting on *0x00—Vendor and Device ID Register*, and the Function 1 subsystem vendor ID registers are defined starting on *0x00—Vendor and Device ID Register*.

3.5.2.1 EEPROM Upload at PCI Reset

The 32-bit subsystem IDs are read from the EEPROM by taking control of the I^{2}C circuit just after PCI reset and performing a 4-byte sequential read access transaction in the 100 kHz mode, starting at physical address 0xFC. The full read sequence is detailed in Table 3-7.

Table 3-7. EEPROM Upload Sequence

Master		Slave		Master	Comment
Control	Data	Data	Control	Control	
START	0xA0	—	ACK	—	Write control byte with slave chip address
	0xFC	—	ACK	—	Data bytes base address
START	0xA1	—	ACK	—	Read control byte with slave chip address
—	—	0x	—	ACK	Subsystem ID [15:8] at 0xFC
—	—	0x	—	ACK	Subsystem ID [7:0] at 0xFD
—	—	0x	—	ACK	Subsystem Vendor ID [15:8] at 0xFE
—	—	0x	—	NACK,STOP	Subsystem Vendor ID [7:0] at 0xFF

If at any time the slave device issues a NACK (because the device is not present), the sequence is aborted, and the subsystem vendor IDs read 0x00000000. Normally it will take ~660 µs to read this DWORD into the PCI configuration register. If this register is accessed before it is updated, the PCI target will issue a RETRY.

3.5.2.2 Register Load from BIOS

The Subsystem IDs register is read-only. However, by enabling SVIDS_EN in the user-defined PCI configuration control register, the Subsystem Vendor IDs can be written. Then SVIDS_EN should be disabled. This value needs to be programmed before OS boots and has access during configuration. This must occur via support from the BIOS versus the IC driver. If this feature can be supported by software (and Vital Product Data is not supported), then the external EEPROM is not required.

3.5.2.3 Programming and Write-Protect

The EEPROM can be programmed before soldering onto the PCB, or it may be programmed through Fusion 878A using the I^2C hardware or software modes. The write transaction sequence is:

1. START
2. 0xA0
3. 8-bit byte address
4. 8-bit write data
5. STOP

This 3-byte transaction then initiates a programming cycle internal to the EEPROM. The write completion status can be monitored by initiating another write transaction and checking the ACK status. Anytime a transaction has been aborted with a slave NACK, that implies the EEPROM device is still busy with the internally timed programming cycle.

The upper half of a 24C02 device can be write-protected by adding a pull-up resistor to the EEPROM WP pin. Just pull the pin to GND during programming.

3.5.3 Vital Product Data

Fusion 878A complies with the Vital Product Data (VPD) capability structure as defined in the PCI Local Bus Specification Revision 2.2. The flag bit in the VPD Capability register indicates the transfer of data between the VPD Data register and the EEPROM.

To read information from the EEPROM, write a 0 to the VPD flag at the same time you supply the 15-bit address to the VPD address bits of the VPD Capability register. The Fusion 878A then sets the VPD flag after it completes reading 4 bytes from the EEPROM, returning Address +3, ... Address +0 (little endian format). Software should monitor the flag to determine the correct time to read the VPD Data Register.

To write information to the R/W portion of the EEPROM, write four bytes (a DWORD) to the VPD Data Register, then set the flat bit to 1 while also supplying the 15-bit address to the appropriate bits in the VPD Capability register. After four bytes are written to the EEPROM, the Fusion 878A resets the flag bit to 0.

The VPD Data Register is byte-accessible; however, all data transfers between the EEPROM and the Fusion 878A are 4-byte transactions.

3.5.3.1 Vital Product Data EEPROM Addressing

The 15-bit logical byte address maps to the EEPROM physical storage space beginning at 0xFB. Only eight bits of the address field are supported. The EEPROM physical address equals the (VPD logical address + 4) xor 0xFF. Since all VPD accesses are a full DWORD, the four bytes will use the VPD address + 3 as its base. Decreasing the VPD logical address will then correspond to increasing the EEPROM physical address.

3.5.3.2 Vital Product Data Read Sequence

When SW resets the VPD flag bit, the device initiates the following I^{2}C sequence to read four bytes from the EEPROM (assumes VPD address was set to 0):

Table 3-8. VPD Read Sequence

Master		Slave		Master	Comment
Control	Data	Data	Control	Control	
START	0xA0		ACK		Write ctrl byte with slave chip adr
	0xF8		ACK		Data bytes base address
START	0xA1		ACK		Read ctrl byte with slave chip adr
		0x		ACK	VPD[31:24] @ 3 @ 0xF8
		0x		ACK	VPD[23:16] @ 2 @ 0xF9
		0x		ACK	VPD[15:8] @ 1 @ 0xFA
		0x		NACK, STOP	VPD[7:0] @ 0 @ 0xFB

The device sets the VPD flag bit once all four bytes are read into the VPD data register. If a slave NACK is received, the sequence is aborted and the flag bit is not set.

NOTE: The VPD base address used is (VPD logical adr + 7) XOR 0xFF for the DWORD page mode read.

3.5.3.3 Vital Product Data Write Sequence

When SW sets the VPD flag bit, the device initiates the following I2C sequence to write four bytes to the EEPROM (assumes VPD address was set to 247 (not DWORD aligned)):

Table 3-9. VPD Write Sequence

Master		Slave		Master	Comment
Control	Data	Data	Control	Control	
START	0xA0		ACK		Write ctrl byte wiht slave chip adr
	0x01		ACK		Data bytes base address
	0x		ACK		VPD[31:24] @ 250 @ 0x01
	0x		ACK	STOP	VPD[23:16] @ 249 @ 0x02
START	0xA0		?ACK?		Loop until ACK
START	0xA0		ACK		Write ctrl byte with slave chip adr
	0x03		ACK		Data bytes base address
	0x		ACK		VPD[15:8] @ 248 @ 0x03
	0x		ACK	STOP	VPD[7:0] @ 247 @ 0x04
START	0xAC		?ACK?	STOP	Loop until ACK, then STOP

The device resets the VPD flag bit once all four bytes from the VPD data register are programmed into the EEPROM. If a slave NACK is received during either page write, the sequence is aborted and the flag bit is not reset.

NOTE: The VPD base address used is (VPD logical adr + 7)^8’hFF for the first word page mode write, and (VPD logical adr + 5) XOR 0xFF for the second word page mode write.

A SW time out on the flag status is the only way to detect an error. It takes ~4 mS to program the DWORD into the EEPROM.

3.6 Power Management Interface

Fusion 878A supports the new capabilities feature for power management as outlined in *PCI Bus Power Management Interface Specification*, *Revision 1.1*. Power management states D0, $D3_{hot}$ and $D3_{cold}$ are supported. Optional power states D1 and D2 are not supported since there is no significant power savings without going to D3. Restoring a function from D1 or D2 would also require device specific interaction that the operating system does not currently support.

3.6.1 PME#

The Power Management Event signal PME# is not used since wake-up events are not generated by the Fusion 878A.

3.6.2 D3 Power States

Fusion 878A supports D0 (on) and $D3_{cold}$ (off) by default. Each function also supports $D3_{hot}$ independently. When placing a function in $D3_{hot}$, the operating system is required to disable I/O and memory space as well as bus mastering via the PCI Command register. Restoring a function from D3 requires the operating system to re-initialize the function. Full context must be restored before the function is capable of resuming normal operation.

Functions in $D3_{hot}$ respond to configuration space accesses as long as the power and clock are supplied. In addition to each function being disabled from memory access and bus mastering, the $D3_{hot}$ power state will enable extra power savings by powering down as many circuits as possible. The video function will disable the VFE (sleep A/Ds, disable AGC), PLL, and decoder clocks (gate off XTAL signals in CLKIOGEN). The audio function will disable its clock as well as the AFE. In addition each function will reset as many circuits as possible without disabling configuration access.

3.7 JTAG Interface

3.7.1 Need for Functional Verification

As the complexity of imaging chips increases, the need to easily access individual chips for functional verification is becoming vital. The Fusion 878A has incorporated special circuitry that allows it to be accessed in full compliance with standards set by the Joint Test Action Group (JTAG). Conforming to IEEE Std P1149.1 "*Standard Test Access Port and Boundary Scan Architecture*," the Fusion 878A has dedicated pins that are used for testability purposes only.

3.7.2 JTAG Approach to Testability

JTAG's approach to testability uses boundary scan cells placed at each digital pin and digital interface. In the Fusion 878A, a digital interface is the boundary between an analog block and a digital block. All cells are interconnected into a boundary scan register that applies or captures test data used for functional verification of the integrated circuit. JTAG is particularly useful for board testers using functional testing methods.

JTAG consists of five dedicated pins comprising the Test Access Port (TAP):

- Test Mode Select (TMS)
- Test Clock (TCK)
- Test Data Input (TDI)
- Test Data Out (TDO)
- Test Reset ($\overline{\text{TRST}}$)

The $\overline{\text{TRST}}$ pin will reset the JTAG controller when pulled low at any time. Verification of the integrated circuit and its connection to other modules on the printed circuit board can be achieved through these five TAP pins.

With boundary scan cells at each digital interface and pin, the Fusion 878A has the capability to apply and capture the respective logic levels. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry. The output result is scanned out on the TDO pin and externally checked. While isolating the Fusion 878A from other components on the board, the user has easy access to all digital pins and digital interfaces through the TAP and can perform complete functionality tests without using expensive bed-of-nails testers.

3.7.3 Optional Device ID Register

The Fusion 878A has the optional device identification register defined by the JTAG specification as displayed in Table 3-10. This register contains information concerning the revision, actual part number, and manufacturer's identification code specific to Conexant. This register can be accessed through the TAP controller via an optional JTAG instruction.

Table 3-10. Device Identification Register

Version				Part Number																Manufacturer ID											
X	X	X	X	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	1	1	0	1	0	1	1	0	1
0				0x036E																0x0D6											
4 Bits				16 Bits																11 Bits											

3.7.4 Verification with the TAP Controller

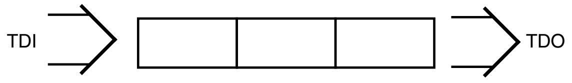
A variety of verification procedures can be performed through the TAP controller. With a set of four instructions, the Fusion 878A can verify board connectivity at all digital interfaces and pins. The instructions (listed below) are accessible by using a state machine standard to all JTAG controllers:

- Sample/Preload
- Extest
- ID Code
- Bypass (see Figure 3-16)

Refer to the IEEE Std 1149.1 specification for details concerning the Instruction Register and JTAG state machine (http://standards.ieee.org/).

Conexant has created a BSDL with the AT&T BSD™ Editor. For JTAG testing, obtain a disk with an ASCII version of the complete BSDL file by contacting your local Conexant sales office.

Figure 3-16. Instruction Register



EXTEST	0	0	0
Sample/Preload	0	0	1
ID Code	0	1	0
Bypass	1	1	1

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4.0 PC Board Layout Considerations

4.1 Layout Considerations

The PC board layout should be optimized for lowest noise on the Fusion 878A power and ground lines. Route digital traces away from analog traces. All shields must be connected to the ground plane with low impedance connection. Use shielded connectors.

4.1.1 Capacitors

From the following pins to ground, place bypass capacitors as close to the Fusion 878A as possible (using 0.1 µF ceramic capacitors):

Table 4-1. Capacitor Location

VBB	Pin 95[(1)]
VBB	Pin 101[(1)]
VAA	Pin 110
VAA	Pin 115
VAA	Pin 117

NOTE(S):
[(1)] These pins should be tied to the same voltage as analog source device.

Additionally, place bypass capacitors from all other voltage pins to ground (using 0.1 µF ceramic capacitors) as close to the Fusion 878A, where possible. Also, whenever possible, place traces from all power pins to a bypass capacitor on the component side, in addition to any feed-through. Finally, place traces from all ground pins to a bypass capacitor on the component side, in addition to any feed-through, when possible.

Ensure that there is ample ground plane under the Fusion 878A. Make wide paths of copper under and around the Fusion 878A, if possible. Avoid creating a cut in the plane with feed-throughs instead, disperse them. Also ensure that there is ample power plane under the Fusion 878A. Make wide paths of copper under and around the Fusion 878A, if possible. Avoid creating a cut in the plane with feed-throughs: instead, disperse them.

To fill:

- Copper fill ground on the component side
- Power fill on the circuit side of two layer boards
- Ground fill on both sides of four or more layer boards

4.1.2 Components

From the following pins, place components as close to the Fusion 878A as possible. Connect a trace from the pin to the component on the component side when possible.

AGCCAP	Pin 111
REFP	Pin 112
VCCAP	Pin 107
VRXP	Pin 103
VCOMI	Pin 104
VCOMO	Pin 105
RBIAS	Pin 106
SMXC	Pin 96

4.2 Split Planes and Voltage Regulators

The reference designs included in the *Bt878/Fusion 878A Hardware Users Guide* have no split planes. Careful attention has been given to creating one continuous ground plane and one continuous power plane. This implementation produces optimal video and audio performance. These boards have acceptable EMI profiles. There is a voltage regulator on one design but it is for the TV tuner only.

An alternative implementation is obtained by adding split digital and analog power and ground planes. Additional noise immunity can be obtained by adding a voltage regulator for the analog and the digital power pins. Tests have been performed with split planes and voltage regulators in a variety of combinations. Measurements have been made and some increased noise reduction has been seen on some systems. The noise improvements have not been substantial enough to warrant additional cost. Additionally, splitting planes requires close consideration to EMI and trace routing. If split planes or regulators are desired, some guidelines are included.

- Digital terminating resistors should be connected to digital supplies.
- Components connected to analog pins should be connected to analog ground.

The following pins have capacitors and/or resistors connected to them. The other end of these components should be connected to analog ground.

AGCCAP	Pin 111
REFP	Pin 112
VCCAP	Pin 107
VRXP	Pin 103
VCOMI	Pin 104
VCOMO	Pin 105
RBIAS	Pin 106
SMXC	Pin 96

- Analog traces should be routed over analog planes only, when possible.
- Digital traces should be routed over digital planes only, when possible.
- Digital ground should be connected to chassis ground (bracket and connector shields).
- Digital and analog grounds should be connected near the voltage regulator.

4.3 Latchup Avoidance

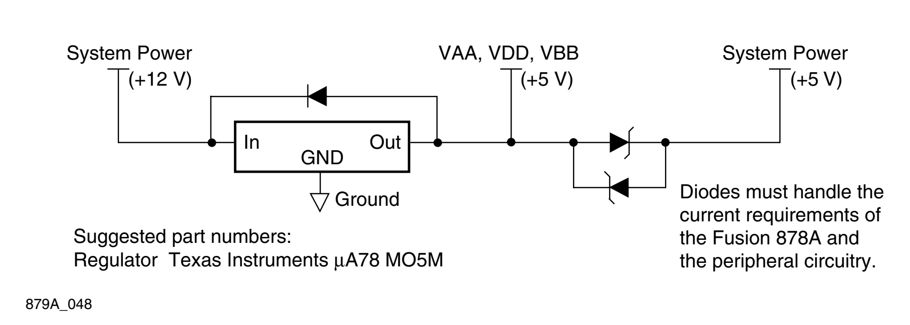
Latchup is possible with all CMOS devices. It is triggered when any signal pin exceeds the voltage on the power pins associated with that pin by more than 0.5 V, or falls below the ground pins associated with that pin by more than 0.5 V. Latchup can also occur if the voltage on any power pin exceeds the voltage on any other power pin by more than 0.5 V.

To avoid latchup of the Fusion 878A, follow these precautions:

- Apply power to the device before or at the same time as you apply power to the interface circuit.
- Connect all VDD, VBB and VAA pins together through a low impedance plane.
- Connect all BGND and AGND pins together through a low impedance plane.
- If you are using a voltage regulator on the digital and/or analog power planes, use protection diodes.

See Figure 4-1 for an illustration of optional regulatory circuitry.

Figure 4-1. Optional Regulatory Circuitry



Suggested part numbers:
Regulator Texas Instruments µA78 MO5M

Diodes must handle the current requirements of the Fusion 878A and the peripheral circuitry.

5.0 Control Register Definitions-Function 0

The Fusion 878A supports two types of address spaces: Function 0 and Function 1. This chapter defines Function 0. The configuration address space includes the predefined PCI configuration registers. The memory address space includes all the local registers used by CN878A to control the remaining portions of the device. Both the PCI configuration address space and the memory address space start at memory location 0x00. The PCI-based system distinguishes the two address spaces based on the Initialization Device Select, PCI address, and command signals that are issued during the appropriate software commands.

5.1 PCI Configuration Space

The PCI configuration space defines the registers used to interface between the host and the PCI local bus. Since the Fusion 878A is a multifunctional device, it operates within two function definitions during a configuration type 0 transaction. Function 0 responds as a multimedia video device. Each function has its own address space. AD[10:8] indicates which function the PCI bus is addressing. AD[10:8] = 000 specifies Function 0. The register definitions in this chapter apply only to Function 0.

The configuration space registers are stored in DWORDs and defined by byte addresses. Therefore, a register one byte in length can have a bit definition other than [7:0] (for example [31:24]), depending on its location in the configuration space. For a discussion on configuration cycle addressing, refer to *PCI Local Bus Specification, Revision 2.2*.

The configuration space is accessible at all times even though it is not typically accessed during normal operation. These registers are normally accessed by the Power On Self Test (POST) code and by the device driver during initialization time. Software will, however, read the status register during normal operation when a PCI bus error occurs and is detected by Fusion 878A.

The configuration space is accessed when the IDSEL pin is high, and AD[1:0] equals 00; otherwise, the cycle is ignored. The configuration register addresses are each offset by four, since AD[1:0] equals 00.

Fusion 878A supports burst R/W cycles. Write operations to reserved, unimplemented, or read-only registers/bits complete normally with the data discarded. Read accesses to reserved or unimplemented registers/bits return a data value equal to 0.

Internal addressing of Fusion 878A registers occurs via AD[7:2] and the byte enable bits of the PCI bus. The 8-bit byte address for each of the following register locations is {AD[7:2], 00}.

CardBus CIS Pointer registers are not implemented in the Fusion 878A. User-definable features, BIST, Cache Line Size, and Expansion ROM Base Address register also are not supported.

This section defines the organization of the registers within the 64-byte predefined header portion of the configuration space. Figure 5-1 illustrates the configuration space header. For details on the PCI bus, refer to the *PCI Local Bus Specification, Revision 2.2*.

Figure 5-1. Function 0 PCI Configuration Space Header

AD[7:2]	31	16	15	0
0x00	Device ID		Vendor ID	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C	Reserved	Header Type 0	Latency Timer	Reserved
0x10	Base Address 0 Register			
0x14	Reserved			
0x18	Reserved			
0x1C				
0x20				
0x24				
0x28	Reserved			
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30	Reserved			
0x34	Reserved			Capabilities Pointer
0x38	Reserved			
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line
0x40	Reserved			Device Control
0x44	VPD Capability			
0x4B	VPD Data			
0x4C	Power Management Capability			
0x50	Power Management Support Registers			

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5.2 PCI Configuration Registers (Header)

The following types are used to specify how the Fusion 878A registers are implemented:

ROx Read only with default value = *x*.
RW Read/Write. All bits initialized to 0 at $\overline{\text{RST}}$, unless otherwise stated.
RW* Same as RW, but data read may not be same as data written.
RR Same as RW, but writing a 1 resets corresponding bit location. Writing a 0 has no effect.

0x00—Vendor and Device ID Register

Bits	Type	Default	Name	Description
[31:16]	RO	0x036E	Device ID	Identifies the particular device or Part ID Code.
[15:0]	RO	0x109E	Vendor ID	Identifies manufacturer of device, assigned by the PCI SIG.

0x04—Command and Status Register

The Command[15:0] register provides control over ability to generate and respond to PCI cycles. When a 0 is written to this register, Fusion 878A is logically disconnected from the PCI bus except for configuration cycles. The unused bits in this register are set to a logical 0. The Status[31:16] register is used to record status information regarding PCI bus related events.

Bits	Type	Default	Name	Description
[31]	RR	0	Detected Parity Error	Set when a parity error is detected, in the address or data, regardless of the Parity Error Response control bit.
[30]	RR	0	Signaled System Error	Set when $\overline{\text{SERR}}$ is asserted.
[29]	RR	0	Received Master Abort	Set when master transaction is terminated with Master Abort.
[28]	RR	0	Received Target Abort	Set when master transaction is terminated with Target Abort.
[27]	RR	0	Signaled Target Abort	Set when target terminates transaction with Target Abort. This occurs when detecting an address parity error.
[26:25]	RO	01	Address Decode Time	Responds with medium $\overline{\text{DEVSEL}}$ timing.
[24]	RR	0	Data Parity Reported	A value of 1 indicates that the bus master asserted $\overline{\text{PERR}}$ during a read transaction or observed $\overline{\text{PERR}}$ asserted by target when writing data to target. The Parity Error Response bit in the command register must have been enabled.
[23]	RO	1	FB2B Capable	Target capable of fast back-to-back transactions.
[20]	RO	1	New Capabilities	A value of 1 indicates that the value read at PCI configuration offset 0x34 is a pointer in configuration space to a linked list of new capabilities.

Bits	Type	Default	Name	Description
[8]	RW	0	$\overline{\text{SERR}}$ enable	A value of 1 enables the $\overline{\text{SERR}}$ driver.
[6]	RW	0	Parity Error Response	A value of 1 enables parity error reporting.
[2]	RW	0	Bus Master	A value of 1 enables Fusion 878A to act as a bus initiator.
[1]	RW	0	Memory Space	A value of 1 enables response to memory space accesses (target decode to memory mapped registers).

0x08—Revision ID and Class Code Register

Bits	Type	Default	Name	Description
[31:8]	RO	0x040000	Class Code	Fusion 878A is a multimedia video device.
[7:0]	RO	0xXX	Revision ID	Current revision

0x0C—Header Type, Latency Timer Register

Bits	Type	Default	Name	Description
[23:16]	RO	0x80	Header type	Multi-function PCI device.
[15:8]	RW	0x00	Latency Timer	The number of PCI bus clocks for the latency timer used by the bus master. Once the latency expires, the master must initiate transaction termination as soon as $\overline{\text{GNT}}$ is removed.

0x10—Base Address 0 Register

Bits	Type	Default	Name	Description
[31:12]	RW	Assigned by CPU at boot-up	Relocatable Memory Pointer	Determine the location of the registers in the 32-bit addressable memory space.
[11:0]	RO	0x008	Memory Usage Specification	Reserve 4 kB of memory-mapped address space for local registers. Address space is pre-fetchable without side effects.

0x2C—Subsystem ID and Subsystem Vendor ID Register

Bits	Type	Default	Name	Description
[31:16]	RW	0x0000	Subsystem ID	Vendor specific.
[15:0]	RW	0x0000	Subsystem Vendor ID	Identify the vendor of the add-on board or subsystem, assigned by PCI SIG.

0x3C—Interrupt Line, Interrupt Pin, Min_Gnt, Max_Lat Register

Bits	Type	Default	Name	Description
[31:25]	RO	0x28	Max_Lat	Requires bus access every 10 μs, at a minimum, in units of 250 ns. Affects the desired settings for the latency timer value.
[24:16]	RO	0x10	Min_Gnt	Requires a minimum grant burst period of 4 μs to empty data FIFO, in units of 250 ns. Affects the desired settings for the latency timer value. Set for 128 DWORDs, with 0 wait states.
[15:8]	RO	0x01	Interrupt Pin	Fusion 878A interrupt pin is connected to $\overline{\text{INTA}}$, the only one usable by a single function device.
[7:0]	RW		Interrupt Line	Communicates interrupt line routing information between the POST code and the device driver. The POST code initializes this register with a value specifying to which input (IRQ) of the system interrupt controller the Fusion 878A interrupt pin is connected. Device drivers can use this value to determine interrupt priority and vector information.

Min_Gnt and Max_Lat values are dependent on target performance (TRDY) and video mode (scale factors and color format). These values were chosen for best case target (0 wait state) and worst-case video delivery (full-resolution 32-bit RGB).

0x34—Capabilities Pointer Register

Bits	Type	Default	Name	Description
[7:0]	RO	0x44	Cap_Ptr	DWORD aligned byte address offset in configuration space to the first item in the list of capabilities.

0x40—Device Control Register

Bits	Type	Default	Name	Description
[7:3]	RO	00000		Reserved
[2]	RW	0	EN_VSFX	Enables VIA/SIS PCI controller compatibility mode for both Functions 0 and 1. 0 = Disable 1 = Enable
[1]	RW	0	EN_TBFX	Enables 430FX PCI controller compatibility mode for both Functions 0 and 1. 0 = Disable 1 = Enable
[0]	RW	0	SVIDS_EN	Enables writes to the Subsystem Vendor ID register for both Functions 0 and 1. 0 = Disable 1 = Enable
NOTE(S): These control bits affect both Function 0 and Function 1.				

0x44—VPD Capability Register

Bits	Type	Default	Name	Description
[31]	RW		VPD_Flag	This flag is set to a value of 1 when the device completes reading and transfer of 4 bytes between the EEPROM and the VPD data register. The flag is reset to 0 when the device completes a 4-byte write transaction. Software initiates R or W transactions by setting this flag to 0 or 1, respectively, when supplying the VPD byte address.
[30:16]	RW		VPD_Adr	Logical byte address of the VPD to be accessed. Only 8 bits supported.
[15:8]	RO	0x4C	VPD_Nxt_Ptr	Pointer to next 'New Capabilities' data structure. A value of 0 indicates there are no more.
[7:0]	RO	0x03	VPD_ID	VPD new capability data structure ID assigned by SIG.

0x48—VPD Data Register

Bits	Type	Default	Name	Description
[31:0]	RW*		VPD Data	Four bytes are always transferred between the VPD data register and the EEPROM. The LSByte...MSByte is transferred from/to VPD_Adr...VPD_Adr+3.

0x4C—Power Management Capability Register

Bits	Type	Default	Name	Description
[31:27]	RO	00000	PMC_PME	PME# cannot be asserted from this function.
[26]	RO	0	PMC_D2	The function does not support the D2 power management state.
[25]	RO	0	PMC_D1	The function does not support the D1 power management state.
[24:22]	RO	000		Reserved.
[21]	RO	1	PMC_DSI	A value of 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.
[20]	RO	0		Reserved.
[19]	RO	0	PMC_PME_Clk	A value of 0 indicates that no PCI clock is required for the function to generate PME#.
[18:16]	RO	010	PMC_Version	Function complies with version 1.1 of the *PCI Power Management Specification*.
[15:8]	RO	0x00	PMC_Nxt_Ptr	Pointer to next 'New Capabilities' data structure. A value of 0 indicates there are no more.
[7:0]	RO	0x01	PMC_ID	PCI Power Management new capability data structure ID assigned by SIG.

0x50—Power Management Support Registers

Bits	Type	Default	Name	Description
[31:24]	RO	0x00	Pwr-Data	This field is used to report the state dependent data requested by Data_Select and scaled by Data_Scale. Optional and not supported.
[23:16]	RO	0x00	PMCSR_BSE	Reserved for bridge support extensions.
[15]	RO	0	PME_Status	Function does not support PME# from $D3_{cold}$.
[14:13]	RO	00	Data_Scale	This field indicates the scaling factor to be used when interpreting the value of the Pwr-Data register. Optional and not supported.
[12:9]	RO	0000	Data_Select	This field selects which data is to be reported through the Pwr-Data register. Optional and not supported.
[8]	RO	0	PME_En	Function does not support PME# from $D3_{cold}$.
[7:2]	RO	000000		Reserved.
[1:0]	RW	00	PowerState*(1)*	This field determines the current power state of a function and supports setting the function into a new power state. 00 = D0 01 = D1 (not supported) 10 = D2 (not supported) 11 = $D3_{hot}$

NOTE(S):
[1] Attempting to set PowerState to D1 or D2 will result in no change of state for that 2-bit field.
2. Bits [15:0] are also known as the Power Management Control/Status Register or PMCSR.

5.3 Local Registers (Memory Mapped)

Fusion 878A's local registers reside in the 4 kB memory addressed space reserved for each function. All of the registers correspond to DWORD or a subset thereof. Local registers may be written to or read through the PCI bus at any time. Internal addressing of the Fusion 878A local registers occurs via AD[11:2] and the byte enable bits of the PCI bus. The local memory-mapped register address locations are specified as 12-bit offsets to the value loaded into the functions memory base address register. The 8-bit byte address for each of the following register locations is {AD[11:2], 0x00}. Any register may be written or read by any combination of the byte enables.

Data to and from the video decoder/scaler registers and VDFC comes from PCI byte lane 0 (AD[7:0]) only. If the upper byte lanes are enabled for reading, the data returned is 0. Thus, each register is separated by a byte address offset of four. All non-used addresses are reserved locations and return an undefined value.

The scaling function needs to be controlled on a field basis to allow for different size/scaled images for preview and capture applications. All registers that affect scaling, translation, and capture on the input side of the FIFO provide for even and odd field values that switch automatically on the internal FIELD signal.

The following types are used to specify how the Fusion 878A registers are implemented:

ROx Read only with default value = *x*.
RW Read/Write. All bits initialized to 0 at $\overline{\text{RST}}$, unless otherwise stated.
RW* Same as RW, but data read may not be same as data written.
RR Same as RW, but writing a 1 resets corresponding bit location. Writing a 0 has no effect.

0x000—Device Status Register (DSTATUS)

Upon reset DSTATUS is initialized to 0x00. COF is the LSB. The COF and LOF status bits hold their values until reset to their default values. The other six bits do not hold their values, but continually output the status.

Bits	Type	Default	Name	Description
[7]	RW	0	PRES	Video Present Status. Video is determined as not present when an input sync is not detected in 31 consecutive line periods. 0 = Video not present. 1 = Video present.
[6]	RW	0	HLOC	Device in H-lock. If HSYNC is found within ±1 clock cycle of the expected position of HSYNC for 32 consecutive lines, this bit is set to a logical 1. Once it is set, if HSYNC is not found within ±1 clock cycle of the expected position of HSYNC for 32 consecutive lines, this bit is set to a logical 0. Writes to this bit are ignored. This bit indicates the stability of the incoming video. While it is an indicator of horizontal locking, some video sources will characteristically vary from line to line by more than one clock cycle so this bit will never be set. 0 = Device not in H-lock. 1 = Device in H-lock.
[5]	RW	0	FIELD	Field Status. This bit reflects whether an odd or even field is being decoded. 0 = Odd field. 1 = Even field.
[4]	RW	0	NUML	This bit identifies the number of lines found in the video stream. This bit is used to determine the type of video input to the Fusion 878A. Before this status bit will change, 32 consecutive fields with the same number of lines are required. 0 = 525 line format (NTSC/PAL-M). 1 = 625 line format (PAL/SECAM).
[3]				Reserved
[2]	RW	0	PLOCK	A logical 1 indicates the PLL is out of lock. Once software has initialized the PLL to run at the desired frequency, this bit should be read and cleared until it is no longer set (up to 100 ms). Then the clock input mode should be switched from XTAL to PLL.
[1]	RW	0	LOF	Luma ADC Overflow. On power-up, this bit is set to 0. If an ADC overflow occurs, the bit is set to a logical 1. It is reset after being written to or a chip reset occurs.
[0]	RW	0	COF	Chroma ADC Overflow. On power-up, this bit is set to 0. If an ADC overflow occurs, the bit is set to a logical 1. It is reset after being written to or a chip reset occurs.

0x004—Input Format Register (IFORM)

Upon reset IFORM is initialized to 0x58. FORMAT(0) is the LSB.

Bits	Type	Default	Name	Description
[7]	RW	0	Reserved	This bit must be set to 0.
[6:5]	RW	10	MUXSEL	Used for software control of video input selection. The Fusion 878A can select between four composite video sources, or three composite sources, and one S-Video source. 00 = Select MUX3 01 = Select MUX2 10 = Select MUX0 11 = Select MUX1
[4:3]	R0	11		Reserved
[2:0]	RW	000	FORMAT	Automatic format detection may be enabled or disabled. The NUML bit is used to determine the input format when automatic format detection is enabled. 000 = Auto format detect enabled 001 = NTSC (M) input format 010 = NTSC without pedestal (Japan) 011 = PAL (B, D, G, H, I) input format 100 = PAL (M) input format 101 = PAL (N) input format 110 = SECAM input format 111 = PAL (N-combination) input format

0x008—Temporal Decimation Register (TDEC)

Upon reset TDEC is initialized to 0x00. DEC_RAT(0) is the LSB. This register enables temporal decimation by discarding a finite number of fields or frames from the incoming video.

Bits	Type	Default	Name	Description
[7]	RW	0	DEC_FIELD	Defines whether decimation is by fields or frames. 0 = Decimate frames. 1 = Decimate fields.
[6]	RW	0	FLDALIGN	Aligns the start of decimation with an even or odd field. 0 = Start decimation on the odd field (an odd field is the first field dropped). 1 = Start decimation on the even field (an even field is the first field dropped).
[5:0]	RW	000000	DEC_RAT	The number of fields or frames dropped out of 60 (NTSC) or 50 (PAL/SECAM) fields or frames. The 0x00 value disables decimation (all video frames and fields are output).

MSB Cropping Register)

0x00C—Even Field (E_CROP)
0x08C—Odd Field (O_CROP)

Upon reset this register is initialized to 0x12. HACTIVE_MSB(0) is the LSB. See the VACTIVE, VDELAY, HACTIVE, and HDELAY registers for descriptions on the operation of this register.

Bits	Type	Default	Name	Description
[7:6]	RW	00	VDELAY_MSB[1]	The most significant two bits of vertical delay register.
[5:4]	RW	01	VACTIVE_MSB	The most significant two bits of vertical active register.
[3:2]	RW	00	HDELAY_MSB	The most significant two bits of horizontal delay register.
[1:0]	RW	10	HACTIVE_MSB	The most significant two bits of horizontal active register.

NOTE(S):
[1] For VDELAY_MSB the E_CROP and O_CROP address pointer is flipped. To write to the even field, VDELAY_MSB bits use the odd field address. To write to the odd field, VDELAY_MSB bits use the even field address.

Vertical Delay Register, Lower Byte

0x090—Even Field (E_VDELAY_LO)
0x010—Odd Field (O_VDELAY_LO)

Upon reset this register is initialized to 0x16. VDELAY_LO(0) is the LSB. This 8-bit register is the lower byte of the 10-bit VDELAY register. The 2 MSBs of VDELAY are contained in the CROP register. VDELAY defines the number of half lines between the trailing edge of VRESET and the start of active video.

Bits	Type	Default	Name	Description
[7:0]	RW	0x16	VDELAY_LO	The LSByte of the vertical delay register.

Vertical Active Register, Lower Byte

0x014—Even Field (E_VACTIVE_LO)
0x094—Odd Field (O_VACTIVE_LO)

Upon reset this register is initialized to 0xE0. VACTIVE_LO(0) is the LSB. This 8-bit register is the lower byte of the 10-bit VACTIVE register. The 2 MSBs of VACTIVE are contained in the CROP register. VACTIVE defines the number of lines used in the vertical scaling process.

Bits	Type	Default	Name	Description
[7:0]	RW	0xE0	VACTIVE_LO	The LSByte of the vertical active register.

Horizontal Delay Register, Lower Byte

0x018—Even Field (E_DELAY_LO)
0x098—Odd Field (O_DELAY_LO)

Upon reset this register is initialized to 0x78. HDELAY_LO(0) is the LSB. This 8-bit register is the lower byte of the 10-bit HDELAY register. The 2 MSBs of HDELAY are contained in the CROP register. HDELAY defines the number of scaled pixels between the falling edge of HRESET and the start of active video.

Bits	Type	Default	Name	Description
[7:0]	RW	0x78	HDELAY_LO	The LSByte of the horizontal delay register. HACTIVE pixels will be output by the chip starting at the fall of HRESET.

Horizontal Active Register, Lower Byte

0x01C—Even Field (E_HACTIVE_LO)
0x09C—Odd Field (O_HACTIVE_LO)

Upon reset it is initialized to 0x80. HACTIVE_LO(0) is the LSB. HACTIVE defines the number of horizontal active pixels per line output by the Fusion 878A. This 8-bit register is the lower byte of the 10-bit HACTIVE register. The two MSBs of HACTIVE are contained in the CROP register.

Bits	Type	Default	Name	Description
[7:0]	RW	0x80	HACTIVE_LO	The LSByte of the horizontal active register.

Horizontal Scaling Register, Upper Byte

0x020—Even Field (E_HSCALE_HI)
0x0A0—Odd Field (O_HSCALE_HI)

Upon reset this register is initialized to 0x02. This 8-bit register is the upper byte of the 16-bit HSCALE register.

Bits	Type	Default	Name	Description
[7:0]	RW	0x02	HSCALE_HI	The MSByte of the horizontal scaling ratio.

Horizontal Scaling Register, Lower Byte

0x024—Even Field (E_HSCALE_LO)
0x0A4—Odd Field (O_HSCALE_LO)

Upon reset this register is initialized to 0xAC. This 8-bit register is the lower byte of the 16-bit HSCALE register.

Bits	Type	Default	Name	Description
[7:0]	RW	0xAC	HSCALE_LO	The LSByte of the horizontal scaling ratio.

0x028—Brightness Control Register (BRIGHT)

Upon reset this register is initialized to 0x00.

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	BRIGHT	The brightness control involves the addition of a two's complement number to the luma channel. Brightness can be adjusted in 255 steps, from –128 to +127. The resolution of brightness change is 1 LSB (0.39% with respect to the full luma range).

Table 5-1. BRIGHT Parameters

Hex Value	Binary Value	Brightness Changed By	
		Number of LSBs	Percent of Full Scale
0x80	1000 0000	–128	–50 %
0x81	1000 0001	–127	–49.6 %
. .	. .	. .	
0xFF	1111 1111	–01	–0.39 %
0x00 [(1)]	0000 0000	00	0 %
0x01	0000 0001	+01	+0.39 %
. .	. .	. .	
0x7E	0111 1110	+126	+49.2 %
0x7F	0111 1111	+127	+49.6 %

NOTE(S):
[(1)] Default Option.

Miscellaneous Control Register

0x02C—Even Field (E_CONTROL)
0x0AC—Odd Field (O_CONTROL)

Upon reset this register is initialized to 0x20. SAT_V_MSB is the LSB.

Bits	Type	Default	Name	Description
[7]	RW	0	LNOTCH	This bit is used to include the luma notch filter. This will output full bandwidth luminance. For monochrome video, the notch filter should not be used. 0 = Enable the luma notch filter 1 = Disable the luma notch filter
[6]	RW	0	COMP	When COMP is set to logical 1, the luma notch is disabled. When COMP is set to logical 0, the C ADC is disabled. 0 = Composite Video 1 = Y/C Component Video
[5]	RW	1	LDEC	The luma decimation filter is used to reduce the high-frequency component of the luma signal. Useful when scaling to CIF resolutions or lower. 0 = Enable luma decimation using selectable H filter 1 = Disable luma decimation
[4]	RW	0	CBSENSE	This bit controls whether the first pixel of a line is a Cb pixel or a Cr pixel. For example, if CBSENSE is low and HDELAY is an even number, the first active pixel output is a Cb pixel. If HDELAY is odd, CBSENSE may be programmed high to produce a Cb pixel as the first active pixel output. 0 = Normal Cb, Cr order 1 = Invert Cb, Cr order
[3]	RW	0	Reserved	This bit should only be written with a logical 0.
[2]	RW	0	CON_MSB	The MSB of the luma gain (contrast) value.
[1]	RW	0	SAT_U_MSB	The MSB of the chroma (u) gain value.
[0]	RW	0	SAT_V_MSB	The MSB of the chroma (v) gain value.

0x030—Luma Gain Register, Lower Byte (CONTRAST_LO)

Upon reset CONTRAST_LO is initialized to 0xD8. CONTRAST_LO(0) is the LSB.

Bits	Type	Default	Name	Description
[7:0]	RW	0xD8	CONTRAST_LO	The CON_MSB bit and the CONTRAST_LO register concatenate to form the 9-bit CONTRAST register. The value in this register is multiplied by the luminance value to provide contrast adjustment.

CONTRAST equals the CON_MSB plus the LSByte of the luma gain (contrast) value.

Table 5-2. CONTRAST Parameters

Decimal Value	Hex Value	Percent of Original Signal
511	0x1FF	236.57 %
510	0x1FE	236.13 %
. .	. .	. .
217	0x0D9	100.46 %
216	0x0D8	100.00 %
. .	. .	. .
128	0x080	59.26 %
. .	. .	. .
1	0x001	0.46 %
0	0x000	0.00 %

0x034—Chroma (U) Gain Register, Lower Byte (SAT_U_LO)

Upon reset SAT_U_LO is initialized to 0xFE. SAT_U_LO(0) is the LSB. SAT_U_MSB in the Miscellaneous CONTROL register, and SAT_U_LO concatenate to create a 9-bit register (SAT_U). Use this register to add a gain adjustment to the U component of the video signal. By adjusting the U and V color components of the video stream the same amount, you adjust the saturation. For normal saturation adjustment, the gain in both the color difference paths must be the same (i.e. the ratio between the value in the U gain register and the value in the V gain register should be kept constant at the default power-up ratio). When changing the saturation, if the SAT_U_MSB bit is altered, take care to ensure that the other bits in the CONTROL register are not affected.

Bits	Type	Default	Name	Description
[7:0]	RW	0xFE	SAT_U_LO	This register is used to add a gain adjustment to the U component of the video signal. By adjusting the U and V color components of the video stream by the same incremental value, you can adjust the saturation.

Table 5-3. (SAT_U_MSB + SAT_U_LO)

Decimal Value	Hex Value	Percent of Original Signal
511	0x1FF	201.18 %
510	0x1FE	200.79 %
. .	. .	. .
255	0x0FF	100.39 %
254	0x0FE	100.00 %
. .	. .	. .
128	0x080	50.39 %
. .	. .	. .
1	0x001	0.39 %
0	0x000	0.00 %

0x038—Chroma (V) Gain Register, Lower Byte (SAT_V_LO)

Upon reset SAT_V_LO is initialized to 0xB4. SAT_V_LO(0) is the LSB. SAT_V_MSB in the Miscellaneous CONTROL register and SAT_V_LO concatenate to create a 9-bit register (SAT_V). Use this register to add a gain adjustment to the V component of the video signal. You adjust the saturation by adjusting the U and V color components of the video stream by the same amount. For normal saturation adjustment, the gain in both the color difference paths must be the same (i.e. the ratio between the value in the U gain register and the value in the V gain register should be kept constant at the default power-up ratio). When changing the saturation, if the SAT_V_MSB bit is altered, take care to ensure that the other bits in the CONTROL register are not affected.

Bits	Type	Default	Name	Description
[7:0]	RW	0xB4	SAT_V_LO	This register is used to add a gain adjustment to the V component of the video signal. You can adjust the saturation by adjusting the U and V color components of the video stream by the same amount.

Table 5-4. SAT_V (SAT_V_MSB + SAT_V_LO)

Decimal Value	Hex Value	Percent of Original Signal
511	0x1FF	283.89 %
510	0x1FE	283.33 %
. .	. .	. .
181	0x0B5	100.56 %
180	0x0B4	100.00 %
. .	. .	. .
128	0x080	71.11 %
. .	. .	. .
1	0x001	0.56 %
0	0x000	0.00 %

0x03C—Hue Control Register (HUE)

Upon reset HUE is initialized to 0x00. HUE(0) is the LSB.

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	HUE	Hue adjustment involves the addition of a two's complement number to the demodulating subcarrier phase. Hue can be adjusted in 256 steps in the range –90° to +89.3°, in increments of 0.7°.
NOTE(S): Not applicable to PAL, SECAM, or Digital Video.				

Table 5-5. HUE Parameters

Hex Value	Binary Value	Subcarrier Reference Changed By	Resulting Hue Changed By
0x80	1000 0000	–90 °	+90 °
0x81	1000 0001	–89.3 °	+89.3 °
. .	. .	. .	. .
0xFF	1111 1111	–0.7 °	+0.7 °
0x00	0000 0000 [(1)]	00 °	00 °
0x01	0000 0001	+0.7 °	–0.7 °
. .	. .	. .	. .
0x7E	0111 1110	+88.6 °	–88.6 °
0x7F	0111 1111	+89.3 °	–89.3 °

NOTE(S):
[(1)] Default Option.

SC Loop Control Register

0x040—Even Field (E_SCLOOP)
0x0C0—Odd Field (O_SCLOOP)

Bits	Type	Default	Name	Description
[7]	RW	0	PEAK	This bit determines whether the normal luma low-pass filters are implemented via the HFILT bits, or the peaking filters are implemented. 0 = Normal luma low pass filtering 1 = Use luma peaking filters
[6]	RW	0	CAGC	This bit controls the Chroma AGC function. When this bit is enabled, Chroma AGC will compensate for non-standard chroma levels. To achieve compensation, multiply the incoming chroma signal by a value in the range of 0.5 to 2.0. 0 = Chroma AGC disabled 1 = Chroma AGC enabled
[5]	RW	0	CKILL	This bit determines whether the low color detector and removal circuitry is enabled. 0 = Low color detection and removal disabled 1 = Low color detection and removal enabled
[4:3]	RW	00	HFILT	These bits control the configuration of the optional 6-tap Horizontal Low-Pass Filter. The auto-format mode determines the appropriate low-pass filter based on the horizontal scaling ratio selected. The LDEC bit in the CONTROL register must be programmed to 0 to use these filters. 00[(1)] = Auto Format. If you select auto format when horizontally scaling between full resolution and half resolution, select no filtering. When scaling between one-half and one-quarter resolution, use the CIF filter. When scaling between one-quarter and one-eighth resolution, use the QCIF filter; and at less than one-eight resolution, use the ICON filter. If you set the PEAK bit to logical 1, the HFILT bits determine which peaking filter is selected. 01 = Maximum full resolution peaking 10 = Minimum CIF resolution peaking 11 = Maximum CIF resolution peaking 00 = Minimum full resolution peaking
[2:0]	RW	00		

NOTE(S):
(1) Default filter mode.

0x044—White Crush Up Register (WC_UP)

This control register may be written to or read by the MPU at any time, and upon reset it is initialized to 0xCF. UPCNT(0) is the least significant bit.

Bits	Type	Default	Name	Description
[7:6]	RW	3	MAJS	These bits determine the majority comparison point for the White Crush Up function. 00 = 3/4 of maximum luma value 01 = 1/2 of maximum luma value 10 = 1/4 of maximum luma value 11 = Automatic
[5:0]	RW	0xF	UPCNT	The value programmed in these bits accumulates once per field or frame, when the majority of the pixels in the active region of the image are below a selected value. The accumulated value determines the extent to which the AGC value needs to be raised in order to keep the SYNC level proportionate with the white level. The UPCNT value is assumed positive, for example: 3F = 63 3E = 62 . . . . 00 = 0

0x048—Output Format Register (OFORM)

Upon reset OFORM is initialized to 0x00. OFORM(0) is the LSB.

Bits	Type	Default	Name	Description
[7]	RW	0	RANGE	Luma Output Range. This bit determines the range for the luminance output on the Fusion 878A. Limit the range when using the control codes as video timing. 0 = Normal operation (Luma range 16–253, chroma range 2–253). Y = 16 is black (pedestal). Cr, Cb = 128 is zero color information. 1 = Full-range Output (Luma range 0–255, chroma range 2–253) Y = 0 is black (pedestal). Cr, Cb = 128 is zero color information.
[6:5]	RW	00	CORE	Luma Coring. These bits control the coring value used by the Fusion 878A. When coring is active and the total luminance level is below the limit programmed into these bits, the luminance signal is truncated to 0. 00 = 0 no coring 01 = 8 10 = 16 11 = 32
[4:0]	RW	00000	Reserved	

Vertical Scaling Register, Upper Byte

0x04C—Even Field (E_VSCALE_HI)
0x0CC—Odd Field (O_VSCALE_HI)

Upon reset this register is initialized to 0x60.

Bits	Type	Default	Name	Description
[7]	RW	0	VSFLDALIGN	Used in conjunction with bit 5 (INT) to align vertical scaling when overlaying fields at CIF resolution (60/50 Hz mode) Bits 7/5 00 = Non-interlaced vertical scaling x1 = Interlaced vertical scaling 10 = Field aligned vertical scaling
[6]	RW	1	COMB	Chroma Comb Enable. This bit determines if the chroma comb is included in the data path. If enabled, a full line store is used to average adjacent lines of color information, reducing cross-color artifacts. 0 = Chroma comb disabled 1 = Chroma comb enabled
[5]	RW	1	INT	Used in conjunction with bit 7 (FLDALIGN) to align vertical scaling when overlaying fields at CIF resolution (60/50 Hz mode) Bits 7/5 00 = Non-interlaced vertical scaling x1 = Interlaced vertical scaling 10 = Field aligned vertical scaling
[4:0]	RW	00000	VSCALE_HI	Vertical Scaling Ratio. These 5 bits represent the most significant portion of the 13-bit vertical scaling ratio register.

Vertical Scaling Register, Lower Byte

0x050—Even Field (E_VSCALE_LO)
0x0D0—Odd Field (O_VSCALE_LO)

Upon reset this register is initialized to 0x00.

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VSCALE_LO	Vertical Scaling Ratio. These 8 bits represent the LSByte of the 13-bit vertical scaling ratio register. They are concatenated with 5 bits in VSCALE_HI. The following equation should be used to determine the value for this register: VSCALE = (0x10000 – { [(scaling_ratio) – 1] × 512 }) + 0x1FFF

0x054—Reserved

A read cycle from this register returns 0x01, and only a write of 0x01 is permitted.

0x5B—Audio Reset Register (ARESET)

Upon reset, ARESET is initialized to 0x00.

Bits	Type	Default	Name	Description
[7]	RW	0	ARESET	This bit must be toggled high and then low to reset the audio circuitry. ARESET must be toggled at least once anytime the audio path is enabled.
[6:0]	RW	000000	Reserved	Must be set to zero for proper orientation.

0x060—AGC Delay Register (ADELAY)

Upon reset, ADELAY is initialized to 0x68.

Bits	Type	Default	Name	Description

[7:0]	RW	0x70	ADELAY	AGC gate delay for back-porch sampling. Use the following equation to determine the value for this register:
				ADELAY = (6.8 µs × 4 × Fsc) + 15
				Example for an NTSC input signal:
				ADELAY = (6.8 µs × 14.32 MHz) + 15 = 112 (0x70)

0x064—Burst Delay Register (BDELAY)

Upon reset, BDELAY is initialized to 0x5D. BDELAY(0) is the LSB.

Bits	Type	Default	Name	Description

[7:0]	RW	0x5D	BDELAY	The burst gate delay for sub-carrier sampling. The following equation should be used to determine the value for this register:
				BDELAY = (6.5 µs × 4 × Fsc)
				Example for an NTSC input signal:
				BDELAY = (6.5 µs × 14.32 MHz) = 93 (0x5D)

0x068—ADC Interface Register (ADC)

Upon reset, ADC is initialized to 0x82. CRUSH is the LSB.

Bits	Type	Default	Name	Description
[7:6]		10		
[5]			Reserved	This bit is reserved and must be set to 0.
[4]	RW	0	AGC_EN	This bit controls the AGC function. If this bit is disabled, REFOUT is not driven and an external reference voltage must be provided. If this bit is enabled, REFOUT is driven to control the A/D reference voltage. 0 = AGC enabled 1 = AGC disabled
[3]	RW	0	CLK_SLEEP	When this bit is at a logical 1, the decoder clock is powered down, but the device registers are still accessible. Recovery time is approximately 1 s to return to capturing video. 0 = Normal clock operation 1 = Shut down the system clock (power down)
[2]	RW	0	Y_SLEEP	This bit enables putting the luma ADC in sleep mode. 0 = Normal Y ADC operation 1 = Sleep Y ADC operation
[1]	RW	1	C_SLEEP	This bit enables putting the chroma ADC in sleep mode. 0 = Normal C ADC operation 1 = Sleep C ADC operation
[0]	RW	0		When the CRUSH bit is high (adaptive AGC), the gain control mechanism monitors the A/Ds for overflow conditions. If an overflow is detected, the REFOUT voltage is increased, which increases the input voltage range on the A/Ds. 0 = Non-adaptive AGC 1 = Adaptive AGC

Video Timing Control Register

0x6C—Even Field (E_VTC)
0xEC—Odd Field (O_VTC)

Upon reset, this register is initialized to 0x00. VFILT(0) is the LSB.

Bits	Type	Default	Name	Description
[7]	RW	0	HSFMT [7:6] 00 = 64 01 = 48 10 = 32 11 = 16	This bit selects between a 32-clock-wide HRESET and the standard 64-clock-wide HRESET. 0 = $\overline{\text{HRESET}}$ is 64 CLKx1 cycles wide 1 = $\overline{\text{HRESET}}$ is 32 CLKx1 cycles wide
[6:3]			Reserved	These bits should be written only with a logical 0.
[2:0]	RW	000	VFILT	These bits control the number of taps in the Vertical Scaling Filter. Choose the number of taps in conjunction with the horizontal scale factor to ensure that the needed data does not overflow the internal FIFO. 000*= 2-tap interpolation only.[1] 001 = 2-tap $\frac{1}{2}(1+Z^{-1})$ and 2-tap interpolation.[2] 010 = 3-tap $\frac{1}{4}(1+2Z^{-1}+Z^{-2})$ and 2-tap interpolation.[3] 011 = 4-tap $\frac{1}{8}(1+3Z^{-1}+3Z^{-2}+Z^{-3})$ and 2-tap interpolation.[3] 100*= 2-tap $\frac{1}{2}(1+Z^{-1})$ [1] 101 = 3-tap $\frac{1}{4}(1+2Z^{-1}+Z^{-2})$ [2] 110 = 4-tap $\frac{1}{8}(1+3Z^{-1}+3Z^{-2}+Z^{-3})$ [3] 111 = 5-tap $\frac{1}{16}(1+4Z^{-1}+6Z^{-2}+4Z^{-3}+Z^{-4})$ [3]

NOTE(S):

[1] Available at all resolutions.

[2] Only available if scaling to less than 385 horizontal active pixels (CIF or smaller).

[3] Only available if scaling to less than 193 horizontal active pixels (QCIF or smaller).

0x07C—Software Reset Register (SRESET)

This command register can be written at any time. Read cycles to this register return an undefined value. A data write cycle to this register resets the video decoder and scaler registers to the default state. Writing any data value into this address resets the device.

0x078—White Crush Down Register

This control register may be written to or read by the MPU at any time, and upon reset is initialized to 0x7F. DNCNT(0) is the least significant bit. This register is programmed with a two's complement number.

[7]	RW	0	VERTEN	0 = Normal operation 1 = Enable vertical sync detection in determining the video presence (PRES) status.
[6]	RW	1	WCFRAME	This bit programs the rate at which the DNCNT and UPCNT values are accumulated. 0 = Once per field 1 = Once per frame
[5:0]	RW	0x22F	DNCNT	The value programmed in these bits accumulates once per field or frame. The accumulated value determines the extent to which the AGC value needs to be lowered in order to keep the SYNC level proportionate to the white level. The DNCNT value is assumed negative. For example: 3F= –1 3E= –2 . . . . 00= –64

0x080—Timing Generator Load Byte (TGLB)

Upon reset, TGLB is initialized to 00.

[7:0]	RW	00		Reading from this address reads only the current byte. The TGC_AI bit must be pulsed by software in order for the SRAM byte location to advance.

0x084—Timing Generator Control (TGCTRL) Register

Upon reset, TGCTRL is initialized to 00.

7			Reserved	Must be written with a logical zero.
[6:5]	RW		TGCKO	GPCLK Output Clock Select 00 = CLKx1 01 = XTAL 0 input 10 = PLL 11 = PLL – inverted
[4:3]	RW		TGCKI	Decoder Input Clock Select. 00 = Normal XTAL 0/XTAL 1 mode 01 = PLL 10 = GPCLK[1] 11 = GPCLK–inverted[1]
2	RW		TGC_AI	Timing Generator Read Address Increment. Active high pulse increments the read address.
1	RW		GPC_AR	Timing Generator Address Reset.
0	RW	00		0 = Read/write mode 1 = Enable timing generator/read mode

NOTE(S):

[1] The entire decoder will be running off the external clock GPCLK when GPCLK is activated. Therefore, the decoder functionality is subject to a halt condition if the input port is disconnected. A clock detect circuit will allow the decoder to fall back on either the PLL or the XTAL, whichever is enabled via PLL_I. If the PLL has been put to sleep, then the decoder will fall back on the XTAL0 input. The VPRES status condition indicates the status of the clock detect output when in Digital Video Input mode, which is monitoring GPCLK.

You should set up the PLL to run at the same frequency as the GPCLK input, so that if the digital camera is disconnected, blue-field timing will run properly.

0x0B0—Total Line Count Register (VTOTAL_LO)

If this register is set to non-zero, the 10-bit value will change the decoder's vertical synchronization line count from the normal 525/625.

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VTOTAL_LO	The LSByte of the 10-bit VTOTAL register, which sets the expected number of horizontal video lines to: VTOTAL_LO = (number of horizontal video lines / frame) – 1

0x0B4—Total Line Count Register (VTOTAL_HI)

Bits	Type	Default	Name	Description
[7:2]	RW	000000		Reserved
[1:0]	RW	00	VTOTAL_HI	The 2 MSBs of the 10-bit VTOTAL register, which sets the expected number of horizontal video lines to: VTOTAL_HI = (number of horizontal video lines / frame) – 1

0x0D4—Color Format Register (COLOR_FMT)

Bits	Type	Default	Name	Description
[7:4]	RW	0000	COLOR_ODD	Odd Field Color Format 0000 = RGB32 0001 = RGB24 0010 = RGB16 0011 = RGB15 0100 = YUY2 4:2:2 0101 = BtYUV 4:1:1 0110 = Y8 (Gray scale) 0111 = RGB8 (Dithered) 1000 = YCrCb 4:2:2 Planar (YUV12) 1001 = YCrCb 4:1:1 Planar (YUV9) 1010 = Reserved 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Raw 8X Data 1111 = Reserved
[3:0]	RW	0000	COLOR_EVEN	Even Field Color Format 0000 = RGB32 0001 = RGB24 0010 = RGB16 0011 = RGB15 0100 = YUY2 4:2:2 0101 = BtYUV 4:1:1 0110 = Y8 (Gray scale) 0111 = RGB8 (Dithered) 1000 = YCrCb 4:2:2 Planar 1001 = YCrCb 4:1:1 Planar 1010 = Reserved 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Raw 8X Data 1111 = Reserved

0x0D8—Color Control Register (COLOR_CTL)

A value of 1 enables byte swapping of data entering the FIFO. B3[31:24] is swapped with B2[23:16] and B1[15:8] is swapped with B0[7:0].

Bits	Type	Default	Name	Description
[7]	RW	0	EXT_FRMRATE	When the GPIO port is in SPI-16 input mode, this bit supplies NTSC(0)/PAL(1) which selects the gamma ROM.
[6]	RW	0	COLOR_BARS	A value of 1 enables a color bars pattern at the input of the VDFC block.
[5]	RW	0	RGB_DED	A value of 0 enables error diffusion for RGB16/RGB15 modes. A value of 1 disables it.
[4]	RW	0	GAMMA	A value of 0 enables gamma correction removal. The inverse gamma correction factor of 2.2 or 2.8 is applied and auto-selected by the respective mode NTSC/PAL. A value of 1 disables gamma correction removal.
[3]	RW	0	WSWAP_ODD	WordSwap Odd Field. A value of 1 enables word swapping of data entering the FIFO. W2[31:16] is swapped with W0[15:0].
[2]	RW	0	WSWAP_EVEN	WordSwap Even Field. A value of 1 enables word swapping of data entering the FIFO. W2[31:16] is swapped with W0[15:0].
[1]	RW	0	BSWAP_ODD	ByteSwap Odd Field. A value of 1 enables byte swapping of data entering the FIFO. B3[31:24] is swapped with B2[23:16], and B1[15:8] is swapped with B0[7:0].
[0]	RW	0	BSWAP_EVEN	ByteSwap Even Field. A value of 1 enables byte swapping of data entering the FIFO. B3[31:24] swapped with B2[23:16], and B1[15:8] is swapped with B0[7:0].

0x0DC—Capture Control Register (CAP_CTL)

Bits	Type	Default	Name	Description
[7:5]	RW	000	Reserved	These bits should be written only with a logical 0.
[4]	RW	0	DITH_FRAME	0 = Dither matrix applied to consecutive lines in a field 1 = Full frame mode
[3]	RW	0	CAPTURE_VBI_ODD	A value of 1 enables VBI data to be captured into the FIFO during the odd field.
[2]	RW	0	CAPTURE_VBI_EVEN	A value of 1 enables VBI data to be captured into the FIFO during the even field.
[1]	RW	0	CAPTURE_ODD	A value of 1 enables odd capture and allows VDFC to write data to FIFOs during the odd field.
[0]	RW	0	CAPTURE_EVEN	A value of 1 enables even capture and allows VDFC to write data to FIFOs during the even field.

0x0E0—VBI Packet Size Register (VBI_PACK_SIZE)

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_PKT_LO	Lower 8 bits for the number of raw data DWORDS (four 8-bit samples) to capture while in VBI capture mode.

0x0E4—VBI Packet Size / Delay Register (VBI_PACK_DEL)

Bits	Type	Default	Name	Description
[7:2]	RW	000000	VBI_HDELAY	The number of CLKx1's to delay from the trailing edge of HRESET before starting VBI line capture.
[1]	RW	0	EXT_FRAME	A value of 1 extends the frame output capture region to include the 10 lines prior to the default VACTIVE region.
[0]	RW	0	VBI_PKT_HI	Upper bit for the number of raw data DWORDS (four 8-bit samples) to capture while in VBI capture mode.

0x0E8—Field Capture Counter Register (FCAP)

Upon reset FCAP is initialized to 00.

Bits	Type	Default	Name	Description
[7:0]	RW[1]	0x00	FCNTR	Counts field transitions when any CAPTURE bit is set.
NOTE(S): [1] Any write to this register resets the contents to 0.				

0x0F0—PLL Reference Multiplier Register (PLL_F_LO)

Upon reset this register is initialized to 00.

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	PLL_F_LO	Lower byte of PLL Frequency register.

0x0F4—PLL Reference Multiplier Register (PLL_F_HI)

Upon reset this register is initialized to 00.

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	PLL_F_HI	Upper byte of PLL Frequency register.

0x0F8—Integer Register (PLL-XCI)

Upon reset this register is initialized to 00.

Bits	Type	Default	Name	Description
[7]	RW	0	PLL_X	PLL Ref XTAL pre-divider. 0 = Use 1 for pre-divider 1 = Use 2 for pre-divider
[6]	RW	0	PLL_C	PLL VCO post-divider. 0 = Use 6 for post-divider 1 = Use 4 for post-divider
[5:0]	RW	000000	PLL_I	PLL_I input[1]. Range 6–63. If set to 0x00, then the PLL sleeps.

NOTE(S):
[1] Minimum allowable PLL_I. PLL_F = 6.8000h.

0x0FC—Digital Video Signal Interface Format (DVSIF) Register

Upon reset, DVSIF is initialized to 0x000.

[7]	RW	0	—	Reserved
[6]	RW	0	VSIF_BCF	Enables bypass of chroma filters. Use when HSCALE is set to 0. 1 = Bypass chroma filters 0 = Use chroma filters
[5]	RW	0	VSIF_ESO	Enable Sync output for synchronizing video Input. 1 = Syncs are outputs 0 = Syncs are inputs
[4:3]	RW	00	SVREF	00 = HS/VS aligned with Cb 01 = HS/VS aligned with Y0 10 = HS/VS aligned with Cr 11 = HS/VS aligned with Y1
[2:0]	RW	000		001 = CCIR 656 010 = Reserved 011 = Reserved 100 = External HSYNC, VSYNC 101 = External HSYNC, Field 110 = Reserved 111 = Reserved

0x100—Interrupt Status Register (INT_STAT)

This register provides status of pending interrupt conditions. To clear the interrupts, read this register and write the same data back. A 1 in the write data clears the particular register bit. The interrupt/status bits can be polled at any time.

Bits	Type	Default	Name	Description
[31:28]	RO		RISCS	Set when RISC status set bits are set in the RISC instruction. Reset when RISC status reset bits are set. Status only, no interrupt.
[27]	RO		RISC_EN	A value of 0 indicates the DMA controller is currently disabled. Status only, no interrupt.
[26]	RO		Reserved	—
[25]	RO		RACK	Set when I^{2}C operation is completed successfully. Otherwise, if the receiver does not acknowledge, this bit will be reset when I2CDONE (bit 8) is set. Status only, no interrupt.
[24]	RO		FIELD	0 = Odd field 1 = Even field. Status only, no interrupt
[23:20]		0000	Reserved	—
[19]	RR	0	SCERR	Set when the DMA EOL sync counter overflows. This is a severe error which requires the software to restart the field capture process. Also set when SYNC codes do not match in the data/instruction streams.
[18]	RR	0	OCERR	Set when the DMA controller detects a reserved/unused opcode in the instruction sequence, or reserved/unused sync status in a SYNC instruction. In general, this includes any detected RISC instruction error.
[17]	RR	0	PABORT	Set whenever the initiator receives a MASTER or TARGET ABORT.
[16]	RR	0	RIPERR	Set when a data parity error is detected (Parity Error Response must be set) while the initiator is reading RISC instructions. RISC_ENABLE is reset by the target to stop the DMA immediately.
[15]	RR	0	PPERR	Set when a parity error is detected on the PCI bus for any of the transactions—R/W, address/data phases, initiator/target, issued/sampled $\overline{\text{PERR}}$—regardless of the Parity Error Response bit. All parity errors are serious except for data written to display.
[14]	RR	0	FDSR	FIFO Data Stream Resynchronization occurred. The number of pixels, lines, or modes passing through FIFO does not match RISC program expectations.
[13]	RR	0	FTRGT	Set when a pixel data FIFO overrun condition results in the master's terminating the transaction due to excessive target latency.
[12]	RR	0	FBUS	Set when a pixel data FIFO overrun condition is being handled by dropping as many DWORDs as needed, indicating bus access latencies are long.
[11]	RR	0	RISCI	Set when the IRQ bit in the RISC instruction is set.
[10]	RO	0	Reserved	—
[9]	RR	0	GPINT	Set upon the programmable edge or level of the GPINTR pin.
[8]	RR	0	I2CDONE	Set when an I^{2}C read or write operation has completed.
[7:6]	RO	0	Reserved	—

Bits	Type	Default	Name	Description
[5]	RR	0	VPRES	Set when the analog video signal input changes from present to absent or vice versa.
[4]	RR	0	HLOCK	Set if the horizontal lock condition changes on incoming video.
[3]	RR	0	OFLOW	Set when an overflow is detected in the luma or chroma ADCs.
[2]	RR	0	HSYNC	Set when the analog input begins a new video line, or at the GPIO HRESET leading edge.
[1]	RR	0	VSYNC	Set when FIELD changes on the analog input or GPIO input.
[0]	RR	0	FMTCHG	Set when a video format change is detected; i.e., the analog input changes from NTSC to PAL or vice versa.

0x104—Interrupt Mask Register (INT_MASK)

Bits	Type	Default	Name	Description
[23:0]	RW	0x000000	INT_MASK	A value of 1 enables the interrupt bit. The bits correspond to the same bits in the Interrupt Status register. Unmasking a bit may generate an interrupt immediately due to a previously pending condition. The PCI $\overline{\text{INTA}}$ is level sensitive. It remains asserted until the device driver clears or masks the pending request.

0x10C—GPIO and DMA Control Register (GPIO_DMA_CTL)

Bits	Type	Default	Name	Description
[15]	RW	0	GPINTC	A value of 0 selects the direct non-inverted/inverted input from GPINTR to go to the interrupt status register. A value of 1 selects the rising edge detect of the GPINTI programmed input.
[14]	RW	0	GPINTI	A value of 1 inverts the input from the GPINTR pin immediately after the input buffer.
[13]				Reserved. Must be logical 0.
[12:11]	RW	00	GPIOMODE	00 = Normal GPIO port 01 = SPI output mode 10 = SPI input mode 11 = Reserved
[10]	RW	0	GPCLKMODE	A value of 1 enables CLKx1 to be output on GPCLK. A value of 0 disables the output and enables GPCLK to supply the internal pixel clock during SPI-16 input mode; otherwise this pin is assumed to be inactive.
[9:8]	RW	00	Reserved	This bit should only be written with a logical 0.
[7:6]	RW	00	PLTP23	Planar mode trigger point for FIFO2 and FIFO3. 00 = 4 DWORDs 01 = 8 DWORDs 10 = 16 DWORDs 11 = 32 DWORDs
[5:4]	RW	00	PLTP1	Planar mode trigger point for FIFO1. 00 = 4 DWORDs 01 = 8 DWORDs 10 = 16 DWORDs 11 = 32 DWORDs
[3:2]	RW	00	PKTP	Packed mode FIFO Trigger Point. The number of DWORDs in the FIFOs in total before the DMA controller begins to burst data onto the PCI bus. 00 = 4 DWORDs 01 = 8 DWORDs 10 = 16 DWORDs 11 = 32 DWORDs
[1]	RW	0	RISC_ENABLE	A value of 1 enables the DMA controller to process pixel data flow instructions beginning at the RISC program start address.
[0]	RW	0	FIFO_ENABLE	A value of 1 enables the data FIFO, whereas 0 flushes or resets it.

0x110—I2C Data/Control Register

Bits	Type	Default	Name	Description
[31:24]	RW	—	I2CDB0	First byte sent in an I^{2}C transaction. Typically this will be the base or chip 7-bit address and the R/$\overline{W}$ bit.
[23:16]	RW	—	I2CDB1	Second byte sent in an I^{2}C write transaction, usually a sub-address.
[15:8]	RW	—	I2CDB2	Third byte sent in an I^{2}C write transaction, usually the data byte. After a read transaction, this byte register will contain the data read from the slave.
[7]	RW	0	I2CMODE	I^{2}C mode. 0 = Software mode 1 = Hardware mode
[6]	RW	0	I2CRATE	I^{2}C timing frequency. 0 = 99.2 kHz mode 1 = 396.8 kHz mode
[5]	RW	0	I2CNOSTOP	I^{2}C stop mode. 0 = Transmits stop at end of transaction 1 = Does not transmit stop at end of transaction. Holds SCL low.
[4]	RW	0	I2CNOS1B	I^{2}C start mode. 0 = Transmits START or repeated START transactions. The R/W status from bit 24 is saved for any future 1 byte transactions. 1 = Enables 1 byte read or write without START
[3]	RW	0	I2CSYNC	I^{2}C synchronization. 0 = Disallows the slave to insert wait states 1 = Allows the slave to insert bit-level clock wait states
[2]	RW	0	I2CW3BRA	Number of bytes sent and master/slave acknowledge. This bit has no meaning when I2CNOS1B (bit 4) is high during a write transaction. 0 = Writes transaction of 2 bytes I2CDB(0-1). During a 1-byte read transaction (I2CNOS1B is high), master sends a NACK to end the reads from the slave. 1 = Writes transaction of 3 bytes I2CDB(0-2). During a 1-byte read transaction (I2CNOS1B is high), master sends an ACK after reading the data byte.
[1]	RW	1	I2CSCL	A value of 1 releases the SCL output, and a 0 forces the SCL output low. This bit must be set to a 1 during hardware mode. This override is for direct software control of the bus. Reading this bit provides access to the buffered SCL input pin.
[0]	RW	1	I2CSDA	A value of 1 releases the SDA output, and a 0 forces the SDA output low. This bit must be set to a 1 during hardware mode. This override is for direct software control of the bus. Reading this bit provides access to the buffered SDA input pin.

0x114—RISC Program Start Address Register (RISC_STRT_ADD)

Bits	Type	Default	Name	Description
[31:0]	RW	0x00000000	RISC_IPC	Base address for the RISC program. Standard 32-bit memory space byte address, although the software must DWORD-align by setting the lowest two bits to 00. The DMA controller begins executing instructions at this address when RISC_ENABLE is set; i.e., the RISC program counter is loaded with this pointer at the rising edge of RISC_ENABLE.

0x118—GPIO Output Enable Control Register (GPIO_OUT_EN)

Bits	Type	Default	Name	Description
[23:0]	RW	0x000000	GPOE	Writes to this register provide data to the output buffer enables. A value of 1 enables the driver.

0x120—RISC Program Counter Register (RISC_COUNT)

Bits	Type	Default	Name	Description
[31:0]	RO	—	RISC_PC	The current value of the RISC program counter. This may be slightly ahead of the current instruction due to pre-fetching instructions into the queue.

0x200–0x2FF—GPIO Data I/O Register (GPIO_DATA)

Bits	Type	Default	Name	Description
[23:0]	RW	—	GPDATA	Writes to this register provide data to the output buffers. Read data is from the input buffer. Data from this register can only be read if output enables are set and GPIOMODE is set to normal.

6.0 Control Register Definitions–Function 1

This chapter defines Function 1 address spaces. As in the previous chapter, the configuration address space includes the pre-defined PCI configuration registers. The memory address space includes all the local registers used by Fusion 878A to control the remaining portions of the device. Both the PCI configuration address space and the memory address space start at memory location 0x00. The PCI-based system distinguishes the two address spaces based on the Initialization Device Select, PCI address, and command signals that are issued during the appropriate software commands.

6.1 PCI Configuration Space

The PCI configuration space defines the registers used to interface between the host and the PCI local bus. Function 1 responds as a multimedia device. Each function has its own address space. AD[10:8] indicates which function the PCI bus is addressing. AD[10:8] = 001 specifies Function 1. The register definitions in this chapter apply only to Function 1.

The configuration space registers are described in the previous chapter. For a discussion on configuration cycle addressing, refer to Section 3.6.4.1 of the *PCI Local Bus Specification, Revision 2.2*.

The configuration space is accessible at all times even though it is not typically accessed during normal operation. These registers are normally accessed by the Power On Self Test (POST) code and by the device driver during initialization time. Software will, however, read the status register during normal operation when a PCI bus error occurs and is detected by Fusion 878A.

The configuration space is accessed when the IDSEL pin is high, and AD[1:0] equals 00; otherwise, the cycle is ignored. The configuration register addresses are each offset by 4, since AD[1:0] equals 00.

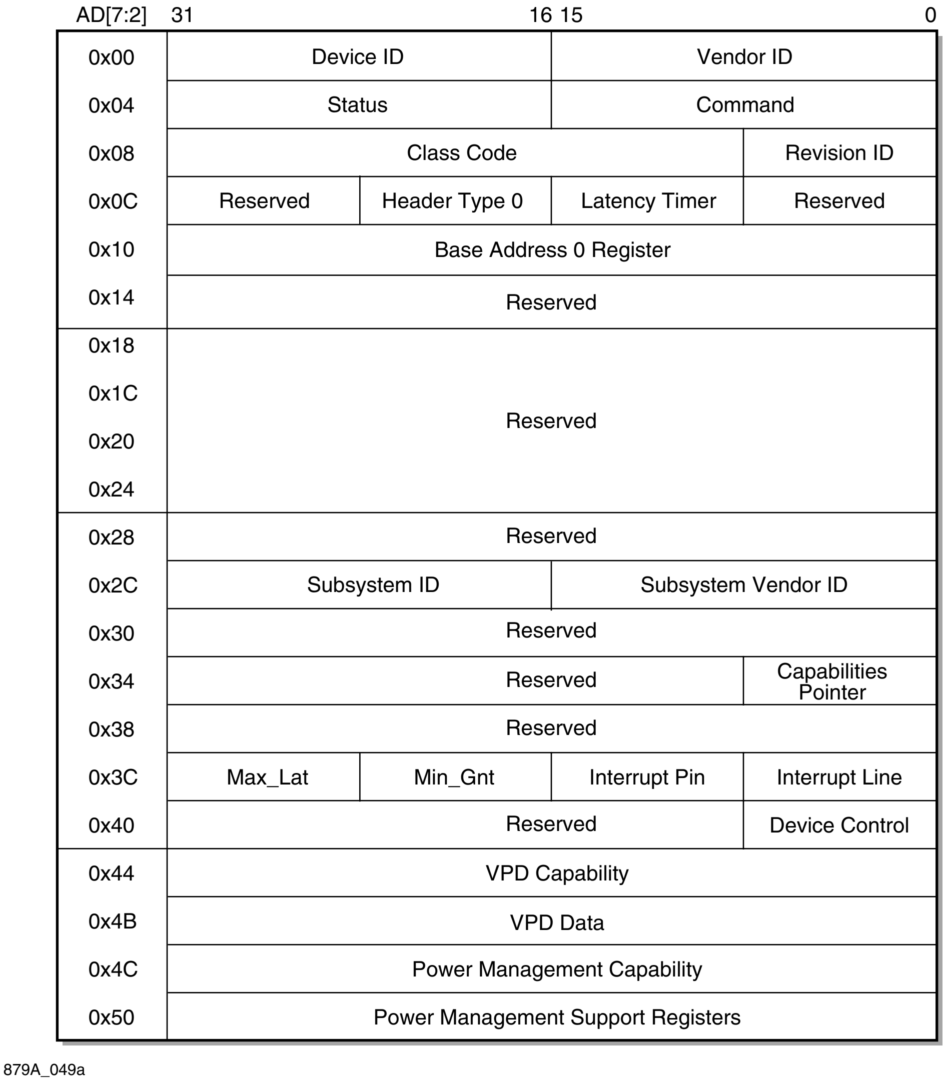
Fusion 878A supports burst R/W cycles. Write operations to reserved, unimplemented, or read-only registers/bits complete normally with the data discarded. Read accesses to reserved or unimplemented registers/bits return a data value equal to 0.

Internal addressing of Fusion 878A registers occurs via AD[7:2] and the byte enable bits of the PCI bus. The 8-bit byte address for each of the following register locations is {AD[7:2], 00}.

CardBus CIS Pointer registers are not implemented in the Fusion 878A. User-definable features, BIST, Cache Line Size, and Expansion ROM Base Address register are also not supported.

This section defines the organization of the registers within the 64-byte predefined header portion of the configuration space. Figure 6-1 shows the configuration space header. For details on the PCI bus, refer to the *PCI Local Bus Specification, Revision 2.2*.

Figure 6-1. Function 1 PCI Configuration Space Header



AD[7:2]	31	16	15	0
0x00	Device ID		Vendor ID	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C	Reserved	Header Type 0	Latency Timer	Reserved
0x10	Base Address 0 Register			
0x14	Reserved			
0x18 0x1C 0x20 0x24	Reserved			
0x28	Reserved			
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30	Reserved			
0x34	Reserved			Capabilities Pointer
0x38	Reserved			
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line
0x40	Reserved			Device Control
0x44	VPD Capability			
0x4B	VPD Data			
0x4C	Power Management Capability			
0x50	Power Management Support Registers			

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6.2 PCI Configuration Registers (Header)

The following types specify how the Fusion 878A registers are implemented:

ROx	Read only with default value = *x*
RW	Read/Write. All bits initialized to 0 at $\overline{\text{RST}}$, unless otherwise stated.
RW*	Same as RW, but data read may not be the same as data written.
RR	Same as RW, but writing a 1 resets the corresponding bit location. Writing a 0 has no effect.

0x00—Vendor and Device ID Register

Bits	Type	Default	Name	Description
[31:16]	RO	0x0878	Device ID	Identifies the particular device or Part ID Code.
[15:0]	RO	0x109E	Vendor ID	Identifies manufacturer of device, assigned by the PCI SIG.

0x04—Command and Status Register

The Command[15:0] register provides control over ability to generate and respond to PCI cycles. When a 0 is written to this register, Fusion 878A is logically disconnected from the PCI bus except for configuration cycles. The unused bits in this register are set to a logical 0. The Status[31:16] register is used to record status information regarding PCI bus related events.

Bits	Type	Default	Name	Description *(1 of 2)*
[31]	RR	0	Detected Parity Error	Set when a parity error is detected, in the address or data, regardless of the Parity Error Response control bit.
[30]	RR	0	Signaled System Error	Set when $\overline{\text{SERR}}$ is asserted.
[29]	RR	0	Received Master Abort	Set when master transaction is terminated with Master Abort.
[28]	RR	0	Received Target Abort	Set when master transaction is terminated with Target Abort.
[27]	RR	0	Signaled Target Abort	Set when target terminates transaction with Target Abort. This occurs when detecting an address parity error.
[26:25]	RO	01	Address Decode Time	Responds with medium $\overline{\text{DEVSEL}}$ timing.
[24]	RR	0	Data Parity Reported	A value of 1 indicates that the bus master asserted $\overline{\text{PERR}}$ during a read transaction or observed $\overline{\text{PERR}}$ asserted by target when writing data to target. The Parity Error Response bit in the command register must have been enabled.
[23]	RO	1	FB2B Capable	Target capable of fast back-to-back transactions.
[20]	RO	1	New Capabilities	A value of 1 indicates that the value read at PCI configuration offset 0x34 is a pointer in configuration space to a linked list of new capabilities.

Bits	Type	Default	Name	Description *(2 of 2)*
[8]	RW	0	$\overline{\text{SERR}}$ enable	A value of 1 enables the $\overline{\text{SERR}}$ driver.
[6]	RW	0	Parity Error Response	A value of 1 enables parity error reporting.
[2]	RW	0	Bus Master	A value of 1 enables Fusion 878A to act as a bus initiator.
[1]	RW	0	Memory Space	A value of 1 enables response to memory space accesses (target decode to memory-mapped registers).

0x08—Revision ID and Class Code Register

Bits	Type	Default	Name	Description
[31:8]	RO	0x048000	Class Code	Fusion 878A is a multimedia other device.
[7:0]	RO	0xXX	Revision ID	Current revision

0x0C—Header Type Register

Bits	Type	Default	Name	Description
[23:16]	RO	0x80	Header Type	Multi-function PCI device.

0x0C—Latency Timer Register

Bits	Type	Default	Name	Description
[15:8]	RW	0x00	Latency Timer	The number of PCI bus clocks for the latency timer used by the bus master. Once the latency expires, the master must initiate transaction termination as soon as $\overline{\text{GNT}}$ is removed.

0x10—Base Address 0 Register

Bits	Type	Default	Name	Description
[31:12]	RW	Assigned by CPU at boot-up	Relocatable Memory Pointer	Determines the location of the registers in the 32-bit addressable memory space.
[11:0]	RO	0x008	Memory Usage Specification	Reserves 4 kB of memory-mapped address space for local registers. Address space is pre-fetchable without side effects.

0x2C—Subsystem ID and Subsystem Vendor ID Register

Bits	Type	Default	Name	Description
[31:16]	RW	0x0000	Subsystem ID	Vendor specific.
[15:0]	RW	0x0000	Subsystem Vendor ID	Identifies the vendor of the add-on board or subsystem assigned by PCI SIG.

0x34—Capabilities Pointer Register

Bits	Type	Default	Name	Description
[7:0]	RO	0x44	Cap_Ptr	DWORD-aligned byte address offset in configuration space to the first item in the list of capabilities.

0x3C—Interrupt Line, Interrupt Pin, Min_Gnt, Max_Lat Register

Bits	Type	Default	Name	Description
[31:24]	RO	0xFF	Max_Lat	Requires bus access every 64 µs, at a minimum, in units of 250 ns. Affects the desired settings for the latency timer value. This register is set to the max value even though the audio can tolerate up to 287 µs bus access latency (a 0 setting would indicate no latency requirements).
[23:16]	RO	0x04	Min_Gnt	Requires a minimum grant burst period of 1 µs to empty data FIFO, in units of 250 ns. Affects the desired settings for the latency timer value. Set for 32 DWORDs, 33 MHz, with 0 wait states.
[15:8]	RO	0x01	Interrupt Pin	Fusion 878A interrupt pin is connected to $\overline{\text{INTA}}$, the only one usable by a single function device.
[7:0]	RW		Interrupt Line	The Interrupt Line register communicates interrupt line routing information between the POST code and the device driver. The POST code initializes this register with a value specifying to which input (IRQ) of the system interrupt controller the Fusion 878A interrupt pin is connected. Device drivers can use this value to determine interrupt priority and vector information.

0x40—Device Control Register

Bits	Type	Default	Name	Description
[7:3]	RO	00000		Reserved
[2]	RW	0	EN_VSFX	Enables VIA/SIS PCI controller compatibility mode for both Functions 0 and 1. 0 = Disable 1 = Enable
[1]	RW	0	EN_TBFX	Enables 430FX PCI controller compatibility mode for both Functions 0 and 1. 0 = Disable 1 = Enable
[0]	RW	0	SVIDS_EN	Enables writes to the Subsystem Vendor ID register for both Functions 0 and 1. 0 = Disable 1 = Enable
NOTE(S): These control bits affect both Function 0 and Function 1.				

0x44—VPD Capability Register

Bits	Type	Default	Name	Description
[31]	RW	—	VPD_Flag	This flag is set to a value of 1 when the device completes the reading and transfer of 4 bytes between the EEPROM and the VPD data register. The flag is reset to 0 when the device completes a 4-byte write transaction. SW initiates R or W transactions by setting this flag to 0 or 1 respectively when supplying the VPD byte address.
[30:16]	RW	—	VPD_Adr	Logical byte address of the VPD to be accessed. Only 8 bits supported.
[15:8]	RO	0x4C	VPD_Nxt_Ptr	Pointer to next ‘New Capabilities’ data structure. A value of 0 indicates there are no more.
[7:0]	RO	0x03	VPD_ID	VPD new capability data structure ID assigned by SIG.

0x48—VPD Data Register

Bits	Type	Default	Name	Description
[31:0]	RW*	—	VPD Data	Always transfers 4 bytes between the VPD data register and the EEPROM. The LSByte...MSByte is transferred from/to VPD_Adr...VPD_Adr+3.

0x4C—Power Management Capability Register

Bits	Type	Default	Name	Description
[31:27]	RO	00000	PMC_PME	PME# cannot be asserted from this function.
[26]	RO	0	PMC_D2	This function does not support the D2 power management state.
[25]	RO	0	PMC_D1	This function does not support the D1 power management state.
[24:22]	RO	000	—	Reserved
[21]	RO	1	PMC_DSI	A value of 1 indicates that this function requires a device-specific initialization sequence following transition to the D0 uninitialized state.
[20]	RO	0	—	Reserved
[19]	RO	0	PMC_PME_Clk	A value of 0 indicates that no PCI clock is required for the function to generate PME#.
[18:16]	RO	010	PMC_Version	Complies with version 1.1 of the *PCI Power Management Specification*.
[15:8]	RO	0x00	PMC_Nxt_Ptr	Pointer to next ‘New Capabilities’ data structure. A value of 0 indicates there are no more.
[7:0]	RO	0x01	PMC_ID	PCI Power Management new capability data structure ID assigned by SIG.

0x50—Power Management Support Register

Bits	Type	Default	Name	Description
[31:24]	RO	0x00	Pwr-Data	This field is used to report the state-dependent data requested by Data_Select and scaled by Data_Scale. Optional and not supported.
[23:16]	RO	0x00	PMCSR_BSE	Reserved for bridge support extensions.
[15]	RO	0	PME_Status	Function does not support PME# from $D3_{cold}$.
[14:13]	RO	00	Data_Scale	This field indicates the scaling factor to be used when interpreting the value of the Pwr-Data register. Optional and not supported.
[12:9]	RO	0000	Data_Select	This field selects which data is to be reported through the Pwr-Data register. Optional and not supported.
[8]	RO	0	PME_En	Function does not support PME# from $D3_{cold}$.
[7:2]	RO	000000	—	Reserved
[1:0]	RW	00	PowerState[(1)]	This field determines the current power state of a function and supports setting the function into a new power state. 00 = D0 01 = D1 (not supported) 10 = D2 (not supported) 11 = $D3_{hot}$

NOTE(S):

[(1)] Attempting to set PowerState to D1 or D2 will result in no change of state for that 2-bit field.

2. Bits [15:0] are also known as the Power Management Control/Status Register or PMCSR.

6.3 Local Registers (Memory Mapped)

Fusion 878A's local registers reside in the 4 kB memory-addressed space reserved for each function. All of the registers correspond to DWORDs or a subset thereof. The local registers may be written to or read through the PCI bus at any time. Internal addressing of the Fusion 878A local registers occurs via AD[11:2] and the byte enable bits of the PCI bus. The local memory-mapped register address locations are specified as 12-bit offsets to the value loaded into the function's memory-base address register. The 8-bit byte address for each of the following register locations is {AD[11:2], 0x00}. Any register may be written or read by any combination of the byte enables.

The following types specify how the Fusion 878A registers are implemented:

ROx	Read only with default value = *x*
RW	Read/Write. All bits initialized to 0 at $\overline{\text{RST}}$, unless otherwise stated.
RW*	Same as RW, but data read may not be the same as data written.
RR	Same as RW, but writing a 1 resets the corresponding bit location. Writing a 0 has no effect.

0x100—Interrupt Status Register (INT_STAT)

This register provides the status of pending interrupt conditions. To clear the interrupts, read this register, then write the same data back. A 1 in the write data clears the particular register bit. The interrupt /status bits can be polled at any time.

Bits	Type	Default	Name	Description
[31:28]	RO	—	RISCS	Set when RISC status set bits are set in the RISC instruction. Reset when RISC status reset bits are set. Status only, no interrupt.
[27]	RO	—	RISC_EN	A value of 0 indicates the DMA controller is currently disabled. Status only, no interrupt.
[26]	RO	—	—	Reserved
[25]	RO	—	—	Reserved
[24]	RO	—	—	Reserved
[23:20]	RO	0000	—	Reserved
[19]	RR	0	SCERR	Set when the DMA EOL sync counter overflows. This is a severe error which requires the software to restart the field capture process. Also set when SYNC codes do not match in the data/instruction streams.
[18]	RR	0	OCERR	Set when the DMA controller detects a reserved/unused opcode in the instruction sequence, or reserved/unused sync status in a SYNC instruction. In general, this includes any detected RISC instruction error.
[17]	RR	0	PABORT	Set whenever the initiator receives a MASTER or TARGET ABORT.
[16]	RR	0	RIPERR	Set when a data parity error is detected (Parity Error Response must be set) while the initiator is reading RISC instructions. RISC_ENABLE is reset by the target to stop the DMA immediately.
[15]	RR	0	PPERR	Set when a parity error is detected on the PCI bus for any of the transactions, R/W, address/data phases, initiator/target, or issued/sampled $\overline{\text{PERR}}$, regardless of the Parity Error Response bit. All parity errors are serious except for data written to display.
[14]	RR	0	FDSR	Set when FIFO Data Stream Resynchronization occurs. The number of pixels, lines, or modes passing through FIFO does not match RISC program expectations.
[13]	RR	0	FTRGT	Set when a pixel data FIFO overrun condition results in the master, terminating the transaction due to excessive target latency.
[12]	RR	0	FBUS	Set when a pixel data FIFO overrun condition is being handled by dropping as many DWORDs as needed, indicating bus access latencies are long.
[11]	RR	0	RISCI	Set when the IRQ bit in the RISC instruction is set.
[10]	RO	0		Reserved
[9]	RO	0		Reserved
[8]	RO	0		Reserved
[7:6]	RO	0		Reserved
[5]	RO	0		Reserved
[4]	RO	0		Reserved

Bits	Type	Default	Name	Description
[3]	RR	0	OFLOW	Set when an overflow is detected in audio A/D nominal range.
[2]	RO	0		Reserved
[1]	RO	0		Reserved
[0]	RO	0		Reserved

0x104—Interrupt Mask Register (INT_MASK)

Bits	Type	Default	Name	Description
[23:0]	RW	0x000000	INT_MASK	A value of 1 enables the interrupt bit. The bits correspond to the same bits in the Interrupt Status register. Unmasking a bit may generate an interrupt immediately due to a previously pending condition. The PCI $\overline{\text{INTA}}$ is level sensitive. It remains asserted until the device driver clears or masks the pending request.

0x10C—Audio Control Register (GPIO_DMA_CTL)

Bits	Type	Default	Name	Description
[31:28]	RW	0000	A_GAIN	Audio input gain control offering 16 discrete linear steps from 0.5 to 3.0. See Table 2-12, *Gain Control*.
[27]	RW	0	A_G2X	Audio gain boost. 0 = Normal gain setting as specified in A_GAIN (0.5 V_{rms} standard input). 1 = Adds +6 dB input signal boost from pre-amp.
[26]	RW	0	A_PWRDN	Analog audio power-down. 0 = No power-down 1 = Power-down the analog audio section
[25:24]	RW	00	A_SEL	Audio select. 00 = STV (tv tuner audio input) 01 = SFM (FM audio input) 10 = SML (MIC/line audio input) 11 = SMXC
[23]	RW	0	DA_SCE	Specifies which edge of ASCLK to sample for ADATA bits. 0 = Rising edge 1 = Falling edge
[22]	RW	0	DA_LRI	This bit has two uses. The rising edge of ALRCK identifies either the right or left sample in digital audio mode. (The falling edge identifies the opposite sample.) 0 = Left sample 1 = Right sample In data packet mode, indicates the edge of ALRCK to use as the frame sync. 0 = Rising edge 1 = Falling edge

Bits	Type	Default	Name	Description
[21]	RW	0	DA_MLB	Selects most significant or LSB format for ADATA 0 = MSB first for I^{2}S format 1 = LSB first for Sony format
[20:16]	RW	00000	DA_LRD	Specifies how many ASCLK clocks to delay from the rising edge of ALRCK before sampling the internal parallel audio data.
[15]	RW	0	DA_DPM	Specifies mode of 3-wire digital audio input interface. 0 = Digital audio mode 1 = Data packet frame synchronized mode
[14]	RW	0	DA_SBR	Specifies number of bits that the digital audio decimation filter will transfer out of the final stage. 0 = 16-bit samples 1 = Rounded 8-bit samples
[13]	RW	0	DA_ES2	Enables Digital Decimation Filter (DDF). 0 = Disables DDF 1 = Enable DDF stage 2 and associated decimation factor of 2
[12]	RW	0	DA_LMT	Enables detection of audio data 0x8000 (0x80) and replacement with 0x8001 (0x81). Mode determined by bit 14, DA_SBR. 0 = Disables 1 = Enables
[11:8]	RW	0000	DA_SDR	Specifies the DDF first stage and decimation rate. Range: 4 to 15.
[7:6]	RW	00	DA_IOM	Specifies audio digital audio I/O mode. 00 = DA_IOM_AFE (audio A/D) 01 = DA_IOM_DA (digital audio in) 10 = Reserved 11 = Reserved
[5]	RW	0	DA_APP	Enables Parallel Data mode (DA_IOM = 01) or High Speed Serial mode (DA_IOM = 00). 0 = Disables 1 = Enables Parallel (DA_IOM = 01) / High Speed Serial (DA_IOM = 00).
[4]	RW	0	ACAP_EN	Enables audio capture into the audio FIFO. 0 = Disables 1 = Enables
[3:2]	RW	00	PKTP	Packed mode FIFO trigger point. Specifies number of DWORDs in the FIFO before the DMA controller begins to burst data onto the PCI bus. 00 = PKTP_4 4 DWORDs 01 = PKTP_8 8 DWORDs 10 = PKTP_16 16 DWORDs 11 = Reserved
[1]	RW	0	RISC_ENABLE	Enables the audio DMA controller to process audio sample data flow instructions beginning at the RISC program start address. 0 = Disables 1 = Enables
[0]	RW	0	FIFO_ENABLE	Enables the audio data FIFO. 0 = Flushes/resets audio data FIFO 1 = Enables audio data FIFO

0x110—Audio Packet Lengths Register

Bits	Type	Default	Name	Description
[23:16]	RW	0x00	AFP_LEN	Number of audio lines in an audio field: max value 255.
[15:10]	—	—	—	Reserved
[11:0]	RW	0x000	ALP_LEN	Number of bytes in an audio line: max value 4095.

0x114—RISC Program Start Address Register (RISC_STRT_ADD)

Bits	Type	Default	Name	Description
[31:0]	RW	0x00000000	RISC_IPC	Base address for the RISC program. Standard 32-bit memory space byte address, although the software must DWORD-align by setting the lowest 2 bits to 00. The DMA controller begins executing pixel instructions at this address when RISC_ENABLE is set. For example, the RISC program counter is loaded with this pointer at the rising edge of RISC_ENABLE.

0x120—RISC Program Counter Register (RISC_COUNT)

Bits	Type	Default	Name	Description
[31:0]	RO	—	RISC_PC	The current value of the RISC program counter. This may be slightly ahead of the current instruction due to pre-fetching instructions into the queue.

7.0 Parametric Information

7.1 DC Electrical Parameters

DC electrical parameters are specified in Tables 7-1 through 7-3.

Table 7-1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply — Analog	V_{AA}, V_{BB}	4.75	5.00	5.25	V
Power Supply — Digital	V_{DD}	4.75	5.00	5.25	V
Maximum Δ $\|V_{DD} - V_{AA}\|$	—	—	—	0.5	V
MUX0, MUX1, MUX2, and MUX3 Input Range (AC coupling required)	—	0.5	1.00	2.00	V
CIN Amplitude Range (AC coupling required)	—	0.5	1.00	2.00	V
STV, SFM, SML Input Range (AC coupling required)	—	—	0.5	1.00	V_{RMS}
Ambient Operating Temperature	T_A	0	—	+70	°C

Table 7-2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
V_{AA} (measured to AGND)	V_{AA}, V_{BB}	—	7.00	V
V_{DD} (measured to GND)	V_{DD}	—	7.00	V
Voltage on any signal pin[(1)]	—	DGND – 0.5	V_{DD} + 0.5	V
Analog Input Voltage	—	AGND – 0.5	V_{AA} + 0.5	V
Ambient Operating Temperature	T_A	0	+70	°C
Storage Temperature	T_S	–65	+150	°C
Junction Temperature	T_J	—	+125	°C
Vapor Phase Soldering (15 Seconds)	T_{VSOL}	—	+220	°C

NOTE(S):

[(1)] Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V or drops below ground by more than +0.5 V can induce destructive latchup.

Table 7-3. DC Characteristics (1 of 2)

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
PCI Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	—	V_{DD} + 0.5	V
Input Low Voltage (TTL)	V_{IL}	–0.5	—	0.8	V
GPIO Input					
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.5	V
Input Low Voltage	V_{IL}	–0.5	—	0.8	V
I^2C Input					
Input High Voltage	V_{IH}	0.7 VDD	—	V_{DD} + 0.5	V
Input Low Voltage	V_{IL}	–0.5	—	0.3 VDD	V
Hysteresis	V_{hys}	0.2	—		V
Input High Current (V_{In} = .9 V_{DDMAX})	I_{IH}	—	—	10	µA
Input Low Current (V_{IN} = 0.4 V)	I_{IL}	—	—	–10	µA
Input High Voltage (XTI)	V_{IH}	3.5	—	V_{DD} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	–0.5	—	1.5	V

***Table 7-3. DC Characteristics** (2 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
Input High Current (V_{IN} = 2.7 V	I_{IH}	—	—	70	µA
Input Low Current (V_{IN} = 0.5 V)	I_{IL}	—	—	–70	µA
Input Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}	—	5	—	pF
Digital Outputs					
PCI Outputs					
Output High Voltage (I_{OH} = –2 mA)	V_{OH}	2.4	—	V_{DD}	V
Output Low Voltage (I_{OL} = 6 mA)	V_{OL}	—	—	0.55	V
GPIO					
Output High Voltage (I_{OH} = –1.2 mA)	V_{OH}	2.4	—	V_{DD}	V
Output Low Voltage (I_{OL} = 6 mA)	V_{OL}	—	—	0.4	V
3-State Current	I_{OZ}	—	—	10	µA
Output Capacitance	C_O	—	5	—	pF
I^2C Output					
Output Low Voltage (I_{OL} = 3 mA)	V_{OL}	—	—	0.4	V
Analog Pin Input Capacitance	C_A	—	5	—	pF

7.2 AC Electrical Parameters

AC electrical parameters are specified in Tables 7-4 through 7-7. Timing diagrams for clock, GPIO, and JTAG are provided in Figures 7-1 through 7-2, respectively. (See also Figure 3-13, *GPIO Timing Diagram*, and Table 3-4, *GPIO SPI Mode Timing Parameters*.)

Table 7-4. Clock Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
8 × NTSC F_{SC} Rate (50 ppm source required)	F_S	28.63493	28.63636	28.63779	MHz
XTI Input:					
Cycle Time	1	—	34.92	—	ns
High Time	2	14	—	—	ns
Low Time	3	14	—	—	ns

Figure 7-1. Clock Timing Diagram

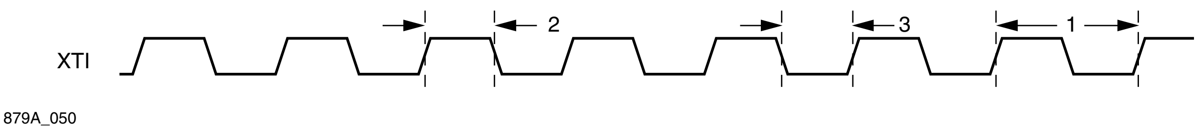


Table 7-5. Power Supply Current Parameters

Parameter	Symbol	Min	Typ	Max	Units
Supply Current					
$V_{AA} = V_{DD} = 5.0$ V, $F_{S2} = 28.64$ MHz, T = 25 °C			240	—	mA
$V_{AA} = V_{DD} = 5.25$ V, $F_{S2} = 35.47$ MHz, T = 70 °C			—	320	mA
$V_{AA} = V_{DD} = 5.25$ V, $F_{S2} = 35.47$ MHz, T = 0 °C			—	330	mA
Supply Current, Power Down			75	—	mA

Table 7-6. JTAG Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
TMS, TDI setup time	10		2		ns
TMS, TDI hold time	11		2		ns
TCK asserted to TDO valid	12		15		ns
TCK asserted to TDO driven	13		14		ns
TCK negated to TDO three-stated	14		85		ns
TCK low time	15	25			ns
TCK high time	16	25			ns

Figure 7-2. JTAG Timing Diagram

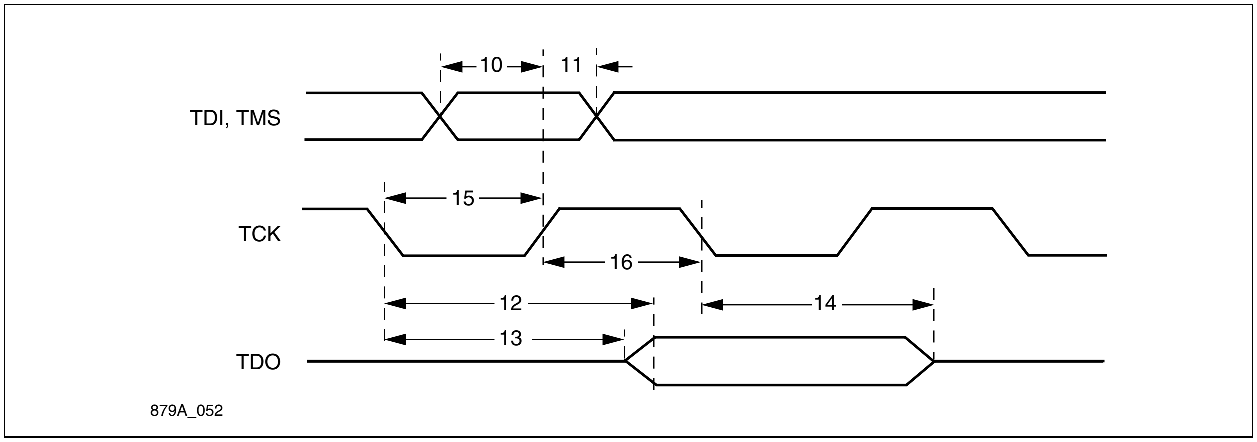


Table 7-7. Decoder Performance Parameters

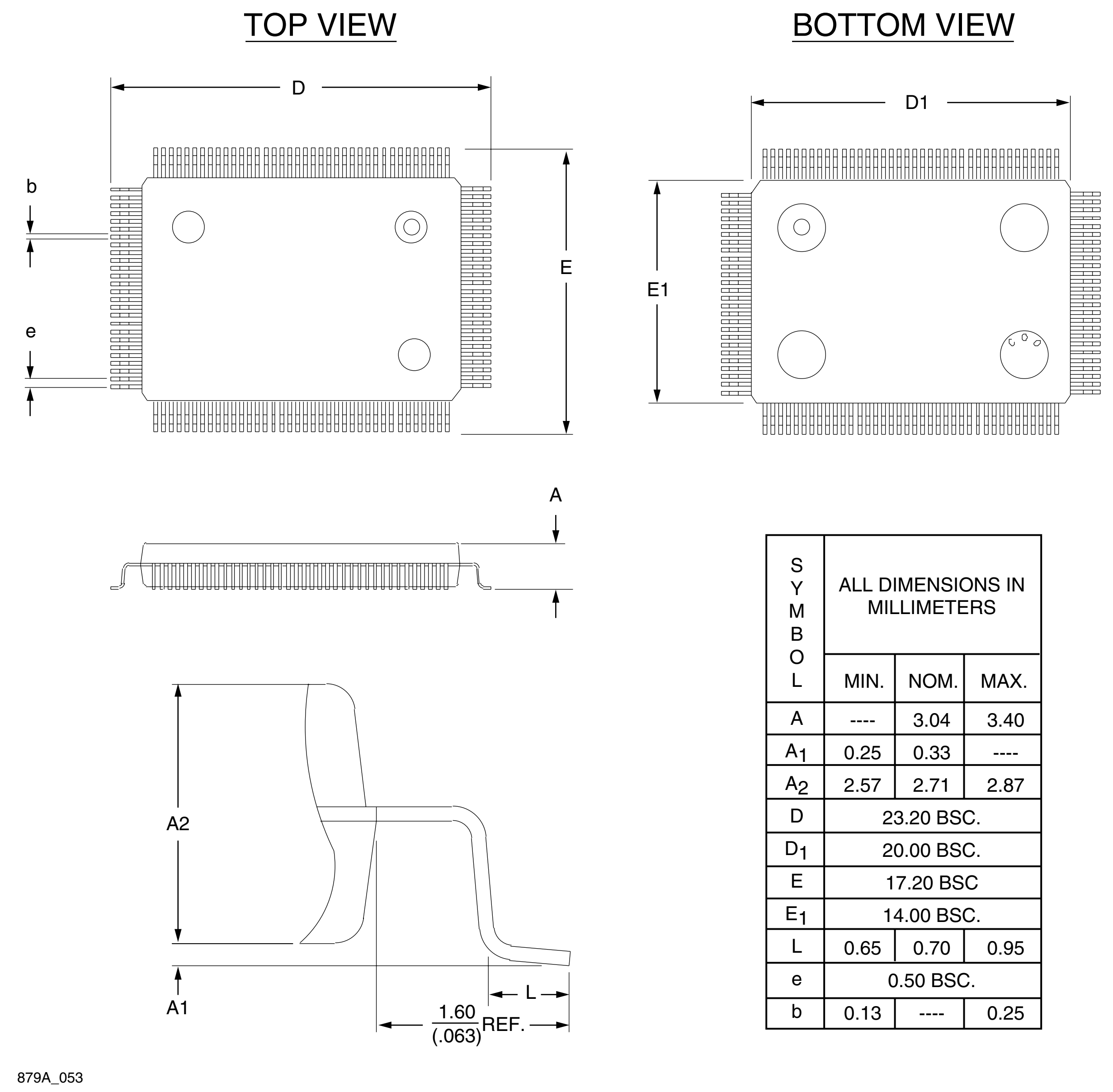
Parameter	Symbol	Min	Typ	Max	Units
Horizontal Lock Range				±7	% of Line Length
Fsc, Lock-in Range		±800			Hz
Gain Range		–6		6	dB

NOTE(S): Test conditions (unless otherwise specified): “Recommended Operating Conditions.” TTL input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. Pixel and control data loads ≤ 30 pF and ≥ 10 pF. GPCLK load ≤ 50 pF. See *PCI Specification Revision 2.2* for PCI timing parameters.

7.3 Package Mechanical Drawing

Figure 7-3 provides a mechanical drawing of the 128-pin PQFP package.

Figure 7-3. 128-pin PQFP Package Mechanical Drawing



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	----	3.04	3.40
A_1	0.25	0.33	----
A_2	2.57	2.71	2.87
D	23.20 BSC.		
D_1	20.00 BSC.		
E	17.20 BSC		
E_1	14.00 BSC.		
L	0.65	0.70	0.95
e	0.50 BSC.		
b	0.13	----	0.25

Appendix A. Acronym List

The acronym list does not include names of pins, registers, or bits.

A/D	Analog-to-Digital
ACGC	Automatic Chrominance Gain Control
ACPI	Advanced Configuration And Power Interface
ADC	Analog to Digital Conversion
AF	Audio Frequency
AFE	Audio Front End
AGC	Automatic Gain Control
ASCII	American Standards Code for Information Interchange
BIOS	Basic Input/Output System
BSDL	Boundary Scan Descriptive Language
BTSC-MTS	Broadcast Television Systems Committee—Multichannel Television Sound
CCIR 601	[A Recommendation From The International Radio Communications Committee]
CIF	Common Interchange
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
DAP	Digital Audio Packetizer
DDF	Digital Decimation Filter
DMA	Direct Memory Access
DWORD	Double Word
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FAFULL	FIFO Almost Full
FIFO	First In First Out
FM	Frequency Modulation
fps	Frames Per Second
Fsc	Frequency of Subcarrier

GFX	Graphics Controller
GPIO	General Purpose Input/output
I^{2}C	Inter-integrated Circuit
IC	Integrated Circuit
ID	Identification
IEEE	Institute of Electrical and Electronic Engineers
INT	Integer
ITU	International Telecommunications Union
JTAG	Joint Test Action Group
LPF	Low Pass Filter
LSB	Least Significant Bit
LSByte	Least Significant Byte
MIC	Microphone
MPU	Microprocessing Unit
MSB	Most Significant Bit
MSByte	Most Significant Byte
MUX	Multiplexer/multiplex
NTSC	National Television Standards Committee [an American video standard]
Opcode	Operational Code
PAL	[A European video standard]
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PLL	Phase Lock Loop
POST	Power-on Self Test
PQFP	Plastic Quad Flat Pack
QCIF	Quarter
RC	Resister Capacitor
RGB	Red, Green, Blue
RISC	Reduced Instruction Set Computer
SECAM	[A European video standard]
SIG	Special Interest Group
SPI	Synchronous Pixel Interface
sync	Synchronizing Signal
TAP	Test Access Port
TTL	Transistor–transistor Logic
VBI	Vertical Blanking Interval

VCR	Video Cassette Recorder
VDFC	Video Data Format Conversion
VFE	Video Front End
VPD	Vital Product Data
VTC	Video Timing Controller
Y/C	Luminance And Chrominance

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