STANDARD MICROSYSTEMS CORPORATION
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# FDC37C661
# FDC37C662

# 2.88MB Super I/O Floppy Disk Controllers

## FEATURES

- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Hardware/Socket Compatible with FDC37C651 and FDC37C652
  - Advanced Digital Data Separator
  - Software and Register Compatible with SMC's Proprietary 82077AA Compatible Core
  - Vertical Recording Format Support
  - 16 Byte FIFO
  - Two 16450 Compatible UARTs
  - One Bidirectional Parallel Port (FDC37C661 Only)
  - ChiProtect™ Circuitry on Parallel Port
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - IDE Interface
  - Game Port Select Logic (FDC37C662 Only)
  - Supports Four Floppy Drives Directly
  - 24 mA AT Bus Drivers
  - **Low Power CMOS 0.8μ Design**
- Licensed CMOS 765B Floppy Disk Controller Core
  - Supports Vertical Recording Format
  - 100% IBM® Compatibility
  - Detects All Overrun and Underrun Conditions
  - 48 mA Drivers and Schmitt Trigger Inputs
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - Uses SMC®'s Proven SuperCell™ Technology
- Enhanced Digital Data Separator
  - SMC Proven Technology
  - Low Cost Implementation - 24 MHz Crystal
    - No Filter Components Required
  - Ease of Test and Use, Lower System Cost, and Reduced Board Area
  - 1 Mb/s, 500 Kb/s, 300 Kb/s, 250 Kb/s Data Rates
  - Supports Floppy Disk Drives and Tape Drives
  - Programmable Precompensation Modes
  - Uses SMC's Proven SuperCell Technology
- Serial Ports
  - INS8250-B and NS16450 Compatible UARTs
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - Uses SMC's Proven SuperCell Technology
- Parallel Port
  - IBM PC/XT®, PC/AT® and PS/2™ Compatible Enhanced Bidirectional Parallel Port (FDC37C661 Only)
  - Incorporates ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - 24 mA Output Drivers
  - Uses SMC's Proven SuperCell Technology
- IDE Interface
  - On-Chip Decode and Select Logic Compatible with IBM PC/XT and PC/AT Embedded Hard Disk Drives
  - Uses SMC's Proven SuperCell Technology
- 100 Pin QFP Package

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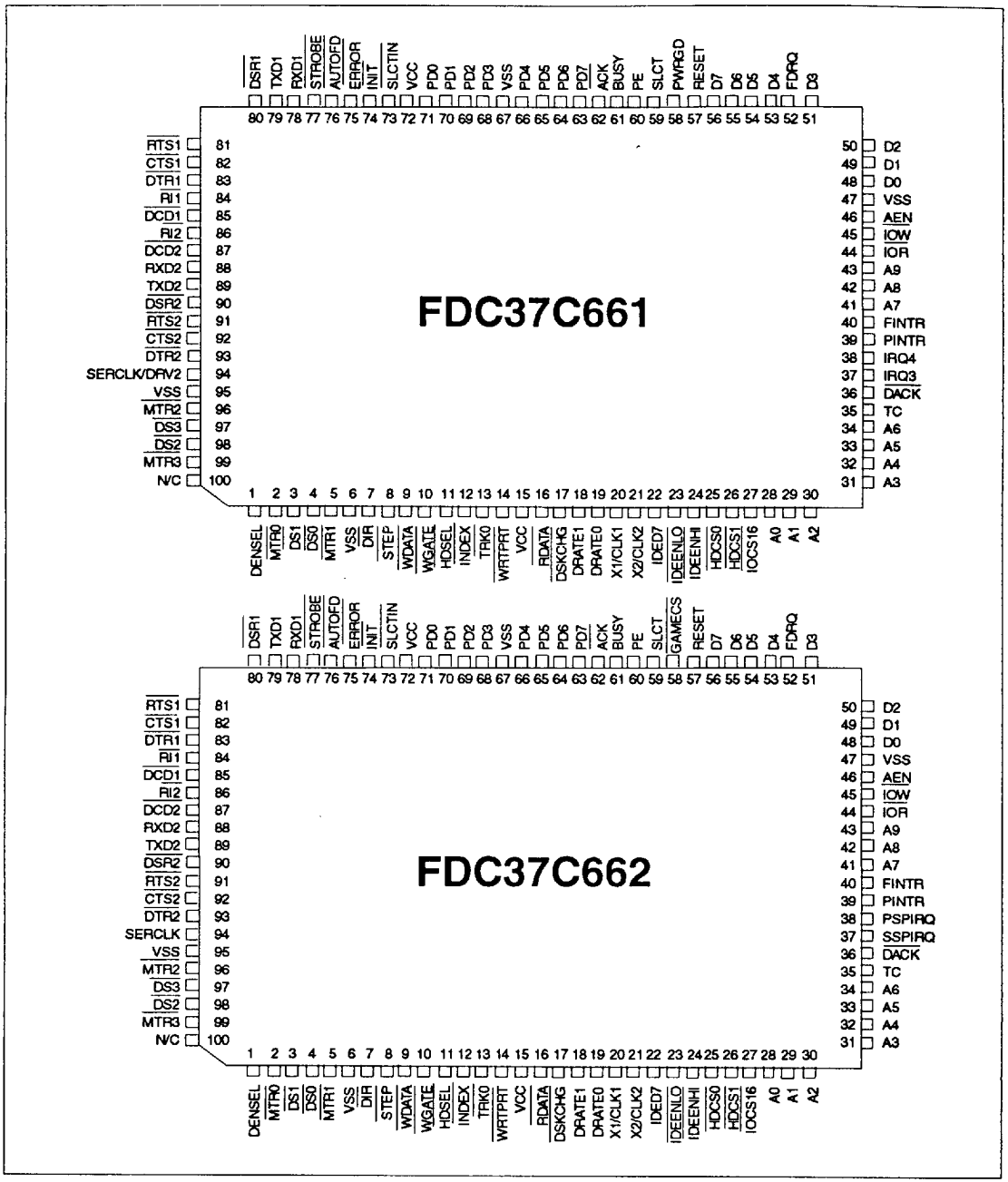
NOTE: This data sheet corresponds to Revision H of the FDC37C661/FDC37C662. The revision letter is denoted by the first character of the date code. For specification changes, if any, for revisions other than Revision H, please contact SMC.

## PIN CONFIGURATION



## GENERAL DESCRIPTION

The SMC FDC37C661 and FDC37C662 2.88MB Super I/O Floppy Disk Controller ICs utilize SMC's proven SuperCell technology for increased product reliability and functionality. The FDC37C661 is optimized for motherboard applications while the FDC37C662 is oriented towards controller card applications. Both devices support 1 Mb/s data rates for vertical recording operation. The FDC37C661 and FDC37C662 are hardware compatible with the FDC37C651 and FDC37C652.

The FDC37C661 and FDC37C662 incorporate SMC's true CMOS 765B floppy disk controller, advanced digital data separator, 16 byte FIFO, two 16450 compatible UARTs, one bidirectional parallel port with ChiProtect circuitry, IDE interface, on-chip 24 mA AT bus drivers, game port chip select (FDC37C662 only), and four floppy direct drive support. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMC advanced digital data separator incorporates SMC's patented data separator technology allowing for ease of testing and use. Both on-chip UARTs are compatible with the INS8250-B and NS16450. The parallel port, as well as the IDE interface and game port select logic, are compatible with IBM PC/XT and PC/AT architectures. The FDC37C661 and FDC37C662 incorporate sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The FDC37C661 Floppy Disk Controller incorporates Software Configurable Logic (SCL) for ease of use. Use of the SCL feature allows programmable system configuration of key functions such as the FDC, parallel port, game port and UARTs. The parallel port ChiProtect prevents damage caused by the printer being powered when the FDC37C661 or FDC37C662 is unpowered.

The FDC37C661 and FDC37C662 do not require any external filter components and are, therefore, easy to use and offer lower system cost and reduced board area. The FDC37C661 and FDC37C662 are software and register compatible with SMC's proprietary 82077AA core.

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| | | HOST PROCESSOR INTERFACE | | |
| 48-51<br>53-56 | Data Bus 0-7 | D0-D7 | I/O24 | The data bus connection used by the host microprocessor to transmit data to and from the FDC37C661. These pins are in a high-impedance state when not in the output mode. |
| 44 | $\overline{\text{I/O Read}}$ | $\overline{\text{IOR}}$ | I | This active low signal is issued by the host microprocessor to indicate a read operation. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 45 | I/O Write | $\overline{IOW}$ | I | This active low signal is issued by the host microprocessor to indicate a write operation. |
| 46 | Address Enable | AEN | I | Active high Address Enable indicates DMA operations on the host data bus. Used internally to qualify appropriate address decodes. |
| 28-34<br>41-43 | I/O Address | A0-A9 | I | These host address bits determine the I/O address to be accessed during $\overline{IOR}$ and $\overline{IOW}$ cycles. These bits are latched internally by the leading edge of $\overline{IOR}$ and $\overline{IOW}$. |
| 52 | FDC DMA Request | FDRQ | O24 | This active high output is the DMA request for byte transfers of data to the host. This signal is cleared on the last byte of the data transfer by the $\overline{DACK}$ signal going low (or by $\overline{IOR}$ going low if $\overline{DACK}$ was already low as in demand mode). |
| 36 | $\overline{DMA\ Acknowledge}$ | $\overline{DACK}$ | I | An active low input acknowledging the request for a DMA transfer of data. This input enables the DMA read or write internally. |
| 35 | Terminal Count | TC | I | This signal indicates to the FDC37C661 that data transfer is complete. TC is only accepted when $\overline{DACK}$ is low. In AT and PS/2 Model 30 modes, TC is active high and in PS/2 mode, TC is active low. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 38 | Serial Port Interrupt Request | IRQ4 | O24 | FDC37C661 (Motherboard application): IRQ4 is the interrupt from the Primary Serial Port (PSP) or Secondary Serial Port (SSP) when the PSP or SSP have their address programmed as COM1 or COM3 (as defined in the Configuration Registers). The appropriate interrupt from the Serial Port is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset. |
| | Primary Serial Port Interrupt | PSPIRQ | O24 | FDC37C662 (Adapter application): PSPIRQ is a source of PSP interrupt. Externally, it should be connected to either IRQ3 or IRQ4 on PC/AT via jumpers. |
| 37 | Serial Port Interrupt Request | IRQ3 | O24 | FDC37C661 (Motherboard application): IRQ3 is the interrupt from the Primary Serial Port (PSP) or secondary Serial Port (SSP) when the PSP or SSP have their address programmed as COM2 or COM4 (as defined in the Configuration Registers). The appropriate interrupt from the Serial Port is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset. |
| | Secondary Serial Port Interrupt | SSPIRQ | O24 | FDC37C662 (Adapter application): SSPIRQ is a source of SSP interrupt. Externally, it should be connected to either IRQ3 or IRQ4 on PC/AT via jumpers. |
| 40 | Floppy Controller Interrupt Request | FINTR | O24 | This interrupt from the Floppy Disk Controller is enabled/disabled via bit 3 of the Digital Output Register (DOR). |
| 39 | Parallel Port Interrupt Request | PINTR | O24 | This interrupt from the Parallel Port is enabled/disabled via bit 4 of the Parallel Port Control Register. If enabled, the interrupt is generated by the $\overline{ACK}$ signal input. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 57 | Reset | RST | IS | This active high signal resets the FDC37C661 and must be valid for 500 ns minimum. The effect on the internal registers is described in the appropriate section. The configuration registers are not affected by this reset. In the FDC37C662, the falling edge of reset latches the jumper configuration. The jumper select lines must be valid 50 ns prior to this edge. |
| | | FLOPPY DISK INTERFACE | | |
| 16 | $\overline{\text{Read Disk Data}}$ | $\overline{\text{RDATA}}$ | IS | Raw serial bit stream from the disk drive, low active. Each falling edge represents a flux transition of the encoded data. |
| 10 | $\overline{\text{Write Gate}}$ | $\overline{\text{WGATE}}$ | OD48 | This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette. |
| 9 | $\overline{\text{Write Data}}$ | $\overline{\text{WDATA}}$ | OD48 | This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media. |
| 11 | $\overline{\text{Head Select}}$ | $\overline{\text{HDSEL}}$ | OD48 | This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed. |
| 7 | $\overline{\text{Direction Control}}$ | $\overline{\text{DIR}}$ | OD48 | This high current low active output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion. |
| 8 | $\overline{\text{Step Pulse}}$ | $\overline{\text{STEP}}$ | OD48 | This active low high current driver issues a low pulse for each track-to-track movement of the head. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 17 | $\overline{\text{Disk Change}}$ | $\overline{\text{DSKCHG}}$ | IS | This input senses that the drive door is open or that the diskette has possibly been changed since the last drive selection. This input is inverted and read via bit 7 of I/O address 3F7H. |
| 4,3, 98,97 | $\overline{\text{Drive Select 0,1,2,3}}$ | $\overline{\text{DS0,1,2,3}}$ | OD48 | Active low open drain outputs select drives 0-3. These drive select outputs are a decode of bits 0 and 1 of the Digital Output Register and qualified by the appropriate Motor Enable Bit of the DOR (bits 4-7). Four drives can be supported directly. |
| 2,5, 96,99 | $\overline{\text{Motor On 0,1,2,3}}$ | $\overline{\text{MTR0,1,2,3}}$ | OD48 | These active low open drain outputs select motor drives 0-3. Four drives are supported directly. These motor enable bits are controlled by software via the Digital Output Register (DOR). |
| 1 | Density Select | DENSEL | OD48 | Indicates whether a low (250/300 Kb/s) or high (500 Kb/s) data rate has been selected. This is determined by the IDENT bit in Configuration Register 3 (Table 12). |
| 14 | $\overline{\text{Write Protected}}$ | $\overline{\text{WRTPRT}}$ | IS | This active low Schmitt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored. |
| 13 | $\overline{\text{Track 00}}$ | $\overline{\text{TR0}}$ | IS | This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track. |
| 12 | $\overline{\text{Index}}$ | $\overline{\text{INDEX}}$ | IS | This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole. |
| 19,18 | Data Rate 0,1 | DRATE0,1 | O8 | These two outputs reflect bits 0 and 1 respectively of the Data Rate Register. At power on, these two outputs are in a high impedance state for the FDC37C661 and are active outputs on the FDC37C662 (refer to Table 38). These two pins have a pull-up to $V_{CC}$ typical value 30$\mu$A. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| | | SERIAL PORT INTERFACE | | |
| 78,88 | Receive Data | RXD1, RXD2 | I | Receiver serial data input. |
| 79 | Transmit Data | TXD1 | O4 | Transmitter serial data output from Primary Serial Port. |
| | | PCF0 | I | FDC37C662(Adapter Mode): Parallel Port Configuration Control 0 - During Reset active this input is read and latched to define the address of the Parallel Port. |
| 81 | $\overline{\text{Request to Send}}$ | $\overline{\text{RTS1}}$ | O4 | Active low Request to Send output for Primary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the $\overline{\text{RTS}}$ signal to inactive mode (high). Forced inactive during loop mode operation. |
| | Parallel Port Configuration Control | PCF1 | I | FDC37C662(Adapter Mode):Parallel Port Configuration Control 1 - During reset active this input is read and latched to define the address of the Parallel Port. |
| 91 | $\overline{\text{Request to Send}}$ | $\overline{\text{RTS2}}$ | O4 | Active low Request to Send output for Secondary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the $\overline{\text{RTS}}$ signal to inactive mode (high). Forced inactive during loop mode operation. |
| | Secondary Serial Port Configuration Control | S2CF0 | I | FDC37C662(Adapter Mode):Secondary Serial Port Configuration Control 0 - During Reset active this input is read and latched to define the address of the Secondary Serial Port. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 83 | Data Terminal Ready | DTR1 | O4 | Active low Data Terminal Ready output for primary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the DTR signal to inactive mode (high). Forced inactive during loop mode operation. |
| | IDE Configuration Control | IDECF | I | FDC37C662(Adapter Mode): IDE Configuration Control During Reset active this input is read and latched to enable/disable the IDE. |
| 93 | Data Terminal Ready | DTR2 | O4 | Active low Data Terminal Ready output for secondary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR), The hardware reset will reset the DTR signal to inactive mode (high). Forced inactive during loop mode operation. |
| | Secondary Serial Port Configuration Control 1 | S2CF1 | I | FDC37C662(Adapter Mode): Secondary Serial Port Configuration Control 1 - During Reset active this input is read and latched to define the address of the Secondary Serial Port. |
| 89 | Transmit Data 2 | TXD2 | O4 | Transmitter Serial Data output from Secondary Serial Port. |
| | | FDCCF | I | FDC37C662 (Adapter Mode): Floppy Disk Configuration. This input is read and latched during Reset to enable/disable the Floppy Disk Controller. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 82,92 | $\overline{\text{Clear to Send}}$ | $\overline{\text{CTS1}}$, $\overline{\text{CTS2}}$ | I | Active low Clear to Send inputs for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of $\overline{\text{CTS}}$ signal by reading bit 4 of Modem Status Register (MSR). A $\overline{\text{CTS}}$ signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{CTS}}$ changes state. The $\overline{\text{CTS}}$ signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of $\overline{\text{CTS}}$. |
| 80,90 | $\overline{\text{Data Set Ready}}$ | $\overline{\text{DSR1}}$, $\overline{\text{DSR2}}$ | I | Active low Data Set Ready inputs for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of $\overline{\text{DSR}}$ signal by reading bit 5 of Modem Status Register (MSR). A $\overline{\text{DSR}}$ signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{DSR}}$ changes state. Note: Bit 5 of MSR is the complement of $\overline{\text{DSR}}$. |
| 85,87 | $\overline{\text{Data Carrier Detect}}$ | $\overline{\text{DCD1}}$, $\overline{\text{DCD2}}$ | I | Active low Data Carrier Detect inputs for primary and secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of $\overline{\text{DCD}}$ signal by reading bit 7 of Modem Status Register (MSR). A $\overline{\text{DCD}}$ signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{DCD}}$ changes state. Note: Bit 7 of MSR is the complement of $\overline{\text{DCD}}$. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 84,86 | $\overline{\text{Ring Indicator}}$ | $\overline{RI1}$, $\overline{RI2}$ | I | Active low Ring Indicator input for primary and secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of $\overline{RI}$ signal by reading bit 6 of Modem Status Register (MSR). A $\overline{RI}$ signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{RI}$ changes state. Note: Bit 6 of MSR is the complement of $\overline{RI}$. |
| 94 | Serial Clock/ Drive 2 | SERCLK/ DRV2 | I/O4 | The 1.8462 MHz clock generated by dividing the 24 MHz crystal frequency by 13 is output as the serial clock.<br><br>In PS/2 mode, this input indicates whether a second drive is connected; DRV2 should be high if a second drive is connected. This status is reflected in a read of Status Register A.<br><br>Defaults to input upon power on for the FDC37C661. The FDC37C662 defaults to SERCLK in output mode on power on.<br><br>This pin has a pull-up to $V_{CC}$, typical value 30$\mu$A. |
| | | PARALLEL PORT INTERFACE | | |
| 73 | $\overline{\text{Printer Select Input}}$ | $\overline{SLCTIN}$ | OD24 | This active low output selects the printer. This is the complement of bit 3 of the Printer Control Register. |
| 74 | $\overline{\text{Initiate Output}}$ | $\overline{INIT}$ | OD24 | This output is bit 2 of the printer control register. This is used to initiate the printer when low. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 76 | $\overline{\text{Autofeed Output}}$ | $\overline{\text{AUTOFD}}$ | OD24 | This output goes low to cause the printer to automatically feed one line after each line is printed. The $\overline{\text{AUTOFD}}$ output is the complement of bit 1 of the Printer Control Register. |
| 77 | $\overline{\text{Strobe Output}}$ | $\overline{\text{STROBE}}$ | OD24 | An active low pulse on this output is used to strobe the printer data into the printer. The $\overline{\text{STROBE}}$ output is the complement of bit 0 of the Printer Control Register. |
| 61 | Busy | BUSY | I | This is a status output from the printer, a high indicating that the printer is not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input. |
| 62 | $\overline{\text{Acknowledge}}$ | $\overline{\text{ACK}}$ | I | A low active output from the printer indicating that it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the $\overline{\text{ACK}}$ input. |
| 60 | Paper End | PE | I | Another status output from the printer, a high indicating that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input. |
| 59 | Printer Selected Status | SLCT | I | This high active output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input. |
| 75 | $\overline{\text{Error}}$ | $\overline{\text{ERR}}$ | I | A low on this input from the printer indicates that there is a error condition at the printer. Bit 3 of the Printer Status register reads the $\overline{\text{ERR}}$ input. |
| 71-68<br>66-63 | Port Data | PD0-PD7 | I/O24 | The bi-directional parallel data bus is used to transfer information between CPU and peripherals. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| | | | IDE | |
| 23 | IDE Low Byte Enable | IDEENLO | O4 | This active low signal is used in both the XT and AT mode. In the AT mode, this pin is active when the IDE is enabled and the I/O address is accessing 1F0H-1F7H and 3F6H-3F7H. In the XT mode, this signal is active for accessing 320H-323H, 8 bit programmed I/O or DMA. |
| | | S1CF1 | I | FDC37C662 (Adapter Mode): Primary Serial Configuration 1. Read and latched during Reset active to select the address of the Secondary Serial Port. |
| 24 | IDE High Byte Enable | IDEENHI | O4 | This signal is active low only in the AT mode, and IO16CSB is also active. The I/O addresses for which this pin reacts are 1F0H-1F7H. This pin is not used in XT mode. |
| | | S1CF0 | I | FDC37C662 (Adapter Mode): Primary Serial Configuration 0. Read and latched during Reset active to define the address of the Secondary Serial Port. |
| 25 | Hard Disk Chip Select | HDCS0 | O24 | This is the Primary Hard Disk Chip select corresponding to addresses 1F0H-1F7H in the AT mode and addresses 320H-323H in the XT mode. |
| 26 | Hard Disk Chip Select | HDCS1 | O24 | This is the Secondary Hard Disk Chip select corresponding to addresses 3F5H-3F7H in the AT and XT modes. |
| 27 | I/O 16 Bit Indicator | IOCS16 | I | This input indicates, in AT mode only, when 16 bit transfers are to take place. This signal is generated by the hard disk interface. Logic "0" = 16 bit mode; logic "1" = 8 bit mode. |
| | | HDACK | I | In the XT mode, this is the Hard Disk Controller DMA Acknowledge, low active. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 22 | IDE Data Bit 7 | IDED7 | I/O24 | IDE data bit 7 in the AT mode. IDED7 transfers data at I/O addresses 1F0H-1F7H (R/W), 3F6 (R/W), 3F7(W). IDED7 should be connected to IDE data bit 7. The FDC37C661 functions as a buffer transferring data bit 7 between the IDE device and the host. During I/O read of 3F7H, IDED7 is the FDC disk change bit. In the XT mode, IDE7 is not used. |
| | | **MISCELLANEOUS** | | |
| 58 | Power Good | PWRGD | I | FDC37C661 (Motherboard Mode) This input indicates that the power ($V_{CC}$) is valid. For device operation, PWRGD must be active. When PWRGD is inactive, all inputs to the FDC37C661 are disconnected and put in a low power mode, all outputs are put into high impedance. The contents of all registers are preserved as long as $V_{CC}$ has a valid value. The driver current drain in this mode drops to ISTBY - standby current. This input has a weak pullup resistor to $V_{CC}$. |
| | Game Port Chip Select | $\overline{\text{GAMECS}}$ | O4 | FDC37C662 (Adapter Mode) - This is the Game Port Chip Select output - active low. It will go active when the I/O address is 201H. |
| 20 | CLOCK 1 | X1/CLK1 | ICLK | The external connection for a parallel resonant 24 MHz crystal. A CMOS compatible oscillator is required if crystal is not used. |
| 21 | CLOCK 2 | X2/CLK2 | OCLK | 24 MHz crystal. If an external clock is used, this pin should not be connected. This pin should not be used to drive any other drivers. |
| 15,72 | Power | $V_{CC}$ | | + 5 Volt supply pin. |
| 6,47, 67,95 | Ground | GND | | Ground pin. |

## BUFFER TYPE DESCRIPTIONS

| BUFFER TYPE | DESCRIPTION |
|---|---|
| I/O24 | Input/output. 24 mA sink; 12 mA source |
| O24 | Output. 24 mA sink; 12 mA source |
| OD48 | Open drain. 48 mA sink |
| O4 | Output. 4 mA sink; 2.0 mA source |
| O8 | Output. 8 mA sink; 4.0 mA source |
| OD24 | Output. 24 mA sink; 50$\mu$A source |
| OCLK | Output to external crystal |
| ICLK | Input to Crystal Oscillator Circuit (CMOS levels) |
| I | Input TTL compatible. |
| IS | Input with Schmitt Trigger. |

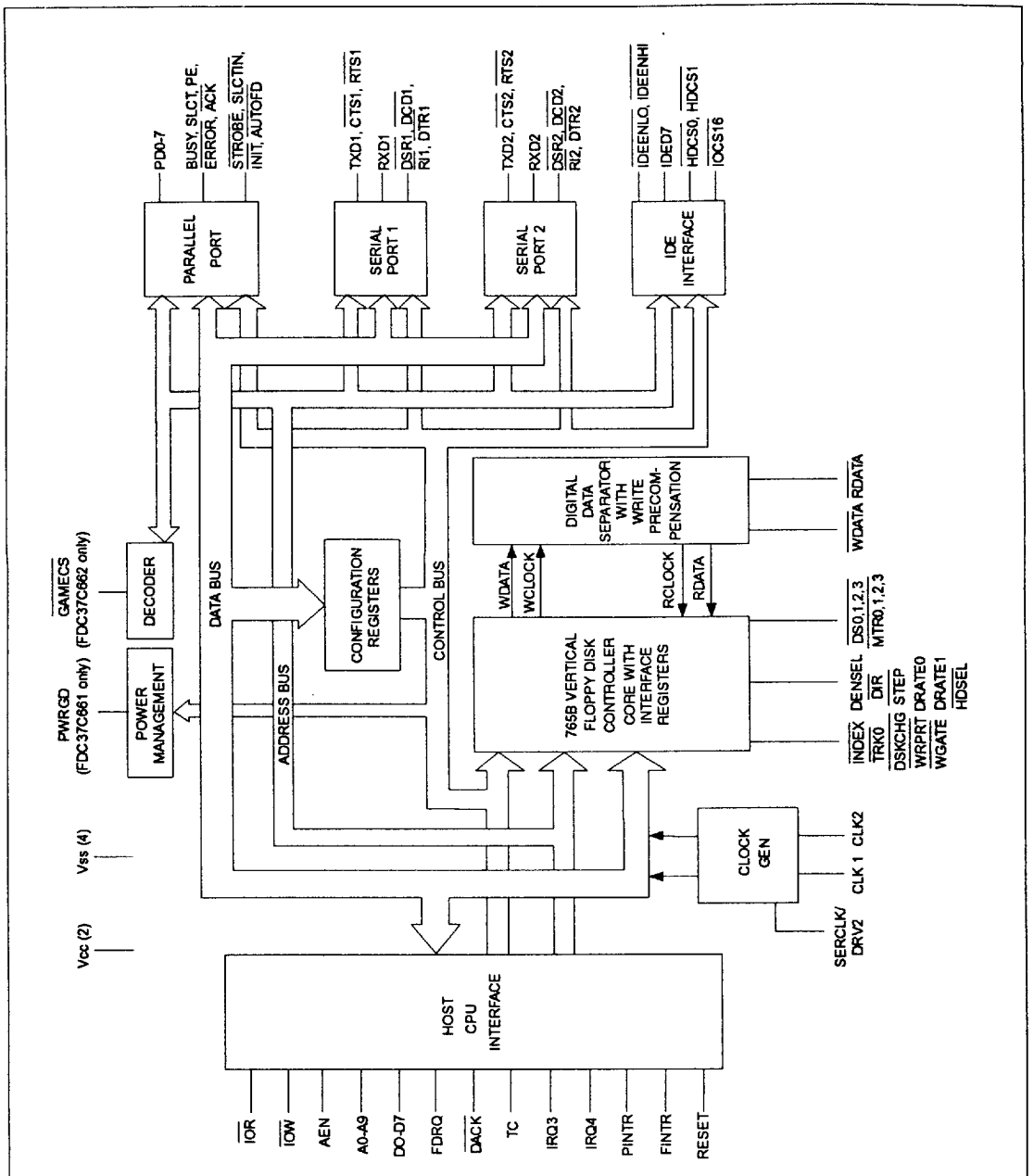



**FIGURE 1 - FDC37C661/FDC37C662 BLOCK DIAGRAM**

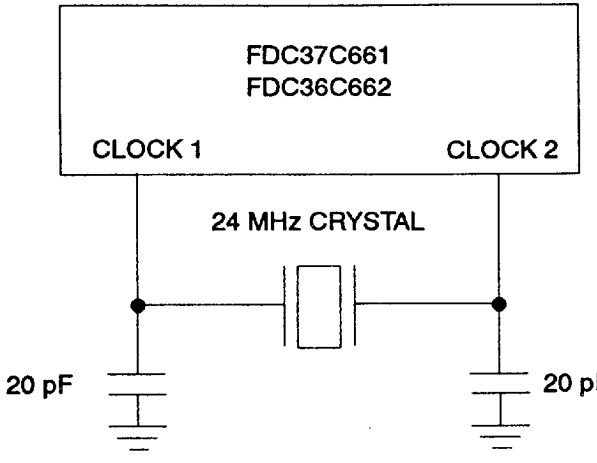



**FIGURE 2 - SUGGESTED 24 MHz OSCILLATOR CIRCUIT**

## FUNCTIONAL DESCRIPTION

### SUPER I/O REGISTERS

The address map, shown below in Table 1, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the serial and parallel ports can be moved via the configuration registers. Some addresses are used to access more than one register.

### HOST PROCESSOR INTERFACE

The host processor communicates with the FDC37C661/662 through a series of read/write registers. The port addresses for these registers are shown in Table 1. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits wide except the IDE data register at port 1F0H which is 16 bits wide. All host interface output buffers are capable of sinking a minimum of 24 mA.

**Table 1 - FDC37C661/662 Block Addresses**

| ADDRESS | BLOCK NAME | NOTES |
|---|---|---|
| 3F0, 3F1 | Configuration | Write only; Note 1 |
| 3F0, 3F1 | Floppy Disk | Read only |
| 3F2, 3F3, 3F4, 3F5, 3F7 | Floppy Disk | |
| 3F8-3FF | Serial Port Com 1 | Address at power up; Note 2 |
| 2F8-2FF | Serial Port Com 2 | Address at power up; Note 2 |
| 278-27A | Parallel Port | Address at power up; Note 2 |
| 1F0-1F7, 3F6, 3F7 | IDE | AT Mode; Note 3 |

Note 1: Configuration registers can only be modified in configuration mode, entered only by writing a security code sequence to 3F0. The configuration registers can only be read in configuration mode by accessing 3F1. Access to status register B of the floppy disk is disabled in configuration mode. Outside of configuration mode, a read of 3F1 accesses status register B of the floppy disk.

Note 2: These addresses can be changed in the configuration setup.

Note 3: Addresses 320H-323H and 3F5-3F7H for XT Mode. Selectable in configuration setup.

## FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC of the FDC37C661 and FDC37C662 is 82077AA compatible.

## FLOPPY DISK CONTROLLER INTERNAL REGISTERS

The Floppy Disk Controller contain eight internal registers which facilitate the interfacing between the host microprocessor and the disk drive. Table 2 shows the addresses required to access these registers. Registers other than the ones shown are not supported.

**Table 2 - Status, Data and Control Registers**

| ADDRESS | | REGISTER | |
|---|---|---|---|
| 3F0 | R | Status Register A | SRA |
| 3F1 | R | Status Register B | SRB |
| 3F2 | R/W | Digital Output Register | DOR |
| 3F3 | R/W | Tape Drive Register | TSR |
| 3F4 | R | Main Status Register | MSR |
| 3F4 | W | Data Rate Select Register | DSR |
| 3F5 | R/W | Data (FIFO) | FIFO |
| 3F6 | | Reserved | |
| 3F7 | R | Digital Input Register | DIR |
| 3F7 | W | Configuration Control Register | CCR |

## STATUS REGISTER A (SRA)

**Address 3F0 READ ONLY**
This register is read-only and monitors the state of the FINTR pin and several disk interface pins, in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F0.

**PS/2 Mode**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | INT PENDING | $\overline{DRV2}$ | STEP | $\overline{TRK0}$ | HDSEL | $\overline{INDX}$ | $\overline{WP}$ | DIR |
| RESET COND. | 0 | N/A | 0 | N/A | 0 | N/A | N/A | 0 |

**BIT 0 DIRECTION**
Active high status indicating the direction of head movement. A logic "1" indicating inward direction a logic "0" outward.

**BIT 1 $\overline{\text{WRITE PROTECT}}$**
Active low status of the WRITE PROTECT disk interface input. A logic "0" indicating that the disk is write protected.

**BIT 2 $\overline{\text{INDEX}}$**
Active low status of the INDEX disk interface input.

**BIT 3 HEAD SELECT**
Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

**BIT 4 $\overline{\text{TRACK 0}}$**
Active low status of the TRK0 disk interface input.

**BIT 5 STEP**
Active high status of the STEP output disk interface output pin.

**BIT 6 $\overline{\text{DRV2}}$**
Active low status of the DRV2 disk interface input pin, indicating that a second drive has been installed.

**BIT 7 INTERRUPT PENDING**
Active high bit indicating the state of the Floppy Disk Interrupt output.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | INT PENDING | DRQ | STEP F/F | TRK0 | $\overline{\text{HDSEL}}$ | INDX | WP | $\overline{\text{DIR}}$ |
| RESET COND. | 0 | 0 | 0 | N/A | 1 | N/A | N/A | 1 |

**BIT 0 $\overline{\text{DIRECTION}}$**
Active low status indicating the direction of head movement. A logic "0" indicating inward direction a logic "1" outward.

**BIT 1 WRITE PROTECT**
Active high status of the WRITE PROTECT disk interface input. A logic "1" indicating that the disk is write protected.

**BIT 2 INDEX**
Active high status of the INDEX disk interface input.

**BIT 3 $\overline{\text{HEAD SELECT}}$**
Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

**BIT 4 TRACK 0**
Active high status of the TRK0 disk interface input.

**BIT 5 STEP**
Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

**BIT 6 DMA REQUEST**
Active high status of the DRQ output pin.

**BIT 7 INTERRUPT PENDING**
Active high bit indicating the state of the Floppy Disk Interrupt output.

**STATUS REGISTER B (SRB)**

**Address F1 READ ONLY**
This register is read-only and monitors the state of several disk interface pins, in PS/2 and Model 30 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F1.

**PS/2 Mode**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 1 | 1 | DRIVE SEL0 | WDATA TOGGLE | RDATA TOGGLE | WGATE | MOT EN1 | MOT EN0 |
| RESET COND. | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**BIT 0 MOTOR ENABLE 0**
Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

**BIT 1 MOTOR ENABLE 1**
Active high status of the MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

**BIT 2 WRITE GATE**
Active high status of the WGATE disk interface output.

**BIT 3 READ DATA TOGGLE**
Every inactive edge of the RDATA input causes this bit to change state.

**BIT 4 WRITE DATA TOGGLE**
Every inactive edge of the WDATA input causes this bit to change state.

**BIT 5 DRIVE SELECT 0**
Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset, it is unaffected by a software reset.

**BIT 6 RESERVED**
Always read as a logic "1".

**BIT 7 RESERVED**
Always read as a logic "1".

**PS/2 Model 30 Mode**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | $\overline{DRV2}$ | $\overline{DS1}$ | $\overline{DS0}$ | WDATA F/F | RDATA F/F | WGATE F/F | $\overline{DS3}$ | $\overline{DS2}$ |
| RESET COND. | N/A | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

**BIT 0 $\overline{\text{DRIVE SELECT 2}}$**
Active low status of the DS2 disk interface output.

**BIT 1 $\overline{\text{DRIVE SELECT 3}}$**
Active low status of the DS3 disk interface output.

**BIT 2 WRITE GATE**
Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

**BIT 3 READ DATA**
Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

**BIT 4 WRITE DATA**
Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

**BIT 5 $\overline{\text{DRIVE SELECT 0}}$**
Active low status of the DS0 disk interface output.

**BIT 6 $\overline{\text{DRIVE SELECT 1}}$**
Active low status of the DS1 disk interface output.

**BIT 7 $\overline{\text{DRV2}}$**
Active low status of the DRV2 disk interface input.

## DIGITAL OUTPUT REGISTER (DOR)

**Address 3F2 READ/WRITE**
The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and contains a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | MOT EN3 | MOT EN2 | MOT EN1 | MOT EN0 | DMAEN | $\overline{\text{RESET}}$ | DRIVE SEL1 | DRIVE SEL0 |
| RESET COND. | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**BIT 0 and 1 DRIVE SELECT**
These two bit a are binary encoded for the four drive selects DS0 -DS3, thereby allowing only one drive to be selected at one time.

**BIT 2 $\overline{\text{RESET}}$**
A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit.This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive write to this register is a valid method of issuing a software reset.

**BIT 3 DMAEN**
PC/AT and Model 30 MODE: Writing this bit to logic "1" will enable the DRQ, $\overline{\text{DACK}}$, TC and FINTR outputs. This bit being a logic "0" will disable the $\overline{\text{DACK}}$ and TC inputs, and hold the DRQ and FINTR outputs in a high impedance state. This bit is a logic "0" after a reset and in these modes.

PS/2 MODE: In this mode the DRQ, $\overline{\text{DACK}}$, TC and FINTR pins are always enabled. During a reset, the DRQ, $\overline{\text{DACK}}$, TC, and FINTR pins will remain enabled, but this bit will be cleared to a logic "0".

**BIT 4 MOTOR ENABLE 0**
This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to go active.

**BIT 5 MOTOR ENABLE 1**
This bit controls the MTR1 disk interface output. A logic "1" in this bit will cause the output pin to go active.

**BIT 6 MOTOR ENABLE 2**
This bit controls the MTR2 disk interface output. A logic "1" in this bit will cause the output pin to go active.

**BIT 7 MOTOR ENABLE 3**
This bit controls the MTR3 disk interface output. A logic "1" in this bit causes the output to go active.

**Table 3 - Drive Activation Values**

| DRIVE | DOR VALUE |
|---|---|
| 0 | 1CH |
| 1 | 2DH |
| 2 | 4EH |
| 3 | 8FH |

**TAPE DRIVE REGISTER (TDR)**

**Address 3F3 READ/WRITE**

**Normal Floppy Mode 0**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | TAPE SEL1 | TAPE SEL0 |
| RESET COND. | N/A | N/A | N/A | N/A | N/A | N/A | 0 | 0 |

This register is included for 82077 software compatability. The robust digital data separator used in the FDC37C661 does not require its characteristics modified for tape support. The contents of this register are not used internal to the device. The TDR is unaffected by a software reset. Bits 2-7 are high impedance when this register is read.

**Table 4- Tape Select Bits**

| TAPE SEL1 | TAPE SEL2 | DRIVE SELECTED |
|---|---|---|
| 0 | 0 | None |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

**Enhanced Floppy Mode 1**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| READ | MEDIA ID1 | MEDIA ID0 | DRIVE SWITCH | DENSITY SELECT | | DMA MODE | TAPE SEL1 | TAPE SEL0 |
| WRITE | X | X | DRIVE SWITCH | DENSITY SELECT | | DMA MODE | TAPE SEL1 | TAPE SEL0 |

Enhanced floppy mode is selected through configuration register CR3 bit 2. The definition of this register is as follows:

**BIT 7 MEDIA ID 1** (READ ONLY)(Pin 96) (See Table 5.)

**BIT 6 MEDIA ID 0** (READ ONLY)(Pin 98) (See Table 6).

These two bits are not affected by a hard or soft reset.

**BIT 5 DRIVE SELECT SWITCH** (READ/WRITE) This bit is cleared by a hardware reset, it is not affected by a soft reset. 0 = Normal operation. 1 = DS0 and DS1 are swapped, MTR0 and MTR1 are swapped.

**BITS 4,3 DENSITY SELECT OUTPUT CONTROL** (READ/WRITE)
In normal mode, DENSEL is affected by the IDENT bit in the configuration register. (There is no INVERT pin.) These bits are cleared by a hard or soft reset.

**BIT 2 DMA MODE CONTROL** (READ/WRITE) This bit is cleared by a hard reset. If the LOCK bit is not set it is also cleared by a soft reset. 0 = Burst mode is enabled for FIFO execution phase data transfers. 1 = Non-Burst mode enabled. The DRQ and IRQ pins are strobed once for each byte transferred while the FIFO is enabled.

**BITS 1,0 TAPE DRIVE SELECT** (READ/WRITE) These bits are cleared by a hard reset only. See Table 4.

**Table 5 - Media ID 1**

| MTR2 | MEDIA ID 1 |
|---|---|
| PIN 96 | BIT 7 |
| 0 | 0 |
| 0 | 0 |
| 1 | 1 |
| 1 | 1 |

**Table 6 - Media ID 0**

| DS2 | MEDIA ID 0 |
|---|---|
| PIN 98 | BIT 6 |
| 0 | 0 |
| 1 | 1 |
| 0 | 0 |
| 1 | 1 |

**Table 7 - Density Select Control**

| BIT 4 | BIT 3 | DENSEL |
|---|---|---|
| 0 | 0 | Normal |
| 0 | 1 | TBD |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## DATA RATE SELECT REGISTER (DSR)

**Address 3F4 WRITE ONLY**

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30 and Microchannel applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250kb/s.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | S/W RESET | POWER DOWN | 0 | PRE-COMP2 | PRE-COMP1 | PRE-COMP0 | DRATE SEL1 | DRATE SEL0 |
| RESET COND. | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**BIT 0 and 1 DATA RATE SELECT**

These bits control the data rate of the floppy controller. See Table 9 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250kb/s after a hardware reset.

**BIT 2 through 4 PRECOMPENSATION SELECT**

These three bits select the value of write precompensation that will be applied to the WDATA output signal. Table 8 shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. this starting track number can be changed by the configure command.

**BIT 5 UNDEFINED**

Should be written as a logic "0".

**BIT 6 LOW POWER**

A logic "1" written to this bit will put the floppy controller into Manual Low Power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or access to the Data Register or Main Status Register.

**BIT 7 SOFTWARE RESET**

This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

**Table 8 - Precompensation Delays**

| PRECOMP 432 | PRECOMPENSATION DELAY |
|---|---|
| 111 | 0.00 ns-DISABLED |
| 001 | 41.67 ns |
| 010 | 83.34 ns |
| 011 | 125.00 ns |
| 100 | 166.67 ns |
| 101 | 208.33 ns |
| 110 | 250.00 ns |
| 000 | DEFAULT |

**Table 9 - Data Rates**

| DRATESEL | | DATA RATE | |
|---|---|---|---|
| 1 | 0 | MFM | FM |
| 1 | 1 | 1 Mbps | Illegal |
| 0 | 0 | 500 Kbps | 250 Kbps |
| 0 | 1 | 300 Kbps | 150 Kbps |
| 1 | 0 | 250 Kbps | 125 Kbps |

**Table 10 - Default Precompensation Delays**

| DATA RATE | PRECOMPENSATION DELAYS |
|---|---|
| 1 Mbps | 41.67 ns |
| 500 Kbps | 125 ns |
| 300 Kbps | 125 ns |
| 250 Kbps | 125 ns |

## MAIN STATUS REGISTER

**Address 3F4 READ ONLY**

The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. NO delay is required when reading the MSR after a data transfer.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RQM | DIO | NON DMA | CMD BUSY | DRV3 BUSY | DRV2 BUSY | DRV1 BUSY | DRV0 BUSY |

**BIT 0 - 3 DRV x BUSY**

These bits are set to 1s when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

**BIT 4 COMMAND BUSY**

This bit is set to a 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a 0 after the last command byte.

**BIT 5 NON-DMA**

This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

**BIT 6 DIO**

Indicates the direction of a data transfer once a RQM is set. A 1 indicates a read and a 0 indicates a write is required.

**BIT 7 RQM**

Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

## DATA REGISTER (FIFO)

**Address 3F5 READ/WRITE**
All command parameter information, disk data and result status are transferred between the host processor and the floppy disk controller through the Data Register.

Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 11 gives several examples of the delays with a FIFO. The data is based upon the following formula:

$$\text{Threshold } \# \times \left| \frac{1}{\text{DATA RATE}} \times 8 \right| - 1.5\ \mu s = \text{DELAY}$$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

**Table 11 - FIFO Service Delay**

| FIFO THRESHOLD EXAMPLES | MAXIMUM DELAY TO SERVICING AT 1 Mbps DATA RATE |
|---|---|
| 1 byte | 1 x 8 $\mu s$ - 1.5 $\mu s$ = 6.5 $\mu s$ |
| 2 bytes | 2 x 8 $\mu s$ - 1.5 $\mu s$ = 14.5 $\mu s$ |
| 8 bytes | 8 x 8 $\mu s$ - 1.5 $\mu s$ = 62.5 $\mu s$ |
| 15 bytes | 15 x 8 $\mu s$ - 1.5 $\mu s$ = 118.5 $\mu s$ |

| FIFO THRESHOLD EXAMPLES | MAXIMUM DELAY TO SERVICING AT 500 Kbps DATA RATE |
|---|---|
| 1 byte | 1 x 16 $\mu s$ - 1.5 $\mu s$ = 14.5 $\mu s$ |
| 2 bytes | 2 x 16 $\mu s$ - 1.5 $\mu s$ = 30.5 $\mu s$ |
| 8 bytes | 8 x 16 $\mu s$ - 1.5 $\mu s$ = 126.5 $\mu s$ |
| 15 bytes | 15 x 16 $\mu s$ - 1.5 $\mu s$ = 238.5 $\mu s$ |

## DIGITAL INPUT REGISTER (DIR)

**Address 3F7 READ**
This register is read-only in all modes.

**PC/AT Mode**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | DSK CHG | | | | | | | |
| RESET COND. | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

**BIT 0 - 6 UNDEFINED**
The data bus outputs D0 - 6 will remain in a high impedance state during a read of this register.

**BIT 7 DSKCHG**
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable.

**PS/2 Mode**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | DSK CHG | 1 | 1 | 1 | 1 | DRATE SEL1 | DRATE SEL0 | $\overline{\text{HIGH}}$ $\overline{\text{DENS}}$ |
| RESET COND. | N/A | N/A | N/A | N/A | N/A | N/A | N/A | 1 |

**BIT 0 $\overline{\text{HIGH DENS}}$**
This bit is low whenever the 500 Kbps or 1 Mbps data rates are selected, and high when 250Kbps and 300Kbps are selected.

**BITS 1 - 2 DATA RATE SELECT**
These bits control the data rate of the floppy controller. See Table 9 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250kb/s after a hardware reset.

**BITS 3 - 6 UNDEFINED**
Always read as a logic "1"

**BIT 7 DSKCHG**
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable.

**Model 30 Mode**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | $\overline{\text{DSK CHG}}$ | 0 | 0 | 0 | DMAEN | NOPREC | DRATE SEL1 | DRATE SEL0 |
| RESET COND. | N/A | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**BITS 0 - 1 DATA RATE SELECT**
These bits control the data rate of the floppy controller. See Table 9 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250kb/s after a hardware reset.

**BIT 2 NOPREC**
This bit reflects the value of NOPREC bit set in the CCR register.

**BIT 3 DMAEN**
This bit reflects the value of DMAEN bit set in the DOR register bit 3.

**BITS 4 - 6 UNDEFINED**
Always read as a logic "0"

**BIT 7 DSKCHG**
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable 300Kbps are selected.

## CONFIGURATION CONTROL REGISTER (CCR)

**Address 3F7 WRITE**
**PC/AT and PS/2 Modes**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | DRATE SEL1 | DRATE SEL0 |
| RESET COND. | N/A | N/A | N/A | N/A | N/A | N/A | 1 | 0 |

**BIT 0 and 1 DATA RATE SELECT 0 and 1**
These bits determine the data rate of the floppy controller. See Table 9 for the appropriate values.

**BIT 2 - 7 RESERVED**
Should be set to a logical "0"

**PS/2 Model 30 Mode**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | NOPREC | DRATE SEL1 | DRATE SEL0 |
| RESET COND. | N/A | N/A | N/A | N/A | N/A | N/A | 1 | 0 |

**BIT 0 and 1 DATA RATE SELECT 0 and 1**
These bits determine the data rate of the floppy controller. See Table 9 for the appropriate values.

**BIT 2 NO PRECOMPENSATION**
This bit can be set by software, but it has no functionality. It can be read by bit 2 of the DSR when in Model 30 register mode. Unaffected by software reset.

**BIT 3 - 7 RESERVED**
Should be set to a logical "0"

Table 12 shows the state of the DENSEL pin. This pin is set high after a hardware reset and is unaffected by the DOR and the DSR resets.

**Table 12 - DENSEL Encoding**

| Data Rate | IDENT | DENSEL |
|---|---|---|
| 1Mbps | 0 | 0 |
| | 1 | 1 |
| 500kbps | 0 | 0 |
| | 1 | 1 |
| 300kps | 0 | 1 |
| | 1 | 0 |
| 250kbps | 0 | 1 |
| | 1 | 0 |

## STATUS REGISTER ENCODING

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

**Table 13 - Status Register 0**

| BIT NO. | SYMBOL | NAME | DESCRIPTION |
|---|---|---|---|
| 7,6 | IC | Interrupt Code | 00 - Normal termination of command. The specified command was properly executed and completed without error.<br>01 - Abnormal termination of command. Command execution was started, but was not successfully completed.<br>10 - Invalid command. The requested command could not be executed.<br>11 - Abnormal termination caused by Polling. |
| 5 | SE | Seek End | The FDC completed a Seek, Relative Seek, or Recalibrate command (used during a Sense Interrupt command). |
| 4 | EC | Equipment Check | The TRK0 pin failed to become a "1" after:<br>1. 80 step pulses in the Recalibrate command.<br>2. The Relative Seek command caused the FDC to step outward beyond Track 0. |
| 3 | | | Unused. This bit is always "0". |
| 2 | H | Head Address | The current head address. |
| 1,0 | DS1,0 | Drive Select | The current selected drive. |

**Table 14 - Status Register 1**

| BIT NO. | SYMBOL | NAME | DESCRIPTION |
|---|---|---|---|
| 7 | EN | End of Cylinder | The FDC tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data command. |
| 6 | | | Unused. This bit is always "0". |
| 5 | DE | Data Error | The FDC detected a CRC error in either the ID field or the data field of a sector. |
| 4 | OR | Overrun/ Underrun | Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun. |
| 3 | | | Unused. This bit is always "0". |
| 2 | ND | No Data | Any one of the following:<br>1. Read Data, Read Deleted Data command - the FDC did not find the specified sector.<br>2. Read ID command - the FDC cannot read the ID field without an error.<br>3. Read A Track command - the FDC cannot find the proper sector sequence. |
| 1 | NW | Not Writable | WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command. |
| 0 | MA | Missing Address Mark | Any one of the following:<br>1. The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the IDX pin twice.<br>2. The FDC cannot detect a data address mark or a deleted data address mark on the specified track. |

Table 15 - Status Register 2

| BIT NO. | SYMBOL | NAME | DESCRIPTION |
|---|---|---|---|
| 7 | | | Unused. This bit is always "0". |
| 6 | CM | Control Mark | Any one of the following:<br>1. Read Data command - the FDC encountered a deleted data address mark.<br>2. Read Deleted Data command - the FDC encountered a data address mark. |
| 5 | DD | Data Error in Data Field | The FDC detected a CRC error in the data field. |
| 4 | WC | Wrong Cylinder | The track address from the sector ID field is different from the track address maintained inside the FDC. |
| 3 | | | Unused. This bit is always "0". |
| 2 | | | Unused. This bit is always "0". |
| 1 | BC | Bad Cylinder | The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format. |
| 0 | MD | Missing Data Address Mark | The FDC cannot detect a data address mark or a deleted data address mark. |

Table 16- Status Register 3

| BIT NO. | SYMBOL | NAME | DESCRIPTION |
|---|---|---|---|
| 7 | | | Unused. This bit is always "0". |
| 6 | WP | Write Protected | Indicates the status of the WP pin. |
| 5 | | | Unused. This bit is always "1". |
| 4 | T0 | Track 0 | Indicates the status of the TRK0 pin. |
| 3 | | | Unused. This bit is always "1". |
| 2 | HD | Head Address | Indicates the status of the HDSEL pin. |
| 1,0 | DS1,0 | Drive Select | Indicates the status of the DS1, DS0 pins. |

**RESET**

There are three sources of system reset on the FDC: the RESET pin of the FDC37C661, a reset generated via a bit in the DOR, and a reset generated via a bit in the DSR. At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upom a RESET, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

**RESET Pin (Hardware Reset)**

The RESET pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

**DOR Reset vs. DSR Reset (Software Reset)**

These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. The DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

**MODES OF OPERATION**

The FDC has three modes of operation, PC/AT mode, PS/2 mode and Model 30 mode. These are determined by the state of the IDENT and MFM bits 6 and 5 respectively of Configuration Register 3.

**PC/AT mode** - (IDENT high, MFM a "don't care")
The PC/AT register set is enabled, the DMA enable bit of the DOR becomes valid (FINTR and DRQ can be hi Z), and TC and DENSEL become active high signals.

**PS/2 mode** - (IDENT low, MFM high)
This mode supports the PS/2 models 50/60/80 configuration and register set. The DMA bit of the DOR becomes a "don't care", (FINTR and DRQ are always valid), TC and DENSEL become active low.

**Model 30 mode** - (IDENT low, MFM low)
This mode supports PS/2 Model 30 configuration and register set. The DMA enable bit of ther DOR becomes valid (FINTR and DRQ can be hi Z), TC is active high and DENSEL is active low.

**DMA TRANSFERS**

DMA transfers are enabled with the Specify command and are initiated by the FDC by activating the FDRQ pin during a data transfer command. The FIFO is enabled directly by asserting $\overline{DACK}$ and addresses need not be valid.

Note that if the DMA controller (i.e. 8237A) is programmed to function in verify mode, a pseudo read is performed by the FDC based only on $\overline{DACK}$. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled, the FDC can perform the above operation by using the new Verify command; no DMA operation is needed.

**CONTROLLER PHASES**

For simplicity, command handling in the FDC can be divided into three phases: Command, Execution, and Result. Each phase is described in the following sections.

**Command Phase**

After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the FDC before the command phase is complete. (Please refer to Table 18 for the command set descriptions.) These bytes of data must be transferred in the order prescribed.

Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM and DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the FDC after each write cycle until the received byte is processed. The FDC asserts RQM again to request each parameter byte of the command unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0" and the FDC automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to provide for the proper handling of the "Invalid Command" condition.

**Execution Phase**

All data transfers to or from the FDC occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the Specify command.

After a reset, the FIFO is disabled. Each data byte is transferred by an FINT or FDRQ depending on the DMA mode. The Configure command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the FDC when service is requested from the host and ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode - Transfers from the FIFO to the Host

The FINT pin and RQM bits in the Main Status Register are activated when the FIFO contains (16-<threshold>) bytes or the last bytes of a full sector have been placed in the FIFO. The FINT pin can be used for interrupt-driven systems, and RQM can be used for polled systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The FDC will deactivate the FINT pin and RQM bit when the FIFO becomes empty.

Non-DMA Mode - Transfers from the Host to the FIFO

The FINT pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The FINT pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The FINT pin will also be deactivated if TC and $\overline{\text{DACK}}$ both go inactive. The FDC enters the result phase after the last byte is taken by the FDC from the FIFO (i.e. FIFO empty condition).

DMA Mode - Transfers from the FIFO to the Host

The FDC activates the DDRQ pin when the FIFO contains (16 - <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The FDC will deactivate the DDRQ pin when the FIFO becomes empty. FDRQ goes inactive after $\overline{\text{DACK}}$ goes active for the last byte of a data transfer (or on the active edge of $\overline{\text{IOR}}$, on the last byte, if no edge is present on $\overline{\text{DACK}}$). A data underrun may occur if FDRQ is not removed in time to prevent an unwanted cycle.

DMA Mode - Transfers from the Host to the FIFO

The FDC activates the FDRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the $\overline{\text{DACK}}$ and $\overline{\text{IOW}}$ pins and placing data in the FIFO. FDRQ remains active until the FIFO becomes full. FDRQ is again set true when the FIFO has <threshold> bytes remaining in the FIFO. The FDC will also deactivate the FDRQ pin when TC becomes true (qualified by $\overline{\text{DACK}}$), indicating that not more data is required. FDRQ goes inactive after $\overline{\text{DACK}}$ goes active for the last byte of a data transfer (or on the active edge of $\overline{\text{IOW}}$ of the last byte, if no edge is present on $\overline{\text{DACK}}$). A data overrun may occur if FDRQ is not removed in time to prevent an unwanted cycle.

Data Transfer Termination

The FDC supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer.

If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the FDC will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indication scan be ignored if they were expected.

Note that when the host is sending data to the FIFO of the FDC, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must tolerate this delay.

**Result Phase**

The generation of FINT determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared, indicating that the FDC is ready to accept the next command.

## COMMAND SET/DESCRIPTIONS

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it is invalid, an interrupt is issued. The user sends a Sense Interrupt Status command which returns an invalid command error. Refer to Table 16 for explanations of the various symbols used. Table 17 lists the required parameters and the results associated with each command that the FDC is capable of performing.

**Table 17 - Description of Command Symbols**

<table>
<tr><th>SYMBOL</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>C</td><td>Cylinder Address</td><td>The currently selected address; 0 to 255.</td></tr>
<tr><td>D</td><td>Data Pattern</td><td>The pattern to be written in each sector data field during formatting.</td></tr>
<tr><td>D0, D1,<br>D2, D3</td><td>Drive Select 0-3</td><td>Designates which drives are perpendicular drives on the Perpendicular Mode Command. A "1" indicates a perpendicular drive.</td></tr>
<tr><td>DIR</td><td>Direction Control</td><td>If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.</td></tr>
<tr><td>DS0, DS1</td><td>Disk Drive Select</td><td><table><tr><th>DS1</th><th>DS0</th><th>DRIVE</th></tr><tr><td>0</td><td>0</td><td>drive 0</td></tr><tr><td>0</td><td>1</td><td>drive 1</td></tr><tr><td>1</td><td>0</td><td>drive 2</td></tr><tr><td>1</td><td>1</td><td>drive 3</td></tr></table></td></tr>
<tr><td>DTL</td><td>Special Sector Size</td><td>By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.</td></tr>
<tr><td>EC</td><td>Enable Count</td><td>When this bit is "1" the "DTL" parameter of the Verify command becomes SC (number of sectors per track).</td></tr>
<tr><td>EFIFO</td><td>Enable FIFO</td><td>This active low bit when a 0, enables the FIFO. A "1" disables the FIFO (default).</td></tr>
</table>

Table 17 - Description of Command Symbols

| SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| EIS | Enable Implied Seek | When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek. |
| EOT | End of Track | The final sector number of the current track. |
| GAP | | Alters Gap 2 length when using Perpendicular Mode. |
| GPL | Gap Length | The Gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field). |
| H/HDS | Head Address | Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field. |
| HLT | Head Load Time | The time interval that FDC waits after loading the head and before initializing a read or write operation. Refer to the Specify command for actual delays. |
| HUT | Head Unload Time | The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the Specify command for actual delays. |
| LOCK | | Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE COMMAND can be reset to their default values by a "software Reset". (A reset caused by writing to the appropriate bits of either tha DSR or DOR) |
| MFM | MFM/FM Mode Selector | A one selects the double density (MFM) mode. A zero selects single density (FM) mode. |
| MT | Multi-Track Selector | When set, this flag selects the multi-track operating mode. In this mode, the FDC treats a complete cylinder under head 0 and 1 as a single track. The FDC operates as this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0. |

**Table 17 - Description of Command Symbols**

| SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| N | Sector Size Code | This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the user's responsibility to not select combinations that are not possible with the drive. |
| NCN | New Cylinder Number | The desired cylinder number. |
| ND | Non-DMA Mode Flag | When set to 1, indicates that the FDC is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the FDC operates in DMA mode, interfacing to a DMA controller by means of the DRQ and $\overline{\text{DACK}}$ signals. |
| OW | Overwrite | The bits D0-D3 of the Perpendicular Mode Command can only be modified if OW is set to 1. OW id defined in the Lock command. |
| PCN | Present Cylinder Number | The current position of the head at the completion of Sense Interrupt Status command. |
| POLL | Polling Disable | When set, the internal polling routine is disabled. When clear, polling is enabled. |
| PRETRK | Precompensation Start Track Number | Programmable from track 00 to FFH. |
| R | Sector Address | The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written. |
| RCN | Relative Cylinder Number | Relative cylinder offset from present cylinder as used by the Relative Seek command. |

| N | SECTOR SIZE |
|---|---|
| 00 | 128 bytes |
| 01 | 256 bytes |
| 02 | 512 bytes |
| 03 | 1024 bytes |
| .. | ... |
| 07 | 16 Kbytes |

Table 17 - Description of Command Symbols

| SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| SC | Number of Sectors Per Track | The number of sectors per track to be initialized by the Format command. The number of sectors per track to be verified during a Verify command when EC is set. |
| SK | Skip Flag | When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands. |
| SRT | Step Rate Interval | The time interval between step pulses issued by the FDC. Programmable from 0.5 to 8 milliseconds in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays. |
| ST0<br>ST1<br>ST2<br>ST3 | Status 0<br>Status 1<br>Status 2<br>Status 3 | Registers within the FDC which store status information after a command has been executed. This status information is available to the host during the result phase after command execution. |
| WGATE | Write Gate | Alters timing of WE to allow for pre-erase loads in perpendicular drives. |

## INSTRUCTION SET

**Table 18 - Instruction Set**

| READ DATA | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | MT | MFM | SK | 0 | 0 | 1 | 1 | 0 | Command Codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system. |
| Result | R | ST0 | | | | | | | | Status information after Command execution. |
| | R | ST1 | | | | | | | | |
| | R | ST2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution. |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

| READ DELETED DATA | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | MT | MFM | SK | 0 | 1 | 1 | 0 | 0 | Command Codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system. |
| Result | R | ST0 | | | | | | | | Status information after Command execution. |
| | R | ST1 | | | | | | | | |
| | R | ST2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution. |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

| WRITE DATA | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | MT | MFM | 0 | 0 | 0 | 1 | 0 | 1 | Command Codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system. |
| Result | R | ST0 | | | | | | | | Status information after Command execution. |
| | R | ST1 | | | | | | | | |
| | R | ST2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution. |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

| WRITE DELETED DATA | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | MT | MFM | 0 | 0 | 1 | 0 | 0 | 1 | Command Codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system. |
| Result | R | ST0 | | | | | | | | Status information after Command execution. |
| | R | ST1 | | | | | | | | |
| | R | ST2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution. |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

| READ A TRACK | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 0 | MFM | 0 | 0 | 0 | 0 | 1 | 0 | Command Codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system. FDC reads all of cylinders' contents from index hole to EOT. |
| Result | R | ST0 | | | | | | | | Status information after Command execution. |
| | R | ST1 | | | | | | | | |
| | R | ST2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution. |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

| VERIFY | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | MT | MFM | SK | 1 | 0 | 1 | 1 | 0 | Command Codes |
| | W | EC | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL/SC | | | | | | | | |
| Execution | | | | | | | | | | No data transfer takes place. |
| Result | R | ST0 | | | | | | | | Status information after Command execution. |
| | R | ST1 | | | | | | | | |
| | R | ST2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution. |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

| VERSION | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Command Code |
| Result | R | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Enhanced Controller |

| FORMAT A TRACK | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 0 | MFM | 0 | 0 | 1 | 1 | 0 | 1 | Command Codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | N | | | | | | | | Bytes/Sector |
| | W | SC | | | | | | | | Sectors/Cylinder |
| | W | GPL | | | | | | | | Gap 3 |
| | W | D | | | | | | | | Filler Byte |
| Execution for Each Sector Repeat: | W | C | | | | | | | | Input Sector Parameters |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | | | | | | | | | | FDC formats an entire cylinder |
| Result | R | ST0 | | | | | | | | Status information after Command execution |
| | R | ST1 | | | | | | | | |
| | R | ST2 | | | | | | | | |
| | R | Undefined | | | | | | | | |
| | R | Undefined | | | | | | | | |
| | R | Undefined | | | | | | | | |
| | R | Undefined | | | | | | | | |

| RECALIBRATE | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Command Codes |
| | W | 0 | 0 | 0 | 0 | 0 | 0 | DS1 | DS0 | |
| Execution | | | | | | | | | | Head retracted to Track 0 Interrupt. |

| SENSE INTERRUPT STATUS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Command Codes |
| Result | R | ——— STO ——— | | | | | | | | Status information at the end of each seek operation. |
| | R | ——— PCN ——— | | | | | | | | |

| SPECIFY | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Command Codes |
| | W | ——— SRT ——— | | | | ——— HUT ——— | | | | |
| | W | ——— HLT ——— | | | | | | | ND | |

| SENSE DRIVE STATUS | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Command Codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| Result | R | ST3 | | | | | | | | Status information about FDD |

| SEEK | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Command Codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | NCN | | | | | | | | |
| Execution | | | | | | | | | | Head positioned over proper cylinder on diskette. |

| CONFIGURE | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | Configure Information |
| | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | W | 0 | EIS | EFIFO | POLL | FIFOTHR | | | | |
| Execution | W | PRETRK | | | | | | | | |

| RELATIVE SEEK | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| PHASE | R/W | DATA BUS D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 1 | DIR | 0 | 0 | 1 | 1 | 1 | 1 | |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | RCN | | | | | | | | |

| DUMPREG | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| PHASE | R/W | DATA BUS D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | *Note: Registers placed in FIFO |
| Execution | | | | | | | | | | |
| Result | R | PCN-Drive 0 | | | | | | | | |
| | R | PCN-Drive 1 | | | | | | | | |
| | R | PCN-Drive 2 | | | | | | | | |
| | R | PCN-Drive 3 | | | | | | | | |
| | R | SRT | | | | | HUT | | | |
| | R | HLT | | | | | | | ND | |
| | R | SC/EOT | | | | | | | | |
| | R | LOCK | 0 | D3 | D2 | D1 | D0 | GAP | WGATE | |
| | R | 0 | EIS | EFIFO | POLL | FIFOTHR | | | | |
| | R | PRETRK | | | | | | | | |

| READ ID | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 0 | MFM | 0 | 0 | 1 | 0 | 1 | 0 | Commands |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| Execution | | | | | | | | | | The first correct ID information on the Cylinder is stored in Data Register |
| Result | R | ST0 | | | | | | | | Status information after Command execution. |
| | R | ST1 | | | | | | | | |
| | R | ST2 | | | | | | | | |
| | R | C | | | | | | | | |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | Disk status after the Command has completed |
| | R | N | | | | | | | | |

| PERPENDICULAR MODE | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Command Codes |
| | | OW | 0 | D3 | D2 | D1 | D0 | GAP | WGATE | |

| INVALID CODES | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | ——— Invalid Codes ——— | | | | | | | | Invalid Command Codes (NoOp - FDC37C661/662 goes into Standby State) |
| Result | R | ——— ST0 ——— | | | | | | | | ST0 = 80H |

| LOCK | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUS | | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| Command | W | LOCK | 0 | 0 | 1 | 0 | 1 | 0 | 0 | Command Codes |
| Result | R | 0 | 0 | 0 | LOCK | 0 | 0 | 0 | 0 | |

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

**NOTE:** These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

## DATA TRANSFER COMMANDS

All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it will be reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

### Read Data

A set of nine (9) bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command.

N determines the number of bytes per sector (see Table 19 below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

**Table 19 - Sector Sizes**

| N | SECTOR SIZE |
|---|---|
| 00 | 128 bytes |
| 01 | 256 bytes |
| 02 | 512 bytes |
| 03 | 1024 bytes |
| .. | ... |
| 07 | 16 Kbytes |

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 22.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads, then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the $\overline{\text{INDEX}}$ pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the Read Data Command. Table 21 describes the effect of the SK bit on the Read Data command execution and results. Except where noted in Table 21, the C or R value of the sector address is automatically incremented (see Table 23).

**Table 20 - Effects of MT and N Bits**

| MT | N | MAXIMUM TRANSFER CAPACITY | FINAL SECTOR READ FROM DISK |
|---|---|---|---|
| 0 | 1 | 256 x 26 = 6,656 | 26 at side 0 or 1 |
| 1 | 1 | 256 x 52 = 13,312 | 26 at side 1 |
| 0 | 2 | 512 x 15 = 7,680 | 15 at side 0 or 1 |
| 1 | 2 | 512 x 30 = 15,360 | 15 at side 1 |
| 0 | 3 | 1024 x 8 = 8,192 | 8 at side 0 or 1 |
| 1 | 3 | 1024 x 16 = 16,384 | 16 at side 1 |

**Table 21 - Skip Bit vs Read Data Command**

| SK BIT VALUE | DATA ADDRESS MARK TYPE ENCOUNTERED | RESULTS | | |
|---|---|---|---|---|
| | | SECTOR READ? | CM BIT OF ST2 SET? | DESCRIPTION OF RESULTS |
| 0 | Normal Data | Yes | No | Normal termination. |
| 0 | Deleted Data | Yes | Yes | Address not incremented. Next sector not searched for. |
| 1 | Normal Data | Yes | No | Normal termination. |
| 1 | Deleted Data | No | Yes | Normal termination. Sector not read ("skipped"). |

**Read Deleted Data**

This command is the same as the Read Data command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 22 describes the effect of the SK bit on the Read Deleted Data command execution and results.

Except where noted in Table 22, the C or R value of the sector address is automatically incremented (see Table 23).

**Table 22 - Skip Bit vs. Read Deleted Data Command**

| SK BIT VALUE | DATA ADDRESS MARK TYPE ENCOUNTERED | RESULTS | | |
|---|---|---|---|---|
| | | SECTOR READ? | CM BIT OF ST2 SET? | DESCRIPTION OF RESULTS |
| 0 | Normal Data | Yes | Yes | Address not incremented. Next sector not searched for. |
| 0 | Deleted Data | Yes | No | Normal termination. |
| 1 | Normal Data | No | Yes | Normal termination. Sector not read ("skipped"). |
| 1 | Deleted Data | Yes | No | Normal termination. |

**Read A Track**

This command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the $\overline{\text{INDEX}}$ pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag of Status Register 1 to a "1" if there is no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors has not been read. If the FDC does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the IDX pin, then it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 23 - Result Phase Table

| MT | HEAD | FINAL SECTOR TRANSFERRED TO HOST | ID INFORMATION AT RESULT PHASE | | | |
|---|---|---|---|---|---|---|
| | | | C | H | R | N |
| 0 | 0 | Less than EOT | NC | NC | R + 1 | NC |
| | | Equal to EOT | C + 1 | NC | 01 | NC |
| | 1 | Less than EOT | NC | NC | R + 1 | NC |
| | | Equal to EOT | C + 1 | NC | 01 | NC |
| 1 | 0 | Less than EOT | NC | NC | R + 1 | NC |
| | | Equal to EOT | NC | LSB | 01 | NC |
| | 1 | Less than EOT | NC | NC | R + 1 | NC |
| | | Equal to EOT | C + 1 | LSB | 01 | NC |

NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented.

**Write Data**

After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the Specify command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the FDC continues writing to the next data field. The FDC continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the Write Data command.

The Write Data command operates in much the same manner as the Read Data command. The following items are the same. Please refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command
- Definition of DTL when N = 0 and when N does not = 0

**Write Deleted Data**

This command is almost the same as the Write Data command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address

Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

**Verify**

The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously-stored value.

Because data is not transferred to the host, TC (pin 25) cannot be used to terminate this command. By setting the EC bit to "1", an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decremented to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0", DTL/SC should be programmed to 0FFH. Refer to Table 23 and Table 24 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

# Sectors Per Side = Number of formatted sectors per each side of the disk.

# Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

**Table 24 - Verify Command Result Phase Table**

| MT | EC | SC/EOT VALUE | TERMINATION RESULT |
|---|---|---|---|
| 0 | 0 | SC = DTL<br>EOT ≤ # Sectors Per Side | Success Termination<br>Result Phase Valid |
| 0 | 0 | SC = DTL<br>EOT > # Sectors Per Side | Unsuccessful Termination<br>Result Phase Invalid |
| 0 | 1 | SC ≤ # Sectors Remaining AND<br>EOT ≤ # Sectors Per Side | Successful Termination<br>Result Phase Valid |
| 0 | 1 | SC > # Sectors Remaining OR<br>EOT > # Sectors Per Side | Unsuccessful Termination<br>Result Phase Invalid |
| 1 | 0 | SC = DTL<br>EOT ≤ # Sectors Per Side | Successful Termination<br>Result Phase Valid |
| 1 | 0 | SC = DTL<br>EOT > # Sectors Per Side | Unsuccessful Termination<br>Result Phase Invalid |
| 1 | 1 | SC ≤ # Sectors Remaining AND<br>EOT ≤ # Sectors Per Side | Successful Termination<br>Result Phase Valid |
| 1 | 1 | SC > # Sectors Remaining OR<br>EOT > # Sectors Per Side | Unsuccessful Termination<br>Result Phase Invalid |

NOTE: If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

**Format A Track**

The Format command allows an entire track to be formatted. After a pulse from the IDX pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields, and data fields per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host; that is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the IDX pin again and it terminates the command.

Table 25 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

## FORMAT FIELDS

### SYSTEM 34 (DOUBLE DENSITY) FORMAT

| GAP4a | SYNC | IAM | | GAP1 | SYNC | IDAM | | C | H | S | N | C | GAP2 | SYNC | DATA AM | | DATA | C | GAP3 | GAP 4b |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 80x 4E | 12x 00 | 3x C2 | FC | 50x 4E | 12x 00 | 3x A1 | FE | Y L | D | E C | O | R C | 22x 4E | 12x 00 | 3x A1 | FB F8 | | R C | | |

### SYSTEM 3740 (SINGLE DENSITY) FORMAT

| GAP4a | SYNC | IAM | GAP1 | SYNC | IDAM | C | H | S | N | C | GAP2 | SYNC | DATA AM | DATA | C | GAP3 | GAP 4b |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 40x FF | 6x 00 | FC | 26x FF | 6x 00 | FE | Y L | D | E C | O | R C | 11x FF | 6x 00 | FB or F8 | | R C | | |

### PERPENDICULAR FORMAT

| GAP4a | SYNC | IAM | | GAP1 | SYNC | IDAM | | C | H | S | N | C | GAP2 | SYNC | DATA AM | | DATA | C | GAP3 | GAP 4b |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 80x 4E | 12x 00 | 3x C2 | FC | 50x 4E | 12x 00 | 3x A1 | FE | Y L | D | E C | O | R C | 41x 4E | 12x 00 | 3x A1 | FB F8 | | R C | | |

Table 25 - Typical Values for Formatting

| | FORMAT | SECTOR SIZE | N | SC | GPL1 | GPL2 |
|---|---|---|---|---|---|---|
| 5.25" Drives | FM | 128 | 00 | 12 | 07 | 09 |
| | | 128 | 00 | 10 | 10 | 19 |
| | | 512 | 02 | 08 | 18 | 30 |
| | | 1024 | 03 | 04 | 46 | 87 |
| | | 2048 | 04 | 02 | C8 | FF |
| | | 4096 | 05 | 01 | C8 | FF |
| | | ... | ... | | | |
| | MFM | 256 | 01 | 12 | 0A | 0C |
| | | 256 | 01 | 10 | 20 | 32 |
| | | 512* | 02 | 09 | 2A | 50 |
| | | 1024 | 03 | 04 | 80 | F0 |
| | | 2048 | 04 | 02 | C8 | FF |
| | | 4096 | 05 | 01 | C8 | FF |
| | | ... | ... | | | |
| 3.5" Drives | FM | 128 | 0 | 0F | 07 | 1B |
| | | 256 | 1 | 09 | 0F | 2A |
| | | 512 | 2 | 05 | 1B | 3A |
| | MFM | 256 | 1 | 0F | 0E | 36 |
| | | 512** | 2 | 09 | 1B | 54 |
| | | 1024 | 3 | 05 | 35 | 74 |

GPL1 = suggested GPL values in Read and Write commands to avoid splice point between data field and ID field of contiguous sections.
GPL2 = suggested GPL value in Format A Track command.
*PC/AT values (typical)
**PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives.
NOTE: All values except sector size are in hex.

## CONTROL COMMANDS

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete: Read ID, Recalibrate, and Seek. The other control commands do not generate an interrupt.

### Read ID

The Read ID command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the $\overline{\text{INDEX}}$ pin, it then sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. The do not return any result bytes. It is highly recommended that control commands be followed by the Sense Interrupt Status command. Otherwise, valuable interrupt status information will be lost.

### Recalibrate

This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the $\overline{\text{TR0}}$ pin from the FDD. As long as the $\overline{\text{TR0}}$ pin is low, the DIR pin remains 0 and step pulses are issued. When the $\overline{\text{TR0}}$ pin goes high, the SE bit in Status Register 0 is set to "1" and the command is terminated. If the $\overline{\text{TR0}}$ pin is still low after 79 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to "1" and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one Recalibrate command to return the head back to physical Track 0.

The Recalibrate command does not have a result phase. The Sense Interrupt Status command must be issued after the Recalibrate command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in a NON-BUSY state. At this time, another Recalibrate command may be issued, and in this manner parallel Recalibrate operations may be done on up to four drives at once.

Upon power up, the software must issue a Recalibrate command to properly initialize all drives and the controller.

### Seek

The read/write head within the drive is moved from track to track under the control of the Seek command. The FDC compares the PCN, which is the current head position, with the NCN and performs the following operation if there is a difference:

| | |
|---|---|
| PCN < NCN: | Direction signal to drive set to "1" (step in) and issues step pulses. |
| PCN > NCN: | Direction signal to drive set to "0" (step out) and issues step pulses. |

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN the SE bit in Status Register 0 is set to "1" and the command is terminated.

During the command phase of the seek or recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in the NON-BUSY state. At this time, another Seek or Recalibrate command may be issued, and in this manner, parallel seek operations may be done on up to four drives at once.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1) Seek command - Step to the proper track
2) Sense Interrupt Status command - Terminate the Seek command
3) Read ID - Verify head is on proper track
4) Issue Read/Write command.

The Seek command does not have a result phase. Therefore, it is highly recommended that the Sense Interrupt Status command be issued after the Seek command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return to a "0". When exiting POWERDOWN mode, the FDC clears the PCN value and the status information to zero. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the Sense Interrupt Status command.

**Sense Interrupt Status**

An interrupt signal on FINT pin is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Track command
   g. Write Deleted Data command
   h. Verify command

2. End of Seek, Relative Seek, or Recalibrate command

3. FDC requires a data transfer during the execution phase in the non-DMA mode

The Sense Interrupt Status command resets the interrupt signal and, via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

**Table 26 - Interrupt Identification**

| SE | IC | INTERRUPT DUE TO |
|---|---|---|
| 0 | 11 | Polling |
| 1 | 00 | Normal termination of Seek or Recalibrate command |
| 1 | 01 | Abnormal termination of Seek or Recalibrate command |

The Seek, Relative Seek, and Recalibrate commands have no result phase. The Sense Interrupt Status command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a Sense Interrupt Status is not issued, the drive will continue to be BUSY and may affect the operation of the next command.

**Sense Drive Status**

Sense Drive Status obtains drive status information. It has not execution phase and goes directly to the result phase from the command phase. Status Register 3 contains the drive status information.

**Specify**

The Specify command sets the initial values for each of the three internal times. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between when the Head Load signal

goes high and the read/write operation starts. The values change with the data rate speed selection and are documented in Table 27. The values are the same for MFM and FM.

**Table 27 - Drive Control Delays (ms)**

| | HUT | | | | SRT | | | |
|---|---|---|---|---|---|---|---|---|
| | 1M | 500K | 300K | 250K | 1M | 500K | 300K | 250K |
| 0 | 128 | 256 | 426 | 512 | 8.0 | 16 | 26.7 | 32 |
| 1 | 8 | 16 | 26.7 | 32 | 7.5 | 15 | 25 | 30 |
| .. | .. | .. | .. | .. | .. | .. | .. | .. |
| E | 112 | 224 | 373 | 448 | 1.0 | 2 | 3.33 | 4 |
| F | 120 | 240 | 400 | 480 | 0.5 | 1 | 1.67 | 2 |

| | HLT | | | |
|---|---|---|---|---|
| | 1M | 500K | 300K | 250K |
| 00 | 128 | 256 | 426 | 512 |
| 01 | 1 | 2 | 3.3 | 4 |
| 02 | 2 | 4 | 6.7 | 8 |
| .. | .. | .. | .. | . |
| 7F | 126 | 252 | 420 | 504 |
| 7F | 127 | 254 | 423 | 508 |

The choice of DMA or non-DMA operations is made by the ND bit. When this bit is "1", the non-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signalled by the FDRQ pin. Non-DMA mode uses the RQM bit and the FINT pin to signal data transfers.

**Configure**

The Configure command is issued to select the special features of the FDC. A Configure command need not be issued if the default values of the FDC meet the system requirements.

Configure Default Values:

EIS - No Implied Seeks
EFIFO - FIFO Disabled
POLL - Polling Enabled
FIFOTHR - FIFO Threshold Set to 1 Byte
PRETRK - Pre-Compensation Set to Track 0

EIS - Enable Implied Seek. When set to "1", the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO - A "1" disables the FIFO (default). This means data transfers are asked for on a byte-by-byte basis. Defaults to "1", FIFO disabled. The threshold defaults to "1".

POLL - Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR - The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte; "0F" selects 16 bytes.

PRETRK - Pre-Compensation Start Track Number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0; "FF" selects track 255.

**Version**

The Version command checks to see if the controller is an enhanced type or the older type (765A). A value of 90 H is returned as the result byte.

**Relative Seek**

The command is coded the same as for Seek, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control

| DIR | ACTION |
|---|---|
| 0 | Step Head Out |
| 1 | Step Head In |

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

The Relative Seek command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time. Relative Seeks may be overlapped with Seeks and Recalibrates. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks. The host needs to read track 300 and the head is on any track (0-255). If a Seek command is issued, the head will stop at track 255. If a Relative Seek command is issued, the FDC will move the head the specified number of tracks, regardless of the internal cylinder position register (but will increment the register). If the head was on track 40 (d), the maximum track that the FDC could position the head on using Relative Seek will be 296 (D); the initial track + 256 (D). The maximum count that the head can be moved with a single Relative Seek command is 256 (D).

The internal register, PCN, will overflow as the cylinder number crosses track 255 and will contain 40 (D). The resulting PCN value is thus (NCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255 (D). It is the user's responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an "extended track area" (greater than 255). Any command issued will use the current PCN value except for the Recalibrate command, which only looks for the TRACK0 signal. Recalibrate will return an error if the head is farther than 79 due to its limitation of issuing a maximum of 80 step pulses. The user simply needs to issue a second Recalibrate command. The Seek command and implied seeks will function correctly within the 44 (D) track (299-255) area of the "extended track area". It is the user's responsibility not to issue a new track position that will exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0-255) of tracks, a Relative Seek should be issued to cross the track 255 boundary.

A Relative Seek can be used instead of the normal Seek, but the host is required to calculate the difference between the current head location and the new (target) head

location. This may require the host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands will return different cylinder results which may be difficult to keep track of with software without the Read ID command.

**Perpendicular Mode**

The Perpendicular Mode command should be issued prior to executing Read/Write/Format commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 24 describes the effects of the WGATE and GAP bits for the Perpendicular Mode command. Upon a reset, the FDC will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register. The user must ensure that these two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The format field shown on page 62 illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the FDC, the controller must begin synchronization at the beginning of the sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But, when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, and approximate two-byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the Write Data case, the FDC activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC as shown in Figure 4. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP = 0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the Perpendicular Mode command is invoked, FDC software behavior from the user standpoint is unchanged.

The perpendicular mode command is enhanced to allow specific drives to be designated Perpendicular recording drives. This

enhancement allows data transfers between Conventional and Perpendicular drives without having to issue Perpendicular mode commnds between the accesses of the different drive types, nor having to change write pre-compensation values.

When both GAP and WGATE bits of the PERPENDICULAR MODE COMMAND are both programmed to "0" (Conventional mode), then D0, D1, D2, D3, and D4 can be programmed independently to "1" for that drive to be set automatically to Perpendicular mode. In this mode the following set of conditions also apply:

1. The GAP2 written to a perpendicular drive during a write operation will depend upon the programmed data rate.
2. The write pre-compensation given to a perpendicular mode drive wil be 0ns.
3. For D0-D3 programmed to "0" for conventional mode drives any data written will be at the currently programmed write pre-compensation.

Note: Bits D0-D3 can only be overwritten when OW is programmed as a "1". If either GAP or WGATE is a "1" then D0-D3 are ignored.

Software and hardware resets have the following effect on the PRPENDICULAR MODE COMMAND:

1. "Software" resets (via the DOR or DSR registers) will only clear GAP and WGATE bits to "0". D0-D3 are unaffected and retain their previous value.
2. "Hardware" resets will clear all bits ( GAP, WGATE and D0-D3) to "0", i.e all conventional mode.

**Table 28 - Effects of WGATE and GAP Bits**

| WGATE | GAP | MODE | LENGTH OF GAP2 FORMAT FIELD | PORTION OF GAP 2 WRITTEN BY WRITE DATA OPERATION |
|---|---|---|---|---|
| 0 | 0 | Conventional | 22 Bytes | 0 Bytes |
| 0 | 1 | Perpendicular (500 Kbps) | 22 Bytes | 19 Bytes |
| 1 | 0 | Reserved (Conventional) | 22 Bytes | 0 Bytes |
| 1 | 1 | Perpendicular (1 Mbps) | 41 Bytes | 38 Bytes |

**LOCK**

In order to protect systems with long DMA latencies against older application software that can disable the FIFO the LOCK Command has been added. This command should only be used by the FDC routines, and application software should refrain from using it. If an application calls for the FIFO to be disabled then the CONFIGURE command should be used.

The LOCK command defines whether the EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to logic "1" all subsequent "software RESETS by the DOR and DSR registers will not change the previously set parameters to their default values. All "hardware" RESET from the RESET pin will set the LOCK bit to logic "0" and return the EFIFO, FIFOTHR, and PRETRK to

their default values. A status byte is returned immediately after issuing a a LOCK command. This byte reflects the value of the LOCK bit set by the command byte.

**ENHANCED DUMPREG**

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. To accommodate the LOCK command and the enhanced PERPENDICULAR MODE command the eighth byte of the DUMPREG command has been modified to contain the additional data from these two commands.

**COMPATIBILITY**

The FDC37C661/662 was designed with software compatibility in mind. It is a fully backwards-compatible solution with the older generation 765A/B disk controllers. The FDC also implements on-board registers for compatibility with the PS/2, as well as PC/AT and PC/XT, floppy disk controller subsystems. After a hardware reset of the FDC, all registers, functions and enhancements default to a PC/AT, PS/2 or PS/2 Model 30 compatible operating mode, depending on how the IDENT and MFM bits are configured by the system bios.

## SERIAL PORT (UART)

The FDC37C661 and FDC37C662 incorporate two full function UARTs. They are compatible with the NS16450 and the 16450 ACE registers. The UARTs perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 115.2K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. Refer to the FDC37C661 Configuration Registers and FDC37C662 Hardware Configuration description for information on disabling, power down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt.

### REGISTER DESCRIPTION

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Configuration section). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The FDC37C661 contains two serial ports, each of which contain a register set as described below.

**Table 29 - Addressing the Serial Port**

| DLAB* | A2 | A1 | A0 | REGISTER NAME |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Receive Buffer (read) |
| 0 | 0 | 0 | 0 | Transmit Buffer (write) |
| 0 | 0 | 0 | 1 | Interrupt Enable (read/write) |
| X | 0 | 1 | 0 | Interrupt Identification (read) |
| X | 0 | 1 | 1 | Line Control (read/write) |
| X | 1 | 0 | 0 | Modem Control (read/write) |
| X | 1 | 0 | 1 | Line Status (read/write) |
| X | 1 | 1 | 0 | Modem Status (read/write) |
| X | 1 | 1 | 1 | Scratchpad (read/write) |
| 1 | 0 | 0 | 0 | Divisor LSB (read/write) |
| 1 | 0 | 0 | 1 | Divisor MSB (read/write) |

*NOTE: DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

**RECEIVE BUFFER REGISTER (RB)**
**Address Offset = 0H, DLAB = 0, READ ONLY**

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

**TRANSMIT BUFFER REGISTER (TB)**
**Address Offset = 0H, DLAB = 0, WRITE ONLY**

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

**INTERRUPT ENABLE REGISTER (IER)**
**Address Offset = 1H, DLAB = 0, READ/WRITE**

The lower four bits of this register control the enables of the four interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the FDC37C661. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

**Bit 0**
This bit enables the Received Data Available Interrupt when set to logic "1".

**Bit 1**
This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

**Bit 2**
This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

**Bit 3**
This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

**Bits 4 through 7**
These bits are always logic "0".

**INTERRUPT IDENTIFICATION REGISTER (IIR)**
**Address Offset = 2H, DLAB = X, READ**

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

**Bit 0**
This bit can be used in either a hardwired

prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

**Bits 1 and 2**
These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

**Bits 3 through 7**
These bits of the IIR are always logic "0".

**Table 30 - Interrupt Control Table**

| INTERRUPT IDENTIFICATION REGISTER | | | INTERRUPT SET AND RESET FUNCTIONS | | | |
|---|---|---|---|---|---|---|
| BIT 2 | BIT 1 | BIT 0 | PRIORITY LEVEL | INTERRUPT TYPE | INTERRUPT SOURCE | INTERRUPT RESET CONTROL |
| 0 | 0 | 1 | - | None | None | - |
| 1 | 1 | 0 | Highest | Receiver Line Status | Overrun Error, Parity Error, Framing Error or Break Interrupt | Reading the Line Status Register |
| 1 | 0 | 0 | Second | Received Data Available | Receiver Data Available | Read Receiver Buffer |
| 0 | 1 | 0 | Third | Transmitter Holding Register Empty | Transmitter Holding Register Empty | Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register |
| 0 | 0 | 0 | Fourth | MODEM Status | Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect | Reading the MODEM Status Register |

**LINE CONTROL REGISTER (LCR)**
**Address Offset = 3H, DLAB = X, READ/WRITE**

This register contains the format information of the serial line. The bit definitions are:

**Bits 0 and 1**
These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

| BIT 1 | BIT 0 | WORD LENGTH |
|---|---|---|
| 0 | 0 | 5 Bits |
| 0 | 1 | 6 Bits |
| 1 | 0 | 7 Bits |
| 1 | 1 | 8 Bits |

The Start, Stop and Parity bits are not included in the word length.

**Bit 2**
This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

| BIT 2 | WORD LENGTH | NUMBER OF STOP BITS |
|---|---|---|
| 0 | – | 1 |
| 1 | 5 bits | 1.5 |
| 1 | 6 bits | 2 |
| 1 | 7 bits | 2 |
| 1 | 8 bits | 2 |

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

**Bit 3**
Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

**Bit 4**
Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

**Bit 5**
Stick Parity bit. When bit 3 is a logic "1" and bit 5 is a logic "1", the parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

**Bit 6**
Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

**Bit 7**
Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

**MODEM CONTROL REGISTER (MCR)**
**Address Offset = 4H, DLAB = X, READ/WRITE**

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

**Bit 0**
This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic "1", the $\overline{DTR}$ output is forced to a logic "0". When bit

0 is a logic "0", the $\overline{DTR}$ output is forced to a logic "1".

**Bit 1**
This bit controls the Request To Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

**Bit 2**
This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

**Bit 3**
Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

**Bit 4**
This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1. The TXD is set to the Marking State (logic "1").
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. All MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$) are disconnected.
5. The four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, and OUT2) are internally connected to the four MODEM Control inputs.
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

**Bits 5 through 7**
These bits are permanently set to logic zero.

**LINE STATUS REGISTER (LSR)**
**Address Offset = 5H, DLAB = X, READ/WRITE**

**Bit 0**
Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will be reset to a logic "0" by the read of the data in the Receiver Buffer Register.

**Bit 1**
Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. The OE indicator is reset whenever the Line Status Register is read.

**Bit 2**
Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read.

**Bit 3**
Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. The Serial Port will try to

resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

**Bit 4**
Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

**Bit 5**
Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. Bit 5 is a read only bit.

**Bit 6**
Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit.

**Bit 7**
This bit is permanently set to logic "0".

**MODEM STATUS REGISTER (MSR)**
**Address Offset = 6H, DLAB = X, READ/WRITE**

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic one whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

**Bit 0**
Delta Clear To Send (DCTS). Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time the MSR was read.

**Bit 1**
Delta Data Set Ready (DDSR). Bit 1 indicates that the $\overline{DSR}$ input has changed state since the last time the MSR was read.

**Bit 2**
Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the $\overline{RI}$ input has changed from logic "0" to logic "1".

**Bit 3**
Delta Data Carrier Detect (DDCD). Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.
NOTE: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

**Bit 4**
This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to $\overline{RTS}$ in the MCR.

**Bit 5**
This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

**Bit 6**
This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

**Bit 7**
This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

**SCRATCHPAD REGISTER (SCR)**
**Address Offset = 7H, DLAB = X, READ/WRITE**

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

**PROGRAMMABLE BAUD RATE GENERATOR (AND DIVISOR LATCHES DLH, DLL)**

The Serial Port contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3 MHz) and dividing it by any divisor from 1 to 65535. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is the 24 MHz crystal divided by 13, giving a 1.8462 MHz clock.

Table 32 shows the baud rates possible with a 1.8462 MHz crystal.

**Effect Of The Reset on Register File**

The Reset Function Table (Table 33) details the effect of the Reset input on each of the registers of the Serial Port.

Table 31 - Register Summary for an Individual UART Channel

| REGISTER ADDRESS* | REGISTER NAME | REGISTER SYMBOL | BIT 0 | BIT 1 |
|---|---|---|---|---|
| ADDR = 0<br>DLAB = 0 | Receive Buffer Register (Read Only) | RBR | Data Bit 0 (Note 1) | Data Bit 1 |
| ADDR = 0<br>DLAB = 0 | Transmitter Holding Register (Write Only) | THR | Data Bit 0 | Data Bit 1 |
| ADDR = 1<br>DLAB = 0 | Interrupt Enable Register | IER | Enable Received Data Available Interrupt (ERDAI) | Enable Transmitter Holding Register Empty Interrupt (ETHREI) |
| ADDR = 2 | Interrupt Ident. Register (Read Only) | IIR | "0" if Interrupt Pending | Interrupt ID Bit |
| ADDR = 3 | Line Control Register | LCR | Word Length Select Bit 0 (WLS0) | Word Length Select Bit 1 (WLS1) |
| ADDR = 4 | MODEM Control Register | MCR | Data Terminal Ready (DTR) | Request to Send (RTS) |
| ADDR = 5 | Line Status Register | LSR | Data Ready (DR) | Overrun Error (OE) |
| ADDR = 6 | MODEM Status Register | MSR | Delta Clear to Send (DCTS) | Delta Data Set Ready (DDSR) |
| ADDR = 7 | Scratch Register (Note 4) | SCR | Bit 0 | Bit 1 |
| ADDR = 0<br>DLAB = 1 | Divisor Latch (LS) | DDL | Bit 0 | Bit 1 |
| ADDR = 1<br>DLAB = 1 | Divisor Latch (MS) | DLM | Bit 8 | Bit 9 |

Table 31 - Register Summary for an Individual UART Channel (continued)

| BIT 2 | BIT 3 | BIT 4 | BIT 5 | BIT 6 | BIT 7 |
|---|---|---|---|---|---|
| Data Bit 2 | Data Bit 3 | Data Bit 4 | Data Bit 5 | Data Bit 6 | Data Bit 7 |
| Data Bit 2 | Data Bit 3 | Data Bit 4 | Data Bit 5 | Data Bit 6 | Data Bit 7 |
| Enable Receiver Line Status Interrupt (ELSI) | Enable MODEM Status Interrupt (EMSI) | 0 | 0 | 0 | 0 |
| Interrupt ID Bit | 0 | 0 | 0 | 0 | 0 |
| Number of Stop Bits (STB) | Parity Enable (PEN) | Even Parity Select (EPS) | Stick Parity | Set Break | Divisor Latch Access Bit (DLAB) |
| OUT1 (Note 3) | OUT2 (Note 3) | Loop | 0 | 0 | 0 |
| Parity Error (PE) | Framing Error (FE) | Break Interrupt (BI) | Transmitter Holding Register (THRE) | Transmitter Empty (TEMT) (Note 2) | 0 |
| Trailing Edge Ring Indicator (TERI) | Delta Data Carrier Detect (DDCD) | Clear to Send (CTS) | Data Set Ready (DSR) | Ring Indicator (RI) | Data Carrier Detect (DCD) |
| Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 |
| Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 |
| Bit 10 | Bit 11 | Bit 12 | Bit 13 | Bit 14 | Bit 15 |

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.
Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.

**Table 32 - Baud Rates Using 1.8462 MHz Clock (24 MHz/13)**

| DESIRED BAUD RATE | DIVISOR USED TO GENERATE 16X CLOCK | PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL* |
|---|---|---|
| 50 | 2304 | 0.1 |
| 75 | 1536 | - |
| 110 | 1047 | - |
| 134.5 | 857 | 0.4 |
| 150 | 768 | - |
| 300 | 384 | - |
| 600 | 192 | - |
| 1200 | 96 | - |
| 1800 | 64 | - |
| 2000 | 58 | 0.5 |
| 2400 | 48 | - |
| 3600 | 32 | - |
| 4800 | 24 | - |
| 7200 | 16 | - |
| 9600 | 12 | - |
| 19200 | 6 | - |
| 38400 | 3 | 0.16 |
| 56000 | 2 | 3 |
| 115200 | 1 | 0.16 |

*Note: The percentage error for all baud rates, except where indicated otherwise, is 0.2%.

Table 33 - Reset Function Table

| REGISTER/SIGNAL | RESET CONTROL | RESET STATE |
|---|---|---|
| Interrupt Enable Register | RESET | All bits low |
| Interrupt Identification Reg. | RESET | Bit 0 is high; Bits 1, 2 low |
| Line Control Reg. | RESET | All bits low |
| MODEM Control Reg. | RESET | All bits low |
| Line Status Reg. | RESET | All bits low except 5, 6 high |
| MODEM Status Reg. | RESET | Bits 0 - 3 low; Bits 4 - 7 input |
| TXD1, TXD2 | RESET | High |
| INTRPT (RCVR errs) | RESET/Read LSR | Low |
| INTRPT (RCVR Data Ready) | RESET/Read RBR | Low |
| INTRPT (THRE) | RESET/ReadIIR/Write THR | Low |
| OUT2B | RESET | High |
| RTSB | RESET | High |
| DTRB | RESET | High |
| OUT1B | RESET | High |

## PARALLEL PORT

The FDC37C661 and FDC37C662 incorporate one IBM XT/AT compatible parallel port. The FDC37C661 supports the optional PS/2 type bi-directional parallel port mode. Refer to the FDC37C661 Configuration Registers and FDC37C662 Hardware Configuration description for information on disabling, power down and changing the base address of the parallel port.

The FDC37C661 and FDC37C662 incorporate protection circuitry which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of three addressable ports, with their associated registers and control gating. These ports are:

DATA PORT
CONTROL PORT
STATUS PORT

The control and data port are read write by the CPU, while the status port is read only. The address map of the Parallel Port is shown below:

| | |
|---|---|
| DATA PORT | BASE ADDRESS + 00H |
| STATUS PORT | BASE ADDRESS + 01H |
| CONTROL PORT | BASE ADDRESS + 02H |

The bit map of these registers is:

| | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
|---|---|---|---|---|---|---|---|---|
| DATA PORT | PD0 | PD1 | PD2 | PD3 | PD4 | PD5 | PD6 | PD7 |
| STATUS PORT | 0 | 0 | 0 | $\overline{ERR}$ | SLCT | PE | $\overline{ACK}$ | $\overline{BUSY}$ |
| CONTROL PORT | STROBE | AUTOFD | $\overline{INIT}$ | SLC | IRQE | PCD | 0 | 0 |

**DATA PORT**
**ADDRESS OFFSET = 00H**

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the controls of the data bus rising edge of the $\overline{IOW}$ input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

**STATUS PORT**
**ADDRESS OFFSET = 01H**

The Status Port is located at an offset of '01H' from the base address. Bits 0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

**BIT 3 $\overline{ERR}$ - $\overline{ERROR}$**
The level on the $\overline{ERROR}$ input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

**BIT 4 SLCT - PRINTER SELECTED STATUS**
The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

**BIT 5 PE - PAPER END**
The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

**BIT 6 $\overline{\text{ACK}}$ - $\overline{\text{ACKNOWLEDGE}}$**
The level on the $\overline{\text{ACK}}$ input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

**BIT 7 $\overline{\text{BUSY}}$ - $\overline{\text{BUSY}}$**
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic 1 means that it is ready to accept the next character.

**CONTROL PORT**
**ADDRESS OFFSET = 02H**

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 4 only being affected; bits 5, 6 and 7 are hard wired low.

**BIT 0 STROBE - STROBE**
This bit is inverted and output onto the $\overline{\text{STROBE}}$ output.
**BIT 1 AUTOFD - AUTOFEED**
This bit is inverted and output onto the $\overline{\text{AUTOFD}}$ output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

**BIT 2 $\overline{\text{INIT}}$ - $\overline{\text{INITIATE OUTPUT}}$**
This bit is output onto the $\overline{\text{INIT}}$ output without inversion.

**BIT 3 SLCTIN - PRINTER SELECT INPUT**
This bit is inverted and output onto the $\overline{\text{SLCTIN}}$ output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

**BIT 4 IRQE - INTERRUPT REQUEST ENABLE**
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going $\overline{\text{ACK}}$ input. When the IRQE bit is programmed low the IRQ is disabled.

**BIT 5 PCD - PARALLEL CONTROL DIRECTION**
Parallel Control Direction is valid in extended mode only (CR#1<3> = 0). In printer mode, the direction is always out regardless of the state of this bit. In extended mode, a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

## INTEGRATED DRIVE ELECTRONICS INTERFACE

The IDE interface enables hard disks with embedded controllers (AT and XT) to be interfaced to the host processor. The following definitions are for reference only. These registers are not implemented in the FDC37C661 and FDC37C662. Access to these registers are controlled by the FDC37C661 and FDC37C662. For more information, refer to the IDE pin descriptions.

### HOST FILE REGISTERS

The HOST FILE REGISTERS are accessed by the AT Host, rather than the Local Processor. There are two groups of registers, the AT Task File, and the Miscellaneous AT Registers.

ADDRESS 1F0H-1F7H

The address space from 1F0H to 1F7H contains the Task File Registers. These registers communicate data, command, and status information with the AT host, and are addressed when $\overline{HDCS0}$ is low.

ADDRESS 3F6H; 3F7H

These AT registers may be used by the BIOS for drive control. They are accessed by the AT interface when $\overline{HDSC1}$ is active.

Figure 3 shows the AT Host Register Map of the FDC37C661 and FDC37C662.

**FIGURE 3 - HOST PROCESSOR REGISTER ADDRESS MAP**

| | |
|---|---|
| 000H<br>\|<br>007H | TASK FILE REGISTERS |
| 3F6H<br>\|<br>3F7H | MISC AT REGISTERS |

### TASK FILE REGISTERS

Task File Registers may be accessed by the host AT when pin $\overline{HDCS0}$ is active (low). The Data Register (1F0H) is 16 bits wide; the remaining task file registers are 8 bits wide. The task file registers are ATA and EATA compatible.

### DATA (READ/WRITE) - 1F0H

The DATA REGISTER provides a 16 bit data path to the IDE disk drive. Programmed I/O data transfers between the host and the disk are through this register. In addition, the sector table is transferred through the data register during format commands.

### ERROR (READ) - 1F1H

This read-only register contains the status from the last command executed by the drive when the error bit (Register 1F8H, bit D0) is set. If the drive has just been powered up, or has just completed internal diagnostic testing, this register should contain a status code.

BIT D7: BAD BLOCK DETECT

D7 = 1: A bad block mark was detected by the controller in the requested sector's ID field.

BIT D6: UNCORRECTABLE DATA ERROR

D6 = 1: An ECC or CRC error has been encountered in the data.

BIT D4: ID NOT FOUND

D4 = 1: A sync error (correct cylinder, head, sector number, or sector size parameter could not be found) or CRC error has been encountered in any command phase other than the data phase.

BIT D2: ABORTED COMMAND

D2 = 1: The requested command has been aborted due to a drive status error. This indicates that either the command was invalid, or the drive specified in the HEAD/DRIVE register did not have Drive Ready Asserted.

BIT D1: TRACK ZERO NOT FOUND

D1 = 1: After receiving a Restore Command, the drive has generated Seek Complete, but not Track 0.

BIT D0: DATA ADDRESS MARK NOT FOUND

D0 = 1: The controller is reporting a Sync error (missing address mark) in the data phase of a command.

**WRITE PRECOMP CYLINDER/FEATURES (WRITE) - 1F1H**

This register is written by the host AT. This register is typically used to define the cylinder number where the write precompensation is to be asserted.

**SECTOR COUNT (READ/WRITE) - 1F2H**

This register is read and written by the host AT. This register is used to store the number of sectors that are to be transferred across the host bus for the subsequent command.

**SECTOR NUMBER (READ/WRITE) - 1F3H**

This register is read and written by the host AT. This register is used to store the sector number for any disk data access for the subsequent command. During a multiple sector command, this register is used to specify the first sector in the transfer.

**CYLINDER LOW (READ/WRITE) - 1F4H**

This register is read and written by the host AT. This register is used to store the 8 least significant bits of the desired cylinder number.

**CYLINDER HIGH (READ/WRITE) - 1F5H**

This register is read and written by the host AT. This register is used to store the 8 most significant bits of the desired cylinder number.

**HEAD, DRIVE (READ/WRITE) - 1F6H**

This register is read and written by the host AT.

**COMMAND (WRITE) - 1F7H**

COMMAND REGISTER 1F7H is a write-only register for the AT host. When the COMMAND REGISTER is written, the IDE drive will execute the specified command.

The commands are as follows:

| COMMAND | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| RESTORE (RECALIBRATE) | 0 | 0 | 0 | 1 | r | r | r | r |
| SEEK | 0 | 1 | 1 | 1 | r | r | r | r |
| READ SECTOR | 0 | 0 | 1 | 0 | D | 0 | L | T |
| WRITE SECTOR | 0 | 0 | 1 | 1 | D | 0 | L | T |
| FORMAT TRACK | 0 | 1 | 0 | 1 | D | 0 | 0 | 0 |
| READ VERIFY | 0 | 1 | 0 | 0 | D | 0 | 0 | T |
| DIAGNOSE | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| SET PARAMETERS | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

Bit definitions:

r: specifies the step rate to be used for the command.
D: If set, 16 bit DMA is to be used for the data transfer. (Optional for high performance)
L: If set, the ECC will be transferred following the data.
T: if set, retries are inhibited for the command.

**AT_STATUS (READ) - 1F7H**

This register is read by the host AT. Status is provided by the IDE drive. A read of this register clears the host interrupt signal.

BIT D7: BUSY

BUSY is set by any of the following conditions:

1. Hard reset.
2. Soft reset. A soft reset is initiated by the host processor setting and resetting the RESET bit of the FIXED DISK REGISTER (Bit D2, 3F6/376H).
3. During execution of a command.

BUSY is made inactive, but not cleared, while DRQ (bit D3 of this register) is active.

BIT D6: DRIVE READY

Bit D6 indicates the Ready status of the drive.

BIT D5: WRITE FAULT

Bit D5 indicates the write fault status of the drive.

BIT D4: SEEK COMPLETE

Bit D4 indicates the seek status of the drive.

BIT D3: DATA REQUEST

When set, Bit D3 indicates that the drive is ready for transfer of a word or byte of data between the host and the disk drive.

BIT D2: CORRECTED DATA

When set, Bit D2 indicates that a correctable data error has been encountered and the data has been corrected.

BIT D1: INDEX

Bit D1 is the latched status of the Index pulse. This bit is cleared by reading the AT_STATUS register.

BIT D0: ERROR

When set, Bit D0 indicates that the previous command ended in an error.

**MISCELLANEOUS AT REGISTERS**

The miscellaneous AT registers provide the AT interface with drive control and status. They are typically used by the BIOS for drive control. These registers are read or written by the AT interface when $\overline{\text{HDCS1}}$ is active (low).

**FIXED DISK (WRITE) - 3F6**

BITS D7-D4: RESERVED

BIT D3: HEAD SELECT 3 ENABLE

HS3EN is set by the Host AT to specify that the $\overline{\text{HS3}}$ signal of the ST-506 drive interface is used to access heads 8 through 15 when the HD SEL 3 bit of the DRIVE/HEAD Register (06H, bit D3). When this bit is low, the $\overline{\text{HS3}}$ signal is used to enable the reduce write current function of the drive.

BIT D2: ADAPTER RESET (RST)

The AT Host may issue a software reset by setting this bit.

BIT D1: DISABLE INTERRUPT REQUEST

The AT Host setting this bit will disable the IRQ output.

BIT D0: RESERVED

**ALTERNATE STATUS (READ) - 3F6**

The ALTERNATE STATUS REGISTER contains the same information as provided in the STATUS REGISTER 1F7H with the difference that a read of this register does not clear the interrupt to the host processor.

For information on the bit definitions, please refer to STATUS REGISTER 1F7H (READ).

**DIGITAL INPUT REGISTER (READ) - 3F7**

This register contains information from the HEAD/DRIVE register and the drive write gate.

BIT D7: NOT USED

BIT D6: $\overline{\text{WGATE}}$

BIT D6 indicates the status of the $\overline{\text{WRITE GATE}}$ output from the disk drive.

BITS D5-D2: $\overline{\text{HEAD SELECT3-0}}$

BITS D5-D2 indicate the contents of the head select bits in the HEAD/DRIVE register. (Bits D3-D0 of register 1F6H.

BIT D1: $\overline{\text{DRIVE SELECT 1}}$

BIT D1 is active low when bit D4 of the HEAD/DRIVE register (1F6H) is set.

BIT D0: $\overline{\text{DRIVE SELECT 0}}$

BIT D0 is active low when bit D3 of the HEAD/DRIVE register (1F6H) is set.

## AT HOST ADDRESSABLE REGISTERS
### (For Reference Only)

### TASK FILE REGISTERS

| ADDR | R/W | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000H | R/W | DATA REGISTER (REDIRECTED TO FIFO) | | | | | | | | | | | | | | | | DATA REG |

| ADDR | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | NAME |
|---|---|---|---|---|---|---|---|---|---|---|
| 001H | R | BB | CRC | - | ID | - | AC | TK | DM | ERROR FLAGS |
| 001H | W | CYLINDER NUMBER + 4 | | | | | | | | WRITE PRECOMP CYLINDER |
| 002H | R/W | NUMBER OF SECTORS | | | | | | | | SECTOR COUNT |
| 003H | R/W | SECTOR NUMBER | | | | | | | | SECTOR NUMBER |
| 004H | R/W | CYLINDER NUMBER (LSB'S) | | | | | | | | CYLINDER LOW |
| 005H | R/W | CYLINDER NUMBER (MSB'S) | | | | | | | | CYLINDER HIGH |
| 006H | R/W | - | - | DRIVE | HEAD | | | | | HEAD, DRIVE |
| 007H | R | BSY | RDY | WF | SC | DRQ | CD | INDEX | ERR | STATUS |
| 007H | W | COMMAND | | | | | | | | COMMAND |

## MISCELLANEOUS AT REGISTERS

| ADDR | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | NAME |
|---|---|---|---|---|---|---|---|---|---|---|
| 3F6H/ 376H | R | BSY | RDY | WF | SC | DRQ | CD | INDEX | ERR | STATUS |
| 3F6H/ 376H | W | RESERVED | | | | HS3EN | ADPTR RESET | DISABLE IRQ | RE-SERVED | FIXED DISK |
| 3F7H/ 377H | R | - | $\overline{WG}$ | $\overline{HS3}$ | $\overline{HS2}$ | $\overline{HST}$ | $\overline{HS0}$ | $\overline{DST}$ | $\overline{DS0}$ | DIGITAL INPUT |
| 3F7H/ 377H | W | - | - | - | - | - | - | - | - | RESERVED |

## CONFIGURATION

The configuration of the FDC37C661 within the user system is selected through software selectable configuration registers. The different configurations of the FDC37C662 can only be selected through jumper options.

### FDC37C661 CONFIGURATION REGISTERS

The configuration registers are used to select programmable options of the FDC. After power up, the FDC is in the default mode. The default modes are identified in the Configuration Mode Register Description. To program the configuration registers, the following sequence must be followed:

1. Enter Configuration Mode.
2. Configure FDC Registers.
3. Exit configuration Mode.

#### Enter Configuration Mode

To enter the configuration mode, two writes in succession to port 3F0H with 55H data are required. If a write to another address or port occurs between these two writes, the chip does not enter the configuration mode. It is strongly recommended that interrupts be disabled for the duration of these two writes.

#### Configure FDC37C661

The FDC37C661 contains five configuration registers, CR0-CR4. These registers are accessed by first writing the number (0-4) of the desired register to port 3F0H and then writing or reading the configuration register through port 3F1H.

#### Exit Configuration Mode

The configuration mode is exited by writing an AAH to port 3F0H.

#### Programming Example

The following is an example of a configuration program in Intel 8086 assembly language. For this example, the FDC37C661 is being reset to the default condition after power up.

```
;------------------------------.
; ENTER CONFIGURATION MODE     |
;------------------------------'
MOV   DX,3F0H
MOV   AX,055H
CLI                ; disable interrupts
OUT   DX,AL
OUT   DX,AL
STI                ; enable interrupts
;------------------------------.
; CONFIGURE REGISTERS CR0-CR3  |
;------------------------------'
MOV   DX,3F0H
MOV   AL,00H
OUT   DX,AL ; Point to CR0
MOV   DX,3F1H
MOV   AL,3FH
OUT   DX,AL ; Update CR0
;
MOV   DX,3F0H      ;
MOV   AL,01H
OUT   DX,AL ; Point to CR1
MOV   DX,3F1H
MOV   AL,9FH
OUT   DX,AL ; Update CR1
;
MOV   DX,3F0H      ;
MOV   AL,02H
OUT   DX,AL ; Point to CR2
MOV   DX,3F1H
MOV   AL,0DCH
OUT   DX,AL ; Update CR2
;
MOV   DX,3F0H      ;
MOV   AL,03H
OUT   DX,AL ; Point to CR3
MOV   DX,3F1H
MOV   AL,78H
OUT   DX,AL ; Update CR3
;
;------------------------------.
; EXIT CONFIGURATION MODE      |
;------------------------------'
MOV   DX,3F0H
MOV   AX,0AAH
OUT   DX,AL
```

**FDC37C661 Configuration Register Description**

The configuration registers consist of six registers, the Configuration Select Register and Configuration Registers 0-4. The configuration select register is written to by writing to port 3F0H. The Configuration Registers 0-4 are accessed by reading or writing to port 3F1H.

**Configuration Select Register (CSR)**

This register can only be accessed when the FDC is in the Configuration Mode. This register, located at port 3F0H, must initialized upon entering the Configuraiton Mode before the configuration registers (CR0-CR4) can be accessed and is used to select which of the Configuration Registers are to be accessed at port 3F1H.

**Configuration Registers 0-4**

These registers are set to their default values at power up and are not affected by RESET. They are accessed at port 3F1H. CR0 is used to set the options for the oscillator, Baud Rate Generator and the FDC and IDE blocks. CR1 is used for allowing reading of the configuration registers and selecting options on the serial ports, IRQ signal and the parallel port. CR2 is used to set the options for the primary and secondary serial ports. CR3 is used to define the mode of operation, PS/2, PC/AT or Model 30. It also controls the SC/DRV2 pin and the DATA RATE 0 and 1 outputs. CR4 is used to set the test modes of the chip.

**CR0**

This register can only be accessed when the FDC is in the Configuration Mode and after the CSR has been initialized to 00H. The default value of this register after power up is 3FH.

**Table 34 - CR0**

| BIT NO. | BIT NAME | DESCRIPTION |
|---|---|---|
| 0 | IDE ENABLE | A high level on this bit, enables the IDE (Default). A low level on this bit disables the IDE. |
| 1 | IDE AT/XT | A high level on this bit sets the IDE to AT type (Default). A low level on this bit sets the IDE to XT type. |
| 2 | RESR | (This bit is Reserved - defaults to 1.) |
| 3 | FDC POWER | A high level on this bit, supplies power to the FDC (Default). A low level on this bit puts the FDC in low power mode. |
| 4 | FDC ENABLE | A high level on this bit, enables the FDC (Default). A low level on this bit disables the FDC. |
| 5,6 | OSC | 6 5<br>0 0 Osc ON, BR Generator (BRG) Clock Enabled.<br>0 1 Osc is On, BRG Clock is ON when PWRGD is active. When PWRGD is inactive, Osc is off and BRG Clock is Disabled (Default).<br>1 0 (same as 0 1 case)<br>1 1 Osc OFF, BR Generator Clock Disabled |
| 7 | VALID | A high level on this software controlled bit indicates that a valid configuration cycle has occurred. The control software must take care to set this bit at the appropriate times. Set to zero after power up. |

**CR1**

This register can only be accessed when the FDC is in the Configuration Mode and after the CSR has been initialized to 01H. The default value of this register after power up is 9FH.

**Table 35 - CR1**

| BIT NO. | BIT NAME | DESCRIPTION |
|---|---|---|
| 0,1 | Parallel Port Address | These bits are used to select the Parallel Port Address.<br>1 0 Parallel Port Address<br>0 0 Disabled<br>0 1 3BCH<br>1 0 378H<br>1 1 278H (Default) |
| 2 | Parallel Port Power | A high level on this bit, supplies power to the Parallel Port (Default). A low level on this bit puts the Parallel Port in low power mode. |
| 3 | Parallel Port Mode | Parallel Port Mode. A high level on this bit, sets the Parallel Port for Printer Mode (Default). A low level on this bit sets the Parallel Port for EXTENDED PARALLEL PORT MODE (Bi-directional). |
| 4 | IRQ Polarity | A high level on this bit, programs IRQ for active high, inactive low (Default). A low level on this bit programs IRQ for active low, inactive hi-Z. |
| 5,6 | COM3,4 | Select the COM3 and COM4 address.<br>6 5 COM3 COM4<br>0 0 338H 238H (Default)<br>0 1 3E8H 2E8H<br>1 0 2E8H 2E0H<br>1 1 220H 228H |
| 7 | Enable CRx | A high level on this bit, enables the reading of CR0-CR3 (Default). A low level on this bit disables the reading of CR0-CR3. |

**CR2**

This register can only be accessed when the FDC is in the Configuration Mode and after the CSR has been initialized to 02H. The default value of this register after power up is DCH.

**Table 36 - CR2**

| BIT NO. | BIT NAME | DESCRIPTION |
|---|---|---|
| 0,1 | UART 1 Address Select | These bits select the Primary Serial Port Address.<br>1 0 COM Port ADDRESS<br>0 0 COM1 3F8H (Default)<br>0 1 COM2 2F8H<br>1 0 COM3 (Refer to CR1, bits 5,6)<br>1 1 COM4 (Refer to CR1, bits 5,6) |
| 2 | UART 1 Enable | A high level on this bit, enables the Primary Serial Port (Default). A low level on this bit disables the Primary Serial Port. |
| 3 | UART 1 Power down | A high level on this bit, allows normal operation of the Primary Serial Port (Default). A low level on this bit places the Primary Serial Port into Power Down Mode. |
| 4,5 | UART 2 Address Select | These bits select the Secondary Serial Port Address.<br>5 4 COM Port ADDRESS<br>0 0 COM1 3F8H<br>0 1 COM2 2F8H (Default)<br>1 0 COM3 (Refer to CR1, bits 5,6)<br>1 1 COM4 (Refer to CR1, bits 5,6) |
| 6 | UART 2 Enable | A high level on this bit enables the Secondary Serial Port (Default). A low level on this bit disables the Secondary Serial Port. |
| 7 | UART 2 Power down | A high level on this bit, allows normal operation of the Secondary Serial Port (Default). A low level on this bit places the Secondary Serial Port into Power Down Mode. |

**CR3**

This register can only be accessed when the FDC is in the Configuration Mode and after the CSR has been initialized to 03H. The default value after power up is 78H.

**Table 37 - CR3**

| BIT NO. | BIT NAME | DESCRIPTION |
|---|---|---|
| 0 | Reserved | Reserved - read as a zero. |
| 1 | Reserved | Reserved - read as a zero. |
| 2 | Reserved | 0 = Normal; 1 = Enhanced Floppy Mode |
| 3 | Drive Opt 0 | These two bits control the DRATE0 and DRATE1 outputs. The mapping from the DRATE SEL bit of the DSR, DIR AND CCR to the DRATE outputs is shown in table 38 below. |
| 4 | Drive Opt 1 | |
| 5 | MFM | IDENT is used in conjunction with MFM to define the interface mode of operation. |
| 6 | IDENT | **IDENT** / **MFM** / **MODE**: 1 / 1 / AT Mode (Default); 1 / 0 / Illegal; 0 / 1 / PS/2; 0 / 0 / Model 30 |
| 7 | SC/DRV2 EN | When set to a logic "0" the Serial Clock/DRV2 pin is in the DRV2 input mode (default). When set to a logic "1", this pin is the Serial Clock output. |

Table 38 - Drive Option 1 and 2

| DATA RATE KB/sec | REGISTER SETTINGS | | CONFIG. REGISTER | | OUTPUTS PINS | |
|---|---|---|---|---|---|---|
| | DRATE SEL 1 | DRATE SEL 0 | DRIVE OPT 0 | DRIVE OPT 1 | DRATE1 | DRATE0 |
| 1000 | 1 | 1 | 0 | 0 | 1 | 1 |
| 500 | 0 | 0 | 0 | 0 | 0 | 0 |
| 300 | 0 | 1 | 0 | 0 | 0 | 1 |
| 250 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1000 | 1 | 1 | 1 | 0 | 1 | 1 |
| 500 | 0 | 0 | 1 | 0 | 1 | 0 |
| 300 | 0 | 1 | 1 | 0 | 0 | 1 |
| 250 | 1 | 0 | 1 | 0 | 0 | 0 |
| X | X | X | 0 | 1 | TBD | TBD |
| X | X | X | 1 | 1 | INPUT | INPUT |

**NOTE:** In the 662 mode, the defaults for DRIVE OPT 0 and DRIVE OPT 1 are 0, 0 and cannot be changed.

CR4

This register can only be accessed when the FDC isin the Configuration Mode and after the CSR has been initialized to 04H. The default value of this register after power up is 00H.

Table 39 - CR4

| BIT NO. | BIT NAME | DESCRIPTION |
|---|---|---|
| 0 | Test 0 | Reserved - Set to zero. |
| 1 | Test 1 | Reserved - Set to zero. |
| 2 | Test 2 | Reserved - Set to zero. |
| 3 | Test 3 | Reserved - Set to zero. |
| 4,5 | Test 4<br>Test 5 | Reserved - Set to zero. |
| 6 | Test 6 | Reserved - Set to zero. |
| 7 | Test 7 | Reserved - Set to zero. |

**FDC37C662 Hardware Configuration**

The FDC37C662 hardware configuration can select or deselect the parallel, serial, FDC and IDE circuits and set the parallel port and serial port addresses.

| PCF1 | PCF0 | PARALLEL PORT ADDRESS |
|---|---|---|
| 0 | 0 | Disabled |
| 0 | 1 | 3BCH |
| 1 | 0 | 378H |
| 1 | 1 | 278H |

The COM3 and COM4 serial port addresses have been changed for Revision C only of the FDC37C662 as shown in the two tables below. COM3 and COM4 for Revisions A and B retain their original addresses.

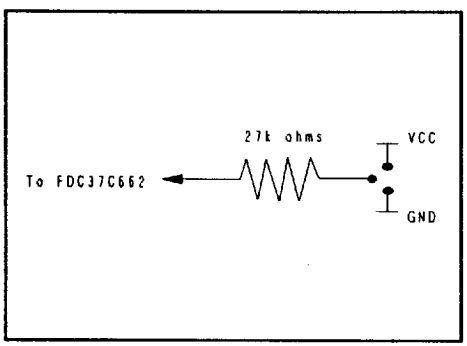
| S1CF1 | S1CF0 | PRIMARY SERIAL PORT ADDRESS | |
|---|---|---|---|
| | | REVISIONS A & B | REVISION C |
| 0 | 0 | Disabled | Disabled |
| 0 | 1 | COM3 338H | COM3 3E8H |
| 1 | 0 | COM2 2F8H | COM2 2F8H |
| 1 | 1 | COM1 3F8H | COM1 3F8H |

| S2CF1 | S2CF0 | SECONDARY SERIAL PORT ADDRESS | |
|---|---|---|---|
| | | REVISIONS A & B | REVISION C |
| 0 | 0 | Disabled | Disabled |
| 0 | 1 | COM4 238H | COM4 2E8H |
| 1 | 0 | COM1 3F8H | COM1 3F8H |
| 1 | 1 | COM2 2F8H | COM2 2F8H |

| IDECF | IDE CONTROL |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

| FDCCF | FDC CONTROL |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

In the FDC37C662, the pins used to configure the part should be connected as per the diagram below. This shows how a jumper can be used to set a high (VCC) or a low (GND) into the port for configuration at the end of the reset pulse.



## OPERATIONAL DESCRIPTION

### MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -55° to +150°C
Lead Temperature Range (soldering, 10 seconds) . . . . . +325°C
Positive Voltage on any pin, with respect to Ground . . . . . $V_{cc}$ +0.3V
Negative Voltage on any pin, with respect to Ground . . . . . -0.3V
Maximum $V_{cc}$ . . . . . +7V

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

**DC ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C - 70°C, $V_{cc}$ = +5.0 V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| **I Type Input Buffer** | | | | | | |
| Low Input Level | $V_{ILI}$ | | | 0.8 | V | TTL Levels |
| High Input Level | $V_{IHI}$ | 2.0 | | | V | |
| **IS Type Input Buffer** | | | | | | |
| Low Input Level | $V_{ILIS}$ | | | 0.8 | V | Schmitt Trigger |
| High Input Level | $V_{IHIS}$ | 2.2 | | | V | Schmitt Trigger |
| Schmitt Trigger Hysteresis | $V_{HYS}$ | | 250 | | mV | |
| **$I_{CLK}$ Input Buffer** | | | | | | |
| Low Input Level | $V_{ILCK}$ | | | 0.4 | V | |
| High Input Level | $V_{IHCK}$ | 3.0 | | | V | |

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| **Input Leakage** (All I and IS buffers except PWRGD) | | | | | | |
| Low Input Leakage | $I_{IL}$ | -10 | | +10 | μA | $V_{IN}$ = 0 |
| High Input Leakage | $I_{IH}$ | -10 | | +10 | μA | $V_{IN}$ = $V_{CC}$ |
| **Input Current** PWRGD | $I_{IL}$ | | -75 | -150 | μA | $V_{IN}$ = 0 |
| **I/O24 Type Buffer** | | | | | | |
| Low Output Level | $V_{OL}$ | | | 0.5 | V | $I_{OL}$ = 24 mA |
| High Output Level | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -12 mA |
| Output Leakage | $I_{OL}$ | -10 | | +10 | μA | $V_{IN}$ = 0 to $V_{CC}$ (Note 1) |
| **O24 Type Buffer** | | | | | | |
| Low Output Level | $V_{OL}$ | | | 0.5 | V | $I_{OL}$ = 24 mA |
| High Output Level | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -12 mA |
| Output Leakage | $I_{OL}$ | -10 | | +10 | μA | $V_{IN}$ = 0 to $V_{CC}$ (Note 1) |
| **OD48 Type Buffer** | | | | | | |
| Low Output Level | $V_{OL}$ | | | 0.5 | V | $V_{OL}$ = 48 mA |
| Output Leakage | $I_{OH}$ | -10 | | +10 | μA | $I_{OH}$ = 0 to $V_{CC}$ (Note 2) |
| **O4 Type Buffer** | | | | | | |
| Low Output Level | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 4 mA |
| High Output Level | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -1 mA |
| Output Leakage | $I_{OL}$ | -10 | | +10 | μA | $V_{IN}$ = 0 to $V_{CC}$ (Note 1) |

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| **O8 Type Buffer** | | | | | | |
| Low Output Level | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8 mA |
| High Output Level | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -4 mA |
| Output Leakage | $I_{OL}$ | -10 | | +10 | $\mu$A | $V_{IN}$ = 0 to $V_{CC}$ (Note 1) |
| **OD24 Type Buffer** | | | | | | |
| Low Output Level | $V_{OL}$ | | | 0.5 | V | $I_{OL}$ = 24 mA |
| High Output Level | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -50 $\mu$A |
| Output Leakage | $I_{OL}$ | -10 | | +10 | $\mu$A | $V_{IN}$ = 0 to $V_{CC}$ (Note 1) |
| Supply Current Active | $I_{CC}$ | | 32 | 40 | mA | All outputs open. |
| Supply Current Standby | $I_{CSBY}$ | | 300 | 500 | $\mu$A | Note 3 |
| ChiProtect (SLCT, PE, BUSY, $\overline{ACK}$, $\overline{ERROR}$) | $I_{IL}$ | | | ±10 | $\mu$A | Chip in circuit: $V_{CC}$ = 0V $V_{IN}$ = 6V Max. |

Note 1: All output leakages are measured with the current pins in high impedance as defined by the PWRGD pin (FDC37C661 only).

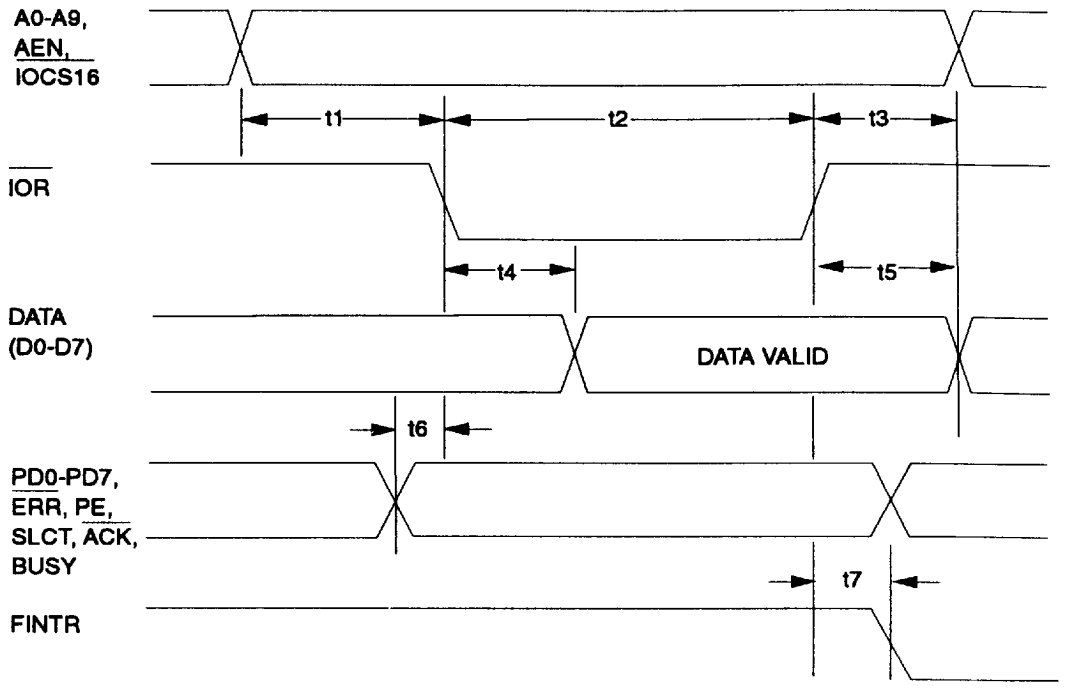
Note 2: Output leakage is measured with the low driving output off, either for a high level output or a high impedance state defined by PWRGD (FDC37C661 only).

Note 3: Defined by the device configuration with the PWRGD input low.

CAPACITANCE $T_A$ = 25°C; fc = 1MHz; $V_{CC}$ = 5V

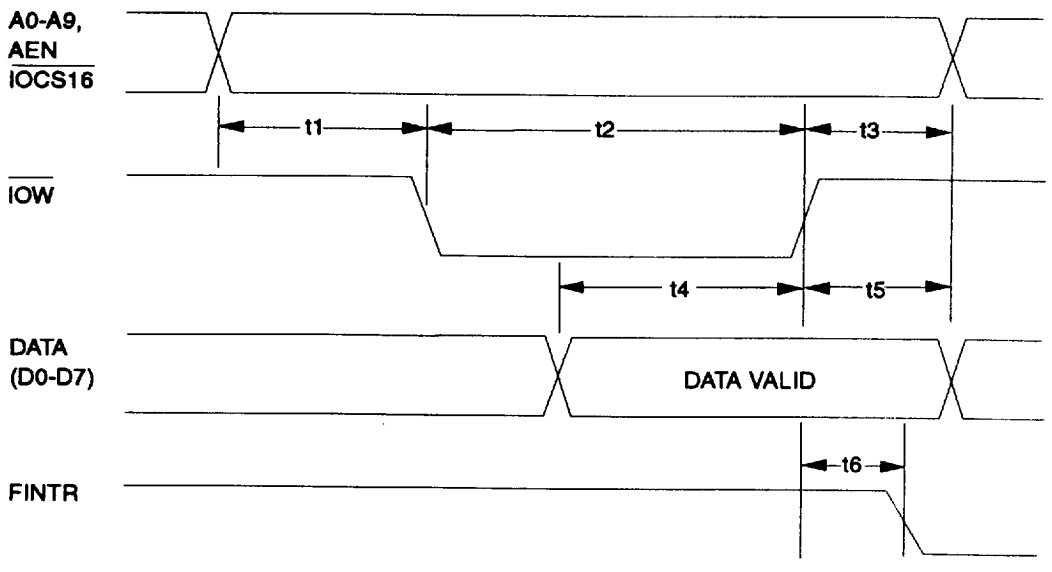
| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Clock Input Capacitance | $C_{IN}$ | | | 20 | pF | All pins except pin under test tied to AC ground |
| Input Capacitance | $C_{IN}$ | | | 10 | pF | |
| Output Capacitance | $C_{OUT}$ | | | 20 | pF | |

## TIMING DIAGRAMS



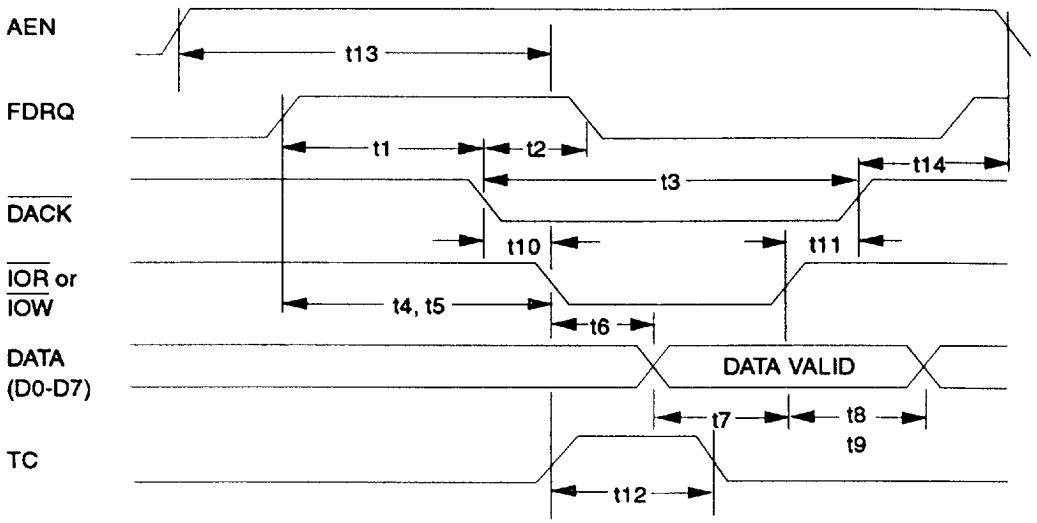

| | Parameter | min | typ | max | units |
|---|---|---|---|---|---|
| t1 | A0-A9, AEN, IOCS16 Set Up to IOR Low | 10 | | | ns |
| t2 | IOR Width | 40 | | | ns |
| t3 | A0-A9, AEN, IOCS16 Hold from IOR High | 10 | | | ns |
| t4 | Data Access Time from IOR Low | | | 25 | ns |
| t5 | Data to Float Delay from IOR High | 10 | | 60 | ns |
| t6 | Port Setup | | 20 | | ns |
| t7 | Read Strobe to Clear FINTR | | 40 | 55 | ns |

**FIGURE 4 - MICROPROCESSOR READ TIMING**



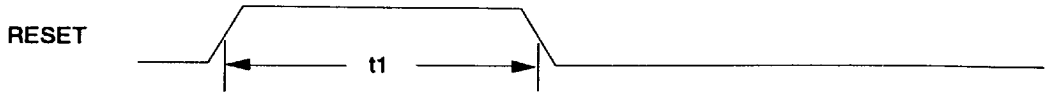

| | Parameter | min | typ | max | units |
|---|---|---|---|---|---|
| t1 | A0-A9, AEN, IOCS16 Set Up to IOW Low | 10 | | | ns |
| t2 | IOW Width | 40 | | | ns |
| t3 | A0-A9, AEN, IOCS16 Hold from IOW High | 10 | | | ns |
| t4 | Data Set Up Time to IOW High | 25 | | | ns |
| t5 | Data Hold Time from IOW High | 0 | | | ns |
| t6 | Write Strobe to Clear FINTR | | 40 | 55 | ns |

**FIGURE 5 - MICROPROCESSOR WRITE TIMING**



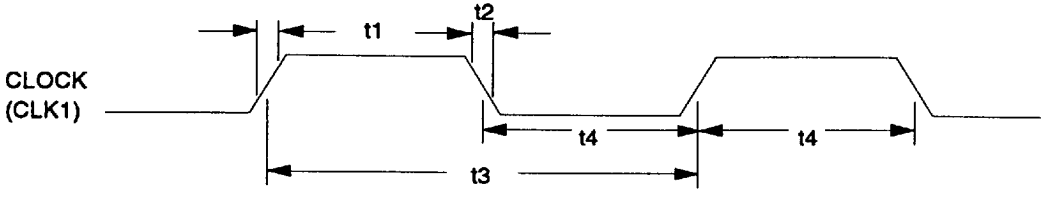

| | Parameter | min | typ | max | units |
|---|---|---|---|---|---|
| t1 | DACK Delay Time from FDRQ High | 0 | | | ns |
| t2 | FDRQ Reset Delay from DACK Low | | | 140 | ns |
| t3 | DACK Width | 150 | | | ns |
| t4 | IOR Delay from FDRQ High | 0 | | | ns |
| t5 | IOW Delay from FDRQ High | 0 | | | ns |
| t6 | Data Access Time from IOR Low | | | 100 | ns |
| t7 | Data Set Up Time to IOW High | 40 | | | ns |
| t8 | Data to Float Delay from IOR High | 10 | | 60 | ns |
| t9 | Data Hold Time from IOW High | 10 | | | ns |
| t10 | DACK Set Up to IOW/IOR Low | 5 | | | ns |
| t11 | DACK Hold After IOW/IOR High | 10 | | | ns |
| t12 | TC Pulse Width | 60 | | | ns |
| t13 | AEN Set Up to IOR/IOW | 40 | | | ns |
| t14 | AEN Hold from DACK | 10 | | | ns |

**FIGURE 6 - DMA TIMING**



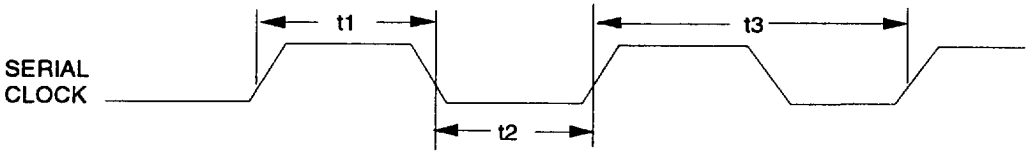

| | Parameter | min | typ | max | units |
|---|---|---|---|---|---|
| t1 | RESET Width | 500 | | | ns |

**FIGURE 7 - RESET TIMING**




| | Parameter | min | typ | max | units |
|---|---|---|---|---|---|
| t1 | Clock Rise Time (VIN = 0.4 to 3.0) | | | 5 | ns |
| t2 | Clock Fall Time (VIN = 3.0 to 0.4) | | | 5 | ns |
| t3 | Clock Period | 40 | 41.67 | | ns |
| t4 | Clock Active (High or Low) | 14 | | | ns |

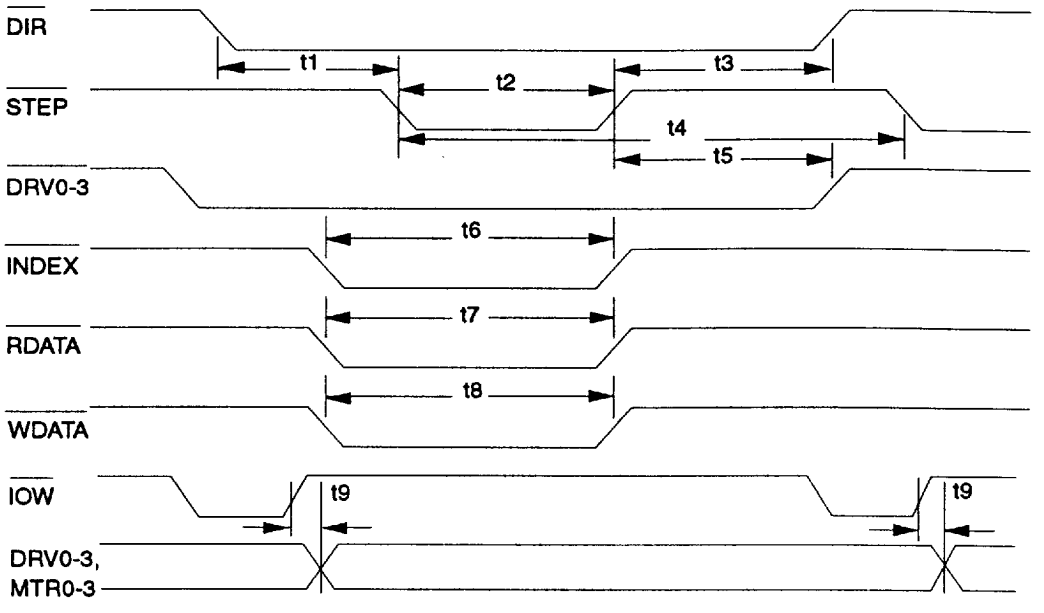
**FIGURE 8 - CLOCK TIMING**




| | Parameter | min | typ | max | units |
|---|---|---|---|---|---|
| t1 | Serial Clock High Pulse Width | 250 | | | ns |
| t2 | Serial Clock Low Pulse Width | 250 | | | ns |
| t3 | Serial Clock Period | | 541.67 | | ns |

Note: t3 = 13 x period CLK1 (t3 Figure 9).

**FIGURE 9 - SERIAL CLOCK TIMING**

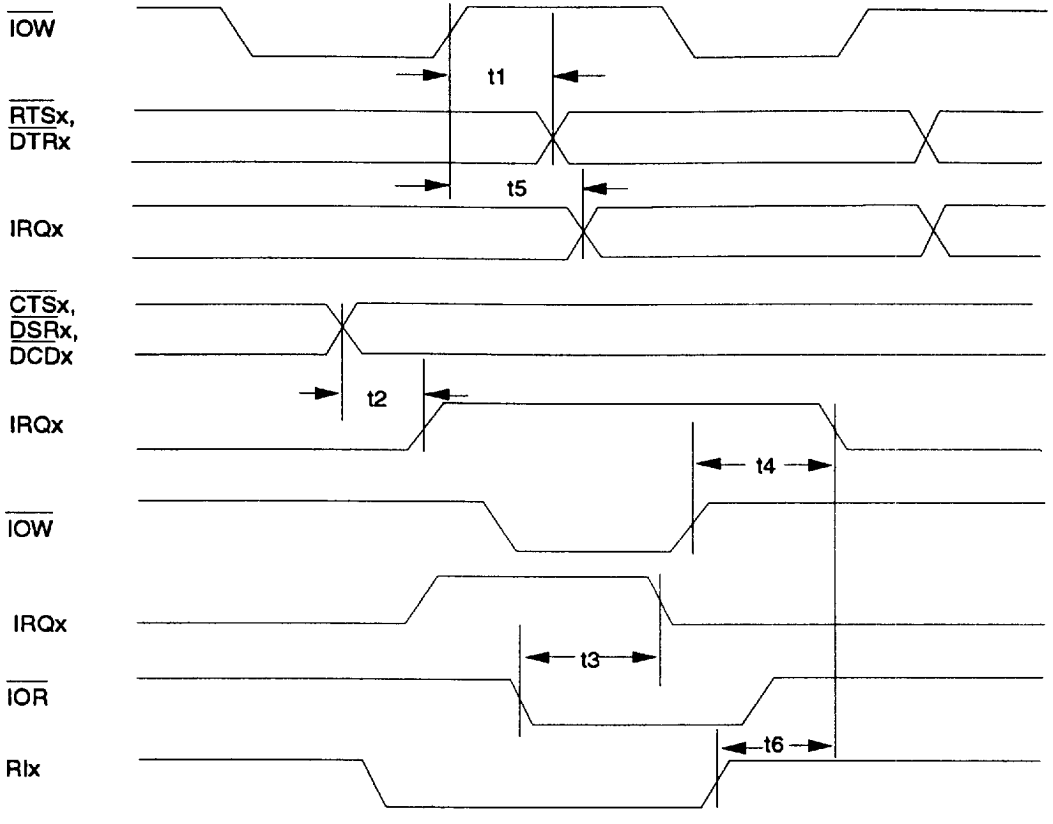



(AT Mode timing only)

| | Parameter | min | typ | max | units |
|---|---|---|---|---|---|
| t1 | DIR Set Up to STEP Low | | 4 | | X* |
| t2 | STEP Active Time Low | | 24 | | X* |
| t3 | DIR Hold Time After STEP | | 96 | | X* |
| t4 | STEP Cycle Time | | 132 | | X* |
| t5 | DRV0-3 Hold Time from STEP Low | | 20 | | X* |
| t6 | INDEX Pulse Width | | 2 | | X* |
| t7 | RDATA Active Time Low | | 40 | | ns |
| t8 | WDATA Write Data Width Low | | .5 | | Y* |
| t9 | DRV0-3, MTR0-3 from End of IOW | | 25 | | ns |

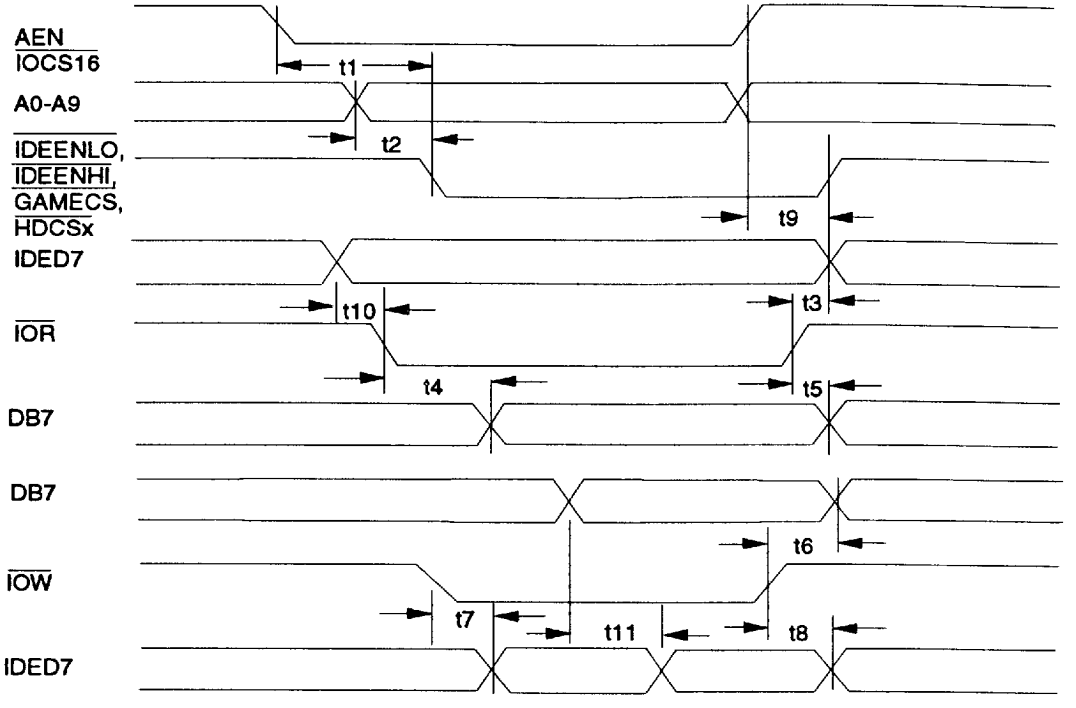
*X specifies one MCLK period and Y specifies one WCLK period.
MCLK = Controller Clock to FDC (See Table 6).
WCLK = 2 x Data Rate (See Table 6).

**FIGURE 10 - DISK DRIVE TIMING**



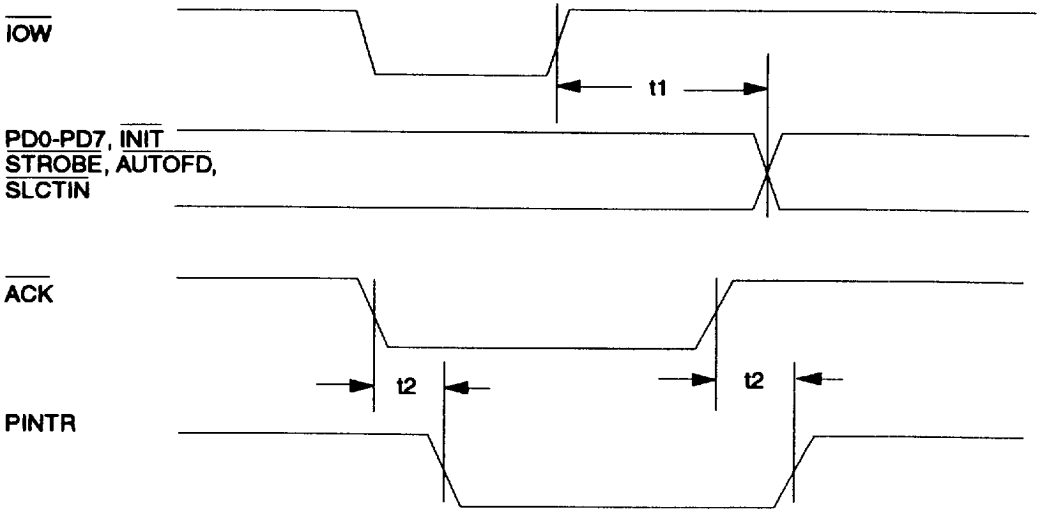

| | Parameter | min | typ | max | units |
|---|---|---|---|---|---|
| t1 | RTSx, DTRx Delay from IOW | | | 200 | ns |
| t2 | IRQx Active Delay from CTSx, DSRx, DCDx | | | 100 | ns |
| t3 | IRQx Inactive Delay from IOR (Leading Edge) | | | 120 | ns |
| t4 | IRQx Inactive Delay from IOW (Trailing Edge) | | | 125 | ns |
| t5 | IRQx Inactive Delay from IOW | 10 | | 100 | ns |
| t6 | IRQx Active Delay from RIx | | | 100 | ns |

**FIGURE 11 - SERIAL PORT TIMING**



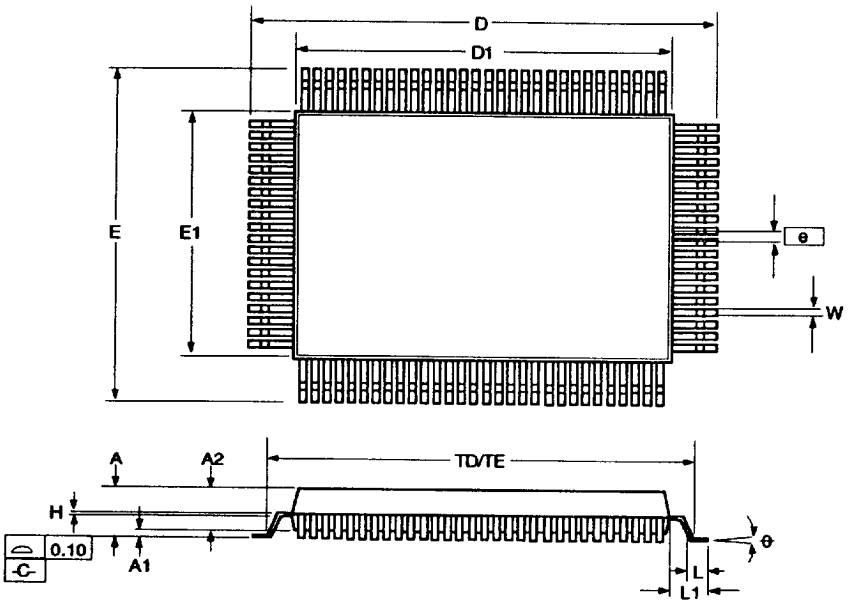

| | Parameter | min | typ | max | units |
|---|---|---|---|---|---|
| t1 | IDEENLO, IDEENHI, GAMECS, HDCSx Delay from AEN, IOCS16 | | | 40 | ns |
| t2 | IDEENLO, IDEENHI, GAMECS, HDCSx Delay from A0-A9 | | | 40 | ns |
| t3 | IDED7 Hold Time after IOR | 10 | | | ns |
| t4 | DB7 Delay from IOR | | | 60 | ns |
| t5 | DB7 Hold Time from IOR | 10 | | 60 | ns |
| t6 | DB7 Hold Time from IOW | 10 | | | ns |
| t7 | IDED7 Delay from Data Bus IOW Active | | | 50 | ns |
| t8 | IDED7 Inactive Delay from IOW | 10 | | 50 | ns |
| t9 | IDEENLO Delay from IDEENHI, IOCS16, AEN | | | 40 | ns |
| t10 | IDED7 Set Up Time before IOR | 40 | | | ns |
| t11 | IDED7 Delay from DB7, IDED7 in Output Mode | | | 25 | |

**FIGURE 12 - IDE INTERFACE TIMING**




| | Parameter | min | typ | max | units |
|---|---|---|---|---|---|
| t1 | PD0-7, INIT, STROBE, AUTOFD Delay from IOW | | | 100 | ns |
| t2 | PINTR Delay from ACK | | | 60 | ns |

**FIGURE 13 - PARALLEL PORT TIMING**




| | Millimeters | | Inches | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.80 | 3.15 | .110 | .124 |
| A1 | 0.1 | 0.45 | .004 | .018 |
| A2 | 2.57 | 2.87 | .101 | .113 |
| D | 23.4 | 24.15 | .921 | .951 |
| D1 | 19.9 | 20.1 | .783 | .791 |
| E | 17.4 | 18.15 | .685 | .715 |
| E1 | 13.9 | 14.1 | .547 | .555 |
| H | 0.1 | 0.2 | .004 | .008 |
| L | 0.65 | 0.95 | .026 | .037 |
| L1 | 1.8 | 2.6 | .071 | .102 |
| e | 0.65 BSC | | .0256 BSC | |
| θ | 0° | 12° | 0° | 12° |
| W | .2 | .4 | .008 | .016 |
| TD(1) | 21.8 | 22.2 | .858 | .874 |
| TE(1) | 15.8 | 16.2 | .622 | .638 |
| TD(2) | 22.21 | 22.76 | .874 | .896 |
| TE(2) | 16.27 | 16.82 | .641 | .662 |

Notes:

1) Coplanarity is 0.100mm (.004") maximum.
2) Tolerance on the position of the leads is 0.200mm (.008") maximum.
3) Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25mm (.010").
4) Dimensions TD and TE are important for testing by robotic handler. Only above combinations of (1) or (2) are acceptable.
5) Controlling dimension: millimeter. Dimensions in inches for reference only and not necessarily accurate.

**FIGURE 14 - 100 PIN QFP**