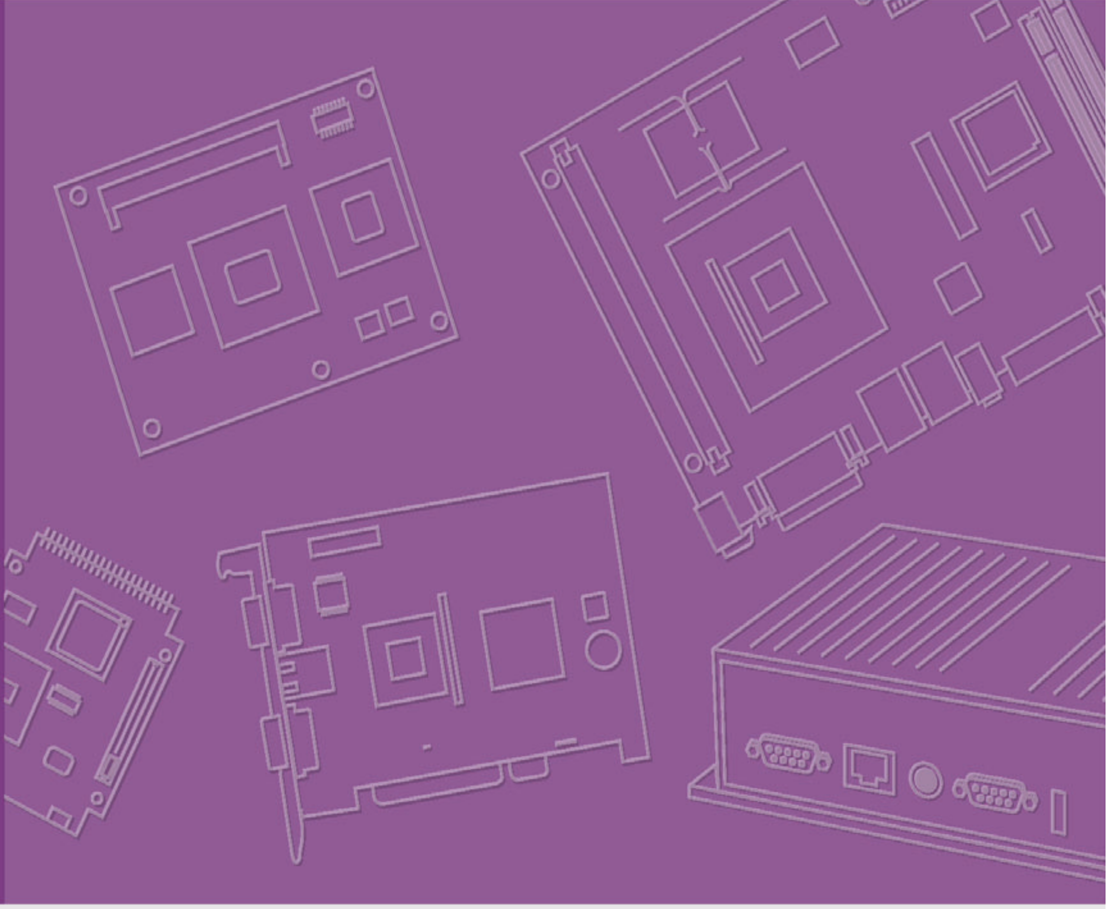
User Manual



EVA-X4300

Product Brief

Trusted ePlatform Services

ADVANTECH

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Part No. 2006X43010 Edition 1
Printed in Taiwan August 2008

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Chapter 1

Overview

1.1 Overview

The EVA-X4300 is a fully static 32-bit x86-based processor that is compatible with a wide-range of PC peripherals, applications and operating systems, such as DOS, WinCE, Linux, and most popular 32-bit RTOSs (Real Time OS). It enables maximum software re-use based on its feature of legacy compatibility. The EVA-X4300 integrates 32 KB write-through direct map L1 cache, a PCI bus interface at 33 MHz, an 8/16-bit ISA bus interface, SDR SDRAM, DDR2 SDRAM, a ROM controller, IPC (Internal Peripheral Controller) with DMA and interrupt timer/counter included, FIFO UART, SPI (Serial Peripheral Interface), LPC (low pin count), a USB 1.1/2.0 host controller, LoC (LAN on Chip), an IDE controller, and 256 KB flash within a single 581-pin BGA package to form a an SoC (System-on-Chip) processor. The EVA-X4300 integrates comprehensive features and rich I/O flexibility within a single System-on-Chip, to reduce board design complexity and shorten product development schedules. Taking advantage of ultra low power consumption, the EVA-X4300 is able to operate in a wide range of temperatures without additional thermal design. With the commitment of long term supply guaranteed for the EVA-X4300, customers can extend product life cycle and receive a maximum return on investment.

The EVA-X4300 provides an ideal solution for embedded systems and communication products (such as the thin client, NAT router, home gateway, access point and tablet PC) producing optimal performance.

Chapter 2

Features

2.1 Features

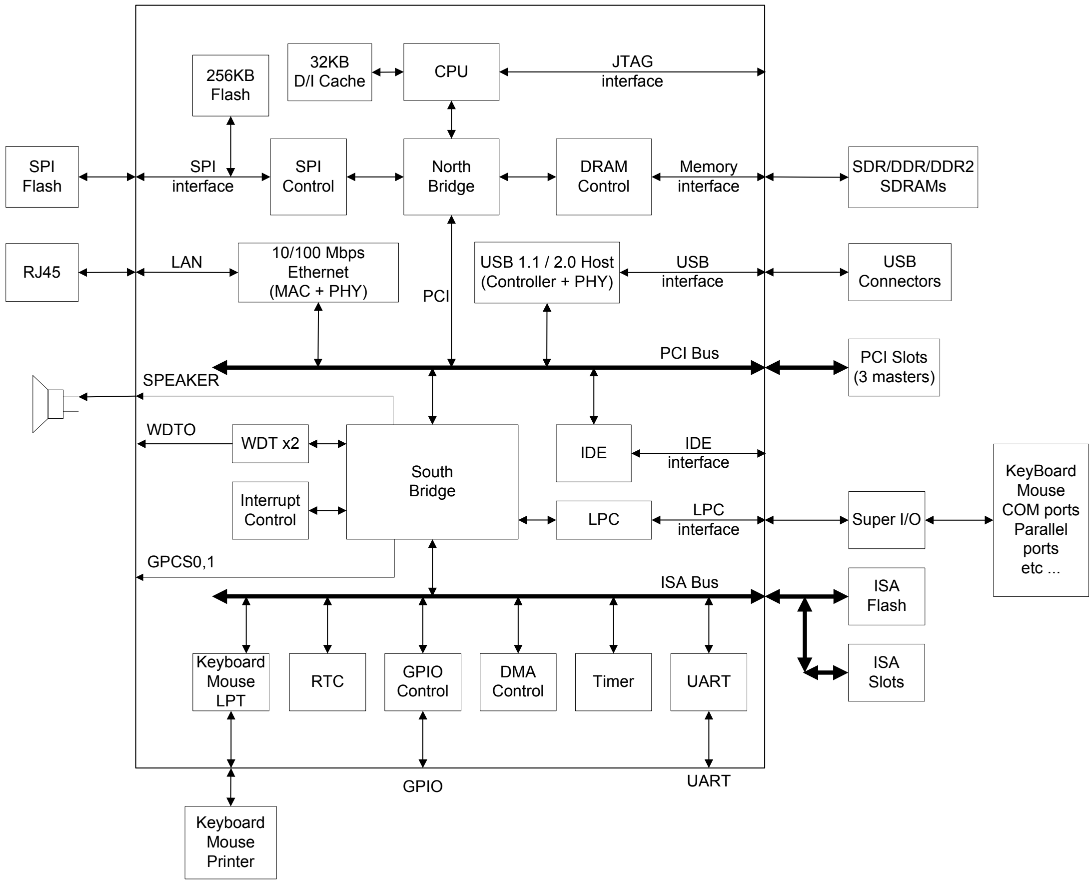
- **RISC Processor Core**
  - 6 stage pipe-line, 300 MHz
- **Embedded L1 Cache**
  - 16 KB I-Cache, 16 KB D-Cache
- **SDR / DDRII SDRAM Control Interface**
  - 16 bits data bus
  - Support DLL for clock phase auto-adjustment
  - SDR support up to 133 MHz, 128 MByte
  - DDRII support up to 166 MHz, 256 MByte
- **DMA Controller**
  - Provide two 82C37 compatible DMA controllers
  - 4-channel 8-bit DMA transfer and 3-channel 16-bit DMA transfer
- **Interrupt Controller**
  - Provide two 8259 compatible interrupt controllers
  - Independent programmable level/edge-trigger interrupt channels
  - Serial IRQ supported
- **Counter / Timer**
  - 2 set of 8254 timer controller
  - Support 2 sets Watch Dog Timer (WDT)
- **General Chip Selector**
  - 2 sets extended Chip Selector
  - Configurable I/O-map or Memory-map
  - I/O Addressing: From 2 byte to 64 Kbyte
  - Memory Address: From 512 byte to 4 Gbyte
- **PCI Control Interface**
  - 32 bit, 33 MHz, compliant with PCI spec. Rev. 2.1
  - Up to 3 individual PCI master devices
  - 3.3 V I/O with 5 V tolerance
- **ISA Bus Interface**
  - AT clock programmable
  - 8/16 bit ISA device with Zero-Wait-State
  - Generate refresh signals to ISA interface during DRAM refresh cycle
  - Complete IRQ set
- **Ethernet Controller**
  - Integrated 1 set of 10/100 Mbps Ethernet (MAC + PHY)
- **IDE Controller**
  - Support 2 channels Ultra-DMA 100 (PATA x 4)
- **Universal Serial Bus**
  - USB 2.0 Host controller, support 4 USB ports
  - Support HS, FS and LS mode
- **LPC (Low Pin Count) Bus Interface**
  - Support 2 programmable registers to decode LPC address

- **FIFO UART Port**
  - Support up to 5 COM ports
  - Compatible with 16C550/16C552
  - Default internal pull-up
  - Support TXD_En signal on COM1 and COM2
  - Support the programmable baud rate generator with the data rate from 50 to 460.8 Kbps
  - The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
  - Port 80h output data could be redirected to COM1
- **General Purpose I/O**
  - Up to 40 GPIO, 8 dedicated and 32 multi-functional programmable I/O pins
  - GPIO pins can be individually configured as inputs, outputs, or as interrupt trigger sources
  - Open-drain with pull-high 75 KΩ
- **SPI Interface**
  - Support SPI flash boot
- **Real Time Clock**
  - Internal RTC or External RTC
  - Under 2 uA power consumption on Internal Mode
- **Parallel Port**
  - Support SPP / EPP / ECP mode
- **PS/2 Keyboard and Mouse Interface**
  - Compatible with 8042 controller
- **MTBF Flag Counter**
- **Stacked 256 KB Flash**
  - SPI interface, for BIOS storage
  - Could be disabled and use external Flash
- **JTAG Interface**
- **Speaker Out**
- **Input Clock**
  - 14.318 MHz, 32.768 KHz
- **Output Clock**
  - 24 MHz, 25 MHz, 14.318 MHz
  - PCI clock
  - ISA clock
  - SDRAM clock
- **Operating Voltage Range**
  - Core Voltage: 1.3 V ~ 1.4 V
  - I/O Voltage: 1.8 V ± 5 %, 3.3 V ± 10 %
- **Operating temperature**
  - -20°C ~ 85°C
- **Power Consumption**
  - Under 1 Watt (est.)
- **Package Type**
  - PBGA, 581 balls
  - Dimension: 27 mm x 27 mm x 2.23mm
  - Lead-free, RoHS compliant

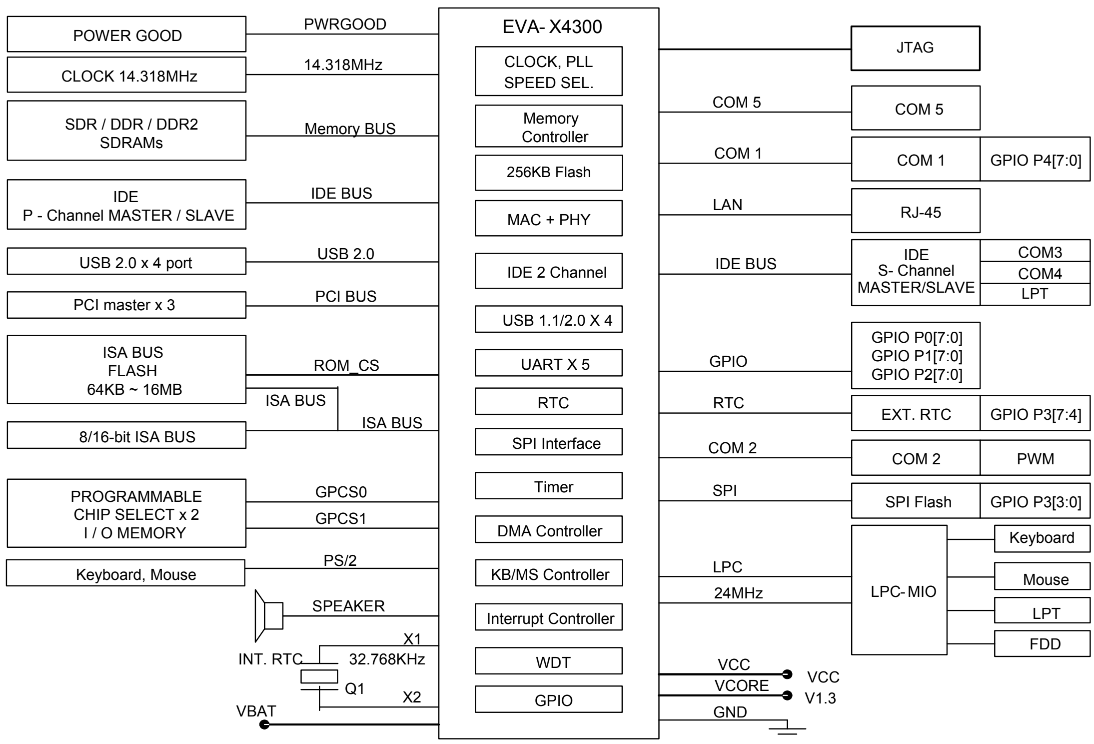
Chapter 3

Block Diagram

3.1 System Block Diagram



3.2 Functions Block Diagram



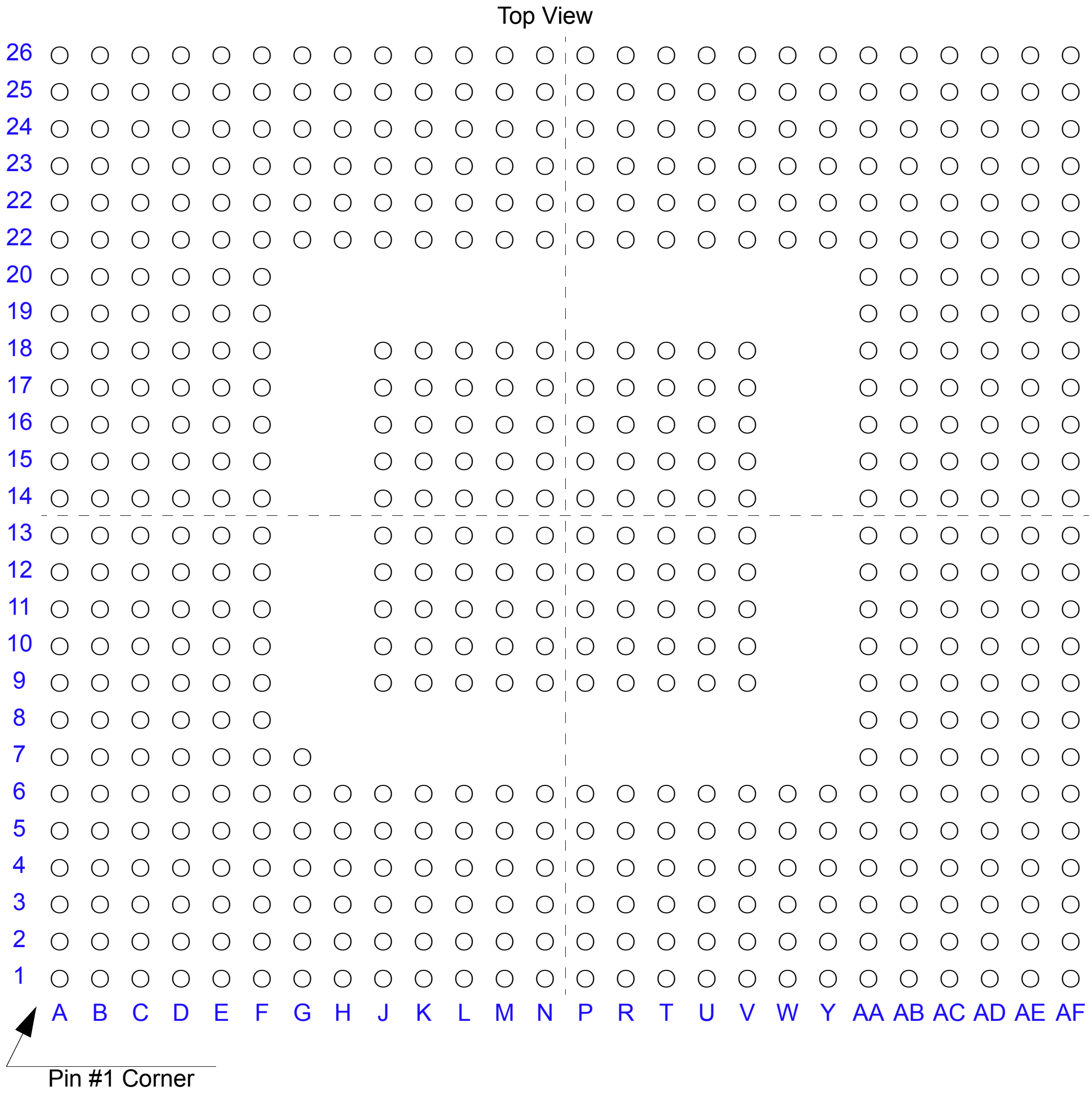
3.3 PCI Device List

Device#	0	1	2	3	4	5	6	7	8	9	10	11	12	13
IDSEL	AD11							AD18	AD19		AD21	AD22	AD23	
Function 0	NB							SB	MAC		USB0 OHCI	USB1 OHCI	IDE	
Function 1											USB0 EHCI	USB1 EHCI		

Chapter 4

PIN Function List

4.1 BGA Ball Map



	A	B	C	D	E	F	G	H	J	K	L	M	N
26	NC	AD24	TRDY_	PCIRST_	AD13	AD10	AD5	AD3	AD1	TXP	RXP	DP1	DP0
25	AD25	CBE_3	IRDY_	STOP_	AD14	AD9	AD7	AD4	AD2	TXN	RXN	DM1	DM0
24	AD26	CBE_2	FRAME_	DEVSEL_	AD15	CBE_0	PAR	AD0	ISET	VCCA0	VCCA1	VSSA1	AVSS0
23	AD27	AD16	AD17	TEST0	TEST4	VCC_SPI	AD11	INTA_	VCCAPLL	VSSAPLL	VSSA0	VCCABG	AVDDPLL 0
22	AD28	AD18	AD19	TEST2	TEST1	ATSTP	CBE_1	AD12	AD6	Duplex	Link/Active	VSSABG	AVDD0
21	AD29	AD20	AD21	GND_SPI	TEST3	ATSTN	ROM_CS_	AD8	TXC0	TXEN0	RXDV0	RXC0	RTC_AS_ GPIO_37
20	PCICLK_2	AD30	AD31	AD23	AD22	INTC_							
19	PCICLK_0	PREQ2	PGNT0	PGNT2	INTD_	INTB_							
18	PCICLK_1	PREQ1	PREQ0	PGNT1	VCC3V	VCC3V			TXD0_3	TXD0_0	RXD0_0	RXD0_3	Vdd_io
17	MD4	MD0	MD14	DQM1	GNDK	GND_R3			TXD0_2	TXD0_1	RXD0_1	RXD0_2	Vdd_io
16	MD3	MD1	MD9	MD15	MD15	GND_R3			MDC	MDIO	COL0	VCC3V	GND_R3
15	MD2	MD7	MD11	MD12	MD8	GND_R3			VCC3V	VCC3V	VCC3V	VCC3V	GND_R3
14	MD5	DQM0	MD13	DQS0	MD10	VCCK			VCCK	VCCK	VCCK	VCCK	GND_R3
13	MD6	CS_1	WE_	RAS_	CS_0	VCCK			GND_R3	GND_R3	GND_R3	GND_R3	GND_R3
12	MA10	MA6	BA2	BA0	CAS_	BA1			GNDK	GNDK	GNDK	GND_R3	GND_R3
11	MA1	MA5	MA7	MA9	MA11	MA13			GNDK	GNDK	GNDK	GNDK	GND_R3
10	MA0	MA3	MA4	VDLL0	GNDDLL0	MA12			GNDK	GNDK	GNDK	GNDK	GND_R3
9	SDRAM- CLKN	SDRAM- CLKP	MA2	VDLL1	GNDDLL1	MA8			TMS	GNDK	GNDK	GNDK	VCCK
8	NC	NC	NC	VCCO	GNDK	VCCK							
7	NC	NC	VCCO	VCCO	GNDK	GNDO	TCK						
6	NC	NC	VCCO	GNDO	GNDO	GNDO	TDO	TDI	SOUT9	SIN9	PE/SDD9	SOUT4	SIN4
5	NC	NC	VCCO	GNDO	GNDO	GNDO	GNDO	GNDPLL0	GNDPLL1	PD6/SDD6	PD5/SDD5	BUSY/ SDD10	SLCT/ SDD8
4	NC	NC	VCCO	VCCO	VCCO	GNDO	VCCK	VPLL0	VPLL1	PD7/SDD7	ACK_/ SDD11	PD4/SDD4	ERR_/ SDD14
3	NC	NC	NC	NC	TEST5	TEST6	SIN3	RTS3_/ SRST_	TESTCLK	PD3/SDD3	AFD_/ SDD15	SLIN_/ SDD12	PDD9
2	NC	NC	NC	NC	TEST7	TEST8	SOUT3	CTS3_/ SIOR_	DCD3_/ SDRQ	PD0/SDD0	PD1/SDD1	PD2/SDD2	PINT
1	NC	NC	NC	NC	NC	DTR3_/ SDACK_	RI3/ SIORDY	DSR3_/ SCBLID_	INIT_/ SDD13	PA2	STB_/ SCS0_	PRST_	PDD3
	A	B	C	D	E	F	G	H	J	K	L	M	N

P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
AVDD33_0	DP3	DP2	AVDD33_1	RTC_Xin	AVDD3	XOUT_14.318	POWER_GOOD	CLK25MOUT	DCD2_/PWM0CLK	CTS2_/PWM1GATE	DSR2_/PWM0GATE	NC	26
AVSSPLL0	DM3	DM2	AVSSPLL1	RTC_Xout	AVSS3	XIN_14.318	MTBF	CLK24Mout	DTR2_/PWM2OUT	RTS2_/PWM1OUT	TXD_EN2/PWM2GATE	SIN2/PWM2CLK	25
REXT0	AVDD1	AVSS2	REXT1	AVDDPLL1	SERIRQ	Vss_pll_1	Vdd_pll_1	Vdd_pll_0	Vss_pll_0	RI2_/PWM1CLK	SOUT2/PWM0OUT	DCD1_/GPIO_40	24
AVSS1	AVDD2	LAD0	LAD1	LAD2	LAD3	SPEAKER	Vdd_core	Vss_io	Vdd_io	DTR1_/GPIO_45	CTS1_/GPIO_47	DSR1_/GPIO_46	23
RTC_RD_GPIO_36	RTC_IRQ8_/GPIO_34	RTC_PS	SYSFAILOut_	Ext_Switch_fail_	E_SPI_CLK/GPIOP_31	E_SPI_DI/GPIOP_33	Vdd_core	Vss_io	Vdd_io	RI1_/GPIO_43	SOUT1/GPIO_41	RTS1_/GPIO_42	22
VBat	VBatGnd	RTC_WR_GPIO_35	ExtSysFailIn_	EXT_GPCS_	E_SPI_CS/GPIOP_30	E_SPI_DO/GPIOP_32	Vdd_core	Vss_io	Vdd_io	TXD_EN1	SIN1/GPIO_44	GPIO_P21/SA25	21
							GPIO_P27/SA31	GPIO_P26/SA30	Vss_io	GPIO_P25/SA29	GPIO_P24/SA28	GPIO_P22/SA26	20
							GPIO_P17	GPIO_P20/SA24	GPIO_P16	GPIO_P15	GPIO_P14	GPIO_P10	19
Vss_io	Vss_io	Vss_core	LFRAME_	LDRQ_			GPIO_P07	GPIO_P13	GPIO_P12	GPIO_P23/SA27	GPIO_P05	GPIO_P03	18
Vss_io	Vss_io	Vss_core	Vss_io	Vss_io			GPIO_P06	GPIO_P11	GPIO_P01	GPIO_P00	GPIO_P04	GPIO_P02	17
Vdd_io	Vss_io	Vss_core	Vss_core	KBDATA / A20GATE_			SD3	IOR_	GPCS0_	GPCS1_	SD15	SD14	16
Vdd_io	Vss_io	Vss_io	Vss_core	MSDATA			LA20	LA18	LA23	LA19	DRQ7	SD12	15
VCC3V	Vdd_io	Vss_io	Vss_core	MSCLK			SD4	IRQ9	SD2	SD6	LA21	SD11	14
VCC3V	Vdd_io	Vss_io	Vss_core	KBCLK_KBRST_			IOCHCK_	SA2	SBHE_	LA22	SA5	DACK_2	13
VCC3V	Vss_io	Vdd_core	Vss_core	Vss_core			SA3	DRQ0	Vss_core	SD8	MEMW_	SA1	12
VCC3V	Vss_io	Vdd_core	Vss_core	Vss_core			DRQ5	SA4	Vss_core	DACK_6	SD10	DRQ6	11
VCC3V	Vdd_io	Vss_io	Vdd_core	Vdd_core			SMEMR_	DACK_5	Vss_core	SD13	SD9	SYSCLK	10
VCCK	Vdd_io	Vss_io	Vss_io	Vss_io			SA19	SA17	DRQ2	DACK_0	LA17	MEMR_	9
							SMEMW_	AEN	IRQ12	0WS_	IOCHRDY_	OSC14M	8
							SD0	SA10	SA8	IRQ5	IRQ7	DACK_7	7
CTS4_/SIOW_	DCD4_/SA2	DSR4_/SCS1_	RTS4_/SINT	DTR4_/SA0	Vss_io	SD7	Vdd_io	Vss_core	Vdd_core	SA7	IRQ10	REFRESH_	6
PDD12	PDD2	PDD1	PDD11	RI4/SA1	Vss_io	DRQ3	Vdd_io	Vss_core	Vdd_core	SA18	SA9	TC	5
PDD10	PDD5	PDD6	PDD7	Vss_core	Vdd_io	SD5	Vdd_io	Vss_core	Vdd_core	DRQ1	BALE	IRQ15	4
PIORDY	PIOW_	PDD0	PDD8	Vdd_io	Vdd_io	DACK_3	SA16	DACK_1	SA0	SA11	IOCS16_	IRQ11	3
PA1	PA0	PCS0_	PDD4	PDD15	PDD14	IOW_	SA12	SA14	SA6	SA13	IRQ3	IRQ14	2
PDD13	PDRQ	PDACK_	PCBLID_	PIOR_	PCS1_	SD1	SA15	RSET_DRV	IRQ6	IRQ4	MEMCS16_	NC	1
P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	

4.2 PIN-Out Table

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
A1	NC	F17	GND_R3	P2	PA1	AA14	SD4
A2	NC	F18	VCC3V	P3	PIORDY	AA15	LA20
A3	NC	F19	INTB_	P4	PDD10	AA16	SD3
A4	NC	F20	INTC_	P5	PDD12	AA17	GPIO_P0_6
A5	NC	F21	ATSTN	P6	CTS4_/SIOW_	AA18	GPIO_P0_7
A6	NC	F22	ATSTP	P9	VCCK	AA19	GPIO_P1_7
A7	NC	F23	VCC_SPI	P10	VCC3V	AA20	GPIO_P2_7/ SA31
A8	NC	F24	CBE_0	P11	VCC3V	AA21	Vdd_core
A9	SDRAMCLKN	F25	AD9	P12	VCC3V	AA22	Vdd_core
A10	MA0	F26	AD10	P13	VCC3V	AA23	Vdd_core
A11	MA1	G1	RI3/SIORDY	P14	VCC3V	AA24	Vdd_pll_1
A12	MA10	G2	SOUT3	P15	Vdd_io	AA25	MTBF
A13	MD6	G3	SIN3	P16	Vdd_io	AA26	POWER_GOOD
A14	MD5	G4	VCCK	P17	Vss_io	AB1	RSET_DRV
A15	MD2	G5	GNDO	P18	Vss_io	AB2	SA14
A16	MD3	G6	TDO	P21	VBat	AB3	DACK_1
A17	MD4	G7	TCK	P22	RTC_RD_GPIO_ 36	AB4	Vss_core
A18	PCICLK_1	G21	ROM_CS_	P23	AVSS1	AB5	Vss_core
A19	PCICLK_0	G22	CBE_1	P26	REXT0	AB6	Vss_core
A20	PCICLK_2	G23	AD11	P25	AVSSPLL0	AB7	SA10
A21	AD29	G24	PAR	P24	AVDD33_0	AB8	AEN
A22	AD28	G25	AD7	R1	PDRQ	AB9	SA17
A23	AD27	G26	AD5	R2	PA0	AB10	DACK_5
A24	AD26	H1	DSR3_/SCBLID_	R3	PIOW_	AB11	SA4
A25	AD25	H2	CTS3_/SIOR_	R4	PDD5	AB12	DRQ0
A26	NC	H3	RTS3_/SRST_	R5	PDD2	AB13	SA2
B1	NC	H4	VPLL0	R6	DCD4_/SA2	AB14	IRQ9
B2	NC	H5	GNDPLL0	R9	Vdd_io	AB15	LA18
B3	NC	H6	TDI	R10	Vdd_io	AB16	IOR_
B4	NC	H21	AD8	R11	Vss_io	AB17	GPIO_P1_1
B5	NC	H22	AD12	R12	Vss_io	AB18	GPIO_P1_3
B6	NC	H23	INTA_	R13	Vdd_io	AB19	GPIO_P2_0/ SA24

B7	NC	H24	AD0	R14	Vdd_io	AB20	GPIO_P2_6/ SA30
B8	NC	H25	AD4	R15	Vss_io	AB21	Vss_io
B9	SDRAMCLKP	H26	AD3	R16	Vss_io	AB22	Vss_io
B10	MA3	J1	INIT_/SDD13	R17	Vss_io	AB23	Vss_io
B11	MA5	J2	DCD3_/SDRQ	R18	Vss_io	AB24	Vdd_pll_0
B12	MA6	J3	TESTCLK	R21	VBatGnd	AB25	CLK24MOut
B13	CS_1	J4	VPLL1	R22	RTC_IRQ8_/ GPIO_34	AB26	CLK25MOUT
B14	DQM0	J5	GNDPLL1	R23	AVDD2	AC1	IRQ6
B15	MD7	J6	SOUT9	R24	AVDD1	AC2	SA6
B16	MD1	J9	TMS	R25	DM3	AC3	SA0
B17	MD0	J10	GNDK	R26	DP3	AC4	Vdd_core
B18	PREQ1	J11	GNDK	T1	PDACK_	AC5	Vdd_core
B19	PREQ2	J12	GNDK	T2	PCS0_	AC6	Vdd_core
B20	AD30	J13	GND_R3	T3	PDD0	AC7	SA8
B21	AD20	J14	VCCK	T4	PDD6	AC8	IRQ12
B22	AD18	J15	VCC3V	T5	PDD1	AC9	DRQ2
B23	AD16	J16	MDC	T6	DSR4_/SCS1_	AC10	Vss_core
B24	CBE_2	J17	TXD0_2	T9	Vss_io	AC11	Vss_core
B25	CBE_3	J18	TXD0_3	T10	Vss_io	AC12	Vss_core
B26	AD24	J21	TXC0	T11	Vdd_core	AC13	SBHE_
C1	NC	J22	AD6	T12	Vdd_core	AC14	SD2
C2	NC	J23	VCCAPLL	T13	Vss_io	AC15	LA23
C3	NC	J24	ISET	T14	Vss_io	AC16	GPCS0_
C4	VCCO	J25	AD2	T15	Vss_io	AC17	GPIO_P0_1
C5	VCCO	J26	AD1	T16	Vss_core	AC18	GPIO_P1_2
C6	VCCO	K1	PA2	T17	Vss_core	AC19	GPIO_P1_6
C7	VCCO	K2	PD0/SDD0	T18	Vss_core	AC20	Vss_io
C8	NC	K3	PD3/SDD3	T21	RTC_WR_GPIO _35	AC21	Vdd_io
C9	MA2	K4	PD7/SDD7	T22	RTC_PS	AC22	Vdd_io
C10	MA4	K5	PD6/SDD6	T23	LAD0	AC23	Vdd_io
C11	MA7	K6	SIN9	T24	AVSS2	AC24	Vss_pll_0
C12	BA2	K9	GNDK	T25	DM2	AC25	DTR2_/ PWM2OUT
C13	WE_	K10	GNDK	T26	DP2	AC26	DCD2_/ PWM0CLK
C14	MD13	K11	GNDK	U1	PCBLID_	AD1	IRQ4
C15	MD11	K12	GNDK	U2	PDD4	AD2	SA13

C16	MD9	K13	GND_R3	U3	PDD8	AD3	SA11
C17	MD14	K14	VCCK	U4	PDD7	AD4	DRQ1
C18	PREQ0	K15	VCC3V	U5	PDD11	AD5	SA18
C19	PGNT0	K16	MDIO	U6	RTS4_/SINT	AD6	SA7
C20	AD31	K17	TXD0_1	U9	Vss_io	AD7	IRQ5
C21	AD21	K18	TXD0_0	U10	Vdd_core	AD8	0WS_
C22	AD19	K21	TXEN0	U11	Vss_core	AD9	DACK_0
C23	AD17	K22	Duplex	U12	Vss_core	AD10	SD13
C24	FRAME_	K23	VSSAPLL	U13	Vss_core	AD11	DACK_6
C25	IRDY_	K24	VCCA0	U14	Vss_core	AD12	SD8
C26	TRDY_	K25	TXN	U15	Vss_core	AD13	LA22
D1	NC	K26	TXP	U16	Vss_core	AD14	SD6
D2	NC	L1	STB_/SCS0_	U17	Vss_io	AD15	LA19
D3	NC	L2	PD1/SDD1	U18	LFRAME_	AD16	GPCS1_
D4	VCCO	L3	AFD_/SDD15	U21	ExtSysFailIn_	AD17	GPIO_P0_0
D5	GNDO	L4	ACK_/SDD11	U22	SYSFAILOut_	AD18	GPIO_P2_3/ SA27
D6	GNDO	L5	PD5/SDD5	U23	LAD1	AD19	GPIO_P1_5
D7	VCCO	L6	PE/SDD9	U26	REXT1	AD20	GPIO_P2_5/ SA29
D8	VCCO	L9	GNDK	U25	AVSSPLL1	AD21	TXD_EN1
D9	VDLL1	L10	GNDK	U24	AVDD33_1	AD22	RI1_/GPIO_43
D10	VDLL0	L11	GNDK	V1	PIOR_	AD23	DTR1_/GPIO_45
D11	MA9	L12	GNDK	V2	PDD15	AD24	RI2_/PWM1CLK
D12	BA0	L13	GND_R3	V3	Vdd_io	AD25	RTS2_/ PWM1OUT
D13	RAS_	L14	VCCK	V4	Vss_core	AD26	CTS2_/ PWM1GATE
D14	DQS0	L15	VCC3V	V5	RI4/SA1	AE1	MEMCS16_
D15	MD12	L16	COL0	V6	DTR4_/SA0	AE2	IRQ3
D16	MD15	L17	RXD0_1	V9	Vss_io	AE3	IOCS16_
D17	DQM1	L18	RXD0_0	V10	Vdd_core	AE4	BALE
D18	PGNT1	L21	RXDV0	V11	Vss_core	AE5	SA9
D19	PGNT2	L22	Link/Active	V12	Vss_core	AE6	IRQ10
D20	AD23	L23	VSSA0	V13	KBCLK_KBRST_	AE7	IRQ7
D21	GND_SPI	L24	VCCA1	V14	MSCLK	AE8	IOCHRDY_
D22	TEST2	L25	RXN	V15	MSDATA	AE9	LA17
D23	TEST0	L26	RXP	V16	KBDATA/ A20GATE_	AE10	SD9
D24	DEVSEL_	M1	PRST_	V17	Vss_io	AE11	SD10

D25	STOP_	M2	PD2/SDD2	V18	LDRQ_	AE12	MEMW_
D26	PCIRST_	M3	SLIN_/SDD12	V21	EXT_GPCS_	AE13	SA5
E1	NC	M4	PD4/SDD4	V22	Ext_Switch_fail_	AE14	LA21
E2	TEST7	M5	BUSY/SDD10	V23	LAD2	AE15	DRQ7
E3	TEST5	M6	SOUT4	V24	AVDDPLL1	AE16	SD15
E4	VCCO	M9	GNDK	V25	RTC_Xout	AE17	GPIO_P0_4
E5	GNDO	M10	GNDK	V26	RTC_Xin	AE18	GPIO_P0_5
E6	GNDO	M11	GNDK	W1	PCS1_	AE19	GPIO_P1_4
E7	GNDK	M12	GND_R3	W2	PDD14	AE20	GPIO_P2_4/ SA28
E8	GNDK	M13	GND_R3	W3	Vdd_io	AE21	SIN1/GPIO_44
E9	GNDDLL1	M14	VCCK	W4	Vdd_io	AE22	SOUT1/GPIO_41
E10	GNDDLL0	M15	VCC3V	W5	Vss_io	AE23	CTS1_/GPIO_47
E11	MA11	M16	VCC3V	W6	Vss_io	AE24	SOUT2/ PWM0OUT
E12	CAS_	M17	RXD0_2	W21	E_SPI_CS/ GPIOP_30	AE25	TXD_EN2/ PWM2GATE
E13	CS_0	M18	RXD0_3	W22	E_SPI_CLK/ GPIOP_31	AE26	DSR2_/ PWM0GATE
E14	MD10	M21	RXC0	W23	LAD3	AF1	NC
E15	MD8	M22	VSSABG	W24	SERIRQ	AF2	IRQ14
E16	DQS1	M23	VCCABG	W25	AVSS3	AF3	IRQ11
E17	GNDK	M24	VSSA1	W26	AVDD3	AF4	IRQ15
E18	VCC3V	M25	DM1	Y1	SD1	AF5	TC
E19	INTD_	M26	DP1	Y2	IOW_	AF6	REFRESH_
E20	AD22	N1	PDD3	Y3	DACK_3	AF7	DACK_7
E21	TEST3	N2	PINT	Y4	SD5	AF8	OSC14M
E22	TEST1	N3	PDD9	Y5	DRQ3	AF9	MEMR_
E23	TEST4	N4	ERR_/SDD14	Y6	SD7	AF10	SYSCLK
E24	AD15	N5	SLCT/SDD8	Y21	E_SPI_DO/ GPIOP_32	AF11	DRQ6
E25	AD14	N6	SIN4	Y22	E_SPI_DI/ GPIOP_33	AF12	SA1
E26	AD13	N9	VCCK	Y23	SPEAKER	AF13	DACK_2
F1	DTR3_/ SDACK_	N10	GND_R3	Y24	Vss_pll_1	AF14	SD11
F2	TEST8	N11	GND_R3	Y25	XIN_14.318	AF15	SD12
F3	TEST6	N12	GND_R3	Y26	XOUT_14.318	AF16	SD14
F4	GNDO	N13	GND_R3	AA1	SA15	AF17	GPIO_P0_2
F5	GNDO	N14	GND_R3	AA2	SA12	AF18	GPIO_P0_3
F6	GNDO	N15	GND_R3	AA3	SA16	AF19	GPIO_P1_0

F7	GNDO	N16	GND_R3	AA4	Vdd_io	AF20	GPIO_P2_2/ SA26
F8	VCCK	N17	Vdd_io	AA5	Vdd_io	AF21	GPIO_P2_1/ SA25
F9	MA8	N18	Vdd_io	AA6	Vdd_io	AF22	RTS1_/GPIO_42
F10	MA12	N21	RTC_AS_GPIO_3 7	AA7	SD0	AF23	DSR1_/GPIO_46
F11	MA13	N22	AVDD0	AA8	SMEMW_	AF24	DCD1_/GPIO_40
F12	BA1	N23	AVDDPLL0	AA9	SA19	AF25	SIN2/PWM2CLK
F13	VCCK	N24	AVSS0	AA10	SMEMR_	AF26	NC
F14	VCCK	N25	DM0	AA11	DRQ5		
F15	GND_R3	N26	DP0	AA12	SA3		
F16	GND_R3	P1	PDD13	AA13	IOCHCK_		

4.3 Function Pin Table

Function	Symbol	PIN Sum
SYSTEM	POWER_GOOD, 25MOUT, XOUT_14318, XIN_14318, MTBF, CLK24MOut, SPEAKER	7 PINs
SDRAM/DDR2	SDRAMCLK,SDRAMCLKN,RAS_ ,CAS_,WE_,CS_[1:0],DQM[1:0],DQS[1:0],BA[2:0],MD[15:0], MA[13:0]	44 PINs
USB 0,1,2,3	DP[3:0],DM[3:0],REXT[1:0]	10 PINs
PCI	PREQ_[2:0],PGNT_[2:0],PCIRST_,PCICLK_0, PCICLK_1,PCICLK_2,AD[31:0],CBE_[3:0], FRAME_, IRDY_, TRDY_, DEVSEL_, STOP_,PAR, INTA_, INTB_, INTC_, INTD_	56 PINs
External SPI / GPIO 3[3:0]	E_SPI_CS/GPIO_P3[0], E_SPI_CLK/GPIO_P3[1], E_SPI_DO/ GPIO_P3[2], E_SPI_DI/GPIO_P3[3]	4 PINs
ISA BUS	IOCHCK_, SD[15:0], IOCHRDY_, AEN, SA[19:0], SBHE_, LA[23:17], MEMR_, MEMW_, RSET_DRV, IRQ[15:14], IRQ[12:9], IRQ[7:3], DRQ[7:5], DRQ[3:0], 0WS_, SMEMR_, SMEMW_, IOW_, IOR_, DACK_[7:5], DACK_[3:0], REFRESH_, SYSCLK, TC, BALE, MEMCS16_,IOCS16_, OSC14M	87 PINs
Chip Selection	GPCS0_, GPCS1_ , ROM_CS_	3 PINs
Redundant	ExtSysFailIn_, SYSFAILOut_, Ext_Switch_fail_, EXT_GPCS_	4 PINs
KBD/MOUSE	KBCLK/KBRST_, KBDATA/A20GATE_, MSCLK, MSDATA	4 PINs
RTC	RTC_AS/GPIO_3[7], RTC_RD_/GPIO_3[6], RTC_WR_/GPIO_3[5], RTC_IRQ8_/GPIO_3[4], RTC_PS, RTC_Xout, RTC_Xin	7 PINs
COM1 / GPIO 4[7:0]	SIN1/GPIO_P4[4], SOUT1/GPIO_P4[1], RTS1_/GPIO_P4[2], CTS1_ / GPIO_P4[7] , DSR1_ / GPIO_P4[6], DCD1_ / GPIO_P4[0] , RI1_ / GPIO_P4[3] , DTR1_ / GPIO_P4[5], TXD_EN1	9 PINs
COM2/PWM	SIN2 / PWM2CLK, SOUT2 / PWM0OUT, RTS2_ / PWM1OUT, CTS2_ / PWM1GATE, DSR2_ / PWM0GATE, DCD2_ / PWM0CLK, RI2_ / PWM1CLK, DTR2_ / PWM2OUT, TXD_EN2 / PWM2GATE	9 PINs

COM 3,4,9	SIN3, SOUT3, SIN4, SOUT4, SIN9, SOUT9	6 PINs
IDE 0,1/COM3, COM4 and Parallel Port	PD/SDD[7 :0], SLCT/SDD8, PE/SDD9, BUSY/SDD10, ACK_/SDD11, SLIN_/SDD12, INIT_/SDD13, ERR_/SDD14, AFD_/SDD15, RTS3_/SRST_, DCD3_/SDRQ, CTS4_/SIOW_, CTS3_/SIOR_, RI3/SIORDY, DTR3_/SDACK_, RTS4_/SINT, RI4/SA1, DSR3_/SCBLID_, DTR4_/SA0, DCD4_/SA2, STB_/SCS0_, DSR4_/SCS1_, PRST_, PDD[15 :0], PDRQ, PIOW_, PIOR_, PIORDY, PDACK_, PINT, PA[2:0], PCBLID_, PCS0_, PCS1_	58 PINs
LPC	SERIRQ, LAD[3:0], LFRAME_, LDRQ_	7 PINs
GPIO 0,1,2[7:0]	GPIO_P0_[7:0],GPIO_P1_[7:0], GPIO_P2_0/SA24, GPIO_P2_1/SA25, GPIO_P2_2/SA26, GPIO_P2_3/SA27, GPIO_P2_4/SA28, GPIO_P2_5/SA29, GPIO_P2_6/SA30, GPIO_P2_7/SA31	24 PINs
Ethernet	Link/Active, Duplex, ISET, ATSTP, ATSTN, TXN, TXP, RXN, RXP MDC,MDIO, COL0, RXC0, RXD0_0, RXD0_1, RXD0_2, RXD0_3, RXDV0, TXC0, TXD0_0, TXD0_1, TXD0_2, TXD0_3, TXEN0	24 PINs
JTAG	TDO, TMS, TCK, TDI	4 PINs
TEST PIN	TESTCLK,TEST[8:0]	10 PINs
Rserved Function	S-ATA, I²C	27 PINs
1.3V Power	VDDLL: 2 PINs, GNDDLL : 2 PINs, VCCK : 10 PINS, GNDK : 17 PINs	31 PINs
1.8V Power	VCCO(SDR/DDR power, 1.8V/3.3V): 8 PINs, GNDO: 9 PINs, Vdd_core: 10 PINs, Vss_core: 18 PINs, AVDD[3:0],AVSS[3:0], AVDDPLL[1:0],AVSSPLL[1:0]: 12 PINs	57 PINs
Battery Power	VBat, VBatGnd : 2 PINs	2 PINs
3.3V Power	VPLL: 2 PINs, GNDPLL: 2 PINs, Vdd_pll : 2 PINs, Vss_pll : 2 PINs VCC3V : 12 PINs, GND_R3 : 15 PINs, Vdd_io : 17 PINs, Vss_io : 23 PINs VSSAPLL, VCCAPLL, VSSABG, VCCABG, VCCA0, VSSA0, VCCA1, VSSA1, AVDD33_[1:0] : 10 PINs VCC _SPI ,GND _SPI : 2 PINs	87 PINs

4.4 Signal Description

This chapter provides a detailed description of EVA-X4300 signals. A signal with the symbol "_n" at the end of itself indicates that this pin is low active. Otherwise, it is high active.

The following notations are used to describe the signal types:

I Input pin
O Output pin
OD Output pin with open-drain
I/O Bi-directional Input/Output pin

- **System (7 PINs)**

PIN No.	Symbol	Type	Description
AA26	PWRGOOD	I	***Power-Good Input.*** This signal comes from Power Good of the power supply to indicate that the power is available. The EVA-X4300 uses this signal to generate reset sequence for the system.
AB26	25MOUT	O	***25MHz Clock output.***
Y26	XOUT_14.318	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator).
Y25	XIN_14.318	I	***Crystal-in.*** 14.318MHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).
AA25	MTBF		***MTBF Flag output.***
AB25	CLK24MOUT	O	***24MHz Clock output***
Y23	SPEAKER	O	***Speaker Output.*** This pin is used to control the Speaker Output and should be connected to the Speaker

- **SDRAM /DDRII Interface (44 PINs)**

PIN No.	Symbol	Type	Description
B9	SDRAMCLK	O	***Clock output.*** This pin provides the fundamental timing for the SDRAM /DDR controller.
A9	SDRAMCLKN	O	***Clock output.*** This pin provides the fundamental timing for the SDRAM /DDR controller.
D13	RAS_	O	***Row Address Strobe.*** When asserted, this signal latches row address on positive edge of the SDRAM/DDR clock. This signal also allows row access and pre-charge.
E12	CAS_	O	***Column Address Strobe.*** When asserted, this signal latches column address on the positive edge of the SDRAM/DDR clock. This signal also allows column access and pre-charge.
C13	WE_	O	***Memory Write Enable.*** This pin is used as a write enable for the memory data bus.
B13, E13	CS_[1:0]	O	***Chip Select CS[1:0].*** These two pins activate the SDRAM devices. First Bank of SDRAM accepts any command when the CS0_n pin is active low. Second Bank of SDRAM accepts any command when the CS1_n pin is active low. For DDRII, only CS0_n activates the DDR device.
D17,B14	DQM[1:0]	O	***Data Mask DQM[1:0].*** These pins act as synchronized output enables during read cycles and byte masks during write cycles.

E16, D14	DQS[1:0]	I/O	***Data Strobe DQS[1:0 for DDR only.*** Output with write data, input with the read data for source synchronous operation.
F12, D12	BA[1:0]/ Strap[17:16]	O	***Bank Address BA[1:0].*** These pins are connected to SDRAM/DDR as bank address pins. ***Strap[17:16].*** Memory Select, Default pull high. Strap[17] Strap[16] DRAM Select 0 0 SDRAM 0 1 Reserved 1 0 DDR 1 1 DDRII (Default)
C12	BA[2]	O	***Bank Address [2].*** These pins are connected to SDRAM/DDR as bank address pins.
D16, C17, C14, D15, C15, E14, C16, E15, B15, A13, A14, A17, A16, A15, B16, B17	MD[15:0]	I/O	***Memory Data MD[15:0].*** These pins are connected to the SDRAM/DDR data bus.
A10	MA[0]	O	***Memory Address MA[0].*** Normally, these pins are used as the row and column address for SDRAM/DDR.
A11	MA[1]/Strap[1]	O	***Memory Address MA[1].*** Normally, these pins are used as the row and column address for SDRAM/DDR. **Strap[1].** Pull it high to enable GPIO2. Default pull high. Pull it low to enable Address[31:24].
C9	MA[2]	O	***Memory Address MA[2].*** Normally, these pins are used as the row and column address for SDRAM/DDR.
B10	MA[3] /Strap[3]	O	***Memory Address MA[3].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[3].*** PLL_TEST_OUT_EN_, Default pull low. Pull it high to enable PLL_TEST_OUT_EN_. Pull it low to disable PLL_TEST_OUT_EN_.
C10	MA[4] /Strap[4]	O	***Memory Address MA[4].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[4]/[10].*** SDRAM/DDR clock, Default pull high. Strap[10] Strap[4] SDRAM clock 0 0 100MHz 0 1 133MHz *(Internal default)* 1 0 166MHz 1 1 200MHz
C11,B12,B11	MA[7:5]/ Strap[7:5]	I/O	***Memory Address MA[7:5].*** Normally, these pins are used as the row and column address for SDRAM/DDR. **Strap[7:5] / CPU Clock** **3b'000 / Bypass mode** ***3b'001 / SYN_DISABLE_ (CPU clock same to SDRAM Clock)*** **3b'010 / 233MHz** **3b'011 / 266MHz** **3b'100 / 300MHz (Internal default)** **3b'101 / 333MHz** **3b'110 / 366MHz** **3b'111 / 400MHz**

F9	MA[8]/Strap[8]	I/O	***Memory Address MA[8].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[8].*** Pull it high to enable EVA-X4300 JTAG. Default internal pull-high.
D11	MA[9]/Strap[9]	I/O	***Memory Address MA[9].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[9].*** Pulled low: 33 PINS is for IDE2. Pulled high: 33 PINS is for COM3/4 and Parallel Port. Default internal pull-high.
A12	MA[10]/ Strap[10]	I/O	***Memory Address MA[10].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[4]/[10].*** SDRAM/DDR clock, Default pull low. Strap[10] Strap[4] Memory clock 0 0 100MHz 0 1 133MHz *(Internal default)* 1 0 166MHz 1 1 200MHz
E11	MA[11]/ Strap[11]	I/O	***Memory Address MA[11].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[11].*** Pulled low is Internal RTC. Default internal pull-low. Pulled high is External RTC
F11,F10	MA[13:12]/ Strap[13:12]	I/O	***Memory Address MA[13:12].*** Normally, these pins are used as the row and column address for SDRAM/DDR. ***Strap[13:12].*** 00 : flash-8bits 01 : flash-16bits 11 : Internal SPI. Default internal pull-high.

- **USB 0, 1, 2, 3 (10 PINs)**

PIN No.	Symbol	Type	Description
T26 T25	USB2_DP USB2_DM	I/O	Universal Serial Bus Controller 0 Port 0. These are the serial data pair for USB Port 0. 15kΩ pull down resistors are connected to DP and DM internally.
R26 R25	USB3_DP USB3_DM	I/O	Universal Serial Bus Controller 0 Port 1. These are the serial data pair for USB Port 1. 15kΩ pull down resistors are connected to DP and DM internally.
N26 N25	USB0_DP USB0_DM	I/O	Universal Serial Bus Controller 1 Port 0. These are the serial data pair for USB Port 2. 15kΩ pull down resistors are connected to DP and DM internally.
M26 M25	USB1_DP USB1_DM	I/O	Universal Serial Bus Controller 1 Port 1. These are the serial data pair for USB Port 3. 15kΩ pull down resistors are connected to DP and DM internally.
P26	REXT[0]:	I	Universal Serial Bus Controller 0 External Reference Resistance. 510Ω±10%
U26	REXT[1]:	I	Universal Serial Bus Controller 1 External Reference Resistance. 510Ω±10%

PCI Bus Interface (56 PINs)

PIN No.	Symbol	Type	Description
B19, B18, C18	PREQ_[2:0]	I	***PCI Bus Request.*** These signals are the PCI bus request signals used as inputs by the internal PCI arbiter.
D19, D18 ,C19	PGNT_[2:0]	O	***PCI Bus Grant.*** These signals are the PCI bus grant output signals generated by the internal PCI arbiter.
D26	PCIRST_	O	***PCI Reset.*** This pin is used to reset PCI devices. When it is asserted low, all the PCI devices will be reset.
A19 A18 A20	PCICLK_0 PCICLK_1 PCICLK_2	O	***PCI Clock Output.*** This clock is used by all of the EVA-X4300 logic that is in the PCI clock domain.
C20, B20, A21 A22, A23, A24, A25, B26, D20, E20, C21, B21, C22, B22, C23, B23, E24, E25, E26, H22, G23, F26, F25, H21, G25, J22, G26, H25, H26, J25, J26, H24	AD[31:0]	I/O	***PCI Address and Data.*** The standard PCI address and data lines. The address is driven with PCI Frame assertion and data is driven or received in the following clocks.
B25, B24, G22, F24	CBE_[3:0]	I/O	***Bus Command and Byte Enables.*** During the address phase, C/BE_n[3:0] defines the Bus Command. During the data phase, C/BE[3:0]_n define the Byte Enables.
C24	FRAME_	I/O	***PCI Frame.*** This pin is driven by a PCI master to indicate the beginning and duration of a PCI transaction.
C25	IRDY_	I/O	***PCI Initiator Ready.*** This pin is asserted low by the master to indicate that it is able to transfer the current data transfer. A data was transferred if both IRDY_n and TRDY_n are asserted low during the rising edge of the PCI clock.
C26	TRDY_	I/O	***PCI Target Ready.*** This pin is asserted low by the target to indicate that it is able to receive the current data transfer. A data was transferred if both IRDY_n and TRDY_n are asserted low during the rising edge of the PCI clock.
D24	DEVSEL_	I/O	***Device Select.*** This pin is driven by the devices which have decoded the addresses belonging to them.
D25	STOP_	I/O	***PCI Stop.*** This pin is asserted low by the target to indicate that it is unable to receive the current data transfer.
G24	PAR	I/O	***PCI Parity.*** This pin is driven to even parity by PCI master over the AD[31:0] and C/BE_n[3:0] bus during address and write data phases. It should be pulled high through a weak external pull-up resistor. The target drives parity during data read.
H23	INTA_	I	***PCI INTA_.*** PCI interrupt input A. It connects to PCI INTA_n when normal modes of PCI Interrupts are supported.
F19	INTB_	I	***PCI INTB_.*** PCI interrupt input B. It connects to PCI INTB_n when normal modes of PCI Interrupts are supported.
F20	INTC_	I	***PCI INTC_.*** PCI interrupt input C. It connects to PCI INTC_n when normal modes of PCI Interrupts are supported.
E19	INTD_	I	***PCI INTD_.*** PCI interrupt input D. It connects to PCI INTD_n when normal modes of PCI Interrupts are supported.

EXTERNAL SPI / PORT3[3:0] Interface (4 PINs)

PIN No.	Symbol	Type	Description
W21	E_SPI_CS_/GPIO_P3[0]	I/O	**External SPI Chip Select** **General-Purpose Input/Output P3[0]**
W22	E_SPI_CLK/GPIO_P3[1]	I/O	**External SPI Clock** **General-Purpose Input/Output P3[1]**
Y21	E_SPI_DO/GPIO_P3[2]	I/O	**External SPI Data Output** **General-Purpose Input/Output P3[2]**
Y22	E_SPI_DI/GPIO_P3[3]	I/O	**External SPI Data Input** **General-Purpose Input/Output P3[3]**

ISA Bus Interface (87 PINs)

PIN No.	Symbol	Type	Description
AA13	IOCHCK_	I	**I/O Channel Check**. Provides the system board with parity (error) information about memory or devices on the I/O channel.
AE16, AF16, AD10, AF15, AF14, AE11, AE10, AD12,Y6, AD14, Y4, AA14, AA16, AC14, Y1, AA7	SD[15:0]	I/O	**ISA high and low byte slot data bus**. These are the system data lines. These signals read data and vectors into CPU during memory or I/O read cycles or interrupt acknowledge cycles and outputs data from CPU during memory or I/O write cycles.
AE8	IOCHRDY_	I	**ISA system ready**. This input signal is used to extend the ISA command width for the CPU and DMA cycles.
AB8	AEN	O	**ISA address enable**. This active high output indicates that the system address is enabled during the DMA refresh cycles.
AA3, AA1, AB2, AD2,AA2, AD3, AB7, AE5, AC7, AD6, AC2, AE13, AB11, AA12, AB13, AF12, AC3	SA[16:0]	O	**ISA slot address bus.** These signals are high impedance during hold acknowledge.
AA9, AD5, AB9	SA[19:17]	O	**ISA slot address bus.** ISA slot address bus for 62-pin slot.
AC13	SBHE_	O	**ISA Bus high enable.** In master cycle, it is an input polarity signal and is driven by the master device.
AC15, AD13, AE14, AA15, AD15, AB15, AE9	LA[23:17]	O	**ISA latched address bus**. These are input signal during ISA master cycle.
AF9	MEMR_	O	**ISA memory read**. This signal is an input during ISA master cycle.
AE12	MEMW_	O	**ISA memory write**. This signal is an input during ISA master cycle.

	RST_DRV	O	**Driver Reset**. This output signal is driven active during system power up.
AF4, AF2, AC8, AF3, AE6, AB14, AE7, AC1, AD7, AD1, AE2	IRQ[15:14], IRQ[12:9], IRQ[7:3]	I	**Interrupt request signals**. These are interrupt request input signals.
AE15, AF11, AA11, Y5, AC9, AD4, AB12	DRQ[7:5], DRQ[3:0]	I	**DMA device request**. These are DMA request input signals.
AD8	0WS_	I	**ISA zero wait state**. This is the ISA device zero-wait state indicator signal. This signal terminates the CPU ISA command immediately.
AA10	SMEMR_	O	**ISA system memory read**. This signal indicates that the memory read cycle is for an address below 1M byte address.
AA8	SMEMW_	O	**ISA system memory write**. This signal indicates that the memory write cycle is for an address below 1M byte address.
Y2	IOW_	O	**ISA I/O write**. This signal is an input during ISA master cycle.
AB16	IOR_	O	**ISA I/O read**. This signal is an input during ISA master cycle.
AF7, AD11, AB10, Y3, AF13, AB3, AD9	DACK_[7:5], DACK_[3:0]	O	**DMA device acknowledge signals**. These are DMA acknowledge demultiplex select signals. Input function is for hardware setting.
AF6	REFRESH_	O	**Refresh cycle indicator**. ISA master uses this signal to notify DRAM needs refresh. During the memory controller's self-acting refresh cycle, M6117D drives this signal to the I/O channels.
AF10	SYSCLK	O	**System Clock Output**. This signal clocks the ISA bus.
AF5	TC	O	**DMA end of process**. This is the DMA channel terminal count indicating signal.
AE4	BALE	O	**Bus address latch enable**. BALE indicates the presence of a valid address at I/O slots.
AE1	MEMCS16_	I	ISA 16-bit memory device select indicator signal.
AE3	IOCS16_	I	ISA 16-bit I/O device select indicator signal.
AF8	OSC14M	O	14.318MHz clock out

Chip Selection Interface (3 PINs)

PIN No.	Symbol	Type	Description
AC16	GPCS0_	O	**ISA Bus Chip Select 0**. This pin is the chip select for ISA bus.
AD16	GPCS1_	O	**ISA Bus Chip Select 1**. This pin is the chip select for ISA bus.
G21	ROMCS_/SPICS_	O	***ROM Chip Select.*** This pin is used as a ROM chip select. ***SPI Chip Select.*** This pin is used as SPI flash chip select.

Redundant (4 PINs)

PIN No.	Symbol	Type	Description
U21	EXTSYSFAILIN_	I	**External system fail input**. This pin is the system fail in for redundancy.
U22	SYSFAILOUT_	O	**System fail output**. This pin is the system fail out for redundancy.
V22	EXT_SWITCH_FAIL_	I	**External switch fail**. This pin is the switch input for redundancy.
V21	EXT_GPCS_	I	**External GPCS input**. This pin is the GPCS in for redundancy.

KBD / MOUSE Interface (4 PINs)

PIN No.	Symbol	Type	Description
V13	KBCLK/KBRST	I/O	**Keyboard Clock**. This pin is keyboard clock when used internal 8042. **Keyboard Reset**. This pin is Keyboard reset when used external 8042.
V16	KBDAT/A20GATE	I/O	**Keyboard Data**. This pin is keyboard data when used internal 8042. **Address Bit 20 Mask**. This pin is A20 mask when used external 8042.
V14	MSCLK	I/O	**Mouse Clock**. This pin is mouse clock when used internal 8042.
V15	MSDAT	I/O	**Mouse Data**. This pin is mouse data when used internal 8042.

RTC / PORT3[7:4] Interface (7 PINs)

PIN No.	Symbol	Type	Description
N21	RTC_AS /GPIO_P3[7]	I/O	***RTC Address Strobe.*** This pin is used as the RTC Address Strobe and should be connected to the RTC. **General-Purpose Input/Output GPIO P3[7].**
P22	RTC_RD_ /GPIO_P3[6]	I/O	***RTC Read Command.*** This pin is used as the RTC Read Command and should be connected to the RTC. **General-Purpose Input/Output GPIO P3[6].**
T21	RTC_WR_ /GPIO_P3[5]	I/O	***RTC Write Command.*** This pin is used as the RTC Write Command and should be connected to the RTC. **General-Purpose Input/Output GPIO P3[5].**
R22	RTC_IRQ8_ /GPIO_P3[4]	I/O	***RTC Interrupt Input.*** This pin is used as the RTC Interrupt input. **General-Purpose Input/Output GPIO P3[4].**
T22	RTC_PS	I	**RTC Battery Power Sense.**
V25	RTC_XOUT	O	***Crystal-out***.
V26	RTC_XIN	I	***Crystal-in.***

COM1 / PORT4 Interface (9 PINs)

PIN No.	Symbol	Type	Description
AE21	SIN1/GPIO_P4[4]	I/O	***Receive Data.*** FIFO UART receiver serial data input signal. **General-Purpose Input/Output GPIO port4 [4].**
AE22	SOUT1/GPIO_P4[1]	I/O	***Transmit Data.*** FIFO UART transmitter serial data output from the serial port. ***General-Purpose Input/Output GPIO port4 [1].***
AF22	RTS1/GPIO_P4[2]	I/O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_n signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation. ***General-Purpose Input/Output GPIO port4 [2].***
AE23	CTS1/GPIO_P4[7]	I/O	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_n signal by reading bit 4 of Modem Status Register (MSR). A CTS_n signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_n changes the state. The CTS_n signal has no effect on the transmitter. **Note:** Bit 4 of the MSR is the complement of CTS_n. ***General-Purpose Input/Output GPIO port4 [7].***
AF23	DSR1/GPIO_P4[6]	I/O	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_n signal by reading bit5 of the Modem Status Register (MSR). A DSR_n signal states the change from low to high after the last MSR read sets bit1 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_n changes state. **Note:** Bit 5 of the MSR is the complement of DSR_n. ***General-Purpose Input/Output GPIO port4 [6].***
AF24	DCD1/GPIO_P4[0]	I/O	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_n signal by reading bit 7 of the Modem Status Register (MSR). A DCD_n signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. **Note:** Bit 7 of the MSR is the complement of DCD_n. ***General-Purpose Input/Output GPIO port4 [0].***

AD22	RI1/GPIO_P4[3]	I/O	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_n signal by reading bit 6 of the Modem Status Register (MSR). A RI_n signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_n changes state. **Note:** Bit 6 of the MSR is the complement of RI_n. **General-Purpose Input/Output GPIO port4 [3].**
AD23	DTR1/GPIO_P4[5]	I/O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_n signal to be inactive during the loop-mode operation. ***General-Purpose Input/Output GPIO port4 [5].***
AD21	TXD_EN1	I/O	***COM1 TX Status.*** This pin will be high when COM1 is transmitting.

■ **COM2 / PWM Interface (9 PINs)**

PIN No.	Symbol	Type	Description
AF25	SIN2/PWM2CLK	I	***COM2 Receive Data.*** FIFO UART receiver serial data input signal. ***PWM Timer2 Clock.*** This pin is PWM timer2 external clock input when SB register C0h bit2 is 1 (PINs for PWM).
AE24	SOUT2/PWM0OUT	O	***COM2 Transmit Data.*** FIFO UART transmitter serial data output from the serial port. ***PWM Timer0 Output.*** This pin is PWM timer0 output when SB register C0h bit2 is 1 (PINs for PWM).
AD25	RTS2/PWM1OUT	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_n signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation. ***PWM Timer1 Output.*** This pin is PWM timer1 output when SB register C0h bit2 is 1 (PINs for PWM).
AD26	CTS2/PWM1GATE	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_n signal by reading bit 4 of Modem Status Register (MSR). A CTS_n signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_n changes the state. The CTS_n signal has no effect on the transmitter. **Note:** Bit 4 of the MSR is the complement of CTS_n. ***PWM Timer1 Gate.*** This pin is PWM timer1 gate mask when SB register C0h bit2 is 1 (PINs for PWM).

AE26	DSR2/PWM0GATE	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_n signal by reading bit5 of the Modem Status Register (MSR). A DSR_n signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_n changes state. **Note:** Bit 5 of the MSR is the complement of DSR_n. ***PWM Timer0 Gate.*** This pin is PWM timer0 gate mask when SB register C0h bit2 is 1 (PINs for PWM).
AC26	DCD2/PWM0CLK	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_n signal by reading bit 7 of the Modem Status Register (MSR). A DCD_n signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. **Note:** Bit 7 of the MSR is the complement of DCD_n. ***PWM Timer0 Clock.*** This pin is PWM timer0 external clock input when SB register C0h bit2 is 1 (PINs for PWM).
AD24	RI2/PWM1CLK	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_n signal by reading bit 6 of the Modem Status Register (MSR). A RI_n signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_n changes state. **Note:** Bit 6 of the MSR is the complement of RI_n. ***PWM Timer1 Clock.*** This pin is PWM timer1 external clock input when SB register C0h bit2 is 1 (PINs for PWM).
AC25	DTR2/PWM2OUT	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_n signal to be inactive during the loop-mode operation. ***PWM Timer1 Output.*** This pin is PWM timer1 output when SB register C0h bit2 is 1 (PINs for PWM).
AE25	TXD_EN2/ PWM2GATE	I/O	***COM2 TX Status.*** This pin will be high when COM2 is transmitting. ***PWM Timer2 Gate.*** This pin is PWM timer2 gate mask when SB register C0h bit2 is 1 (PINs for PWM).

COM3, 4, 9 (6 PIN)

PIN No.	Symbol	Type	Description
G3	SIN3	I	***COM3 Receive Data.*** FIFO UART receiver serial data input signal.
G2	SOUT3	O	***COM3 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
N6	SIN4	I	***COM4 Receive Data.*** FIFO UART receiver serial data input signal.
M6	SOUT4	O	***COM4 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
K6	SIN9	I	***COM9 Receive Data.*** FIFO UART receiver serial data input signal.
J6	SOUT9	O	***COM9 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.

IDE 0, 1 / COM3,4,PRINT1 Interface (58 PINs)

PIN No.	Symbol	Type	Description
K4, K5, L5, M4, K3, M2, L2, K2	PD[7:0]/SDD[7:0]	I/O	***Parallel port data bus bit .*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. **IDE Secondary Channel Data Bus.**
N5	SLCT/SDD8	I/O	***SLCT.*** An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode. **IDE Secondary Channel Data Bus.**
L6	PE/SDD9	I/O	***PE.*** An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. **IDE Secondary Channel Data Bus.**
M5	BUSY/SDD10	I/O	***BUSY.*** An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode. **IDE Secondary Channel Data Bus.**
L4	ACK_/SDD11	I/O	***ACK_.*** An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. **IDE Secondary Channel Data Bus.**
M3	SLIN_/SDD12	SLIN_: OD SDD12: I/O	***SLIN_.*** Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. **IDE Secondary Channel Data Bus.**
J1	INIT_/SDD13	INIT_: OD SDD13: I/O	***INIT_.*** Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. **IDE Secondary Channel Data Bus.**
N4	ERR_/SDD14	I/O	***ERR_.*** An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. **IDE Secondary Channel Data Bus.**

L3	AFD_/SDD15	AFD_: OD SDD15: I/O	***AFD_.*** An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. **IDE Secondary Channel Data Bus.**
H3	RTS3_/SRST_	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_n signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation. ***IDE Secondary Channel Reset.***
J2	DCD3_/SDRQ	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_n signal by reading bit 7 of the Modem Status Register (MSR). A DCD_n signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. **Note:** Bit 7 of the MSR is the complement of DCD_n. **IDE Secondary Channel DMA Request.**
P6	CTS4_/SIOW_	I/O	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_n signal by reading bit 4 of Modem Status Register (MSR). A CTS_n signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_n changes the state. The CTS_n signal has no effect on the transmitter. **Note:** Bit 4 of the MSR is the complement of CTS_n. **IDE Secondary Channel IO Write Strobe.**
H2	CTS3_/SIOR_	I/O	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_n signal by reading bit 4 of Modem Status Register (MSR). A CTS_n signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_n changes the state. The CTS_n signal has no effect on the transmitter. **Note:** Bit 4 of the MSR is the complement of CTS_n. **IDE Secondary Channel IO Read Strobe.**
G1	RI3/SIORDY	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_n signal by reading bit 6 of the Modem Status Register (MSR). A RI_n signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_n changes state. **Note:** Bit 6 of the MSR is the complement of RI_n. **IDE Secondary Channel IO Channel Ready.**

F1	DTR3_/SDACK_	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_n signal to be inactive during the loop-mode operation. **IDE Secondary Channel DMA Acknowledge.**
U6	RTS4_/SINT	I/O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_n signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation. **IDE Secondary Channel Interrupt.**
V5	RI4/SA1	I/O	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_n signal by reading bit 6 of the Modem Status Register (MSR). A RI_n signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_n changes state. **Note:** Bit 6 of the MSR is the complement of RI_n. **IDE Secondary Channel Device Address.**
H1	DSR3_/SCBLID_	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_n signal by reading bit5 of the Modem Status Register (MSR). A DSR_n signal states the change from low to high after the last MSR read sets bit1 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_n changes state. **Note:** Bit 5 of the MSR is the complement of DSR_n. **IDE Secondary Channel Cable Assembly Type Identifier.**
V6	DTR4_/SA0	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_n signal to be inactive during the loop-mode operation. **IDE Secondary Channel Device Address.**
R6	DCD4_/SA2	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_n signal by reading bit 7 of the Modem Status Register (MSR). A DCD_n signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. **Note:** Bit 7 of the MSR is the complement of DCD_n. **IDE Secondary Channel Device Address.**

L1	STB_/SCS_0	STB_: OD SCC_0: I	***STB_.*** An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. **IDE Secondary Channel Chip Select.**
T6	DSR4_/SCS1_	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_n signal by reading bit5 of the Modem Status Register (MSR). A DSR_n signal states the change from low to high after the last MSR read sets bit1 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_n changes state. **Note:** Bit 5 of the MSR is the complement of DSR_n. **IDE Secondary Channel Chip Select.**
M1	PRST_	O	**IDE Primary Channel Reset.**
V2, W2, P1, P5, U5, P4, N3, U3, U4 T4, R4, U2, N1, R5, T5, T3	PDD[15:0]	I/O	**IDE Primary Channel Data Bus.**
R1	PDRQ	I	**IDE Primary Channel DMA Request.**
R3	PIOW_	O	**IDE Primary Channel IO Write Strobe.**
V1	PIOR_	O	**IDE Primary Channel IO Read Strobe.**
P3	PIORDY	I	**IDE Primary Channel IO Channel Ready.**
T1	PDACK_	O	**IDE Primary Channel DMA Acknowledge.**
N2	PINT	I	**IDE Primary Channel Interrupt.**
K1, P2, R2	PA[2:0]	O	**IDE Primary Channel Device Address**
U1	PCBLID_	I	**IDE Primary Channel Cable Assembly Type Identifier.**
W1	PCS1_	O	**IDE Primary Channel Chip Select.**
T2	PCS0_	O	**IDE Primary Channel Chip Select.**

LPC Bus Interface (7 PINs)

PIN No.	Symbol	Type	Description
W24	SERIRQ	I/O	***Serial Interrupt Request.*** This pin is used to support the serial interrupt protocol of common architecture.
W23, V23, U23, T23	LAD[3:0]	I/O	***LPC Command, Address and Data LAD[3:0].*** These pins are used to be command/address/data pins of Low-Pin-Count Function.
U18	LFRAME_	O	***Low Pin Count FRAME_n Signal.*** This signal is used as a frame signal of low pin count protocol..
V18	LDRQ_	I	***Low Pin Count DMA Request Signal.*** This signal is used as a DMA request signal of low pin count protocol.

GPIO Interface (24 PINs)

PIN No.	Symbol	Type	Description
AA18, AA17, AE18, AE17, AF18, AF17, AC17, AD17, AA19, AC19, AD19, AE19, AB18, AC18, AB17, AF19	GPIO_P0[7:0] GPIO_P1[7:0]	I/O	***General-Purpose Input/Output P0[7-0] and P1[7-0].*** Those pins can be programmed input or output individually.
AA20, AB20, AD20, AE20, AD18, AF20, AF21, AB19	GPIO_P2[7:0]/ Address[31:24]	I/O	***General-Purpose Input/Output P2[7-0] .*** Those pins can be programmed input or output individually. **Address[31:24].**

Ethernet Interface (24 PINs)

PIN No.	Symbol	Type	Description
L22	Link/Active		***Link/Active:*** Link/active status
K22	Duplex		***Duplex:*** Duplex status
J24	ISET		***ISET:*** External resistor connecting pin for BIAS
F22	ATSTP		***ATSTP:*** VGA and ADC testing pin for input and output (positive)
F21	ATSTN		***ATSTN:*** VGA and ADC testing pin for input and output (negative)
K25	TXN		***TXN:*** 10B-T/100BT transmitting output pin/ reviving input pin (positive)
K26	TXP		***TXP:*** 10B-T/100BT transmitting output pin/ reviving input pin (negative)
L25	RXN		***RXN:*** 10B-T/100BT reviving input pin/ transmitting output pin (positive)
L26	RXP		***RXP:*** 10B-T/100BT reviving input pin/ transmitting output pin (negative)
J16	MDC	O	***MDC:*** MII management data clock is sourced by the EVA-X4300 to the external PHY devices as a timing reference for the transfer of information on the MDIO signal.
K16	MDIO	I/O	***MDIO:*** MII management data input/output transfers control information and status between the external PHY and the EVA-X4300.
L16	COL0	I	***COL0:*** This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
M21	RXC0	I	***RXC0:*** Supports the receive clock supplied by the external PMD device. This clock should always be active.
M18, M17 L17, L18	RXD0_[3:0]	I	***RXD0_[3:0]:*** Four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal.
L21	RXDV0	I	***RXDV0:*** Data valid is asserted by an external PHY when the received data is present on the RXD[3:0] lines and is de-asserted at the end of the packet. This signal should be synchronized with the RXC signal.
J21	TXC0	I	***TXC0:*** Supports the transmit clock supplied by the external PMD device. This clock should always be active.
J18, J17, K17, K18	TXD0_[3:0]	O	***TXD0_[3:0]:*** Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal.
K21	TXEN0	O	***TXEN0:*** This pin functions as Transmit Enable. It indicates that a transmission to an external PHY device is active on the MII port.

JTAG Interface (4 PINs)

PIN No.	Symbol	Type	Description
G6	TDO	O	***TDO:*** JTAG Test Data Output pin.
J9	TMS	I	***TMS:*** JTAG Test Mode Select pin.
G7	TCK	I	***TCK:*** JTAG Test Clock Input pin.
H6	TDI	I	***TDI:*** JTAG Test Data Input pin.

TEST PIN (10 PIN)

PIN No.	Symbol	Type	Description
J3	TESTCLK	I/O	For Testing used.
E23, E21, D22, E22, D23, F2, F3, E2, E3	TEST[8:0]	I/O	For Testing used. Test 3 and Test 4 must pull high to 3.3 V.

1.3 V POWER (14 PINs)

PIN No.	Symbol	Type	Description
D9, D10	VDDLL (2 PINs)	I	DLL power
E9, E10	GNDDLL (2 PINs)	I	DLL ground
F8,F13,F14,G4,J14 ,K14,L14,N9,M14,P9	VCCK (10 PINs)	I	Core power
E7,E8,E17,J10,J11,J12,K9, K10,K11,K12, L9,L10,L11, L12,M9,M10, M11	GNDK (17 PINs)	I	Code ground

1.8 V POWER (57 PINs)

PIN No.	Symbol	Type	Description
C4,C5,C6,C7, D4,D7,D8,E4	VCCO (8 PINs)	I	SDR/DDRII power (3.3 V/1.8 V)
D5,D6,E5,E6, F4,F5,F6,F7, G5	GNDO (9 PINs)	I	SDR/DDRII ground
AA21,AA22, AA23,AC4, AC5,AC6,T11, T12,U10,V10	Vdd_core (10 PINs)	I	Core power
T16, T17, T18, U11, U12, U13, U14, U15, U16, V4, V11, V12, AB4, AB5, AB6, AC10, AC11, AC12	Vss_core (18 PINs)	I	Core ground
W26, R23, R24, N22	AVDD[3:0]	I	Analog power
W25, T24, P23, N24	AVSS[3:0]	I	Analog ground
V24, N23	AVDDPLL[1:0]	I	USB PLL power
U25, P25	AVSSPLL[1:0]	I	USB PLL ground

Battery POWER (2 PINs)

PIN No.	Symbol	Type	Description
P21	VBat	I	Battery power for RTC
R21	VBatGnd	I	Battery ground for RTC

3.3 V Power (87 PINs)

PIN No.	Symbol	Type	Description
H4, J4	VPLL (2 PINs)	I	Analog power
H5, J5	GNDPLL (2 PINs)	I	Analog ground
AA24, AB24	Vdd_pll (2 PINs)	I	Analog power
Y24, AC24	Vss_pll (2 PINs)	I	Analog ground
E18, F18, J15, K15, L15, M15, M16, P10, P11, P12, P13, P14	VCC3V (12 PINs)	I	Analog power
F15, F16, F17, J13, K13, L13, M12, M13, N10, N11, N12, N13, N14, N15, N16	GND_R3 (15 PINs)	I	Analog ground
AA4, AA5, AA6, AC21, AC22, AC23, N17, N18, P15, P16, R9, R10, R13, R14, V3, W3, W4	Vdd_io (17 PINs)	I	IO power
P17, P18, R11, R12, R15, R16, R17, R18,T9, T10, T13, T14, T15, U9, U17, V9, V17, W5, W6, AB21, AB22, AB23, AC20	Vss_io (23 PINs)	I	IO ground
K23	VSSAPLL	I	Analog ground
J23	VCCAPLL	I	Analog power
M22	VSSABG	I	Analog ground
M23	VCCABG	I	Analog power
K24	VCCA0	I	Analog power
L23	VSSA0	I	Analog ground
L24	VCCA1	I	Analog power
M24	VSSA1	I	Analog ground
P24	AVDD33_0	I	Analog power
U24	AVDD33_1	I	Analog power
F23	VCC_SPI	I	SPI flash power
D21	GND_SPI	I	SPI flash ground

Chapter 5

System Address Map

The EVA-X4300 microprocessor supports 4 Gbytes of addressable memory space and 64 Kbytes of addressable I/O space. In order to be compatible with PC/AT system, the lower 1 Mbytes of this addressable memory is divided into regions which can be individually controlled with programmable attributes such as disable, read/write, write only, or read only (see Chapter 11, Register Description section for details on attribute programming).

5.1 Memory Address Ranges

Figure 5.1 represents EVA-X4300 microprocessor memory address map. It shows the main memory regions defined and supported by the EVA-X4300. At the highest level, the address space is divided into two main conceptual regions. One is the 0~1-Mbyte DOS compatibility region and the other is 1-Mbyte to 4-Gbyte extended memory region. The EVA-X4300 processor supports several main memory sizes from 2 MB to 256 MB. The main memory type and size in the system will be auto-detected by the system BIOS.

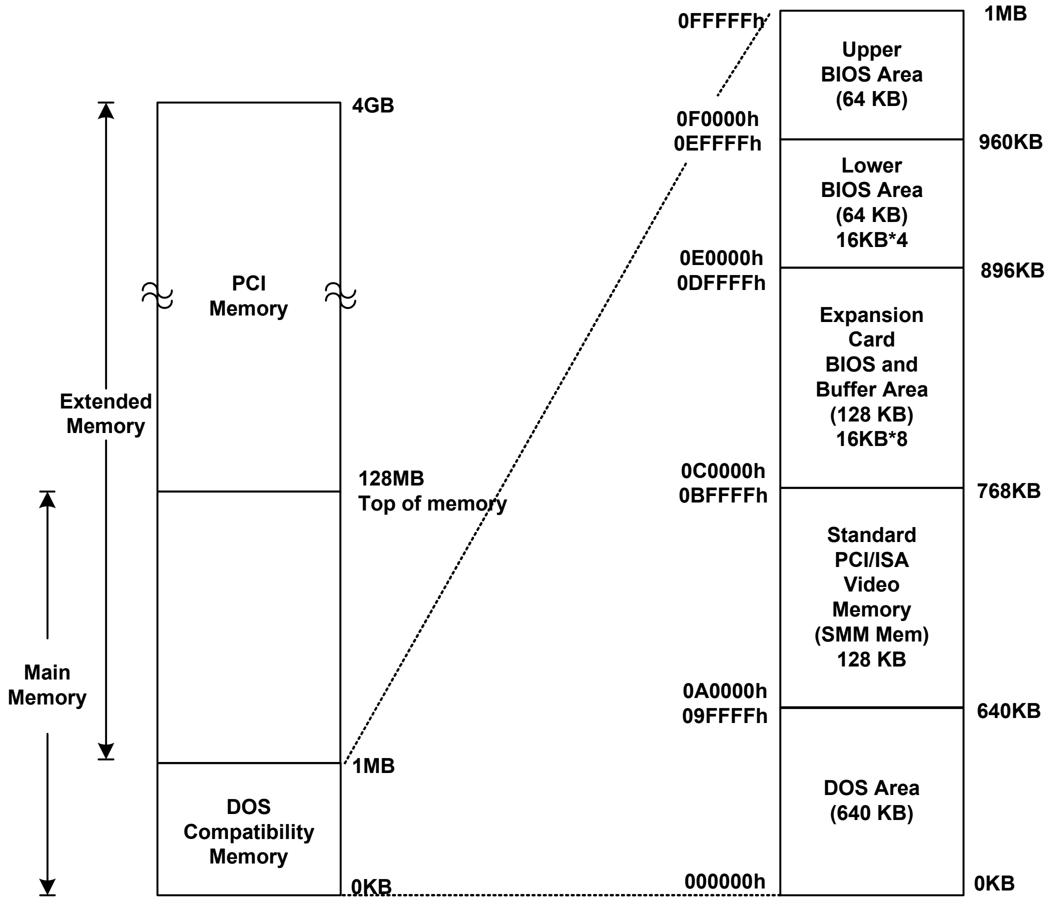


Figure 5.1 Memory Address Map

5.1.1 DOS Compatibility Region

The first region of memory is called the Dos Compatibility Region because it is defined for early PC. This area is divided into the following address regions:

- 0 ~ 640-Kbyte DOS Area
- 640 ~ 768-Kbyte Video Buffer Area
- 768 ~ 896-Kbyte in 16-Kbyte sections (total of 8 sections) - Expansion Area
- 896 ~ 960-Kbyte in 16-Kbyte sections (total of 4 sections) - Extended System BIOS Area
- 960-Kbyte ~ 1-Mbyte Memory (BIOS Area) - System BIOS Area

From 640 Kbytes - 1Mbytes: it can be divided into fourteen ranges which can be enabled or disabled independently for both read and write. These regions can also be mapped to either main DRAM or PCI by system BIOS. (See A/B Page control Register and Memory Attribute Register in Section 3, Chapter 11.)

DOS Area (00000 ~ 9FFFFh)

The DOS area (00000h ~ 9FFFFh) is 640 Kbytes in size. It is always mapped to the main memory controlled by the EVA-X4300 microprocessor.

Video Buffer Area (A0000 ~ BFFFFh)

The 128-Kbyte graphics adapter memory region is normally mapped to a video device on the PCI bus (typically VGA controller). This area is controlled by the A/B Page control Register. It can be mapped to either main DRAM or PCI for both read and write command.

ISA Expansion Area (C0000 ~ DFFFFh)

This 128-Kbyte ISA Expansion region is divided into eight 16-Kbyte segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through the PCI Bridge to ISA space. Memory that is disabled is not remapped.

Extended System BIOS Area (E0000 ~ EFFFFh)

This 64-Kbyte area is divided into four 16-Kbyte segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to PCI. Typically, this area is used for RAM or ROM. Memory that is disabled is not remapped.

System BIOS Area (F0000 ~ FFFFFh)

This area is a single 64-Kbyte segment that can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to PCI. By manipulating the read/write attributes, the EVA-X4300 microprocessor can “shadow” BIOS into main memory. Memory that is disabled is not remapped.

5.1.2 Extended Memory Region

This memory region covers 10_0000h (1 Mbytes) to FFFF_FFFFh (4 Gbytes minus 1) address range and is divided into the following regions:

- DRAM memory from 1 Mbytes to a top of memory (maximum: 256 Mbytes)
- PCI Memory space from the top of memory to 4 Gbytes
- APIC Configuration Space from FEC00000h (4 Gbytes minus 20 Mbytes) to FEC0_FFFFh
- High BIOS area from 4 Gbytes to 4 Gbytes minus 2 Mbytes

Main DRAM Address Range (0010_0000h to Top of Main Memory)

The address range from 1 Mbytes to the top of main memory is mapped to the main memory address range controlled by the EVA-X4300 microprocessor. All accesses to addresses within this range are forwarded to the main memory.

PCI Memory Address Range (Top of Main Memory to 4 Gbytes)

The address range from the top of main DRAM to 4 Gbytes is normally mapped to PCI. The PMC forwards all accesses within this address range to PCI.

Within this address range, there are two sub-ranges defined as APIC Configuration Space and High BIOS Address Range.

1. High BIOS Area (FFE0_0000 ~ FFFF_FFFFh)

The top 2 Mbytes of the Extended Memory Region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The CPU begins execution from the High BIOS after reset. This region is mapped to the PCI so that the upper subset of this region is aliased to 16 Mbytes minus 256 Kbytes range. The actual address space required for the BIOS is less than 2 Mbytes. However, the minimum CPU MTRR range for this region is 2 Mbytes. Thus, the full 2 Mbytes must be considered.

5.2 Memory Shadowing

Any block of memory that can be designated as read only or write only can be “shadowed” into PMC DRAM memory. Typically, this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as read only during the copy process while DRAM at the same time is designated write only. After copying, the DRAM is designated read only so that ROM is shadowed. CPU bus transactions are routed accordingly. The PMC does not respond to transactions originating from PCI or ISA masters and targeted at shadowed memory blocks.

5.3 I/O Address Space

The EVA-X4300 positively decodes accesses to all internal registers, including PCI configuration registers (CF8h and CFCh), PC/AT Compatible IO registers (8237, 8254 & 8259), and all relocatable IO space registers (UART).

Chapter 6

Operation Mode

6.1 Operation Mode

The EVA-X4300 microprocessor supports three operation modes: protected mode and real-address mode. The operation mode determines which instructions and architectural features are accessible:

- **Protected mode.** In this mode all instructions and architectural features are available, providing the highest performance and capability. This is the recommended mode for all new applications and operating systems.

  Among the capabilities of protected mode is the ability to directly execute “real-address mode” 8086 software in a protected, multitasking environment. This feature is called virtual-8086 mode, although it is not actually a processor mode. Virtual-8086 mode is actually a protected mode attribute that can be enabled for any task.
- **Real-address mode.** It provides the programming environment of the Intel 8086 processor with a few extensions (such as the ability to switch to protected or system management mode). The processor is placed in real-address mode following power-up or a reset.
- **Flat mode.** In general, this mode is similar with Real-Address mode. But there is one difference involved, i.e. Flat mode can access 4 GBytes address.

Chapter 7

Package Information

7.1 Package Information

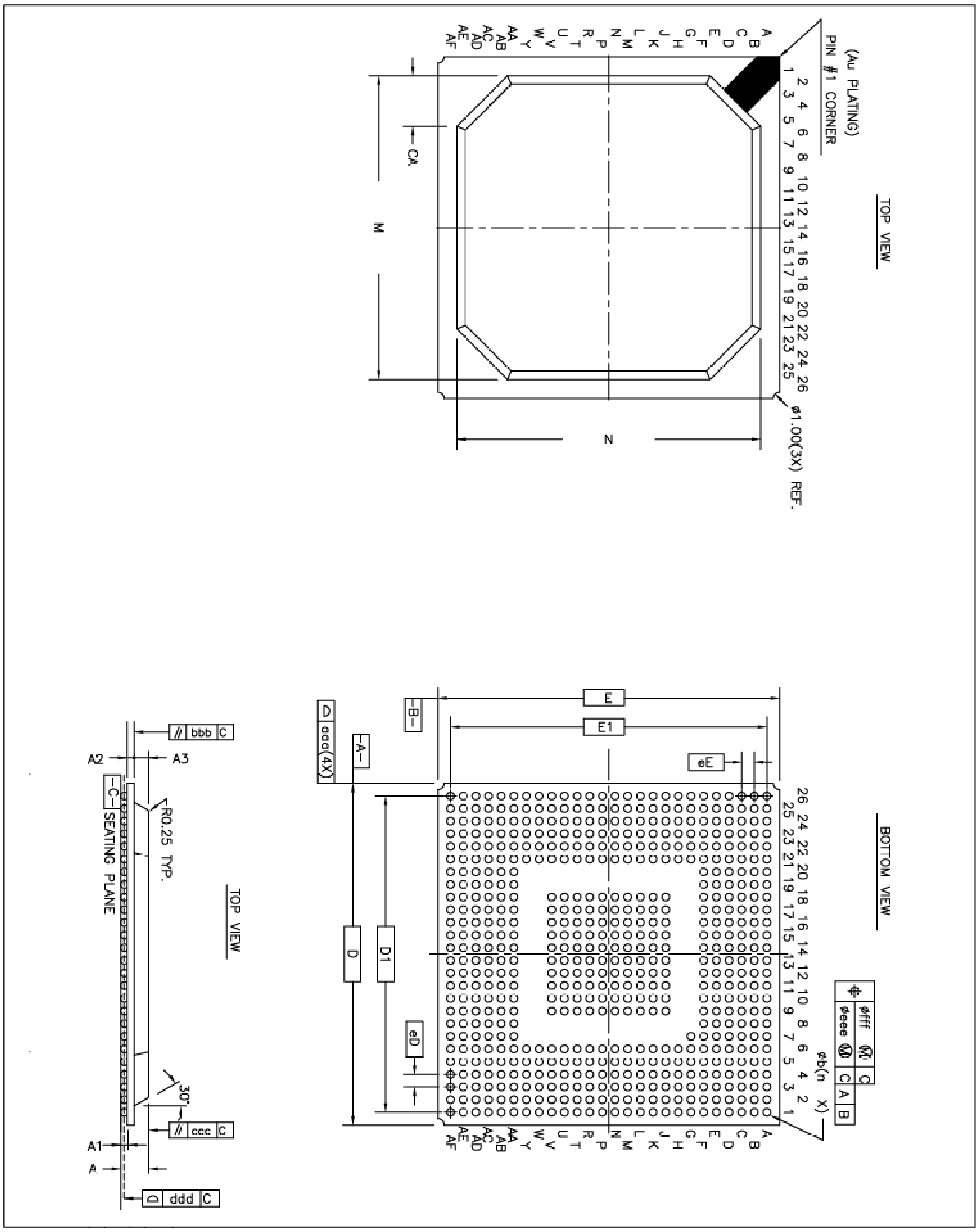


Figure 7.1 Package Information

		Symbol	Common Dimensions
Package :			PBGA
Body Size:	X	D	27
	Y	E	27
Ball Pitch :	X	eD	1
	Y	eE	1
Total Thickness :		A	2.23 +/− 0.13
Mold Thickness :		A3	1.17 Ref.
Substrate Thickness :		A2	0.56 Ref.
Ball Diameter :			0.60
Stand Off :		A1	0.40~0.60
Width :		b	0.50 ~ 0.70
Mold Area :	X	M	24
	Y	N	24
Chamfer		CA	4
Package Edge Tolerance :		aaa	0.20
Substrate Flatness :		bbb	0.25
Mold Flatness :		ccc	0.35
Coplanarity:		ddd	0.20
Ball Offset (Package) :		eee	0.25
Ball Offset (Ball) :		fff	0.10
Ball Count :		n	581
Edge Ball Center to Center :	X	D1	25
	Y	E1	25

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