User Manual

EVA-X4150

Product Brief

Trusted ePlatform Services

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Chapter 1

Overview

1.1 Overview

The EVA-X4150 is a fully static 32-bit x86-based processor that is compatible with a wide-range of PC peripherals, applications and operating systems, such as DOS, WinCE, Linux, and most popular 32-bit RTOSs (Real Time OS). It enables maximum software re-use based on its feature of legacy compatibility. The EVA-X4150 integrates 16 KB write-through direct map L1 cache, a PCI bus interface at 33 MHz, an 8/16-bit ISA bus interface, SDRAM, a ROM controller, IPC (Internal Peripheral Controllers) with DMA and interrupt timer/counter included, FIFO UART, I2C, SPI (Serial Peripheral Interface), LPC (Low Pin Count), a USB 1.1/2.0 host controller, an Ethernet MAC, and an IDE controller within a single 456-pin BGA package to form an SoC (System-on-Chip) processor. The EVA-X4150 integrates comprehensive features and rich I/O flexibility within a single System-on-Chip, to reduce board design complexity and shorten product development schedules. Taking advantage of ultra low power consumption, the EVA-X4150 is able to operate in a wide range of temperatures without additional thermal design. With the commitment of long term supply guaranteed for the EVA-X4150, customers can extend product life cycle and receive a maximum return on investment. Implement the perfect x86-based SoC for diverse embedded applications with the EVA-X4150.

The EVA-X4150 provides an ideal solution for embedded system and communication products producing optimal performance.

Chapter   2

**Features**

2.1 Features

- **RISC Processor Core**
  - 6 stage pipeline, 150 MHz
- **Embedded L1 Cache**
  - 16 K L1 Cache
- **SDRAM Control Interface**
  - Speeds up to 150 MHz
  - 8/16 bits data bus width
  - Memory space up to 128 MB
  - Supports DLL for clock phase auto-adjust
- **DMA Controller**
  - Provides two 82C37 compatible DMA controllers
  - 4-channel 8-bit DMA transfer and 3-channel 16-bit DMA controller
- **Interrupt Controller**
  - Provides two 8259 compatible interrupt controllers
  - Independent programmable level/edge-trigger interrupt channels
- **Counter / Timers**
  - One set 8254 compatible timer controller
  - Three independent programmable timers / counters
  - Supports one Watch Dog Timer (WDT)
- **General Chip Selector**
  - Two sets extended Chip Selector
  - Configurable I/O-map or Memory-map
  - I/O Addressing: From 2 byte to 64 KB
  - Memory Address: From 512 byte to 16 MB
- **PCI Control Interface**
  - 32 bit, 33 MHz, compliant with PCI spec. Rev. 2.1
  - Up to 3 individual PCI master devices
  - Up to 133 MB/s maximum bandwidth
  - 3.3 V I/O with 5 V tolerance
- **ISA Bus Interface**
  - AT clock programmable
  - 8/16 bit ISA device with Zero-Wait-State
  - Generate refresh signals to ISA interface during DRAM refresh cycle
  - 3.3 V I/O with 5 V tolerance
- **Ethernet Controller**
  - Support two-port 10/100 Fast Ethernet MAC
  - IEEE 802.3u MII interface
  - IEEE 802.3x flow control in full-duplex mode
  - Descriptor architecture for packet TX/RX
- **IDE Controller**
  - Support 2 channels Ultra-DMA 100 (PATA x 4)
- **Universal Serial Bus**
  - USB 1.1/2.0 Host controller, supports 2 USB ports
  - Supports HS, FS and LS mode
- **LPC (Low Pin Count) Bus Interface**
  - Support 3 programmable registers to decode LPC address

- **FIFO UART Port**
  - Supports up to 5 COM ports
  - Compatible with 16C550/16C552
  - COM1 and COM2 support programmable TXD_EN
  - Supports the programmable baud rate generator with the data rate from 50 to 460.8 Kbps
  - The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
- **General Purpose I/O**
  - Up to 40 GPIO, supports 8 dedicated and 32 multi-functional GPIO
  - GPIO pins can be individually configured as inputs, outputs, or as interrupt trigger sources
  - Open-drain with a pull-high 75 KΩ
- **I2C Controller**
  - Compliant with V2.1
  - Supports standard, fast and high speed mode
  - Configurable for master and slave mode
- **SPI Interface**
  - Support SPI flash boot
- **Real Time Clock**
  - Internal RTC or External RTC
  - Under 2 uA power consumption on internal mode
- **JTAG Interface**
- **Speaker (Buzzer)**
- **Input Clock**
  - 4.318 MHz
  - 32.768 KHz
- **Output Clock**
  - 24 MHz
  - 25 MHz
  - 14.318 MHz
  - PCI clock
  - ISA clock
  - SDRAM clock
- **Configurable I/O Driving Current**
  - SDRAM, PCI, ISA, IDE, I2C, GPIO
- **Operating Voltage Range**
  - Core voltage: 1.8 V ± 5 %
  - Digital I / O voltage: 3.3 V ± 10 %
  - Analog I/O voltage: 3.3 V ± 5 %
- **Operating Temperature**
  - -20°C ~ 85°C
- **Package Type**
  - PBGA, 456 balls
  - Dimension: 27 mm x 27 mm x 2.23 mm
  - Lead-free, RoHS compliant

Chapter 3

Block Diagram

3.1 System Block Diagram
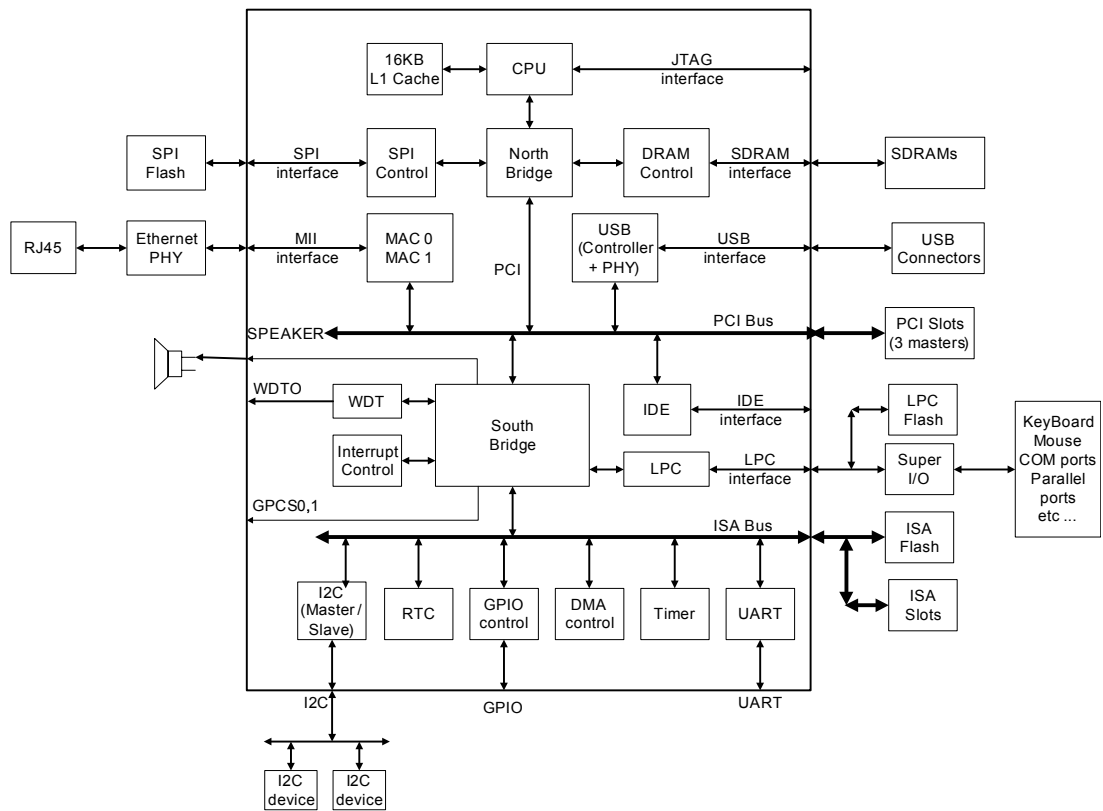
3.2 Functions Block Diagram
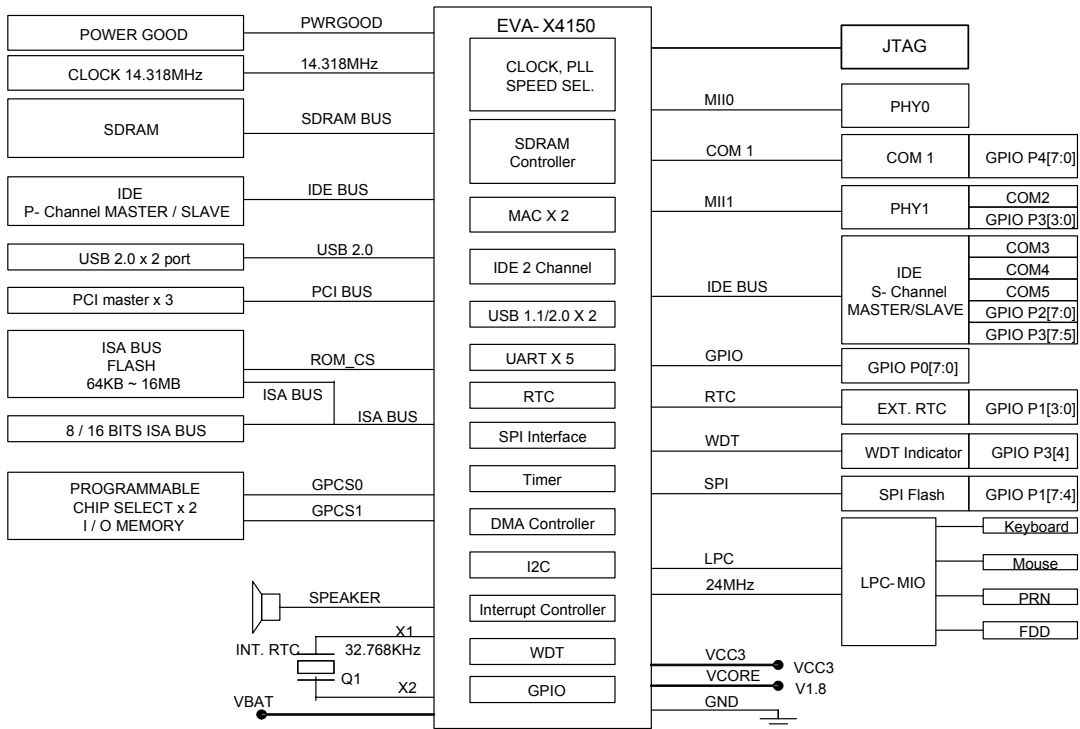
3.3 PCI Device List

Device#	0	1	2	3	4	5	6	7	8	9	10	11	12
ID Select	AD11	AD12	AD13	AD14		AD16		AD18		AD20	AD21	AD22	
Function 0	NB	MAC0	MAC1	USB OHCI		IDE		SB		Slot1	Slot2	Slot3	
Function 1				USB EHCI									

Chapter 4

PIN Function List

4.1 BGA Ball Map

Top View
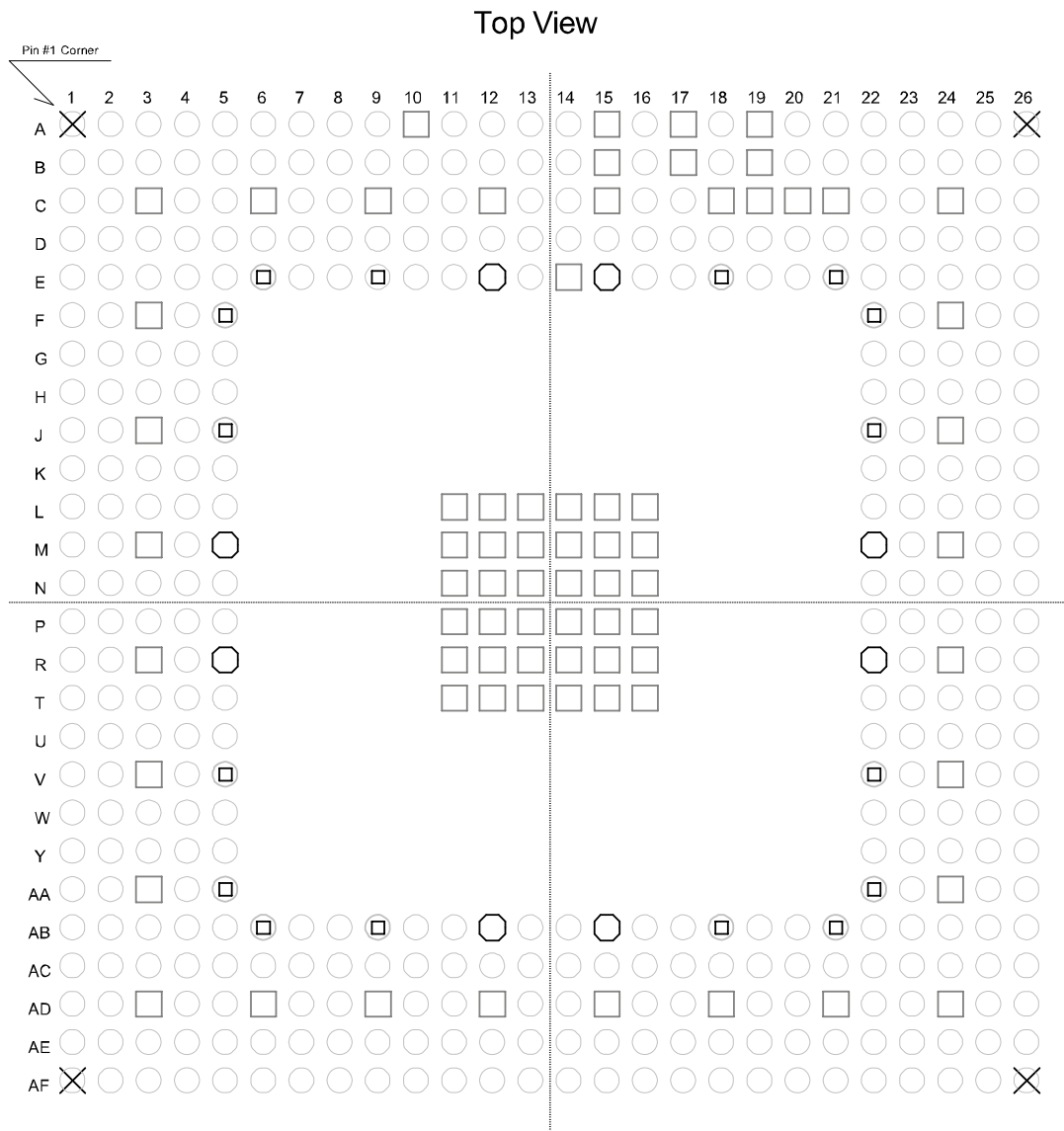
GND :A10,A15,A17,A19,B15,B17,B19,C3,C6,C9,C12,C15,C18,C19,C20,C21,C24,F3,F24,J3,J24,L11~L16,M3,M11~M16,M24
N11~N16,P11~P16,R3,R11~R16,R24,T11~T16,V3,V24,AA3,AA24,AD3,AD6,AD9,AD12,AD15,AD18,AD21,AD24,E14

1.8V Power: E12,E15,M5,M22,R5,R22,AB12,AB15

3.3V Power: E6,E9,E18,E21,F5,F22,J5,J22,V5,V22,AA5,AA22,AB6,AB9,AB18,AB21

N.C. Pin : A1,A26,AF1,AF26

Signal Pin :

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	TDO	TMS	SDA	GPIO_PORT0[4]	GPIO_PORT0[0]	LAD[3]	LAD[0]	CLK24MOUT	GND	Vss33_PLL	XIN_14318	Vss18_PLL
B	INTC_	TDI	TCK	SCL	GPIO_PORT0[5]	GPIO_PORT0[1]	LFRAME_	LAD[1]	RTC_AS/GPIO_PORT1[3]	CLK25MOUT	Vss18_PLL	XOUT_14318	Vss18_PLL
C	INTA_	INTD_	GND	WDTTI/GPIO_PORT3[4]	GPIO_PORT0[6]	GND	LDRQ_	LAD[2]	GND	PWR-GOOD	Vdd33_PLL	GND	Vdd18_PLL
D	GNT_[0]	REQ_[2]	REQ_[0]	INTB_	GPIO_PORT0[7]	GPIO_PORT0[3]	KBRST_	SERIRQ	RTC_WR_/GPIO_PORT1[1]	RTC_RD_/GPIO_PORT1[2]	Vdd33_PLL	Vss18_IO	Vdd18_PLL
E	PCICLK[0]	PCIRST_	GNT_[1]	GNT_[2]	GNT_[3]	3.3V POWER	GPIO_PORT0[2]	A20GATE_	3.3V POWER	IRQ8/GPIO_PORT1[0]	SPEAKER	1.8V POWER	Vdd18_IO
F	AD[30]	PCICLK[1]	GND	PCICLK[2]	3.3V POWER								
G	AD[27]	AD[26]	AD[28]	AD[29]	AD[31]								
H	AD[24]	AD[25]	CBE[3]	AD[23]	AD[22]								
J	AD[21]	AD[19]	GND	AD[20]	3.3V POWER								
K	AD[18]	AD[17]	AD[16]	CBE[2]	IRDY_								
L	FRAME_	TRDY_	DEVSEL_	STOP_	PAR						GND	GND	GND
M	CBE[1]	AD[15]	GND	AD[14]	1.8V POWER						GND	GND	GND
N	AD[13]	AD[12]	AD[11]	AD[10]	AD[9]						GND	GND	GND

	1	2	3	4	5	6	7	8	9	10	11	12	13
P	AD[8]	CBE[0]	AD[7]	AD[6]	AD[5]						GND	GND	GND
R	AD[4]	AD[3]	GND	AD[2]	1.8V POWER						GND	GND	GND
T	AD[1]	AD[0]	RTS3_/SRST	GPIO_PORT2[7]/SDD[7]	GPIO_PORT3[7]/SDD[10]						GND	GND	GND
U	GPIO_PORT3[5]/SDD[8]	GPIO_PORT2[6]/SDD[6]	GPIO_PORT3[6]/SDD[9]	GPIO_PORT2[5]/SDD[5]	SOUT3/SDD[12]								
V	GPIO_PORT2[4]/SDD[4]	SIN3/SDD[11]	GND	GPIO_PORT2[3]/SDD[3]	3.3V POWER								
W	GPIO_PORT2[2]/SDD[2]	SIN4/SDD[13]	GPIO_PORT2[1]/SDD[1]	SOUT4/SDD[14]	RI3_/SIORDY								
Y	GPIO_PORT2[0]/SDD[0]	SIN5/SDD[15]	DCD3_/SDRQ	CTS4_/SIOW	DSR3_/SCBLID								
AA	CTS3_/SIOR	DTR3_/SDACK	GND	RTS4_/SINT	3.3V POWER								
AB	RI4_/SA1	DCD4_/SA2	DTR4_/SA0	DSR4_/SCS1	PDD[9]	3.3V POWER	PIOR_	PCBLID	3.3V POWER	MD[1]	MD[4]	1.8V POWER	Vdd18_DLL
AC	SOUT5/SCS0	PRST	PDD[7]	PDD[5]	PDD[13]	PDRQ	PA[1]	PCS_[0]	MD[0]	MD[2]	MD[5]	MD[7]	Vss18_DLL
AD	PDD[6]	PDD[8]	GND	PDD[12]	PDD[0]	GND	PINT	SPI_DO/GPIO_PORT1[6]	GND	MD[3]	MD[6]	GND	DQM[1]
AE	PDD[10]	PDD[4]	PDD[11]	PDD[1]	PDD[15]	PIORDY	PA[0]	PCS_[1]	SPI_CS_/GPIO_PORT1[4]	MD[14]	MD[12]	MD[10]	MD[8]
AF	NC	PDD[3]	PDD[2]	PDD[14]	PIOW_	PDACK_	PA[2]	SPI_CLK/GPIO_PORT1[5]	SPI_DI/GPIO_PORT1[7]	MD[15]	MD[13]	MD[11]	MD[9]

	14	15	16	17	18	19	20	21	22	23	24	25	26	
	RTC_PS	GND	DM0	GND	DM1	GND	SE_DI	SE_CS	TXD0[1]	RXD0[3]	RXD0[0]	TXEN1/SOUT2	NC	A
	RTC_XOUT	GND	DP0	GND	DP1	GND	SE_DO	SE_CLK	TXD0[0]	RXDV0	RXC0	MDC	TXD1[2]/GPIO_PORT3[2]	B
	VBatGnd	GND	AVSS0	AVSSPLL	GND	GND	GND	GND	TXC0	RXD0[2]	GND	TXD1[3]/GPIO_PORT3[3]	TXD1[1]/GPIO_PORT3[1]	C
	VBat	RTC_XIN	AVDD0	AVDDPLL	AVSS1	AVDD1	TXEN0	TXD0[2]	TXD0[1]	MDIO	TXD1[0]/GPIO_PORT3[0]	TXC1/DCD2_	RXD1[2]/DTR2_	D
	GND	1.8V POWER	AVDD33	REXT	3.3V POWER	OVRCUR	TXD0[3]	3.3V POWER	COL0	RXDV1/RI2_	RXD1[3]/SIN2	RXD1[1]/DSR2_	RXD1[0]/CTS2_	E
									3.3V POWER	COL1/TXD_EN2	GND	TXD_EN1	DTR1_/GPIO_PORT4[5]	F
									RXC1/RTS2_	DCD1_/GPIO_PORT4[0]	DSR1_/GPIO_PORT[6]	CTS1_/GPIO_PORT4[7]	RTS1_/GPIO_PORT4[2]	G
									RI1_/GPIO_PORT4[3]	SOUT1/GPIO_PORT4[1]	SIN1/GPIO_PORT4[4]	ROMCS_	GPCS1_	H
									3.3V POWER	SD[15]	GND	SD[14]	SD[13]	J
									GPCS0	SD[12]	DACK_[7]	SD[11]	DRQ[6]	K
	GND	GND	GND						DRQ[7]	SD[10]	DACK_[6]	SD[9]	DRQ[5]	L
	GND	GND	GND						1.8V POWER	SD[8]	GND	DACK_[5]	MEMW_	M
	GND	GND	GND						DRQ[0]	MEMR_	DACK_[0]	LA[17]	IRQ[14]	N

	14	15	16	17	18	19	20	21	22	23	24	25	26	
	GND	GND	GND						LA[18]	IRQ[15]	LA[19]	IRQ[12]	LA[20]	P
	GND	GND	GND						1.8V POWER	IRQ[11]	GND	LA[21]	IRQ[10]	R
	GND	GND	GND						LA[22]	LA[23]	IOCS16_	MEMCS16_	SBHE_	T
									SA[0]	OSC14.318	SA[2]	SA[1]	BALE	U
									3.3V POWER	TC	GND	SA[4]	SA[3]	V
									IRQ[4]	IRQ[3]	SA[6]	DACK_[2]	SA[5]	W
									SA[10]	IRQ[7]	IRQ[5]	SA[8]	SA[7]	Y
									3.3V POWER	SA[11]	GND	IRQ[6]	SA[9]	AA
	Vdd18_DLL	1.8V POWER	CAS_	BA[1]	3.3V POWER	0WS_	SD[0]	3.3V POWER	SA[18]	DRQ[3]	SA[12]	REFRESH_	SYSCLK	AB
	Vss18_DLL	WE_	RAS_	MA[10]	MA[11]/Strap[11]	SD[5]	DRQ[2]	SD[2]	AEN	SMEMR_	SA[14]	DRQ[1]	SA[13]	AC
	CS_[1]	GND	CS_[0]	MA[0]/Strap[0]	GND	SD[7]	SD[6]	GND	SD[1]	SA[19]	GND	SA[15]	DACK_[1]	AD
	SDRAM-CLK	MA[9]	MA[7]/Strap[7]	MA[5]/Strap[5]	MA[1]/Strap[1]	MA[3]/Strap[3]	IOCHCK_	IRQ[9]	SD[3]	SMEMW_	IOW_	IOR_	DACK_[3]	AE
	DQM[0]	BA[0]	MA[8]/Strap[8]	MA[6]/Strap[6]	MA[4]/Strap[4]	MA[2]/Strap[2]	MA[12]	PSTDRV	SD[4]	IOCHRDY	SA[17]	SA[16]	NC	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

4.2 PIN-Out Table

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
A1	NC	E11	SPEAKER	P1	AD[8]	AB17	BA[1]
A2	TDO	E12	1.8 V POWER	P2	CBE[0]	AB18	3.3 V POWER
A3	TMS	E13	Vdd18_IO	P3	AD[7]	AB19	0WS_
A4	SDA	E14	GND	P4	AD[6]	AB20	SD[0]
A5	GPIO_PORT0[4]	E15	1.8 V POWER	P5	AD[5]	AB21	3.3 V POWER
A6	GPIO_PORT0[0]	E16	AVDD33	P11	GND	AB22	SA[18]
A7	LAD[3]	E17	REXT	P12	GND	AB23	DRQ[3]
A8	LAD[0]	E18	3.3 V POWER	P13	GND	AB24	SA[12]
A9	CLK24MOUT	E19	OVRCUR	P14	GND	AB25	REFRESH_
A10	GND	E20	TXD0[3]	P15	GND	AB26	SYSCLK
A11	Vss33_PLL	E21	3.3 V POWER	P16	GND	AC1	SOUT5/SCS0
A12	XIN_14318	E22	COL0	P22	LA[18]	AC2	PRST
A13	Vss18_PLL	E23	RXDV1/RI2_	P23	IRQ[15]	AC3	PDD[7]
A14	RTC_PS	E24	RXD1[3]/SIN2	P24	LA[19]	AC4	PDD[5]
A15	GND	E25	RXD1[1]/DSR2_	P25	IRQ[12]	AC5	PDD[13]
A16	DM0	E26	RXD1[0]/CTS2_	P26	LA[20]	AC6	PDRQ
A17	GND	F1	AD[30]	R1	AD[4]	AC7	PA[1]
A18	DM1	F2	PCICLK[1]	R2	AD[3]	AC8	PCS_[0]
A19	GND	F3	GND	R3	GND	AC9	MD[0]
A20	SE_DI	F4	PCICLK[2]	R4	AD[2]	AC10	MD[2]
A21	SE_CS	F5	3.3 V POWER	R5	1.8V POWER	AC11	MD[5]
A22	TXD0[1]	F22	3.3 V POWER	R11	GND	AC12	MD[7]
A23	RXD0[3]	F23	COL1/TXD_EN2	R12	GND	AC13	Vss18_DLL
A24	RXD0[0]	F24	GND	R13	GND	AC14	Vss18_DLL
A25	TXEN1/SOUT2	F25	TXD_EN1	R14	GND	AC15	WE_
A26	NC	F26	DTR1_/GPIO_PORT4[5]	R15	GND	AC16	RAS_
B1	INTC_	G1	AD[27]	R16	GND	AC17	MA[10]
B2	TDI	G2	AD[26]	R22	1.8V POWER	AC18	MA[11]/Strap[11]
B3	TCK	G3	AD[28]	R23	IRQ[11]	AC19	SD[5]
B4	SCL	G4	AD[29]	R24	GND	AC20	DRQ[2]
B5	GPIO_PORT0[5]	G5	AD[31]	R25	LA[21]	AC21	SD[2]
B6	GPIO_PORT0[1]	G22	RXC1/RTS2_	R26	IRQ[10]	AC22	AEN
B7	LFRAME_	G23	DCD1_/GPIO_PORT4[0]	T1	AD[1]	AC23	SMEMR_
B8	LAD[1]	G24	DSR1_/GPIO_PORT[6]	T2	AD[0]	AC24	SA[14]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
B9	RTC_AS/ GPIO_PORT1[3]	G25	CTS1_/ GPIO_PORT4[7]	T3	RTS3_/SRST	AC25	DRQ[1]
B10	CLK25MOUT	G26	RTS1_/ GPIO_PORT4[2]	T4	GPIO_PORT2[7]/SDD[7]	AC26	SA[13]
B11	Vss18_PLL	H1	AD[24]	T5	GPIO_PORT3[7]/SDD[10]	AD1	PDD[6]
B12	XOUT_14318	H2	AD[25]	T11	GND	AD2	PDD[8]
B13	Vss18_PLL	H3	CBE[3]	T12	GND	AD3	GND
B14	RTC_XOUT	H4	AD[23]	T13	GND	AD4	PDD[12]
B15	GND	H5	AD[22]	T14	GND	AD5	PDD[0]
B16	DP0	H22	RI1_/ GPIO_PORT4[3]	T15	GND	AD6	GND
B17	GND	H23	SOUT1/ GPIO_PORT4[1]	T16	GND	AD7	PINT
B18	DP1	H24	SIN1/ GPIO_PORT4[4]	T22	LA[22]	AD8	SPI_DO/ GPIO_PORT1[6]
B19	GND	H25	ROMCS_	T23	LA[23]	AD9	GND
B20	SE_DO	H26	GPCS1_	T24	IOCS16_	AD10	MD[3]
B21	SE_CLK	J1	AD[21]	T25	MEMCS16_	AD11	MD[6]
B22	TXD0[0]	J2	AD[19]	T26	SBHE_	AD12	GND
B23	RXDV0	J3	GND	U1	GPIO_PORT3[5]/SDD[8]	AD13	DQM[1]
B24	RXC0	J4	AD[20]	U2	GPIO_PORT2[6]/SDD[6]	AD14	CS_[1]
B25	MDC	J5	3.3 V POWER	U3	GPIO_PORT3[6]/SDD[9]	AD15	GND
B26	TXD1[2]/ GPIO_PORT3[2]	J22	3.3 V POWER	U4	GPIO_PORT2[5]/SDD[5]	AD16	CS_[0]
C1	INTA_	J23	SD[15]	U5	SOUT3/ SDD[12]	AD17	MA[0]/Strap[0]
C2	INTD_	J24	GND	U22	SA[0]	AD18	GND
C3	GND	J25	SD[14]	U23	OSC14.318	AD19	SD[7]
C4	WDTTI/ GPIO_PORT3[4]	J26	SD[13]	U24	SA[2]	AD20	SD[6]
C5	GPIO_PORT0[6]	K1	AD[18]	U25	SA[1]	AD21	GND
C6	GND	K2	AD[17]	U26	BALE	AD22	SD[1]
C7	LDRQ_	K3	AD[16]	V1	GPIO_PORT2[4]/SDD[4]	AD23	SA[19]
C8	LAD[2]	K4	CBE[2]	V2	SIN3/SDD[11]	AD24	GND
C9	GND	K5	IRDY_	V3	GND	AD25	SA[15]
C10	PWRGOOD	K22	GPCS0	V4	GPIO_PORT2[3]/SDD[3]	AD26	DACK_[1]
C11	Vdd33_PLL	K23	SD[12]	V5	3.3V POWER	AE1	PDD[10]
C12	GND	K24	DACK_[7]	V22	3.3V POWER	AE2	PDD[4]
C13	Vdd18_PLL	K25	SD[11]	V23	TC	AE3	PDD[11]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
C14	VBatGnd	K26	DRQ[6]	V24	GND	AE4	PDD[1]
C15	GND	L1	FRAME_	V25	SA[4]	AE5	PDD[15]
C16	AVSS0	L2	TRDY_	V26	SA[3]	AE6	PIORDY
C17	AVSSPLL	L3	DEVSEL_	W1	GPIO_PORT2[2]/SDD[2]	AE7	PA[0]
C18	GND	L4	STOP_	W2	SIN4/SDD[13]	AE8	PCS_[1]
C19	GND	L5	PAR	W3	GPIO_PORT2[1]/SDD[1]	AE9	SPI_CS_/GPIO_PORT1[4]
C20	GND	L11	GND	W4	SOUT4/SDD[14]	AE10	MD[14]
C21	GND	L12	GND	W5	RI3_/SIORDY	AE11	MD[12]
C22	TXC0	L13	GND	W22	IRQ[4]	AE12	MD[10]
C23	RXD0[2]	L14	GND	W23	IRQ[3]	AE13	MD[8]
C24	GND	L15	GND	W24	SA[6]	AE14	SDRAMCLK
C25	TXD1[3]/GPIO_PORT3[3]	L16	GND	W25	DACK_[2]	AE15	MA[9]
C26	TXD1[1]/GPIO_PORT3[1]	L22	DRQ[7]	W26	SA[5]	AE16	MA[7]/Strap[7]
D1	GNT_[0]	L23	SD[10]	Y1	GPIO_PORT2[0]/SDD[0]	AE17	MA[5]/Strap[5]
D2	REQ_[2]	L24	DACK_[6]	Y2	SIN5/SDD[15]	AE18	MA[1]/Strap[1]
D3	REQ_[0]	L25	SD[9]	Y3	DCD3_/SDRQ	AE19	MA[3]/Strap[3]
D4	INTB_	L26	DRQ[5]	Y4	CTS4_/SIOW	AE20	IOCHCK_
D5	GPIO_PORT0[7]	M1	CBE[1]	Y5	DSR3_/SCBLID	AE21	IRQ[9]
D6	GPIO_PORT0[3]	M2	AD[15]	Y22	SA[10]	AE22	SD[3]
D7	KBRST_	M3	GND	Y23	IRQ[7]	AE23	SMEMW_
D8	SERIRQ	M4	AD[14]	Y24	IRQ[5]	AE24	IOW_
D9	RTC_WR_/GPIO_PORT1[1]	M5	1.8V POWER	Y25	SA[8]	AE25	IOR_
D10	RTC_RD_/GPIO_PORT1[2]	M11	GND	Y26	SA[7]	AE26	DACK_[3]
D11	Vdd33_PLL	M12	GND	AA1	CTS3_/SIOR	AF1	NC
D12	Vss18_IO	M13	GND	AA2	DTR3_/SDACK	AF2	PDD[3]
D13	Vdd18_PLL	M14	GND	AA3	GND	AF3	PDD[2]
D14	VBat	M15	GND	AA4	RTS4_/SINT	AF4	PDD[14]
D15	RTC_XIN	M16	GND	AA5	3.3V POWER	AF5	PIOW_
D16	AVDD0	M22	1.8 V POWER	AA22	3.3 V POWER	AF6	PDACK_
D17	AVDDPLL	M23	SD[8]	AA23	SA[11]	AF7	PA[2]
D18	AVSS1	M24	GND	AA24	GND	AF8	SPI_CLK/GPIO_PORT1[5]
D19	AVDD1	M25	DACK_[5]	AA25	IRQ[6]	AF9	SPI_DI/GPIO_PORT1[7]
D20	TXEN0	M26	MEMW_	AA26	SA[9]	AF10	MD[15]
D21	TXD0[2]	N1	AD[13]	AB1	RI4_/SA1	AF11	MD[13]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
D22	TXD0[1]	N2	AD[12]	AB2	DCD4_/SA2	AF12	MD[11]
D23	MDIO	N3	AD[11]	AB3	DTR4_/SA0	AF13	MD[9]
D24	TXD1[0]/ GPIO_PORT3[0]	N4	AD[10]	AB4	DSR4_/SCS1	AF14	DQM[0]
D25	TXC1/DCD2_	N5	AD[9]	AB5	PDD[9]	AF15	BA[0]
D26	RXD1[2]/DTR2_	N11	GND	AB6	3.3 V POWER	AF16	MA[8]/Strap[8]
E1	PCICLK[0]	N12	GND	AB7	PIOR_	AF17	MA[6]/Strap[6]
E2	PCIRST_	N13	GND	AB8	PCBLID	AF18	MA[4]/Strap[4]
E3	GNT_[1]	N14	GND	AB9	3.3 V POWER	AF19	MA[2]/Strap[2]
E4	GNT_[2]	N15	GND	AB10	MD[1]	AF20	MA[12]
E5	GNT_[3]	N16	GND	AB11	MD[4]	AF21	PSTDRV
E6	3.3V POWER	N22	DRQ[0]	AB12	1.8V POWER	AF22	SD[4]
E7	GPIO_PORT0[2]	N23	MEMR_	AB13	Vdd18_DLL	AF23	IOCHRDY
E8	A20GATE_	N24	DACK_[0]	AB14	Vdd18_DLL	AF24	SA[17]
E9	3.3V POWER	N25	LA[17]	AB15	1.8V POWER	AF25	SA[16]
E10	IRQ8/ GPIO_PORT1[0]	N26	IRQ[14]	AB16	CAS_	AF26	NC

4.3 **Function Pin Table**

Function	Symbol	PIN Sum
SYSTEM	POWER_GOOD, XOUT_14318, XIN_14318, CLK25MOUT, CLK24MOUT, SPEAKER	6 PINs
SDRAM/Strap[11-0]	SDRAMCLK, RAS_ , CAS_, WE_, CS_[1-0], DQM[1-0], BA[1-0], MD[15-0], MA[12-0]	39 PINs
PCI	REQ_[2-0],GNT_[2-0],INTA_,INTB_,INTC_,INTD_, PCIRST_,PCICLK[2-0], AD[31-0],CBE[3-0],FRAME_, IRDY_, TRDY_, DEVSEL_, STOP_,PAR	56 PINs
SPI/ GPIO_PORT1[7-4]	SPI_CS_/GPIO_PORT1[4], SPI_CLK/GPIO_PORT1[5], SPI_DO/GPIO_PORT1[6], SPI_DI/GPIO_PORT1[7]	4 PINs
MII Interface MAC0	TXD0[3-0], TXC0, TXEN0, RXD0[3-0], RXC0, RXDV0, COL0, MDC, MDIO, SE_CS, SE_CLK, SE_DO, SE_DI	19 PINs
MAC1/ GPIO_PORT3[3-0], COM2	TXD1[3-0]/GPIO_PORT3[3-0], TXC1/DCD2_, TXEN1/SOUT2, RXC1/RTS2_, RXDV1/RI2_, RXD1[3]/SIN2, RXD1[2]/DTR2_, RXD1[1]/DSR2_, RXD1[0]/CTS2_, COL1/TXD_EN2	13 PINs
USB 2.0	OVRCUR, DP0, DP1, DM0, DM1, REXT	6 PINs
Primary ULTRA DMA IDE	PDD[15-0], PIORDY, PDRQ, PCBLID, PIOR_, PIOW_, PDACK_, PA[2-0], PCS_[1-0], PRST, PINT	29 PINs
Secondary ULTRA DMA IDE/ COM3,4,5, GPIO_PORT2[7-0], GPIO_PORT3[7-5]	GPIO_PORT2[7-0]/SDD[7-0],GPIO_PORT3[7-5]/SDD[10-8], SIN3/SDD[11], SOUT3/SDD[12], SIN4/SDD[13], SOUT4/SDD[14], SIN5/SDD[15], SOUT5/SCS0, RTS3_/SRST, DCD3_/SDRQ, CTS3_/SIOR, RI3_/SIORDY, DTR3_/SDACK, DSR3_/SCBLID, RTS4_/SINT, DCD4_/SA2, CTS4_/SIOW, RI4_/SA1, DTR4_/SA0, DSR4_/SCS1	29 PINs
ExtRTC/ GPIO_PORT1[3-0]	RTC_AS/GPIO_PORT1[3], RTC_RD_/GPIO_PORT1[2], RTC_WR/GPIO_PORT1[1], IRQ8/GPIO_PORT1[0]	4 PINs

Function	Symbol	PIN Sum
IntRTC	RTC_PS, RTC_XOUT, RTC_XIN	3 PINs
LPC	SERIRQ, LAD[3-0], LFRAME_, LDRQ_	7 PINs
GPIO_PORT0[7-0]	GPIO_PORT0[7-0]	8 PINs
JTAG	TDI, TMS, TCK, TDO	4 PINs
COM1/ GPIO_PORT4[7-0]	DCD1_/GPIO_PORT4[0],SOUT1/GPIO_PORT4[1], RTS1_/GPIO_PORT4[2], RI1_/GPIO_PORT4[3], SIN1/GPIO_PORT4[4], DTR1_/GPIO_PORT4[5], DSR1_/GPIO_PORT4[6], CTS1_/GPIO_PORT4[7], TXD_EN1	9 PINs
ISA BUS	IOCHCK_, SD[15-0], IOCHRDY, AEN, SA[16-0], SA[19-17], SBHE_, LA[23-17], MEMR_, MEMW_, RSTDRV, IRQ[15-14], IRQ[12-9], IRQ[7-3], DRQ[7-5], DRQ[3-0], 0WS_, SMEMR_, SMEMW_, IOW_, IOR_, DACK_[7-5], DACK_[3-0], REFRESH_, SYSCLK, TC, BALE, MEMCS16_,IOCS16_, OSC14.318	87 PINs
NOR FLASH	ROMCS_	1 PIN
GPCS	GPCS0_, GPCS1_	2 PINs
KB	KBRST_, A20GATE_	2 PINs
I2C	SDA, SCL	2 PINs
WDT Timeout Indi-cator/ GPIO_PORT3[4]	WDTTI/GPIO_PORT3[4]	1 PIN
Battery Power	VBat, VBatGnd	2 PINs
1.8 V POWER	Vdd18_PLL:2 PINs, Vss18_PLL:2 PINs, Vdd18_DLL:2 PINs, Vss18_DLL:2 PINs, Vdd18_IO, Vss18_IO, AVDDPLL, AVSSPLL, AVDD0, AVSS0, AVDD1, AVSS1	16 PINs
1.8 V core POWER	Vdd_core: 8 PINs	8 PINs
3.3 V POWER	Vdd33_PLL:2 PINs, Vss33_PLL:2 PINs, AVDD33	5 PINs
3.3 V IO POWER	Vdd_IO : 16 PINs	16 PINs
1.8 V core and 3.3 V IO Ground	Vss:74 PINs	74 PINs

4.4 Signal Description

This chapter provides a detailed description of EVA-X4150 signals. A signal with the symbol "_" at the end of itself indicates that this pin is low active. Otherwise, it is high active.

The following notations are used to describe the signal types:

I   Input pin

O   Output pin

OD   Output pin with open-drain

I/OD   Bi-directional Input/Output pin with open-drain

I/O   Bi-directional Input/Output pin

■ System (6 PINs)

PIN No.	Symbol	Type	Description
C10	PWRGOOD	I	**Power-Good Input.** This signal comes from Power Good of the power supply to indicate that the power is available. The EVA-X4150 uses this signal to generate reset sequence for the system.
B12	XOUT_14318	O	**Crystal-out**. Frequency output from the inverting amplifier (oscillator).
A12	XIN_14318	I	**Crystal-in.** 14.318MHz frequency input, within 30 ppm tolerance, to the amplifier (oscillator).
B10	CLK25MOUT	O	25 MHz Clock output.
A9	CLK24MOUT	O	24 MHz Clock output.
E11	SPEAKER	O	**Speaker Output.** This pin is used to control the Speaker Output and should be connected to the Speaker.

■ SDRAM Interface (39 PINs)

PIN No.	Symbol	Type	Description
AE14	SDRAM-CLK	O	**Clock output.** This pin provides the fundamental timing for SDRAM.
AC16	RAS_	O	**Row Address Strobe.** When asserted, this signal latches row address on positive edge of the SDRAM clock. This signal also allows row access and pre-charge.
AB16	CAS_	O	**Column Address Strobe.** When asserted, this signal latches column address on the positive edge of the SDRAM clock. This signal also allows column access and pre-charge.
AC15	WE_	O	**Memory Write Enable.** This pin is used as a write enable for the memory data bus.
AD14;AD16	CS_[1-0]	O	**Chip Select.** This pin activates the SDRAM devices.
AD13;AF14	DQM[1-0]	O	**Data Mask DQM[1-0].** These pins act as synchronized output enables during read cycles and byte masks during write cycles.
AB17;AF15	BA[1-0]	O	**Bank Address BA[1-0].** These pins are connected to SDRAM as bank address pins.
AF10;AE10;AF11; AE11;AF12;AE12; AF13;AE13;AC12; AD11;AC11;AB11; AD10;AC10;AB10; AC9	MD[15-0]	I/O	**Memory Data MD[15-0].** These pins are connected to the SDRAM data bus.
AF19;AE18; AD17	MA[2-0]/ Strap[2-0]	I/O	Memory Address MA[2-0]. Normally, these pins are used as the row and column address for SDRAM. Strap[2-0]: CPU/SDRAM clock 0 0 0 66 Mhz 0 0 1 100 Mhz 0 1 0 133 Mhz (default) 0 1 1 150 Mhz 1 0 0 166 Mhz
AE19	MA[3]/ Strap[3]	I/O	Memory Address MA[3]. Normally, these pins are used as the row and column address for SDRAM. Strap[3]: PLL_TEST_OUT_EN Pull it high to enable PLL_TEST_OUT_EN. Pull it low to disable PLL_TEST_OUT_EN. (default)

PIN No.	Symbol	Type	Description
AF18	MA[4]/ Strap[4]	I/O	Memory Address MA[4]. Normally, these pins are used as the row and column address for SDRAM. Strap[4]: MAC1 enable Pull it high to enable MAC1 function. Pull it low to enable COM2 + GPIO_PORT3[3-0]. (default)
AE17	MA[5]/ Strap[5]	I/O	Memory Address MA[5]. Normally, these pins are used as the row and column address for SDRAM. Strap[5]: Secondary IDE enable Pull it high to enable Secondary IDE function. (default) Pull it low to enable COM3/4/5 + GPIO_PORT2[7-0]+GPIO_PORT3[7-5].
AE16;AF17	MA[7-6]/ Strap[7-6]	I/O	Memory Address MA[7-6]. Normally, these pins are used as the row and column address for SDRAM. Strap[7-6]: Boot Flash select 00 : flash-8bits 01 : flash-16bits 10 : LPC flash (default) 11 : SPI flash
AF16	MA[8]/ Strap[8]	I/O	Memory Address MA[8]. Normally, these pins are used as the row and column address for SDRAM. Strap[8]: JTAG enable Pull it high to enable JTAG. (default) Pull it low to disable JTAG.
AC17;AE15	MA[10-9]	I/O	Memory Address MA[10-9]. Normally, these pins are used as the row and column address for SDRAM.
AC18	MA[11]/ Strap[11]	I/O	Memory Address MA[11]. Normally, these pins are used as the row and column address for SDRAM. Strap[11]: Internal/external RTC select Pulled high is External RTC. Pulled low is Internal RTC. (default)
AF20	MA[12]	I/O	Memory Address MA[12]. Normally, these pins are used as the row and column address for SDRAM.

■ **PCI Bus Interface (56 PINs)**

PIN No.	Symbol	Type	Description
D2; E5;D3	REQ_[2-0]	I	**PCI Bus Request.** These signals are the PCI bus request signals used as inputs by the internal PCI arbiter.
E4; E3;D1	GNT_[2-0]	O	**PCI Grant.** These signals are the PCI bus grant output signals generated by the internal PCI arbiter.
C1	INTA_	I	**PCI INTA_.** PCI interrupt input A. It connects to PCI INTA_ when normal modes of PCI Interrupts are supported.
D4	INTB_	I	**PCI INTB_.** PCI interrupt input B. It connects to PCI INTB_ when normal modes of PCI Interrupts are supported.
B1	INTC_	I	**PCI INTC_.** PCI interrupt input C. It connects to PCI INTC_ when normal modes of PCI Interrupts are supported.
C2	INTD_	I	**PCI INTD_.** PCI interrupt input D. It connects to PCI INTD_ when normal modes of PCI Interrupts are supported.

PIN No.	Symbol	Type	Description
E2	PCIRST_	O	**PCI Reset.** This pin is used to reset PCI devices. When it is asserted low, all the PCI devices will be reset.
F4; F2;E1	PCI-CLK[2-0]	O	**PCI Clock Output.** This clock is used by all of the EVA-X4150 logic that is in the PCI clock domain.
G5;F1;G4;G3;G1; G2;H2;H1;H4;H5; J1;J4;J2;K1;K2; K3;M2;M4;N1;N2; N3;N4;N5;P1;P3; P4;P5;R1;R2;R4; T1;T2	AD[31-0]	I/O	**PCI Address and Data.** The standard PCI address and data lines. The address is driven with PCI Frame assertion and data is driven or received in the following clocks.
H3;K4;M1;P2	CBE[3-0]	I/O	**Bus Command and Byte Enables.** During the address phase, CBE[3-0] define the Bus Command. During the data phase, CBE[3-0] define the Byte Enables.
L1	FRAME_	I/O	**PCI Frame.** This pin is driven by a PCI master to indicate the beginning and duration of a PCI transaction.
K5	IRDY_	I/O	**PCI Initiator Ready.** This pin is asserted low by the master to indicate that it is able to transfer the current data transfer. A data was transferred if both IRDY_ and TRDY_ are asserted low during the rising edge of the PCI clock.
L2	TRDY_	I/O	**PCI Target Ready.** This pin is asserted low by the target to indicate that it is able to receive the current data transfer. A data was transferred if both IRDY_ and TRDY_ are asserted low during the rising edge of the PCI clock.
L3	DEVSEL_	I/O	**Device Select.** This pin is driven by the devices which have decoded the addresses belonging to them.
L4	STOP_	I/O	**PCI Stop.** This pin is asserted low by the target to indicate that it is unable to receive the current data transfer.
L5	PAR	I/O	**PCI Parity.** This pin is driven to even parity by PCI master over the AD[31-0] and CBE[3-0] bus during address and write data phases. It should be pulled high through a weak external pull-up resistor. The target drives parity during data read.

■ **SPI / GPIO_PORT1[7-4] Interface (4 PINs)**

PIN No.	Symbol	Type	Description
AE9	SPI_CS_/ GPIO_PORT1[4]	I/OD	SPI Chip Select General-Purpose Input / Output GPIO_PORT1[4]
AF8	SPI_CLK/ GPIO_PORT1[5]	I/OD	SPI Clock General-Purpose Input / Output GPIO_PORT1[5]
AD8	SPI_DO/ GPIO_PORT1[6]	I/OD	SPI Data Output General-Purpose Input / Output GPIO_PORT1[6]
AF9	SPI_DI/ GPIO_PORT1[7]	I/OD	SPI Data Input General-Purpose Input / Output GPIO_PORT1[7]

■   **MII Interface, MAC0 (19 PINs)**

PIN No.	Symbol	Type	Description
E20; D21; A22;B22	TXD0[3-0]	I/O	**TXD0[3-0]:** Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal.
C22	TXC0	I/O	**TXC0:** Supports the transmit clock supplied by the external PMD device. This clock should always be active.
D20	TXEN0	I/O	**TXEN0:** This pin functions as Transmit Enable. It indicates that a transmission to an external PHY device is active on the MII port.
A23; C23; D22; A24	RXD0[3-0]	I/O	**RXD0[3-0]:** Four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal.
B24	RXC0	I/O	**RXC0:** Supports the receive clock supplied by the external PMD device. This clock should always be active.
B23	RXDV0	I/O	**RXDV0:** Data valid is asserted by an external PHY when the received data is present on the RXD[3-0] lines and is de-asserted at the end of the packet. This signal should be synchronized with the RXC signal.
E22	COL0	I/O	**COL0:** This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
B25	MDC	I/O	**MDC:** MII management data clock is sourced by the R3210 to the external PHY devices as a timing reference for the transfer of information on the MDIO signal.
D23	MDIO	I/O	**MDIO:** MII management data input/output transfers control information and status between the external PHY and the EVA-X4150.
A21	SE_CS	O	SE_CS: Serial EEPROM Chip Select
B21	SE_CLK	O	SE_CLK: Serial EEPROM Clock
B20	SE_DO	O	SE_DO: Serial EEPROM Data Output
A20	SE_DI	I	SE_DI: Serial EEPROM Data In

■ **MAC 1 / GPIO_PORT3[3-0], COM2 (13 PINs)**

PIN No.	Symbol	Type	Description
C25; B26; C26;D24	TXD1[3-0] / GPIO_POR T3[3-0]	I/OD	**TXD1[3-0]:** Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal. **General-Purpose Input/Output GPIO_PORT3[3-0].** Those pins can be programmed input or output individually.
D25	TXC1 / DCD2_	I/O	**TXC1:** Supports the transmit clock supplied by the external PMD device. This clock should always be active. **Data Carrier Detect.** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_ signal by reading bit 7 of the Modem Status Register (MSR). A DCD_ signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD_ changes state. **Note:** Bit 7 of the MSR is the complement of DCD_.
A25	TXEN1 / SOUT2	I/O	**TXEN1:** This pin functions as Transmit Enable. It indicates that a transmission to an external PHY device is active on the MII port. **Transmit Data.** FIFO UART transmitter serial data output from the serial port.
G22	RXC1 / RTS2_	I/O	**RXC1:** Supports the receive clock supplied by the external PMD device. This clock should always be active. **Request to Send.** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_ signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
E23	RXDV1/ RI2_	I/O	**RXDV1:** Data valid is asserted by an external PHY when the received data is present on the RXD[3-0] lines and is de-asserted at the end of the packet. This signal should be synchronized with the RXC signal. **Ring Indicator.** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_ signal by reading bit 6 of the Modem Status Register (MSR). An RI_ signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_ changes state. **Note:** Bit 6 of the MSR is the complement of RI_.
E24	RXD1 [3]/SIN2	I/O	**RXD1[3]:** One of the four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal. **Receive Data.** FIFO UART receiver serial data input signal.

PIN No.	Symbol	Type	Description
D26	RXD1 [2]/DTR2_	I/O	**RXD1[2]:** One of the four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal. **Data Terminal Ready.** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_ signal to be inactive during the loop-mode operation.
E25	RXD1 [1]/DSR2_	I/O	**RXD1[1]:** One of the four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal. **Data Set Ready.** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_ signal by reading bit5 of the Modem Status Register (MSR). A DSR_ signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_ changes state. **Note:** Bit 5 of the MSR is the complement of DSR_.
E26	RXD1[0]/ CTS2_	I/O	**RXD1[0]:** One of the four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal. **Clear to Send.** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_ signal by reading bit 4 of Modem Status Register (MSR). A CTS_ signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_ changes the state. The CTS_ signal has no effect on the transmitter. **Note:** Bit 4 of the MSR is the complement of CTS_.
F23	COL1/ TXD_EN2	I/O	**COL1:** This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin. **COM2 TX Status.** This pin will be high when COM2 is transmitting.

■ USB Interface (6 PINs)

PIN No.	Symbol	Type	Description
E19	OVRCUR	I	Over Current Detect for USB Host Controller. This pin is used to monitor USB Power Over Current Status.
B16; A16	DP0 DM0	I/O	Universal Serial Bus Controller Port 0. These are the serial data pair for USB Port 0. Internal already has 15 KΩ pull down.
B18; A18	DP1 DM1	I/O	Universal Serial Bus Controller 0 Port 1. These are the serial data pair for USB Port 1. Internal already has 15 KΩ pull down.
E17	REXT	I	Universal Serial Bus Controller External Reference Resistance. 510 Ω ±5%

■ Primary IDE (29 PINs)

PIN No.	Symbol	Type	Description
AE5; AF4; AC5; AD4; AE3; AE1; AB5; AD2; AC3; AD1; AC4; AE2; AF2; AF3; AE4; AD5	PDD[15-0]	I/O	IDE Primary Channel Data Bus.
AE6	PIORDY	I	IDE Primary Channel IO Channel Ready.
AC6	PDRQ	I	IDE Primary Channel DMA Request.
AB8	PCBLID	I	IDE Primary Channel Cable Assembly Type Identifier.
AB7	PIOR_	O	IDE Primary Channel IO Read Strobe.
AF5	PIOW_	O	IDE Primary Channel IO Write Strobe.
AF6	PDACK_	O	IDE Primary Channel DMA Acknowledge.
AF7; AC7;AE7	PA[2-0]	O	IDE Primary Channel Device Address
AE8; AC8	PCS_[1-0]	O	IDE Primary Channel Chip Select.
AC2	PRST	O	IDE Primary Channel Reset.
AD7	PINT	I	IDE Primary Channel Interrupt.

■ Secondary IDE / COM 3~5, GPIO_PORT2[7-0], GPIO_PORT3[7-5] (29 PINs)

PIN No.	Symbol	Type	Description
T4;U2;U4;V1;V4;W1;W3;Y1	GPIO_PORT2[7-0] / SDD[7-0]	I/OD	**General-Purpose Input/Output GPIO_PORT2[7-0].** Those pins can be programmed input or output individually. IDE Secondary Channel Data Bus.
T5; U3; U1	GPIO_PORT3[7-5] / SDD[10-8]	I/OD	**General-Purpose Input/Output GPIO_PORT3[7-5].** Those pins can be programmed input or output individually. IDE Secondary Channel Data Bus.
V2	SIN3 / SDD[11]	I/O	**Receive Data.** FIFO UART receiver serial data input signal. IDE Secondary Channel Data Bus.
U5	SOUT3 / SDD[12]	I/O	**Transmit Data.** FIFO UART transmitter serial data output from the serial port. IDE Secondary Channel Data Bus.
W2	SIN4 / SDD[13]	I/O	**Receive Data.** FIFO UART receiver serial data input signal. IDE Secondary Channel Data Bus.

PIN No.	Symbol	Type	Description
W4	SOUT4 / SDD[14]	I/O	**Transmit Data.** FIFO UART transmitter serial data output from the serial port. IDE Secondary Channel Data Bus.
Y2	SIN5 / SDD[15]	I/O	**Receive Data.** FIFO UART receiver serial data input signal. IDE Secondary Channel Data Bus.
AC1	SOUT5 / SCS0	I/O	**Transmit Data.** FIFO UART transmitter serial data output from the serial port. IDE Secondary Channel Chip Select.
T3	RTS3_ / SRST	O	**Request to Send.** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_ signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation. IDE Secondary Channel Reset.
Y3	DCD3_ / SDRQ	I	**Data Carrier Detect.** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_ signal by reading bit 7 of the Modem Status Register (MSR). A DCD_ signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD_ changes state. **Note:** Bit 7 of the MSR is the complement of DCD_. IDE Secondary Channel DMA Request.
AA1	CTS3_ / SIOR	I/O	**Clear to Send.** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_ signal by reading bit 4 of Modem Status Register (MSR). A CTS_ signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_ changes the state. The _ signal has no effect on the transmitter. **Note:** Bit 4 of the MSR is the complement of CTS_. IDE Secondary Channel IO Read Strobe.
W5	RI3_ / SIORDY	I	**Ring Indicator.** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_ signal by reading bit 6 of the Modem Status Register (MSR). An RI_ signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_ changes state. **Note:** Bit 6 of the MSR is the complement of RI_. IDE Secondary Channel IO Channel Ready.

PIN No.	Symbol	Type	Description
AA2	DTR3_ / SDACK	O	**Data Terminal Ready.** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_ signal to be inactive during the loop-mode operation. IDE Secondary Channel DMA Acknowledge.
Y5	DSR3_ / SCBLID	I	**Data Set Ready.** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_ signal by reading bit5 of the Modem Status Register (MSR). A DSR_ signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_ changes state. **Note:** Bit 5 of the MSR is the complement of DSR_. IDE Secondary Channel Cable Assembly Type Identifier.
AA4	RTS4_ / SINT	I/O	**Request to Send.** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_ signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation. IDE Secondary Channel Interrupt.
AB2	DCD4_ / SA2	I/O	**Data Carrier Detect.** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_ signal by reading bit 7 of the Modem Status Register (MSR). A DCD_ signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD_ changes state. **Note:** Bit 7 of the MSR is the complement of DCD_. IDE Secondary Channel Device Address.
Y4	CTS4_ / SIOW	I/O	**Clear to Send.** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_ signal by reading bit 4 of Modem Status Register (MSR). A CTS_ signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_ changes the state. The CTS_ signal has no effect on the transmitter. **Note:** Bit 4 of the MSR is the complement of CTS_. IDE Secondary Channel IO Write Strobe.

PIN No.	Symbol	Type	Description
AB1	RI4_ / SA1	I/O	**Ring Indicator.** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_ signal by reading bit 6 of the Modem Status Register (MSR). An RI_ signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_ changes state. **Note:** Bit 6 of the MSR is the complement of RI_. IDE Secondary Channel Device Address.
AB3	DTR4_ / SA0	O	**Data Terminal Ready.** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_ signal to be inactive during the loop-mode operation. IDE Secondary Channel Device Address.
AB4	DSR4_ / SCS1	I/O	**Data Set Ready.** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_ signal by reading bit5 of the Modem Status Register (MSR). A DSR_ signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_ changes state. **Note:** Bit 5 of the MSR is the complement of DSR_. IDE Secondary Channel Chip Select.

■   **ExtRTC / GPIO_PORT1[3-0] Interface (4 PINs)**

PIN No.	Symbol	Type	Description
B9	RTC_AS / GPIO_PORT1[3]	I/OD	**RTC Address Strobe.** This pin is used as the RTC Address Strobe and should be connected to the RTC. General-Purpose Input/Output GPIO_PORT1[3].
D10	RTC_RD_/ GPIO_PORT1[2]	I/OD	**RTC Read Command.** This pin is used as the RTC Read Command and should be connected to the RTC. General-Purpose Input/Output GPIO_PORT1[2].
D9	RTC_WR_/ GPIO_PORT1[1]	I/OD	**RTC Write Command.** This pin is used as the RTC Write Command and should be connected to the RTC. General-Purpose Input/Output GPIO_PORT1[1].
E10	IRQ8 / GPIO_PORT1[0]	I/OD	**RTC Interrupt Input.** This pin is used as the RTC Interrupt input. General-Purpose Input/Output GPIO_PORT1[0].

■   **IntRTC (3 PINs)**

PIN No.	Symbol	Type	Description
A14	RTC_PS	I	RTC Battery Power Sense.
D15	RTC_XIN	I	**Crystal-in.** 32.768KHz frequency input.
B14	RTC_XOUT	O	**Crystal-out**. Frequency output from the inverting amplifier (oscillator).

■ **LPC Bus Interface (7 PINs)**

PIN No.	Symbol	Type	Description
D8	SERIRQ	I/ O	**Serial Interrupt Request.** This pin is used to support the serial interrupt protocol of common architecture. Internal Pull Up.
A7; C8; B8; A8	LAD[3-0]	I/ O	**LPC Command, Address and Data LAD[3-0].** These pins are used to be command/address/data pins of Low-Pin-Count Function. Internal Pull Up.
B7	LFRAME_	O	**Low Pin Count FRAME_ Signal.** This signal is used as a frame signal of low pin count protocol.
C7	LDRQ_	I	**Low Pin Count DMA Request Signal.** This signal is used as a DMA request signal of low pin count protocol. Internal Pull Up.

■ **GPIO_PORT0[7-0] (8 PINs)**

PIN No.	Symbol	Type	Description
D5; C5; A5; D6; E7; B6; A6	GPIO_PORT0[7-0]	I/OD	General-Purpose Input/Output GPIO_PORT0[7-0]. Those pins can be programmed input or output individually. Open drain, Internal pull high 75 kΩ.

■ **JTAG Interface (4 PINs)**

PIN No.	Symbol	Type	Description
B2	TDI	I	**TDI:** JTAG Test Data Input pin.
A3	TMS	I	**TMS:** JTAG Test Mode Select pin.
B3	TCK	I	**TCK:** JTAG Test Clock Input pin.
A2	TDO	O	**TDO:** JTAG Test Data Output pin.

■ **COM1 / GPIO_PORT4[7-0] (9 PINs)**

PIN No.	Symbol	Type	Description
G23	DCD1_/ GPIO_PORT4[0]	I / OD	**Data Carrier Detect.** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD_ signal by reading bit 7 of the Modem Status Register (MSR). A DCD_ signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD_ changes state. **Note:** Bit 7 of the MSR is the complement of DCD_. General-Purpose Input/Output GPIO_PORT4[0].
H23	SOUT1/ GPIO_PORT4[1]	I / OD	**Transmit Data.** FIFO UART transmitter serial data output from the serial port. General-Purpose Input/Output GPIO_PORT4 [1].

PIN No.	Symbol	Type	Description
G26	RTS1_/ GPIO_PORT4[2]	I / OD	**Request to Send.** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS_ signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation. General-Purpose Input/Output GPIO_PORT4[2].
H22	RI1_/ GPIO_PORT4[3]	I / OD	**Ring Indicator.** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI_ signal by reading bit 6 of the Modem Status Register (MSR). An RI_ signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI_ changes state. **Note:** Bit 6 of the MSR is the complement of RI_. General-Purpose Input/Output GPIO_PORT4 [3].
H24	SIN1/ GPIO_PORT4[4]	I / OD	**Receive Data.** FIFO UART receiver serial data input signal. General-Purpose Input/Output GPIO_PORT4 [4].
F26	DTR1_/ GPIO_PORT4[5]	I / OD	**Data Terminal Ready.** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR_ signal to be inactive during the loop-mode operation. General-Purpose Input/Output GPIO_PORT4[5].
G24	DSR1_/ GPIO_PORT4[6]	I / OD	**Data Set Ready.** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR_ signal by reading bit5 of the Modem Status Register (MSR). A DSR_ signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR_ changes state. **Note:** Bit 5 of the MSR is the complement of DSR_. General-Purpose Input/ Output GPIO_PORT4 [6].
G25	CTS1_/ GPIO_PORT4[7]	I / OD	**Clear to Send.** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS_ signal by reading bit 4 of Modem Status Register (MSR). A CTS_ signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS_ changes the state. The CTS_ signal has no effect on the transmitter. **Note:** Bit 4 of the MSR is the complement of CTS_. General-Purpose Input/Output GPIO_PORT4 [7].

PIN No.	Symbol	Type	Description
F25	TXD_EN1	I/O	**COM1 TX Status.** This pin will be active when COM1 is transmitting.

■ **ISA Bus Interface (87 PINs)**

PIN No.	Symbol	Type	Description
AE20	IOCHCK_	I	**I/O Channel Check**. Provides the system board with parity (error) information about memory or devices on the I/O channel.
J23; J25; J26; K23; K25; L23; L25; M23; AD19; AD20; AC19; AF22; AE22; AC21; AD22; AB20	SD[15-0]	I/O	**ISA high and low byte slot data bus**. These are the system data lines. These signals read data and vectors into CPU during memory or I/O read cycles or interrupt acknowledge cycles and outputs data from CPU during memory or I/O write cycles.
AF23	IOCHRDY	I	**ISA system ready**. This input signal is used to extend the ISA command width for the CPU and DMA cycles.
AC22	AEN	O	**ISA address enable**. This active high output indicates that the system address is enabled during the DMA refresh cycles.
AF25; AD25; AC24; AC26; AB24; AA23; Y22; AA26; Y25; Y26; W24; W26; V25; V26; U24; U25;U22	SA[16-0]	O	**ISA slot address bus.** These signals are high impedance during hold acknowledge.
AD23; AB22; AF24	SA[19-17]	O	ISA slot address bus for 62-pin slot.
T26	SBHE_	O	**ISA Bus high enable.** In master cycle, it is an input polarity signal and is driven by the master device.
T23;T22; R25; P26; P24; P22; N25	LA[23-17]	O	**ISA latched address bus**. These are input signal during ISA master cycle.
N23	MEMR_	O	**ISA memory read**. This signal is an input during ISA master cycle.
M26	MEMW_	O	**ISA memory write**. This signal is an input during ISA master cycle.
AF21	RSTDRV	O	**Driver Reset**. This output signal is driven active during system power up.
Y23; AA25; Y24; W22; W23; P25; R23; R26; AE21; P23; N26	IRQ[7-3], IRQ[12-9], IRQ[15-14]	I	**Interrupt request signals**. These are interrupt request input signals.
L22; K26; L26; AB23; AC20; AC25; N22	DRQ[7-5], DRQ[3-0]	I	**DMA device request**. These are DMA request input signals.
AB19	0WS_	I	**ISA zero wait state**. This is the ISA device zero-wait state indicator signal. This signal terminates the CPU ISA command immediately.

PIN No.	Symbol	Type	Description
AC23	SMEMR_	O	**ISA system memory read**. This signal indicates that the memory read cycle is for an address below 1 M byte address.
AE23	SMEMW_	O	**ISA system memory write**. This signal indicates that the memory write cycle is for an address below 1 M byte address.
AE24	IOW_	O	**ISA I/O write**. This signal is an input during ISA master cycle.
AE25	IOR_	O	**ISA I/O read**. This signal is an input during ISA master cycle.
K24; L24; M25; AE26; W25; AD26; N24	DACK_[7-5], DACK_[3-0]	O	**DMA device acknowledge signals**. These are DMA acknowledge demultiplex select signals. Input function is for hardware setting.
AB25	REFRESH_	O	**Refresh cycle indicator**. ISA master uses this signal to notify DRAM needs refresh. During the memory controller's self-acting refresh cycle, M6117D drives this signal to the I/O channels.
AB26	SYSCLK	O	**System Clock Output**. This signal clocks the ISA bus.
V23	TC	O	**DMA end of process**. This is the DMA channel terminal count indicating signal.
U26	BALE	O	**Bus address latch enable**. BALE indicates the presence of a valid address at I/O slots.
T25	MEMCS16_	I	ISA 16-bit memory device select indicator signal.
T24	IOCS16_	I	ISA 16-bit I/O device select indicator signal.
U23	OSC14.318	O	14.318 MHz clock out.

■ **NOR Flash Interface (1 PIN)**

PIN No.	Symbol	Type	Description
H25	ROMCS_	O	**ROM Chip Select.** This pin is used as a ROM chip select.

■ **GPCS Interface (2 PINs)**

PIN No.	Symbol	Type	Description
K22	GPCS0_	O	**ISA Bus Chip Select 0**. This pin is the chip select for ISA bus.
H26	GPCS1_	O	**ISA Bus Chip Select 1**. This pin is the chip select for ISA bus.

■ **KB Interface (2 PINs)**

PIN No.	Symbol	Type	Description
D7	KBRST_	I/O	**Keyboard Reset**. This pin is Keyboard reset when used external 8042.
E8	A20GATE_	I/O	**Address Bit 20 Mask**. This pin is A20 mask when used external 8042.

■ **I2C Interface (2 PINs)**

PIN No.	Symbol	Type	Description
A4	SDA	I/O	I²C serial data
B4	SCL	I/O	I²C serial clock

■ **WDT Timeout Indicator / GPIO_PORT3[4] (1 PINs)**

PIN No.	Symbol	Type	Description
C4	WDTTI / GPIO_PORT3[4]	I/OD	Watch Dog Timer out indicator. General-Purpose Input/Output GPIO_PORT3[4].

■ **IntRTC Battery POWER (2 PINs)**

PIN No.	Symbol	Type	Description
D14	VBat	I	Battery Power for RTC. Voltage : 2.2 ~ 3.3 V
C14	VBatGnd	I	Battery Ground for RTC.

■ **1.8 V Power (16 PINs)**

PIN No.	Symbol	Type	Description
C13;D13	Vdd18_PLL	I	CPU PLL power: 2 PINs
A13;B13	Vss18_PLL	I	CPU PLL Ground: 2 PINs
AB13;AB14	Vdd18_DLL	I	SDRAM DLL power: 2 PINs
AC13;AC14	Vss18_DLL	I	SDRAM DLL Ground: 2 PINs
E13	Vdd18_IO	I	XIN_14318 power
D12	Vss18_IO	I	XIN_14318 ground
D17	AVDDPLL	I	USB PLL power
C17	AVSSPLL	I	USB PLL ground
D16;D19	AVDD0 AVDD1	I	USB Analog power
C16;D18	AVSS0 AVSS1	I	USB Analog ground

■ **1.8 V core Power (8 PINs)**

PIN No.	Symbol	Type	Description
E12;E15;M5;M22;R5;R22;AB12;AB15	Vdd_core	I	Vdd_core: 8 PINs

■ **3.3 V Power (5 PINs)**

PIN No.	Symbol	Type	Description
C11;D11	Vdd33_PLL	I	IDE PLL power: 2 PINs
A11;B11	Vss33_PLL	I	IDE PLL ground: 2 PINs
E16	AVDD33	I	USB I/O power

■ **3.3 V IO Power (16 PINs)**

PIN No.	Symbol	Type	Description
E6;E9;E18;E21;F5;F22;J5;J22;V5;V22;AA5; AA22;AB6;AB9;AB18;AB21	Vdd_IO	I	IO power: 16 PINs

■ **1.8 V core and 3.3 V IO Ground (74 PINs)**

PIN No.	Symbol	Type	Description
A10;A15;A17;A19;B15;B17;B19;C3;C6;C9;C12; C15;C18;C19;C20;C21;C24;F3;F24;J3;J24;L11 ~L16;M3;M11~M16;M24;N11~N16;P11~P16;R3 ;R11~R16;R24;T11~T16;V3;V24;AA3;AA24;AD 3;AD6;AD9;AD12;AD15;AD18;AD21;AD24;E14	Vss	I	Ground : 74 PINs

■ **NC pin (4 PINs)**

PIN No.	Symbol	Type	Description
A1;A26;AF1;AF26	NC	I	NC

Chapter 5

System Address Map

The **EVA-X4150** microprocessor supports 4 Gbytes of addressable memory space and 64 Kbytes of addressable I/O space. In order to be compatible with PC/AT system, the lower 1 Mbytes of this addressable memory is divided into regions which can be individually controlled with programmable attributes such as disable, read/write, write only, or read only (see Chapter 11, Register Description section for details on attribute programming).

5.1 Memory Address Ranges

Figure 5.1 represents EVA-X4150 microprocessor memory address map. It shows the main memory regions defined and supported by the EVA-X4150. At the highest level, the address space is divided into two main conceptual regions. One is the 0-1-Mbyte DOS compatibility region and the other is 1-Mbyte to 4-Gbyte extended memory region. The EVA-X4150 processor supports several main memory sizes from 2 MB to 256 MB. The main memory type and size in the system will be auto-detected by the system BIOS.
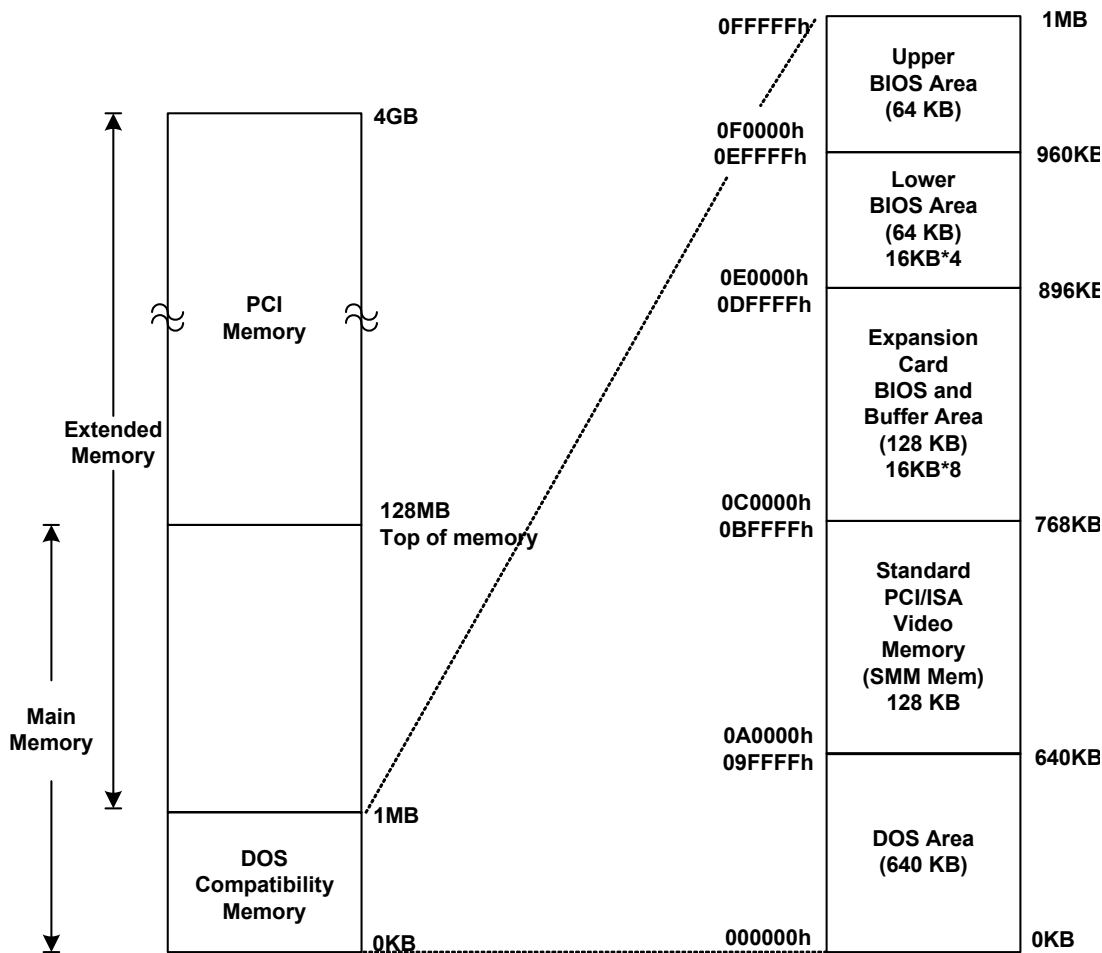
Figure 5.1 Memory Address Map

5.1.1 DOS Compatibility Region

The first region of memory is called the Dos Compatibility Region because it is defined for early PC. This area is divided into the following address regions:

- 0-640-Kbyte DOS Area
- 640-768-Kbyte Video Buffer Area
- 768-896-Kbyte in 16-Kbyte sections (total of 8 sections) - Expansion Area
- 896-960-Kbyte in 16-Kbyte sections (total of 4 sections) - Extended System BIOS Area
- 960-Kbyte-1-Mbyte Memory (BIOS Area) - System BIOS Area

From 640 Kbytes-1Mbytes: it can be divided into fourteen ranges which can be enabled or disabled independently for both read and write. These regions can also be mapped to either main DRAM or PCI by system BIOS. (See A/B Page and SMM Range Register and Memory Attribute Register in Section 3, Chapter 11.)

DOS Area (00000 - 9FFFFh)

The DOS area (00000h - 9FFFFh) is 640 Kbytes in size. It is always mapped to the main memory controlled by the EVA-X4150 microprocessor.

Video Buffer Area (A0000 - BFFFFh)

The 128-Kbyte graphics adapter memory region is normally mapped to a video device on the PCI bus (typically VGA controller). This area is controlled by the A/B Page and SMM Range Register. It can be mapped to either main DRAM or PCI for both read and write command.

This Region is also the default region for SMM space.

ISA Expansion Area (C0000 - DFFFFh)

This 128-Kbyte ISA Expansion region is divided into eight 16-Kbyte segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through the PCI bridge to ISA space. Memory that is disabled is not remapped.

Extended System BIOS Area (E0000 - EFFFFh)

This 64-Kbyte area is divided into four 16-Kbyte segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to PCI. Typically, this area is used for RAM or ROM. Memory that is disabled is not remapped.

System BIOS Area (F0000 - FFFFFh)

This area is a single 64-Kbyte segment that can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to PCI. By manipulating the read/write attributes, the EVA-X4150 microprocessor can "shadow" BIOS into main memory. Memory that is disabled is not remapped.

5.1.2 Extended Memory Region

This memory region covers 10_0000h (1 Mbytes) to FFFF_FFFFh (4 Gbytes minus 1) address range and is divided into the following regions:

- DRAM memory from 1 Mbytes to a top of memory (maximum: 256 Mbytes)
- PCI Memory space from the top of memory to 4 Gbytes
- APIC Configuration Space from FEC00000h (4 Gbytes minus 20 Mbytes) to FEC0_FFFFh
- High BIOS area from 4 Gbytes to 4 Gbytes minus 2 Mbytes

Main DRAM Address Range (0010_0000h to Top of Main Memory)

The address range from 1 Mbytes to the top of main memory is mapped to the main memory address range controlled by the EVA-X4150 microprocessor. All accesses to addresses within this range are forwarded to the main memory.

PCI Memory Address Range (Top of Main Memory to 4 Gbytes)

The address range from the top of main DRAM to 4 Gbytes is normally mapped to PCI. The PMC forwards all accesses within this address range to PCI.

Within this address range, there are two sub-ranges defined as APIC Configuration Space and High BIOS Address Range.

1. High BIOS Area (FFE0_0000 - FFFF_FFFFh)

The top 2 Mbytes of the Extended Memory Region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The CPU begins execution from the High BIOS after reset. This region is mapped to the PCI so that the upper subset of this region is aliased to 16 Mbytes minus 256 Kbytes range. The actual address space required for the BIOS is less than 2 Mbytes. However, the minimum CPU MTRR range for this region is 2 Mbytes. Thus, the full 2 Mbytes must be considered.7

5.2 Memory Shadowing

Any block of memory that can be designated as read only or write only can be "shadowed" into PMC DRAM memory. Typically, this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as read only during the copy process while DRAM at the same time is designated write only. After copying, the DRAM is designated read only so that ROM is shadowed. CPU bus transactions are routed accordingly. The PMC does not respond to transactions originating from PCI or ISA masters and targeted at shadowed memory blocks.

5.3 I / O Address Space

The EVA-X4150 positively decodes accesses to all internal registers, including PCI configuration registers (CF8h and CFCh), PC/AT Compatible IO registers (8237, 8254 & 8259), and all relocatable IO space registers (UART).

Chapter 6

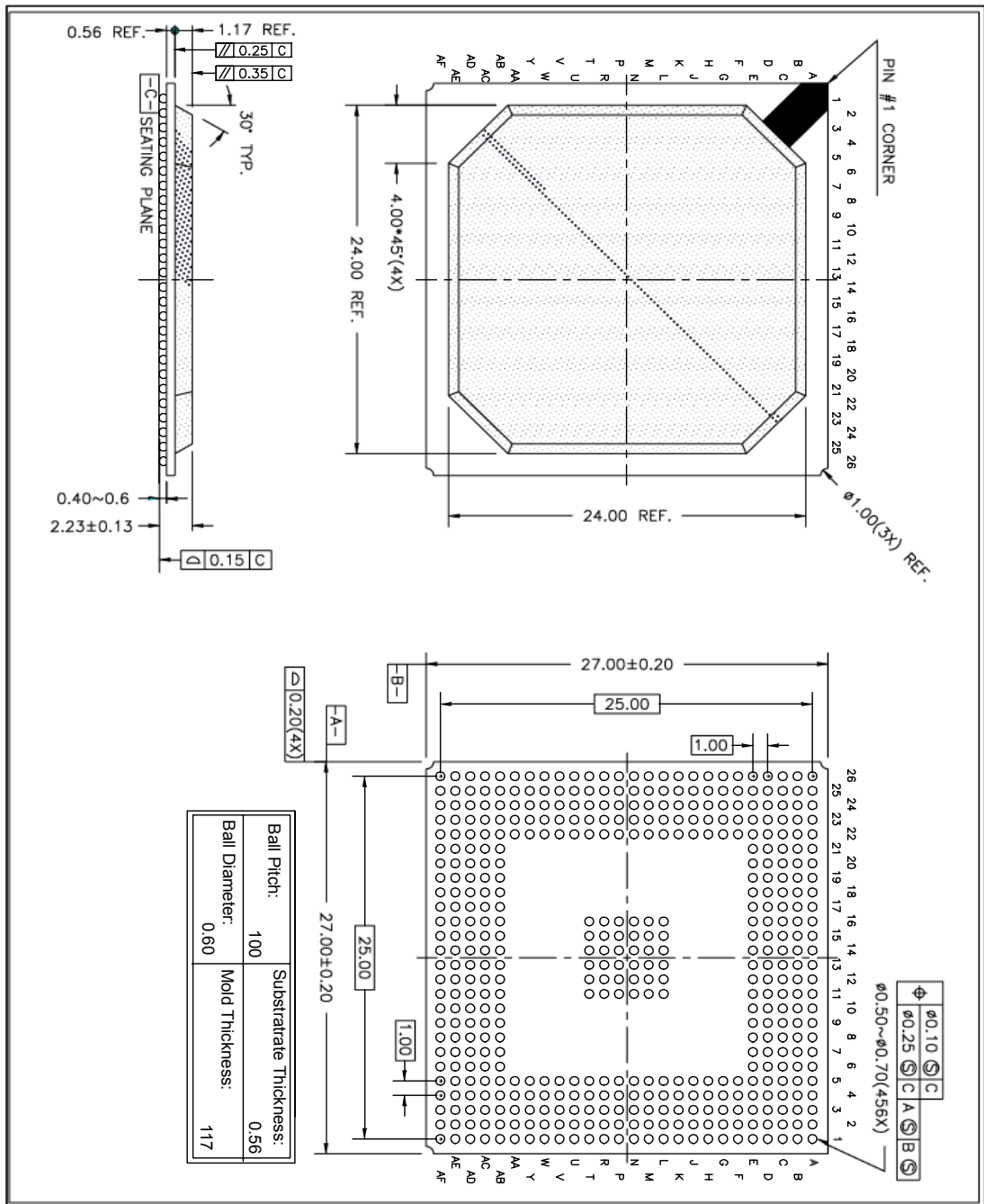## Operating Mode

6.1 Operation Mode

The EVA-X4150 microprocessor supports three operation modes: protected mode, real-address mode, and system management mode. The operation mode determines which instructions and architectural features are accessible:

- **Protected mode.** In this mode all instructions and architectural features are available, providing the highest performance and capability. This is the recommended mode for all new applications and operating systems.
  Among the capabilities of protected mode is the ability to directly execute "real-address mode" 8086 software in a protected, multitasking environment. This feature is called virtual-8086 mode, although it is not actually a processor mode. Virtual-8086 mode is actually a protected mode attribute that can be enabled for any task.

- **Real-address mode.** It provides the programming environment of the Intel 8086 processor with a few extensions (such as the ability to switch to protected or system management mode). The processor is placed in real-address mode following power-up or a reset.

- **Flat mode.** In general, this mode is similar with Real-Address mode. But there is one difference involved, i.e. Flat mode can access 4GBytes address.

Chapter 7

Package Information

7.1 Package Information

Trusted ePlatform Services

ADVANTECH