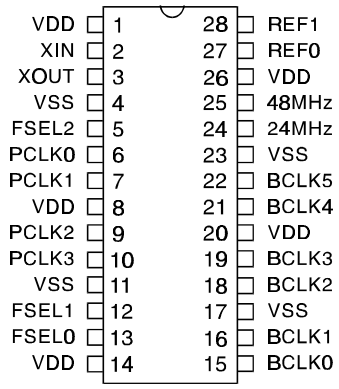
System Clock Generator with Integrated Buffers

FEATURES

- Generates all clock frequencies for Pentium, CYRIX and AMD CPU.
- Provides 4 copies of CPU clock, 6 copies of PCI clock, two system clocks, one 24Mhz and one 48Mhz clock.
- Support 32Mhz Asynchronous PCI BUS clock.
- On chip loop filter components for dual PLLs.
- 3.3V and 5V operation; 50 percent duty cycle.
- Meets Intel Triton system clocking requirements
- Available in 28 pin 300 mil SOIC.

PIN INFORMATION



PLL52C59-14A

DESCRIPTION

The PLL52C59-14A is a high performance system clock generator designed to support Pentium/PCI based systems. Both synchronous and asynchronous mode for PCI BUS clock are provided. All output clocks skew and jitter performance are designed to be fully compliant with INTEL Pentium CPU timing requirements.

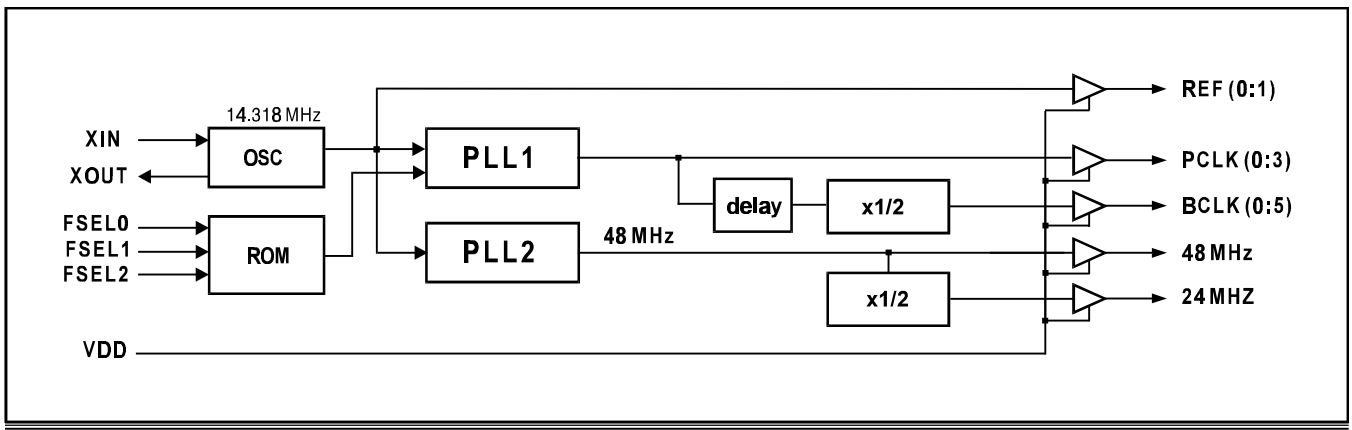
TIMING SPECIFICATIONS

PCLK-PCLK skew	<250 ps
BCLK-BCLK skew	<500 ps
PCLK-BCLK skew	1~5 ns (PCLK leads)
PCLK,BCLK slew rate	> 1 V/ns (0.4 ~2.4V)
PCLK Jitter	±200 ps cycle-cycle

FREQUENCY SELECTION (MHz)

FSEL2	FSEL1	FSEL0	PCLK(0:3)	BCLK(0:5)
1	0	0	50	25
1	0	1	66.6	33.3
1	1	0	60	30
1	1	1	55	27.5
0	0	0	83.3	41.6
0	0	1	83.3	32 (Asyn)
0	1	0	75	32 (Asyn)
0	1	1	75	37.5

BLOCK DIAGRAM



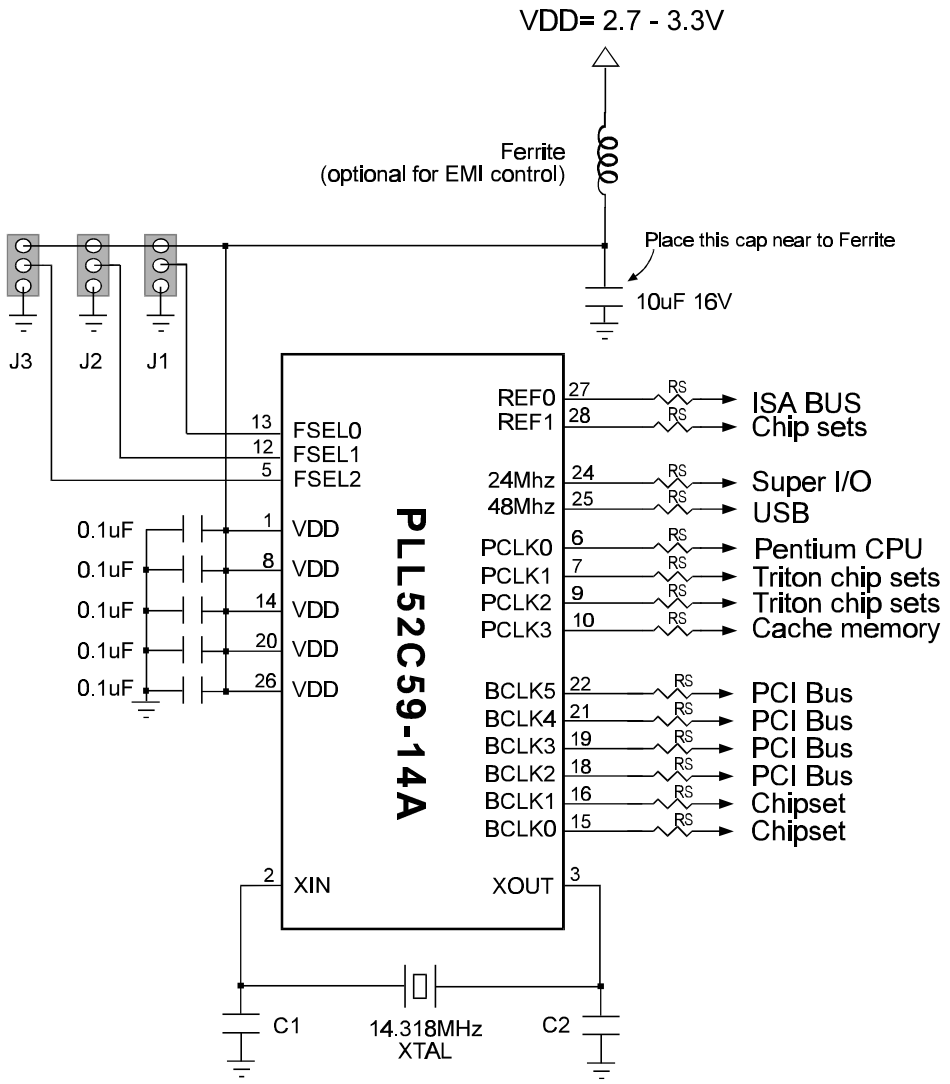
SIGNAL DESCRIPTIONS

PIN NUMBER	NAME	PIN TYPE	DESCRIPTION
1,8,14 20,26	VDD	P	Power supply (3V ~ 5V).
2	XIN	I	14.318MHz crystal input to be connected to one end of the crystal. This input can also be connected directly to other source of 14.318MHz from the PC board.
3	XOUT	O	14.318 Mhz crystal output.
4,11 17,23	VSS	P	Ground.
6,7,9,10	PCLK(0:3)	O	CPU clock output.
5,12,13	FSEL(2:0)	I	FSEL2, FSEL1 and FSEL0 determine the CPU clock frequency. They have internal pull-up resistor. (see Frequency Selection Table)
15,16,18 19,21,22	BCLK(0:5)	O	PCI bus clock output.
24	24Mhz	O	Fixed at 24Mhz for disk controller or super I/O applications.
25	48 Mhz	O	Fixed at 48Mhz for audio, super I/O and bus bridge devices.
27,28	REF(0:1)	O	Buffered reference clock at 14.318Mhz.

ACTUAL CPU CLOCK OUTPUT FREQUENCIES

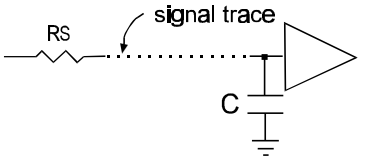
INPUT FREQUENCY SELECTION			OUTPUT FREQUENCIES	
FSEL2	FSEL1	FSEL0	DESIRED	ACTUAL
1	0	0	50 Mhz	50.11 Mhz
1	0	1	66.6 Mhz	66.81 Mhz
1	1	0	60 Mhz	60.14 Mhz
1	1	1	55 Mhz	55.23 Mhz
0	0	0	83.3 Mhz	83.52 Mhz
0	0	1	83.3 Mhz	83.52 Mhz
0	1	0	75 Mhz	75.17 Mhz
0	1	1	75 Mhz	75.17 Mhz

APPLICATION CIRCUITS



Notes:

1. J1, J2, J3: frequency Selection Jumper
2. C1-C2: (optional) for fine tuning the crystal frequency.
3. RS: Series clock terminating resistor is recommended using 20~30 ohm resistor. To further reduce signal ringing and EMI, a capacitor could be placed near the receiving end of the clock line.



4. All 0.1uF power bypass capacitor should be placed as close to each VDD pin as is physically possible

MAXIMUM RATINGS

SUPPLY VOLTAGE	VSS-0.5 TO 7V
INPUT VOLTAGE	VSS-0.5V to VDD+0.5V
ESD VOLTAGE	2000V
POWER DISSIPATION	0.75W

Exposure of the device under conditions beyond the limits specified by Maximum Ratings may cause permanent damage to the device

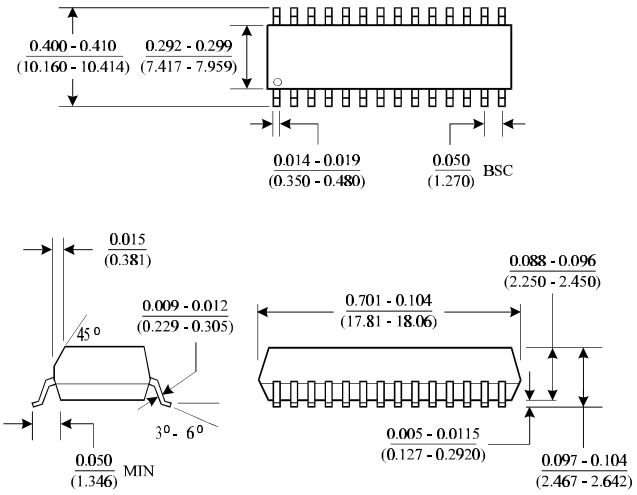
AC SPECIFICATIONS

VDD=3.3V±10% 0°C to 70°C						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reference input clock rise time	T_{IR}	From 0.8 V to 2V			20	ns
Reference input clock fall time	T_{IF}	From 2V to 0.8V			20	ns
Output rise time	T_{OR}	From 0.8V to 2V 25pF load		1	2	ns
		From 10% to 90% 25pF load		2	4	ns
Output fall time	T_{OF}	From 2V to 0.8V 25pF load		1	2	ns
		From 90% to 10% 25pF load		2	4	ns
Duty cycle	D_T	15pF load.	45	50/50	55	%
Clock Skew (20pF load, @ 1.4V)	T_{SKW}	PCLK to PCLK		50	250	ps
		BCLK to BCLK		90	500	ps
		PCLK to BCLK	1	2.5	5	ns
Jitter, Absolute (20pF load)	T_{JA}	PCLK, BCLK	-250		250	ps
Jitter, One Sigma (20pF load)	T_{JO}	PCLK, BCLK		50	150	ps

DC SPECIFICATIONS

VDD=3.3V±10% 0°C to 70°C						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Dynamic Current	I_{DYN}	PCLK at 66.6 MHZ no load		55	110	mA
Static Current	I_{STAT}	All internal circuitry off, XIN=0		25	50	µA
Input High Voltage	V_{IH}	All Inputs except XIN	2			V
Input Low Voltage	V_{IL}	All Inputs except XIN			0.8	V
Output High Current @VOH=2.0V	I_{OH}	PCLK(0:3), BCLK(0:5), 24Mhz,48Mhz		-66		mA
		REF(0:1)		-47		mA
Output Low Current @VOL=0.8V	I_{OL}	PCLK(0:3), BCLK(0:5), 24Mhz, 48Mhz		47		mA
		REF(0:1)		38		mA
Pull-up resistor	R_{Pu}	Pin 5, 12, 13		150		Kohm

PACKAGE INFORMATION



28 PIN SOIC

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

90 Bonaventura Dr., San Jose, CA 95134, USA

Tel: (408) 944-0880 Fax: (408) 944-0110

PART NUMBER

The order number for this device is a combination of the following: device number, package type and operating temperature range.

PLL52C59-14A S C

PART NUMBER

TEMPERATURE
C=COMMERCIAL
I=INDUSTRIAL

PACKAGE TYPE
S=SOIC