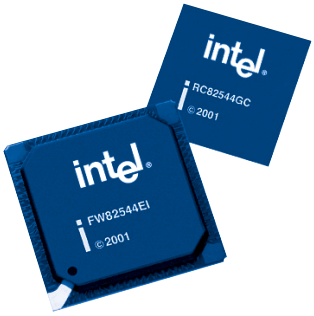

Intel® 82544 Gigabit Ethernet Controllers with Integrated PHY

Network Silicon

Product Brief

Overview

The Intel® 82544EI and 82544GC Gigabit Ethernet Controllers with Integrated PHY are Intel's single-chip Gigabit Ethernet Solutions. The Intel 82544EI Gigabit Ethernet Controller is available in a 27x27mm package for standard servers or workstations, and the Intel 82544GC Gigabit Ethernet Controller is available in a reduced-size, 21x21mm package, for ultra-dense or space-constrained servers.

- Over 50% smaller than the smallest two-chip solution
- Consumes up to 50% less power than other solutions
- Supports PCI-X for faster network performance
- Integrated third-generation MAC and proven IEEE 803.3ab compatible PHY

Product Description

The Intel 82544EI and 82544GC Gigabit Ethernet Controllers are integrated, third-generation, Ethernet-LAN components, capable of supporting 1000Mb/s, 100Mb/s, and 10Mb/s data rates. These single-chip devices allow faster, smaller, simpler designs. The 82544EI and 82544GC manage both the MAC and PHY layer functions, and are optimized for LAN on Motherboard (LOM) designs, enterprise networking, and Internet appliances that use the Peripheral Component Interconnect (PCI) or PCI-X bus. The controllers provide a direct 32/64 bit, 33/66MHz interface to the PCI bus that supports the PCI Local Bus Specification (revision 2.2), as well as the emerging PCI-X extension to the PCI Local Bus (revision 1.0a) at clock rates up to 133MHz.

The Intel 82544EI and 82544GC Gigabit Ethernet Controllers provide an interface to host processors using on-chip command and status registers, and a shared host-memory area. The controller's descriptor ring management architecture is optimized to deliver both high performance and PCI/PCI-X bus efficiency. Using hardware acceleration, the controllers can offload various tasks from the host processor, such as TCP/UDP/IP checksum calculations and TCP segmentation. The Intel 82544EI and 82544GC Gigabit Ethernet Controllers cache up to 64 packet descriptors in a single burst for efficient PCI-bandwidth usage while the large 64KB on-chip packet buffer maintains superior performance as available PCI bandwidth descriptors change.

Fully integrated physical-layer circuitry provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3ab, 802.3u, 802.3). And, with the addition of an appropriate serializer/deserializer (SERDES), the Intel 82544EI and 82544GC Gigabit Ethernet Controllers alternatively provide an Ethernet interface for 1000BASE-SX or LX applications (802.3z).

Applications

The Intel 82544EI and 82544GC Gigabit Ethernet Controllers are designed for use in the following applications:

- LAN on Motherboard (LOM) for servers and workstations
- Industrial PCs including Compact-PCI and PMC designs
- Embedded designs that use a PCI bus (such as Ethernet switches, routers, firewalls, NAS filers, and other server appliances)

The 82544EI and 82544GC single-chip Gigabit Ethernet (MAC/PHY) solutions take up less space, making it easier to provide high-speed network connections as a standard part of a system.

Features	Benefits
PCI/PCI-X Features	
■ PCI revision 2.2 at 32/64 bit, 33/66MHz	■ Application flexibility in LOM or embedded use ■ 64-bit addressing for systems with more than 4GB of physical memory
■ PCI-X, rev.1.0a compliant host interface at clock rates up to 133MHz	■ Optimized server bus performance
■ Algorithms that optimally use advanced PCI MWI, MRM, MRL and PCI-X MRD, MRB, and MWB commands	■ Efficient bus operations
Network Interface (MAC) Features	
■ Low-latency transmit and receive queues	■ Network packets handled without waiting or buffer overflow
■ TBI interface, in addition to internal PHY, for IEEE 802.3z full-duplex operation with SERDES	■ Single device to interface with fiber or CAT-5 twisted-pair transmission mediums
■ IEEE 802.3x compliant flow control support with software controllable pause times and threshold values	■ Control over the transmission of pause frames through software or hardware triggering
Internal Transceiver (PHY) Features	
■ Integrated PHY for 10/100/1000Mb/s full and half operation	■ Reduced board space and lower power dissipation compared to multichip MAC/PHY solutions
■ IEEE 802.3ab Auto-Negotiation	■ Automatic link configuration including speed, duplex, and flow control
■ Proven PHY compatible with IEEE 802.3ab	■ Robust operation over the installed base of CAT-5 twisted-pair cabling
■ State-of-the-art DSP architecture implements digital adaptive equalization, echo cancellation, and cross-talk cancellation	■ Robust performance in noisy environments ■ Tolerance of common electrical signal impairments
Host Offloading Features	
■ RX and TX IP and TCP/UDP checksum off-loading capabilities	■ Reduced host CPU utilization
■ Transmit TCP segmentation offloads host by sending up to 64K of block TCP data to network controller	■ Increased throughput and lower CPU utilization. Compatible with large send offload feature found in Windows* XP
■ Advanced packet filtering	■ 16 exact matched (unicast or multicast) ■ 4096-bit hash filter for multicast frames ■ Promiscuous (unicast/multicast) transfer mode ■ Optional filtering of erred frames
■ IEEE 802.1Q VLAN support	■ VLAN tag insertion and stripping ■ Packet filtering for up to 4096 VLAN tags
■ Descriptor ring management hardware for TX and RX	■ Optimized fetching and write-back mechanisms for efficient system memory and PCI bandwidth usage
■ 16KB jumbo frame support	■ High throughput for large data transfers on compatible network segments
■ Interrupt coalescing (more than one packet per interrupt)	■ Reduced interrupts generated by RX and TX operations, increasing throughput
Memory Features	
■ Programmable host memory receive buffers (256B to 16KB) ■ Programmable cache line size from 16B to 256B	■ Efficient usage of PCI bandwidth
■ 128-bit internal data path architecture	■ Superior DMA transfer rate performance
■ Independent transmit and receive queues	■ Enables simultaneous access by multiple CPUs
■ 64KB of configurable RX and TX Packet FIFOs	■ No external FIFO memory requirements
Management Features	
■ SDG3.0, WfM 2.0, PC2001 compliance	■ Remote network management capabilities via DMI 2.0 and SNMP software
■ Pre-boot eXecution Environment (PXE) Flash interface support	■ Local flash interface for a PXE image
■ ACPI, PCI Power Management, Version 1.1 compliance	■ PCI power management capability requirements for NIC and LOM applications
■ SNMP and RMON statistic counters	■ Ease of monitoring system status
■ Wake on LAN* support	■ Packet recognition and wakeup for NIC and LOM applications without software configuration
Additional Items	
■ Six activity and link indication outputs that directly drive LEDs	■ Indications for Link, RX, TX, and 10, 100, 1000Mb/s
■ PHY detects polarity, MDI-X, and cable lengths. Auto MDI, MDI-X	■ Easier network installation and maintenance at all speeds ■ No need to know the difference between crossover and non-crossover cables ■ End-to-end wiring tolerance
■ Internal PLL for clock generation using a 25MHz crystal or a 25MHz oscillator	■ Lower component count and cost
■ JTAG (IEEE 1149.1) Test Access Port built in	■ Simplified testing using boundary scan

Characteristics

Electrical

■ PCI Signaling	3.3V or 5V environments
■ Power Dissipation	2.1W (typical). Low power and heat – optimized for space-constrained applications.

Environmental

■ Operating temperature	82544EI: 0°C to 70°C (maximum); 82544GC: 0°C to 55°C (maximum). Does not require a heat sink or forced airflow.
■ Storage temperature	-65°C to 140°C

Physical

■ Two package sizes to simplify LOM and embedded board designs	82544EI: 416 pin PBGA, 27x27mm 82544GC: 364 pin TFBGA, 21x21mm

For more information, contact your Intel® sales representative.

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