Data Sheet

KT600 Desktop North Bridge

Revision 1.02
January 28, 2004

VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	9/17/03	Initial external release (same as internal rev 0.6 except for cover page reformatting)	DH
1.01	10/23/03	Added Device 0 Rx60 register description	AT
1.02	1/28/04	Updated Device 0 RxD8-D9 bit descriptions	DH

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North Bridge

Single-Chip North Bridge
for Socket-A (Socket-462) Based Athlon CPUs
with 400 / 333 / 266 MHz Front Side Bus
with 8x / 4x / 2x AGP and V-Link Interfaces
plus Advanced ECC Memory Controller
supporting DDR400, DDR333, and DDR266
(PC3200 / 2700 / 2100 / 1600 DDR DRAM)
for Desktop & Mobile PC Systems

PRODUCT FEATURES

- **High Performance and High Integration Athlon AGP 8x / DDR North Bridge with Advanced System Power Management**
  - Single chip Athlon system controller with 64-bit Socket-A Athlon CPU, 64-bit 200 / 166 / 133 MHz DDR system memory, 8-bit 533 MB/sec high bandwidth V-Link NB / SB, and 32-bit AGP interfaces
  - V-Link interface to VT8235 south bridge chip that includes UltraDMA-133 / 100 / 66 / 33 EIDE, 6 USB 2.0 Ports, AC97 / MC97 link (for Audio and Modem support), LPC, SMBus, Power Management, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip
  - Supports separately powered 2.5V interface to system memory and 1.5V interface to AGP
  - Modular power management and clock control for advanced system power management
- **High Performance Athlon CPU Interface**
  - Supports Socket-A (Socket-462) AMD Athlon processors
  - HSTL-like 1.5V high-speed transceiver logic signal levels
  - Support independent address, data, and snoop interfaces
  - 200 / 166 / 133 MHz DDR (Double Data Rate) transfer on Athlon CPU address and data buses
  - Built-in PLL (Phase Lock Loop) circuitry for optimal skew control within and between clocking regions
  - Four-entry command queue to accommodate maximum CPU throughput
  - Four-entry probe queue to stores probes from the system to the processor
  - Twenty four-entry processor system data and control queue to store system data control commands in two separate read and write buffers for data movement in and out of processor interface
  - Supports WC (Write Combining) cycles
  - Sleep mode support
  - System management interrupt, memory remap and STPCLK mechanism

- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - Supports 533 MHz 8x, 266 MHz 4x, and 133 MHz 2x transfer modes for AD and SBA signaling
  - AGP v3.0 compliant with 8x transfer mode
  - Pseudo-synchronous with the host CPU bus with optimal skew control
  - Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
  - AGP pipelined split-transaction long-burst transfers up to 2.1 GB/sec (4 bytes x 533 MHz)
  - Eight level read request queue
  - Four level posted-write request queue
  - Thirty-two level (quadwords) read data FIFO (256 bytes)
  - Sixteen level (quadwords) write data FIFO (128 bytes)
  - Intelligent request reordering for maximum AGP bus utilization
  - Supports Flush/Fence commands
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme
    - Independent GART lookup control for host / AGP / PCI master accesses
  - Windows 95 OSR-2 VXD and integrated Windows 98 / Windows 2000 miniport driver support
- **High Bandwidth 533 MB / Sec 8-bit V-Link Host Controller**
  - Supports 66 MHz V-Link Host interface with total bandwidth of 533 MB/sec
  - Operates in 4x and 8x modes
  - Full duplex transfers with separate command / strobe in 4x mode, half-duplex in 8x mode
  - Request / Data split transaction
  - Configurable outstanding transaction queue for Host to V-Link Client accesses
  - Supports Defer / Defer-Reply transactions
  - Transaction assurance for V-Link Host to Client access eliminates V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to eliminate data wait-state / throttle transfer latency
  - All V-Link transactions for both Host and Client have a consistent view of transaction data depth and buffer size to avoid data overflow
  - Highly efficient V-Link arbitration with minimum overhead
  - All V-Link transactions have predictable cycle length with known command / data duration

- **Advanced High-Performance DDR DRAM Controller**
  - Supports DDR400, DDR333, and DDR266 double-data-rate synchronous DRAM
  - DRAM interface synchronous with host CPU (200/166/133 MHz) for most flexible configuration
  - DRAM interface may be faster or slower than CPU by 33 MHz
  - Concurrent CPU, AGP, and V-Link access
  - Clock Enable (CKE) control for DRAM power reduction in high speed systems
  - Mixed 1M / 2M / 4M / 8M / 16M / 32M / 64M / 128M x 4/8/16/32 DRAMs
  - Supports 4 DIMMs (8 banks) up to 4 GB DRAMs
  - Allows use of either unbuffered or registered memory modules
  - Flexible row and column addresses. 64-bit data width only
  - 2.5V SSTL-2 DRAM interface
  - Programmable I/O drive capability for MA, MD, and command signals
  - Dual copies of MA and control signals for improved drive
  - ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
  - Two-bank interleaving for 16Mbit DRAM support
  - Four bank interleaving for 64Mb, 128Mb, 256Mb, 512Mb, and 1Gb DRAM support
  - Supports maximum 16-bank interleave (i.e., 16 pages open simultaneously); banks are allocated based on LRU
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
  - Four cache lines (16 quadwords) of CPU to DRAM write buffers
  - Four cache lines of CPU to DRAM read prefetch buffers
  - Read around write capability for non-stalled CPU read
  - Speculative DRAM read before snoop result
  - Burst read and write operation
  - Burst length 4 and 8
  - Supports CL 2 / 2.5 for DDR266 / 333 and CL 2.5 / 3 for DDR400
  - Programmable timing / drive for CS, CKE, MA, Scmd, DQ, DM, DQS
  - Decoupled and burst DRAM refresh with staggered RAS timing (CAS before RAS or self refresh)
- **Advanced System Power Management Support**
  - Dynamic power down of DRAM (CKE)
  - PCI and AGP bus clock run and clock generator control
  - VTT suspend power plane preserves memory data
  - Suspend-to-DRAM and Self-Refresh operation
  - DRAM self-refresh power down
  - 8 bytes of BIOS scratch registers
  - Low-leakage I/O pads
- **Built-in NAND-Tree Pin Scan Test Capability**
- **2.5V, 0.22um, High Speed / Low Power CMOS Process**
- **High-Density 822-Pin HSBGA Package**
  - Integrated heat spreader
  - 35x35mm package body
  - 34x34 ball grid
  - 1.0 mm ball pitch

OVERVIEW

The KT600 is a high performance, cost-effective and energy efficient north bridge for the implementation of AGP / PCI desktop personal computer systems based on 64-bit Socket-A (AMD Athlon) processors with 400, 333, or 266 MHz Front Side Bus.

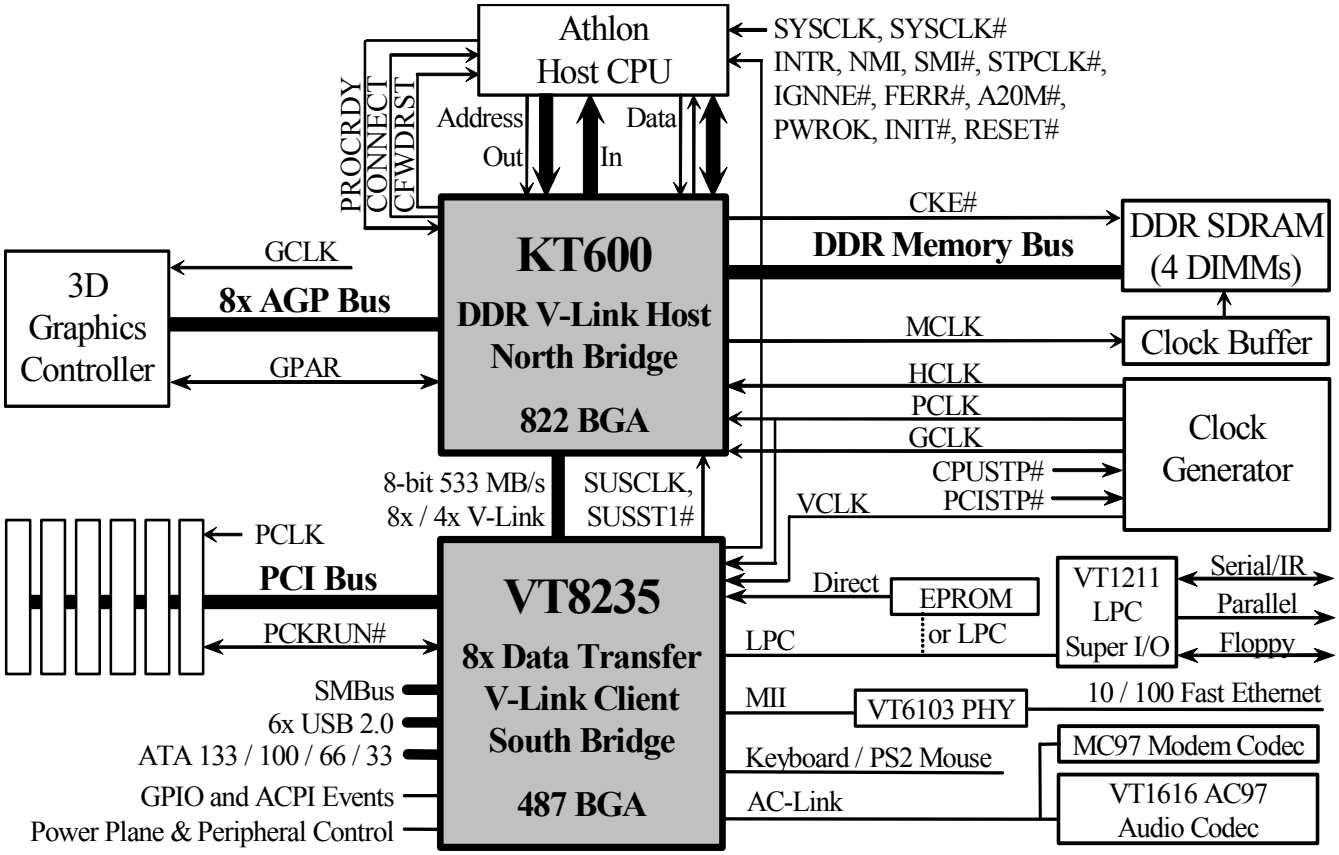


Figure 1. System Block Diagram

The complete chipset consists of the KT600 north bridge "host system controller" (822 pin HSBGA) and the VT8235 V-Link south bridge (487 pin BGA). The KT600 provides superior performance between the CPU, DRAM, AGP bus, and V-Link bus with pipelined, burst, and concurrent operation. The VT8235 (also referred to as a "V-Link Client controller") is a highly integrated PCI / LPC controller. Its internal bus structure is based on a 66 MHz PCI bus that provides 2x bandwidth compared to previous generation PCI / ISA bridge chips. The VT8235 also provides a 533 MB/sec bandwidth Host / Client 8x V-Link interface with V-Link-to-PCI and V-Link-to-LPC controllers. It supports six PCI slots of arbitration and decoding for all integrated functions and LPC bus.

North Bridge

The KT600 supports 4 DIMMs (eight banks) of DDR Synchronous DRAMs up to 8 GB for registered modules (3 DIMMs and six banks up to 6 GB for unbuffered modules). The DRAM controller supports DDR400, DDR333, and DDR266 (PC3200 / PC2700 / PC2100) Double-Data-Rate (DDR) DRAM. The DDR DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 200 / 166 / 133 MHz. The different banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32M / 64M / 128M xN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus (200 / 166 / 133 MHz).

The KT600 also supports full AGP v3.0 capability for maximum bus utilization including 2x, 4x, and 8x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write

request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / Windows 2000 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

The KT600 host system controller supports a high speed 8-bit 8x 66 MHz Quad Data Transfer interconnect (V-Link) to the South Bridge. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and V-Link operation. For V-Link Host operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent V-Link bus and DRAM/cache accesses. When combined, the V-Link Host / Client controllers realize a complete PCI sub-system and support enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

South Bridge

The 487-pin Ball Grid Array VT8235 Client V-Link PCI / LPC controller supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization (PCI-2.2 compliant). The VT8235 integrated PCI controller and PCI arbitration for up to six PCI slots. One of the PCI REQ / GNT pairs can be configured as high-priority to better support a low latency PCI bus master device. The VT8235 integrated networking MAC controller with standard MII interface to an external PHY for 10/100Mb base-T Ethernet or 1/10Mb PNA home networking.

The VT8235 also includes an integrated Audio Subsystem with an AC97 interface to an external AC97 Audio Codec and MC97 Modem codec, an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-133 / 100 / 66 / 33 for 133 / 100 / 66 / 33 MB/sec transfer rate, integrated USB 2.0 interface with three root hubs and six functional ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface.

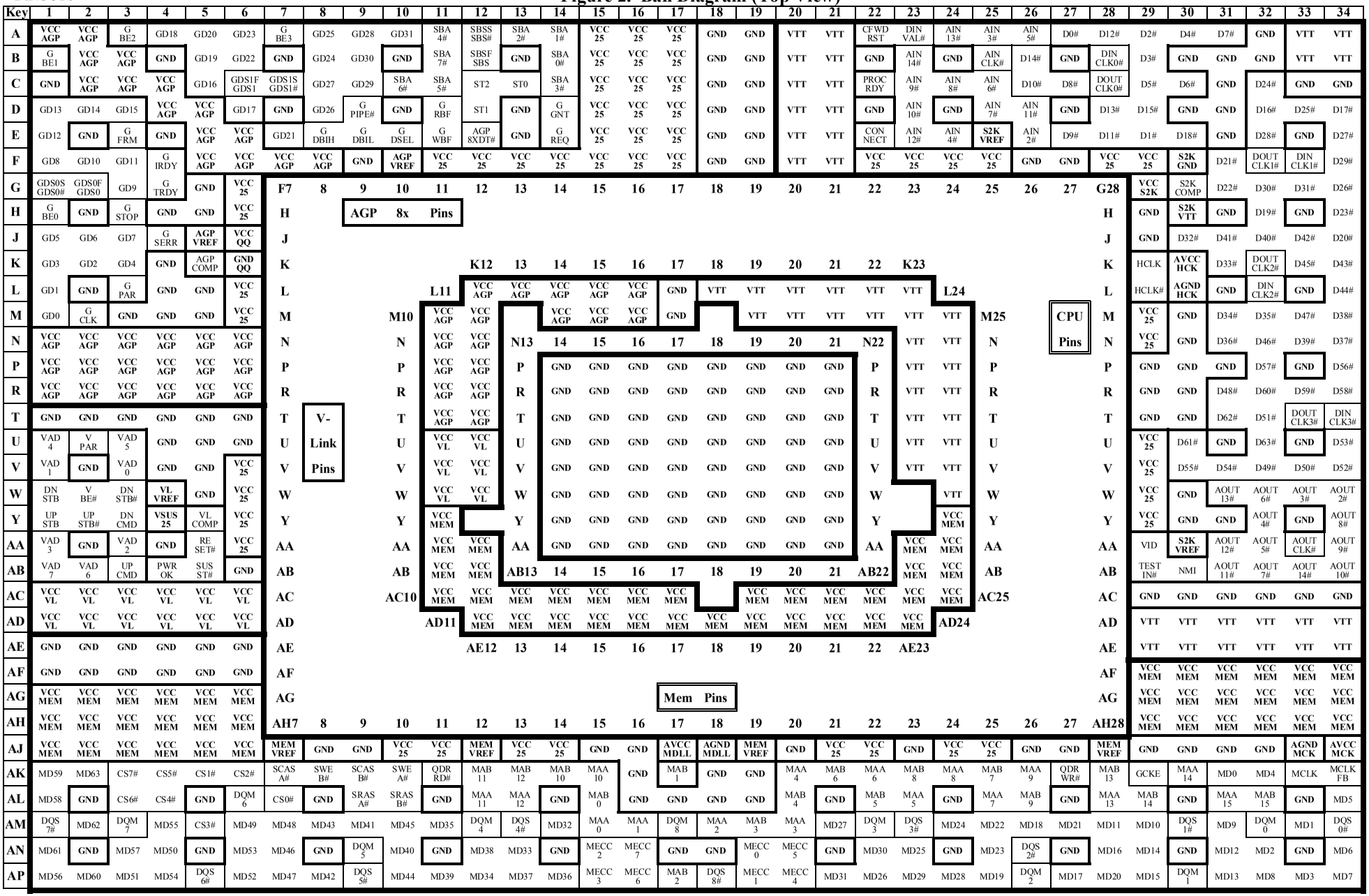
Power Management

For sophisticated power management, the KT600 provides independent clock stop control for the CPU / DRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the DRAM. A separate suspend-well plane is implemented for the DRAM control signals for Suspend-to-DRAM operation. Coupled with the VT8235 south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

The KT600 is ideal for high performance, high quality, high energy efficient and high integration desktop and notebook AGP / PCI / LPC computer systems.

PINOUTS

Figure 2. Ball Diagram (Top View)



Pin Lists

Table 1. Pin List (Numerical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
A03	IO	GBE2	D11	I	GRBF	**J06**	**P**	**VCCQQ**	W32	I	AOUT06#	AK27	O	QDRWR#	AM34	O	DQS0# / CKE0
A04	IO	GD18	D12	O	ST1	J30	IO	D32#	W33	I	AOUT03#	AK28	O	MAB13	AN01	IO	MD61
A05	IO	GD20	D14	O	GGNT	J31	IO	D41#	W34	I	AOUT02#	AK29	O	GCKE	AN03	IO	MD57
A06	IO	GD23	D23	O	AIN10#	J32	IO	D40#	Y01	I	UPSTB	AK30	O	MAA14	AN04	IO	MD50
A07	IO	GBE3	D25	O	AIN07#	J33	IO	D42#	Y02	I	UPSTB#	AK31	IO	MD00	AN06	IO	MD53
A08	IO	GD25	D26	O	AIN11#	J34	IO	D20#	Y03	O	DNCMD	AK32	IO	MD04	AN07	IO	MD46
A09	IO	GD28	D28	IO	D13#	K01	IO	GD3	**Y04**	**P**	**VSUS25**	AK33	O	MCLK	AN09	O	DQM5 / CKE5
A10	IO	GD31	D29	IO	D15#	K02	IO	GD2	Y05	AI	VLCOMP	AK34	I	MCLKFB	AN10	IO	MD40
A11	I	SBA4#	D32	IO	D16#	K03	IO	GD4	Y32	I	AOUT04#	AL01	IO	MD58	AN12	IO	MD38
A12	I	SBSS / SBS#	D33	IO	D25#	K05	AI	AGPCOMP	Y34	I	AOUT08#	AL03	O	CS6#	AN13	IO	MD33
A13	I	SBA2#	D34	IO	D17#	**K06**	**P**	**GNDQQ**	AA01	IO	VAD3 / strap	AL04	O	CS4#	AN15	IO	MECC2 / CKE2
A14	I	SBA1#	E01	IO	GD12	K29	I	HCLK	AA03	IO	VAD2 / strap	AL06	O	DQM6 / CKE6	AN16	IO	MECC7 / CKE7
A22	O	CFWDRST	E03	IO	GFRM	**K30**	**P**	**AVCCHCK**	AA05	I	RESET#	AL07	O	CS0#	AN19	IO	MECC0 / CKE0
A23	O	DINVAL#	E07	IO	GD21	K31	IO	D33#	AA29	I	VID	AL09	O	SRASA#	AN20	IO	MECC5 / CKE5
A24	O	AIN13#	E08	IO	GDBIH	K32	I	DOUTCLK2#	**AA30**	**P**	**S2KVREF**	AL10	O	SRASB#	AN22	IO	MD30
A25	O	AIN03#	E09	IO	GDBIL	K33	IO	D45#	AA31	I	AOUT12#	AL12	O	MAA11	AN23	IO	MD25
A26	O	AIN05#	E10	IO	GDEVSEL	K34	IO	D43#	AA32	I	AOUT05#	AL13	O	MAA12	AN25	IO	MD23
A27	IO	D00#	E11	I	GWBF	L01	IO	GD1	AA33	I	AOUTCLK#	AL15	O	MAB00	AN26	O	DQS2# / CKE2
A28	IO	D12#	E12	I	AGP8XDT#	L03	IO	GPAR	AA34	I	AOUT09#	AL20	O	MAB04	AN28	IO	MD16
A29	IO	D02#	E14	I	GREQ	L29	I	HCLK#	AB01	IO	VAD7 / strap	AL22	O	MAB05	AN29	IO	MD14
A30	IO	D04#	E22	O	CONNECT	**L30**	**P**	**AGNDHCK**	AB02	IO	VAD6 / strap	AL23	O	MAA05	AN31	IO	MD12
A31	IO	D07#	E23	O	AIN12#	L32	O	DINCLK2#	AB03	I	UPCMD	AL25	O	MAA07	AN32	IO	MD02
B01	IO	GBE1	E24	O	AIN04#	L34	IO	D44#	AB04	I	PWROK	AL26	O	MAB09	AN34	IO	MD06
B05	IO	GD19	**E25**	**P**	**S2KVREF**	M01	IO	GD0	AB05	I	SUSST#	AL28	O	MAA13	AP01	IO	MD56
B06	IO	GD22	E26	O	AIN02#	M02	I	GCLK	AB29	I	TESTIN#	AL29	O	MAB14	AP02	IO	MD60
B08	IO	GD24	E27	IO	D09#	M31	IO	D34#	AB30	O	NMI	AL31	O	MAA15	AP03	IO	MD51
B09	IO	GD30	E28	IO	D11#	M32	IO	D35#	AB31	I	AOUT11#	AL32	o	MAB15	AP04	IO	MD54
B11	I	SBA7#	E29	IO	D01#	M33	IO	D47#	AB32	I	AOUT07#	AL34	IO	MD05	AP05	O	DQS6# / CKE6
B12	I	SBSF / SBS	E30	IO	D18#	M34	IO	D38#	AB33	I	AOUT14#	AM01	O	DQS7# / CKE7	AP06	IO	MD52
B14	I	SBA0#	E32	IO	D28#	N31	IO	D36#	AB34	I	AOUT10#	AM02	IO	MD62	AP07	IO	MD47
B23	O	AIN14#	E34	IO	D27#	N32	IO	D46#	**AJ07**	**P**	**MVREF**	AM03	O	DQM7 / CKE7	AP08	IO	MD42
B25	O	AINCLK#	F01	IO	GD8	N33	IO	D39#	**AJ12**	**P**	**MVREF**	AM04	IO	MD55	AP09	O	DQS5# / CKE5
B26	IO	D14#	F02	IO	GD10	N34	IO	D37#	**AJ17**	**P**	**AVCCMDLL**	AM05	O	CS3#	AP10	IO	MD44
B28	O	DINCLK0#	F03	IO	GD11	P32	IO	D57#	**AJ18**	**P**	**AGNDMDLL**	AM06	IO	MD49	AP11	IO	MD39
B29	IO	D03#	F04	IO	GIRDY	P34	IO	D56#	**AJ19**	**P**	**MVREF**	AM07	IO	MD48	AP12	IO	MD34
C05	IO	GD16	**F10**	**P**	**AGPVREF**	R31	IO	D48#	**AJ28**	**P**	**MVREF**	AM08	IO	MD43	AP13	IO	MD37
C06	IO	GDS1F / GDS1	**F30**	**P**	**S2KGND**	R32	IO	D60#	**AJ33**	**P**	**AGNDMCK**	AM09	IO	MD41	AP14	IO	MD36
C07	IO	GDS1S / GDS1#	F31	IO	D21#	R33	IO	D59#	**AJ34**	**P**	**AVCCMCK**	AM10	IO	MD45	AP15	IO	MECC3 / CKE3
C08	IO	GD27	F32	I	DOUTCLK1#	R34	IO	D58#	AK01	IO	MD59	AM11	IO	MD35	AP16	IO	MECC6 / CKE6
C09	IO	GD29	F33	O	DINCLK1#	T31	IO	D62#	AK02	IO	MD63	AM12	O	DQM4 / CKE4	AP17	O	MAB02
C10	I	SBA6#	F34	IO	D29#	T32	IO	D51#	AK03	O	CS7#	AM13	O	DQS4# / CKE4	AP18	O	DQS8#
C11	I	SBA5#	G01	IO	GDS0S / GDS0#	T33	I	DOUTCLK3#	AK04	O	CS5#	AM14	IO	MD32	AP19	IO	MECC1 / CKE1
C12	O	ST2	G02	IO	GDS0F / GDS0	T34	O	DINCLK3#	AK05	O	CS1#	AM15	O	MAA00	AP20	IO	MECC4 / CKE4
C13	O	ST0	G03	IO	GD9	U01	IO	VAD4 /strap	AK06	O	CS2#	AM16	O	MAA01	AP21	IO	MD31
C14	I	SBA3#	G04	IO	GTRDY	U02	IO	VPAR	AK07	O	SCASA#	AM17	O	DQM8	AP22	IO	MD26
C22	I	PROCRDY	**G29**	**P**	**VCCS2K**	U03	IO	VAD5 / strap	AK08	O	SWEB#	AM18	O	MAA02	AP23	IO	MD29
C23	O	AIN09#	G30	AI	S2KCOMP	U30	IO	D61#	AK09	O	SCASB#	AM19	O	MAB03	AP24	IO	MD28
C24	O	AIN08#	G31	IO	D22#	U32	IO	D63#	AK10	O	SWEA#	AM20	O	MAA03	AP25	IO	MD19
C25	O	AIN06#	G32	IO	D30#	U34	IO	D53 #	AK11	O	QDRRD#	AM21	IO	MD27	AP26	O	DQM2 / CKE2
C26	IO	D10#	G33	IO	D31#	V01	IO	VAD1 / strap	AK12	O	MAB11	AM22	O	DQM3 / CKE3	AP27	IO	MD17
C27	IO	D08#	G34	IO	D26#	V03	IO	VAD0 / strap	AK13	O	MAB12	AM23	O	DQS3# / CKE3	AP28	IO	MD20
C28	I	DOUTCLK0#	H01	IO	GBE0	V30	IO	D55#	AK14	O	MAB10	AM24	IO	MD24	AP29	IO	MD15
C29	IO	D05#	H03	IO	GSTOP	V31	IO	D54#	AK15	O	MAA10	AM25	IO	MD22	AP30	O	DQM1 / CKE1
C30	IO	D06#	**H30**	**P**	**S2KVTT**	V32	IO	D49#	AK17	O	MAB01	AM26	IO	MD18	AP31	IO	MD13
C32	IO	D24#	H32	IO	D19#	V33	IO	D50#	AK20	O	MAA04	AM27	IO	MD21	AP32	IO	MD08
D01	IO	GD13	H34	IO	D23#	V34	IO	D52#	AK21	O	MAB06	AM28	IO	MD11	AP33	IO	MD03
D02	IO	GD14	J01	IO	GD5	W01	O	DNSTB	AK22	O	MAA06	AM29	IO	MD10	AP34	IO	MD07
D03	IO	GD15	J02	IO	GD6	W02	IO	VBE#	AK23	O	MAB08	AM30	O	DQS1# / CKE1			
D06	IO	GD17	J03	IO	GD7	W03	O	DNSTB#	AK24	O	MAA08	AM31	IO	MD09			
D08	IO	GD26	J04	IO	GSERR	**W04**	**P**	**VLVREF**	AK25	O	MAB07	AM32	O	DQM0 / CKE0			
D09	I	GPIPE#	**J05**	**P**	**AGPVREF**	W31	I	AOUT13#	AK26	O	MAA09	AM33	IO	MD01			

VCC25 (50 pins): A15-17, B15-17, C15-17, D15-17, E15-17, F11-17,22-25,28-29, G6, H6, L6, M6,29, N29, U29, V6,29, W6,29, Y6,29, AA6, AJ10-11,13-14,21-22,24-25

VCCMEM (71 pins): Y11,24, AA11-12,23-24, AB11-12,23-24, AC11-17,19-24, AD12-23, AF29-34, AG1-6,29-34, AH1-6,29-34, AJ1-6

VCCAGP (51 pins): A1-2, B2-3, C2-4, D4-5, E5-6, F5-8, L12-16, M11-12,14-16, N1-6,11-12, P1-6,11-12, R1-6,11-12, T11-12

VCCVL (18 pins): U11-12, V11-12, W11-12, AC1-6, AD1-6

VTT (53 pins): A20-21,33-34,B20-21,33-34,C20-21,D20-21,E20-21,F20-21,L18-23,M19-24,N23-24,P23-24,R23-24,T23-24,U23-24,V23-24,W24,AD29-34,AE29-34

GND (217 pins): A18-19,32, B4,7,10,13,18-19,22,24,27,30-32, C1,18-19,31,33-34, D7,10,13,18-19,22,24,27,30-31, E2,4,13,18-19,31,33, F9,18-19,26-27, G5, H2,4-5,29,31,33, J29, K4, L2,4-5,17,31,33, M3-5,17,30, N30, P14-21,29-31,33, R14-21,29-30, T1-6,14-21,29-30, U4-6,14-21,31,33, V2,4-5,14-21, W5,14-21,30, Y14-21,30-31,33, AA2,4,14-21, AB6, AC29-34, AE1-6, AF1-6, AJ8-9,15-16,20,23,26-27,29-32, AK16,18-19, AL2,5,8,11,14,16-19,21,24,27,30,33, AN2,5,8,11,14,17-18,21,24,27,30,33

Table 2. Pin List (Alphabetical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
L30	**P**	**AGNDHCK**	D28	IO	D13#	W01	O	DNSTB	G02	IO	GDS0F / GDS0	AM31	IO	MD09	AP16	IO	MECC6 / CKE6
AJ33	**P**	**AGNDMCK**	B26	IO	D14#	W03	O	DNSTB#	G01	IO	GDS0S / GDS0#	AM29	IO	MD10	AN16	IO	MECC7 / CKE7
AJ18	**P**	**AGNDMDLL**	D29	IO	D15#	AM32	O	DQM0 / CKE0	C06	IO	GDS1F / GDS1	AM28	IO	MD11	**AJ07**	**P**	**MVREF**
E12	I	AGP8XDT#	D32	IO	D16#	AP30	O	DQM1 / CKE1	C07	IO	GDS1S / GDS1#	AN31	IO	MD12	**AJ12**	**P**	**MVREF**
K05	AI	AGPCOMP	D34	IO	D17#	AP26	O	DQM2 / CKE2	E03	IO	GFRM	AP31	IO	MD13	**AJ19**	**P**	**MVREF**
F10	**P**	**AGPVREF**	E30	IO	D18#	AM22	O	DQM3 / CKE3	D14	O	GGNT	AN29	IO	MD14	**AJ28**	**P**	**MVREF**
J05	**P**	**AGPVREF**	H32	IO	D19#	AM12	O	DQM4 / CKE4	F04	IO	GIRDY	AP29	IO	MD15	AB30	O	NMI
K30	**P**	**AVCCHCK**	J34	IO	D20#	AN09	O	DQM5 / CKE5	**K06**	**P**	**GNDQQ**	AN28	IO	MD16	C22	I	PROCRDY
AJ34	**P**	**AVCCMCK**	F31	IO	D21#	AL06	O	DQM6 / CKE6	L03	IO	GPAR	AP27	IO	MD17	AB04	I	PWROK
AJ17	**P**	**AVCCMDLL**	G31	IO	D22#	AM03	O	DQM7 / CKE7	D09	I	GPIPE#	AM26	IO	MD18	AK11	O	QDRRD#
E26	O	AIN02#	H34	IO	D23#	AM17	O	DQM8	D11	I	GRBF	AP25	IO	MD19	AK27	O	QDRWR#
A25	O	AIN03#	C32	IO	D24#	AM34	O	DQS0# / CKE0	E14	I	GREQ	AP28	IO	MD20	AA05	I	RESET#
E24	O	AIN04#	D33	IO	D25#	AM30	O	DQS1# / CKE1	J04	IO	GSERR	AM27	IO	MD21	G30	AI	S2KCOMP
A26	O	AIN05#	G34	IO	D26#	AN26	O	DQS2# / CKE2	H03	IO	GSTOP	AM25	IO	MD22	**F30**	**P**	**S2KGND**
C25	O	AIN06#	E34	IO	D27#	AM23	O	DQS3# / CKE3	G04	IO	GTRDY	AN25	IO	MD23	**E25**	**P**	**S2KVREF**
D25	O	AIN07#	E32	IO	D28#	AM13	O	DQS4# / CKE4	E11	I	GWBF	AM24	IO	MD24	**AA30**	**P**	**S2KVREF**
C24	O	AIN08#	F34	IO	D29#	AP09	O	DQS5# / CKE5	K29	I	HCLK	AN23	IO	MD25	**H30**	**P**	**S2KVTT**
C23	O	AIN09#	G32	IO	D30#	AP05	O	DQS6# / CKE6	L29	I	HCLK#	AP22	IO	MD26	B14	I	SBA0#
D23	O	AIN10#	G33	IO	D31#	AM01	O	DQS7# / CKE7	AM15	O	MAA00	AM21	IO	MD27	A14	I	SBA1#
D26	O	AIN11#	J30	IO	D32#	AP18	O	DQS8#	AM16	O	MAA01	AP24	IO	MD28	A13	I	SBA2#
E23	O	AIN12#	K31	IO	D33#	H01	IO	GBE0	AM18	O	MAA02	AP23	IO	MD29	C14	I	SBA3#
A24	O	AIN13#	M31	IO	D34#	B01	IO	GBE1	AM20	O	MAA03	AN22	IO	MD30	A11	I	SBA4#
B23	O	AIN14#	M32	IO	D35#	A03	IO	GBE2	AK20	O	MAA04	AP21	IO	MD31	C11	I	SBA5#
B25	O	AINCLK#	N31	IO	D36#	A07	IO	GBE3	AL23	O	MAA05	AM14	IO	MD32	C10	I	SBA6#
W34	I	AOUT02#	N34	IO	D37#	AK29	O	GCKE	AK22	O	MAA06	AN13	IO	MD33	B11	I	SBA7#
W33	I	AOUT03#	M34	IO	D38#	M02	I	GCLK	AL25	O	MAA07	AP12	IO	MD34	B12	I	SBSF / SBS
Y32	I	AOUT04#	N33	IO	D39#	M01	IO	GD0	AK24	O	MAA08	AM11	IO	MD35	A12	I	SBSS / SBS#
AA32	I	AOUT05#	J32	IO	D40#	L01	IO	GD1	AK26	O	MAA09	AP14	IO	MD36	AK07	O	SCASA#
W32	I	AOUT06#	J31	IO	D41#	K02	IO	GD2	AK15	O	MAA10	AP13	IO	MD37	AK09	O	SCASB#
AB32	I	AOUT07#	J33	IO	D42#	K01	IO	GD3	AL12	O	MAA11	AN12	IO	MD38	AL09	O	SRASA#
Y34	I	AOUT08#	K34	IO	D43#	K03	IO	GD4	AL13	O	MAA12	AP11	IO	MD39	AL10	O	SRASB#
AA34	I	AOUT09#	L34	IO	D44#	J01	IO	GD5	AL28	O	MAA13	AN10	IO	MD40	C13	O	ST0
AB34	I	AOUT10#	K33	IO	D45#	J02	IO	GD6	AK30	O	MAA14	AM09	IO	MD41	D12	O	ST1
AB31	I	AOUT11#	N32	IO	D46#	J03	IO	GD7	AL31	O	MAA15	AP08	IO	MD42	C12	O	ST2
AA31	I	AOUT12#	M33	IO	D47#	F01	IO	GD8	AL15	O	MAB00	AM08	IO	MD43	AB05	I	SUSST#
W31	I	AOUT13#	R31	IO	D48#	G03	IO	GD9	AK17	O	MAB01	AP10	IO	MD44	AK10	O	SWEA#
AB33	I	AOUT14#	V32	IO	D49#	F02	IO	GD10	AP17	O	MAB02	AM10	IO	MD45	AK08	O	SWEB#
AA33	I	AOUTCLK#	V33	IO	D50#	F03	IO	GD11	AM19	O	MAB03	AN07	IO	MD46	AB29	I	TESTIN#
A22	O	CFWDRST	T32	IO	D51#	E01	IO	GD12	AL20	O	MAB04	AP07	IO	MD47	AB03	I	UPCMD
E22	O	CONNECT	V34	IO	D52#	D01	IO	GD13	AL22	O	MAB05	AM07	IO	MD48	Y01	I	UPSTB
AL07	O	CS0#	U34	IO	D53 #	D02	IO	GD14	AK21	O	MAB06	AM06	IO	MD49	Y02	I	UPSTB#
AK05	O	CS1#	V31	IO	D54#	D03	IO	GD15	AK25	O	MAB07	AN04	IO	MD50	V03	IO	VAD0 / strap
AK06	O	CS2#	V30	IO	D55#	C05	IO	GD16	AK23	O	MAB08	AP03	IO	MD51	V01	IO	VAD1 / strap
AM05	O	CS3#	P34	IO	D56#	D06	IO	GD17	AL26	O	MAB09	AP06	IO	MD52	AA03	IO	VAD2 / strap
AL04	O	CS4#	P32	IO	D57#	A04	IO	GD18	AK14	O	MAB10	AN06	IO	MD53	AA01	IO	VAD3 / strap
AK04	O	CS5#	R34	IO	D58#	B05	IO	GD19	AK12	O	MAB11	AP04	IO	MD54	U01	IO	VAD4 /strap
AL03	O	CS6#	R33	IO	D59#	A05	IO	GD20	AK13	O	MAB12	AM04	IO	MD55	U03	IO	VAD5 / strap
AK03	O	CS7#	R32	IO	D60#	E07	IO	GD21	AK28	O	MAB13	AP01	IO	MD56	AB02	IO	VAD6 / strap
A27	IO	D00#	U30	IO	D61#	B06	IO	GD22	AL29	O	MAB14	AN03	IO	MD57	AB01	IO	VAD7 / strap
E29	IO	D01#	T31	IO	D62#	A06	IO	GD23	AL32	o	MAB15	AL01	IO	MD58	W02	IO	VBE#
A29	IO	D02#	U32	IO	D63#	B08	IO	GD24	AK33	O	MCLK	AK01	IO	MD59	**J06**	**P**	**VCCQQ**
B29	IO	D03#	B28	O	DINCLK0#	A08	IO	GD25	AK34	I	MCLKFB	AP02	IO	MD60	**G29**	**P**	**VCCS2K**
A30	IO	D04#	F33	O	DINCLK1#	D08	IO	GD26	AK31	IO	MD00	AN01	IO	MD61	AA29	I	VID
C29	IO	D05#	L32	O	DINCLK2#	C08	IO	GD27	AM33	IO	MD01	AM02	IO	MD62	Y05	AI	VLCOMP
C30	IO	D06#	T34	O	DINCLK3#	A09	IO	GD28	AN32	IO	MD02	AK02	IO	MD63	**W04**	**P**	**VLVREF**
A31	IO	D07#	A23	O	DINVAL#	C09	IO	GD29	AP33	IO	MD03	AN19	IO	MECC0 / CKE0	U02	IO	VPAR
C27	IO	D08#	C28	I	DOUTCLK0#	B09	IO	GD30	AK32	IO	MD04	AP19	IO	MECC1 / CKE1	**Y04**	**P**	**VSUS25**
E27	IO	D09#	F32	I	DOUTCLK1#	A10	IO	GD31	AL34	IO	MD05	AN15	IO	MECC2 / CKE2			
C26	IO	D10#	K32	I	DOUTCLK2#	E08	IO	GDBIH	AN34	IO	MD06	AP15	IO	MECC3 / CKE3			
E28	IO	D11#	T33	I	DOUTCLK3#	E09	IO	GDBIL	AP34	IO	MD07	AP20	IO	MECC4 / CKE4			
A28	IO	D12#	Y03	O	DNCMD	E10	IO	GDEVSEL	AP32	IO	MD08	AN20	IO	MECC5 / CKE5			

VCC25 (50 pins): A15-17, B15-17, C15-17, D15-17, E15-17, F11-17,22-25,28-29, G6, H6, L6, M6,29, N29, U29, V6,29, W6,29, Y6,29, AA6, AJ10-11,13-14,21-22,24-25

VCCMEM (71 pins): Y11,24, AA11-12,23-24, AB11-12,23-24, AC11-17,19-24, AD12-23, AF29-34, AG1-6,29-34, AH1-6,29-34, AJ1-6

VCCAGP (51 pins): A1-2, B2-3, C2-4, D4-5, E5-6, F5-8, L12-16, M11-12,14-16, N1-6,11-12, P1-6,11-12, R1-6,11-12, T11-12

VCCVL (18 pins): U11-12, V11-12, W11-12, AC1-6, AD1-6

VTT (53 pins): A20-21,33-34,B20-21,33-34,C20-21,D20-21,E20-21,F20-21,L18-23,M19-24,N23-24,P23-24,R23-24,T23-24,U23-24,V23-24,W24,AD29-34,AE29-34

GND (217 pins): A18-19,32, B4,7,10,13,18-19,22,24,27,30-32, C1,18-19,31,33-34, D7,10,13,18-19,22,24,27,30-31, E2,4,13,18-19,31,33, F9,18-19,26-27, G5, H2,4-5,29,31,33, J29, K4, L2,4-5,17,31,33, M3-5,17,30, N30, P14-21,29-31,33, R14-21,29-30, T1-6,14-21,29-30, U4-6,14-21,31,33, V2,4-5,14-21, W5,14-21,30, Y14-21,30-31,33, AA2,4,14-21, AB6, AC29-34, AE1-6, AF1-6, AJ8-9,15-16,20,23,26-27,29-32, AK16,18-19, AL2,5,8,11,14,16-19,21,24,27,30,33, AN2,5,8,11,14,17-18,21,24,27,30,33

Pin Descriptions

Table 3. Pin Descriptions

CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
CFWDRST	A22	O	**Clock Forward Reset.** Reset the clock forward circuitry for the Athlon™ interface.
CONNECT	E22	O	**Connect.** Used for power management and clock-forward initialization at reset.
PROCRDY	C22	I	**Processor Ready.** Used for power management and clock-forward initialization at reset.
AIN[14-2]#	(see pin list)	O	**Host CPU Address / Command Output.** Unidirectional system address / command interface to the processor from the system controller. It is used to transfer probes or data movement commands into the processor during PCI-to-DRAM cycles to snoop the CPU internal Cache. AIN[14:2]# is skew-aligned with the forward clock, AINCLK#
AINCLK#	B25	O	**Host CPU Address Output Clock.** Single-ended forwarded clock for the AIN[14:2]# bus that is driven by the system controller. Both rising and falling edges are used to transfer addresses or commands to the processor.
AOUT[14-2]#	(see pin list)	I	**Host CPU Address Input.** Unidirectional system address / command interface from the processor to the system controller. It is used to transfer processor commands or probes responses to the system controller. AOUT[14:2]# is skew-aligned with the forward clock, AOUTCLK#
AOUTCLK#	AA33	I	**Host CPU Address Input Clock.** Single-ended forwarded clock for the AOUT[14:2]# bus that is driven by the processor. Both rising and falling edges are used to transfer commands or probe responses.
D[63-0]#	(see pin list)	IO	**Host CPU Data.** Bi-directional interface between the processor and the system controller for data movement. D[63:0]# bus is skew-aligned with either the DICLK[3:0]# or DOCLK[3:0]# forward clocks.
DINCLK[3-0]#	T34, L32, F33, B28	O	**Host CPU Data Input Clock.** Single-ended forwarded clocks for the D[63:0]# bus, driven by the system controller to the processor. Each 16-bit data word is skew-aligned with one of these clocks. Both rising and falling edges are used to transfer data to the □rocessor.
DOUTCLK[3-0]#	T33, K32, F32, C28	I	**Host CPU Data Output Clock.** Single-ended forwarded clocks for the D[63:0]# bus, driven by the processor to the system controller. Each 16-bit data word is skew-aligned with one of these clocks. Both rising and falling edges are used to transfer data to the system controller.
DINVAL#	A23	O	**Host CPU Data Read In Valid.** Driven by the system controller to control the flow of data into the processor. DINVAL# can be used to introduce an arbitrary number of cycles between octawords into the processor.

Note: I/O pads for the above pins are powered by VTT. Differential input voltage levels are referenced to S2KVREF.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.

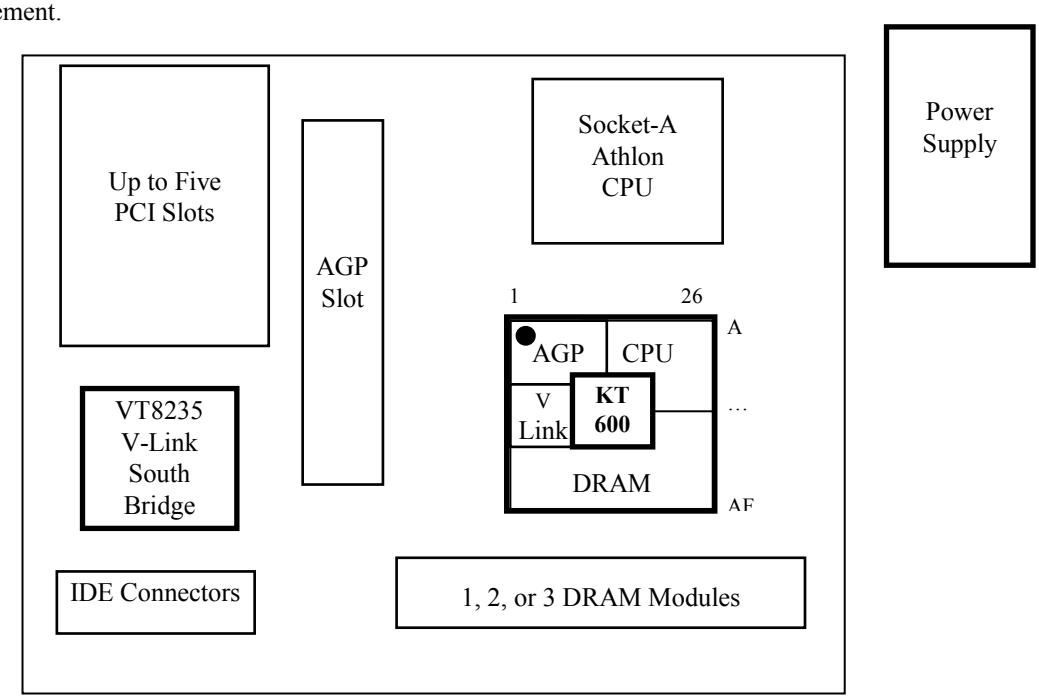


Figure 3. PCB Layout Component Placement Guide

DRAM Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MD[63:0]	(see pin lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 RxE8.
MECC[7:0] / CKE[7:0]	AN16, AP16, AN20, AP20, AP15, AN15, AP19, AN19	IO	**DRAM ECC or EC Data:** when ECC is enabled. **Clock Enables:** For each DRAM bank for powering down the SDRAMs in notebook applications. Also used in desktop systems for clock control to reduce power usage and for reducing heat/temperature in high-speed memory systems.
MAA[15:0]	(see pin lists)	O	**Memory Address A.** DRAM address lines (two sets for better drive). Output drive strength may be set by Device 0 RxEA.
MAB[15:0]	(see pin lists)	O	**Memory Address B.** DRAM address lines (two sets for better drive). Output drive strength may be set by Device 0 RxEB.
SRASA#, **SCASA#, SWEA#**	AL9, AK7, AK10	O	**Row Address, Column Address and Write Enable Command Indicator Set A.** (two sets for better drive). Output drive strength may be set by Device 0 RxEA.
SRASB#, **SCASB#, SWEB#**	AL10, AK9, AK8	O	**Row Address, Column Address and Write Enable Command Indicator Set B.** (two sets for better drive). Output drive strength may be set by Device 0 RxEB.
CS[7:0]#	AK3, AL3, AK4, AL4, AM5, AK6, AK5, AL7	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 RxE9.
DQM[8], **DQM[7:0]** / CKE[7:0]	AM17, AM3, AL6, AN9, AM12, AM22, AP26, AP30, AM32	O	**Data Mask.** Data mask of each byte lane plus DQM8 for ECC byte. Output drive strength may be set by Device 0 RxE8.
DQS[8], **DQS[7:0]**# / CKE[7:0]	AP18, AM1, AP5, AP9, AM13, AM23, AN26, AM30, AM34	IO	**DDR Data Strobe.** Data strobe of each byte lane plus DQS8# for ECC byte. Output drive strength may be set by Device 0 RxE8.
CKE[7:0] / MECC[7:0] **-or-** **CKE[7:0]** / DQM[7:0] **-or-** **CKE[7:0]** / DQS[7:0]#	(see above)	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems. See Device 0 RxBD[6] for CKE function enable.
GCKE	AK29	O	**Global Clock Enable.**
QDRRD#	AK11	O	**QDR Read.** Reserved for future use. Requires 4.7K ohm pullup to VCCMEM for proper system operation.
QDRWR#	AK27	O	**QDR Write.** Reserved for future use.

Note: I/O pads for all pins on this page are powered by VCCMEM. MD / MECC / DQS input voltage levels are referenced to MEMVREF.

V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VAD7 / strap, **VAD6** / strap, **VAD5** / strap, **VAD4** / strap, **VAD3** / strap, **VAD2** / strap, **VAD1** / strap, **VAD0** / strap	AB1, AB2, U3, U1, AA1, AA3, V1, V3	IO	**Address/Data Bus.** Strap / Connection / Register / South Bridge Strap Pin VAD7 strap – reserved for future use – n/a – SDCS3# VAD6 strap – CPU FSB Clk Speed Msb – LL = 100, LH = 133, – Rx54[7] – SDA2 VAD4 strap – CPU FSB Clk Speed Lsb – HL = 200, HH = 166 MHz – Rx54[6] – SDA0 VAD5 strap – Strap Source – L=MA, SCASA, SWEA, H=ROM – Rx54[5] – SDA1 VAD3 strap – CPU Clock Divide Bit-3 – (see Device 0 Rx97[6]) – Rx97[6] – SA19 VAD2 strap – CPU Clock Divide Bit-2 – (see Device 0 Rx97[5]) – Rx97[5] – SA18 VAD1 strap – CPU Clock Divide Bit-1 – (see Device 0 Rx97[4]) – Rx97[4] – SA17 VAD0 strap – CPU Clock Divide Bit-0 – (see Device 0 Rx97[3]) – Rx97[3] – SA16 The VAD pins are used to communicate strap information to the north bridge from the south bridge at system power up (i.e., the actual straps are on the indicated pin of the south bridge chip). Note that in the KT266A, strap VAD6 is used to select Center DQ / Edge DQ. In the KT333 and KT600, Center / Edge DQ may only be selected via the ROMSIP.
VPAR	U2	IO	**Parity.**
VBE#	W2	IO	**Byte Enable.**
UPCMD	AB3	I	**Command from Client-to-Host.**
UPSTB	Y1	I	**Strobe from Client-to-Host.**
UPSTB#	Y2	I	**Complement Strobe from Client-to-Host.**
DNCMD	Y3	O	**Command from Host-to-Client.**
DNSTB	W1	O	**Strobe from Host-to-Client.**
DNSTB#	W3	O	**Complement Strobe from Host-to-Client.**

Note: I/O pads for all pins on this page are powered by VCCVL. Input voltage levels are referenced to VLVREF.

AGP Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GD[31:0]	(see pin list)	IO	**Address / Data Bus.** Address is driven with GDS assertion for AGP-style transfers and with GFRM# assertion for PCI-style transfers.
GBE[3:0] (GBE[3:0#] for 4x mode)	A7, A3, B1, H1	IO	**Command / Byte Enable.** (Interpreted as C/BE# for AGP 2x/4x and C#/BE for 8x). For AGP cycles these pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# (2x/4x only as GPIPE# isn't used in 8x mode). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data. For PCI cycles, commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	L3	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GBE[3:0].
GDBIH, **GDBIL**	E8, E9	IO	**Dynamic Bus Inversion High / Low.** AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group.
GDS0F (GDS0 for 4x), **GDS0S** (GDS0# for 4x)	G2 G1	IO	**Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). GDS0 provides timing for 2x data transfer mode; GDS0 and GDS0# provide timing for 4x mode. For 8x transfer mode, GDS0 is interpreted as GDS0F ("First" strobe) and GDS0# as GDS0S ("Second" strobe).
GDS1F (GDS1 for 4x), **GDS1S** (GDS1# for 4x)	C6 C7	IO	**Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). GDS1 provides timing for 2x data transfer mode; GDS1 and GDS1# provide timing for 4x transfer mode. For 8x transfer mode, GDS1 is interpreted as GDS1F ("First" strobe) and GDS1# as GDS1S ("Second" strobe).
GFRM (GFRM# for 4x)	E3	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. Interpreted as active high for 8x.
GIRDY (GIRDY# for 4x)	F4	IO	**Initiator Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP write cycles, the assertion of this pin indicates that the master is ready to provide *all* write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For AGP read cycles, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. For PCI cycles, ssserted when the initiator is ready for data transfer.
GTRDY (GTRDY# for 4x)	G4	IO	**Target Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. For PCI cycles, asserted when the target is ready for data transfer.
GSTOP (GSTOP# for 4x)	H3	IO	**Stop.** Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x.
GDSEL (GDSEL# for 4x mode)	E10	IO	**Device Select (PCI transactions only).** This signal is driven by the north bridge when a PCI initiator is attempting to access main memory. It is an input when the chip is acting as PCI initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x.
GPIPE#	D9	I	**Pipelined Request.** Not used by AGP 8x. Asserted by the master (external graphics controller) to indicate that a full-width request is to be enqueued by the target (north bridge). The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus.

Note: I/O pads for all pins on this page are powered by VCCAGP. Input voltage levels are referenced to AGPVREF.

AGP Bus Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AGP8XDT#	E12	I	**AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode
GRBF (GRBF# for 4x)	D11	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the north bridge will not return low priority read data to the graphics controller.
GWBF (GWBF# for 4x)	E11	I	**Write Buffer Full.**
SBA[7:0]# (SBA[7:0] for 4x)	B11, C10, C11, A11, C14, A13, A14, B14	I	**SideBand Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (north bridge). These pins are ignored until enabled.
SBSF (SBS for 4x), **SBSS** (SBS# for 4x)	B12, A12	I	**Sideband Strobe.** Driven by the master to provide timing for SBA[7:0]. SBS is used for AGP 2x while SBS and SBS# are used together for AGP 4x. For 8x mode, the strobe mechanism works differently with SBS interpreted as SBSF ("First" strobe) and SBS# as SBSS ("Second" strobe).
ST[2:0]	C12, D12, C13	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the target (north bridge logic) and inputs to the master (graphics controller).
GREQ (GREQ# for 4x)	E14	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT (GGNT# for 4x)	D14	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR (GSERR# for 4x)	J4	IO	**AGP System Error.**

Note: I/O pads for all pins on this page are powered by VCCAGP. Input voltage levels are referenced to AGPVREF.

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an internal pullup to maintain it in the de-asserted state in case it is not implemented on the master device. AGP 8x mode allows only SBA (GPIPE# isn't used in 8x mode).

Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

Interrupt, Test, Clock, Reset, and Power Control				
Signal Name	**Pin #**	**I/O**	**Signal Description**	**Power Plane**
HCLK	K29	I	**Host Clock.** This pin receives the host CPU clock (200 / 166 / 133 / 100 MHz). This clock is used by all KT600 logic that is in the host CPU domain. The memory interface logic will also use this clock if selected (memory system timing can alternately be selected to use the AGP bus clock). The CPU clock must lead the AGP clock by 0.2 ± 0.5 nsec.	**VTT**
HCLK#	L29	I	**Host Clock Complement.**	**VTT**
GCLK	M2	I	**AGP Clock.** 66 MHz clock used by all KT600 logic that is in the AGP clock domain. The AGP clock must be synchronous to the 200 MHz host CPU clock.	**VCCAGP**
MCLK	AK33	O	**DRAM Clock.** Output from internal clock generator to the DIMMs or to external clock buffer (if needed for fanout).	**VCCMEM**
MCLKFB	AK34	I	**DRAM Clock Feedback.** Input from MCLK.	**VCCMEM**
RESET#	AA5	I	**Reset.** Input from south bridge chip. When asserted, this signal resets the KT600 and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options	**VSUS25**
PWROK	AB4	I	**Power OK.**	**VSUS25**
SUSST#	AB5	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.	**VSUS25**
NMI	AB30	O	**Non Maskable Interrupt.** Connect to South Bridge NMI input.	**VTT**
VID	AA29	I	**Voltage ID.** CPU FSB interface voltage select. 0 = desktop, 1 = mobile.	**VCCMEM**
TESTIN#	AB29	I	**PLL Test Input.** Normally connected to VCC25 with a 4.7K pullup.	**VCCMEM**

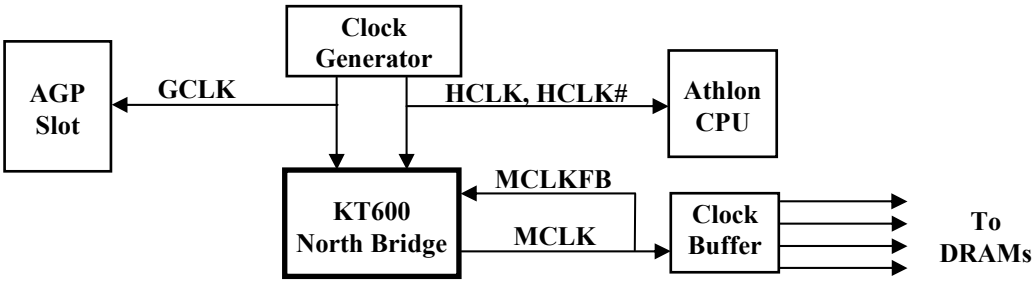


Figure 4. Clock Distribution

Reference Voltages				
Signal Name	**Pin #**	**I/O**	**Signal Description**	**Power Plane**
S2KVREF	E25, AA30	P	**S2K Bus Differential Input Voltage Reference.** 1/2 VTT derived using 100 Ω 1% + 100 Ω 1% resistive voltage divider. See Design Guide.	**VTT**
MEMVREF	AJ7, AJ12, AJ19, AJ28	P	**Memory MD / MECC / DQS Input Voltage Reference.** 1/2 VCCMEM ±2% typically derived using a resistive voltage divider. See Design Guide.	**VCCMEM**
VLVREF	W4	P	**V-Link Input Voltage Reference.** 0.625V ±2% derived using a resistive voltage divider. See Design Guide.	**VCCVL**
AGPVREF	F10, J5	P	**AGP Input Voltage Reference.** 0.5 VCCAGP (0.75V) for AGP 2.0 (4x transfer mode) and 0.23 VCCAGP (0.35V) for AGP 3.0 (8x mode). See Design Guide for additional information and circuit implementation details.	**VCCAGP**

Compensation				
Signal Name	**Pin #**	**I/O**	**Signal Description**	**Power Plane**
S2KCOMP	G30	AI	**S2K Bus Compensation.** Connect to 300 Ω 1% resistor to ground.	**VTT**
VLCOMP	Y5	AI	**V-Link Compensation.** Connect 360Ω 1% resistor to ground.	**VCCVL**
AGPCOMP	K5	AI	**AGP Compensation.** Connect to 60Ω 1% resistor to VCCQQ.	**VCCAGP**

Compensation Power				
Signal Name	**Pin #**	**I/O**	**Signal Description**	**Power Plane**
S2KVTT	H30	P	**S2K Bus Compensation Voltage.** Connect to same voltage as VTT. Voltage is CPU dependent. See Design Guide for recommended power circuit implementation details.	**VTT**
S2KGND	F30	P	**S2K Bus Ground.** Connect to main ground plane.	–
VCCQQ	J6	P	**AGP Quiet Power (AGP Compensation Circuit Power).** Connect to main AGP power (VCCAGP) through a ferrite bead.	**VCCAGP**
GNDQQ	K6	P	**Ground for AGP Quiet Power.** Connect to main ground plane.	–

Analog Power / Ground				
Signal Name	**Pin #**	**I/O**	**Signal Description**	**Power Plane**
AVCCHCK	K30	P	**Power for Host CPU Clock PLL** (2.5V ±5%)	**VTT**
AGNDHCK	L30	P	**Ground for Host CPU Clock Circuitry.** Connect to main ground plane through a ferrite bead.	–
AVCCMCK	AJ34	P	**Power for Memory Clock PLL** (2.5V ±5%)	**VCCMEM**
AGNDMCK	AJ33	P	**Ground for Memory Clock Circuitry.** Connect to main ground plane through a ferrite bead.	–
AVCCMDLL	AJ17	P	**Power for Memory Strobe DLL** (2.5V ±5%)	**VCCMEM**
AGNDMDLL	AJ18	P	**Ground for Memory Strobe DLL Circuitry.** Connect to main ground plane through a ferrite bead.	–

Digital Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VTT	(see pin lists)	P	**Power** for **CPU I/O Interface Logic (55 Pins).** Voltage is CPU dependent.
VCCS2K	G29	P	**Power for CPU Internal Circuitry.** (2.5V ±5%)
VCCMEM	(see pin lists)	P	**Power** for **Memory I/O Interface Logic (74 Pins).** 2.5V ±5%.
VCCVL	(see pin lists)	P	**Power** for **V-Link I/O Interface Logic (18 Pins).** 2.5V ±5%
VCCAGP	(see pin lists)	P	**Power** for **AGP Bus I/O Interface Logic (52 Pins).** 1.5V ±5%
VCC25	(see pin lists)	P	**Power** for **Internal Logic (50 Pins).** 2.5V ±5%
VSUS25	Y4	P	**Suspend Power.** 2.5V ±5%
GND	(see pin lists)	P	**Digital Ground (217 Pins).** Connect to main ground plane.

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the KT600 North Bridge chip (refer to the separate VT8235 data sheet for the register definitions of the South Bridge chip). These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 4. Registers

KT600 I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

KT600 Device 0 Registers - Host Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3189**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	**0000 0008**	**RW**
14-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	**W1**
2F-2E	Subsystem ID	0000	**W1**
30-33	-reserved-	00	—
34	Capability Pointer **AGP 2.0:**	**A0**	RO
	(CAPPTR) **AGP 3.0:**	**80**	RO
35-3F	-reserved-	00	—

Device-Specific Registers

Offset	V-Link Control	Default	Acc
40	V-Link Revision ID	00	**RO**
41	V-Link NB Capability	**19**	**RO**
42	V-Link NB Downlink Command	**88**	RW
44-43	V-Link NB Uplink Status	**8280**	**RO**
45	V-Link NB Bus Timer	**44**	RW
46	V-Link Misc NB Control	00	RW
47	V-Link Control	00	RW
48	V-Link NB/SB Configuration	**18**	RW
49	V-Link SB Capability	**19**	**RO**
4A	V-Link SB Downlink Status	**88**	**RO**
4C-4B	V-Link SB Uplink Command	**8280**	RW
4D	V-Link SB Bus Timer	**44**	RW
4E	CCA Master High Priority	00	RW
4F	V-Link SB Miscellaneous Control	00	RW

Offset	CPU Configuration	Default	Acc
50	S2K Duty Cycle Adjust 1	**04**	RW
51	S2K Duty Cycle Adjust 2	00	RW
52	S2K Duty Cycle Adjust 3	00	RW
53	S2K Duty Cycle Adjust 4	**80**	RW
54	CPU Frequency Select	x0	RW

Device-Specific Registers (continued)

Offset	DRAM Control	Default	Acc
55	DRAM Control	00	RW
56-57	(see below)		
59-58	MA Map Type	**2222**	RW
5F-5A	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[31:24])	**01**	RW
5B	Bank 1 Ending (HA[31:24])	**01**	RW
5C	Bank 2 Ending (HA[31:24])	**01**	RW
5D	Bank 3 Ending (HA[31:24])	**01**	RW
5E	Bank 4 Ending (HA[31:24])	**01**	RW
5F	Bank 5 Ending (HA[31:24])	**01**	RW
56	Bank 6 Ending (HA[31:24])	**01**	RW
57	Bank 7 Ending (HA[31:24])	**01**	RW
60	DRAM Fast Precharge Control	00	RW
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for All Banks	**64**	RW
65	DRAM Arbitration Timer	00	RW
66	DRAM Arbitration Control	00	RW
67	DRAM DQS/SDR/MD Read Delay	00	RW
68	DRAM DDR Control	00	RW
69	Extended SMRAM Control	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	**10**	RW
6C	DRAM Drive Strength Control	00	RW
6D	DRAM MD Output Delay	00	RW
6E	ECC Control	00	RW
6F	ECC Status	00	**RO**

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control	**48**	RW
72	-reserved-	00	—
73	PCI Master Control	00	RW
74	-reserved-	00	—
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77-7F	-reserved-	00	—

Offset	AGP 2.0 Control (RxFD[1]=1)	Default	Acc
83-80	AGP 2.0 GART/TLB Control	0000 0000	RW
84	AGP 2.0 Graphics Aperture Size	00	RW
85-87	Reserved (Do Not Program)	00	RW
8B-88	AGP 2.0 GART Table Base	0000 0000	RW
8C-9F	-reserved-	00	—
A3-A0	AGP 2.0 Capabilities	**0020 C002**	**RO**
A7-A4	AGP 2.0 Status	**1F00 0201**	**RO**
AB-A8	AGP 2.0 Command	0000 0000	RW

Registers A0-AB in the AGP 2.0 register group in the table above are actually offsets from CAPPTR (Rx34) which (with Rx34 = A0h for AGP 2.0) result in the offsets listed above.

Offset	AGP 3.0 Control (RxFD[1]=0)	Default	Acc
83-80	AGP 3.0 Capabilities	**0030 C002**	**RO**
87-84	AGP 3.0 Status	**1F00 0A03**	**RO**
8B-88	AGP 3.0 Command	**1F00 0000**	RW
8F-8C	-reserved-	0000 0000	—
93-90	AGP 3.0 GART / TLB Control	0000 0000	RW
97-94	AGP 3.0 Graphics Aperture Size	**0001 0F00**	RW
9B-98	AGP 3.0 GART Table Base	0000 0000	RW
9C-AB	-reserved-	00	—

Registers 80-AB in the AGP 3.0 register group in the table above are actually offsets from CAPPTR (Rx34) which (with Rx34 = 80h for AGP 3.0) result in the offsets listed above.

Offset	AGP 2.0 / 3.0 Control	Default	Acc
AC	AGP Control	00	RW
AD	AGP Latency Timer	**02**	RW
AE	AGP Miscellaneous Control	00	RW
AF	AGP 3.0 Control	00	RW
B0	AGP Pad Control / Status	**8x**	RW
B1	AGP Drive Strength	**63**	RW
B2	AGP Pad Drive / Delay Control	**08**	RW
B3	AGP Strobe Output Drive Control	00	RW

Offset	V-Link Control	Default	Acc
B4	V-Link NB Compensation Control	00	RW
B5	V-Link NB Strobe Drive Control	00	RW
B6	V-Link NB Data Drive Control	00	RW
B7	-reserved-	00	—
B8	V-Link SB Compensation Control	00	RW
B9	V-Link SB Strobe Drive Control	00	RW
BA	V-Link SB Data Drive Control	00	RW
BB	-reserved-	00	—

Offset	Power Control	Default	Acc
BC	Power Management Mode	00	RW
BD	DRAM Power Management Control	00	RW
BE	Dynamic Clock Stop Control	00	RW
BF	MA / SCMD Pad Toggle Reduction	00	RW

Offset	Extended Power Management	Default	Acc
C0	Power Management Capability ID	**01**	**RO**
C1	Power Management New Pointer	00	**RO**
C2	Power Management Capabilities I	**02**	**RO**
C3	Power Management Capabilities II	00	**RO**
C4	Power Management Control / Status	00	RW
C5	Power Management Status	00	RW
C6	PCI-to-PCI Bridge Support Extension	00	RW
C7	Power Management Data	00	RW
C8-CF	-reserved-	00	—

Offset	Host CPU Control	Default	Acc
D0-D1	-reserved-	00	—
D2	S2K Timing Control	**78**	RW
D3	BIU Arbitration Control	00	RW
D4	BIU Control 1	00	RW
D5	BIU Control 2	00	RW
D6	BIU Control 3	00	RW
D7	CPU Strapping	**strapping**	**RO**
D8	S2K Compensation Strapping	00	RW
D9	S2K Compensation Result 1	00	**RO**
DA	S2K Compensation Result 2	00	RW
DB	S2K Compensation Result 3	00	**RO**
DC	S2K Compensation Result 4	**07**	RW
DD	S2K Compensation Result 5	00	RW
DE	BIU Control 4	00	RW
DF	BIU Control 5	00	RW
E0-E5	-reserved-	00	—
E6	APIC Decoding	00	RW
E7	-reserved-	00	—

Offset	DRAM Drive	Default	Acc
E8	DRAM DQ Drive	00	RW
E9	DRAM CS# Drive	00	RW
EA	DRAM MAA Drive	00	RW
EB	DRAM MAB Drive	00	RW
EC	DRAM S-Port Control	00	RW
ED	DRAM DQS Drive Control	00	RW
EE	DRAM DQS/MD Duty Cycle Control	00	RW
EF	-reserved-	00	—

Offset	Miscellaneous	Default	Acc
F0-FC	-reserved- (Do Not Program)	00	—
FD	AGP 2.0 / 3.0 Select	00	RW
FE-FF	-reserved- (Do Not Program)	00	—

KT600 Device 1 - PCI-to-PCI Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**B168**	RO
5-4	Command	**0007**	**RW**
7-6	Status	**0230**	**WC**
8	Revision ID	**nn**	RO
9	Program Interface	00	RO
A	Sub Class Code	**04**	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	**01**	RO
F	Built In Self Test (BIST)	00	RO
10-17	-reserved-	00	—
18	Primary Bus Number	00	**RW**
19	Secondary Bus Number	00	**RW**
1A	Subordinate Bus Number	00	**RW**
1B	Secondary Latency Timer	00	RO
1C	I/O Base	**F0**	**RW**
1D	I/O Limit	00	**RW**
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	**FFF0**	**RW**
23-22	Memory Limit (Inclusive)	0000	**RW**
25-24	Prefetchable Memory Base	**FFF0**	**RW**
27-26	Prefetchable Memory Limit	0000	**RW**
28-33	-reserved-	00	—
34	Capability Pointer	**80**	RO
35-3D	-reserved-	00	—
3F-3E	PCI-to-PCI Bridge Control	00	**RW**

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	00	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	**22**	RW
44	Back-Door Register Control	**20**	RW
45	Fast Write Control	**72**	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48	Parity Error Reporting	00	RW
49-7F	-reserved-	00	—
80	Capability ID	**01**	**RO**
81	Next Pointer	00	**RO**
82	Power Management Capabilities 1	**02**	**RO**
83	Power Management Capabilities 2	00	**RO**
84	Power Management Control / Status	00	RW
85	Power Management Status	00	**RO**
86	PCI-PCI Bridge Support Extensions	00	**RO**
87	Power Management Data	00	**RO**
88-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined in the KT600: Port 22.

Port 22 – PCI / AGP Arbiter Disable..... RW

7-2 Reserved ..... always reads 0

1 AGP Arbiter Disable
- 0 Respond to GREQ# signal ..... default
- 1 Do not respond to GREQ# signal

0 PCI Arbiter Disable
- 0 Respond to all REQ# signals..... default
- 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 76.

Configuration Space I/O

All registers in the KT600 (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address .....RW

31 Configuration Space Enable
- 0 Disabled.....default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved ..... always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system (devices 0 and 1 are defined for the KT600)

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the KT600).

7-2 Register Number (also called the "Offset")
Used to select a specific DWORD in the KT600 configuration space

1-0 Fixed ..... always reads 0

Port CFF-CFC - Configuration Data .....RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

Device 0 Header Registers - Host Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID (1106h)..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID (3189h) ..... RO

15-0 ID Code (reads 3189h to identify the KT600)

Device 0 Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable.....RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable.....RO
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping .....RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... **RW**
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop .....RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command.....RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring .....RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 PCI Bus Master.....RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master..... default

1 Memory Space.....RO
- 0 Does not respond to memory space
- 1 Responds to memory space ..... default

0 I/O Space .....RO
- 0 Does not respond to I/O space ..... default
- 1 Responds to I/O space

Device 0 Offset 7-6 – Status (0210h) .....RWC

15 Detected Parity Error
- 0 No parity error detected.....default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

14 Signaled System Error (SERR# Asserted)
..... always reads 0

13 Signaled Master Abort
- 0 No abort received .....default
- 1 Transaction aborted by the master ....write one to clear

12 Received Target Abort
- 0 No abort received .....default
- 1 Transaction aborted by the target ....write one to clear

11 Signaled Target Abort ..... always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected .....default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and KT600 was initiator of the operation in which the error occurred. .....write one to clear

7 Fast Back-to-Back Capable..... always reads 0

6 User Definable Features ..... always reads 0

5 66MHz Capable..... always reads 0

4 Supports New Capability list ..... always reads 1

3-0 Reserved ..... always reads 0

Device 0 Offset 8 - Revision ID (0nh).....RO

7-0 Chip Revision Code ...always reads 0nh (n=rev code)

Device 0 Offset 9 - Programming Interface (00h) .....RO

7-0 Interface Identifier..... always reads 00

Device 0 Offset A - Sub Class Code (00h) .....RO

7-0 Sub Class Code..... reads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code (06h) .....RO

7-0 Base Class Code... reads 06 to indicate Bridge Device

Device 0 Host Bridge Header Registers (continued)

Device 0 Offset D - Latency Timer (00h)..... RW

Specifies the latency timer value in PCI bus clocks.

7-3 **Guaranteed Time Slice for CPU**..... default=0

2-0 **Reserved** (fixed granularity of 8 clks) ....always read 0
Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Offset 75 bits 5-4 (PCI Arbitration 1).

Device 0 Offset E - Header Type (00h) ..... RO

7-0 **Header Type Code** ..... reads 00: single function

Device 0 Offset F - Built In Self Test (BIST) (00h)..... RO

7 **BIST Supported** ..... reads 0: no supported functions

6-0 **Reserved** ..... always reads 0

Device 0 Offset 13-10 - Graphics Aperture Base (AGP 2.0) (00000008h) ..... RW

This register is interpreted per the following definition if RxFD[1]=1 (AGP 2.0 registers enabled).

31-28 **Upper Programmable Base Address Bits** ..... def=0

27-20 **Lower Programmable Base Address Bits**..... def=0
These bits behave as if hardwired to 0 if the corresponding AGP 2.0 Graphics Aperture Size register bit (Device 0 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(Base)
7	6	5	4	3	2	1	0	(Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-4 **Reserved** ..... always reads 0

3 **Prefetchable** **always reads 1**
Indicates that the locations in the address range defined by this register are prefetchable.

2-1 **Type** ..... always reads 0
Indicates the address range in the 32-bit address space.

0 **Memory Space**..... always reads 0
Indicates the address range in the memory address space.

Device 0 Offset 13-10 - Graphics Aperture Base (AGP 3.0) (00000008h) .....RW

This register is interpreted per the following definition if RxFD[1]=0 (AGP 3.0 registers enabled). This register may only be read if AGP 3.0 register Rx90[8] = 1.

31-22 **Programmable Base Address Bits**..... def=0
These bits behave as if hardwired to 0 if the corresponding AGP 3.0 Graphics Aperture Size register bit (Device 0 Offset 94h) is 0.

31	30	29	28	-	-	27	26	25	24	23	22	(Base)
11	10	9	8	7	6	5	4	3	2	1	0	(Size)
RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	RW	4M
RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	0	8M
RW	RW	RW	RW	0	0	RW	RW	RW	RW	0	0	16M
RW	RW	RW	RW	0	0	RW	RW	RW	0	0	0	32M
RW	RW	RW	RW	0	0	RW	RW	0	0	0	0	64M
RW	RW	RW	RW	0	0	RW	0	0	0	0	0	128M
RW	RW	RW	RW	0	0	0	0	0	0	0	0	256M
RW	RW	RW	0	0	0	0	0	0	0	0	0	512M
RW	RW	0	0	0	0	0	0	0	0	0	0	1G
RW	0	0	0	0	0	0	0	0	0	0	0	2G-max
0	0	0	0	0	0	0	0	0	0	0	0	4G

21-4 **Reserved** ..... always reads 0

3 **Prefetchable** **always reads 1**
Indicates that the locations in the address range defined by this register are prefetchable.

2-1 **Type** ..... always reads 0
Indicates the address range in the 32-bit address space.

0 **Memory Space**..... always reads 0
Indicates the address range in the memory address space.

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h) W1/R

15-0 **Subsystem Vendor ID**..... default = 0

This register may be written once and is then read only.

Device 0 Offset 2F-2E – Subsystem ID (0000h) W1/R

15-0 **Subsystem ID**..... default = 0

This register may be written once and is then read only.

Device 0 Offset 34 - Capability Pointer (CAPPTR) .....RO

Contains an offset from the start of configuration space.

7-0 **AGP Capability List Pointer**..... always reads A0h

Device 0 Configuration Registers - Host Bridge

These registers are normally programmed once at system initialization time.

V-Link Registers

Device 0 Offset 40 – V-Link Specification ID (00h)..... RO

7-0 Specification Revision ..... always reads 00

Device 0 Offset 41 – NB V-Link Capability (19h)..... RO

7 V-Link Parity Error Detected by NB ..... RO
- 0 No V-Link parity error detected ..... default
- 1 V-Link parity error detected

6 Reserved ..... always reads 0

5 16-bit Bus Width Supported ..... RO
- 0 Not Supported ..... default
- 1 Supported

4 8-Bit Bus Width Supported..... RO
- 0 Not Supported
- 1 Supported ..... default

3 4x Rate Supported..... RO
- 0 Not Supported
- 1 Supported ..... default

2 2x Rate Supported..... RO
- 0 Not Supported ..... default
- 1 Supported

1 Reserved ..... always reads 0

0 8x Rate Supported..... RO
- 0 Not Supported
- 1 Supported **..... default**

Device 0 Offset 42 – NB Downlink Command (88h)..... RW

7-4 DnCmd Max Request Depth (0=1 DnCmd)... def = 8

3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Device 0 Offset 44-43 – NB Uplink Status (8280h) ..... RO

15-12 UpCmd P2C Write Buffer Size (max lines)... def = 8

11-8 UpCmd P2P Write Buffer Size (max lines)... def = 2

7-4 UpCmd Max Request Depth (0=1 UpCmd)... def = 8

3-0 Reserved ..... always reads 0

Device 0 Offset 45 –NB V-Link Bus Timer (44h) .....RW

7-4 Timer for Normal Priority Requests from SB
- 0000 Immediate
- 0001 1*4 VCLKs
- 0010 2*4 VCLKs
- 0011 3*4 VCLKs
- 0100 4*4 VCLKs .....default
- 0101 5*4 VCLKs
- 0110 6*4 VCLKs
- 0111 7*4 VCLKs
- 1000 8*4 VCLKs
- 1001 16*4 VCLKs
- 1010 32*4 VCLKs
- 1011 64*4 VCLKs
- 11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from SB
- 0000 Immediate
- 0001 1*2 VCLKs
- 0010 2*2 VCLKs
- 0011 3*2 VCLKs
- 0100 4*2 VCLKs .....default
- 0101 5*2 VCLKs
- 0110 6*2 VCLKs
- 0111 7*2 VCLKs
- 1000 8*2 VCLKs
- 1001 16*2 VCLKs
- 1010 32*2 VCLKs
- 1011 64*2 VCLKs
- 11xx Own the bus for as long as there is a request

Device 0 Offset 46 – NB V-Link Misc Control (00h) ..... RW

7 Downstream High Priority
- 0 Disable High Priority Down Commands..... def
- 1 Enable High Priority Down Commands

6 Downlink Priority
- 0 Treat Downlink Cycles as Normal Priority . def
- 1 Treat Downlink Cycles as High Priority

5-4 Combine Multiple STPGNT Cycles into One V-Link Command
- 00 Compatible, 1 command per V-Link cmd .... def
- 01 2 commands per V-Link command
- 10 3 commands per V-Link command
- 11 4 commands per V-Link command

3-2 V-Link Master Access Ordering Rules
- 00 High priority read, pass normal read (not pass write) ..... default
- 01 Read (high/normal) pass write (HR>LR>W)
- 1x Read / write in order

1 Reserved ..... always reads 0

0 Ready Queue Full Performance
- 0 Full Performance ..... default
- 1 Backwards Compatible

Device 0 Offset 47 – V-Link Control (00h)..... RW

7 Parity Error or SERR Reporting to NMI
- 0 Disable..... default
- 1 Enable

6 Parity Error or SERR Reporting to SB via V-Link
- 0 Disable..... default
- 1 Enable

5 L1 Ready Return
- 0 When C2P read acknowledgement is received ..... default
- 1 After previous P2C write data is flushed

4 Reserved ..... always reads 0

3 Dynamic Stop of Down Strobe
- 0 Disable..... default
- 1 Enable

2 Auto-Disconnect
- 0 Disable..... default
- 1 Enable

1 V-Link Disconnect Cycle for HALT cycle
- 0 Disable..... default
- 1 Enable

0 V-Link Disconnect Cycle for STPGNT Cycle
- 0 Disable..... default
- 1 Enable

Device 0 Offset 48 – NB/SB V-Link Configuration (18h)RW

7 V-Link Parity Check
- 0 Disable.....default
- 1 Enable

6 Rest Bus Width Support
- 0 Not Supported .....default
- 1 Supported

5 16-bit Bus Width Support
- 0 Disable.....default
- 1 Enable

4 8-Bit Bus Width Support
- 0 Disable
- 1 Enable..... **default**

3 4x Rate Support
- 0 Disable
- 1 Enable..... **default**

2 2x Rate Support
- 0 Disable.....default
- 1 Enable

1 Reserved ..... always reads 0

0 8x Rate Support
- 0 Disable.....default
- 1 Enable

Device 0 Offset 49 – SB V-Link Capability (19h).....RO

7 V-Link Parity Error Detected by SB .....RO
- 0 No V-Link parity error detected .....default
- 1 V-Link parity error detected

6 Reserved ..... always reads 0

5 16-bit Bus Width Supported .....RO
- 0 Not Supported .....default
- 1 Supported

4 8-Bit Bus Width Supported.....RO
- 0 Not Supported
- 1 Supported ..... **default**

3 4x Rate Supported.....RO
- 0 Not Supported
- 1 Supported ..... **default**

2 2x Rate Supported.....RO
- 0 Not Supported .....default
- 1 Supported

1 Reserved ..... always reads 0

0 8x Rate Supported.....RO
- 0 Not Supported
- 1 Supported ..... **default**

Device 0 Offset 4A – SB Downlink Status (88h) .....RO

7-4 DnCmd Max Request Depth (0=1 DnCmd)... def = 8

3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Device 0 Offset 4C-4B – SB Uplink Command (8280h)..RW

15-12 UpCmd P2C Write Buffer Size (max lines)... def = 8

11-8 UpCmd P2P Write Buffer Size (max lines)... def = 2

7-4 UpCmd Max Request Depth (0=1 UpCmd)... def = 8

3-0 Reserved ..... always reads 0

Device 0 Offset 4D – SB V-Link Bus Timer (44h) ..... RW

7-4 Timer for Normal Priority Requests from NB

0000 Immediate
0001 1*4 VCLKs
0010 2*4 VCLKs
0011 3*4 VCLKs
0100 4*4 VCLKs..... default
0101 5*4 VCLKs
0110 6*4 VCLKs
0111 7*4 VCLKs
1000 8*4 VCLKs
1001 16*4 VCLKs
1010 32*4 VCLKs
1011 64*4 VCLKs
11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from NB

0000 Immediate
0001 1*2 VCLKs
0010 2*2 VCLKs
0011 3*2 VCLKs
0100 4*2 VCLKs..... default
0101 5*2 VCLKs
0110 6*2 VCLKs
0111 7*2 VCLKs
1000 8*2 VCLKs
1001 16*2 VCLKs
1010 32*2 VCLKs
1011 64*2 VCLKs
11xx Own the bus for as long as there is a request

Device 0 Offset 4E – CCA Master Priority (00h) .....RW

7 1394 High Priority
0 Low priority.....default
1 High priority

6 LAN / NIC High Priority
0 Low priority.....default
1 High priority

5 Reserved ..... always reads 0

4 USB High Priority
0 Low priority.....default
1 High priority

3 Reserved ..... always reads 0

2 IDE High Priority
0 Low priority.....default
1 High priority

1 AC97-ISA High Priority
0 Low priority.....default
1 High priority

0 PCI High Priority
0 Low priority.....default
1 High priority

Device 0 Offset 4F – SB V-Link Misc Control (00h).....RW

7 Upstream Command High Priority
0 Disable high priority up commands .....default
1 Enable high priority up commands

6-1 Reserved ..... always reads 0

0 Down Cycle Wait for Up Cycle Write Flush (Except Down Cycle Post Write)
0 Disable.....default
1 Enable

Device 0 Offset 50 – S2K Duty Cycle Adjust 1 (08h)..... RW

7-6 S2K Data In Rise Control
- 00 Normal Rise Delay ..... default
- 01 Delay Rise by 70 ps
- 10 Delay Rise by 135 ps
- 11 Delay Rise by 300 ps

5-4 S2K Data In Fall Control
- 00 Normal Fall Delay ..... default
- 01 Delay Fall by 70 ps
- 10 Delay Fall by 135 ps
- 11 Delay Fall by 300 ps

3-2 S2K Data In Clock-to-Data In Delay
- 00 Data In Clock Earlier by 300 ps
- 01 Data In Clock Earlier by 150 ps
- 10 DataInClk & DataIn have same delay**.... default**
- 11 DataInClk Later than DataIn by 150 ps

1-0 Reserved ..... always reads 0

Device 0 Offset 51 – S2K Duty Cycle Adjust 2 (00h)..... RW

7-6 S2K Data In Clock Output Rise Control
- 00 Normal Rise Delay ..... default
- 01 Delay Rise by 70 ps
- 10 Delay Rise by 135 ps
- 11 Delay Rise by 300 ps

5-4 S2K Data In Clock Output Fall Control
- 00 Normal Fall Delay ..... default
- 01 Delay Fall by 70 ps
- 10 Delay Fall by 135 ps
- 11 Delay Fall by 300 ps

3-2 S2K Data Out Clock Input Rise Control
- 00 Normal Rise Delay ..... default
- 01 Delay Rise by 70 ps
- 10 Delay Rise by 135 ps
- 11 Delay Rise by 300 ps

1-0 S2K Data Out Clock Input Fall Control
- 00 Normal Fall Delay ..... default
- 01 Delay Fall by 70 ps
- 10 Delay Fall by 135 ps
- 11 Delay Fall by 300 ps

Device 0 Offset 52 – S2K Duty Cycle Adjust 3 (00h) .....RW

7-6 S2K Address Out Clock Input Rise Control
- 00 Normal Rise Delay .....default
- 01 Delay Rise by 70 ps
- 10 Delay Rise by 135 ps
- 11 Delay Rise by 300 ps

5-4 S2K Address Out Clock Input Fall Control
- 00 Normal Fall Delay .....default
- 01 Delay Fall by 70 ps
- 10 Delay Fall by 135 ps
- 11 Delay Fall by 300 ps

3-2 S2K Address In Rise Control
- 00 Normal Rise Delay .....default
- 01 Delay Rise by 70 ps
- 10 Delay Rise by 135 ps
- 11 Delay Rise by 300 ps

1-0 S2K Address In Fall Control
- 00 Normal Fall Delay .....default
- 01 Delay Fall by 70 ps
- 10 Delay Fall by 135 ps
- 11 Delay Fall by 300 ps

Device 0 Offset 53 – S2K Duty Cycle Adjust 4 (80h) .....RW

7-6 S2K Address In Clock-to-Address In Delay
- 00 Address In Clock Earlier by 300 ps
- 01 Address In Clock Earlier by 150 ps
- 10 AddrInClk & AddrIn have same delay**.. default**
- 11 AddrInClk Later than AddrIn by 150 ps

5-4 Reserved ..... always reads 0

3-2 S2K Address In Clock Output Rise Control
- 00 Normal Rise Delay .....default
- 01 Delay Rise by 70 ps
- 10 Delay Rise by 135 ps
- 11 Delay Rise by 300 ps

1-0 S2K Address In Clock Output Fall Control
- 00 Normal Fall Delay .....default
- 01 Delay Fall by 70 ps
- 10 Delay Fall by 135 ps
- 11 Delay Fall by 300 ps

Device 0 Offset 54 – CPU Frequency Select (x0h) ..... RW

7-6 CPU FSB Frequency Select..... RO
.....Set by Straps VAD6 and VAD4
Default set from South Bridge SDA2 and SDA0 pins communicated to the KT600 via VAD6 and VAD4.
00 100 MHz
01 133 MHz
10 200 MHz
11 166 MHz

5 ROMSIP Configuration ....RO, Set by Strap VAD5
0 Disable (config per MA / SCASA / SWEA straps)
1 Enable (configure per ROMSIP)

4 DRAM Burst Length 8QW
0 Disable..... default
1 Enable

1 Reserved (Do Not Program)..... default = 0

2 PCI Master 8QW Operation
0 Disable..... default
1 Enable

1 Reserved (Do Not Program)..... default = 0

0 VPX Mode
0 AGP Mode..... default
1 VPX Mode

DRAM Registers

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies VT8633 BIOS porting guide for details).

Table 5. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys Bus Init	1MB D Top 4G-64K	—	00100000-DRAM Top DRAM Top-FFFEFFFF FFFEFFFF-FFFFFFFF	Can have hole 000Fxxxx alias

Device 0 Offset 55 – DRAM Control (00h).....RW

7 0WS Back-to-Back Write to Different DDR Bank
- 0 Disable.....default
- 1 Enable

6 Fast Read-to-Read Turn-Around
(DQS postamble overlap with preamble)
- 0 Disable.....default
- 1 Enable

5 DQS Input DLL Adjustment
- 0 Disable.....default
- 1 Enable

4 DQS Output DLL Adjustment
- 0 Disable.....default
- 1 Enable

3 DQM Removal (Always Perform 4-Burst RW)
- 0 Disable.....default
- 1 Enable

2 DQS Output
- 0 Disable.....default
- 1 Enable

1 Auto Precharge for TLB Read or CPU WriteBack
- 0 Disable.....default
- 1 Enable

0 Write Recovery Time

	DDR333	DDR400	
0	2T	3T	.....default
1	3T	5T	

Device 0 Offset 59-58 - DRAM MA Map Type (2222h). RW

15-13 Bank 5/4 MA Map Type (see table below)
12 Bank 5/4 1T Command Rate
0 2T Command..... default
1 1T Command
11-9 Bank 7/6 MA Map Type (see table below)
8 Bank 7/6 1T Command Rate
0 2T Command..... default
1 1T Command
7-5 Bank 1/0 MA Map Type (see table below)
4 Bank 1/0 1T Command Rate
0 2T Command..... default
1 1T Command
3-1 Bank 3/2 MA Map Type (see table below)
0 Bank 3/2 1T Command Rate
0 2T Command..... default
1 1T Command

Table 6. MA Map Type Encoding

000	16Mb	8-bit, 9-bit, 10-bit Column Address
001	64/128Mb	8/9-bit Column Address..... default
010	64/128Mb	9/10-bit Column Address
011	64/128Mb	10/11-bit Column Address
100	1Gb	10/11/12-bit Column Address
101	256/512Mb	8-bit Column Address
110	256/512Mb	9-bit Column Address
111	256/512Mb	10/11/12-bit Column Address

Device 0 Offset 5F-5A – DRAM Row Ending Address:

Offset 5A – Bank 0 Ending (HA[31:24]) (01h).....RW
Offset 5B – Bank 1 Ending (HA[31:24]) (01h).....RW
Offset 5C – Bank 2 Ending (HA[31:24]) (01h).....RW
Offset 5D – Bank 3 Ending (HA[31:24]) (01h).....RW
Offset 5E – Bank 4 Ending (HA[31:24]) (01h).....RW
Offset 5F – Bank 5 Ending (HA[31:24]) (01h).....RW
Offset 56 – Bank 6 Ending (HA[31:24]) (01h) .....RW
Offset 57 – Bank 7 Ending (HA[31:24]) (01h) .....RW

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Table 7. Memory Address Mapping Table

MA:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
16Mb (000)			24		13	12	11	14	22	21	20	19	18	17	16	15	12 row
					13	PC	24	23	10	9	8	7	6	5	4	3	10,9,8 col
64/128Mb																	
2K page		14	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (14,8)
001			27	14	13	PC	26	25	10	9	8	7	6	5	4	3	x16 (14,8)
4K page		14	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (14,9)
010			27	14	131	PC	26	11	10	9	8	7	6	5	4	3	x8 (14,9)
8K page		14	26	14	3	25	24	23	22	21	20	19	18	17	16	15	x8 (14,10)
011			27	14	13	PC	12	11	10	9	8	7	6	5	4	3	x4 (14,10)
																	x4 (14,11)
256/512Mb																	
2K page		25	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (15,8)
101			27	14	13	PC	26	25	10	9	8	7	6	5	4	3	
4K page		26	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x32 (15,9)
110			27	14	13	PC	26	11	10	9	8	7	6	5	4	3	x16 (15,9)
8K page		27	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x16 (15,10)
111		29	28	14	13	PC	12	11	10	9	8	7	6	5	4	3	x8 (15,10)
																	x8 (15,11)
																	x4 (15,11)
																	x4 (15,12)
1Gb																	
8K page	28	27	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x16 (16,10)
100	31	30	29	14	13	PC	12	11	10	9	8	7	6	5	4	3	x8 (16,11)
																	x4 (16,12)

Device 0 Offset 60 - DRAM Fast Precharge Control (00h)RW

7-6 Precharge Command to Active Command Period
- 00 TRP = 2T ..... default
- 01 TRP = 3T
- 10 TRP = 4T
- 11 TRP = 5T

5 Use Address Bit-14=0 & Bit-19=1 as Sub Bank Select 1
- 0 Disable..... default
- 1 Enable

4 Use Address Bit-13=0 & Bit-18=1 as Sub Bank Select 0
- 0 Disable..... default
- 1 Enable

3 Reserved ..... always reads 0

2 Increase TFRC For 1Gbit DRAMs
- 0 Disable..... default
- 1 Enable

1-0 TFRC

	Bit-2=0	Bit-2=1	
00	12T	21T	..... default
01	13T	22T	
10	14T	23T	
11	15T	24T	

Device 0 Offset 61 - Shadow RAM Control 1 (00h)..... RW

7-6 CC000h-CFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 C8000h-CBFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 C4000h-C7FFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 C0000h-C3FFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2 (00h) .....RW

7-6 DC000h-DFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 D8000h-DBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 D4000h-D7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 D0000h-D3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3 (00h) .....RW

7-6 E0000h-EFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 F0000h-FFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 Memory Hole
- 00 None .....default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

1-0 SMI Mapping Control
(Bit-1 = A,BK Direct Access SMRAM Disable)
(Bit-0 = A,BK DRAM Access Enable)

	SMM		Non-SMM	
	Code	Data	Code	Data
00	DRAM	DRAM	PCI	PCI
01	DRAM	DRAM	DRAM	DRAM
10	DRAM	PCI	PCI	PCI
11	DRAM	DRAM	DRAM	DRAM

Device 0 Offset 64 - DRAM Timing for All Banks (64h) RW

7-6 Active Command to Precharge Command Period
- 00 TRAS = 6T
- 01 TRAS = 7T ..... **default**
- 10 TRAS = 8T
- 11 TRAS = 9T

5-4 CAS Latency
- 00 1.5T
- 01 2T
- 10 2.5T ..... **default**
- 11 3T

3-2 ACTIVE to CMD
- 00 TRCD = 2T
- 01 TRCD = 3T ..... **default**
- 10 TRCD = 4T
- 11 TRCD = 5T

1-0 Bank Interleave
- 00 No Interleave ..... default
- 01 2-way
- 10 4-way
- 11 Reserved

For 16Mb DRAMs, bank interleave is always 2-way

Device 0 Offset 65 - DRAM Arbitration Timer (00h) .... RW

7-4 AGP Timer (units of 4 MCLKs)..... default = 0

3-0 CPU Timer (units of 4 MCLKs)..... default = 0

Device 0 Offset 66 - DRAM Arbitration Control (00h).. RW

7 SDR – Feedback Clock Select
DDR - DQS Input Delay Setting
- 0 Auto (Rx67 reads DLL calibration result).... def
- 1 Manual (Rx67 reads DQS input delay)

6 DRAM Access
- 0 2T ..... default
- 1 3T

5-4 Arbitration Parking Policy
- 00 Park at last bus owner..... default
- 01 Park at CPU
- 10 Park at AGP
- 11 -reserved-

3-0 AGP / CPU Priority (units of 4 MCLKs)

Device 0 Offset 67 – DDR Strobe Input Delay (00h) ..... RW

7 DRAM Operating Frequency (See also Rx69[7-6]
- 0 DRAM same as or faster than CPU..... default
- 1 DRAM slower than CPU by 33 or 66 MHz

6 Reserved ..... always reads 0

5-0 DQS Input Delay ..... default = 0
(if Rx66[7]=0, read DLL calibration result)

Device 0 Offset 68 – DDR Strobe Output Delay (00h) ... RW

7-0 DDR DQS Output Delay ..... default = 0

Device 0 Offset 69 – DRAM Clock Select (00h) .....RW

7 DRAM Operating Frequency
- 0 DRAM / CPU freq difference 0 or 33 .....default
- 1 DRAM / CPU freq difference 66 MHz

6 DRAM Operating Frequency Faster Than CPU
- 0 DRAM same as or slower than CPU.....default
- 1 DRAM faster than CPU by 33 or 66 MHz

Bits 7-6	Rx67 Bit-7	CPU Frequency	DRAM Frequency
00	0	133	133
	0	166	166
	0	200	200
01	0	100	133
	0	133	166
	0	166	200
10	0	-reserved-	-reserved-
11	0	133	200
00	1	166	133
00	1	200	166
10	1	200	133
x1	1	-reserved-	-reserved-

5 DRAM Queue More Than 2
- 0 Disable.....default
- 1 Enable

4 DRAM Queue Not Equal to 4
- 0 Disable.....default
- 1 Enable

3 DRAM 8K Page Enable
- 0 Disable.....default
- 1 Enable

2 DRAM 4K Page Enable
- 0 Disable.....default
- 1 Enable

1 DIMM Type
- 0 Unbuffered .....default
- 1 Registered

0 Multiple Page Mode
- 0 Disable.....default
- 1 Enable

Device 0 Offset 6A - Refresh Counter (00h).....RW

7-0 Refresh Counter (in units of 16 MCLKs)
- 00 DRAM Refresh Disabled .....default
- 01 32 MCLKs
- 02 48 MCLKs
- 03 64 MCLKs
- 04 80 MCLKs
- 05 96 MCLKs
- … …

The programmed value is the desired number of 16-MCLK units minus one.

Device 0 Offset 6B - DRAM Arbitration Control (10h). RW

7 Fast Read to Write turn-around
- 0 Disable..... default
- 1 Enable

6 Page Kept Active When Cross Bank
- 0 Disable..... default
- 1 Enable

5 Burst Refresh
- 0 Disable..... default
- 1 Enable

4 Reserved ..... always reads 0

3 Swap CA22 / CA14
- 0 Disable..... default
- 1 Enable

2-0 DRAM Operation Mode Select
- 000 Normal Synchronous DRAM Mode..... default
- 001 NOP Command Enable
- 010 All-Banks-Precharge Command Enable (CPU-to-DRAM cycles are converted to All-Banks-Precharge commands).
- 011 MSR Enable CPU-to-DRAM cycles are converted to commands and the commands are driven on MA[14:0]. The BIOS selects an appropriate host address for each row of memory such that the right commands are generated on MA[14:0].
- 100 CBR Cycle Enable (if this code is selected, CAS-before-RAS refresh is used; if it is not selected, RAS-Only refresh is used)
- 101 Reserved
- 11x Reserved

Device 0 Offset 6C – DRAM Drive Control (00h) .....RW

7-6 CS# / CKE Early Clock Select
- 00 Latest .....default
- 01
- 10
- 11 Earliest

5-4 SCMD / MA Early Clock Select (for 1T Command)
- 00 Latest .....default
- 01
- 10
- 11 Earliest

3-2 Rank Interleaver Setting
- 00 15 .....default
- 01 17
- 10 20
- 11 21

1 Rank Interleaver
- 0 Disable.....default
- 1 Enable

0 DDR400 T_{WTR} Timing Control
- 0 1T .....default
- 1 2T

Device 0 Offset 6D – DRAM MD Output Delay (00h)....RW

7-0 MD Output Delay..... default = 00h

Note: Refer to the BIOS Developers Guide for recommended memory configuration detection algorithms and recommended settings for the bits of the above registers.

Device 0 Offset 6E - ECC Control (00h)..... RW

7 ECC / EC Mode Select
- 0 ECC Checking and Reporting..... default
- 1 ECC Checking, Reporting, and Correcting

6 Reserved ..... always reads 0

5 Enable SERR# on ECC / EC Multi-Bit Error
- 0 Don't assert SERR# for multi-bit errors..... def
- 1 Assert SERR# for multi-bit errors

4 Enable SERR# on ECC / EC Single-Bit Error
- 0 Don't assert SERR# for single-bit errors ..... def
- 1 Assert SERR# for single-bit errors

3 ECC / EC Enable - Bank 7/6 (DIMM 3)
- 0 Disable (no ECC or EC for banks 7/6)... default
- 1 Enable (ECC or EC per bit-7)

2 ECC / EC Enable - Bank 5/4 (DIMM 2)
- 0 Disable (no ECC or EC for banks 5/4)... default
- 1 Enable (ECC or EC per bit-7)

1 ECC / EC Enable - Bank 3/2 (DIMM 1)
- 0 Disable (no ECC or EC for banks 3/2)... default
- 1 Enable (ECC or EC per bit-7)

0 ECC / EC Enable - Bank 1/0 (DIMM 0)
- 0 Disable (no ECC or EC for banks 1/0)... default
- 1 Enable (ECC or EC per bit-7)

Error checking / correction may be enabled bank-pair by bank-pair (DIMM by DIMM) by using bits 0-2 above. Bank pairs must be populated with 72-bit memory to enable for EC or ECC since the additional data bits must be present in either case. For this reason, if 64-bit memory is populated in a particular bank pair, the corresponding bit 0-2 should be set to 0 to disable both EC and ECC for that bank pair. For those bank pairs that have 72-bit memory available (and have the corresponding bit 0-2 set), either EC or ECC may be selected via bit-7 above (i.e., all enabled bank pairs will use EC or all will use ECC).

If error checking / reporting only (EC) is selected, all read and write cycles will use normal timing. Partial writes (with EC or ECC enabled) will use read-modify-write cycles to maintain correct error correction codes in the additional 8 data bits. If EC and ECC are disabled for a particular bank pair, partial writes to that bank pair will use the byte enables to write only the selected bytes (using normal write cycles and cycle timing). If error correction (ECC) is selected, the first read of a transaction will always have one additional cycle of latency.

Bit-7	Bits 2-0	RMW	Error Checking	Error Correction
0/1	0	No	No	No
0	1	Yes	Yes	No
1	1	Yes	Yes	Yes

Device 0 Offset 6F - ECC Status (00h) .....RWC

7 Multi-bit Error Detected ..... write of '1' resets

6-4 Multi-bit Error DRAM Bank ..... default=0
Encoded value of the bank with the multi-bit error.

3 Single-bit Error Detected ..... write of '1' resets

2-0 Single-bit Error DRAM Bank ..... default=0
Encoded value of the bank with the single-bit error.

Host PCI Bridge Registers

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer Control (00h)..... RW

7 CPU to PCI Post-Write
- 0 Disable..... default
- 1 Enable

6 Reserved ..... always reads 0

5-4 PCI Master to DRAM Prefetch Control
- 00 Always Prefetch..... default
- x1 Never Prefetch
- 10 Prefetch only for enhance command

3 Reserved ..... always reads 0

2 PCI Master Read Buffering
- 0 Disable..... default
- 1 Enable

1 Delay Transaction
- 0 Disable..... default
- 1 Enable

0 Reserved ..... always reads 0

Device 0 Offset 71 - CPU to PCI Flow Control (48h).....RW

7 Retry Status
- 0 No retry occurred.....default
- 1 Retry occurred

6 Retry Timeout Action
- 0 Retry forever (record status only)
- 1 Flush buffer or return FFFFFFFF for read ... def

5-4 Retry Count and Retry Backoff
- 00 Retry 2 times, Boff CPU .....default
- 01 Retry 16 times
- 10 Retry 4 times
- 11 Retry 64 times

3 PCI Burst
- 0 Disable
- 1 Enable.....default

2 Reserved ..... always reads 0

1 Configuration Cycle
- 0 Fix AD31.....default
- 1 Compatible Type #1 AD31

0 IDSEL Control
- 0 AD11 / AD12 .....default
- 1 AD30 / AD31

Device 0 Offset 73 - PCI Master Control (00h)..... RW

7 Reserved ..... always reads 0

6 PCI Master 1-Wait-State Write
- 0 Zero wait state TRDY# response ..... default
- 1 One wait state TRDY# response

5 PCI Master 1-Wait-State Read
- 0 Zero wait state TRDY# response ..... default
- 1 One wait state TRDY# response

4 WSC#
- 0 Disable..... default
- 1 Enable

3-1 Reserved ..... always reads 0

0 PCI Master Broken Timer Enable
- 0 Disable..... default
- 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Device 0 Offset 75 - PCI Arbitration 1 (00h)..... RW

7 Arbitration Mode
- 0 REQ-based (arbitrate at end of REQ#)... default
- 1 Frame-based (arbitrate at FRAME# assertion)

6-4 CPU Latency

3 Reserved ..... always reads 0

2-0 PCI Master Bus Time-Out
(force into arbitration after a period of time)
- 000 Disable..... default
- 001 1x16 PCICLKs
- 010 2x16 PCICLKs
- 011 3x16 PCICLKs
- 100 4x16 PCICLKs
- ... ...
- 111 7x16 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2 (00h) .....RW

7 I/O Port 22 Enable
- 0 CPU access to I/O address 22h is passed on to the PCI bus .....default
- 1 CPU access to I/O port 22h is processed by internal I/O

6 Reserved ..... always reads 0

5-4 Master Priority Rotation Control
- 00 Disable..... def
- 01 Grant to CPU after every PCI master grant
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

With setting 01, the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting. With setting 10, if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes. With setting 11, if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus. In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

3-2 REQn# to REQ4# Mapping
- 00 REQ4#
- 01 REQ0#
- 10 REQ1#
- 11 REQ2#

1 Reserved ..... always reads 0

0 REQ4# Master Priority
- 0 Normal.....default
- 1 High

GART / Graphics Aperture

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the KT600.

This scheme is shown in the figure below.

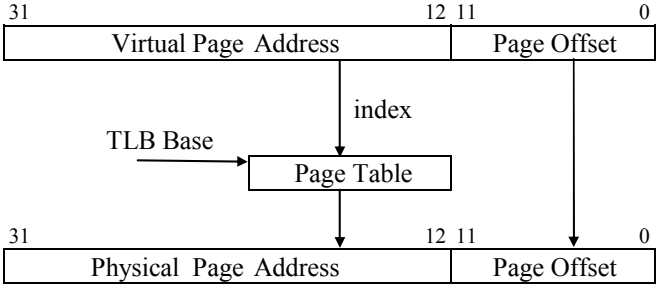


Figure 5. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the KT600 contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc) for AGP 2.0 and 4MB to 2GB for AGP 3.0. The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register groups (Rx84 and 88 respectively for AGP 2.0 and Rx94 and 98 for AGP 3.0) along with various control bits.

AGP 2.0 Registers

AGP 2.0 registers Rx80-AB are enabled if RxFD[1] = 1 and AGP 3.0 registers Rx80-AB are enabled if RxFD[1] = 0.

Device 0 Offset 83-80 – AGP 2.0 GART/TLB Control... RW

31-16 Reserved ..... always reads 0
15-8 Reserved (test mode status) ..... RO
7 Flush Page TLB
0 Disable..... default
1 Enable
6-0 Reserved (always program to 0) ..... RW

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 – AGP 2.0 Graphics Aperture Size... RW

7-0 Graphics Aperture Size

11111111	1M
11111110	2M
11111100	4M
11111000	8M
11110000	16M
11100000	32M
11000000	64M
10000000	128M
00000000	256M

Offset 8B-88 – AGP 2.0 GART Table Base..... RW

31-12 Graphics Aperture Translation Table Base. Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).
11-2 Reserved ..... always reads 0
1 Graphics Aperture
0 Disable..... default
1 Enable
Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.
0 Reserved ..... always reads 0

Device 0 Offset A3-A0 - AGP 2.0 Capabilities (0020C002h) ..... RO

31-24 Reserved ..... always reads 00
23-20 Major Specification Revision .... always reads 0010b
Major rev # of AGP spec that device conforms to
19-16 Minor Specification Revision .... always reads 0000b
Minor rev # of AGP spec that device conforms to
15-8 Pointer to Next Item..... always reads C0 (last item)
7-0 AGP Capability ID
(always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP 2.0 Status (1F000201h) .....RO

31-24 Maximum AGP Requests..... always reads 1Fh
Max # of AGP requests the device can manage (32)
23-10 Reserved ..... always reads 0s
9 Supports SideBand Addressing..... **always reads 1**
8-6 Reserved ..... always reads 0s
5 Addresses Above 4G Supported ..... always reads 0†
4 Fast Write Supported ..... always reads 0†
3 Reserved ..... always reads 0s
2 4X Rate Supported..... always reads 0†
1 2X Rate Supported..... always reads 0†
0 1X Rate Supported..... **always reads 1**

†Writable if RxFD[0] = 1.

Device 0 Offset AB-A8 - AGP 2.0 Command.....RW

31-24 Request Depth (reserved for target)....always reads 0s
23-10 Reserved ..... always reads 0s
9 SideBand Addressing Enable
0 Disable..... default
1 Enable
8 AGP Enable
0 Disable..... default
1 Enable
7-6 Reserved ..... always reads 0s
5 4G Enable
0 Disable..... default
1 Enable
4 Fast Write Enable
0 Disable..... default
1 Enable
3 Reserved ..... always reads 0s
2 4X Mode Enable
0 Disable..... default
1 Enable
1 2X Mode Enable
0 Disable..... default
1 Enable
0 1X Mode Enable
0 Disable..... default
1 Enable

AGP 3.0 Registers

AGP 3.0 registers Rx80-AB are enabled if RxFD[1] = 0 and AGP 2.0 registers Rx80-AB are enabled if RxFD[1] = 1.

Device 0 Offset 83-80 - AGP 3.0 Capabilities (0030C002h) ..... RO

31-24 **Reserved** ..... always reads 00
23-20 **Major Specification Revision** .... always reads 0011b
Major rev # of AGP spec that device conforms to
19-16 **Minor Specification Revision** .... always reads 0000b
Minor rev # of AGP spec that device conforms to
15-8 **Pointer to Next Item** ..... always reads C0 (last item)
7-0 **AGP Capability ID**
(always reads 02 to indicate it is AGP)

Device 0 Offset 87-84 - AGP 3.0 Status (1F000201h) ..... RO

31-24 **Maximum AGP Requests** ..... always reads 1Fh
Max # of AGP requests the device can manage (32)
23-16 **Reserved** ..... always reads 0s†
15-13 **Optimum Async Request Size** ..... always reads 0s†
Suggested setting is 010b or 2^(2+4)=64 Bytes for 8QW access
12-10 **Calibration Cycle Setting**
000 4 ms
001 16 ms
010 64 ms ..... **default†**
011 256 ms
9 **Supports SideBand Addressing** ..... **always reads 1**
8 **Reserved** ..... always reads 0†
7 **64-Bit GART Entries** ..... always reads 0
6 **CPU GART Translation Supported** .. always reads 0
5 **Addresses Above 4G Supported** ..... always reads 0
4 **Fast Write Supported** ..... always reads 0
3 **AGP 8x Detected** ..... Set from AGP8XDT# pin
2 **4X Rate Supported** ..... Reads 0 if bit-3 = 1
..... Reads 1 if bit-3 = 0
1 **2X Rate Supported** ..... **always reads 1**
0 **1X Rate Supported** ..... **always reads 1**

†Writable if RxFD[0] = 1.

Device 0 Offset 8B-88 - AGP 3.0 Command .....RW

31-24 **Request Depth** (reserved for target).... always reads 0s
23-13 **Reserved** ..... always reads 0s
12-10 **Calibration Cycle Select** ..... default = 0
9 **SideBand Addressing**
0 Disable..... default
1 Enable
8 **AGP**
0 Disable..... default
1 Enable
7-6 **Reserved** ..... always reads 0s
5 **Addresses Over 4G**
0 Disable..... default
1 Enable
4 **Fast Write**
0 Disable..... default
1 Enable
3 **Reserved** ..... always reads 0s
2-0 **Transfer Mode Select** ..... default = 000b
Rx84[3] = 0 (8x mode **not detected** via AGP8XDT#)
001 1x data transfer rate
010 2x data transfer rate
100 4x data transfer rate
Rx84[3] = 1 (8x mode **detected** via AGP8XDT#)
000 -reserved ..... default
001 4x data transfer rate
010 8x data transfer rate

Device 0 Offset 93-90 - AGP 3.0 GART / TLB Control . RW

31-10 Reserved .....always reads 0s

9 Calibration Cycle
- 0 Disable..... default
- 1 Enable

8 Graphics Aperture Base Register (Rx13-10) Read
- 0 Disable..... default
- 1 Enable

7 GART TLB
- 0 Disable (TLB entries are invalidated)..... default
- 1 Enable

6-0 Reserved .....always reads 0s

Device 0 Offset 97-94 - AGP 3.0 Graphics Aperture SizeRW

31-28 Aperture Page Size Select..... default = 0000b
Only 4K pages are allowed

27 Reserved .....always reads 0s

26-16 Page Size Supported .....default = 001h
If bit-n of this field is 1, indicates support of 2^(n+12) page size. Must be set to 001h (field bit-0 set) to indicate only 4K pages allowed.

15-12 Reserved .....always reads 0s

11-0 Aperture Size..... default = 0

111100111111	4MB
111100111110	8MB
111100111100	16MB
111100111000	32MB
111100110000	64MB
111100100000	128MB
111100000000	256MB
111000000000	512MB
110000000000	1GB
100000000000	2GB <= Max supported
000000000000	4GB <= Do not program

Device 0 Offset 9B-98 - AGP 3.0 GART Table Base .....RW

31-12 GART Base Address [31:12]..... default = 0

11-0 Reserved .....always reads 0s

AGP 2.0 / 3.0 Registers

Device 0 Offset AC - AGP Control (00h)..... RW

7 AGP .....RO per strap on MAB9
- 0 Disable..... default
- 1 Enable

6 AGP Read Synchronization
- 0 Disable..... default
- 1 Enable

5 AGP Read Snoop DRAM Post-Write Buffer
- 0 Disable..... default
- 1 Enable

4 GREQ# Priority Becomes Higher When Arbiter is Parked at AGP Master
- 0 Disable..... default
- 1 Enable

3-2 Reserved .....always reads 0s

1 AGP Arbitration Parking
- 0 Disable..... default
- 1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)

0 AGP to PCI Master or CPU to PCI Turnaround Cycle
- 0 2T or 3T Timing..... default
- 1 1T Timing

Device 0 Offset AD – AGP Latency Timer (02h)..... RW

7 AGP Performance Improvement
- 0 Disable..... default
- 1 Enable

6 Pipe Mode Performance Improvement
- 0 Disable..... default
- 1 Enable

5 AGP Data Input Enable (for Power Saving)
- 0 AGP data input always enabled..... default
- 1 AGP data input only enabled when necessary to avoid redundant transitions

4 AGP Performance Improvement
- 0 Disable..... default
- 1 Enable

3-0 AGP Data Phase Latency Timer ..... default = 02h

Device 0 Offset AE – AGP Misc Control (00h).....RW

7-3 Reserved ..... always reads 0

2 AGP Performance Improvement
- 0 Disable.....default
- 1 Enable

1 DBI / PIPE Mux Function
- 0 From DBIH (0.95).....default
- 1 From PIPE (0.9)

0 CPU GART Read, AGP GART Write Coherency
- 0 Disable.....default
- 1 Enable

Device 0 Offset AF – AGP 3.0 Control (00h) .....RW

7 CPU / PCI Master GART Access
- 0 Disable.....default
- 1 Enable

6 AGP Calibration
- 0 Disable.....default
- 1 Enable

5 Mix Coherent / Non-coherent Accesses
- 0 Disable.....default
- 1 Enable

4 Reserved ..... always reads 0

3 DBI Function
- 0 Disable (DBI input masked and all outputs assume DBI=0).....default
- 1 Enable

2 DBI Output for AGP Transactions
- 0 Disable.....default
- 1 Enable

1 DBI Output for Frame Transactions Including Fast-Write
- 0 Disable.....default
- 1 Enable

0 DBI Output from Frame Transactions
- 0 Disable.....default
- 1 Enable

Device 0 Offset B0 – AGP Pad Control / Status (8xh).... RW

7 AGP 4x Strobe VREF Control
- 0 STB VREF is STB# and vice versa
- 1 STB VREF is AGPREF **..... default**

6 AGP 4x Strobe & GD Pad Drive Strength
- 0 Drive strength set to compensation circuit default..... default
- 1 Drive strength controlled by RxB1[7-0]

5-3 AGP Compensation Circuit N Control Output. RO

2-0 AGP Compensation Circuit P Control Output. RO

Note: N = low drive, P = high drive

Device 0 Offset B1 – AGP Drive Strength (63h)..... RW

7-4 AGP Output Buffer Low Drive Strength .....def=6

3-0 AGP Output Buffer High Drive Strength.....def=3

Device 0 Offset B2 – AGP Pad Drive / Delay (08h).....RW

7 GD/GBE/GDS, SBA/SBS Control
- 0 SBA/SBS = no cap .....default
  GD/GBE/GDS = no cap
- 1 SBA/SBS = **cap**
  GD/GBE/GDS = **cap**

6-5 GD / GBE Receive Strobe Delay
- 00 None .....default
- 01 Delay by 1.5 ns
- 10 Delay by 3.0 ns
- 11 Delay by 4.5 ns

4 GD[31-16] Staggered Delay
- 0 None .....default
- 1 GD[31:16] delayed by 1 ns

3 AGP Slew Rate Control
- 0 Disable
- 1 Enable**..... default**

2 SBA Receive Strobe Delay
- 0 None .....default
- 1 Delay by 1.5 ns

1-0 GDS Output Delay
- 00 None .....default
- 01 Delay by 1.5 ns
- 10 Delay by 3.0 ns
- 11 Delay by 4.5 ns

(GDS1 & GDS1# will be delayed an additional 1ns if bit-4 = 1)

Device 0 Offset B3 – AGP Strobe Drive Strength .....RW

7-4 AGP Strobe Output Low Drive Strength ..... def=0

3-0 AGP Strobe Output High Drive Strength ..... def=0

V-Link Drive Control Registers

Device 0 Offset B4 – V-Link NB Compensation Ctrl (00h)RW

7-5 **V-Link Autocomp High Output Value**.... def=0, RO
4 **Reserved** ..... always reads 0
3-1 **V-Link Autocomp Low Output Value** .... def=0, RO
0 **Compensation Selection**
0 Auto Comp (use values in bits 7-1)..... default
1 Manual Comp (use values in RxB5-B6)

Device 0 Offset B5 – V-Link NB Strobe Drive Ctrl (00h)RW

7-5 **Strobe High Drive Manual Setting**..... default = 0
4 **Reserved** ..... always reads 0
3-1 **Strobe Low Drive Manual Setting** ..... def = 0
0 **Reserved** ..... always reads 0

Device 0 Offset B6 – V-Link NB Data Drive Ctrl (00h) . RW

7-5 **Data High Drive Manual Setting**..... default = 0
4 **Reserved** ..... always reads 0
3-1 **Data Low Drive Manual Setting** ..... default = 0
0 **Reserved** ..... always reads 0

Device 0 Offset B8 – V-Link SB Compensation Ctrl (00h)RW

7-5 **V-Link Autocomp High Output Value** ....def=0, RO
4 **Reserved** ..... always reads 0
3-1 **V-Link Autocomp Low Output Value** .....def=0, RO
0 **Compensation Selection**
0 Auto Comp (use values in bits 7-1).....default
1 Manual Comp (use values in RxB9-BA)

Device 0 Offset B9 – V-Link SB Strobe Drive Ctrl (00h)RW

7-5 **Strobe High Drive Manual Setting**..... default = 0
4 **Reserved** ..... always reads 0
3-1 **Strobe Low Drive Manual Setting** ..... def = 0
0 **Reserved** ..... always reads 0

Device 0 Offset BA – V-Link SB Data Drive Ctrl (00h)..RW

7-5 **Data High Drive Manual Setting**..... default = 0
4 **Reserved** ..... always reads 0
3-1 **Data Low Drive Manual Setting** ..... default = 0
0 **Reserved** ..... always reads 0

Power Management Registers

Device 0 Offset BC – Power Management Mode (00h).. RW

7 Dynamic Power Management
- 0 Disable..... default
- 1 Enable

6 Halt / Shutdown Enables Power Management
- 0 Disable..... default
- 1 Enable

5 Stop Clock Enables Power Management
- 0 Disable..... default
- 1 Enable

4 Suspend Status Enables Power Management
- 0 Disable..... default
- 1 Enable

3-0 Reserved ..... always reads 0

Device 0 Offset BD – DRAM Power Mgmt Mode (00h) RW

7 DRAM Self-Refresh in Power Management Mode
- 0 Disable..... default
- 1 Enable

6 Dynamic CKE When DRAM Is Idle
- 0 Disable..... default
- 1 Enable

5 Dynamic DRAM I/O Pad Power-Down (Float)
- 0 Disable..... default
- 1 Enable

4-0 Reserved ..... always reads 0

Device 0 Offset BE – Dynamic Clock Stop Control (00h)RW

7 Host CPU Interface Power Management
- 0 Disable..... default
- 1 Enable

6 DRAM Interface Power Management
- 0 Disable..... default
- 1 Enable

5 V-Link Interface Power Management
- 0 Disable..... default
- 1 Enable

4 AGP Interface Power Management
- 0 Disable..... default
- 1 Enable

3 PCI#2 Interface Power Management
- 0 Disable..... default
- 1 Enable

2 Graphics Interface Power Management
- 0 Disable..... default
- 1 Enable

1 Reserved ..... always reads 0

0 Host CPU Fast Power Management (DADS Fast Timing)
- 0 Disable..... default
- 1 Enable

Device 0 Offset BF – DRAM Pad Toggle Reduction (00h)RW

7 MA / SCMD Pin Toggle Reduction
- 0 Disable.....default
- 1 Enable (MA and S command pins won't toggle if not accessed)

6-4 Reserved ..... always reads 0

3 DIMM #3 MAA / MAB Select
- 0 MAA .....default
- 1 MAB

2 DIMM #2 MAA / MAB Select
- 0 MAA .....default
- 1 MAB

1 DIMM #1 MAA / MAB Select
- 0 MAA .....default
- 1 MAB

0 DIMM #0 MAA / MAB Select
- 0 MAA .....default
- 1 MAB

Extended Power Management Registers

Device 0 Offset C0 – Power Management Capability ID RO

7-0 Capability ID ..... always reads 01h

Device 0 Offset C1 – Power Management New Pointer.. RO

7-0 New Pointer ..... always reads 00h ("Null" Pointer)

Device 0 Offset C2 – Power Mgmt Capabilities I..... RO

7-0 Power Management Capabilities... always reads 02h

Device 0 Offset C3 – Power Mgmt Capabilities II ..... RO

7-0 Power Management Capabilities... always reads 00h

Device 0 Offset C4 – Power Mgmt Control / Status.....RW

7-2 Reserved ..... always reads 0

1-0 Power State

00 D0 .....default
01 -reserved-
10 -reserved-
11 D3 Hot

Device 0 Offset C5 – Power Management Status .....RW

7-0 Power Management Status ..... default = 0

Device 0 Offset C6 – PCI-to-PCI Bridge Support Ext. ...RW

7-0 P2P Bridge Support Extensions..... default = 0

Device 0 Offset C7 – Power Management Data.....RW

7-0 Power Management Data ..... default = 0

Host CPU Interface Control Registers

Device 0 Offset D2 – S2K Timing Control III (78h)..... RW

The contents of this register are preserved during suspend. Bits 2-0 have no default value.

- **7 Disconnect Enable When STPGNT Detected**
- **6 Write to Read Delay**..... default = 1
- **5-4 Read to Write Delay**..... default = 11b
- **3 Reserved (Do Not Program)**..... default = 1
- **2-0 Write Data Delay from SYSDC to CPU Data Output** ..... (WrDataDly)

Device 0 Offset D3 – BIU Arbitration Control ..... RW

- **7-6 Max of Contiguous Probe SysDC Before Switch to Other Type of SysDC**
- **5-3 Max of Contiguous Read SysDC Before Switch to Other Type of SysDC**
- **2-0 Max of Contiguous Write SysDC Before Switch to Other Type of SysDC**

Device 0 Offset D4 – BIU Control 1 ..... RW

- **7 DRAM Self-Refresh When Disconnected**
  - 0 Disable..... default
  - 1 Enable
- **6 Probe Next Tag State T1 When PCI Master Read Caching Enabled**
  - 0 Disable..... default
  - 1 Enable
- **5 64 HCLK Wait Time**
  - 0 Disable..... default
  - 1 Enable
- **4 Master Request Full Protocol**
  - 0 Enhanced ..... default
  - 1 Backwards compatible

  VIA recommends setting this bit to 0
- **3 DRAM Speculative Read for PCI Master Read (Before Probe Result is Known)**
  - 0 Disable..... default
  - 1 Enable
- **2 PCI Master Pipeline Request**
  - 0 Disable..... default
  - 1 Enable
- **1 PCI-to-CPU / CPU-to-PCI (P2C / C2P) Concurrency**
  - 0 Disable..... default
  - 1 Enable
- **0 Fast Write-to-Read Turnaround**
  - 0 Disable..... default
  - 1 Enable

Device 0 Offset D5 – BIU Control 2 .....RW

- **7 FWDVLD / PSQHPTR Concurrency**
  - 0 Backwards Compatible .....default
  - 1
- **6 RHOCTW**
  - 0 .....default
  - 1
- **5 PMW Address Compare**
  - 0 Backward compatible.....default
  - 1 Compare address qualified with PMW
- **4 Write Policy for CPU Write to DRAM**
  - 0 Issue DRAM write when FIFO holds more than two requests or DRAM controller idle..... def
  - 1 Disable Write Policy
- **3 PMR Cycle Control**
  - 0 Stall PMR cycle if MWQ is full.....default
  - 1 Execute PMR cycles normally whether MWQ is full or not
- **2 FID Command Detect**
  - 0 Disable (command will not have new FID).. def
  - 1 Enable
- **1 HALT Command Detect**
  - 0 Disable (command will not do self refresh) . def
  - 1 Enable
- **0 Reserved** ..... always reads 0

Device 0 Offset D6 – BIU Control 3 .....RW

- **7 Memory Write Queue Timer Function**
  - 0 Disable.....default
  - 1 Enable
- **6 Memory Write Queue Timer Function Trigger**
  - 0 Trigger by data ready for C2M Wr Req..... def
  - 1 Trigger by command FIFO utilization
- **5-3 Memory Write Queue Timer High Bound**..... def=0
- **2-0 Memory Write Queue Timer Low Bound**..... def=0

  Bits 5-0 are defined in units of 4QW / request number

Device 0 Offset D7 – CPU Strapping Control..... RO

7-3 CPU Clock Divide ..... set from VAD[3-0] straps

00000 11 .....no strap default
00001 11.5
00010 12
00011 12.5
00100 5
00101 5.5
00110 6
00111 6.5
01000 7
01001 7.5
01010 8
01011 8.5
01100 9
01101 9.5
01110 10
01111 10.5
10000 3
10001 3.5
10010 4
10011 4.5
101xx -reserved-

2 S2K Drive Strength

0 Determined by register settings ..... default
1 Determined by auto compensation

1 Fast Address Out Decode ..... set from ROMSIP#

0 Normal.....no strap default
1 Fast

0 S2K Compensation Circuit

0 Always Enable ..... default
1 Enable on Disconnect

Device 0 Offset D8 – S2K Compensation Strapping (00h)RW

7 Reserved ..... always reads 0
6-4 S2K Pullup Drive Strength ..... default = 0
3 Reserved ..... always reads 0
2-0 S2K Pulldown Drive Strength ..... default = 0

Device 0 Offset D9 – S2K Compensation Result 1 (00h)..RO

7 Reserved ..... always reads 0
6-4 Pullup Auto Compensation Result..... default = 0
3 Reserved ..... always reads 0
2-0 Pulldown Auto Compensation Result .... default = 0

Device 0 Offset DA – S2K Compensation Result 2.....RW

7 S2K Edge DQ Mode.....RO, set from MA11 strap

0 Central DQ .....default
1 Edge DQ

6-0 S2K Strobe Delay (EdgeDQ)..... ..... set from MA[8-4] straps

0 Auto Mode .....no-strap default
~0 Strapping Mode

Device 0 Offset DB – S2K Compensation Result 3.....RO

7-0 S2K Strobe DLL Delay Counter (Auto)..... def = 0

Device 0 Offset DC – S2K Compensation Result 4 (07h)RW

7 S2K Compensation Circuit Trigger
6 DLL Autodetect.....RO
5 Delay Compensation Counter Control
4-3 S2K Pad AC Coupling to VREF Signal in Address / Data Output Clock
2-0 S2K Pad Slew Rate Ctrl (7h is strongest) .....def=7h

Device 0 Offset DD – S2K Compensation Result 5.....RW

7-4 S2K Strobe Output Drive Strength P Control
3-0 S2K Strobe Output Drive Strength N Control

Device 0 Offset DE – BIU Control 4 ..... RW

7 Pending Memory Read
- 0 Read not pending..... default
- 1 Read pending

6 Issue Memory Write Queue Ready When Command FIFO is Empty Enough (>24)
- 0 Disable..... default
- 1 Enable

5 Issue Memory Write Queue If More Than 4 CPU Requests Are Pending
- 0 Disable..... default
- 1 Enable

4 Fast Write Performance Improvement
- 0 Backwards Compatible..... default
- 1 Enable performance improvement

3 Issue Write DADS Only When Memory Write Queue Timer or DM Idle or HB Hit
- 0 Disable..... default
- 1 Enable

2 Compare Partial Address to Decide if CPU-to-Memory Read Hit CPU-to-Memory Write
- 0 Compare HA[31:6] (backwards compatible) def
- 1 Compare HA[31:12]

1 P2C Write Priority Over Read
- 0 Priority not given to Write..... default
- 1 Priority given to write

0 DPH5 Performance Improvement
- 0 Enable..... default
- 1 Disable

Device 0 Offset DF – BIU Control 5..... RO

7 Transparent MD to HD in Synchronous Mode for Performance Improvement
- 0 Disable..... default
- 1 Enable

6 Delay 1T For Speculative Read Command
- 0 Disable..... default
- 1 Enable

5 166/200 Performance Improvement in Master Request Logic
- 0 Disable..... default
- 1 Enable

4 166 / 200 Performance Improvement in Host CPU Master Read Ready Logic
- 0 Disable..... default
- 1 Enable

3-0 Reserved ..... always reads 0

Device 0 Offset E6 –APIC Decoding (00h).....RW

7-5 Reserved ..... always reads 0

4 I/O APIC Decoding
- 0 FECxxxxx accesses go to PCI.....default
- 1 FEC00000 to FEC7FFFF accesses go to PCI
  FEC80000 to FECFFFFF accesses go to AGP

3-0 Reserved ..... always reads 0

DRAM Drive Control Registers

Device 0 Offset E8 – DQ Drive Control ..... RW

7-4 High Drive – MD, MECC, DQS#, DQM Pins
0000 Lowest ..... default
0001
… …
1111 Highest

3-0 Low Drive – MD, MECC, DQS#, DQM Pins
0000 Lowest ..... default
0001
… …
1111 Highest

Device 0 Offset E9 – CS Drive Control ..... RW

7-4 High Drive – CS#, CKE Pins
0000 Lowest ..... default
0001
… …
1111 Highest

3-0 Low Drive – CS#, CKE Pins
0000 Lowest ..... default
0001
… …
1111 Highest

Device 0 Offset EA – MAA Drive Control ..... RW

7-4 High Drive – MAA, SRASA, SCASA, SWEA Pins
0000 Lowest ..... default
0001
… …
1111 Highest

3-0 Low Drive – MAA, SRASA, SCASA, SWEA Pins
0000 Lowest ..... default
0001
… …
1111 Highest

Device 0 Offset EB – MAB Drive Control ..... RW

7-4 High Drive – MAB, SRASB, SCASB, SWEB Pins
0000 Lowest ..... default
0001
… …
1111 Highest

3-0 Low Drive – MAB, SRASB, SCASB, SWEB Pins
0000 Lowest ..... default
0001
… …
1111 Highest

Device 0 Offset EC – DRAM S-Port Control ..... RW

7 DQ S-Port Control ..... default = 0
6 CS# S-Port Control ..... default = 0
5 MAA S-Port Control ..... default = 0
4 MAB S-Port Control ..... default = 0
3 DQS S-Port Control ..... default = 0
2-0 Reserved ..... always reads 0

Device 0 Offset ED – DRAM DQS Drive Control ..... RW

7-4 High Drive - DQS
0000 Lowest ..... default
0001
… …
1111 Highest

3-0 Low Drive - DQS
0000 Lowest ..... default
0001
… …
1111 Highest

Device 0 Offset EE – DRAM DQS/MD Duty Cycle Ctrl RW

This register is used for duty cycle adjustment.

7-6 MD Output Rise Time Control ..... default = 00b
5-4 MD Output Fall Time Control ..... default = 00b
3-2 DQS Output Rise Time Control ..... default = 00b
1-0 DQS Output Fall Time Control ..... default = 00b

Miscellaneous Registers

Device 0 Offset FD – AGP 2.0 / 3.0 Select ..... RW

7-3 Reserved ..... always reads 0
2 AGP Capability Pointer (Rx34) Value
0 Rx34 = A0h (AGP 2.0) ..... default
1 Rx34 = 80h (AGP 3.0)
1 Compatible Rx80-AF
0 AGP 3.0 registers at Rx80-B3 ..... default
1 AGP 2.0 registers at Rx80-B3
0 AGP Status Register Write
0 Disable (AGP 3.0 Rx84 is RO) ..... default
1 Enable (AGP 3.0 Rx84 is RW)

Device 1 Header Registers - PCI-to-PCI Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h)..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (B168h)..... RO

15-0 ID Code (reads B168h to identify the KT600 PCI-to-PCI Bridge device)

Device 1 Offset 5-4 – Command (0007h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable.....RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable.....RO
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping .....RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... **RW**
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop (Not Supported) .....RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette writes on PCI bus (10-bit decode of I/O addresses 3C6-3C9 hex)

4 Memory Write and Invalidate Command.....RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring .....RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 Bus Master ..... **RW**
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface..... **default**

1 Memory Space..... **RW**
- 0 Does not respond to memory space
- 1 Enable memory space access..... **default**

0 I/O Space ..... **RW**
- 0 Does not respond to I/O space
- 1 Enable I/O space access..... **default**

Device 1 Offset 7-6 - Status (Primary Bus) (0230h) .....RWC

15 Detected Parity Error ..... always reads 0

14 Signaled System Error (SERR#) ..... always reads 0

13 Signaled Master Abort
- 0 No abort received .....default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles) .... **write 1 to clear**

12 Received Target Abort
- 0 No abort received .....default
- 1 Transaction aborted by the target with Target-Abort .....**write 1 to clear**

11 Signaled Target Abort ..... always reads 0

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... **always reads 01**
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected ..... always reads 0

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features ..... always reads 0

5 66MHz Capable..... always reads 1

4 Supports New Capability list ..... always reads 1

3-0 Reserved ..... always reads 0

Device 1 Offset 8 - Revision ID (00h).....RO

7-0 KT600 Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface (00h) .....RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier..... always reads 00

Device 1 Offset A - Sub Class Code (04h) .....RO

7-0 Sub Class Code.. reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h) .....RO

7-0 Base Class Code... reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer (00h).....RO

7-0 Reserved ..... always reads 0

Device 1 Offset E - Header Type (01h).....RO

7-0 Header Type Code .....reads 01: PCI-PCI Bridge

Device 1 Offset F - Built In Self Test (BIST) (00h).....RO

7 BIST Supported ..... reads 0: no supported functions

6 Start Test ..... write 1 to start but writes ignored

5-4 Reserved ..... always reads 0

3-0 Response Code.....0 = test completed successfully

Device 1 Offset 18 - Primary Bus Number (00h)..... RW

7-0 Primary Bus Number ..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h) ..... RW

7-0 Secondary Bus Number..... default = 0

Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h) .... RW

7-0 Primary Bus Number ..... default = 0

Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1B – Secondary Latency Timer (00h) .... RO

7-0 Reserved ..... always reads 0

Device 1 Offset 1C - I/O Base (f0h) ..... RW

7-4 I/O Base AD[15:12] ..... **default = 1111b**

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1D - I/O Limit (00h)..... RW

7-4 I/O Limit AD[15:12]..... default = 0

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1F-1E - Secondary Status (0000h)..... RO

15-0 Rx44[4] = 0: No Function (always reads 0)
Rx44[4] = 1: Read same value as Rx7-6 (Pri Status)

Device 1 Offset 21-20 - Memory Base (FFF0h)..... RW

15-4 Memory Base AD[31:20] .....default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) RW

15-4 Memory Limit AD[31:20]..... default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 25-24 - Prefetchable Mem Base (FFF0h) RW

15-4 Prefetchable Memory Base AD[31:20].. **def = FFFh**

3-0 Reserved ..... always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit (0000h) ..... RW

15-4 Prefetchable Memory Limit AD[31:20] .....
..... default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 34 – Capability Pointer (80h) .....RO

7-0 Capability Pointer..... **always reads 80h**

Device 1 Offset 3F-3E – PCItoPCI Bridge Ctrl (0000h) RW

15-4 Reserved ..... always reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus.....default

1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D) .....default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved ..... always reads 0

Device 1 Configuration Registers - PCI-to-PCI Bridge

AGP Bus Control Registers

Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h) RW

7 CPU-AGP Post Write
- 0 Disable..... default
- 1 Enable

6 CPU-AGP One Wait State Burst Write
- 0 Disable..... default
- 1 Enable

5-4 Read Prefetch Control
- 00 Always prefetch..... default
- x1 Never prefetch
- 10 Prefetch only for Enhance command

3 Reserved ..... always reads 0

2 MDA Present on AGP
- 0 Forward MDA accesses to AGP..... default
- 1 Forward MDA accesses to PCI

Note: Forward despite IO / Memory Base / Limit

Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.

Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).

1 AGP Master Read Caching
- 0 Disable..... default
- 1 Enable

0 AGP Delay Transaction
- 0 Disable..... default
- 1 Enable

Table 8. VGA / MDA Memory / IO Redirection

3E[3] VGA Pres.	40[2] MDA Pres.	VGA is on	MDA is on	Axxxx, B8xxx Access	B0000 -B7FFF Access	3Cx, 3Dx I/O	3Bx I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (00h) RW

7 Retry Status
- 0 No retry occurred.....default
- 1 Retry Occurred ..... **write 1 to clear**

6 Retry Timeout Action
- 0 No action taken except to record status..... def
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Count
- 00 Retry 2, backoff CPU .....default
- 01 Retry 4, backoff CPU
- 10 Retry 16, backoff CPU
- 11 Retry 64, backoff CPU

3 CPU-to-AGP Bursting Timeout
- 0 Disable.....default
- 1 Enable

2 Reserved ..... always reads 0

1 Invalidate Bufferred PCI/AGP Read Data (Read Cache Data) on CPU-to-PCI/AGP Read
- 0 Disable.....default
- 1 Enable

0 Reserved ..... always reads 0

Device 1 Offset 42 - AGP Master Control (00h).....RW

7 Disconnect PCI on AGP Data Ready
- 0 Continue current PCI master even if AGP data is ready .....default
- 1 Disconnect current PCI master when AGP data is ready

6 AGP Master One Wait State Write
- 0 Disable.....default
- 1 Enable

5 AGP Master One Wait State Read
- 0 Disable.....default
- 1 Enable

4 Break Consecutive PCI Master Accesses
- 0 Disable.....default
- 1 Enable

3 Reserved ..... always reads 0

2 Claim I/O R/W and Memory Read Cycles
- 0 Disable.....default
- 1 Enable

1 Claim Local APIC FEEx_xxxx Cycles
- 0 Disable.....default
- 1 Enable

0 Snoop Write Enable 2T Rate
- 0 Disable.....default
- 1 Enable

Device 1 Offset 43 - AGP Master Latency Timer (22h) RW

7-4 Host to AGP Time Slot
- 0 Disable (no timer
- 1 16 GCLKs
- 2 32 GCLKs) ..... default
- 3 48 GCLKs
- … …
- F 240 GCLKs

3-0 AGP Master Time Slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs ..... default
- 3 48 GCLKs
- … …
- F 240 GCLKs

Device 1 Offset 44 – Backdoor Register Control (20h).. RW

7 Revision ID Writeable
- 0 Revision ID is RO ..... default
- 1 Revision ID is RW

6 Reserved ..... always reads 0

5 Power Management Capability Support
- 0 Rx34 reads 00
- 1 Rx34 reads 80h ..... default

4 Reflect Rx7-6 Status in Rx1F-1E
- 0 Disable (Rx1F-1E always reads 0) ..... default
- 1 Enable (Rx1F-1E reads same as Rx7-6)

3-2 Rx83[2-1] Back Door Value

1 Rx82[5] Back Door Value (Device Specific Intfc)

0 Back Door Register Enable for AGP Device ID (Rx47-46)
- 0 Disable..... default
- 1 Enable

Device 1 Offset 45 – Fast Write Control (72h).....RW

7 Force Fast Write Cycle to be QW Aligned (if Rx45[6] = 0)
- 0 Disable.....default
- 1 Enable

6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction
- 0 Disable
- 1 Enable**..... default**

5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable**..... default**

4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable**..... default**

3 Reserved ..... always reads 0

2 Fast Write Burst 4T Max (No Slave Flow Control)
- 0 Disable.....default
- 1 Enable

1 Fast Write Fast Back to Back
- 0 Disable
- 1 Enable**..... default**

0 Fast Write Initial Block 1 Wait State
- 0 Disable.....default
- 1 Enable

Rx45 Bits 7-4	CPU Write Address in Mem1	CPU Write Address in Mem2	Fast Write Cycle Alignment
x1xx	-	-	QW aligned, burstable
0000	-	-	DW aligned, nonburstable
x010	0	0	n/a
0010	0	1	DW aligned, non-burstable
x010	1	-	QW aligned, burstable
x001	0	0	n/a
x001	-	1	QW aligned, burstable
0001	1	0	DW aligned, non-burstable
x011	0	0	n/a
x011	1	-	QW aligned, burstable
x011	0	1	QW aligned, burstable
1000	-	-	QW aligned, non-burstable
1010	0	1	QW aligned, non-burstable
1001	1	0	QW aligned, non-burstable

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID ... RW

15-0 PCI-to-PCI Bridge Device ID..... default = 0000

Device 1 Offset 48 – Parity Error Reporting .....RWC

7 AGP Data Parity Error Status.....RWC
- 0 No error ..... default
- 1 AGP Data Parity error occurred

6 AGP SERR Status.....RWC
- 0 No SERR ..... default
- 1 SERR occurred

5 Reserved ..... always reads 0

4 Parity Error Reporting – AGP Cycles ..... RW
- 0 Disable (parity error not reported)..... default
- 1 Enable (parity error reported)

3-2 Reserved ..... always reads 0

1 Parity Error Reporting – PCI2 Data..... RW
- 0 Disable (parity error not reported)..... default
- 1 Enable (parity error reported)

0 Parity Error Reporting – PCI2 Address..... RW
- 0 Disable (parity error not reported)..... default
- 1 Enable (parity error reported)

Device 1 Offset 80 – Capability ID (01h).....RO

7-0 Capability ID ..... always reads 01h

Device 1 Offset 81 – Next Pointer (00h).....RO

7-0 Next Pointer: Null ..... always reads 00h

Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h) ...RO

7-6 Power Mgmt Capabilities..... always reads 0
5 Power Mgmt Capabilities.. programmed via Rx44[1]
4-0 Power Mgmt Capabilities..... always reads 02h

Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h) ...RO

7-3 Power Mgmt Capabilities..... always reads 0
2-1 Power Mgmt Capabilitiesprogrammed via Rx44[3-2]
0 Power Mgmt Capabilities..... always reads 0

Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h).....RW

7-2 Reserved ..... always reads 0

1-0 Power State
- 00 D0 .....default
- 01 -reserved-
- 10 -reserved-
- 11 D3 Hot

Device 1 Offset 85 – Power Mgmt Status (00h) .....RO

7-0 Power Mgmt Status..... default = 00

Device 1 Offset 86 – P2P Br. Support Extensions (00h)...RO

7-0 P2P Bridge Support Extensions..... default = 00

Device 1 Offset 87 – Power Management Data (00h).....RO

7-0 Power Management Data ..... default = 00

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-55	125	^{O}C
Case Operating Temperature	0	85	^{O}C
Input Voltage	-0.5	5.5	Volts
Output Voltage (V_{CC} = 3.1 - 3.6V)	-0.5	V_{CC} + 0.5	Volts

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

T_C = 0-85^{O}C, V_{CC3}=3.3V+/-5%, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.50	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input leakage current	-	+/-10	uA	$0<V_{IN}<V_{CC}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45<V_{OUT}<V_{CC}$

Power Characteristics

T_C = 0-85^{O}C, V_{RAIL} = V_{CC} +/- 5%, V_{CORE} = 2.5V +/- 5%, GND=0V

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CC33}	Power Supply Current - Internal Logic & I/O Intfc			mA	Max operating frequency
I_{CCSUS}	Power Supply Current - Suspend Power			mA	Max operating frequency
I_{CCTT}	Power Supply Current - CPU Interface Termination			mA	Max operating frequency
I_{CCHCK}	Power Supply Current - Host CPU Clock Logic			mA	Max operating frequency
I_{CCMCK}	Power Supply Current - DRAM Clock Logic			mA	Max operating frequency
I_{CCGCK}	Power Supply Current - AGP Clock Deskew Logic			mA	Max operating frequency
I_{CCQ}	Power Supply Current - AGP 1.5V or 3.3V Power			mA	Max operating frequency
I_{CCQQ}	Power Supply Current - AGP Quiet Power			mA	Max operating frequency
$I_{CCS2KREF}$	Power Supply Current - CPU Interface Voltage Ref			uA	Max operating frequency
$I_{CCCLKREF}$	Power Supply Current - Clock Voltage Reference			uA	Max operating frequency
$I_{CCAGPREF}$	Power Supply Current - AGP Voltage Reference			uA	Max operating frequency
P_D	Power Dissipation			W	Max operating frequency

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 9. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
3.3V Power	3.135	3.465	Volts
2.5V Power	2.375	2.625	Volts
Case Temperature	0	85	^{O}C

Drive strength for each output pin is programmable. See Rx6D for details.

MECHANICAL SPECIFICATIONS

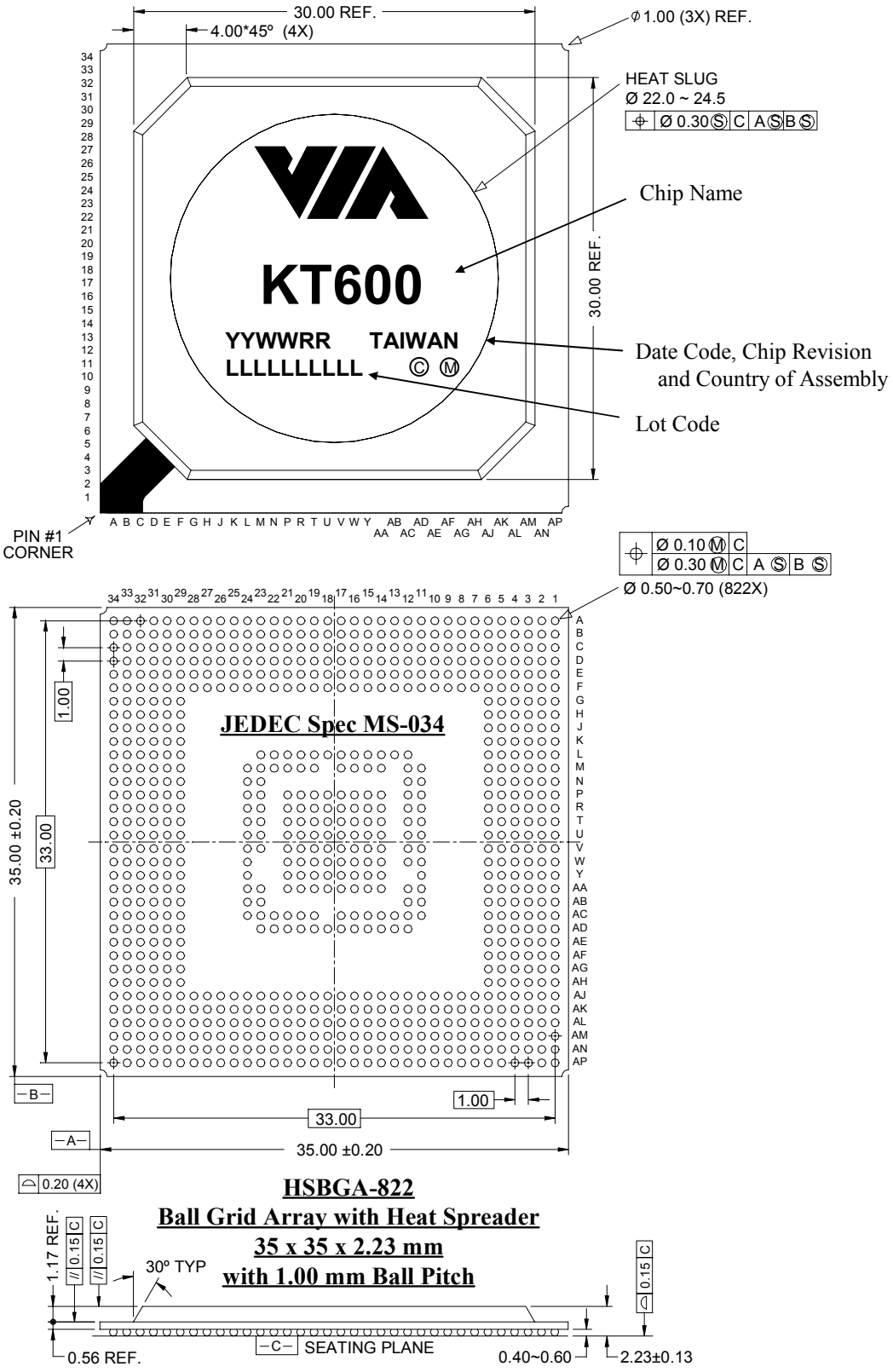


Figure 6. Mechanical Specifications – 822-Pin HSBGA Ball Grid Array Package with Heat Spreader