Data Sheet

KM400A Desktop North Bridge

with Integrated UniChrome 3D / 2D Graphics Controller

Revision 1.23
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VIA TECHNOLOGIES, INC.

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Offices:

VIA Technologies Incorporated
Taiwan Office:
8th Floor, No. 533
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: (886-2) 2218-5452
Fax: (886-2) 2218-5453
Home page: http ://www.via.com.tw

VIA Technologies Incorporated
USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: (510) 683-3300
Fax: (510) 683-3301 or (510) 687-4654
Home Page: http://www.viatech.com

S3 Graphics Incorporated
USA Office:
1045 Mission Court
Fremont, CA 94539
USA
Tel: (510) 687-4900
Fax: (510) 687-4901
Home Page: http://www.s3graphics.com

REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	4/17/03	Initial external release, same as KM400 release 1.1 with DDR400 support added	DH
1.01	4/22/03	Fixed typographical error on cover page; fixed note under Device 0 Rx69[6]	DH
1.02	5/6/03	Fixed core / IO voltage feature bullet	DH
1.03	5/28/03	Removed 1920x1440 from Table 1; Fixed DP0Dxx strap definitions	DH
1.04	6/13/03	Updated AGP-muxed display functions in ballout on F3, G4, G5, H4, J5 (ballout matches R&D document revision 1.1 dated 6/10/03)	DH
1.1	7/1/03	Removed "Confidential" watermark from cover page Added 400 MHz FSB support (cover page, feature bullets, overview, block diagram, VAD pin descriptions and Rx54[7-6]) Fixed "2.5V Core and …" feature bullet; Changed south bridge to VT8237 Removed 8MB frame buffer support from feature bullets, table 1 and RxE0[6-4]	DH
1.11	7/1/03	Fixed document revision number in page footers	DH
1.12	8/19/03	Removed registered DIMM support; fixed typos in Overview south bridge section Changed "Flat Panel Monitor" to "DVI Monitor" in system block diagram	DH
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1.17	12/4/03	Fixed top marking on mechanical specifications	AT
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1.21	3/19/04	Modified graphic features Capitalized north bridge and south bridge in pin description table Fixed minor typo error in pin description table Modified name of pinlist table 2 and table 3 Modified mechanical specification figure	SV
1.22	4/19/04	Added Dev 0 Rx50-Rx53 registers	EY
1.23	4/28/04	Added DirectX 9.0 in full software support feature	SV

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KM400A
NORTH BRIDGE

400 / 333 / 266 / 200 MHz AMD Athlon™ Front Side Bus
Integrated UniChrome 3D / 2D Graphics & Video Controller
Advanced DDR400 SDRAM Controller
533 MB/Sec V-Link Interface
External 8x / 4x AGP Bus

PRODUCT FEATURES

- **Defines Highly Integrated Solutions for Performance Desktop PC Designs**
  - High performance UMA North Bridge: Integrated VIA KT600 and UniChrome 3D / 2D Graphics and Video Controllers in a single chip
  - Advanced 64-bits DDR SDRAM controller supporting DDR400 / 333 / 266 SDRAM
  - Multiple CRT, DVI monitor and TV-Out interfaces
  - Combines with VIA VT8235 / VT8237 V-Link South Bridge for integrated 10 / 100 LAN, Audio, ATA133 IDE, LPC, USB 2.0 and Serial ATA (VT8237)
  - 2.5V Core power
  - 35 x 35mm HSBGA package (Ball Grid Array with Heat Spreader) with 552 balls
  - Pin-compatible with VIA KM400 North Bridge
- **High Performance CPU Interface**
  - Supports Socket-A (Socket-462) AMD Athlon / Duron processors
  - Supports dynamically adjustable HSTL-like transceiver signal levels within a range from 1.1V to 1.7V
  - Supports 400 / 333 / 266 / 200 MHz host address and data transfer rate
  - Four-entry command queue for optimal CPU throughput
  - Four-entry probe queue for probes from the system to the processor
  - Eight-entry deep data and control queue separately for CPU-Memory-Read, CPU- Memory-Write and CPU-to-PCI operations
  - Integrated CPU-to-DRAM write buffers and CPU-to-DRAM read prefetch buffers
  - Supports WC (Write Combining) cycles
  - Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - AGP v3.0 compliant 8x / 4x transfer mode with Fast Write support
  - 1.5V AGP I/O interface
  - Pipelined split-transaction long-burst transfers up to 2.1 GB/sec
  - Supports Side Band Addressing (SBA) mode
  - Supports Flush / Fence commands
  - Supports DBI (Dynamic Bus Inversion)
  - Pseudo-synchronous AGP and CPU interfaces with optimal skew control
  - Thirty-two level request queue for read and write
  - Thirty-two level (quadwords) of read and write data FIFO separately
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme

- **Advanced High-Performance 64-bit DDR SDRAM Controller**
  - Supports DDR400 / 333 / 266 memory types with 2.5V SSTL-2 DRAM interface
  - Supports mixed 64 / 128 / 256 / 512 / 1024 Mb SDRAM in x8 or x16 configurations
  - Supports CL 2 / 2.5 for DDR266 / 333 and CL 2.5 / 3 for DDR400
  - Supports 3 unbuffered double-sided DIMMs and up to 6 GB of physical memory
  - Programmable I/O drive capability for memory address, data and control signals
  - DRAM interface pseudo-synchronous with host CPU for optimal memory performance
  - Concurrent CPU, AGP, internal graphics controller and V-Link access for minimum memory access latency
  - Rank interleave, and up to 16-bank page interleave (i.e., 16 pages open simultaneously) based on LRU to effectively reduce memory access latency
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
  - CPU Read-Around-Write capability for non-stalled operation
  - Speculative memory read before snoop result to reduce PCI master memory read latency
  - Supports burst read and write operations with burst length of 4 or 8
  - Optional dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)
  - Supports self-refresh and CAS-before-RAS DRAM refresh with staggered RAS timing
- **High Bandwidth 533 MB/Sec 8-bit V-Link Host Controller**
  - Supports 66 MHz, 4x and 8x transfer modes, V-Link Host interface with 533 MB/sec total bandwidth
  - Half duplex transfers with separate command / strobe for 4x8 bit mode and full duplex for 8x4 bit mode
  - Request / Data split transaction
  - Transaction assurance for V-Link Host-to-Client access eliminates V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to minimize data wait-states and throttle transfer latency to avoid data overflow
  - Highly efficient V-Link arbitration with minimum overhead
- **Advanced System Power Management Support**
  - ACPI 2.0 and PCI Bus Power Management 1.1 compliant
  - Supports Suspend-to-DRAM (STR) and DRAM self refresh
  - Supports dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)
  - Supports SMI, SMM and STPCLK mechanisms
  - Supports AMD PowerNow! Technology
  - Low-leakage I/O pads

- **Integrated Graphics with 2D / 3D / Video Controllers**
  - Optimized Unified Memory Architecture (UMA)
  - Supports 16 / 32 / 64 MB Frame Buffers size
  - Graphics engine clocks up to 133 MHz decoupled from memory clock
  - Internal AGP 8x performance
  - Two independent 128-bit data buses between North Bridge and graphics core to improve the video performance, one for frame buffer and one for texture /command access
  - PCI v2.2 Host Bus compliant
  - AGP v3.0 compliant

2D Hardware Acceleration Features

- 128-bit 2D graphics engine
- Supports ROP3, 256 operations
- Supports 8bpp, 15/16bpp and 32bpp color depth modes
- BitBLT (Bit Block Transfer) functions including alpha BLTs
- High-color hardware cursor (64x64x16bpp)
- Color expansion, source Color Key and destination Color Key
- Bresenham line drawing / style line function
- Transparency mode
- Window clipping
- Text function

3D Hardware Acceleration Features

3D Graphics Processor

- 128-bit 3D graphics engine
- Floating-point setup engine
- Internal full 32-bit ARGB format for high rendering quality
- 4K Texture Cache

Capability

- Supports ROP2
- Supports various texture formats, including: 16 / 32bbp ARGB, 8 bbp Palletized (ARGB) and YUV 422 / 420
- Texture sizes up to 2048x2048
- High quality texture filter for Nearest, Linear, Bi-linear, Tri-linear and Anisotropic modes
- Flat and Gouraud shading
- Vertex Fog and Fog Table
- Z-Bias, LOD-Bias, Edge Anti-aliasing and Alpha Blending
- Hardware Back-Face culling
- Specular Lighting

Performance

- Two textures per pass
- Triangle rate up to 3 million triangles per second
- Pixel rate up to 133 million pixels per second for 2 textures each
- Texel bilinear fill rate up to 266 million texels per second
- High quality dithering

Video Acceleration Features

High Quality Video Processor

- High quality scaler (up or down) for both horizontal and vertical scaling (linear interpolation for horizontal and vertical p-scaling and filtering for horizontal and vertical down-scaling)
- Color enhancement for contrast, hue, saturation and brightness
- YUV-to-RGB color space conversion
- Bob, Weave de-interlacing mode and advanced de-interlacing to improve video quality
- 1 set of Color & Chroma key support

Video Overlay

- Supports video window overlay
- Hardware sub-picture blending

MPEG Video Playback

- MPEG-2 hardware motion compensation for full speed DVD playback
- High quality DVD video playback
- DVD playback auto-flipping
- DVD sub-picture playback overlay

Dual View+™ Capability

- Supports multi-monitor and extended desktop for Win98, WinME and WinXP
- Provides two independent display engines, each of which can display completely different information at different resolutions, pixel depths and refresh rates
- Improved display flexibility with simultaneous CRT / DVI, CRT / TV, DVI / TV and other combined operations

Full Software Support

- Microsoft DirectX 7.0, 8.0 and 9.0 compatible
- Supports OpenGL™
- Drivers for major operating systems and APIs: Windows® 9x/ME, Windows 2000, Windows XP, Direct3D™, DirectDraw™ and DirectShow™, and OpenGL™ ICD for Windows 9x/ME, and XP
- Windows NT 4.0 Standard VGA driver support

- **Extensive Display Support for External Video Output**
  - CRT display interface
  - Digital Video Port supporting TV-Out interface to TV encoder
  - 12-bit interface to external TMDS transmitter for driving a DVI monitor
  - 12-bit TV-Out interface to TV encoder

  ### CRT Display

  - CRT display interface with 24-bit true-color RAMDAC up to 250 MHz pixel rate with gamma correction capability
  - Supports CRT resolutions up to 1600x1200

  ### 12-bit TMDS Transmitter Interface

  - 12-bit, 1.5V low-swing, DVO interface for connecting DVI Monitor through TMDS transmitter
  - 12-bit DDR and clock rate up to 165 MHz
  - Built-in digital phase adjuster to fine tune signal timing between clock and data bus

  ### TV-Out interface

  - 12-bit Interface to external TV encoder for NTSC or PAL TV display

- **Advanced Graphics Power Management Support**
  - Built-in reference voltage generator and monitor sense circuits
  - Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down
  - External I/O signal controlling enabling graphics accelerator into standby / suspend-off state
  - Auto clock gating for each engine to achieve power saving
  - I^2C Serial Bus and DDC Monitor Communications for CRT Plug-and-Play configuration

KM400A System Overview

The KM400A is a high performance, cost-effective and energy efficient UMA North Bridge with integrated UniChrome graphics / video controller used for the implementation of desktop personal computer systems based on 400 / 333 / 266 / 200 CPU host bus ("Front Side Bus") for Socket-A AMD Athlon™ and AMD Duron™ processors.

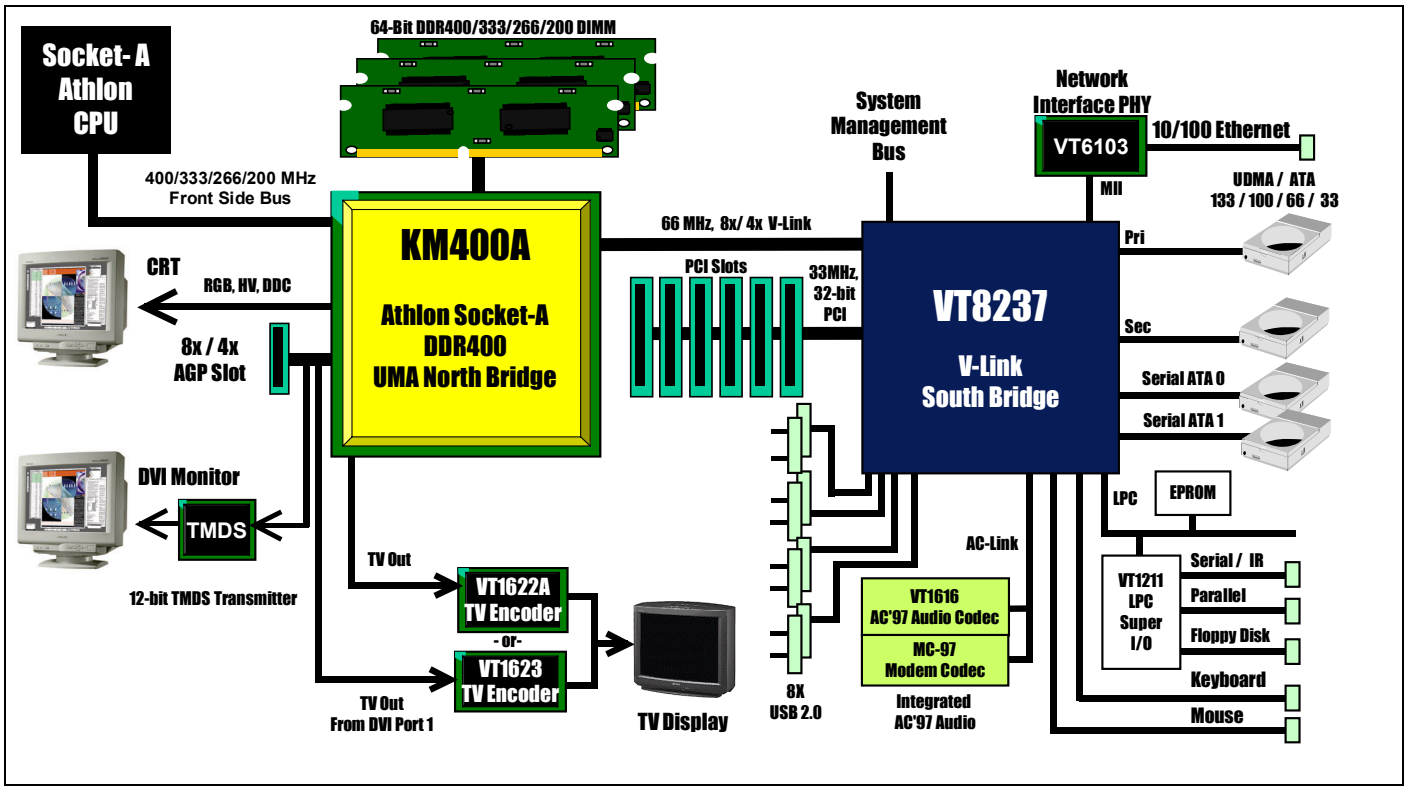


Figure 1. System Block Diagram

The complete desktop chipset consists of the KM400A North Bridge and the VT8237 V-Link South Bridge. The KM400A integrates VIA's most advanced system controller with high-performance UniChrome 3D / 2D graphics and video controller, LCD panel, DVI monitor and TV-Out interfaces. The KM400A provides superior performance between the CPU, DRAM, V-Link and internal or external AGP 8x graphics controller with pipelined, burst and concurrent operation. The VT8237 is a highly integrated peripheral controller which includes V-Link-to-PCI / V-Link-to-LPC controllers, Ultra DMA IDE controllers, Serial ATA controller, USB2.0 host controller, 10 / 100Mb networking MAC, AC97 and system power management controllers.

KM400A Overview

The KM400A supports 400 / 333 / 266 / 200 MHz FSB AMD Athlon XP and Duron processors; it implements a deep command (4-level), probe (4-level) and memory read/write/PCI command (8-level each) queues for optimal system performance. AMD PowerNow! technology is supported to reduce system power consumption while sustaining CPU's processing power.

The AGP controller is AGP v3.0 compliant with up to 2.1GB/second data transfer rate capability. . It supports pseudo-synchronous AGP and CPU interface to maximize system performance. Deep read and write (256 bytes each) FIFO are integrated for optimal bus utilization and minimum data transfer latency.

The KM400A supports dual 64-bit memory channel and up to 3 double-sided DDR400 / 333 / 266 SDRAM DIMMs for 6 GB maximum physical memory. The DDR SDRAM interface allows zero wait-state data transfer bursting between the DRAM and memory controller's data buffers. The different banks of DRAM can be composed of an arbitrary mixture of 64 / 128 / 256 / 512 / 1024 Mb SDRAM in x8 or x16 configurations. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus.

The KM400A North Bridge interfaces to the South Bridge through a high speed (up to 533 MB/sec) 8x 66 MHz Data Transfer interconnect bus called V-Link interface. Deep pre-fetch and post-write buffers are included to allow for concurrent CPU and V-Link operation. The combined KM400A North Bridge and VT8237 South Bridge system supports enhanced PCI bus commands such as "Memory-Read-Line", "Memory-Read-Multiple" and "Memory-Write-Invalid" commands to minimize snoop overhead. In addition, advanced features are supported such as CPU write-back forward to PCI master and CPU write-back merged with PCI post-write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The KM400A North Bridge also integrates a 128-bit graphics controller into the chip. This brings mainstream graphics performance to the Value PC with leading-edge 2D, 3D and DVD video acceleration into a cost effective package. Based on its capabilities, the KM400A is an ideal solution for the consumer, corporate desktop users and entry-level professionals.

System Power Management

For sophisticated power management, the KM400A supports dynamic CKE control to minimize DDR SDRAM power consumption during normal system state (S0). A separate suspend power plane is implemented for the memory control logic for Suspend-to-DRAM state. AMD PowerNow! Technology enables minimization of CPU power consumption while sustaining processing power. The KM400A graphics controller implements dynamic clock gating for inactive functions to achieve maximum power saving. The system can be switched to standby or suspend states to further reduce power consumption when idle. Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down are supported. Coupled with the VT8237 South Bridge chip, a complete power conscious PC main board can be implemented with no external glue logic.

3D Graphics Engine

Featuring an integrated 128-bit 3D graphics engine, the KM400A North Bridge utilizes a highly pipelined architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including two pixel rendering pipes, single-pass multitexturing, bump and cubic mapping, texture compression, edge anti-aliasing, vertex fog and fog table, hardware back-face culling, specular lighting, anisotropic filtering and an 8-bit stencil buffer. The chip also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. Image quality is further enhanced with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. The advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications.

2D Graphics Engine

The KM400A North Bridge's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. The enhanced 2D architecture with direct access frame buffer capability optimizes UMA performance and provides acceleration of all color depths.

MPEG Video Playback

The KM400A North Bridge provides the ideal architecture for high quality MPEG-2 based video applications. For MPEG video playback, the integrated video engine offloads the CPU by performing planar-to-packed format conversation and motion video compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback.

DVI Monitor and TV Output Display Support

Two 12-bit "Display Port" interfaces are provided (with functions multiplexed with AGP interface functions) plus a dedicated 12-bit display port interface. Multiplexing display functions with AGP bus allows desktop systems to support an external AGP connector for future performance upgrade through external graphics controller. It also allows add-in cards to be designed with an AGP-compatible connector for implementation of the display interface logic to reduce cost in the base (CRT-only) configuration. In value system configurations, external AGP upgrade capability is not normally required by the system, allowing all the AGP pins to be used for implementation of very flexible display functions.

One of the two AGP-multiplexed "Display Ports" implements 12-bit TMDS transmitter interface and is normally connected to external TMDS transmitter (such as VIA VT1632) to drive external DVI monitor via DVI interface connector, while the other AGP-multiplexed "Display Port" provides 12-bit interface to external TV encoder chip (such as VIA VT1623 and VT1623M) for display of video on a TV display. The dedicated 12-bit interface may optionally be configured for support of external TV encoder (such as VIA VT1622A and VT1622AM) as well.

The flexible display configurations of the KM400A allow support of a DVI monitor (TMDS interface), TV display and CRT display at the same time. Internally the KM400A North Bridge provides two separate display engines; if two display devices are connected, each can display completely different information at different resolution, pixel depth and refresh rate. The maximum display resolutions supported for one display device are listed in the table below. If more than one display is implemented (i.e, if both display engines are functioning at the same time), then available memory bandwidth may limit the display resolutions supported on one or both displays. This will be dependent on many factors including primarily clock rates and memory speeds (contact VIA for additional information).

High Screen Resolution Display Support

Resolutions Supported	Resolution Name	Pixel Depths Supported	System Memory Frame Buffer Size		
			16 MB	32 MB	64 MB
640x480 (4:3)	VGA	8 / 16 / 32	√	√	√
800x600 (4:3)	SVGA	8 / 16 / 32	√	√	√
1024x768 (4:3)	XGA	8 / 16 / 32	√	√	√
1280x1024 (5:4)	SXGA	8 / 16 / 32	√	√	√
1400x1050 (4:3)	SXGA+	8 / 16 / 32	√	√	√
1600x1200 (4:3)	UXGA	8 / 16 / 32	√	√	√

Table 1. Supported CRT and Panel Screen Resolutions

PINOUTS

Figure 2. Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND RGB	AG	AR	VCC PLL2	BIST IN	V SYNC	DP0D11 TVD11	DP0D7 TVD7	DP0D3 TVD3	DP0DET TVCKI	DP0DE TVDE	VCC 25	AIN 13#	AIN 4#	AIN 6#	AIN 11#	D10#	D12#	DI CLK0#	D4#	D16#	D27#	D25#	DI CLK1#	D29#	D19#
B	VCC QQ	GND DAC	AB	VCC PLL1	R SET	H SYNC	DP0D10 TVD10	DP0D6 TVD6	DP0D2 TVD2	DP0HS TVHS	DP0VS TVVS	VCC 25	GND	AIN 8#	AIN CLK#	GND	D0#	D8#	GND	D2#	D7#	GND	D26#	DO CLK1#	GND	D23#
C	AGP COMP	GND QQ	VCC RGB	VCC DAC	DCLK O	SP CLK2	DP0D9 TVD9	DP0D8 TVD8	DP0D1 TVD1	GND	VCC 25	VCC 25	AIN 14#	CON NECT	AIN 9#	AIN 3#	D14#	D11#	DO CLK0#	D3#	D5#	D18#	D21#	D31#	D20#	D30#
D	SBA 3#	SBA 0#	SBA 1#	GND PLL2	DCLK I	SP DAT2	SP DAT1	DP0CK TVCLK	DP0D0 TVD0	GPIO 0	VCC 25	VCC 25	GND	CKFWD RST	AIN 12#	GND	AIN 5#	D13#	GND	D1#	D17#	GND	D28#	D22#	D42#	D43#
E	SBSF (SBS)	SBSS (SBS#)	SBA 2#	G GNT	GND PLL1	XIN XDCLK	GP OUT	DP0D5 TVD5	DP0D4 TVD4	TEST IN1	VCC 25	VCC 25	DIN VAL#	PROC RDY	AIN 10#	AIN 7#	AIN 2#	D9#	D6#	D15#	D24#	D40#	GND	D41#	GND	D32#
F	SBA 5#	GND	ST1	GND	G REQ	INT A#	SP CLK1	VCC 25	VCC 25	VCC 25	GND	TEST IN0	GND	GND	VCC 25	VCC 25	S2K VREF	VCC 25	VCC 25	VCC 25	GND HCK	H CLK#	DO CLK2#	D45#	D44#	D33#
G	SBA 6#	SBA 7#	SBA 4#	GD31	ST0	AGP 8XDT#	G7	8	9	10	11	12	13	14	15	16	17	18	19	G20	H CLK	VCC HCK	DI CLK2#	D38#	D34#	D35#
H	GD28	GD30	GD29	GD27	GD25	AGP VREF	H	CRT Pins	DVI/TV Pins											H	VCC 25	D47#	GND	D39#	GND	D37#
J	GD24	GND	GD26	G DBIL	ST2	VCC AGP	J		GND	VCC DP	VCC DP	VCC DP	VTT	VTT	VTT	VTT	VTT	VTT	CPU Pins	J	VCC 25	D62#	D60#	D56#	D46#	D36#
K	GDS1S GDS1#	GDS1F GDS1	GBE 3	G RBF	GDBIH GPIPE	VCC 25	K		VCC AGP	K10	11	12	13	14	15	16	K17	VTT		K	GND S2K	D57#	D53#	D63#	D58#	D59#
L	GD20	GD22	GD23	GD21	G WBF	VCC 25	L		VCC AGP	L	GND	GND	GND	GND	GND	GND	L	VTT		L	S2K COMP	DO CLK3#	GND	DI CLK3#	GND	D48#
M	GD17	GND	GD18	GND	GD19	AGP VREF	M	AGP Pins	VCC AGP	M	GND	GND	GND	GND	GND	GND	M	VTT		M	VCC S2K	D55#	D51#	D52#	D50#	D49#
N	GBE 2	GD16	GD15	G DSEL	G FRM	VCC AGP	N		VCC AGP	N	GND	GND	GND	GND	GND	GND	N	VTT		N	S2K VREF	D54#	D61#	AOUT 4#	AOUT 6#	AOUT 2#
P	GD13	GD11	GD14	GBE 1	G IRDY	VCC AGP	P		VCC AGP	P	GND	GND	GND	GND	GND	GND	P	VTT		P	VCC 25	AOUT 3#	GND	AOUT 8#	GND	AOUT 5#
R	GD12	GND	GD10	G SERR	G TRDY	VCC AGP	R		VCC AGP	R	GND	GND	GND	GND	GND	GND	R	VTT		R	VCC 25	AOUT 9#	AOUT 12#	AOUT 14#	AOUT CLK#	AOUT 13#
T	GBE 0	GDS0S GDS0#	GDS0F GDS0	GD8	GD9	VCC AGP	T		VCC VL	T	GND	GND	GND	GND	GND	GND	T	VCC M		T	GND	AOUT 7#	AOUT 11#	AOUT 10#	VCC 25	VCC 25
U	GD6	GD5	GD7	G PAR	G STOP	VCC AGP	U		VCC VL	U10	11	12	13	14	15	16	U17	VCC M		U	GND	VCC 25	GND	VCC 25	GND	VCC 25
V	GD4	GND	GD2	GND	G CLK	VCC 25	V	Vlink Pins	VCC M	VCC M	VCC M	VCC M	VCC M	VCC M	VCC M	VCC M	VCC M	VCC M		V	VCC 25	VCC 25	VCC 25	VCC 25	VCC 25	VCC 25
W	GD1	GD0	GD3	VAD 0	VAD 1	VCC 25	W						DDR SDRAM Pins							W	VCC 25	VCC 25	MD0	MD1	MD5	MD4
Y	VAD 3	VAD 5	VBE#	VUP CMD	VL VREF	VCC VL	Y7	8	9	10	11	12	13	14	15	16	17	18	19	Y20	GND MCK	MCLK	GND	DQS 0#	GND	DQM 0
AA	VUP STB	VUP STB#	GND	VAD 2	GND	VCC VL	VCC M	VCC 25	VCC 25	M VREF	VCC 25	VCC 25	GND MDLL	VCC MDLL	VCC M	VCC 25	VCC 25	M VREF	VCC 25	VCC 25	VCC M	VCC MCK	MCLK FB	MD7	MD2	MD6
AB	VDN STB	VDN STB#	VDN CMD	VAD 6	VL COMP	CS3#	CS4#	DQM 6	S WEA#	MA10	S RASA#	MA1	MD45	MA3	MA6	MA4	MA5	MA13	MA14	CKE4 SRASC#	MD23	CKE2 SWEB#	MD12	MD9	MD8	MD3
AC	VAD 7	VAD 4	GND	GND	CS1#	CS2#	GND	DQS 6#	MA11	GND	MA0	MA2	GND	MD34	MD33	GND	MA9	MA7	GND	MD24	CKE0 SWEC#	GND	MD20	CKE3 SCASB#	GND	MD13
AD	PWR OK	SUS ST#	VSUS 25	DQS 7#	CS5#	CS0#	S CASA#	MD55	MD53	MD47	MD42	MD41	MD44	MD38	MD37	MD36	MD31	MD27	DQS 3#	MD28	MD18	DQM 2	MD16	CKE1 SCASC#	DQM 1	DQS 1#
AE	RE SET#	GND	MD58	GND	MD61	MD56	GND	MD50	MD49	GND	MD46	DQS 5#	GND	MD35	DQM 4	GND	MA8	MD30	GND	MD29	MD22	GND	MD17	MD11	GND	MD14
AF	MD59	MD63	MD62	DQM 7	MD57	MD60	MD51	MD54	MD52	MD48	MD43	DQM 5	MD40	MD39	DQS 4#	MD32	MA12	MD26	DQM 3	MD25	MD19	DQS 2#	MD21	CKE5 SRASB#	MD10	MD15

Figure 3. Ball Diagram (Top View) – Digital Video Output Enabled on AGP Pins

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND RGB	AG	AR	VCC PLL2	BIST IN	V SYNC	DP0D11 TVD11	DP0D7 TVD7	DP0D3 TVD3	DP0DET TVCKI	DP0DE TVDE	VCC 25	AIN 13#	AIN 4#	AIN 6#	AIN 11#	D10#	D12#	DI CLK0#	D4#	D16#	D27#	D25#	DI CLK1#	D29#	D19#
B	VCC QQ	GND DAC	AB	VCC PLL1	R SET	H SYNC	DP0D10 TVD10	DP0D6 TVD6	DP0D2 TVD2	DP0HS TVHS	DP0VS TVVS	VCC 25	GND	AIN 8#	AIN CLK#	GND	D0#	D8#	GND	D2#	D7#	GND	D26#	DO CLK1#	GND	D23#
C	AGP COMP	GND QQ	VCC RGB	VCC DAC	DCLK O	SP CLK2	DP0D9 TVD9	DP0D8 TVD8	DP0D1 TVD1	GND	VCC 25	VCC 25	AIN 14#	CON NECT	AIN 9#	AIN 3#	D14#	D11#	DO CLK0#	D3#	D5#	D18#	D21#	D31#	D20#	D30#
D	DP1 HS	DP1 VS	DP1 DE	GND PLL2	DCLK I	SP DAT2	SP DAT1	DP0CK TVCLK	DP0D0 TVD0	GPIO 0	VCC 25	VCC 25	GND	CKFWD RST	AIN 12#	GND	AIN 5#	D13#	GND	D1#	D17#	GND	D28#	D22#	D42#	D43#
E	DP1 D01	DP1 D02	DP1 D00	DDC DA	GND PLL1	XIN XDCLK	GP OUT	DP0D5 TVD5	DP0D4 TVD4	TEST IN1	VCC 25	VCC 25	DIN VAL#	PROC RDY	AIN 10#	AIN 7#	AIN 2#	D9#	D6#	D15#	D24#	D40#	GND	D41#	GND	D32#
F	DP1 D03	GND	ENA VDD	GND	DDC CK	INT A#	SP CLK1	VCC 25	VCC 25	VCC 25	GND	TEST IN0	GND	GND	VCC 25	VCC 25	S2K VREF	VCC 25	VCC 25	VCC 25	GND HCK	H CLK#	DO CLK2#	D45#	D44#	D33#
G	DP1 CLK	DP1 CLK#	DP1 D05	DP1 DET	ENA VEE	NC	G7	8	9	10	11	12	13	14	15	16	17	18	19	G20	H CLK	VCC HCK	DI CLK2#	D38#	D34#	D35#
H	DP1 D07	DP1 D08	DP1 D06	DP1 D04	NC	AGP VREF	H	CRT	DVI Port0 / TV Pins											H	VCC 25	D47#	GND	D39#	GND	D37#
J	DP1 D09	GND	DP1 D10	NC	ENA BLT	VCC AGP	J	Pins	GND	VCC DP	VCC DP	VCC DP	VTT	VTT	VTT	VTT	VTT	VTT	CPU	J	VCC 25	D62#	D60#	D56#	D46#	D36#
K	DP2 DET	DP2 D00	DP1 D11	NC	NC	VCC 25	K	DVI	VCC AGP	K10	11	12	13	14	15	16	K17	VTT	Pins	K	GND S2K	D57#	D53#	D63#	D58#	D59#
L	DP2 D02	DP2 D01	DP2 D03	DP2 CLK	DP2 CLK#	VCC 25	L	Port1	VCC AGP	L	GND	GND	GND	GND	GND	GND	L	VTT		L	S2K COMP	DO CLK3#	GND	DI CLK3#	GND	D48#
M	DP2 D05	GND	DP2 D04	GND	DP2 DE	AGP VREF	M	DVI	VCC AGP	M	GND	GND	GND	GND	GND	GND	M	VTT		M	VCC S2K	D55#	D51#	D52#	D50#	D49#
N	DP2 D07	DP2 D06	DP2 D08	DP2 VS	DP2 HS	VCC AGP	N	Port2	VCC AGP	N	GND	GND	GND	GND	GND	GND	N	VTT		N	S2K VREF	D54#	D61#	AOUT 4#	AOUT 6#	AOUT 2#
P	DP2 D10	DP2 D11	DP2 D09	SB DAT	SB CLK	VCC AGP	P	Pins	VCC AGP	P	GND	GND	GND	GND	GND	GND	P	VTT		P	VCC 25	AOUT 3#	GND	AOUT 8#	GND	AOUT 5#
R	DP3 D00	GND	DP3 D01	DP3 DE	NC	VCC AGP	R	DVI	VCC AGP	R	GND	GND	GND	GND	GND	GND	R	VTT		R	VCC 25	AOUT 9#	AOUT 12#	AOUT 14#	AOUT CLK#	AOUT 13#
T	DP3 D03	DP3 D02	DP3 D04	DP3 DET	DP3 HS	VCC AGP	T	Port3	VCC VL	T	GND	GND	GND	GND	GND	GND	T	VCC M		T	GND	AOUT 7#	AOUT 11#	AOUT 10#	VCC 25	VCC 25
U	DP3 D06	DP3 D07	DP3 D05	DP3 VS	DP3 CLK#	VCC AGP	U	Pins	VCC VL	U10	11	12	13	14	15	16	U17	VCC M		U	GND	VCC 25	GND	VCC 25	GND	VCC 25
V	DP3 D08	GND	DP3 CLK	GND	G CLK	VCC 25	V	Vlink	VCC M	VCC M	VCC M	VCC M	VCC M	VCC M	VCC M	VCC M	VCC M	VCC M		V	VCC 25	VCC 25	VCC 25	VCC 25	VCC 25	VCC 25
W	DP3 D11	DP3 D10	DP3 D09	VAD 0	VAD 1	VCC 25	W	Pins	DDR SDRAM Pins											W	VCC 25	VCC 25	MD0	MD1	MD5	MD4
Y	VAD 3	VAD 5	VBE#	VUP CMD	VL VREF	VCC VL	Y7	8	9	10	11	12	13	14	15	16	17	18	19	Y20	GND MCK	MCLK	GND	DQS 0#	GND	DQM 0
AA	VUP STB	VUP STB#	GND	VAD 2	GND	VCC VL	VCC M	VCC 25	VCC 25	M VREF	VCC 25	VCC 25	GND	VCC 25	VCC M	VCC 25	VCC 25	M VREF	VCC 25	VCC 25	VCC M	VCC MCK	MCLK FB	MD7	MD2	MD6
AB	VDN STB	VDN STB#	VDN CMD	VAD 6	VL COMP	CS3#	CS4#	DQM 6	S WEA#	MA10	S RASA#	MA1	MD45	MA3	MA6	MA4	MA5	MA13	MA14	CKE4 SRASC#	MD23	CKE2 SWEB#	MD12	MD9	MD8	MD3
AC	VAD 7	VAD 4	GND	GND	CS1#	CS2#	GND	DQS 6#	MA11	GND	MA0	MA2	GND	MD34	MD33	GND	MA9	MA7	GND	MD24	CKE0 SWEC#	GND	MD20	CKE3 SCASB#	GND	MD13
AD	PWR OK	SUS ST#	VSUS 25	DQS 7#	CS5#	CS0#	S CASA#	MD55	MD53	MD47	MD42	MD41	MD44	MD38	MD37	MD36	MD31	MD27	DQS 3#	MD28	MD18	DQM 2	MD16	CKE1 SCASC#	DQM 1	DQS 1#
AE	RE SET#	GND	MD58	GND	MD61	MD56	GND	MD50	MD49	GND	MD46	DQS 5#	GND	MD35	DQM 4	GND	MA8	MD30	GND	MD29	MD22	GND	MD17	MD11	GND	MD14
AF	MD59	MD63	MD62	DQM 7	MD57	MD60	MD51	MD54	MD52	MD48	MD43	DQM 5	MD40	MD39	DQS 4#	MD32	MA12	MD26	DQM 3	MD25	MD19	DQS 2#	MD21	CKE5 SRASB#	MD10	MD15

Table 2. Pin List (Listed by Pin Number)

Pin #		Pin Name
A01	**P**	**GNDRGB**
A02	O	AG
A03	O	AR
A04	**P**	**VCCPLL2**
A05	I	BISTIN
A06	O	VSYNC
A07	O	DP0D11 / TVD11
A08	O	DP0D07 / TVD7
A09	O	DP0D03 / TVD3
A10	OI	DP0DET/TVCKI
A11	IO	DP0DE / TVDE
A12	**P**	**VCC25**
A13	O	AIN13#
A14	O	AIN04#
A15	O	AIN06#
A16	O	AIN11#
A17	IO	D10#
A18	IO	D12#
A19	O	DICLK0#
A20	IO	D04#
A21	IO	D16#
A22	IO	D27#
A23	IO	D25#
A24	O	DICLK1#
A25	IO	D29#
A26	IO	D19#
B01	**P**	**VCCOO**
B02	**P**	**GNDDAC**
B03	O	AB
B04	**P**	**VCCPLL1**
B05	A	RSET
B06	O	HSYNC
B07	O	DP0D10 / TVD10
B08	O	DP0D06 / TVD6
B09	O	DP0D02 / TVD2
B10	O	DP0HS / TVHS
B11	O	DP0VS / TVVS
B12	**P**	**VCC25**
B13	**P**	**GND**
B14	O	AIN08#
B15	O	AINCLK#
B16	**P**	**GND**
B17	IO	D00#
B18	IO	D08#
B19	**P**	**GND**
B20	IO	D02#
B21	IO	D07#
B22	**P**	**GND**
B23	IO	D26#
B24	I	DOCLK1#
B25	**P**	**GND**
B26	IO	D23#
C01	AI	AGPCOMP
C02	**P**	**GNDQQ**
C03	**P**	**VCCRGB**
C04	**P**	**VCCDAC**
C05	O	DCLKO
C06	IO	SPCLK2
C07	O	DP0D09 / TVD9
C08	O	DP0D08 / TVD8
C09	O	DP0D01 / TVD1
C10	**P**	**GND**
C11	**P**	**VCC25**
C12	**P**	**VCC25**
C13	O	AIN14#
C14	O	CONNECT
C15	O	AIN09#
C16	O	AIN03#
C17	IO	D14#
C18	IO	D11#
C19	I	DOCLK0#
C20	IO	D03#
C21	IO	D05#
C22	IO	D18#
C23	IO	D21#
C24	IO	D31#
C25	IO	D20#
C26	IO	D30#
D01	I	SBA3# / DP1HS
D02	I	SBA0# / DP1VS
D03	I	SBA1# / DP1DE
D04	**P**	**GNDPLL2**
D05	I	DCLKI
D06	IO	SPDAT2
D07	IO	SPDAT1
D08	O	DP0CLK/TVCK
D09	O	DP0D00 / TVD0
D10	IO	GPIO0
D11	**P**	**VCC25**
D12	**P**	**VCC25**
D13	**P**	**GND**
D14	O	CFWDRST
D15	O	AIN12#
D16	**P**	**GND**
D17	O	AIN05#
D18	IO	D13#
D19	**P**	**GND**
D20	IO	D01#
D21	IO	D17#
D22	**P**	**GND**
D23	IO	D28#
D24	IO	D22#
D25	IO	D42#
D26	IO	D43#
E01	I	SBSF / DP1D01
E02	I	SBSS / DP1D02
E03	I	SBA2# /DP1D00
E04	O	GGNT /DDCDA
E05	**P**	**GNDPLL1**
E06	I	XIN
E07	IO	GPOUT
E08	O	DP0D05 / TVD5
E09	O	DP0D04 / TVD4
E10	I	TESTIN1
E11	**P**	**VCC25**
E12	**P**	**VCC25**
E13	O	DINVAL#
E14	I	PROCRDY
E15	O	AIN10#
E16	O	AIN07#
E17	O	AIN02#
E18	IO	D09#
E19	IO	D06#
E20	IO	D15#
E21	IO	D24#
E22	IO	D40#
E23	**P**	**GND**
E24	IO	D41#
E25	**P**	**GND**
E26	IO	D32#
F01	I	SBA5# / DP1D3
F02	**P**	**GND**
F03	O	ST1 / ENAVDD
F04	**P**	**GND**
F05	I	GREO / DDCCK
F06	O	INTA#
F07	IO	SPCLK1
F08	**P**	**VCC25**
F09	**P**	**VCC25**
F10	**P**	**VCC25**
F11	**P**	**GND**
F12	I	TESTIN0
F13	**P**	**GND**
F14	**P**	**GND**
F15	**P**	**VCC25**
F16	**P**	**VCC25**
F17	**P**	**S2KVREF**
F18	**P**	**VCC25**
F19	**P**	**VCC25**
F20	**P**	**VCC25**
F21	**P**	**GNDHCK**
F22	I	HCLK#
F23	I	DOCLK2#
F24	IO	D45#
F25	IO	D44#
F26	IO	D33#
G01	I	SBA6# / DP1CK
G02	I	SBA7# /DP1CK#
G03	I	SBA4# / DP1VS
G04	IO	GD31 / DP1DET
G05	O	ST0 / ENAVEE
G06	I	AGP8XDT#
G21	I	HCLK
G22	**P**	**VCCHCK**
G23	O	DICLK2#
G24	IO	D38#
G25	IO	D34#
G26	IO	D35#
H01	IO	GD28 / DP1D7
H02	IO	GD30 / DP1D8
H03	IO	GD29 / DP1D6
H04	IO	GD27 / DP1D4
H05	IO	GD25
H06	**P**	**AGPVREF**
H21	**P**	**VCC25**
H22	IO	D47#
H23	**P**	**GND**
H24	IO	D39#
H25	**P**	**GND**
H26	IO	D37#
J01	IO	GD24 / DP1D9
J02	**P**	**GND**
J03	IO	GD26 / DP1D10
J04	IO	GDBIL
J05	O	ST2 / ENABLT
J06	**P**	**VCCAGP**
J21	**P**	**VCC25**
J22	IO	D62#
J23	IO	D60#
J24	IO	D56#
J25	IO	D46#
J26	IO	D36#
K01	IO	GDS1S/DP2DET
K02	IO	GDS1F/DP2D00
K03	IO	GBE3 /DP1D11
K04	I	GRBF
K05	I	GDBIH / GPIPE
K06	**P**	**VCC25**
K21	**P**	**GNDS2K**
K22	IO	D57#
K23	IO	D53#
K24	IO	D63#
K25	IO	D58#
K26	IO	D59#
L01	IO	GD20 / DP2D02
L02	IO	GD22 / DP2D01
L03	IO	GD23 / DP2D03
L04	IO	GD21 / DP2CK
L05	I	GWBF/DP2CK#
L06	**P**	**VCC25**
L21	A	S2KCOMP
L22	I	DOCLK3#
L23	**P**	**GND**
L24	O	DICLK3#
L25	**P**	**GND**
L26	IO	D48#
M01	IO	GD17 / DP2D05
M02	**P**	**GND**
M03	IO	GD18 / DP2D04
M04	**P**	**GND**
M05	IO	GD19 / DP2DE
M06	**P**	**AGPVREF**
M21	**P**	**VCCS2K**
M22	IO	D55#
M23	IO	D51#
M24	IO	D52#
M25	IO	D50#
M26	IO	D49#
N01	IO	GBE2 / DP2D07
N02	IO	GD16 / DP2D06
N03	IO	GD15 / DP2D08
N04	IO	GDSEL / DP2VS
N05	IO	GFRM / DP2HS
N06	**P**	**VCCAGP**
N21	**P**	**S2KVREF**
N22	IO	D54#
N23	IO	D61#
N24	I	AOUT04#
N25	I	AOUT06#
N26	I	AOUT02#
P01	IO	GD13 / DP2D10
P02	IO	GD11 / DP2D11
P03	IO	GD14 / DP2D09
P04	IO	GBE1 / SBDA
P05	IO	GIRDY/ SBCK
P06	**P**	**VCCAGP**
P21	**P**	**VCC25**
P22	I	AOUT03#
P23	**P**	**GND**
P24	I	AOUT08#
P25	**P**	**GND**
P26	I	AOUT05#
R01	IO	GD12 / DP3D00
R02	**P**	**GND**
R03	IO	GD10 / DP3D01
R04	IO	GSERR /DP3DE
R05	IO	GTRDY
R06	**P**	**VCCAGP**
R21	**P**	**VCC25**
R22	I	AOUT09#
R23	I	AOUT12#
R24	I	AOUT14#
R25	I	AOUTCLK#
R26	I	AOUT13#
T01	IO	GBE0 / DP3D03
T02	IO	GDS0S/DP3D02
T03	IO	GDS0F/DP3D04
T04	IO	GD08 / DP3DET
T05	IO	GD09 / DP3HS
T06	**P**	**VCCAGP**
T21	**P**	**GND**
T22	I	AOUT07#
T23	I	AOUT11#
T24	I	AOUT10#
T25	**P**	**VCC25**
T26	**P**	**VCC25**
U01	IO	GD06 / DP3D06
U02	IO	GD05 / DP3D07
U03	IO	GD07 / DP3D05
U04	IO	GPAR / DP3VS
U05	IO	GSTP /DP3CK#
U06	**P**	**VCCAGP**
U21	**P**	**GND**
U22	**P**	**VCC25**
U23	**P**	**GND**
U24	**P**	**VCC25**
U25	**P**	**GND**
U26	**P**	**VCC25**
V01	IO	GD04 / DP3D08
V02	**P**	**GND**
V03	IO	GD02 / DP3CK
V04	**P**	**GND**
V05	I	GCLK
V06	**P**	**VCC25**
V21	**P**	**VCC25**
V22	**P**	**VCC25**
V23	**P**	**VCC25**
V24	**P**	**VCC25**
V25	**P**	**VCC25**
V26	**P**	**VCC25**
W01	IO	GD01 / DP3D11
W02	IO	GD00 / DP3D10
W03	IO	GD03 / DP3D09
W04	IO	VAD0
W05	IO	VAD1
W06	**P**	**VCC25**
W21	**P**	**VCC25**
W22	**P**	**VCC25**
W23	IO	MD00
W24	IO	MD01
W25	IO	MD05
W26	IO	MD04
Y01	IO	VAD3
Y02	IO	VAD5
Y03	IO	VBE#
Y04	I	VUPCMD
Y05	**P**	**VLVREF**
Y06	**P**	**VCCVL**
Y21	**P**	**GNDMCK**
Y22	O	MCLK
Y23	**P**	**GND**
Y24	O	DQS0#
Y25	**P**	**GND**
Y26	O	DQM0
AA01	I	VUPSTB
AA02	I	VUPSTB#
AA03	**P**	**GND**
AA04	IO	VAD2
AA05	**P**	**GND**
AA06	**P**	**VCCVL**
AA07	**P**	**VCCM**
AA08	**P**	**VCC25**
AA09	**P**	**VCC25**
AA10	**P**	**MEMVREF**
AA11	**P**	**VCC25**
AA12	**P**	**VCC25**
AA13	**P**	**GND**
AA14	**P**	**VCC25**
AA15	**P**	**VCCM**
AA16	**P**	**VCC25**
AA17	**P**	**VCC25**
AA18	**P**	**MEMVREF**
AA19	**P**	**VCC25**
AA20	**P**	**VCC25**
AA21	**P**	**VCCM**
AA22	**P**	**VCCMCK**
AA23	I	MCLKFB
AA24	IO	MD07
AA25	IO	MD02
AA26	IO	MD06
AB01	O	VDNSTB
AB02	O	VDNSTB#
AB03	O	VDNCMD
AB04	IO	VAD6
AB05	**A**	**VLCOMP**
AB06	O	CS3#
AB07	O	CS4#
AB08	O	DQM6
AB09	O	SWEA# / strap
AB10	O	MA10 / strap
AB11	O	SRASA# / strap
AB12	O	MA01 / strap
AB13	IO	MD45
AB14	O	MA03 / strap
AB15	O	MA06 / strap
AB16	O	MA04 / strap
AB17	O	MA05 / strap
AB18	O	MA13 / strap
AB19	O	MA14 / strap
AB20	O	CKE4 / SRASC#
AB21	IO	MD23
AB22	O	CKE2 / SWEB#
AB23	IO	MD12
AB24	IO	MD09
AB25	IO	MD08
AB26	IO	MD03
AC01	IO	VAD7
AC02	IO	VAD4
AC03	**P**	**GND**
AC04	**P**	**GND**
AC05	O	CS1#
AC06	O	CS2#
AC07	**P**	**GND**
AC08	O	DQS6#
AC09	O	MA11 / strap
AC10	**P**	**GND**
AC11	O	MA00 / strap
AC12	O	MA02 / strap
AC13	**P**	**GND**
AC14	IO	MD34
AC15	IO	MD33
AC16	**P**	**GND**
AC17	O	MA09 / strap
AC18	O	MA07 / strap
AC19	**P**	**GND**
AC20	IO	MD24
AC21	O	CKE0 / SWEC#
AC22	**P**	**GND**
AC23	IO	MD20
AC24	O	CKE3 / SCASB#
AC25	**P**	**GND**
AC26	IO	MD13
AD01	I	PWROK
AD02	I	SUSST#
AD03	**P**	**VSUS25**
AD04	O	DQS7#
AD05	O	CS5#
AD06	O	CS0#
AD07	O	SCASA# / strap
AD08	IO	MD55
AD09	IO	MD53
AD10	IO	MD47
AD11	IO	MD42
AD12	IO	MD41
AD13	IO	MD44
AD14	IO	MD38
AD15	IO	MD37
AD16	IO	MD36
AD17	IO	MD31
AD18	IO	MD27
AD19	O	DQS3#
AD20	IO	MD28
AD21	IO	MD18
AD22	O	DQM2
AD23	IO	MD16
AD24	O	CKE1 / SCASC#
AD25	O	DQM1
AD26	O	DQS1#
AE01	I	RESET#
AE02	**P**	**GND**
AE03	IO	MD58
AE04	**P**	**GND**
AE05	IO	MD61
AE06	IO	MD56
AE07	**P**	**GND**
AE08	IO	MD50
AE09	IO	MD49
AE10	**P**	**GND**
AE11	IO	MD46
AE12	O	DQS5#
AE13	**P**	**GND**
AE14	IO	MD35
AE15	O	DQM4
AE16	**P**	**GND**
AE17	O	MA08 / strap
AE18	IO	MD30
AE19	**P**	**GND**
AE20	IO	MD29
AE21	IO	MD22
AE22	**P**	**GND**
AE23	IO	MD17
AE24	IO	MD11
AE25	**P**	**GND**
AE26	IO	MD14
AF01	IO	MD59
AF02	IO	MD63
AF03	IO	MD62
AF04	O	DQM7
AF05	IO	MD57
AF06	IO	MD60
AF07	IO	MD51
AF08	IO	MD54
AF09	IO	MD52
AF10	IO	MD48
AF11	IO	MD43
AF12	O	DQM5
AF13	IO	MD40
AF14	IO	MD39
AF15	O	DQS4#
AF16	IO	MD32
AF17	O	MA12 / strap
AF18	IO	MD26
AF19	O	DQM3
AF20	IO	MD25
AF21	IO	MD19
AF22	O	DQS2#
AF23	IO	MD21
AF24	O	CKE5 / SRASB#
AF25	IO	MD10
AF26	IO	MD15

Center **VTT** Pins (12 pins): **J13-18, K18, L18, M18, N18, P18, R18**
Center **VCCVL** Pin (2 pins)s **T9, U9**
Center **VCCAGP** pins (6 pins): **K9, L9, M9, N9, P9, R9**
Center **GND** Pins (37 pins): **J9, L11-16, M11-16, N11-16, P11-16, R11-16, T11-16**
Center **VCCDP** Pins (3 pins): **J10-12**
Center **VCCM** Pins (12 pins): **T18, U18, V9-18**

Table 3. Pin List (Listed by Pin Name)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
B03	O	AB	C26	IO	D30#	N01	IO	GBE2 / DP2D07	**AA03**	**P**	**GND**	AF23	IO	MD21	Y02	IO	VAD5
A02	O	AG	C24	IO	D31#	K03	IO	GBE3 / DP1D11	**AA05**	**P**	**GND**	AE21	IO	MD22	AB04	IO	VAD6
G06	I	AGP8XDT#	E26	IO	D32#	V05	I	GCLK	**AA13**	**P**	**GND**	AB21	IO	MD23	AC01	IO	VAD7
C01	AI	AGPCOMP	F26	IO	D33#	W02	IO	GD00 / DP3D10	**AC03**	**P**	**GND**	AC20	IO	MD24	Y03	IO	VBE#
H06	**P**	**AGPVREF**	G25	IO	D34#	W01	IO	GD01 / DP3D11	**AC04**	**P**	**GND**	AF20	IO	MD25	**A12**	**P**	**VCC25**
M06	**P**	**AGPVREF**	G26	IO	D35#	V03	IO	GD02 / DP3CK	**AC07**	**P**	**GND**	AF18	IO	MD26	**B12**	**P**	**VCC25**
E17	O	AIN02#	J26	IO	D36#	W03	IO	GD03 / DP3D09	**AC10**	**P**	**GND**	AD18	IO	MD27	**C11**	**P**	**VCC25**
C16	O	AIN03#	H26	IO	D37#	V01	IO	GD04 / DP3D08	**AC13**	**P**	**GND**	AD20	IO	MD28	**C12**	**P**	**VCC25**
A14	O	AIN04#	G24	IO	D38#	U02	IO	GD05 / DP3D07	**AC16**	**P**	**GND**	AE20	IO	MD29	**D11**	**P**	**VCC25**
D17	O	AIN05#	H24	IO	D39#	U01	IO	GD06 / DP3D06	**AC19**	**P**	**GND**	AE18	IO	MD30	**D12**	**P**	**VCC25**
A15	O	AIN06#	E22	IO	D40#	U03	IO	GD07 / DP3D05	**AC22**	**P**	**GND**	AD17	IO	MD31	**E11**	**P**	**VCC25**
E16	O	AIN07#	E24	IO	D41#	T04	IO	GD08 / DP3DET	**AC25**	**P**	**GND**	AF16	IO	MD32	**E12**	**P**	**VCC25**
B14	O	AIN08#	D25	IO	D42#	T05	IO	GD09 / DP3HS	**AE02**	**P**	**GND**	AC15	IO	MD33	**F08**	**P**	**VCC25**
C15	O	AIN09#	D26	IO	D43#	R03	IO	GD10 / DP3D01	**AE04**	**P**	**GND**	AC14	IO	MD34	**F09**	**P**	**VCC25**
E15	O	AIN10#	F25	IO	D44#	P02	IO	GD11 / DP2D11	**AE07**	**P**	**GND**	AE14	IO	MD35	**F10**	**P**	**VCC25**
A16	O	AIN11#	F24	IO	D45#	R01	IO	GD12 / DP3D00	**AE10**	**P**	**GND**	AD16	IO	MD36	**F15**	**P**	**VCC25**
D15	O	AIN12#	J25	IO	D46#	P01	IO	GD13 / DP2D10	**AE13**	**P**	**GND**	AD15	IO	MD37	**F16**	**P**	**VCC25**
A13	O	AIN13#	H22	IO	D47#	P03	IO	GD14 / DP2D09	**AE16**	**P**	**GND**	AD14	IO	MD38	**F18**	**P**	**VCC25**
C13	O	AIN14#	L26	IO	D48#	N03	IO	GD15 / DP2D08	**AE19**	**P**	**GND**	AF14	IO	MD39	**F19**	**P**	**VCC25**
B15	O	AINCLK#	M26	IO	D49#	N02	IO	GD16 / DP2D06	**AE22**	**P**	**GND**	AF13	IO	MD40	**F20**	**P**	**VCC25**
N26	I	AOUT02#	M25	IO	D50#	M01	IO	GD17 / DP2D05	**AE25**	**P**	**GND**	AD12	IO	MD41	**H21**	**P**	**VCC25**
P22	I	AOUT03#	M23	IO	D51#	M03	IO	GD18 / DP2D04	**B02**	**P**	**GNDDAC**	AD11	IO	MD42	**J21**	**P**	**VCC25**
N24	I	AOUT04#	M24	IO	D52#	M05	IO	GD19 / DP2DE	**F21**	**P**	**GNDHCK**	AF11	IO	MD43	**K06**	**P**	**VCC25**
P26	I	AOUT05#	K23	IO	D53#	L01	IO	GD20 / DP2D02	**Y21**	**P**	**GNDMCK**	AD13	IO	MD44	**L06**	**P**	**VCC25**
N25	I	AOUT06#	N22	IO	D54#	L04	IO	GD21 / DP2CK	**E05**	**P**	**GNDPLL1**	AB13	IO	MD45	**P21**	**P**	**VCC25**
T22	I	AOUT07#	M22	IO	D55#	L02	IO	GD22 / DP2D01	**D04**	**P**	**GNDPLL2**	AE11	IO	MD46	**R21**	**P**	**VCC25**
P24	I	AOUT08#	J24	IO	D56#	L03	IO	GD23 / DP2D03	**C02**	**P**	**GNDQQ**	AD10	IO	MD47	**T25**	**P**	**VCC25**
R22	I	AOUT09#	K22	IO	D57#	J01	IO	GD24 / DP1D9	**A01**	**P**	**GNDRGB**	AF10	IO	MD48	**T26**	**P**	**VCC25**
T24	I	AOUT10#	K25	IO	D58#	H05	IO	GD25	**K21**	**P**	**GNDS2K**	AE09	IO	MD49	**U22**	**P**	**VCC25**
T23	I	AOUT11#	K26	IO	D59#	J03	IO	GD26 / DP1D10	U04	IO	GPAR / DP3VS	AE08	IO	MD50	**U24**	**P**	**VCC25**
R23	I	AOUT12#	J23	IO	D60#	H04	IO	GD27 / DP1D04	D10	IO	GPIO0	AF07	IO	MD51	**U26**	**P**	**VCC25**
R26	I	AOUT13#	N23	IO	D61#	H01	IO	GD28 / DP1D7	E07	IO	GPOUT	AF09	IO	MD52	**V06**	**P**	**VCC25**
R24	I	AOUT14#	J22	IO	D62#	H03	IO	GD29 / DP1D6	K04	I	GRBF	AD09	IO	MD53	**V21**	**P**	**VCC25**
R25	I	AOUTCLK#	K24	IO	D63#	H02	IO	GD30 / DP1D8	F05	I	GREQ / DDCCK	AF08	IO	MD54	**V22**	**P**	**VCC25**
A03	O	AR	D05	I	DCLKI	G04	IO	GD31 / DP1DET	R04	IO	GSERR / DP3DE	AD08	IO	MD55	**V23**	**P**	**VCC25**
A05	I	BISTIN	C05	O	DCLKO	K05	I	GDBIH / GPIPE	U05	IO	GSTOP/DP3CK#	AE06	IO	MD56	**V24**	**P**	**VCC25**
D14	O	CFWDRST	A19	O	DICLK0#	J04	IO	GDBIL	R05	IO	GTRDY	AF05	IO	MD57	**V25**	**P**	**VCC25**
AC21	O	CKE0 / SWEC#	A24	O	DICLK1#	T03	IO	GDS0F /DP3D04	L05	I	GWBF /DP2CK#	AE03	IO	MD58	**V26**	**P**	**VCC25**
AD24	O	CKE1 / SCASC#	G23	O	DICLK2#	T02	IO	GDS0S /DP3D02	G21	I	HCLK	AF01	IO	MD59	**W06**	**P**	**VCC25**
AB22	O	CKE2 / SWEB#	L24	O	DICLK3#	K02	IO	GDS1F /DP2D00	F22	I	HCLK#	AF06	IO	MD60	**W21**	**P**	**VCC25**
AC24	O	CKE3 / SCASB#	E13	O	DINVAL#	K01	IO	GDS1S/DP2DET	B06	O	HSYNC	AE05	IO	MD61	**W22**	**P**	**VCC25**
AB20	O	CKE4 / SRASC#	C19	I	DOCLK0#	N04	IO	GDSEL / DP2VS	F06	O	INTA#	AF03	IO	MD62	**AA08**	**P**	**VCC25**
AF24	O	CKE5 / SRASB#	B24	I	DOCLK1#	N05	IO	GFRM / DP2HS	AC11	O	MA00 / strap	AF02	IO	MD63	**AA09**	**P**	**VCC25**
C14	O	CONNECT	F23	I	DOCLK2#	E04	O	GGNT /DDCDA	AB12	O	MA01 / strap	**AA10**	**P**	**MEMVREF**	**AA11**	**P**	**VCC25**
AD06	O	CS0#	L22	I	DOCLK3#	P05	IO	GIRDY/ SBCK	AC12	O	MA02 / strap	**AA18**	**P**	**MEMVREF**	**AA12**	**P**	**VCC25**
AC05	O	CS1#	D08	O	DP0CLK / TVCLK	**B13**	**P**	**GND**	AB14	O	MA03 / strap	E14	I	PROCRDY	**AA14**	**P**	**VCC25**
AC06	O	CS2#	D09	O	DP0D00 / TVD0	**B16**	**P**	**GND**	AB16	O	MA04 / strap	AD01	I	PWROK	**AA16**	**P**	**VCC25**
AB06	O	CS3#	C09	O	DP0D01 / TVD1	**B19**	**P**	**GND**	AB17	O	MA05 / strap	AE01	I	RESET#	**AA17**	**P**	**VCC25**
AB07	O	CS4#	B09	O	DP0D02 / TVD2	**B22**	**P**	**GND**	AB15	O	MA06 / strap	B05	A	RSET	**AA19**	**P**	**VCC25**
AD05	O	CS5#	A09	O	DP0D03 / TVD3	**B25**	**P**	**GND**	AC18	O	MA07 / strap	L21	A	S2KCOMP	**AA20**	**P**	**VCC25**
B17	IO	D00#	E09	O	DP0D04 / TVD4	**C10**	**P**	**GND**	AE17	O	MA08 / strap	**F17**	**P**	**S2KVREF**	**J06**	**P**	**VCCAGP**
D20	IO	D01#	E08	O	DP0D05 / TVD5	**D13**	**P**	**GND**	AC17	O	MA09 / strap	**N21**	**P**	**S2KVREF**	**N06**	**P**	**VCCAGP**
B20	IO	D02#	B08	O	DP0D06 / TVD6	**D16**	**P**	**GND**	AB10	O	MA10 / strap	D02	I	SBA0# / DP1VS	**P06**	**P**	**VCCAGP**
C20	IO	D03#	A08	O	DP0D07 / TVD7	**D19**	**P**	**GND**	AC09	O	MA11 / strap	D03	I	SBA1# / DP1DE	**R06**	**P**	**VCCAGP**
A20	IO	D04#	C08	O	DP0D08 / TVD8	**D22**	**P**	**GND**	AF17	O	MA12 / strap	E03	I	SBA2# /DP1D00	**T06**	**P**	**VCCAGP**
C21	IO	D05#	C07	O	DP0D09 / TVD9	**E23**	**P**	**GND**	AB18	O	MA13 / strap	D01	I	SBA3# / DP1HS	**U06**	**P**	**VCCAGP**
E19	IO	D06#	B07	O	DP0D10 / TVD10	**E25**	**P**	**GND**	AB19	O	MA14 / strap	G03	I	SBA4# / DP1VS	**C04**	**P**	**VCCDAC**
B21	IO	D07#	A07	O	DP0D11 / TVD11	**F02**	**P**	**GND**	Y22	O	MCLK	F01	I	SBA5# / DP1D3	**G22**	**P**	**VCCHCK**
B18	IO	D08#	A11	IO	DP0DE / TVDE	**F04**	**P**	**GND**	AA23	I	MCLKFB	G01	I	SBA6# / DP1CK	**AA07**	**P**	**VCCM**
E18	IO	D09#	A10	OI	DP0DET / TVCKI	**F11**	**P**	**GND**	W23	IO	MD00	G02	I	SBA7# /DP1CK#	**AA15**	**P**	**VCCM**
A17	IO	D10#	B10	O	DP0HS / TVHS	**F13**	**P**	**GND**	W24	IO	MD01	E01	I	SBSF / DP1D01	**AA21**	**P**	**VCCM**
C18	IO	D11#	B11	O	DP0VS / TVVS	**F14**	**P**	**GND**	AA25	IO	MD02	E02	I	SBSS / DP1D02	**AA22**	**P**	**VCCMCK**
A18	IO	D12#	Y26	O	DQM0	**H23**	**P**	**GND**	AB26	IO	MD03	AD07	O	SCASA# / strap	**B04**	**P**	**VCCPLL1**
D18	IO	D13#	AD25	O	DQM1	**H25**	**P**	**GND**	W26	IO	MD04	F07	IO	SPCLK1	**A04**	**P**	**VCCPLL2**
C17	IO	D14#	AD22	O	DQM2	**J02**	**P**	**GND**	W25	IO	MD05	C06	IO	SPCLK2	**B01**	**P**	**VCCQQ**
E20	IO	D15#	AF19	O	DQM3	**L23**	**P**	**GND**	AA26	IO	MD06	D07	IO	SPDAT1	**C03**	**P**	**VCCRGB**
A21	IO	D16#	AE15	O	DQM4	**L25**	**P**	**GND**	AA24	IO	MD07	D06	IO	SPDAT2	**M21**	**P**	**VCCS2K**
D21	IO	D17#	AF12	O	DQM5	**M02**	**P**	**GND**	AB25	IO	MD08	AB11	O	SRASA# / strap	**Y06**	**P**	**VCCVL**
C22	IO	D18#	AB08	O	DQM6	**M04**	**P**	**GND**	AB24	IO	MD09	G05	O	ST0 / ENAVEE	**AA06**	**P**	**VCCVL**
A26	IO	D19#	AF04	O	DQM7	**P23**	**P**	**GND**	AF25	IO	MD10	F03	O	ST1 / ENAVDD	AB03	O	VDNCMD
C25	IO	D20#	Y24	O	DQS0#	**P25**	**P**	**GND**	AE24	IO	MD11	J05	O	ST2 / ENABLT	AB01	O	VDNSTB
C23	IO	D21#	AD26	O	DQS1#	**R02**	**P**	**GND**	AB23	IO	MD12	AD02	I	SUSST#	AB02	O	VDNSTB#
D24	IO	D22#	AF22	O	DQS2#	**T21**	**P**	**GND**	AC26	IO	MD13	AB09	O	SWEA# /strap	**AB05**	**A**	**VLCOMP**
B26	IO	D23#	AD19	O	DQS3#	**U21**	**P**	**GND**	AE26	IO	MD14	F12	I	TESTIN0	**Y05**	**P**	**VLVREF**
E21	IO	D24#	AF15	O	DQS4#	**U23**	**P**	**GND**	AF26	IO	MD15	E10	I	TESTIN1	**AD03**	**P**	**VSUS25**
A23	IO	D25#	AE12	O	DQS5#	**U25**	**P**	**GND**	AD23	IO	MD16	W04	IO	VAD0	A06	O	VSYNC
B23	IO	D26#	AC08	O	DQS6#	**V02**	**P**	**GND**	AE23	IO	MD17	W05	IO	VAD1	Y04	I	VUPCMD
A22	IO	D27#	AD04	O	DQS7#	**V04**	**P**	**GND**	AD21	IO	MD18	AA04	IO	VAD2	AA01	I	VUPSTB
D23	IO	D28#	T01	IO	GBE0 / DP3D03	**Y23**	**P**	**GND**	AF21	IO	MD19	Y01	IO	VAD3	AA02	I	VUPSTB#
A25	IO	D29#	P04	IO	GBE1 / SBDA	**Y25**	**P**	**GND**	AC23	IO	MD20	AC02	IO	VAD4	E06	I	XIN

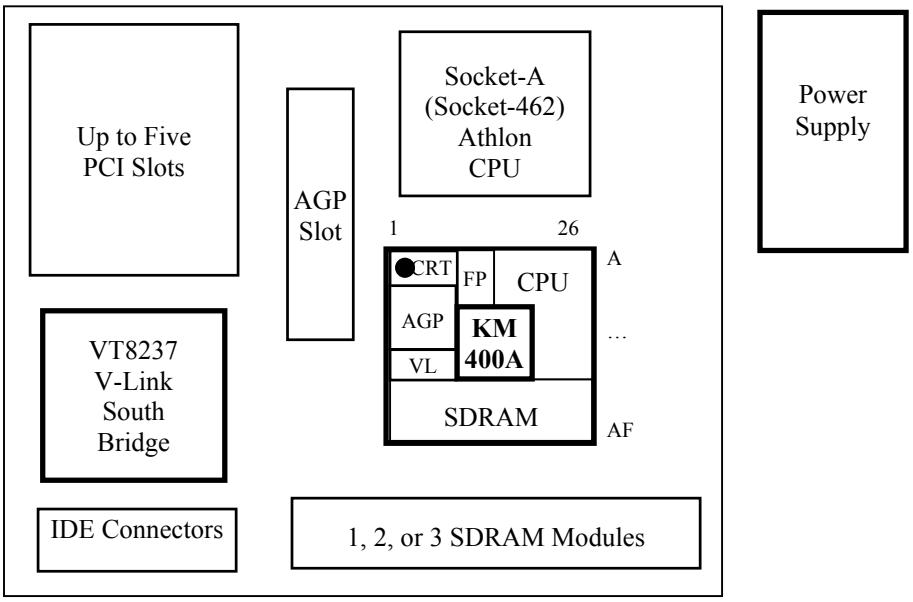
Center **VTT** Pins (12 pins): **J13-18, K18, L18, M18, N18, P18, R18** Center **VCCVL** Pin (2 pins)s **T9, U9** Center **VCCAGP** pins (6 pins): **K9, L9, M9, N9, P9, R9**
Center **GND** Pins (37 pins): **J9, L11-16, M11-16, N11-16, P11-16, R11-16, T11-16** Center **VCCDP** Pins (3 pins): **J10-12** Center **VCCM** Pins (12 pins): **T18, U18, V9-18**

PIN DESCRIPTIONS

Table 4. Pin Descriptions

CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
CFWDRST	D14	O	**CLK Forward Reset.** Reset the clock forward circuitry for the Athlon™ interface.
CONNECT	C14	O	**Connect.** Used for power management and CLK-forward initialization at reset.
PROCRDY	E14	I	**Processor Ready.** Used for power management and clock-forward initialization at reset.
AIN[14-2]#	(see pin list)	O	**Host CPU Address / Command Output.** Unidirectional system address / command interface to the processor from the system controller. It is used to transfer probes or data movement commands into the processor during PCI-to-DRAM cycles to snoop the CPU internal Cache. AIN[14:2]# is skew-aligned with the forward clock, AINCLK#
AINCLK#	B15	O	**Host CPU Address Output Clock.** Single-ended forwarded clock for the AIN[14:2]# bus that is driven by the system controller. Both rising and falling edges are used to transfer addresses or commands to the processor.
AOUT[14-2]#	(see pin list)	I	**Host CPU Address Input.** Unidirectional system address / command interface from the processor to the system controller. It is used to transfer processor commands or probes responses to the system controller. AOUT[14:2]# is skew-aligned with the forward clock, AOUTCLK#
AOUTCLK#	R25	I	**Host CPU Address Input Clock.** Single-ended forwarded clock for the AOUT[14:2]# bus that is driven by the processor. Both rising and falling edges are used to transfer commands or probe responses.
D[63-0]#	(see pin list)	IO	**Host CPU Data.** Bi-directional interface between the processor and the system controller for data movement. D[63:0]# bus is skew-aligned with either the DICLK[3:0]# or DOCLK[3:0]# forward clocks.
DICLK[3-0]#	L24, G23, A24, A19	O	**Host CPU Data Input Clock.** Single-ended forwarded clocks for the D[63:0]# bus, driven by the system controller to the processor. Each 16-bit data word is skew-aligned with one of these clocks. Both rising and falling edges are used to transfer data to the processor.
DOCLK[3-0]#	L22, F23, B24, C19	I	**Host CPU Data Output Clock.** Single-ended forwarded clocks for the D[63:0]# bus, driven by the processor to the system controller. Each 16-bit data word is skew-aligned with one of these clocks. Both rising and falling edges are used to transfer data to the system controller.
DINVAL#	E13	O	**Host CPU Data Read In Valid.** Driven by the system controller to control the flow of data into the processor. DINVAL# can be used to introduce an arbitrary number of cycles between octawords into the processor.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX and NLX) were also considered and can typically follow the same general component placement.



V-Link Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VAD7, **VAD6,** **VAD5**, **VAD4**, **VAD3**, **VAD2**, **VAD1**, **VAD0**	AC1 AB4 Y2 AC2 Y1 AA4 W5 W4	IO IO IO IO IO IO IO IO	**Address/Data Bus.** Also used to transmit strap information from the South Bridge (the straps are not on the VAD pins but are on the indicated pins of the South Bridge chip).
VBE#	Y3	IO	**Byte Enable.**
VUPCMD	Y4	I	**Command from Client-to-Host.**
VUPSTB	AA1	I	**Strobe from Client-to-Host.**
VUPSTB#	AA2	I	**Complement Strobe from Client-to-Host.**
VDNCMD	AB3	O	**Command from Host-to-Client.**
VDNSTB	AB1	O	**Strobe from Host-to-Client.**
VDNSTB#	AB2	O	**Complement Strobe from Host-to-Client.**

AGP 8x / 4x Bus Interface

Signal Name	Pin #	I/O	Signal Description
GD[31:0]	(see pin list)	IO	**Address / Data Bus.** Address is driven with GDS assertion for AGP-style transfers and with GFRM# assertion for PCI-style transfers.
GBE[3:0] (GBE[3:0#] for 4x mode)	K3 N1 P4 T1	IO	**Command / Byte Enable.** (Interpreted as C/BE# for AGP 2x/4x and C#/BE for 8x). For AGP cycles these pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# (2x/4x only as GPIPE# isn't used in 8x mode). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data. For PCI cycles, commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	U4	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GBE[3:0].
GDBIH / GPIPE# **GDBIL**	K5 J4	IO	**Dynamic Bus Inversion High / Low.** AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group. **Pipelined Request.** Not used by AGP 8x. Asserted by the master (external graphics controller) to indicate that a full-width request is to be enqueued by the target (North Bridge). The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus. **Note**: See RxAE[1] for GPIPE# / GDBIH pin function selection.
GDS0F (GDS0 for 4x), **GDS0S** (GDS0# for 4x)	T3 T2	IO	**Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). GDS0 provides timing for 2x data transfer mode; GDS0 and GDS0# provide timing for 4x mode. For 8x transfer mode, GDS0 is interpreted as GDS0F ("First" strobe) and GDS0# as GDS0S ("Second" strobe).
GDS1F (GDS1 for 4x), **GDS1S** (GDS1# for 4x)	K2 K1	IO	**Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). GDS1 provides timing for 2x data transfer mode; GDS1 and GDS1# provide timing for 4x transfer mode. For 8x transfer mode, GDS1 is interpreted as GDS1F ("First" strobe) and GDS1# as GDS1S ("Second" strobe).
GFRM (GFRM# for 4x)	N5	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. Interpreted as active high for 8x.
GIRDY (GIRDY# for 4x)	P5	IO	**Initiator Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP write cycles, the assertion of this pin indicates that the master is ready to provide *all* write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For AGP read cycles, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. For PCI cycles, asserted when the initiator is ready for data transfer.
GTRDY (GTRDY# for 4x)	R5	IO	**Target Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. For PCI cycles, asserted when the target is ready for data transfer.
GDSEL (GDSEL# for 4x mode)	N4	IO	**Device Select (PCI transactions only).** This signal is driven by the North Bridge when a PCI initiator is attempting to access main memory. It is an input when the chip is acting as PCI initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x.

Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see "Additional I2C Interfaces" and "Digital Display" pin description tables later in this document for more information).

AGP 8x / 4x Bus Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GSTOP (GSTOP# for 4x)	U5	IO	**Stop (PCI transactions only).** Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x.
AGP8XDT#	G6	I	**AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode
GRBF (GRBF# for 4x)	K4	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the North Bridge will not return low priority read data to the graphics controller.
GWBF (GWBF# for 4x)	L5	I	**Write Buffer Full.**
SBA[7:0]# (SBA[7:0] for 4x)	(see pin list)	I	**SideBand Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (North Bridge). These pins are ignored until enabled.
SBSF (SBS for 4x), **SBSS** (SBS# for 4x)	E1 E2	I	**Sideband Strobe.** Driven by the master to provide timing for SBA[7:0]. SBS is used for AGP 2x while SBS and SBS# are used together for AGP 4x. For 8x mode, the strobe mechanism works differently with SBS interpreted as SBSF ("First" strobe) and SBS# as SBSS ("Second" strobe).
ST[2:0]	J5, F3, G5	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the target (North Bridge logic) and inputs to the master (graphics controller).
GREQ (GREQ# for 4x)	F5	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT (GGNT# for 4x)	E4	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR (GSERR# for 4x)	R4	IO	**AGP System Error.**

Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see "Additional I2C Interfaces" and "Digital Display" pin description tables later in this document for more information).

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an internal pullup to maintain it in the de-asserted state in case it is not implemented on the master device. AGP 8x mode allows only SBA (GPIPE# isn't used in 8x mode).

Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

DDR Synchronous DRAM Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MD[63:0]	(see pinout tables)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Rx6D[1-0].
MA[14:0]	AB19, AB18, AF17, AC9, AB10, AC17, AE17, AC18, AB15, AB17, AB16, AB14, AC12, AB12, AC11	O	**Memory Address.** DRAM address lines. Output drive strength may be set by Device 0 Rx6C[7-6].
CS[5:0]#	AD5, AB7, AB6, AC6, AC5, AD6	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 Rx6D[3-2].
DQM[7:0]	AF4, AB8, AF12, AE15, AF19, AD22, AD25, Y26	O	**Data Mask.** Data mask of each byte lane. Output drive strength may be set by Device 0 Rx6D[5-4].
DQS[7:0]#	AD4, AC8, AE12, AF15, AD19, AF22, AD26, Y24	IO	**DDR Data Strobe.** Data strobe of each byte lane. Output drive strength may be set by Device 0 Rx6C[3-2].
SRASA#, **SRASB#** / CKE5, **SRASC#** / CKE4	AB11 AF24 AB20	O	**Row Address Command Indicator.** Output drive strength may be set by Device 0 Rx6C[7-4].
SCASA#, **SCASB#** / CKE3, **SCASC#** / CKE1	AD7 AC24 AD24	O	**Column Address Command Indicator.** Output drive strength may be set by Device 0 Rx6C[7-4].
SWEA# **SWEB#** / CKE2, **SWEC#** / CKE0	AB9 AB22 AC21	O	**Write Enable Command Indicator.** Output drive strength may be set by Device 0 Rx6C[7-4].
CKE5 / SRASB#, **CKE4** / SRASC#, **CKE3** / SCASB#, **CKE2** / SWEB#, **CKE1** / SCASC#, **CKE0** / SWEC#	AF24 AB20 AC24 AB22 AD24 AC21	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems. See Device 0 Rx78[0] and RxE0[4].

Serial Bus / I2C Interfaces				
Signal Name	**AGP Name**	**Pin #**	**I/O**	**Signal Description**
SBCK	GIRDY	P5	IO	**I2C Serial Bus Clock for Panel (Muxed on AGP Bus Pins).**
SBDA	GBE1	P4	IO	**I2C Serial Bus Data for Panel (Muxed on AGP Bus Pins).**
DDCCK	GREQ	F5	IO	**I2C Serial Bus Clock for CRT DDC (Muxed on AGP Bus Pins).**
DDCDA	GGNT	E4	IO	**I2C Serial Bus Data for CRT DDC (Muxed on AGP Bus Pins).**
SPCLK1	n/a	F7	IO	**I2C Serial Bus Clock for Display Port 1.** As an output, it is programmed via Rx3C5.31[5]. As an input, its status is read via Rx3C5.31[3]. In either case the serial port must be enabled by Rx3C5.31[0] = 1.
SPDAT1	n/a	D7	IO	**I2C Serial Bus Data for Display Port 1.** As an output, it is programmed via Rx3C5.31[4]. As an input, its status is read via Rx3C5.31[2]. In either case the serial port must be enabled by Rx3C5.31[0] = 1.
SPCLK2	n/a	C6	IO	**I2C Serial Bus Clock for Display Port 2 (or DDC if AGP Enabled).** As an output, it is programmed via Rx3C5.26[5]. As an input, its status is read via Rx3C5.26[3]. In either case the serial port must be enabled by Rx3C5.26[0] = 1.
SPDAT2	n/a	D6	IO	**I2C Serial Bus Data for Display Port 2 (or DDC if AGP Enabled).** As an output, it is programmed via Rx3C5.26[4]. As an input, its status is read via Rx3C5.26[2]. In either case the serial port must be enabled by Rx3C5.26[0] = 1.

"Display Ports 1-2" above refer to the 12-bit "DVI" interfaces typically connected to external TMDS transmitters for driving flat panel monitors. One option possible as a result of multiplexing display functions on the AGP port pins is that if AGP is not enabled, an add-in card can be designed to fit in the AGP slot to bring out panel display pins. In this case, the first two sets of serial ports defined above (SBxx and DDCxx) can be used.

Panel Power Control (Muxed with AGP)				
Signal Name	**AGP Name**	**Pin #**	**I/O**	**Signal Description**
ENAVDD	ST1	F3	IO	**Enable Panel VDD Power.**
ENAVEE	ST0	G5	IO	**Enable Panel VEE Power.**
ENABLT	ST2	J5	IO	**Enable Panel Back Light.**

CRT Display Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AR	A3	A	**Analog Red.** Analog red output to the CRT monitor.
AB	B3	A	**Analog Blue.** Analog blue output to the CRT monitor.
AG	A2	A	**Analog Green.** Analog green output to the CRT monitor.
HSYNC	B6	O	**Horizontal Sync.** Output to CRT.
VSYNC	A6	O	**Vertical Sync.** Output to CRT.
RSET	B5	A	**Reference Resistor.** Tie to GNDRGB through an external 90.9 Ω ± 1% Ω resistor to control the RAMDAC full-scale current value.

Dedicated Digital Display Interface Port 0 (Muxed with TV Out)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
DP0D11 / TVD11, **DP0D10** / TVD10 / strap, **DP0D9** / TVD9, **DP0D8** / TVD8, **DP0D7** / TVD7 / strap, **DP0D6** / TVD6 / strap, **DP0D5** / TVD5 / strap, **DP0D4** / TVD4 / strap, **DP0D3** / TVD3 / strap, **DP0D2** / TVD2 / strap, **DP0D1** / TVD1 / strap, **DP0D0** / TVD0 / strap	A7 B7 C7 C8 A8 B8 E8 E9 A9 B9 C9 D9	O	**Digital Display Port 0 Data.** Default output drive is 8 mA. 16 mA may be selected via SR3D[6]=1. TV Encoder outputs are muxed on the DP0D[11:0] pins (see the TV Encoder Interface pin list for details).
DP0HS / TVHS	B10	O	**Digital Display Port 0 Horizontal Sync.** Internally pulled down.
DP0VS / TVVS	B11	O	**Digital Display Port 0 Vertical Sync.** Internally pulled down.
DP0DE / TVDE	A11	O	**Digital Display Port 0 Data Enable.** Internally pulled down.
DP0DET / TVCLKI	A10	I	**Digital Display Port 0 Display Detect.** If VGA register 3C5.12[5]=0, 3C5.1A[5] will read 1 if a Flat Panel is connected.
DP0CLK / TVCLK	D8	O	**Digital Display Port 0 Clock.** Internally pulled down during reset. 8mA is the default. 16mA may also be selected.

The above pins are designed to connect to an external TMDS transmitter for driving a DVI connector to a flat panel monitor.
The terminology "3C5.nn" above refers to the VGA "Sequencer" registers at I/O port 3C5 index "nn"

Dedicated TV Encoder Interface (Muxed with Digital Display Port 0)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
TVD11 / DP0D11, **TVD10** / DP0D10 / strap, **TVD9** / DP0D9, **TVD8** / DP0D8, **TVD7** / DP0D7 / strap, **TVD6** / DP0D6 / strap, **TVD5** / DP0D5 / strap, **TVD4** / DP0D4 / strap, **TVD3** / DP0D3 / strap, **TVD2** / DP0D2 / strap, **TVD1** / DP0D1 / strap, **TVD0** / DP0D0 / strap	A7 B7 C7 C8 A8 B8 E8 E9 A9 B9 C9 D9	O	**TV Encoder Data.**
TVHS / DP0HS	B10	O	**TV Encoder Horizontal Sync.** Internally pulled down during reset
TVVS / DP0VS	B11	O	**TV Encoder Vertical Sync.** Internally pulled down during reset
TVDE / DP0DE	A11	O	**TV Encoder Display Enable.** Internally pulled down during reset
TVCLKI / DP0DET	A10	I	**TV Encoder Clock In.** Input clock from TV encoder. Internally pulled down.
TVCLK / DP0CLK	D8	O	**TV Encoder Clock Out.** Output clock to TV encoder. Internally pulled down.

The above pins are designed to connect to an external TV Encoder chip such as the VIA VT1621 or VT1622 for driving a TV set.

Digital Display Interface Port 1 (Muxed with AGP)				
Signal Name	**AGP Name**	**Pin #**	**I/O**	**Signal Description**
DP1D11, **DP1D10**, **DP1D9**, **DP1D8**, **DP1D7**, **DP1D6**, **DP1D5**, **DP1D4**, **DP1D3**, **DP1D2**, **DP1D1**, **DP1D0**	GBE3 GD26 GD24 GD30 GD28 GD29 SBA4# GD27 SBA5# SBSS SBSF SBA2#	K3 J3 J1 H2 H1 H3 G3 H4 F1 E2 E1 E3	O	**Digital Display Port 1 Data.**
DP1HS	SBA3#	D1	O	**Digital Display Port 1 Horizontal Sync.**
DP1VS	SBA0#	D2	O	**Digital Display Port 1 Vertical Sync.**
DP1DE	SBA1#	D3	O	**Digital Display Port 1 Data Enable.**
DP1DET	GD31	G4	I	**Digital Display Port 1 Display Detect.** If VGA register 3C5.3E[0] = 1, 3C5.1A[4] will read 1 if a panel is connected. Must be tied to GND if not used.
DP1CLK	SBA6#	G1	O	**Digital Display Port 1 Clock.**
DP1CLK#	SBA7#	G2	O	**Digital Display Port 1 Clock Complement.**

The above pins are designed to connect to an external TMDS transmitter for driving a DVI connector to a flat panel monitor.

Digital Display Port 2 Interface (Muxed with AGP)				
Signal Name	**AGP Name**	**Pin #**	**I/O**	**Signal Description**
DP2D11, **DP2D10,** **DP2D09,** **DP2D08,** **DP2D07,** **DP2D06,** **DP2D05,** **DP2D04,** **DP2D03,** **DP2D02,** **DP2D01,** **DP2D00**	GD11 GD13 GD14 GD15 GBE2 GD16 GD17 GD18 GD23 GD20 GD22 GDS1F	P2 P1 P3 N3 N1 N2 M1 M3 L3 L1 L2 K2	O	**Display Port 2 Data.** 3C5.12[4] must be set to 0. Used for driving an external flat panel monitor via external TMDS transmitters.
DP2HS	GFRAME	N5	O	**Display Port 2 Horizontal Sync.**
DP2VS	GDEVSEL	N4	O	**Display Port 2 Vertical Sync.**
DP2DE	GD19	M5	O	**Display Port 2 Data Enable.**
DP2DET	GDS1S	K1	I	**Display Port 2 Detect.** If Rx??[?]=0, Rx??[?] will read 1 if a Flat Panel Monitor is properly connected. Must be tied to GND if not used.
DP2CLK	GD21	L4	O	**Display Port 2 Clock.**
DP2CLK#	GWBF	L5	O	**Display Port 2 Clock Complement.**

The above pins are designed to connect to an external TMDS transmitter for driving a DVI connector to a flat panel monitor.

Digital Display Port 3 Interface (Muxed with AGP)				
Signal Name	**AGP Name**	**Pin #**	**I/O**	**Signal Description**
DP3D11, **DP3D10,** **DP3D09,** **DP3D08,** **DP3D07,** **DP3D06,** **DP3D05,** **DP3D04,** **DP3D03,** **DP3D02,** **DP3D01,** **DP3D00**	GD1 GD0 GD3 GD4 GD5 GD6 GD7 GDS0F GBE0 GDS0S GD10 GD12	W1 W2 W3 V1 U2 U1 U3 T3 T1 T2 R3 R1	O	**Display Port 3 Data.** 3C5.12[4] must be set to 0. Used for driving an external flat panel monitor via external TMDS transmitters.
DP3HS	GD9	T5	O	**Display Port 3 Horizontal Sync.**
DP3VS	GPAR	U4	O	**Display Port 3 Vertical Sync.**
DP3DE	GSERR	R4	O	**Display Port 3 Data Enable.**
DP3DET	GD8	T4	I	**Display Port 3 Detect.** If Rx??[?]=0, Rx??[?] will read 1 if a Flat Panel Monitor is properly connected. Must be tied to GND if not used.
DP3CLK	GD2	V3	O	**Display Port 3 Clock.**
DP3CLK#	GSTOP	U5	O	**Display Port 3 Clock Complement.**

The above pins are designed to connect to an external TMDS transmitter for driving a DVI connector to a flat panel monitor.

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HCLK	G21	I	**Host Clock.** This pin receives the host CPU clock (100 / 133 MHz). This clock is used by all KM400A logic that is in the host CPU domain.
HCLK#	F22	I	**Host Clock Complement.** HCLK inverted. Used for Quad Data Transfer on host CPU bus.
MCLK	Y22	O	**Memory (SDRAM) Clock.** Output from internal clock generator to the external clock buffer.
MCLKFB	AA23	I	**Memory (SDRAM) Clock Feedback.** Input from the external clock buffer.
DCLKI	D5	I	**Dot Clock (Pixel Clock) In.** Used for external EMI reduction circuit if used. Loop back from DCLKO if external EMI reduction circuit not implemented.
DCLKO	C5	O	**Dot Clock (Pixel Clock) Out.** Used for external EMI reduction circuit if used. Loop back to DCLKI if external EMI reduction circuit not implemented.
GCLK	V5	I	**Graphics Clock.**
XIN	E6	I	**Reference Frequency Input.** An external 14.31818 MHz clock source is normally connected to this pin. All internal graphics controller clocks are synthesized on chip using this frequency as a reference.
RESET#	AE1	I	**Reset.** Input from the South Bridge chip. When asserted, this signal resets the KM400A and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options
PWROK	AD1	I	**Power OK.** Connect to South Bridge and Power Good circuitry.
SUSST#	AD2	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.
GPIO0	D10	O	**General Purpose I/O 0.** For programming, see VGA register 3C5.25
GPOUT	E7	O	**General Purpose Output.** For programming, see VGA register 3C5.25
INTA#	F6	O	**Interrupt.** PCI interrupt output (handled by the interrupt controller in the South Bridge)
BISTIN	A5	I	**BIST In.** This pin is used for testing and must be left unconnected or tied to GND on all board designs.
TESTIN0	F12	I	**Test In 0.** This pin is used for testing and must be left unconnected or tied high on all board designs.
TESTIN1	E10	I	**Test In 1.** This pin is used for testing and must be left unconnected or tied high on all board designs.

Reference Voltages			
Signal Name	**Pin #**	**I/O**	**Signal Description**
S2KVREF	F17, N21	P	**S2K Bus Voltage Reference.** 0.5 VTT derived using resistive voltage divider. See KM400A Design Guide.
AGPVREF	H6, M6	P	**AGP Voltage Reference.** 0.4 VCCQQ (1.32V) when VCCQQ is 3.3V and 0.5 VCCQQ (0.75V) when VCCQQ is 1.5V. See KM400A Design Guide.
MEMVREF	AA10, AA18	P	**Memory Voltage Reference.** 0.5 VCCM derived using resistive voltage divider. See KM400A Design Guide.
VLVREF	Y5	P	**V-Link Voltage Reference.** 0.625V derived using a resistive voltage divider. See KM400A Design Guide.

Compensation			
Signal Name	**Pin #**	**I/O**	**Signal Description**
S2KCOMP	L21	I	**S2K Bus Compensation.** Connect to 49.9 Ω 1% resistor to ground.
AGPCOMP	C1	AI	**AGP Compensation.**
VLCOMP	AB5	I	**Vlink P-Channel Compensation.** Connect 360 Ω 1% resistor to ground.

Analog & Quiet Power and Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCCS2K	M21	P	**Power for S2K Bus Circuitry.** (2.5V ±5%)
VCCQQ	B1	P	**AGP Quiet Power.** Connect to main AGP power (VCCAGP = 1.5 / 3.3V ±5%) through a ferrite bead.
VCCHCK	G22	P	**Power for Host CPU Clock DLL** (2.5V ±5%)
VCCMCK	AA22	P	**Power for Memory Clock DLL** (2.5V ±5%)
VCCRGB	C3	P	**Power for CRT RGB Outputs** (2.5V ±5%).
VCCDAC	C4	P	**Power for DAC Digital Logic** (2.5V ±5%)
VCCPLL1	B4	P	**Power for Graphics Controller PLL1** (2.5V ±5%).
VCCPLL2	A4	P	**Power for Graphics Controller PLL2** (2.5V ±5%).
GNDS2K	K21	P	**Ground for S2K Bus Circuitry.** Connect to main ground plane.
GNDQQ	C2	P	**Ground for AGP Quiet Power.** Connect to main ground plane.
GNDHCK	F21	P	**Ground for Host CPU Clock Circuitry.** Connect to main ground plane through a ferrite bead.
GNDMCK	Y21	P	**Ground for Memory Clock Circuitry.** Connect to main ground plane through a ferrite bead.
GNDRGB	A1	P	**Connection Point for RGB Load Resistors.**
GNDDAC	B2	P	**Ground for DAC Analog Circuitry.**
GNDPLL1	E5	P	**Ground for Graphics Controller PLL1.**
GNDPLL2	D4	P	**Ground for Graphics Controller PLL2.**

Digital Power and Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCC25	(see pin list)	P	**Power** for **Internal Logic** (2.5V ±5%).
VSUS25	AD3	P	**Suspend Power** (2.5V ±5%).
VTT	J13-J18, K18, L18, M18, N18, P18, R18	P	**Power** for **CPU I/O Interface Logic.** Voltage is CPU dependent. See also VID (Voltage ID) pin.
VCCAGP	J6, K9, L9, M9, N6, N9, P6, P9, R6, R9, T6, U6	P	**Power** for **AGP Bus I/O Interface Logic.** 1.5V±5%
VCCM	T18, U18, V9-V18, AA7, AA15, AA21	P	**Power** for **Memory I/O Interface Logic** (2.5 / 3.3V ±5%).
VCCVL	T9, U9, Y6, AA6	P	**Power** for **V-Link I/O Interface Logic** (2.5V ±5%).
VCCDP	J10-J12	P	**Power for Digital Display Interface** (3.3V ±5%).
GND	(see pin table)	P	**Ground.** Connect to main ground plane.

Strap Pins (External pullup / pulldown straps are required to select "H" / "L")				
Signal	**Actual Strap Pin**	**Function**	**Description**	**Status Bit**
DP0D[10,7]	DP0D[10,7]	-reserved-	Must be pulled low	-
DP0D[6]	DP0D[6]	DP0 Port Enable	L: Disable H: Enable	3C5.12[6]
DP0D[5]	DP0D[5]	DP0 Port Configuration	L: Display H: TV out	3C5.12[5]
DP0D[4]	DP0D[4]	FP Port Configuration	L: 2 x 12-bit FP interface H: 24-bit FP interface	3C5.12[4]
DP0D[3:0]	DP0D[3:0]	OEM Panel Type	Reserved for customer configuration	3C5.12[3:0]
VAD7	**VT8235-CD:** SDCS3# **VT8235-CE:** SDCS3# **VT8237:** PDCS3#	-reserved-	-	-
VAD5	**VT8235-CD:** SDA1 **VT8235-CE:** SDA1 **VT8237:** PDA1	Auto-Configure	L: Disable (used on-chip defaults) H: Enable (get from ROM) VAD5 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	Rx54[5]
VAD[6,4]	**VT8235-CD:** SDA[2, 0] **VT8235-CE:** SDA[2, 0] **VT8237:** PDA[2, 0]	FSB Frequency Select	LL: 100Mhz LH: 133MHz HL: 166MHz VAD6 and VAD4 are sampled during system initialization; The actual strapping pins are located on the South Bridge chip.	Rx54[7:6]
VAD[3:0]	**VT8235-CD:** SA[19:16] **VT8235-CE:** Strap_VAD[3:0] **VT8237:** GPIO[D, B, A, C]	CPU Clock Divider	LLLL: 11 LLLH: 11.5 LLHL: 12 LLHH: 12 LHLL: 5 LHLH: 5.5 LHHL: 6 LHHH: 6.5 HLLL: 7 HLLH: 7.5 HLHL: 8 HLHH: 8.5 HHLL: 9 HHLH: 9.5 HHHL: 10 HHHH: 10.5 VAD[3:0] are sampled during system initialization; The actual strapping pins are located on the South Bridge chip.	RxD7[6:3]

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the KM400A North Bridge. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO) and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

The graphics registers are described in a separate document.

Table 5. Registers

I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

Device 0 Registers - Host Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3205**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	**0000 0008**	**RW**
14-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	**W1**
2F-2E	Subsystem ID	0000	**W1**
30-33	-reserved-	00	—
37-34	Capability Pointer	**0000 00A0**	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	V-Link Control	Default	Acc
40	V-Link Revision ID	00	RW
41	V-Link NB Capability	**19**	RW
42	V-Link NB Downlink Command	**88**	RW
44-43	V-Link NB Uplink Status	**8280**	**RO**
45	V-Link NB Bus Timer	**44**	RW
46	V-Link Misc NB Control	00	RW
47	V-Link Control	00	RW
48	V-Link NB/SB Configuration	00	RW
49	V-Link SB Capability	**19**	RW
4A	V-Link SB Downlink Status	**88**	**RO**
4C-4B	V-Link SB Uplink Command	**8280**	RW
4D	V-Link SB Bus Timer	**44**	RW
4E	CCA Master High Priority	00	RW
4F	V-Link SB Miscellaneous Control	00	RW

Offset	CPU Interface Control	Default	Acc
50	S2K Duty Cycle Adjust 1	**08**	RW
51	S2K Duty Cycle Adjust 2	00	RW
52	S2K Duty Cycle Adjust 3	00	RW
53	S2K Duty Cycle Adjust 4	**80**	RW
54	CPU FSB Frequency	00	RW

Offset	DRAM Control	Default	Acc
55	DRAM Control	**00**	RW
56-57	-reserved-	00	—
59-58	MA Map Type	**2222**	RW
5F-5A	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[31:24])	**01**	RW
5B	Bank 1 Ending (HA[31:24])	**01**	RW
5C	Bank 2 Ending (HA[31:24])	**01**	RW
5D	Bank 3 Ending (HA[31:24])	**01**	RW
5E	Bank 4 Ending (HA[31:24])	**01**	RW
5F	Bank 5 Ending (HA[31:24])	**01**	RW
60	-reserved-	00	—
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for All Banks	**E4**	RW
65	DRAM Arbitration Timer	00	RW
66	DRAM Arbitration Control	00	RW
67	DDR Strobe Input Delay	00	RW
68	DDR Strobe Output Delay	00	RW
69	DRAM Clock Select	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	00	RW
6C	DRAM Early Clock Select	00	RW
6D	DRAM MD Output Delay	00	RW
6E-6F	-reserved-	00	—

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control	**48**	RW
72	-reserved-	00	—
73	PCI Master Control	00	RW
74	-reserved-	00	—
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77	Chip Test (do not program)	00	RW
78-7F	-reserved-	00	—

Device-Specific Registers (continued)

Offset	AGP 2.0 Control (RxFD[1]=1)	Default	Acc
83-80	AGP 2.0 GART/TLB Control	0000 0000	RW
84	AGP 2.0 Graphics Aperture Size	00	RW
85-87	Reserved (Do Not Program)	00	RW
8B-88	AGP 2.0 GART Table Base	0000 0000	RW
8C-9F	-reserved-	00	—
A3-A0	AGP 2.0 Capabilities	**0020 C002**	**RO**
A7-A4	AGP 2.0 Status	**1F00 0201**	**RO**
AB-A8	AGP 2.0 Command	0000 0000	RW

Registers A0-AB in the AGP 2.0 register group in the table above are actually offsets from CAPPTR (Rx34) which (with Rx34 = A0h for AGP 2.0) result in the offsets listed above.

Offset	AGP 3.0 Control (RxFD[1]=0)	Default	Acc
83-80	AGP 3.0 Capabilities	**0030 C002**	**RO**
87-84	AGP 3.0 Status	**1F00 0A03**	**RO**
8B-88	AGP 3.0 Command	**1F00 0000**	RW
8F-8C	-reserved-	0000 0000	—
93-90	AGP 3.0 GART / TLB Control	0000 0000	RW
97-94	AGP 3.0 Graphics Aperture Size	**0001 0F00**	RW
9B-98	AGP 3.0 GART Table Base	0000 0000	RW
9C-AB	-reserved-	00	—

Registers 80-AB in the AGP 3.0 register group in the table above are actually offsets from CAPPTR (Rx34) which (with Rx34 = 80h for AGP 3.0) result in the offsets listed above.

Offset	AGP 2.0 / 3.0 Control	Default	Acc
AC	AGP Control	00	RW
AD	AGP Latency Timer	**02**	RW
AE	AGP Miscellaneous Control	00	RW
AF	AGP 3.0 Control	00	RW
B0	AGP Pad Control / Status	**8x**	RW
B1	AGP Drive Strength	**63**	RW
B2	AGP Pad Drive / Delay Control	**08**	RW
B3	AGP Strobe Output Drive Control	00	RW

Offset	V-Link Control	Default	Acc
B4	V-Link NB Compensation Control	00	RW
B5	V-Link NB Strobe Drive Control	00	RW
B6	V-Link NB Data Drive Control	00	RW
B7	-reserved-	00	—
B8	V-Link SB Compensation Control	00	RW
B9	V-Link SB Strobe Drive Control	00	RW
BA	V-Link SB Data Drive Control	00	RW
BB	-reserved-	00	—

Offset	Power Control	Default	Acc
BC	Power Management Mode	00	RW
BD	DRAM Power Management Control	00	RW
BE	Dynamic Clock Stop Control	00	RW
BF	MA / SCMD Pad Toggle Reduction	00	RW

Offset	Extended Power Management	Default	Acc
C0	Power Management Capability ID	**01**	**RO**
C1	Power Management New Pointer	00	**RO**
C2	Power Management Capabilities I	**02**	**RO**
C3	Power Management Capabilities II	00	**RO**
C4	Power Management Control / Status	00	RW
C5	Power Management Status	00	RW
C6	PCI-to-PCI Bridge Support Extension	00	RW
C7	Power Management Data	00	RW
C8-CF	-reserved-	00	—

Offset	Host CPU Control	Default	Acc
D0-D1	-reserved-	00	—
D2	S2K Timing Control	**78**	RW
D3	BIU Arbitration Control	00	RW
D4	BIU Control 1	00	RW
D5	BIU Control 2	00	RW
D6	BIU Control 3	00	RW
D7	CPU Strapping	**strapping**	**RO**
D8	S2K Compensation Strapping	00	RW
D9	S2K Compensation Result 1	00	**RO**
DA	S2K Compensation Result 2	00	RW
DB	S2K Compensation Result 3	00	**RO**
DC	S2K Compensation Result 4	**07**	RW
DD	S2K Compensation Result 5	00	RW
DE	BIU Control 4	00	RW
DF	BIU Control 5	00	RW

Offset	UMA Control	Default	Acc
E0	CPU Direct Access FB Base	00	RW
E1	CPU Direct Access FB Size	00	RW
E2	VGA Arbitration Timer	00	RW
E3	Graphics Arbitration Timer	00	RW
Offset	**DRAM Above 4G Control**	**Default**	**Acc**
E4	Low Top Address Low	00	RW
E5	Low Top Address High	**FF**	RW
E6	SMM / APIC Decoding	**01**	RW
E7	-reserved-	00	—
Offset	**DRAM Drive**	**Default**	**Acc**
E8	DRAM DQ Drive	00	RW
E9	DRAM CS# Drive	00	RW
EA	DRAM MAA Drive	00	RW
EB	-reserved-	00	—
EC	DRAM S-Port Control	00	RW
ED	DRAM DQS Drive Control	00	RW
EE	DRAM DQS/MD Duty Cycle Control	00	RW
EF	-reserved-	00	—

Offset	Test, BIOS Scratch, Miscellaneous	Default	Acc
F0-F2	Reserved (Do Not Program)	00	RW
F3-F4	BIOS Scratch Registers	00	RW
F5-FC	Reserved (Do Not Program)	00	RW
FD	AGP 2.0 / 3.0 Select	00	RW
FE-FF	Reserved (Do Not Program)	00	RW

Device 1 – PCI-to-PCI Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**B168**	RO
5-4	Command	**0007**	**RW**
7-6	Status	**0230**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	**04**	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	**01**	RO
F	Built In Self Test (BIST)	00	RO
10-17	-reserved-	00	—
18	Primary Bus Number	00	**RW**
19	Secondary Bus Number	00	**RW**
1A	Subordinate Bus Number	00	**RW**
1B	Secondary Latency Timer	00	RO
1C	I/O Base	**F0**	**RW**
1D	I/O Limit	00	**RW**
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	**FFF0**	**RW**
23-22	Memory Limit (Inclusive)	0000	**RW**
25-24	Prefetchable Memory Base	**FFF0**	**RW**
27-26	Prefetchable Memory Limit	0000	**RW**
28-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	**W1**
2F-2E	Subsystem ID	0000	**W1**
30-33	-reserved-	00	—
34	Capability Pointer	**80**	RO
35-3D	-reserved-	00	—
3F-3E	PCI-to-PCI Bridge Control	00	**RW**

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	00	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	**22**	RW
44	Back-Door Register Control	00	RW
45	Fast Write Control	**72**	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48	AGP Parity Error Control	00	RW
49-7F	-reserved-	00	—
80	Capability ID	**01**	**RO**
81	Next Pointer	00	**RO**
82	Power Management Capabilities 1	**02**	**RO**
83	Power Management Capabilities 2	00	**RO**
84	Power Management Control / Status	00	RW
85	Power Management Status	00	**RO**
86	PCI-PCI Bridge Support Extensions	00	**RO**
87	Power Management Data	00	**RO**
88-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined in the KM400A: Port 22.

Port 22 – PCI / AGP Arbiter Disable .....RW

7-1 Reserved ..... always reads 0

0 PCI / AGP Arbiter Disable

0 Respond to all REQ# signals.....default

1 Do not respond to any REQ# signals

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 78.

Configuration Space I/O

All registers in the KM400A (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

31 Configuration Space Enable

0 Disabled..... default

1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved .....always reads 0

23-16 PCI Bus Number

Used to choose a specific PCI bus in the system

15-11 Device Number

Used to choose a specific device in the system (devices 0 and 1 are defined for the KM400A)

10-8 Function Number

Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the KM400A).

7-2 Register Number (also called the "Offset")

Used to select a specific DWORD in the KM400A configuration space

1-0 Fixed .....always reads 0

Port CFF-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

Device 0 Header Registers - Host Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID (1106h) ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID (3205h) ..... RO

15-0 ID Code (reads 3205h to identify the KM400A)

Device 0 Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable ..... RO
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... RW
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop ..... RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 PCI Bus Master ..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master ..... default

1 Memory Space ..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space ..... default

0 I/O Space ..... RO
- 0 Does not respond to I/O space ..... default
- 1 Responds to I/O space

Device 0 Offset 7-6 – Status (0210h) ..... RWC

15 Detected Parity Error
- 0 No parity error detected ..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). ..... write one to clear

14 Signaled System Error (SERR# Asserted) ..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master ..... write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target ..... write one to clear

11 Signaled Target Abort ..... always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and KM400A was initiator of the operation in which the error occurred. ..... write one to clear

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features ..... always reads 0

5 66MHz Capable ..... always reads 0

4 Supports New Capability list ..... always reads 1

3-0 Reserved ..... always reads 0

Device 0 Offset 8 - Revision ID (0nh) ..... RO

0-7 Chip Revision Code ..... default to 0nh (n=rev code)

Device 0 Offset 9 - Programming Interface (00h) ..... RO

7-0 Interface Identifier ..... always reads 00

Device 0 Offset A - Sub Class Code (00h) ..... RO

7-0 Sub Class Code ..... reads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code (06h) ..... RO

7-0 Base Class Code .. reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer (00h) ..... RW

Specifies the latency timer value in PCI bus clocks.

7-3 Guaranteed Time Slice for CPU ..... default=0

2-0 Reserved (fixed granularity of 8 clks) .. always read 0

Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Offset 75 bits 5-4 (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)

Device 0 Offset E - Header Type (00h).....RO

7-0 Header Type Code ..... reads 00: single function

Device 0 Offset F - Built In Self Test (BIST) (00h).....RO

7 BIST Supported .....reads 0: no supported functions

6-0 Reserved ..... always reads 0

Device 0 Offset 13-10 - Graphics Aperture Base (00000008h) .....RW

31-28 Upper Programmable Base Address Bits ..... def=0

27-20 Lower Programmable Base Address Bits ..... def=0

These bits behave as if hardwired to 0 if the corresponding Graphics Aperture Size register bit (Device 0 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(This Register)
7	6	5	4	3	2	1	0	(Gr Aper Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-0 Reserved ..... always reads 00008

Note: The locations in the address range defined by this register are prefetchable.

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h)R/W1

15-0 Subsystem Vendor ID ..... default = 0

This register may be written once and is then read only.

Device 0 Offset 2F-2E – Subsystem ID (0000h)..... R/W1

15-0 Subsystem ID ..... default = 0

This register may be written once and is then read only.

Device 0 Offset 37-34 - Capability Pointer (000000A0h) RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Pointer ..... always reads A0h

Device 0 Configuration Registers - Host Bridge

These registers are normally programmed once at system initialization time.

V-Link Control

Device 0 Offset 40 – V-Link Specification ID (00h).....RO

7-0 Specification Revision..... always reads 00

Device 0 Offset 41 – NB V-Link Capability (19h) .....RO

7-6 Reserved ..... always reads 0

5 16-bit Bus Width Supported .....RO
- 0 Not Supported .....default
- 1 Supported

4 8-Bit Bus Width Supported.....RO
- 0 Not Supported
- 1 Supported .....**default**

3 4x Rate Supported .....RO
- 0 Not Supported
- 1 Supported .....**default**

2 2x Rate Supported .....RO
- 0 Not Supported .....default
- 1 Supported

1 Reserved ..... always reads 0

0 8x Rate Supported .....RO
- 0 Not Supported
- 1 Supported .....**default**

Device 0 Offset 42 – NB Downlink Command (88h) .....RW

7-4 DnCmd Max Request Depth (0=1 DnCmd).. def = 8

3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Device 0 Offset 44-43 – NB Uplink Status (8280h).....RO

15-12 UpCmd P2C Write Buffer Size (max lines).. def = 8

11-8 UpCmd P2P Write Buffer Size (max lines) .. def = 2

7-4 UpCmd Max Request Depth (0=1 UpCmd).. def = 8

3-0 Reserved ..... always reads 0

Device 0 Offset 45 –NB V-Link Bus Timer (44h)..... RW

7-4 Timer for Normal Priority Requests from SB
- 0000 Immediate
- 0001 1*4 VCLKs
- 0010 2*4 VCLKs
- 0011 3*4 VCLKs
- 0100 4*4 VCLKs..... default
- 0101 5*4 VCLKs
- 0110 6*4 VCLKs
- 0111 7*4 VCLKs
- 1000 8*4 VCLKs
- 1001 16*4 VCLKs
- 1010 32*4 VCLKs
- 1011 64*4 VCLKs
- 11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from SB
- 0000 Immediate
- 0001 1*2 VCLKs
- 0010 2*2 VCLKs
- 0011 3*2 VCLKs
- 0100 4*2 VCLKs..... default
- 0101 5*2 VCLKs
- 0110 6*2 VCLKs
- 0111 7*2 VCLKs
- 1000 8*2 VCLKs
- 1001 16*2 VCLKs
- 1010 32*2 VCLKs
- 1011 64*2 VCLKs
- 11xx Own the bus for as long as there is a request

Device 0 Offset 46 – NB V-Link Misc Control (00h).....RW

- **7 Downstream High Priority**
  - 0 Disable High Priority Down Commands .....def
  - 1 Enable High Priority Down Commands
- **6 Downlink (C2P) Priority**
  - 0 Treat Downlink Cycles as Normal Priority..def
  - 1 Treat Downlink Cycles as High Priority
- **5-4 Combine Multiple STPGNT Cycles into V-Link Command**
  - 00 Compatible, 1 command per V-Link cmd....def
  - 01 2 commands per V-Link command
  - 10 3 commands per V-Link command
  - 11 4 commands per V-Link command
- **3-2 V-Link Master Access Ordering Rules**
  - 00 High priority read, pass normal read (not pass write) .....default
  - 01 Read (high/normal) pass write (HR>LR>W)
  - 1x Read / write in order
- **1-0 Reserved** ..... always reads 0

Device 0 Offset 47 – V-Link Control (00h).....RW

- **7-6 Reserved** ..... always reads 0
- **5 C2P Read Return Timing**
  - 0 Right after read ack command .....default
  - 1 Wait until P2C write data flushed
- **4-3 Reserved** ..... always reads 0
- **2 Auto-Disconnect**
  - 0 Disable .....default
  - 1 Enable
- **1 V-Link Disconnect Cycle for HALT cycle**
  - 0 Disable .....default
  - 1 Enable
- **0 V-Link Disconnect Cycle for STPGNT Cycle**
  - 0 Disable .....default
  - 1 Enable

Device 0 Offset 48 – NB/SB V-Link Configuration (00h)RW

- **7 Reserved** .....always reads 0
- **6 Rest Bus Width**
  - 0 Disable..... default
  - 1 Enable
- **5 16-bit Bus Width**
  - 0 Disable..... default
  - 1 Enable
- **4 8-Bit Bus Width**
  - 0 Disable..... default
  - 1 Enable
- **3 4x Rate**
  - 0 Disable..... default
  - 1 Enable
- **2 2x Rate**
  - 0 Disable..... default
  - 1 Enable
- **1 Reserved** .....always reads 0
- **0 8x Rate**
  - 0 Disable..... default
  - 1 Enable

Device 0 Offset 49 – SB V-Link Capability (19h).....RO

7-6 Reserved ..... always reads 0
5 16-bit Bus Width Supported .....RO
0 Not Supported .....default
1 Supported
4 8-Bit Bus Width Supported.....RO
0 Not Supported
1 Supported .....**default**
3 4x Rate Supported .....RO
0 Not Supported
1 Supported .....**default**
2 2x Rate Supported .....RO
0 Not Supported .....default
1 Supported
1 Reserved ..... always reads 0
0 8x Rate Supported .....RO
0 Not Supported
1 Supported .....**default**

Device 0 Offset 4A – SB Downlink Status (88h) .....RO

7-4 DnCmd Max Request Depth (0=1 DnCmd).. def = 8
3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Device 0 Offset 4C-4B – SB Uplink Command (8280h).RW

15-12 UpCmd P2C Write Buffer Size (max lines).. def = 8
11-8 UpCmd P2P Write Buffer Size (max lines) .. def = 2
7-4 UpCmd Max Request Depth (0=1 UpCmd).. def = 8
3-0 Reserved ..... always reads 0

Device 0 Offset 4D – SB V-Link Bus Timer (44h).....RW

7-4 Timer for Normal Priority Requests from NB
0000 Immediate
0001 1*4 VCLKs
0010 2*4 VCLKs
0011 3*4 VCLKs
0100 4*4 VCLKs .....default
0101 5*4 VCLKs
0110 6*4 VCLKs
0111 7*4 VCLKs
1000 8*4 VCLKs
1001 16*4 VCLKs
1010 32*4 VCLKs
1011 64*4 VCLKs
11xx Own the bus for as long as there is a request
3-0 Timer for High Priority Requests from NB
0000 Immediate
0001 1*2 VCLKs
0010 2*2 VCLKs
0011 3*2 VCLKs
0100 4*2 VCLKs .....default
0101 5*2 VCLKs
0110 6*2 VCLKs
0111 7*2 VCLKs
1000 8*2 VCLKs
1001 16*2 VCLKs
1010 32*2 VCLKs
1011 64*2 VCLKs
11xx Own the bus for as long as there is a request

Device 0 Offset 4E – CCA Master Priority (00h)..... RW

7 1394 High Priority
0 Low priority..... default
1 High priority
6 NIC High Priority
0 Low priority..... default
1 High priority
5 Reserved .....always reads 0
4 USB High Priority
0 Low priority..... default
1 High priority
3 Reserved .....always reads 0
2 IDE High Priority
0 Low priority..... default
1 High priority
1 AC97-ISA High Priority
0 Low priority..... default
1 High priority
0 PCI High Priority
0 Low priority..... default
1 High priority

Device 0 Offset 4F – SB V-Link Misc Control (00h)..... RW

7 Upstream Command High Priority
0 Disable high priority up commands..... default
1 Enable high priority up commands
6-1 Reserved .....always reads 0
0 Down Cycle Wait for Up Cycle Write Flush (Except Down Cycle Post Write)
0 Disable..... default
1 Enable

CPU Interface Control

Device 0 Offset 50 – S2K Duty Cycle Adjust 1 (08h).....RW

7-6 S2K Data In Rise Control
- 00 Normal Rise Delay.....default
- 01 Delay Rise by 70 ps
- 10 Delay Rise by 135 ps
- 11 Delay Rise by 300 ps

5-4 S2K Data In Fall Control
- 00 Normal Fall Delay.....default
- 01 Delay Fall by 70 ps
- 10 Delay Fall by 135 ps
- 11 Delay Fall by 300 ps

3-2 S2K Data In Clock-to-Data In Delay
- 00 Data In Clock Earlier by 300 ps
- 01 Data In Clock Earlier by 150 ps
- 10 DataInClk & DataIn have same delay**...default**
- 11 DataInClk Later than DataIn by 150 ps

1-0 Reserved ..... always reads 0

Device 0 Offset 51 – S2K Duty Cycle Adjust 2 (00h).....RW

7-6 S2K Data In Clock Output Rise Control
- 00 Normal Rise Delay.....default
- 01 Delay Rise by 70 ps
- 10 Delay Rise by 135 ps
- 11 Delay Rise by 300 ps

5-4 S2K Data In Clock Output Fall Control
- 00 Normal Fall Delay.....default
- 01 Delay Fall by 70 ps
- 10 Delay Fall by 135 ps
- 11 Delay Fall by 300 ps

3-2 S2K Data Out Clock Input Rise Control
- 00 Normal Rise Delay.....default
- 01 Delay Rise by 70 ps
- 10 Delay Rise by 135 ps
- 11 Delay Rise by 300 ps

1-0 S2K Data Out Clock Input Fall Control
- 00 Normal Fall Delay.....default
- 01 Delay Fall by 70 ps
- 10 Delay Fall by 135 ps
- 11 Delay Fall by 300 ps

Device 0 Offset 52 – S2K Duty Cycle Adjust 3 (00h)..... RW

7-6 S2K Address Out Clock Input Rise Control
- 00 Normal Rise Delay ..... default
- 01 Delay Rise by 70 ps
- 10 Delay Rise by 135 ps
- 11 Delay Rise by 300 ps

5-4 S2K Address Out Clock Input Fall Control
- 00 Normal Fall Delay ..... default
- 01 Delay Fall by 70 ps
- 10 Delay Fall by 135 ps
- 11 Delay Fall by 300 ps

3-2 S2K Address In Rise Control
- 00 Normal Rise Delay ..... default
- 01 Delay Rise by 70 ps
- 10 Delay Rise by 135 ps
- 11 Delay Rise by 300 ps

1-0 S2K Address In Fall Control
- 00 Normal Fall Delay ..... default
- 01 Delay Fall by 70 ps
- 10 Delay Fall by 135 ps
- 11 Delay Fall by 300 ps

Device 0 Offset 53 – S2K Duty Cycle Adjust 4 (80h)..... RW

7-6 S2K Address In Clock-to-Address In Delay
- 00 Address In Clock Earlier by 300 ps
- 01 Address In Clock Earlier by 150 ps
- 10 AddrInClk & AddrIn have same delay**. default**
- 11 AddrInClk Later than AddrIn by 150 ps

5-4 Reserved .....always reads 0

3-2 S2K Address In Clock Output Rise Control
- 00 Normal Rise Delay ..... default
- 01 Delay Rise by 70 ps
- 10 Delay Rise by 135 ps
- 11 Delay Rise by 300 ps

1-0 S2K Address In Clock Output Fall Control
- 00 Normal Fall Delay ..... default
- 01 Delay Fall by 70 ps
- 10 Delay Fall by 135 ps
- 11 Delay Fall by 300 ps

Device 0 Offset 54 – CPU FSB Frequency (00h).....RW

7-6 CPU FSB Frequency.....RO
- 00 100 MHz ..... default set from VAD[6,4]
- 01 133 MHz
- 10 200 MHz
- 11 166 MHz

5 ROMSIP .....RO
- 0 Disable ..... default set from VAD[5]
- 1 Enable

4 SDRAM Burst Length 8
- 0 Disable .....default
- 1 Enable

3 Reserved ..... always reads 0

2 PCI Master 8QW Operation
- 0 Disable .....default
- 1 Enable

1-0 Reserved ..... always reads 0

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies VT8633 BIOS porting guide for details).

Table 6. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys Bus Init	1MB D Top 4G-64K	— 64K	00100000-DRAM Top DRAM Top-FFFEFFFF FFFEFFFF-FFFFFFFF	Can have hole 000Fxxxx alias

Device 0 Offset 55 – DRAM Control (00h) ..... RW

7 0WS Back-to-Back Write to Different DDR Bank
- 0 Disable..... default
- 1 Enable

6 Reserved .....always reads 0

5 DQS Input DLL Adjustment
- 0 Disable..... default
- 1 Enable

4 DQS Output DLL Adjustment
- 0 Disable..... default
- 1 Enable

3 DQM Removal (Always Perform 4-Burst RW)
- 0 Disable..... default
- 1 Enable

2 DQS Output
- 0 Disable..... default
- 1 Enable

1 Auto Precharge for TLB Read or CPU WriteBack
- 0 Disable..... default
- 1 Enable

0 Write Recovery Time
- 0 1T (DDR333/266/200) 3T (DDR400) . default
- 1 2T (DDR333/266/200) 4T (DDR400)

Device 0 Offset 59-58 - DRAM MA Map Type (2222h).RW

15-13 Bank 5/4 MA Map Type (see Table 7 below)

12 Bank 5/4 1T Command Rate
- 0 2T Command .....default
- 1 1T Command

11-9 Bank 7/6 MA Map Type (see Table 7 below)

8 Bank 7/6 1T Command Rate
- 0 2T Command .....default
- 1 1T Command

7-5 Bank 1/0 MA Map Type (see Table 7 below)

4 Bank 1/0 1T Command Rate
- 0 2T Command .....default
- 1 1T Command

3-1 Bank 3/2 MA Map Type (see Table 7 below)

0 Bank 3/2 1T Command Rate
- 0 2T Command .....default
- 1 1T Command

Table 7. MA Map Type Encoding

000	16Mb	8-bit, 9-bit, 10-bit Column Address
001	64/128Mb	8-bit Column Address .....default
010	64/128Mb	9-bit Column Address
011	64/128Mb	10/11-bit Column Address
100		-reserved-
101	256Mb	8-bit Column Address
110	256Mb	9-bit Column Address
111	256Mb	10/11-bit Column Address

Table 8. Memory Address Mapping Table

MA:	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
16Mb		24		13	12	11	14	22	21	20	19	18	17	16	15	12 row
(000)				13	PC	24	23	10	9	8	7	6	5	4	3	10,9,8 col
64/128Mb																x16 (14,8)
2K page	14	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (14,8)
001		27	14	13	PC	26	25	10	9	8	7	6	5	4	3	x8 (14,9)
4K page	14	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (14,9)
010		27	14	13	PC	26	11	10	9	8	7	6	5	4	3	
8K page	14	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x8 (14,10)
011		27	14	13	PC	12	11	10	9	8	7	6	5	4	3	
256Mb																
2K page	25	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (15,8)
101		27	14	13	PC	26	25	10	9	8	7	6	5	4	3	
4K page	26	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (15,9)
110		27	14	13	PC	26	11	10	9	8	7	6	5	4	3	
8K page	27	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x8 (15,10)
111		28	14	13	PC	12	11	10	9	8	7	6	5	4	3	

Device 0 Offset 5F-5A – DRAM Row Ending Address:

Offset 5A – Bank 0 Ending (HA[31:24]) (01h)..... RW
Offset 5B – Bank 1 Ending (HA[31:24]) (01h)..... RW
Offset 5C – Bank 2 Ending (HA[31:24]) (01h)..... RW
Offset 5D – Bank 3 Ending (HA[31:24]) (01h)..... RW
Offset 5E – Bank 4 Ending (HA[31:24]) (01h)..... RW
Offset 5F – Bank 5 Ending (HA[31:24]) (01h)..... RW
Offset 56 – Bank 6 Ending (HA[31:24]) (01h)..... RW
Offset 57 – Bank 7 Ending (HA[31:24]) (01h)..... RW

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Device 0 Offset 61 - Shadow RAM Control 1 (00h).....RW

7-6 CC000h-CFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 C8000h-CBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 C4000h-C7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 C0000h-C3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2 (00h).....RW

7-6 DC000h-DFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 D8000h-DBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 D4000h-D7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 D0000h-D3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3 (00h)..... RW

7-6 E0000h-EFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 F0000h-FFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 Memory Hole
- 00 None ..... default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

1-0 SMI Mapping Control
(Bit-1 = A,BK Direct Access SMRAM Disable)
(Bit-0 = A,BK DRAM Access Enable)

	SMM		Non-SMM	
	Code	Data	Code	Data
00	DRAM	DRAM	PCI	PCI
01	DRAM	DRAM	DRAM	DRAM
10	DRAM	PCI	PCI	PCI
11	DRAM	DRAM	DRAM	DRAM

Device 0 Offset 64 - DRAM Timing for All Banks (E4h)RW

7 Precharge Command to Active Command Period
- 0 TRP = 2T
- 1 TRP = 3T (DDR333/266/200), 4T (400).default

6 Active Command to Precharge Command Period
- 0 TRAS = 6T (DDR333/266/200), 8T (400)
- 1 TRAS = 7T (DDR333/266/200), 10T (400)...def

5-4 CAS Latency
- 00 1.5T
- 01 2T
- 10 2.5T .....default
- 11 3T

3 Reserved ..... always reads 0

2 ACTIVE to CMD
- 0 2T
- 1 3T (DDR333/266/200), 4T (DDR400)...default

1-0 Bank Interleave
- 00 No Interleave.....default
- 01 2-way
- 10 4-way
- 11 Reserved

For 16Mb SDRAMs, bank interleave is always 2-way

Device 0 Offset 65 - DRAM Arbitration Timer (00h) ....RW

7-4 AGP Timer (units of 4 MCLKs)..... default = 0

3-0 CPU Timer (units of 4 MCLKs)..... default = 0

Device 0 Offset 66 - DRAM Arbitration Control (00h)..RW

7 DQS Input Delay Setting
- 0 Auto (Rx67 reads DLL calibration result) ...def
- 1 Manual (Rx67 reads DQS input delay)

6 DRAM Access Timing
- 0 2T .....default
- 1 3T (Set for 133 MHz DRAM clock)

5-4 Arbitration Parking Policy
- 00 Park at last bus owner .....default
- 01 Park at CPU
- 10 Park at AGP
- 11 -reserved-

3-0 AGP / CPU Priority (units of 4 MCLKs)

Device 0 Offset 67 – DDR Strobe Input Delay (00h)..... RW

7-6 Reserved .....always reads 0

5-0 DQS# Input Delay .....default = 0

(if Rx66[7]=0, read DLL calibration result)

Device 0 Offset 68 – DDR Strobe Output Delay (00h)... RW

7-0 DDR DQS Output Delay .....default = 0

Device 0 Offset 69 – DRAM Clock Select (00h).....RW

7 CPU Operating Frequency Faster Than DRAM
- 0 CPU Same As or Equal to DRAM.....default
- 1 CPU Faster Than DRAM by 33 MHz

6 DRAM Operating Frequency Faster Than CPU
- 0 DRAM Same As or Equal to CPU.....default
- 1 DRAM Faster Than CPU by 33 MHz

Bits 7-6	CPU FSB Freq	DDR DRAM Freq
00	100	100 (DDR200)
	133	133 (DDR266)
	166	166 (DDR333)
01	100	133 (DDR266)
	133	166 (DDR333)
10	–	200 (DDR400)
11	100	166 (DDR333)

Note: The strap information sent from the South Bridge on VAD6,4 determines the CPU FSB frequency, then Rx69[7-6] determines the DRAM frequency and type per the table above. All other combinations are reserved.

5 DRAM Queue More Than 2
- 0 Disable .....default
- 1 Enable

4 DRAM Controller Queue Not Equal To 4
- 0 Disable .....default
- 1 Enable

3 DRAM 8K Page Enable
- 0 Disable .....default
- 1 Enable

2 DRAM 4K Page Enable
- 0 Disable .....default
- 1 Enable

1 Reserved (Do Not Program)..... default = 0

0 Multiple Page Mode
- 0 Disable .....default
- 1 Enable

Device 0 Offset 6A - Refresh Counter (00h)..... RW

7-0 Refresh Counter (in units of 16 DRAM Clocks)
- 00 DRAM Refresh Disabled ..... default
- 01 32 DRAM Clocks
- 02 48 DRAM Clocks
- 03 64 DRAM Clocks
- 04 80 DRAM Clocks
- 05 96 DRAM Clocks
- … …

The programmed value is the desired number of 16-DRAM-Clock units minus one.

Device 0 Offset 6B - DRAM Arbitration Control (00h).RW

7 Fast Read to Write Turn-Around
- 0 Disable .....default
- 1 Enable

6 Page Kept Active When Cross Bank
- 0 Disable .....default
- 1 Enable

5 Burst Refresh
- 0 Disable .....default
- 1 Enable

4 Reserved ..... always reads 0

3 Swap CA22 / CA14
- 0 Enable .....default
- 1 Disable

2-0 SDRAM Operation Mode Select
- 000 Normal SDRAM Mode.....default
- 001 NOP Command Enable
- 010 All-Banks-Precharge Command Enable (CPU-to-DRAM cycles are converted to All-Banks-Precharge commands).
- 011 MSR Enable CPU-to-DRAM cycles are converted to commands and the commands are driven on MA[14:0]. The BIOS selects an appropriate host address for each row of memory such that the right commands are generated on MA[14:0].
- 100 CBR Cycle Enable (if this code is selected, CAS-before-RAS refresh is used; if it is not selected, RAS-Only refresh is used)
- 101 Reserved
- 11x Reserved

Device 0 Offset 6C – DRAM Early Clock Select (00h).. RW

7-6 CS / CKE Early Clock Select
- 00 Latest ..... default
- 01
- 10
- 11 Earliest

5-4 Early Clock Select for SCMD, MA Output (for 1T Command)
- 00 Latest ..... default
- 01
- 10
- 11 Earliest

3-1 Reserved .....always reads 0

0 Reserved (Do Not Program)..... default = 0

Device 0 Offset 6D – DRAM MD Output Delay (00h)... RW

7-0 MD Output Delay..... default = 0

Note: Refer to the BIOS Developers Guide for recommended memory configuration detection algorithms and recommended settings for the bits of the above two registers.

PCI Bus Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer Control (00h).....RW

7 CPU to PCI Post-Write
- 0 Disable .....default
- 1 Enable

6 Reserved ..... always reads 0

5-4 PCI Master to DRAM Prefetch
- 00 Always prefetch .....default
- x1 Never prefetch
- 10 Prefetch only for Enhance command

3 Reserved ..... always reads 0

2 PCI Master Read Buffering
- 0 Disable .....default
- 1 Enable

1 Delay Transaction
- 0 Disable .....default
- 1 Enable

0 Reserved ..... always reads 0

Device 0 Offset 71 - CPU to PCI Flow Control (48h)..RWC

7 Retry Status.....RWC
- 0 No retry occurred .....default
- 1 Retry occurred

6 Retry Timeout Action
- 0 Retry forever (record status only)
- 1 Flush buffer or return FFFFFFFFh for reads .....default

5-4 Retry Count and Retry Backoff
- 00 Retry 2 times, backoff CPU .....default
- 01 Retry 16 times
- 10 Retry 4 times
- 11 Retry 64 times

3 PCI Burst
- 0 Disable
- 1 Enable .....default

2 Reserved ..... always reads 0

1 Compatible Type#1 Configuration Cycles
- 0 Disable (fixed AD31).....default
- 1 Enable

0 IDSEL Control
- 0 AD11, AD12 .....default
- 1 AD30, AD31

Device 0 Offset 73 - PCI Master Control (00h) ..... RW

7 Reserved .....always reads 0

6 PCI Master 1-Wait-State Write
- 0 Zero wait state TRDY# response..... default
- 1 One wait state TRDY# response

5 PCI Master 1-Wait-State Read
- 0 Zero wait state TRDY# response..... default
- 1 One wait state TRDY# response

4 WSC# Enable
- 0 Disable..... default
- 1 Enable

3-1 Reserved .....always reads 0

0 PCI Master Broken Timer Enable
- 0 Disable..... default
- 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Device 0 Offset 75 - PCI Arbitration 1 (00h) .....RW

7 Arbitration Mode
- 0 REQ-based (arbitrate at end of REQ#) ..default
- 1 Frame-based (arbitrate at FRAME# assertion)

6-4 Latency Timer.....read only, reads Rx0D bits 2:0

3 Reserved ..... always reads 0

2-0 PCI Master Bus Time-Out

(force into arbitration after a period of time)
- 000 Disable .....default
- 001 1x16 PCICLKs
- 010 2x16 PCICLKs
- 011 3x16 PCICLKs
- 100 4x16 PCICLKs
- ... ...
- 111 7x16 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2 (00h)..... RW

7 I/O Port 22 Access
- 0 CPU access to I/O address 22h is passed on to the PCI bus ..... default
- 1 CPU access to I/O address 22h is processed internally

6 Reserved .....always reads 0

5-4 Master Priority Rotation Control
- 00 Disable..... default
- 01 Grant to CPU after every PCI master grant
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

With setting 01, the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting. With setting 10, if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes. With setting 11, if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus. In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

3-2 REQn# to REQ4# Mapping
- 00 REQ4# ..... default
- 01 REQ0#
- 10 REQ1#
- 11 REQ2#

1 Reserved .....always reads 0

0 REQ4# Is High Priority Master
- 0 Disable..... default
- 1 Enable

GART / Graphics Aperture

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the VT8377.

This scheme is shown in the figure below.

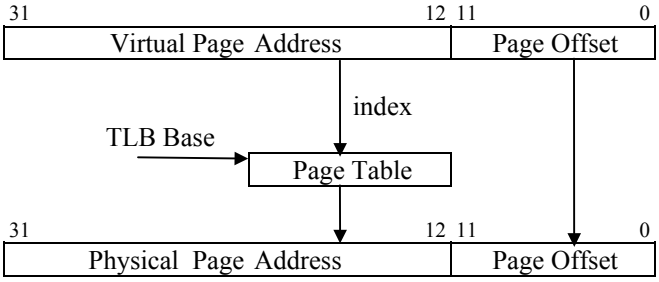


Figure 4. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the VT8377 contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc) for AGP 2.0 and 4MB to 2GB for AGP 3.0. The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register groups (Rx84 and 88 respectively for AGP 2.0 and Rx94 and 98 for AGP 3.0) along with various control bits.

AGP 2.0 Registers

AGP 2.0 registers Rx80-AB are enabled if RxFD[1] = 1 and AGP 3.0 registers Rx80-AB are enabled if RxFD[1] = 0.

Device 0 Offset 83-80 – AGP 2.0 GART/TLB Control...RW

31-16 Reserved ..... always reads 0
15-8 Reserved (test mode status)..... RO
7 Flush Page TLB
0 Disable .....default
1 Enable
6-0 Reserved (always program to 0) ..... RW

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 – AGP 2.0 Graphics Aperture Size ..RW

7-0 Graphics Aperture Size
11111111 -reserved-
11111110 -reserved-
11111100 4M
11111000 8M
11110000 16M
11100000 32M
11000000 64M
10000000 128M
00000000 256M

Offset 8B-88 – AGP 2.0 GART Table Base.....RW

31-12 Graphics Aperture Translation Table Base. Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).
11-2 Reserved ..... always reads 0
1 Graphics Aperture
0 Disable .....default
1 Enable
Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.
0 Reserved ..... always reads 0

Device 0 Offset A3-A0 - AGP 2.0 Capabilities (0020C002h) .....RO

31-24 Reserved ..... always reads 00
23-20 Major Specification Revision ... always reads 0010b
Major rev # of AGP spec that device conforms to
19-16 Minor Specification Revision ... always reads 0000b
Minor rev # of AGP spec that device conforms to
15-8 Pointer to Next Item ..... always reads C0 (last item)
7-0 AGP Capability ID
(always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP 2.0 Status (1F000201h).... RO

31-24 Maximum AGP Requests .....always reads 1Fh
Max # of AGP requests the device can manage (32)
23-10 Reserved ..... always reads 0s
9 Supports SideBand Addressing..... **always reads 1**
8-6 Reserved ..... always reads 0s
5 Addresses Above 4G Supported.....always reads 0†
4 Fast Write Supported .....always reads 0†
3 Reserved ..... always reads 0s
2 4X Rate Supported.....always reads 0†
1 2X Rate Supported.....always reads 0†
0 1X Rate Supported..... **always reads 1**
†Writable if RxFD[0] = 1.

Device 0 Offset AB-A8 - AGP 2.0 Command ..... RW

31-24 Request Depth (reserved for target).. always reads 0s
23-10 Reserved ..... always reads 0s
9 SideBand Addressing Enable
0 Disable..... default
1 Enable
8 AGP Enable
0 Disable..... default
1 Enable
7-6 Reserved ..... always reads 0s
5 4G Enable
0 Disable..... default
1 Enable
4 Fast Write Enable
0 Disable..... default
1 Enable
3 Reserved ..... always reads 0s
2 4X Mode Enable
0 Disable..... default
1 Enable
1 2X Mode Enable
0 Disable..... default
1 Enable
0 1X Mode Enable
0 Disable..... default
1 Enable

AGP 3.0 Registers

AGP 3.0 registers Rx80-AB are enabled if RxFD[1] = 0 and AGP 2.0 registers Rx80-AB are enabled if RxFD[1] = 1.

Device 0 Offset 83-80 - AGP 3.0 Capabilities (0030C002h) .....RO

31-24 Reserved ..... always reads 00
23-20 Major Specification Revision ... always reads 0011b
Major rev # of AGP spec that device conforms to
19-16 Minor Specification Revision ... always reads 0000b
Minor rev # of AGP spec that device conforms to
15-8 Pointer to Next Item ..... always reads C0 (last item)
7-0 AGP Capability ID
(always reads 02 to indicate it is AGP)

Device 0 Offset 87-84 - AGP 3.0 Status (1F000201h) .....RO

31-24 Maximum AGP Requests..... always reads 1Fh
Max # of AGP requests the device can manage (32)
23-16 Reserved .....always reads 0s†
15-13 Optimum Async Request Size.....always reads 0s†
Suggested setting is 010b or 2^(2+4)=64 Bytes for 8QW access
12-10 Calibration Cycle Setting
000 4 ms
001 16 ms
010 64 ms **.....default†**
011 256 ms
9 Supports SideBand Addressing ..... **always reads 1**
8 Reserved ..... always reads 0†
7 64-Bit GART Entries..... always reads 0
6 CPU GART Translation Supported. always reads 0
5 Addresses Above 4G Supported ..... always reads 0
4 Fast Write Supported..... always reads 0
3 AGP 8x Detected.....Set from AGP8XDT# pin
2 4X Rate Supported .....Reads 0 if bit-3 = 1
.....Reads 1 if bit-3 = 0
1 2X Rate Supported ..... **always reads 1**
0 1X Rate Supported ..... **always reads 1**

†Writable if RxFD[0] = 1.

Device 0 Offset 8B-88 - AGP 3.0 Command..... RW

31-24 Request Depth (reserved for target).. always reads 0s
23-13 Reserved ..... always reads 0s
12-10 Calibration Cycle Select..... default = 0
9 SideBand Addressing
0 Disable..... default
1 Enable
8 AGP
0 Disable..... default
1 Enable
7-6 Reserved ..... always reads 0s
5 Addresses Over 4G
0 Disable..... default
1 Enable
4 Fast Write
0 Disable..... default
1 Enable
3 Reserved ..... always reads 0s
2-0 Transfer Mode Select..... default = 000b
Rx84[3] = 0 (8x mode **not detected** via AGP8XDT#)
001 1x data transfer rate
010 2x data transfer rate
100 4x data transfer rate
Rx84[3] = 1 (8x mode **detected** via AGP8XDT#)
000 -reserved..... default
001 4x data transfer rate
010 8x data transfer rate

Device 0 Offset 93-90 - AGP 3.0 GART / TLB Control .RW

31-10 Reserved .....always reads 0s

9 Calibration Cycle
- 0 Disable .....default
- 1 Enable

8 Graphics Aperture Base Register (Rx13-10) Read
- 0 Disable .....default
- 1 Enable

7 GART TLB
- 0 Disable (TLB entries are invalidated) ....default
- 1 Enable

6-0 Reserved .....always reads 0s

Device 0 Offset 97-94 - AGP 3.0 Graphics Aperture SizeRW

31-28 Aperture Page Size Select.....default = 0000b
Only 4K pages are allowed

27 Reserved ..... always reads 0s

26-16 Page Size Supported.....default = 001h
If bit-n of this field is 1, indicates support of 2^(n+12) page size. Must be set to 001h (field bit-0 set) to indicate only 4K pages allowed.

15-12 Reserved ..... always reads 0s

11-0 Aperture Size.....default = 0

111100111111	4MB
111100111110	8MB
111100111100	16MB
111100111000	32MB
111100110000	64MB
111100100000	128MB
111100000000	256MB
111000000000	512MB
110000000000	1GB
100000000000	2GB <= Max supported
000000000000	4GB <= Do not program

Device 0 Offset 9B-98 - AGP 3.0 GART Table Base..... RW

31-12 GART Base Address [31:12] .....default = 0

11-0 Reserved ..... always reads 0s

AGP 2.0 / 3.0 Registers

Device 0 Offset AC - AGP Control (00h) .....RW

7 AGP .....RO per strap on MAB9
- 0 Disable .....default
- 1 Enable

6 AGP Read Synchronization
- 0 Disable .....default
- 1 Enable

5 AGP Read Snoop DRAM Post-Write Buffer
- 0 Disable .....default
- 1 Enable

4 GREQ# Priority Becomes Higher When Arbiter is Parked at AGP Master
- 0 Disable .....default
- 1 Enable

3-2 Reserved .....always reads 0s

1 AGP Arbitration Parking
- 0 Disable .....default
- 1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)

0 AGP to PCI Master or CPU to PCI Turnaround Cycle
- 0 2T or 3T Timing.....default
- 1 1T Timing

Device 0 Offset AD – AGP Latency Timer (02h).....RW

7 AGP Performance Improvement
- 0 Disable .....default
- 1 Enable

6 Pipe Mode Performance Improvement
- 0 Disable .....default
- 1 Enable

5 AGP Data Input Enable (for Power Saving)
- 0 AGP data input always enabled .....default
- 1 AGP data input only enabled when necessary to avoid redundant transitions

4 AGP Performance Improvement
- 0 Disable .....default
- 1 Enable

3-0 AGP Data Phase Latency Timer ..... default = 02h

Device 0 Offset AE – AGP Misc Control (00h) ..... RW

7-3 Reserved .....always reads 0

2 AGP Performance Improvement
- 0 Disable..... default
- 1 Enable

1 DBI / PIPE Mux Function
- 0 From DBIH (0.95)..... default
- 1 From PIPE (0.9)

0 CPU GART Read, AGP GART Write Coherency
- 0 Disable..... default
- 1 Enable

Device 0 Offset AF – AGP 3.0 Control (00h)..... RW

7 CPU / PCI Master GART Access
- 0 Disable..... default
- 1 Enable

6 AGP Calibration
- 0 Disable..... default
- 1 Enable

5 Mix Coherent / Non-coherent Accesses
- 0 Disable..... default
- 1 Enable

4 Reserved .....always reads 0

3 DBI Function
- 0 Disable (DBI input masked and all outputs assume DBI=0)..... default
- 1 Enable

2 DBI Output for AGP Transactions
- 0 Disable..... default
- 1 Enable

1 DBI Output for Frame Transactions Including Fast-Write
- 0 Disable..... default
- 1 Enable

0 DBI Output from Frame Transactions
- 0 Disable..... default
- 1 Enable

Device 0 Offset B0 – AGP Pad Control / Status (8xh)....RW

7 AGP 4x Strobe VREF Control
- 0 STB VREF is STB# and vice versa
- 1 STB VREF is AGPREF **.....default**

6 AGP 4x Strobe & GD Pad Drive Strength
- 0 Drive strength set to compensation circuit default .....default
- 1 Drive strength controlled by RxB1[7-0]

5-3 AGP Compensation Circuit N Control Output.RO

2-0 AGP Compensation Circuit P Control Output .RO

Note: N = low drive, P = high drive

Device 0 Offset B1 – AGP Drive Strength (63h).....RW

7-4 AGP Output Buffer Low Drive Strength..... def=6

3-0 AGP Output Buffer High Drive Strength..... def=3

Device 0 Offset B2 – AGP Pad Drive / Delay (08h)..... RW

7 GD/GBE/GDS, SBA/SBS Control
- 0 SBA/SBS = no cap ..... default
  GD/GBE/GDS = no cap
- 1 SBA/SBS = **cap**
  GD/GBE/GDS = **cap**

6-5 GD / GBE Receive Strobe Delay
- 00 None ..... default
- 01 Delay by 0.15 ns
- 10 Delay by 0.30 ns
- 11 Delay by 0.45 ns

4 GD[31-16] Staggered Delay
- 0 None ..... default
- 1 GD[31:16] delayed by 1 ns

3 AGP Slew Rate Control
- 0 Disable
- 1 Enable**..... default**

2 SBA Receive Strobe Delay
- 0 None ..... default
- 1 Delay by 0.15 ns

1-0 GDS Output Delay
- 00 None ..... default
- 01 Delay by 0.15 ns
- 10 Delay by 0.30 ns
- 11 Delay by 0.45 ns

(GDS1 & GDS1# will be delayed an additional 1ns if bit-4 = 1)

Device 0 Offset B3 – AGP Strobe Drive Strength..... RW

7-4 AGP Strobe Output Low Drive Strength.....def=0

3-0 AGP Strobe Output High Drive Strength .....def=0

V-Link Drive Control Registers

Device 0 Offset B4 – V-Link NB Compensation Ctrl (00h)RW

7-5 **V-Link Autocomp High Output Value** ...def=0, RO
4 **Reserved** ..... always reads 0
3-1 **V-Link Autocomp Low Output Value** ....def=0, RO
0 **Compensation Selection**
0 Auto Comp (use values in bits 7-1).....default
1 Manual Comp (use values in RxB5-B6)

Device 0 Offset B5 – V-Link NB Strobe Drive Ctrl (00h)RW

7-5 **Strobe High Drive Manual Setting**..... default = 0
4 **Reserved** ..... always reads 0
3-1 **Strobe Low Drive Manual Setting** ..... def = 0
0 **Reserved** ..... always reads 0

Device 0 Offset B6 – V-Link NB Data Drive Ctrl (00h).RW

7-5 **Data High Drive Manual Setting**..... default = 0
4 **Reserved** ..... always reads 0
3-1 **Data Low Drive Manual Setting** ..... default = 0
0 **Reserved** ..... always reads 0

Device 0 Offset B8 – V-Link SB Compensation Ctrl (00h)RW

7-5 **V-Link Autocomp High Output Value**... def=0, RO
4 **Reserved** .....always reads 0
3-1 **V-Link Autocomp Low Output Value**.... def=0, RO
0 **Compensation Selection**
0 Auto Comp (use values in bits 7-1) ..... default
1 Manual Comp (use values in RxB9-BA)

Device 0 Offset B9 – V-Link SB Strobe Drive Ctrl (00h)RW

7-5 **Strobe High Drive Manual Setting** .....default = 0
4 **Reserved** .....always reads 0
3-1 **Strobe Low Drive Manual Setting** .....def = 0
0 **Reserved** .....always reads 0

Device 0 Offset BA – V-Link SB Data Drive Ctrl (00h) RW

7-5 **Data High Drive Manual Setting** .....default = 0
4 **Reserved** .....always reads 0
3-1 **Data Low Drive Manual Setting** .....default = 0
0 **Reserved** .....always reads 0

Power Management Registers

Device 0 Offset BC – Power Management Mode (00h)..RW

7 Dynamic Power Management
- 0 Disable .....default
- 1 Enable

6 Halt / Shutdown Enables Power Management
- 0 Disable .....default
- 1 Enable

5 Stop Clock Enables Power Management
- 0 Disable .....default
- 1 Enable

4 Suspend Status Enables Power Management
- 0 Disable .....default
- 1 Enable

3-0 Reserved ..... always reads 0

Device 0 Offset BD – DRAM Power Mgmt Mode (00h) RW

7 DRAM Self-Refresh in Power Management Mode
- 0 Disable .....default
- 1 Enable

6 Dynamic CKE When DRAM Is Idle
- 0 Disable .....default
- 1 Enable

5 Dynamic DRAM I/O Pad Power-Down (Float)
- 0 Disable .....default
- 1 Enable

4-0 Reserved ..... always reads 0

Device 0 Offset BE – Dynamic Clock Stop Control (00h)RW

7 Host CPU Interface Power Management
- 0 Disable .....default
- 1 Enable

6 DRAM Interface Power Management
- 0 Disable .....default
- 1 Enable

5 V-Link Interface Power Management
- 0 Disable .....default
- 1 Enable

4 AGP Interface Power Management
- 0 Disable .....default
- 1 Enable

3 PCI#2 Interface Power Management
- 0 Disable .....default
- 1 Enable

2 Graphics Interface Power Management
- 0 Disable .....default
- 1 Enable

1 Reserved ..... always reads 0

0 Host CPU Fast Power Management (DADS Fast Timing)
- 0 Disable .....default
- 1 Enable

Device 0 Offset BF – DRAM Pad Toggle Reduction (00h)RW

7 MA / SCMD Pin Toggle Reduction
- 0 Disable..... default
- 1 Enable (MA and S command pins won't toggle if not accessed)

6-0 Reserved .....always reads 0

Extended Power Management

Device 0 Offset C0 – Power Management Capability ID RO

7-0 Capability ID ..... always reads 01h

Device 0 Offset C1 – Power Management New Pointer .. RO

7-0 New Pointer ..... always reads 00h ("Null" Pointer)

Device 0 Offset C2 – Power Mgmt Capabilities I ..... RO

7-0 Power Management Capabilities .. always reads 02h

Device 0 Offset C3 – Power Mgmt Capabilities II ..... RO

7-0 Power Management Capabilities .. always reads 00h

Device 0 Offset C4 – Power Mgmt Control / Status ..... RW

7-2 Reserved ..... always reads 0

1-0 Power State

00 D0 ..... default
01 -reserved-
10 -reserved-
11 D3 Hot

Device 0 Offset C5 – Power Management Status..... RW

7-0 Power Management Status ..... default = 0

Device 0 Offset C6 – PCI-to-PCI Bridge Support Ext... RW

7-0 P2P Bridge Support Extensions ..... default = 0

Device 0 Offset C7 – Power Management Data ..... RW

7-0 Power Management Data ..... default = 0

Host CPU Interface Control Registers

Device 0 Offset D2 – S2K Timing Control III (78h).....RW

The contents of this register are preserved during suspend. Bits 2-0 have no default value.

- **7** **Disconnect Enable When STPGNT Detected**
- **6** **Write to Read Delay** ..... default = 1
- **5-4** **Read to Write Delay** ..... default = 11b
- **3** **Reserved (Do Not Program)**..... default = 1
- **2-0** **Write Data Delay from SYSDC to CPU Data Output** ..... (WrDataDly)

Device 0 Offset D3 – BIU Arbitration Control .....RW

- **7-6** **Max of Contiguous Probe SysDC Before Switch to Other Type of SysDC**
- **5-3** **Max of Contiguous Read SysDC Before Switch to Other Type of SysDC**
- **2-0** **Max of Contiguous Write SysDC Before Switch to Other Type of SysDC**

Device 0 Offset D4 – BIU Control 1.....RW

- **7** **DRAM Self-Refresh When Disconnected**
  - 0 Disable .....default
  - 1 Enable
- **6** **Probe Next Tag State T1 When PCI Master Read Caching Enabled**
  - 0 Disable .....default
  - 1 Enable
- **5** **64 HCLK Wait Time**
  - 0 Disable .....default
  - 1 Enable
- **4** **Master Request Full Protocol**
  - 0 Enhanced.....default
  - 1 Backwards compatible

  VIA recommends setting this bit to 0
- **3** **DRAM Speculative Read for PCI Master Read (Before Probe Result is Known)**
  - 0 Disable .....default
  - 1 Enable
- **2** **PCI Master Pipeline Request**
  - 0 Disable .....default
  - 1 Enable
- **1** **PCI-to-CPU / CPU-to-PCI (P2C / C2P) Concurrency**
  - 0 Disable .....default
  - 1 Enable
- **0** **Fast Write-to-Read Turnaround**
  - 0 Disable .....default
  - 1 Enable

Device 0 Offset D5 – BIU Control 2 ..... RW

- **7** **FWDVLD / PSQHPTR Concurrency**
  - 0 Backwards Compatible..... default
  - 1
- **6** **RHOCTW**
  - 0 ..... default
  - 1
- **5** **PMW Address Compare**
  - 0 Backward compatible ..... default
  - 1 Compare address qualified with PMW
- **4** **Write Policy for CPU Write to DRAM**
  - 0 Issue DRAM write when FIFO holds more than two requests or DRAM controller idle def
  - 1 Disable Write Policy
- **3** **PMR Cycle Control**
  - 0 Stall PMR cycle if MWQ is full ..... default
  - 1 Execute PMR cycles normally whether MWQ is full or not
- **2** **FID Command Detect**
  - 0 Disable (command will not have new FID). def
  - 1 Enable
- **1** **HALT Command Detect**
  - 0 Disable (command will not do self refresh) def
  - 1 Enable
- **0** **Reserved** .....always reads 0

Device 0 Offset D6 – BIU Control 3 ..... RW

- **7** **Memory Write Queue Timer Function**
  - 0 Disable..... default
  - 1 Enable
- **6** **Memory Write Queue Timer Function Trigger**
  - 0 Trigger by data ready for C2M Wr Req ..... def
  - 1 Trigger by command FIFO utilization
- **5-3** **Memory Write Queue Timer High Bound**.....def=0
- **2-0** **Memory Write Queue Timer Low Bound**.....def=0

  Bits 5-0 are defined in units of 4QW / request number

Device 0 Offset D7 – CPU Strapping Control.....RO

7-3 CPU Clock Divide.....set from VAD[3-0] straps

00000 11 .....no strap default
00001 11.5
00010 12
00011 12.5
00100 5
00101 5.5
00110 6
00111 6.5
01000 7
01001 7.5
01010 8
01011 8.5
01100 9
01101 9.5
01110 10
01111 10.5
10000 3
10001 3.5
10010 4
10011 4.5
101xx -reserved-

2 S2K Drive Strength

0 Determined by register settings.....default
1 Determined by auto compensation

1 Fast Address Out Decode .....set from ROMSIP#

0 Normal .....no strap default
1 Fast

0 S2K Compensation Circuit

0 Always Enable .....default
1 Enable on Disconnect

Device 0 Offset D8 – S2K Compensation Strapping (00h)RW

7-4 S2K Pullup Drive Strength ..... default = 0
3-0 S2K Pulldown Drive Strength ..... default = 0

Device 0 Offset D9 – S2K Compensation Result 1 (00h).RO

7-4 Pullup Auto Compensation Result ..... default = 0
3-0 Pulldown Auto Compensation Result ... default = 0

Device 0 Offset DA – S2K Compensation Result 2.....RW

7 S2K Edge DQ Mode..... RO, set from MA11 strap

0 Central DQ .....default
1 Edge DQ

6-0 S2K Strobe Delay (EdgeDQ)..... .....set from MA[8-4] straps

0 Auto Mode .....no-strap default
~0 Strapping Mode

Device 0 Offset DB – S2K Compensation Result 3.....RO

7-0 S2K Strobe DLL Delay Counter (Auto)..... def = 0

Device 0 Offset DC – S2K Compensation Result 4 (07h)RW

7 S2K Compensation Circuit Trigger
6 DLL Autodetect..... RO
5 Delay Compensation Counter Control
4-3 S2K Pad AC Coupling to VREF Signal in Address / Data Output Clock
2-0 S2K Pad Slew Rate Ctrl (7h is strongest).... def=7h

Device 0 Offset DD – S2K Compensation Result 5..... RW

7-4 S2K Strobe Output Drive Strength P Control
3-0 S2K Strobe Output Drive Strength N Control

Device 0 Offset DE – BIU Control 4..... RW

7 Pending Memory Read

0 Read not pending..... default
1 Read pending

6 Issue Memory Write Queue Ready When Command FIFO is Empty Enough (>24)

0 Disable..... default
1 Enable

5 Issue Memory Write Queue If More Than 4 CPU Requests Are Pending

0 Disable..... default
1 Enable

4 Fast Write Performance Improvement

0 Backwards Compatible..... default
1 Enable performance improvement

3 Issue Write DADS Only When Memory Write Queue Timer or DM Idle or HB Hit

0 Disable..... default
1 Enable

2 Compare Partial Address to Decide if CPU-to-Memory Read Hit CPU-to-Memory Write

0 Compare HA[31:6] (backwards compatible)def
1 Compare HA[31:12]

1 P2C Write Priority Over Read

0 Priority not given to Write..... default
1 Priority given to write

0 DPH5 Performance Improvement

0 Enable..... default
1 Disable

Device 0 Offset DF – BIU Control 5..... RO

7 Transparent MD to HD Synchronous Mode Performance Improvement .....def = 0

0 Disable..... default
1 Enable

6-0 Reserved .....always reads 0

Frame Buffer Control

Device 0 Offset E0 – CPU Direct Access FB Base (00h) RW

7-1 CPU Direct Access FB Base Address[27:21] . def=0

0 CPU Direct Access Frame Buffer

0 Disable .....default
1 Enable

Device 0 Offset E1 – CPU Direct Access FB Size (00h)..RW

7 Internal VGA

0 Disable .....default
1 Enable

6-4 Frame Buffer Size

000 None .....default
001 -reserved-
010 -reserved-
011 -reserved-
100 16MB
101 32MB
110 64MB
111 -reserved-

3-0 CPU Direct Access FB Base Address[31:28] . def=0

Device 0 Offset E2 – VGA Arbitration Timer (00h) .....RW

7-4 VGA High Priority Timer (units of 16 MCLKs)def=0

3-0 VGA Timer (units of 16 MCLKs) ..... default = 0

Device 0 Offset E3 – Graphics Arbitration Timer (00h)RW

7-4 Timer to Promote Graphics Priority
(units of 16 MCLKs) ..... default = 0

3-2 Reserved ..... always reads 0

1-0 Probing Signal Select..... default = 0

DRAM Above 4G Control

Device 0 Offset E4 – Low Top Address Low (00h) ..... RW

7-4 Low Top Address Low.....default = 0

3-0 DRAM Granularity

0 16M Total DRAM less than 4G ..... default
1 32M Total DRAM less than 8G
2 64M Total DRAM less than 16G
3 128M Total DRAM less than 32G
4 256M Total DRAM less than 64G
5-7 -reserved-

Device 0 Offset E5 – Low Top Address High (FFh) ..... RW

7-0 Low Top Address High.....default = FFh

Device 0 Offset E6 – SMM / APIC Decoding (01h) ..... RW

7-6 Reserved .....always reads 0

5 Reserved (Do Not Program)..... default = 0

4 I/O APIC Decoding

0 FECxxxxx accesses go to PCI..... default
1 FEC00000 to FEC7FFFF accesses go to PCI
FEC80000 to FECFFFFF accesses go to AGP

3 MSI (Processor Message) Support

0 Disable (master access to FEExxxxx will go to PCI) ..... default
1 Enable (master access to FEExxxxx will be passed to host side to do snoop)

2 Top SMM

0 Disable..... default
1 Enable

1 Reserved .....always reads 0

0 Compatible SMM

0 Disable
1 Enable**..... default**

DRAM Drive Control Registers

Device 0 Offset E8 – DQ Drive Control.....RW

7-4 High Drive – MD and DQM Pins
0000 Lowest.....default
0001
… …
1111 Highest

3-0 Low Drive – MD and DQM Pins
0000 Lowest.....default
0001
… …
1111 Highest

Device 0 Offset E9 – CS Drive Control .....RW

7-4 High Drive – CS#, CKE Pins
0000 Lowest.....default
0001
… …
1111 Highest

3-0 Low Drive – CS#, CKE Pins
0000 Lowest.....default
0001
… …
1111 Highest

Device 0 Offset EA – MAA Drive Control .....RW

7-4 High Drive – MAA, SRASA, SCASA, SWEA Pins
0000 Lowest.....default
0001
… …
1111 Highest

3-0 Low Drive – MAA, SRASA, SCASA, SWEA Pins
0000 Lowest.....default
0001
… …
1111 Highest

Device 0 Offset EC – DRAM S-Port Control ..... RW

7 DQ S-Port Control .....default = 0
6 CS# S-Port Control .....default = 0
5 MAA S-Port Control.....default = 0
4 Reserved .....always reads 0
3 DQS S-Port Control .....default = 0
2-0 Reserved .....always reads 0

Device 0 Offset ED – DRAM DQS Drive Control..... RW

7-4 High Drive - DQS
0000 Lowest ..... default
0001
… …
1111 Highest

3-0 Low Drive - DQS
0000 Lowest ..... default
0001
… …
1111 Highest

Device 0 Offset EE – DRAM DQS/MD Duty Cycle CtrlRW

This register is used for duty cycle adjustment.

7-6 DQS / MD Output Rise Time Control
5-4 DQS / MD Output Fall Time Control
3-0 Reserved .....always reads 0

BIOS Scratch

Device 0 Offset F3 – BIOS Scratch Register 3 ..... RW

7-0 No hardware function .....default = 0

Device 0 Offset F4 – BIOS Scratch Register 4 ..... RW

7-0 No hardware function .....default = 0

Miscellaneous

Device 0 Offset FD – AGP 2.0 / 3.0 Select..... RW

7-3 Reserved .....always reads 0
2 AGP Capability Pointer (Rx34) Value
0 Rx34 = A0h (AGP 2.0)..... default
1 Rx34 = 80h (AGP 3.0)
1 Compatible Rx80-AF
0 AGP 3.0 registers at Rx80-B3 ..... default
1 AGP 2.0 registers at Rx80-B3
0 AGP Status Register Write
0 Disable (AGP 3.0 Rx84 is RO) ..... default
1 Enable (AGP 3.0 Rx84 is RW)

Device 1 Header Registers - PCI-to-PCI Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h) .....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (B168h) .....RO

15-0 ID Code (reads B091h to identify the KM400A PCI-to-PCI Bridge device)

Device 1 Offset 5-4 – Command (0007h) .....RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....**RW**
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop (Not Supported) ..... RO
- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette writes on PCI bus (10-bit decode of I/O addresses 3C6-3C9 hex)

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

2 Bus Master .....**RW**
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface .....default

1 Memory Space.....**RW**
- 0 Does not respond to memory space
- 1 Enable memory space access .....default

0 I/O Space .....**RW**
- 0 Does not respond to I/O space
- 1 Enable I/O space access .....default

Device 1 Offset 7-6 - Status (Primary Bus) (0230h) .... RWC

15 Detected Parity Error .....always reads 0

14 Signaled System Error (SERR#).....always reads 0

13 Signaled Master Abort
- 0 No abort received..... default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles)..... ..... write 1 to clear

12 Received Target Abort
- 0 No abort received..... default
- 1 Transaction aborted by the target with Target-Abort.....

11 Signaled Target Abort.....always reads 0

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium .....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected .....always reads 0

7 Fast Back-to-Back Capable .....always reads 0

6 User Definable Features.....always reads 0

5 66MHz Capable.....always reads 1

4 Supports New Capability list.....always reads 1

3-0 Reserved .....always reads 0

Device 1 Offset 8 - Revision ID (0nh) ..... RO†

7-0 KM400A Chip Revision Code (00=First Silicon)

† May be write enabled by Rx44[7])

Device 1 Offset 9 - Programming Interface (00h) ..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier .....always reads 00

Device 1 Offset A - Sub Class Code (04h)..... RO

7-0 Sub Class Code reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code..reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer (00h) ..... RO

7-0 Reserved .....always reads 0

Device 1 Offset E - Header Type (01h) ..... RO

7-0 Header Type Code.....reads 01: PCI-PCI Bridge

Device 1 Offset F - Built In Self Test (BIST) (00h) ..... RO

7 BIST Supported.....reads 0: no supported functions

6 Start Test .....write 1 to start but writes ignored

5-4 Reserved .....always reads 0

3-0 Response Code..... 0 = test completed successfully

Device 1 Offset 18 - Primary Bus Number (00h).....RW

7-0 Primary Bus Number ..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h) .....RW

7-0 Secondary Bus Number..... default = 0

Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h) ....RW

7-0 Primary Bus Number ..... default = 0

Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1B – Secondary Latency Timer (00h) ....RO

7-0 Reserved ..... always reads 0

Device 1 Offset 1C - I/O Base (f0h).....RW

7-4 I/O Base AD[15:12]..... default = 1111b

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1D - I/O Limit (00h).....RW

7-4 I/O Limit AD[15:12] ..... default = 0

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1F-1E - Secondary Status (0000h).....RO

15-0 Rx44[4] = 0: No Function (always reads 0)
Rx44[4] = 1: Read same value as Rx7-6 (Pri Status)

Device 1 Offset 21-20 - Memory Base (fff0h).....RW

15-4 Memory Base AD[31:20].....default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) .....RW

15-4 Memory Limit AD[31:20] ..... default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 25-24 - Prefetchable Memory Base (fff0h) .....RW

15-4 Prefetchable Memory Base AD[31:20]default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit (0000h) .....RW

15-4 Prefetchable Memory Limit AD[31:20] .....
..... default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 2D-2C – Subsystem Vendor ID (0000h)R/W1

15-0 Subsystem Vendor ID .....default = 0

This register may be written once and is then read only.

Device 1 Offset 2F-2E – Subsystem ID (0000h)..... R/W1

15-0 Subsystem ID .....default = 0

This register may be written once and is then read only.

Device 1 Offset 34 – Capability Pointer ..... RO

7-0 Capability Pointer . (default) reads 80h if Rx44[5]=1
.....reads 00h if Rx44[5]=0

Device 1 Offset 3F-3E – PCI-to-PCI Bridge Control (0000h) ..... RW

15-4 Reserved .....always reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus ..... default

1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D)
..... default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved .....always reads 0

Device 1 Configuration Registers - PCI-to-PCI Bridge

AGP Bus Control

Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h) RW

7 CPU-AGP Post Write
- 0 Disable .....default
- 1 Enable

6 Reserved ..... always reads 0

5 CPU-AGP One Wait State Burst Write
- 0 Disable .....default
- 1 Enable

4-3 Read Prefetch Control
- 00 Always prefetch .....default
- x1 Never prefetch
- 10 Prefetch only for Enhance command

2 MDA Present on AGP
- 0 Forward MDA accesses to AGP .....default
- 1 Forward MDA accesses to PCI

Note: Forward despite IO / Memory Base / Limit

Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.

Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).

1 AGP Master Read Caching
- 0 Disable .....default
- 1 Enable

0 AGP Delay Transaction
- 0 Disable .....default
- 1 Enable

Table 9. VGA / MDA Memory / IO Redirection

3E[3] VGA Pres.	40[2] MDA Pres.	VGA is on	MDA is on	Axxxx, B8xxx Access	B0000 -B7FFF Access	3Cx, 3Dx I/O	3Bx I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (08h) RW

7 Retry Status
- 0 No retry occurred..... default
- 1 Retry Occurred .....**write 1 to clear**

6 Retry Timeout Action
- 0 No action taken except to record status ..... def
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Count
- 00 Retry 2, backoff CPU ..... default
- 01 Retry 4, backoff CPU
- 10 Retry 16, backoff CPU
- 11 Retry 64, backoff CPU

3 CPU-to-AGP Bursting Timeout
- 0 Disable
- 1 Enable**..... default**

2 Reserved .....always reads 0

1 CPU-to-PCI/AGP Cycles Invalidate PCI/AGP Buffered Read Data
- 0 Disable..... default
- 1 Enable

0 Reserved .....always reads 0

Device 1 Offset 42 - AGP Master Control (00h)..... RW

7 Read Prefetch for Enhance Command
- 0 Always Perform Prefetch..... default
- 1 Prefetch only if Enhance Command

6 AGP Master One Wait State Write
- 0 Disable..... default
- 1 Enable

5 AGP Master One Wait State Read
- 0 Disable..... default
- 1 Enable

4 Break Consecutive PCI Master Accesses
- 0 Disable..... default
- 1 Enable

3 Dynamic AGP Memory Read Ready Head / Tail Select
- 0 Use tail of ready to return data ..... default
- 1 Dynamically use head or tail

2 Claim I/O R/W and Memory Read Cycles
- 0 Disable..... default
- 1 Enable

1 Claim Local APIC FEEx xxxx Cycles
- 0 Disable..... default
- 1 Enable

0 Support CPU Cycles at 2T Rate
- 0 Disable..... default
- 1 Enable

Device 1 Offset 43 - AGP Master Latency Timer (22h) RW

7-4 Host to AGP Time Slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs .....default
- … …
- F 240 GCLKs

3-0 AGP Master Time Slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs.....default
- … …
- F 240 GCLKs

Device 1 Offset 44 – Backdoor Register Control (20h) .RW

7 Revision ID (Rx8) Write Enable
- 0 Disable (Rx8 RO) .....default
- 1 Enable (Rx8 RW)

6 Reserved ..... always reads 0

5 Power Management Capability Support
- 0 Rx34 reads 00h
- 1 Rx34 reads 80h **.....default**

4 Reflect Rx7-6 Status in Rx1F-1E
- 0 Disable (Rx1F-1E always reads 0).....default
- 1 Enable (Rx1F-1E reads same as Rx7-6)

3-2 Rx83[2-1] Back Door Value

1 Rx82[5] Back Door Value (Device Specific Intfc)

0 Back Door Register Enable for AGP Device ID (Rx47-46)
- 0 Disable .....default
- 1 Enable

Device 1 Offset 45 – Fast Write Control (72h) ..... RW

7 Force Fast Write Cycle to be QW Aligned (if Rx45[6] = 0)
- 0 Disable..... default
- 1 Enable

6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction
- 0 Disable
- 1 Enable**..... default**

5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable**..... default**

4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable**..... default**

3 Reserved .....always reads 0

2 Fast Write Burst 4T Max (No Slave Flow Control)
- 0 Disable..... default
- 1 Enable

1 Fast Write Fast Back to Back
- 0 Disable
- 1 Enable**..... default**

0 Fast Write Initial Block 1 Wait State
- 0 Disable..... default
- 1 Enable

Rx45 Bits 7-4	CPU Write Address in Mem1	CPU Write Address in Mem2	Fast Write Cycle Alignment
x1xx	-	-	QW aligned, burstable
0000	-	-	DW aligned, nonburstable
x010	0	0	n/a
0010	0	1	DW aligned, non-burstable
x010	1	-	QW aligned, burstable
x001	0	0	n/a
x001	-	1	QW aligned, burstable
0001	1	0	DW aligned, non-burstable
x011	0	0	n/a
x011	1	-	QW aligned, burstable
x011	0	1	QW aligned, burstable
1000	-	-	QW aligned, non-burstable
1010	0	1	QW aligned, non-burstable
1001	1	0	QW aligned, non-burstable

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID...RW

15-0 PCI-to-PCI Bridge Device ID ..... default = 0000

Device 1 Offset 48 – AGP Parity Error Control (00h)...RW

7-2 Reserved ..... always reads 0

1 Pass AGP Data Parity Error to V-Link if Rx4[6]=1 (Parity Error Response Enable)

0 Disable .....default

1 Enable

0 Pass AGP Address Parity Error to V-Link if Rx5-4[8]=1 (SERR# Enable)

0 Disable .....default

1 Enable

Device 1 Offset 80 – Capability ID (01h) ..... RO

7-0 Capability ID .....always reads 01h

Device 1 Offset 81 – Next Pointer (00h) ..... RO

7-0 Next Pointer: Null.....always reads 00h

Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h) .. RO

7-6 Power Mgmt Capabilities .....always reads 0

5 Power Mgmt Capabilities .programmed via Rx44[1]

4-0 Power Mgmt Capabilities .....always reads 02h

Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h) .. RO

7-3 Power Mgmt Capabilities .....always reads 0

2-1 Power Mgmt Capabilitiesprogrammed via Rx44[3-2]

0 Power Mgmt Capabilities .....always reads 0

Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h)..... RW

7-2 Reserved .....always reads 0

1-0 Power State

00 D0 ..... default

01 -reserved-

10 -reserved-

11 D3 Hot

Device 1 Offset 85 – Power Mgmt Status (00h)..... RO

7-0 Power Mgmt Status .....default = 00

Device 1 Offset 86 – P2P Br. Support Extensions (00h) . RO

7-0 P2P Bridge Support Extensions .....default = 00

Device 1 Offset 87 – Power Management Data (00h) ..... RO

7-0 Power Management Data .....default = 00

FUNCTIONAL DESCRIPTION - INTEGRATED GRAPHICS

Configuration Strapping

Certain KM400A graphics functions have options that must be selected and fixed at reset (before the register bits controlling these functions can be programmed by software). This is accomplished via power-on configuration strapping.

The strapping pins are pulled low internally and can be individually pulled high through 10 KOhm resistors. These pull-ups and pull-downs do not affect normal operation of the pins, but they do force the pins to a definite state during reset. At the rising edge of the reset signal, this state is sampled, the result is inverted and the data loaded into VGA Sequencer extended register index 12 (EXSR12). The data is used for system configuration. The definitions of the strapping bits at the rising edge of the reset signal are shown in Table 10. Non-graphics straps are described in the pin descriptions for the V-Link signals in the pin descriptions section.

Pin Name	Ball #	CR Bit(s) Value	Description
DP0D10	B7	–	**Reserved for test** (must be pulled down)
DP0D7	A8	–	**Reserved for test** (must be pulled down)
DP0D6	B8	EXSR12[6]	**Dedicated Display Port 0**
			1 = Enable
			0 = Disable
DP0D5	E8	EXSR12[5]	**Dedicated Display Port Configuration**
			1 = TV Encoder
			0 = TMDS
DP0D4	E9	EXSR12[4]	**Panel Port Configuration**
			1 = Single 24-bit
			0 = Dual 12-bit
DP0D3 DP0D2 DP0D1 DP0D0	A9 B9 C9 D9	EXSR12[3] EXSR12[2] EXSR12[1] EXSR12[0]	**OEM-Defined Panel Type**

Table 10. Definition of Strapping Bits at the Rising Edge of the Reset Signal

PCI Configuration and Integrated AGP

PCI Configuration

The KM400A graphics Vendor ID register (Index 00H) in the PCI Configuration space is hardwired to 5333H to specify S3 Graphics Incorporated as the vendor. The Device ID register is hardwired to 8D01H.

Bits 10-9 of the Status register (Index 06H) are hardwired to 01b to specify medium DEVSEL timing. The Class Code register (Index 08H) is hardwired to 30000xxH to specify that the KM400A is a VGA compatible device.

PCI06[4] is hardwired to 1 to indicate a capabilities list is available. PCI34[7-0] point to the PCI power management registers starting at offset DC. The basic power states (D0-D3) are supported as explained by the PCI Bus Power Management Interface Specification, Revision 1.1.

PCI Subsystem ID

The Subsystem ID and Subsystem Vendor ID are located in a 32-bit read only register at PCI Configuration Space Index 2C. These registers reflect the content of 4 read/write CR registers as follows:

Register	CR Space	PCI Config Space
Subsystem Vendor ID Low Byte	CR35	Index 2CH
Subsystem Vendor ID High Byte	CR36	Index 2DH
Subsystem ID Low Byte	CR37	Index 2EH
Subsystem ID High Byte	CR38	Index 2FH

Table 11. PCI Subsystem ID and Subsystem Vendor ID Registers

These registers allow identification of particular vendors using the same graphics chip. The following design allows the subsystem identification to be handled by software (no hardwiring).

All KM400A motherboard designs will incorporate the video BIOS into the system BIOS ROM. The system BIOS must load the subsystem ID information in the KM400A before any ID scanning takes place. To do this, it must turn on the KM400A, enable I/O accesses in the PCI configuration space, unlock the CR registers, program the subsystem ID information in the registers described above, then turn off the KM400A.

Display Memory

The KM400A North Bridge utilizes a Shared Memory Architecture (SMA) for Frame Buffer Memory. SMA allows system memory to be efficiently shared by the host CPU and the KM400A North Bridge graphics controller. By default, no system memory is allocated for the graphics frame buffer, but up to 32 Mbytes may be allocated depending on user preference, application requirements and the total size of system memory.

Note: Frame buffer memory is allocated from system memory at bootup time. Changing the display settings to a resolution requiring additional frame buffer memory will require a system reboot to be performed.

Frame Buffer Size	Dev 0 RxFB[6-4] Register Setting	CR36[7-5] † Register Setting
0 Mbytes	000	000
8 Mbytes	011	011
16 Mbytes	100	100
32 Mbytes	101	101

† For driver information only (not connected to hardware)

Table 12. Supported Frame Buffer Memory Configurations

Display Output

S3 Graphics endeavors to provide the maximum available noise-free mode support for any given device. Mode support is influenced by:

- Amount and speed of system memory
- Display resolution and color depth
- Maximum refresh capability detected for the display device
- Single or dual display engine usage

All the tables in this section are based on the use of DDR266 system memory.

Single CRT or Panel Display

Panel displays follow the 60 Hz refresh rate column.

Resolution	Bpp	CRT Maximum Refresh				
		60	75	85	100	120
640x480	8	√	√	√	√	√
	16	√	√	√	√	√
	32	√	√	√	√	√
800x600	8	√	√	√	√	√
	16	√	√	√	√	√
	32	√	√	√	√	
1024x768	8	√	√	√	√1	
	16	√	√	√1	√1	
	32	√	√	√1		
1152x864	8	√	√			
	16	√	√			
	32	√	√			
1280x1024	8	√	√	√		
	16	√	√	√		
	32	√	√	√2		
1440x1050	8	√	√	√		
	16	√	√	√1		
	32	√	√2	√3		
1600x1200	8	√	√	√		
	16	√	√1	√1		
	32	√2				

Table 13. Single CRT / Panel Display Resolutions

Legend:
√ = Mode and overlay available with either DDR200 or DDR266
1 = Overlay not available with DDR200
2 = Mode and overlay not available with DDR200
3 = Mode and overlay not available with DDR200, Overlay not available with DDR266

Multiple Displays – CRT + 640x480 (VGA) Panel

CRT Resolution	BPP	LCD 8BPP					LCD 16BPP					LCD 32BPP				
		CRT Maximum Refresh					CRT Maximum Refresh					CRT Maximum Refresh				
		60	75	85	100	120	60	75	85	100	120	60	75	85	100	120
640x480	8	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
800x600	8	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√1
	16	√	√	√	√	√	√	√	√	√	√1	√	√	√	√	√1
	32	√	√	√	√1		√	√	√	√1		√	√	√	√1	
1024x768	8	√	√	√	√1		√	√	√	√1		√	√	√1	√1	
	16	√	√	√1			√	√	√1			√	√	√1		
	32	√	√	√1			√	√	√1			√	√	√1		
1152x864	8	√	√				√	√				√	√			
	16	√	√				√	√				√	√1			
	32	√	√				√	√1				√	√1			
1280x1024	8	√	√1	√1			√	√1	√1			√	√1			
	16	√	√1	√1			√	√1	√1			√	√2			
	32	√	√1	√1			√	√				√2				
1400x1050	8	√	√1				√	√1				√2				
	16	√	√1				√2					√2				
	32	√2														
1600x1200	8	√2					√2									
	16	√2														
	32															

Table 14. Supported Resolutions – CRT + 640x480 (VGA) Panel

Legend:
√ = Mode and overlay available with either DDR200 or DDR266
1 = Overlay not available with DDR200
2 = Mode and overlay not available with DDR200
3 = Mode and overlay not available with DDR200, overlay not available with DDR266

Multiple Displays – CRT + 800x600 (SVGA) Panel

CRT Resolution	BPP	LCD 8BPP					LCD 16BPP					LCD 32BPP				
		CRT Maximum Refresh					CRT Maximum Refresh					CRT Maximum Refresh				
		60	75	85	100	120	60	75	85	100	120	60	75	85	100	120
640x480	8	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
800x600	8	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√1
	16	√	√	√	√	√	√	√	√	√	√1	√	√	√	√	√1
	32	√	√	√	√1		√	√	√	√1		√	√	√	√1	
1024x768	8	√	√	√	√1		√	√	√	√1		√	√	√1	√1	
	16	√	√	√1			√	√	√1			√	√	√1		
	32	√	√	√1			√	√	√1			√	√	√1		
1152x864	8	√	√				√	√				√	√			
	16	√	√				√	√				√	√1			
	32	√	√				√	√1				√	√1			
1280x1024	8	√	√1	√1			√	√1	√1			√				
	16	√	√1	√1			√	√1	√1			√2				
	32	√	√1	√1			√	√				√2				
1400x1050	8	√	√1				√	√1				√2				
	16	√	√1				√2									
	32	√2														
1600x1200	8	√2														
	16	√2														
	32															

Table 15. Supported Resolutions – CRT + 800x600 (SVGA) Panel

Legend:
√ = Mode and overlay available with either DDR200 or DDR266
1 = Overlay not available with DDR200
2 = Mode and overlay not available with DDR200
3 = Mode and overlay not available with DDR200, overlay not available with DDR266

Multiple Displays – CRT + 1024x768 (XGA) Panel

CRT Resolution	BPP	LCD 8BPP					LCD 16BPP					LCD 32BPP				
		CRT Maximum Refresh					CRT Maximum Refresh					CRT Maximum Refresh				
		60	75	85	100	120	60	75	85	100	120	60	75	85	100	120
640x480	8	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2
	16	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2
	32	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2
800x600	8	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2
	16	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2	√2
	32	√2	√2	√2	√2		√2	√2	√2	√2		√2	√2	√2	√2	
1024x768	8	√2	√2	√2	√2		√2	√2	√2	√2		√2	√2	√2	√2	
	16	√2	√2	√2			√2	√2	√2			√2	√2	√2		
	32	√2	√2	√2			√2	√2	√2			√2	√2	√2		
1152x864	8	√2	√2				√2	√2				√2	√2			
	16	√2	√2				√2	√2				√2	√2			
	32	√2	√2				√2	√2				√2	√2			
1280x1024	8	√2	√2	√2			√2	√2	√2			√2	√3			
	16	√2	√2	√2			√2	√2	√2			√2	√3			
	32	√2	√2				√2					√2				
1400x1050	8	√2	√2				√2					√2				
	16	√2					√2									
	32	√2														
1600x1200	8	√2														
	16	√2														
	32															

Table 16. Supported Resolutions – CRT + 1024x768 (XGA) Panel

Legend:
√ = Mode and overlay available with either DDR200 or DDR266
1 = Overlay not available with DDR200
2 = Mode and overlay not available with DDR200
3 = Mode and overlay not available with DDR200, overlay not available with DDR266

TV Display

Resolution	Bpp	VT1621 TV Encoder		VT1622 TV Encoder		CH7009/ CH7010		SAA7108/ SAA7109	
		NTSC	PAL	NTSC	PAL	NTSC	PAL	NTSC	PAL
40x25 Text	color	√	√	√	√	√	√	√	√
80x25 Text	color	√	√	√	√	√	√	√	√
320x200	8	√	√	√	√	√	√	√	√
640x480	4	√	√	√	√	√	√	√	√
	8	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√
800x600	8	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√
1024x768	8			√	√	√	√		
	16			√	√	√	√		
	32			√	√	√	√		

Table 17. Supported Resolutions – TV Display

Legend:
√ = Supported

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 18. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_C	Case operating temperature	0	85	°C	1
T_S	Storage temperature	–55	125	°C	1
V_{IN}	Input voltage	–0.5	V_{RAIL} + 10%	Volts	1, 2
V_{OUT}	Output voltage	–0.5	V_{RAIL} + 10%	Volts	1, 2

Note 1. Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Note 2. V_{RAIL} is defined as the V_{CC} level of the respective rail. The CPU interface is CPU dependent. Memory can be 1.5V or 3.3V. V-Link can be 2.5V only. Display can be 3.3V only. AGP can be 1.5V only.

DC Characteristics

T_C = 0-85°C, V_{RAIL} = V_{CC} ±5%, V_{CORE} = 2.5V ±5%, GND=0V

Table 19. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	–0.50	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	-	0.55	V	I_{OL} = 4.0mA
V_{OH}	Output High Voltage	2.4	–	V	I_{OH} = –1.0mA
I_{IL}	Input Leakage Current	–	±10	uA	$0 < V_{IN} < V_{CC}$
I_{OZ}	Tristate Leakage Current	–	±20	uA	$0.55 < V_{OUT} < V_{CC}$

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 20. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
5.0V Power	4.75	5.25	Volts
3.3V Power (I/O Pads, VCCQ for 2x transfer mode)	3.135	3.465	Volts
2.5V Power (Internal Logic)	2.375	2.625	Volts
1.5V Power (VCCQ for 8x/4x transfer mode)	1.425	1.575	Volts
Case Temperature	0	85	°C

Drive strength for selected output pins is programmable. See Rx6D for details.

MECHANICAL SPECIFICATIONS

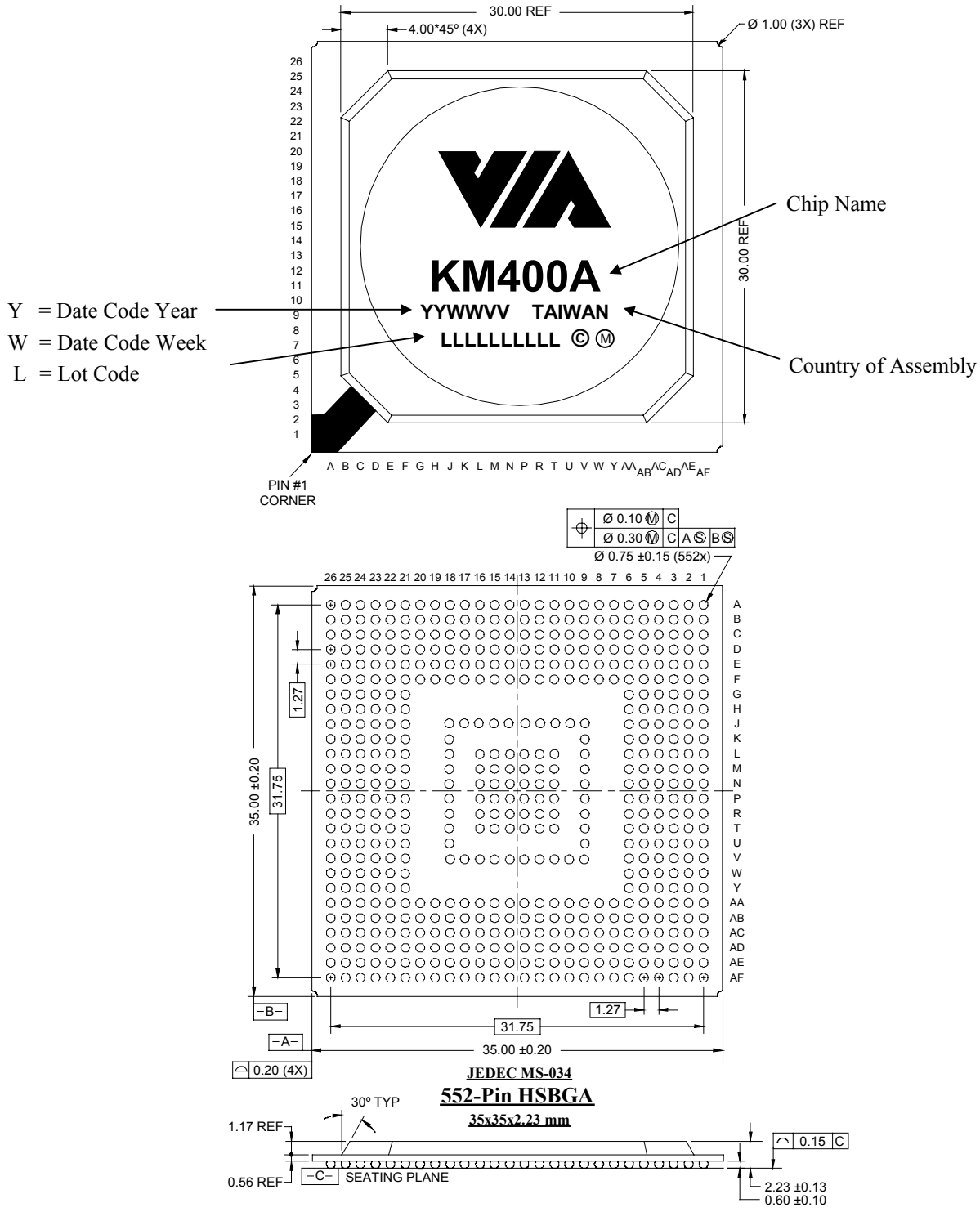


Figure 5. Mechanical Specifications - 552-Pin HSBGA Ball Grid Array Package with Heat Spreader