General Description

The DM9102A is a fully integrated and cost-effective single chip Fast Ethernet NIC controller. It is designed with the low power and high performance process. It is a 3.3V device with 5V tolerance then it supports 3.3V and 5V signaling.

The DM9102A provides direct interface to the PCI or the CardBus. It supports bus master capability and fully complies with PCI 2.2. In media side, The DM9102A interfaces to the UTP3,4,5 in 10Base-T and UTP5 in 100Base-TX. It is fully compliance with the IEEE 802.3u Spec. Its auto-negotiation function will automatically configure the DM9102A to take the maximum advantage of its abilities. The DM9102A is also support IEEE 802.3x full-duplex flow control.

The DM9102A supports two types of power-management mechanisms. The main mechanism is based upon the OnNow architecture, which is required for PC99. The alternative mechanism is based upon the remote Wake-On-LAN mechanism.

Block Diagram

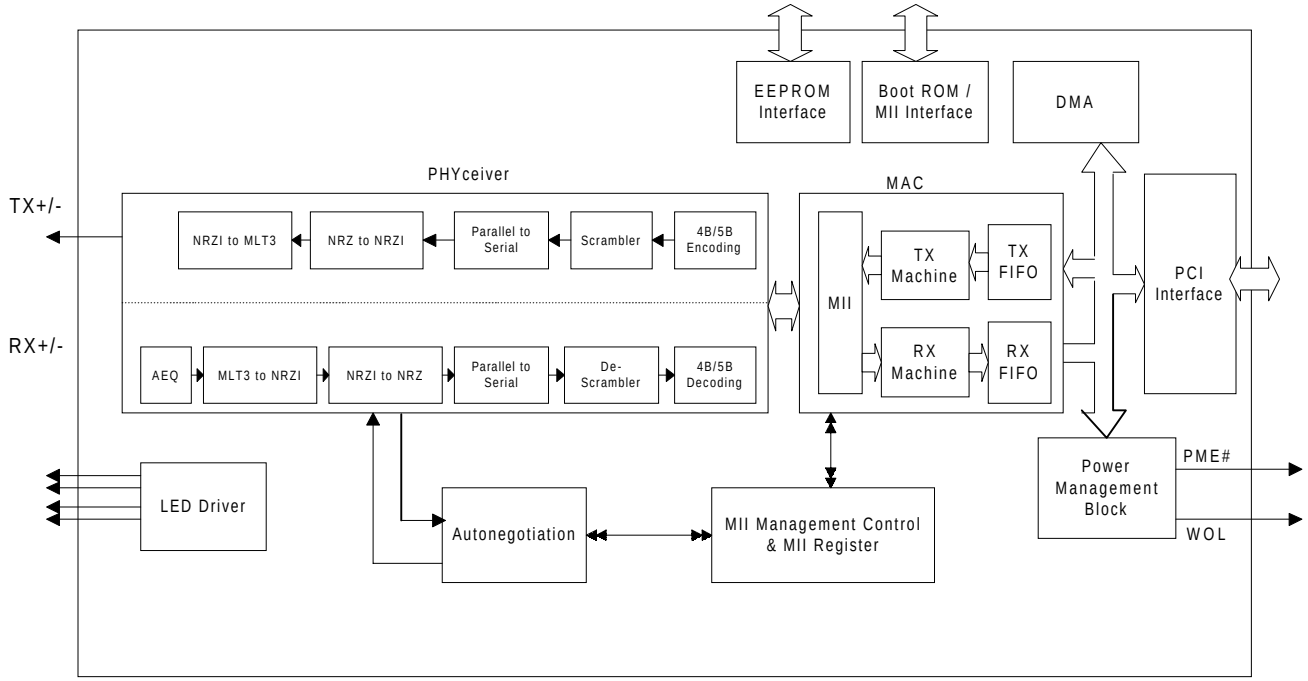
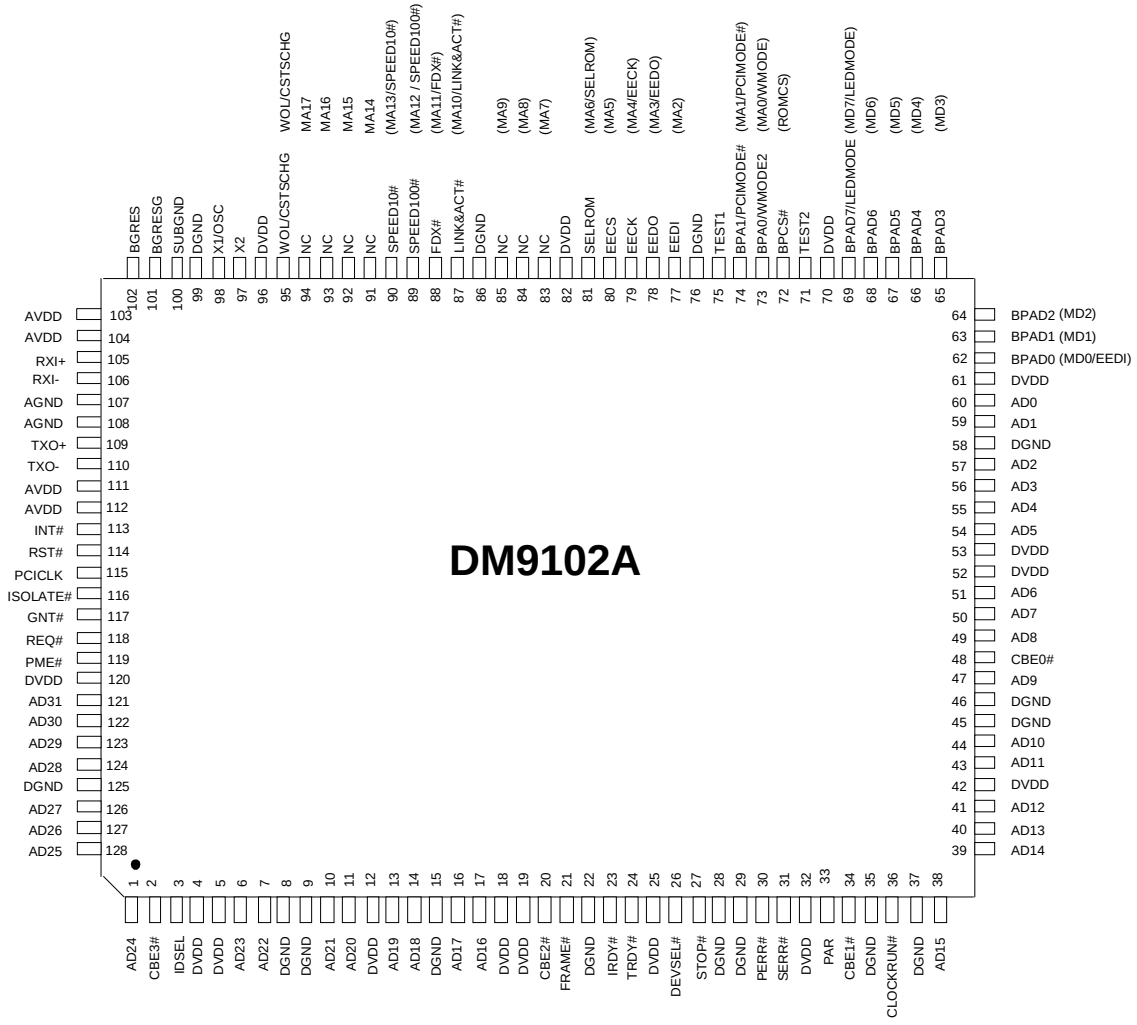


Table of Contents

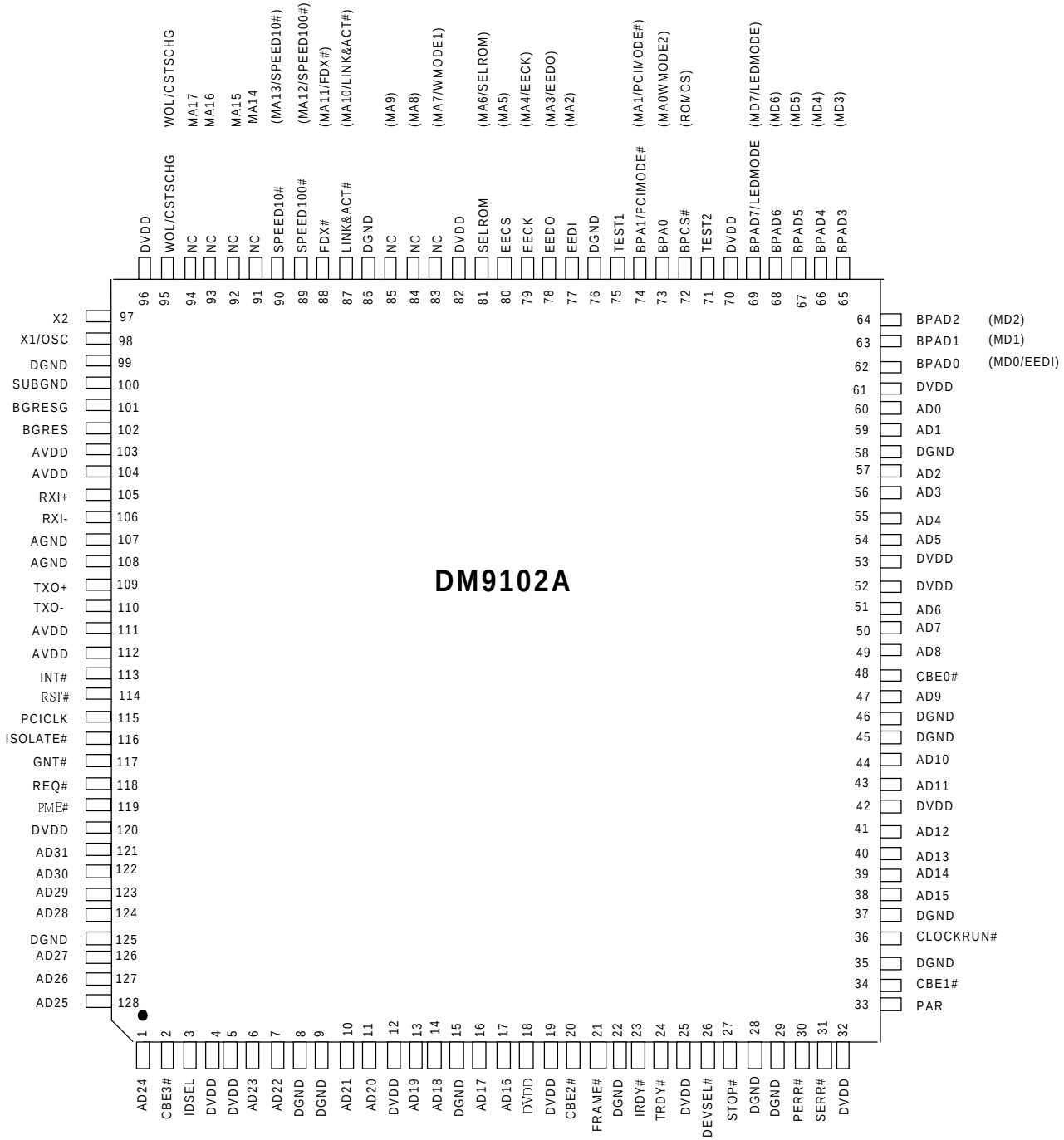
Features

- Integrated Fast Ethernet MAC, Physical Layer and transceiver in one chip.
- 128pin QFP/128pin TQFP with CMOS process.
- +3.3V Power supply with +5V tolerant I/O.
- Supports PCI and CardBus interfaces.
- Comply with PCI specification 2.2.
- PCI clock up to 40MHz.
- PCI bus master architecture.
- PCI bus burst mode data transfer.
- Two large independent FIFO; receive FIFO & transmit FIFO.
- Up to 256K bytes Boot EPROM or Flash interface.
- EEPROM 93C46 interface supports node ID accesses configuration information and user define message.
- Node address auto-load and reload.
- Comply with IEEE 802.3u 100Base-TX and 802.3 10Base-T.
- Comply with IEEE 802.3u auto-negotiation protocol for automatic link type selection.
- Full Duplex/Half Duplex capability.
- Support IEEE 802.3x Full Duplex Flow Control
- VLAN support.
- Comply with ACPI and PCI Bus Power Management.
- Supports the MII (Media Independent Interface).
- Supports Wake-On-LAN function and remote wake-up (Magic packet, Link Change and Microsoft® wake-up frame).
- Supports 4 Wake-On-LAN (WOL) signals (active high pulse, active low pulse, active high , active low).
- High performance 100Mbps clock generator and data recovery circuit.
- Digital clock recovery circuit using advanced digital algorithm to reduce jitter.
- Adaptive equalization circuit and Baseline wandering restoration circuit for 100Mbps receiver.
- Provides Loopback mode for easy system diagnostics.

Pin Configuration : 128 pin QFP



Pin Configuration : 128 pin TQFP



Pin Description

I = Input, O = Output, I/O = Input / Output, O/D = Open Drain, P = Power,
LI = reset Latch Input, # = asserted Low

PCI Bus and CardBus Interface Signals

Pin No. 128QFP/128TQFP	Pin Name	I/O	Description
113	INT#	O/D	Interrupt Request This signal will be asserted low when an interrupt condition as defined in CR5 is set, and the corresponding mask bit in CR7 is not set.
114	RST#	I	System Reset When this signal is asserted low, DM9102A performs the internal system reset to its initial state.
115	PCICLK	I	PCI system clock PCI bus clock that provides timing for DM9102A related to PCI bus transactions. The clock frequency range is up to 40MHz.
117	GNT#	I	Bus Grant This signal is asserted low to indicate that DM9102A has been granted ownership of the bus by the central arbiter.
118	REQ#	O	Bus Request The DM9102A will assert this signal low to request the ownership of the bus.
119	PME#	O/D	Power Management Event. Open drain. Active Low. The DM9102A drive it low to indicates that a power management event has occurred.
3	IDSEL	I	Initialization Device Select This signal is asserted high during the Configuration Space read/write access.
21	FRAME#	I/O	Cycle Frame This signal is driven low by the DM9102A master mode to indicate the beginning and duration of a bus transaction.
23	IRDY#	I/O	Initiator Ready This signal is driven low when the master is ready to complete the current data phase of the transaction. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted.
24	TRDY#	I/O	Target Ready This signal is driven low when the target is ready to complete the current data phase of the transaction. During a read, it indicates that valid data is asserted. During a write, it indicates the target is prepared to accept data.
26	DEVSEL#	I/O	Device Select The DM9102A asserts the signal low when it recognizes its target address after FRAME# is asserted. As a bus master, the DM9102A will sample this signal that insures its

			destination address of the data transfer is recognized by a target.
27	STOP#	I/O	Stop This signal is asserted low by the target device to request the master device to stop the current transaction.
30	PERR#	I/O	Parity Error The DM9102A as a master or slave will assert this signal low to indicate a parity error on any incoming data.
31	SERR#	I/O	System Error This signal is asserted low when address parity is detected with PCICS bit31 (detected parity error) Is enabled. The system error asserts two clock cycles after the falling address if an address parity error is detected.
33	PAR	I/O	Parity This signal indicates even parity across AD0~AD31 and C/BE0#~C/BE3# including the PAR pin. This signal is an output for the master and input for the slave device. It is stable and valid one clock after the address phase.
2 20 34 48	C/BE3# C/BE2# C/BE1# C/BE0#	I/O	Bus Command/Byte Enable During the address phase, these signals define the bus command or the type of bus transaction that will take place. During the data phase these pins indicate which byte lanes contain valid data. C/BE0# applies to bit7-0 and C/BE3# applies to bit31-24.
121,122,123,124,126,127, 128,1,6,7,10, 11,13,14,16, 17,38,39,40, 41,43,44,47, 49,50,51,54, 55,56,57,59, 60	AD31~AD0	I/O	Address & Data These are multiplexed address and data bus signals. As a bus master, the DM9102A will drive address during the first bus phase. During subsequent phases, the DM9102A will either read or write data expecting the target to increment its address pointer. As a target, the DM9102A will decode each address on the bus and respond if it is the target being addressed.

Boot ROM and EEPROM Interface (Including multiplex mode or direct mode)
Multiplex mode

Pin No. 128QFP/128TQFP	Pin Name	I/O	Description
62,63,64,65, 66,67,68,69	BPAD0~BPAD7 (BPAD7/LEDMODE)	I/O, LI	Boot ROM address and data bus (bits 0~7) Boot ROM address and data multiplexed lines bits 0~7. In MUX mode, there are two consecutive address cycles, these lines contain the boot ROM address pins 7~2, out_enable and write_enable of Boot ROM in the first cycle; and these lines contain address pins 15~8 in second cycle. After the first two cycles, these lines contain data bit 7~0 in consective cycles. BPAD1 is also a reset latch pin. It is Boot ROM address and data bus when normal operation. When at power on reset, it is used to pull up or down externally through a resister to select

			the WOL as pulse or DC signal. 0 = WOL pulse mode (default) 1 = WOL DC mode BPAD2 is also a reset latch pin. It is Boot ROM address and data bus when normal operation. When at power on reset, it is used to pull up or down externally through a resister to select the PME as pulse or DC signal. 0 = PME pulse mode (default) 1 = PME DC mode BPAD7 is also a reset latch pin. It is Boot ROM address and data bus when normal operation. When at power on reset, it is used to pull up or down externally through a resister to select LED mode. 0 = LED mode 0 (default) 1 = LED mode 1
72	BPCS#	O	Boot ROM Chip Select Boot ROM or external register chip select signal.
73	BPA0/WMODE	O, LI	Boot ROM address line/WOL mode selection This multiplexed pin acts as boot ROM address bit 0 output signal during normal operation. When at power on reset, it used to select the type of WOL signal. 0 = WOL high active (default) 1 = WOL low active
74	BPA1/PCIMODE#	I/O, LI	Boot ROM address line / PCI mode selection This multiplexed pin acts as the boot ROM address bit 1 output signal during normal operation. When RST# is active (low), it acts as the input system type. If the DM9102A is used in a CardBus system, this pin should be connected to a pull-up resistor; otherwise, the DM9102A consider the host as a PCI system. 0 = PCI mode (default) 1 = CardBus mode
77	EEDI	I	EEPROM Data In The DM9102A will read the contents of EEPROM serially through this pin.
78	EEDO	O	EEPROM Data Out The DM9102A will use this pin to serially write opcodes, addresses and data into the EEPROM.
79	EECK	O	EEPROM Serial Clock This pin provides the clock for the EEPROM data transfer.
80	EECS	O	EEPROM Chip Select This pin will enable the EEPROM during loading of the Configuration Data.
81	SELROM	I	Multiplex or Director mode selection 0 = Multiplex mode (default) 1 = Direct mode
83,84,85,91,92,93,94	NC	NC	In Multiplex mode, these pins are not connected.

Direct mode

Pin No. 128QFP/128TQFP	Pin Name	I/O	Description
62	MD0/EEDI	I	Boot ROM data input/EEPROM data in This is multiplexed pin used by EEDI and MD0. When boot ROM is selected, it acts as boot ROM data input. When ROMCS select the EEPROM, the DM9102A will read the contents of EEPROM serially through this pin.
63,64,65,66,67,68,69	MD1~MD7	I	Boot ROM data input bus MD1 is also a reset latch pin. It is Boot ROM address and data bus when normal operation. When at power on reset, it is used to pull up or down externally through a resister to select the WOL as pulse orlevel signal. 0 = WOL pulse mode (default) 1 = WOL level mode MD2 is also a reset latch pin. It is Boot ROM address and data bus when normal operation. When at power on reset, it is used to pull up or down externally through a resister to select the PME as pulse or level signal. 0 = PME pulse mode (default) 1 = PME level mode MD7 is also a reset latch pin. It is Boot ROM address and data bus when normal operation. When at power on reset, it is used to pull up or down externally through a resister to select LED mode. 0 = LED mode 0 (default) 1 = LED mode 1
72	ROMCS	O	Boot ROM or EEPROM chip selection.
73	MA0/WMODE	O	Boot ROM address output line/WOL mode selection This multiplexed pin acts as boot ROM address output bus during normal operation. When RST# is active, it is used to pull up or down externally through a resister to select WOL High active or LOW active. (WMODE) 0 = WOL high active (default) 1 = WOL low active
74	MA1/PCIMODE#	O, LI	Boot ROM address output signal/PCI mode selection This multiplexed pin acts as a boot ROM address output signal during normal operation. When RST# is active, it acts as the input system type. If the DM9102A is used in a CardBus system, this pin should be connected to a pull-up resistor; otherwise, the DM9102A consider the host as a PCI system. 0 = PCI mode (default) 1 = CardBus mode
77	MA2	O	Boot ROM address output signal
78	MA3/EEDO	O	Boot ROM address output/EEPROM data out This is multiplexed pin used by MA3 and EEDO.

			When The DM9102A will use this pin to serially write opcodes, addresses and data into the EEPROM.
79	MA4/EECK	O	Boot ROM address output/EEPROM serial clock This is multiplexed pin used by MA4 and EECK . This pin provides the clock for the EEPROM data transfer.
80	MA5	O	Boot ROM address output signal
81	MA6/SELROM	O/LI	Boot ROM address output/Multiplex or Direct mode selection This multiplexed pin acts as boot ROM address output bus during normal operation. When RST# is active, it is used as multiplex and direct mode selection : 0 = Boot ROM interface is in multiplex mode (default) 1 = Boot ROM interface is in direct mode.
83,84,85	MA7~MA9	O	Boot ROM address output bus
87	MA10/LINK&ACT#	O	Boot ROM address output signal/Link & Active LED In DIR mode, this pin represents the Boot ROM address bit 10 when at the time of boot ROM operation. When Boot ROM is not accessed, this pin acts as traffic-and- link led in LED MODE 0 or traffic led in LED MODE 1.
88	MA11/FDX#	O	Boot ROM address output/Full-duplex LED In DIR mode, this pin represents the Boot ROM address bit 11 when at the time of boot ROM operation. When Boot ROM is not accessed, this pin acts as full-duplex led.
89	MA12 / SPEED100#	O	Boot ROM address output/ 100Mbps LED In DIR mode, this pin represents the Boot ROM address bit 12 when at the time of boot ROM operation. When Boot ROM is not accessed, this pin acts as speed-100 led.
90	MA13/SPEED10#	O	Boot ROM address output signal/10Mbps LED In DIR mode, this pin represents the Boot ROM address bit 13 when at the time of boot ROM operation. When Boot ROM is not accessed, this pin acts as speed-10 led.
91,92,93, 94	MA14~MA17	O	Boot ROM address output bus

LED Pins (Please refer to p.11 "NOTE: LED Mode" for details.)

Pin No. 128QFP/128TQFP	Pin Name	I/O	Description
87	LINK&ACT# / ACT#	O	LED output pin, active low mode 0 = Link and traffic LED. Active low to indicate normal link, and it will flash as a traffic LED when transmitting or receiving. mode 1 = traffic LED only
88	FDX# / FDX#	O	LED output pin, active low mode 0 = Full duplex LED mode 1 = Full duplex LED
89	SPEED100# / SPEED100#	O	LED output pin, active low mode 0 = 100Mbps LED mode 1 = 100Mbps LED

90	SPEED10# / LINK#	O	LED output pin, active low mode 0 = 10Mbps LED mode 1 = Link LED

Network Interface

Pin No. 128QFP/128TQFP	Pin Name	I/O	Description
105,106	RXI+ RX-	I	100M/10Mbps differential input pair. These two pins are differential receive input pair for 100BASE-TX and 10BASE-T. They are capable of receiving 100BASE-TX MLT-3 or 10BASE-T Manchester encoded data.
109,110	TXO+ TXO-	O	100M/10Mbps differential output pair. These two pins are differential output pair for 100BASE-TX and 10BASE-T. This output pair provides controlled rise and fall times designed to filter the transmitter output.

Miscellaneous Pins

Pin No. 128QFP/128TQFP	Pin Name	I/O	Description
36	CLOCKRUN#	I/O, O/D	Clockrun# The clockrun# signal is used by the system to pause or slow down the PCI clock signal. It is used by the DM9102A to enable or disable suspension of the PCI clock signal or restart of the PCI clock. When the clockrun# signal is not used, this pin should connected to an external pull-down resistor.
71	TEST2	I	TEST mode control 2 In normal operation, this pin is pulled-high.
75	TEST1	I	TEST mode control 1 In normal operation, this pin is pulled low.
95	WOL/CSTSCHG	O	Wake up signal/Card Status Change This is multiplexed pin to provide Wake on LAN signal or Card Status Change. In a PCI system, it is used as a WOL signal. In a CardBus system, it is used as the Card Status Change output signal and is asynchronous to the clock signal. It indicates that a power management event has occurred in a CardBus system. The DM9102A can assert this pin if it detects link status change, or magic packet, or sample frame. The default is "normal low, active high pulse". DM9102A also support High/Low and Pulse/Level options.
97	X2	O	Crystal feedback output pin used for crystal connection only. Leave this pin open if oscillator is used.
98	X1/OSC	I	Crystal or Oscillator input. (25MHZ± 50ppm) 25MHz Oscillator or series-resonance, fundamental frequency crystal.
102	BGRES	I	Bandgap Voltage Reference Resistor.

			It connects to a 6200Ω, 1% error tolerance resistor between this pin and BGRESG pin to provide an accurate current reference for DM9102A..
101	BGRESG	I	For Bandgap circuit It is used together with the BGRESG pin.
116	ISOLATE#	I	Isolate This isolate signal is used to isolate the DM9102A from the system, and it is suitable for LAN on motherboard. When isolate signal is active low, it disables the DM9102A function and the DM9102A will not drive any outputs and sample inputs. In this case, the power consumption is minimum.

Power Pins

Pin No. 128QFP/128TQFP	Pin Name	I/O	Description
100,107, 108	AGND	P	Analog ground
103,104, 111,112	AVDD	P	Analog power, +3.3V
8,9,15,22,28,29,35,37,45, 46,58,76,86,99,125	DGND	P	Digital ground
4,5,12,18,19,25,32,42,52, 53,61,70,82,96,120	DVDD	P	Digital power, +3.3V

NOTE :
LED Mode

Pin No. 128QFP/128TQFP	MODE 0	MODE 1
87	LINK&ACT# Link and traffic LED	ACT# Traffic LED
88	FDX# Full-duplex LED	FDX# Full-duplex LED
89	SPEED100# 100Mbps LED	SPEED100# 100Mbps LED
90	SPEED10# 10Mbps LED	LINK# Link LED

Register Definition

PCI Configuration Registers

The definitions of PCI Configuration Registers are based on the PCI specification revision 2.2 and provides the initialization and configuration information to operate the PCI interface in the DM9102A. All registers can be accessed with byte, word, or double word mode. As defined in PCI specification 2.1, read accesses to reserve or unimplemented registers will return a value of "0." These registers are to be described in the following sections.

The default value of PCI configuration registers after reset.

Description	Identifier	Address Offset	Value of Reset
Identification	PCIID	00H	91021282H
Command & Status	PCICS	04H	02100007H
Revision	PCIRV	08H	02000031H
Miscellaneous	PCILT	0CH	BIOS determine
I/O Base Address	PCIIO	10H	System allocate
Memory Base Address	PCIMEM	14H	System allocate
Reserved	-------	18H - 28H	00000000H
CardBus ICS pointer	CIS	24H	00000000H
Subsystem Identification	PCISID	2CH	load from SROM
Expansion ROM Base Address	PCIROM	30H	00000000H
Capability Pointer	CAP_PTR	34H	00000050H
Reserved	-------	38H	00000000H
Interrupt & Latency	PCIINT	3CH	System allocate bit7~0
Device Specific Configuration Register	PCIUSR	40H	00000000H
Power Management Register	PCIPMR	50H	C0310001H
Power Management Control & Status	PMCSR	54H	00000100H

Key to Default

In the register description that follows, the default column takes the form <Reset Value>

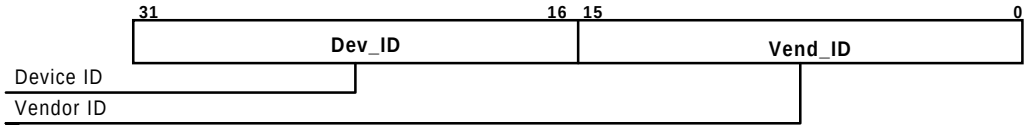
Where：

<Reset Value>:

1 Bit set to logic one
0 Bit set to logic zero
X No default value

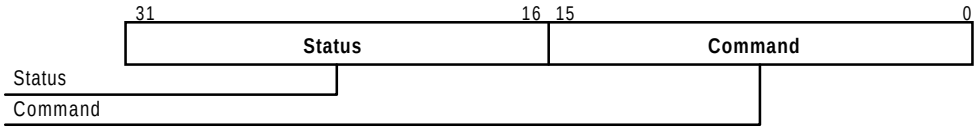
<Access Type>:
RO = Read only
RW = Read/Write
R/C: means Read / Write & Write "1" for Clear.

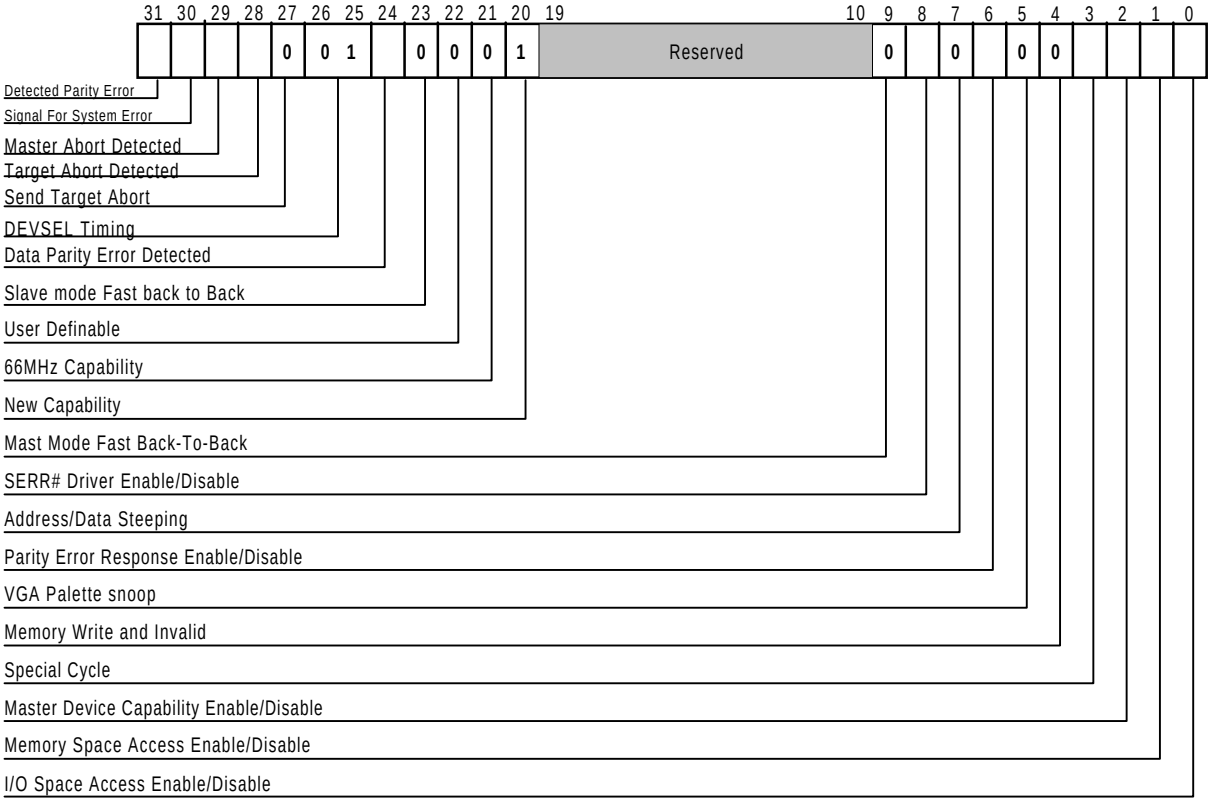
Identification ID (xxxxxx00 - PCIID)



Bit	Default	Type	Description
16:31	9102h	RO	The field identifies the particular device. Unique and fixed number for the DM9102A is 9102h. It is the product number assigned by DAVICOM.
0:15	1282h	RO	This field identifies the manufacturer of the device. Unique and fixed number for Davicom is 1282h. It is a registered number from SIG.

Command & Status (xxxxxx04 - PCICS)

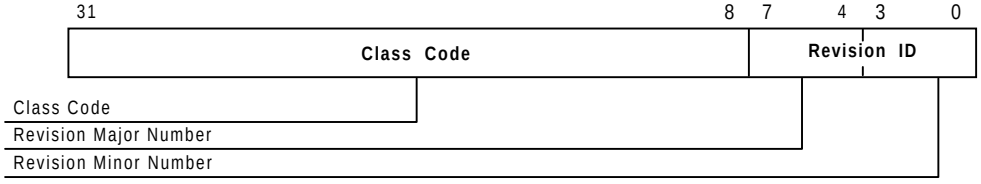




Bit	Default	Type	Description
31	0	R/C	Detected Parity Error The DM9102A samples the AD[0:31], C/BE[0:3]#, and the PAR signal to check parity and to set parity errors. In slave mode, the parity check falls on command phase and data valid phase (IRDY# and TRDY# both active). While in master mode, the DM9102A will check during each data phase of a memory read cycle for a parity error During a memory write cycle, if an error occurs, the PERR# signal will be driven by the target. This bit is set by the DM9102A and cleared by writing "1". There is no effect by writing "0".
30	0	R/C	Signal For System Error This bit is set when the SERR# signal is driven by the DM9102A. This system error occurs when an address parity is detected under the condition that bit 8 and bit 6 in command register below are set.
29	0	R/C	Master Abort Detected This bit is set when the DM9102A terminates a master cycle with the master-abort bus transaction.
28	0	R/C	Target Abort Detected This bit is set when the DM9102A terminates a master cycle due to a target-abort signal from other targets.
27	0	R/C	Send Target Abort (0 For No Implementation) The DM9102A will never assert the target-abort sequence.
26:25	01	R/C	DEVSEL Timing (01 Select Medium Timing) Medium timing of DEVSEL# means the DM9102A will assert DEVSEL# signal two clocks after FRAME# is sample “asserted.”
24	0	R/C	Data Parity Error Detected This bit will take effect only when operating as a master and when a Parity Error Response Bit in command configuration register is set. It is set under two conditions: (i) PERR# asserted by the DM9102A in memory data read error, (ii) PERR# sent from the target due to memory data write error.
23	0	RO	Slave mode Fast Back-To-Back Capable (0 For Not Support) This bit is always reads "1" to indicate that the DM9102A is capable of accepting fast back-to-back transaction as a slave mode device.
22	0	RO	User-Definable-Feature Supported (0 For Not Support)
21	0	RO	66 MHz Capable (0 For No Capability)
20	1	RO	New Capabilities (1 For Good Capability) This bit indicates whether this function implements a list of extended capabilities such as PCI power management. When set this bit indicates the presence of New Capabilities. A value of 0 means that this function does not implement New Capabilities.
19:10	0	RO	Reserved
9	0	RO	Master Mode Fast Back-To-Back (0 For Not Support) The DM9102A does not support master mode fast back-to-back capability and will not generate fast back-to-back cycles.
8	0	RW	SERR# Driver Enable/Disable This bit controls the assertion of SERR# signal output. The SERR# output will be asserted on detection of an address parity error and if both this bit

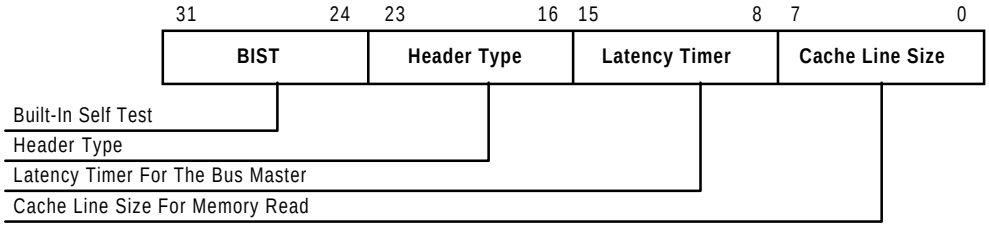
			and bit 6 are set.
7	0	RO	Address/Data Stepping (0 For No Stepping)
6	0	RW	Parity Error Response Enable/Disable Setting this bit will enable the DM9102A to assert PERR# on the detection of a data parity error and to assert SERR# for reporting address parity error.
5	0	RO	VGA Palette Snooping (0 For Not Support)
4	0	RO	Memory Write and Invalid (0 For Not Implementation) The DM9102A only generates Memory write cycle.
3	0	RO	Special Cycles (0 For Not Implementation)
2	1	RW	Master Device Capability Enable/Disable When this bit is set, DM9102A has the ability of master mode operation.
1	1	RW	Memory Space Access Enable/Disable This bit controls the ability of memory space access. The memory access includes memory mapped I/O access and Boot ROM access. As the system boots up, this bit will be enabled by BIOS for Boot ROM memory access. While in normal operation using memory mapped I/O access, this bit should be set by driver before memory access cycles.
0	1	RW	I/O Space Access Enable/Disable This bit controls the ability of I/O space access. It will be set by BIOS after power on.

Revision ID (xxxxxx08 - PCIRV)



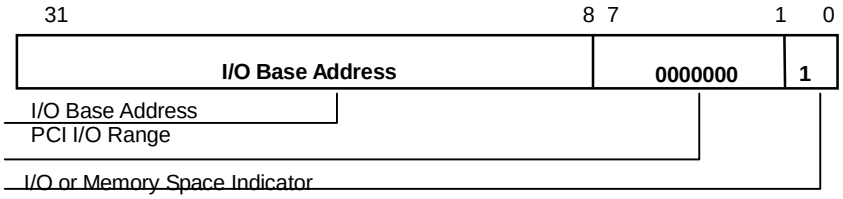
Bit	Default	Type	Description
31:8	020000h	RO	Class Code (020000h) This is the standard code for Ethernet LAN controller.
7:4	0011	RO	Revision Major Number This is the silicon-major revision number that will increase for the subsequent versions of the DM9102.A.
3:0	0001	RO	Revision Minor Number This is the silicon-minor revision number that will increase for the subsequent versions of the DM9102A.

Miscellaneous Function (xxxxxx0c - PCILT)



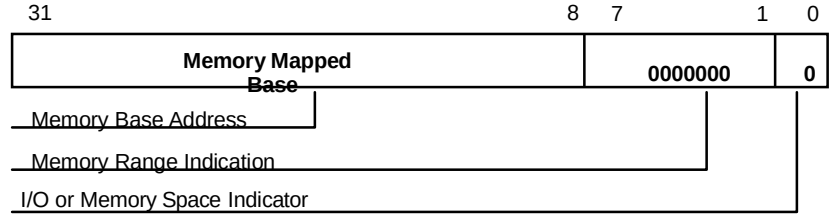
Bit	Default	Type	Description
31:24	00h	RO	Built In Self Test (00h Means Not Implementation)
23:16	00h	RO	Header Type (00h Means single function with Predefined Header Type)
15:8	00h	RW	Latency Timer For The Bus Master. The latency timer is guaranteed by the system and measured by clock cycles. When the FRAME# asserted at the beginning of a master period by the DM9102A, the value will be copied into a counter and start counting down. If the FRAME# is de-asserted prior to count expiration, this value is meaningless. When the count expires before GNT# is de-asserted, the master transaction will be terminated as soon as the GNT# is removed. While GNT# signal is removed and the counter is non-zero, the DM9102A will continue with its data transfers until the count expires. The system host will read MIN_GNT and MAX_LAT registers to determine the latency requirement for the device and then initialize the latency timer with an appropriate value. The reset value of Latency Timer is determined by BIOS.
7:0	00h	RO	Cache line Size For Memory Read Mode Selection (00h Means Not Implementation For Use)

I/O Base Address (xxxxxx10 - PCIIO)



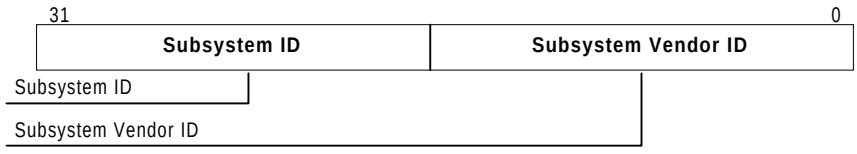
Bit	Default	Type	Description
31:7	Undefined	RW	PCI I/O Base Address This is the base address value for I/O accesses cycles. It will be compared to AD[31:7] in the address phase of bus command cycle for the I/O resource access.
6:1	000000	RO	PCI I/O Range Indication It indicates that the minimum I/O resource size is 80h.
0	1	RO	I/O Space Or Memory Space Base Indicator Determines that the register maps into the I/O space.(= 1 Indicates I/O Base)

Memory Mapped Base Address (xxxxxx14 - PCIMEM)



Bit	Default	Type	Description
31:7	Undefined	R/W	PCI Memory Base Address This is the base address value for Memory accesses cycles. It will be compared to the AD[31:7] in the address phase of bus command cycle for the Memory resource access.
6:1	000000	RO	PCI Memory Range Indication It indicates that the minimum Memory resource size is 80h.
0	0	RO	I/O Space Or Memory Space Base Indicator Determines that the register maps into the memory space(= 0 Indicates Memory Base)

Subsystem Identification (xxxxxx2c - PCISID)



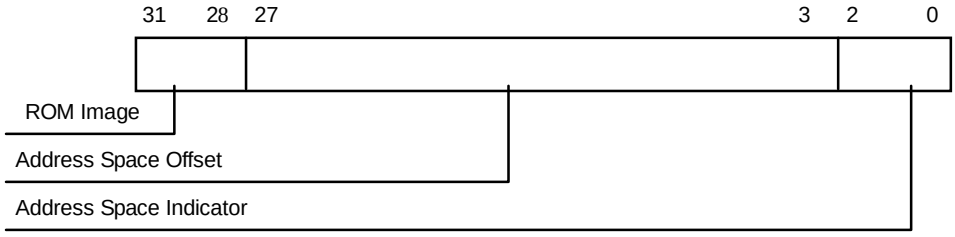
Bit	Default	Type	Description
31:16	XXXXh	RO	Subsystem ID It can be loaded from EEPROM word 1 and different from each card.
15:0	XXXXh	RO	Subsystem Vendor ID Unique number given by PCI SIG and loaded from EEPROM word 0.

CardBus CIS Pointer (xxxxxx28 - CCIS)

This Card Information Structure (CIS), also known as tuples, is a set of data structures saved in a nonvolatile memory on the CardBus Card. The data stored in CIS describes the product. Included in this data are the product manufacturer's name, product name, and most importantly, the hardware description. The CIS is supported in the boot ROM space or the memory space (serial ROM).

CIS is read upon card insertion into the socket. The software entity that traditionally reads the CIS is usually known as Card Services and Socket Services (CS & SS).

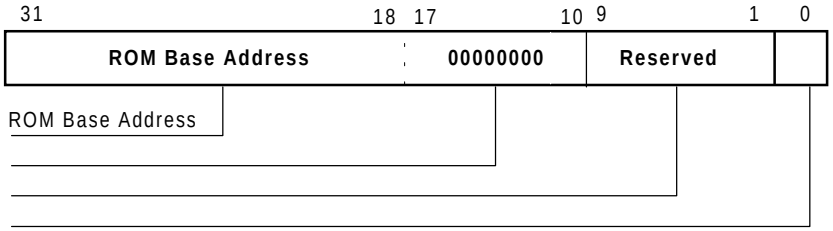
The CCIS pointer register is a read-only 32-bit register. This register points to one of the possible address space where the card information structure (CIS) begins. The pointer is used in a CardBus environment. The content of CCIS is loaded from the serial ROM after a hardware reset. A value of 0 in this register indicates that CIS is not supported.



Bit	Default	Type	Description
31:28	Note	R/W	ROM Image The 4-bit ROM image field value when the CIS reside in an expansion ROM.
27:3	Note	R/W	Address Space Offset This field contains the address offset within the address space indicated by the address space indicator field (CCIS<2:0>)
2:0	Note	R/W	Address Space Indicator This field indicates the location of the CIS base address. The value of 2 indicates that the CIS is stored in the serial ROM, and 7, indicates that the CIS is stored in the expansion ROM.

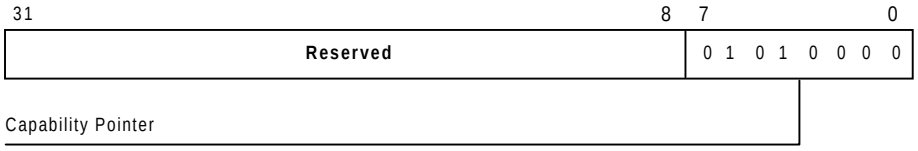
note : read from serial ROM

Expansion ROM Base Address (xxxxxx30 - PCIROM)



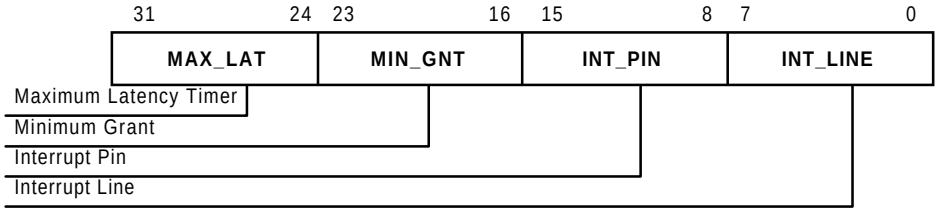
Bit	Default	Type	Description
31:10	00h	RW	ROM Base Address With 256K Boundary PCIROM bit17~10 are hardwired to 0, indicating ROM Size is up to 256K Size
9:1	000000000	RO	Reserved Bits Read As 0
0	0	RW	Expansion ROM Decoder Enable/Disable If this bit and the memory space access bit are both set to 1, the DM9102A will responds to its expansion ROM.

Capabilities Pointer (xxxxxx34 - Cap _Ptr)



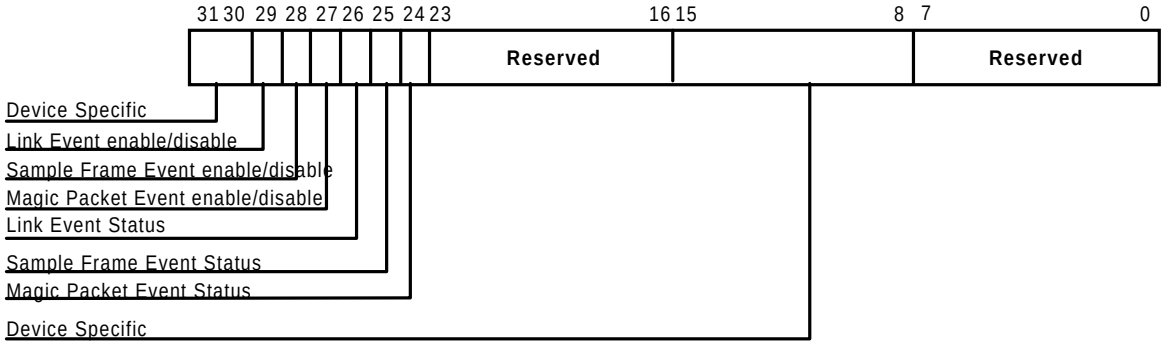
Bit	Default	Type	Description
31:8	000000h	RO	Reserved
7:0	01010000	RO	Capability Pointer The Cap_Ptr provides an offset (default is 50h) into the function's PCI Configuration Space for the location of the first term in the Capabilities Linked List. The Cap_Ptr offset is DOUBLE WORD aligned so the two least significant bits are always "0"s

Interrupt & Latency Configuration (xxxxxx3c - PCIINT)



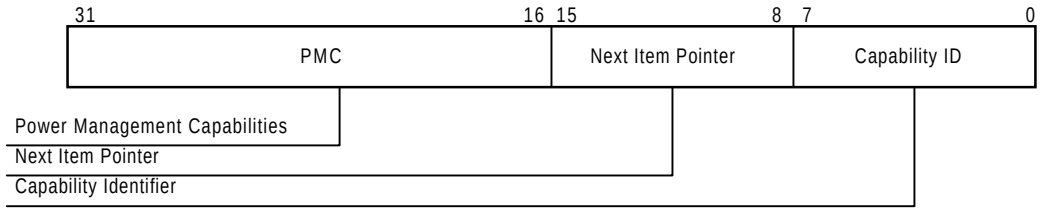
Bit	Default	Type	Description
31:24	28h	RO	Maximum Latency Timer that can be sustained (Read Only and Read As 28h)
23:16	14h	RO	Minimum Grant Minimum Length of a Burst Period (Read Only and Read As 14h)
15:8	01h	RO	Interrupt Pin read as 01h to indicate INTA#
7:0	XXh	RW	Interrupt Line that Is Routed to the Interrupt Controller The value depends on mainboard.

Device Specific Configuration Register (xxxxxx40h- PCIUSR)



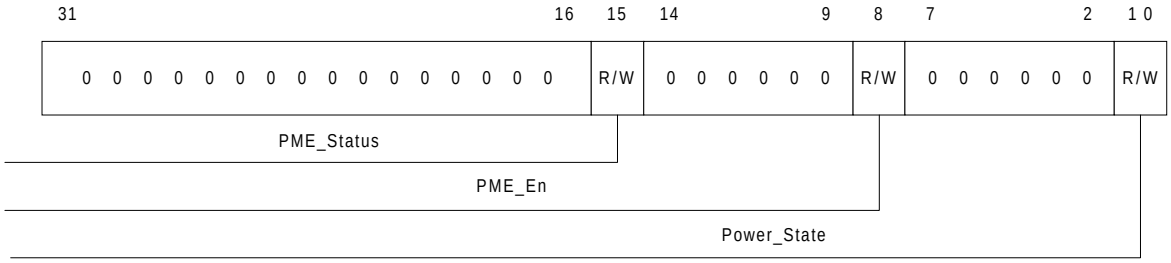
Bit	Default	Type	Description
31	0	RW	Device Specific Bit (sleep mode)
30	0	RW	Device Specific Bit (snooze mode)
29	0	RW	When set enable Link Status Change Wake-up Event
28	0	RW	When set enable Sample Frame Wake-up Event
27	0	RW	When set enable Magic Packet Wake-up Event
26	0	RO	When set, indicates link change and Link Status Change Event occurred
25	0	RO	When set, indicates the sample frame is received and Sample Frame Event occurred
24	0	RO	When set, indicates the Magic Packet is received and Magic packet Event occurred
23:16	00h	RO	Reserved Bits Read As 0
15:8	00h	RW	Device Specific
7:0	00h	RO	Reserved Bits Read As 0

Power Management Register (xxxxxx50h~PCIPMR)



Bit	Default	Type	Description
31:27	11000	RO	PME_Support These five bits field indicate the power states in which the function may assert PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit27 → PME# support D0 bit28 → PME# support D1 bit29 → PME# support D2 bit30 → PME# support D3(hot) bit31 → PME# support D3(cold) DM9102A's bit31~27=11000 indicates PME# can be asserted fromD3(hot) & D3(cold).
26:22	00000	RO	Reserved (DM9102A not supports D1, D2)
21	1	RO	A "1" indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.
20	1	RO	Auxiliary Power Source This bit is only meaningful if bit31 is a "1". This bit is "1" in DM9102A indicates that support for PME# in D3(cold) requires auxiliary power.
19	0	RO	PME# Clock "0" indicates that no PCI clock is required for the function to generate PME#.
18:16	001	RO	Version A value of 001 indicates that this function complies with the Revision 1.0 of the PCI Power Management Interface Specification. A value of 010 is for DM9102A/A that complies with the revision 1.1 of the PCI Power Management Interface Specification.
15:8	00h	RO	Next Item Pointer The offset into the function's PCI Configuration Space pointing to the location of next item in the function's capability list is "00h"
7:0	01h	RO	Capability Identifier When "01h" indicates the linked list item as being the PCI Power Management Registers.

Power Management Control/Status (xxxxxx54h~PMCSR)



Bit	Default	Type	Description
31:16	0000h	RO	Reserved
15	0	RW/C	PME_Status This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit. Writing a "1" to this bit will clear it. This bit defaults to "0" if the function does not support PME# generation from D3(cold).If the function supports PME# from D3(cold) then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.
14:9	000000	RO	Reserved. It means that the DM9102A does not support reporting power consumption.
8	1	RW	PME_En Write "1" to enables the function to assert PME#, write "0" to disable PME# assertion. This bit defaults to "0" if the function does not support PME# generation from D3(cold). If the function supports PME# from D3(cold) then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.
7:2	000000	RO	Reserved
1:0	00	RW	This two bits field is both used to determine the current power state of a function and to set the function into a new power state. The definitions given below. 00 : D0 11 : D3(hot)

Control and Status Registers (CR)

The DM9102A implements 16 control and status registers, which can be accessed by the host. These CRs are double long word aligned. All CRs are set to their default values by hardware or software reset unless otherwise specified. All Control and Status Registers with their definitions and offset from IO or memory Base Address are shown below:

Register	Description	Offset from CSR Base Address	Default value after reset
CR0	System Control Register	00H	FEC00000
CR1	Transmit Descriptor Poll Demand	08H	FFFFFFFF
CR2	Receive Descriptor Poll Demand	10H	FFFFFFFF
CR3	Receive Descriptor Base Address Register	18H	00000000
CR4	Transmit Descriptor Base Address Register	20H	00000000
CR5	Network Status Report Register	28H	FC000000
CR6	Network Operation Mode Register	30H	02040000
CR7	Interrupt Mask Register	38H	FFFE0000
CR8	Statistical Counter Register	40H	00000000
CR9	External Management Access Register	48H	044097FF
CR10	Programming ROM Address Register	50H	Unpredictable
CR11	General Purpose Timer Register	58H	FFFE0000
CR12	PHY Status Register	60H	FFFFFFXX
CR13	Sample Frame Access Register	68H	XXXXXX00
CR14	Sample Frame Data Register	70H	Unpredictable
CR15	Watchdog And Jabber Timer Register	78H	00000000H

Key to Default

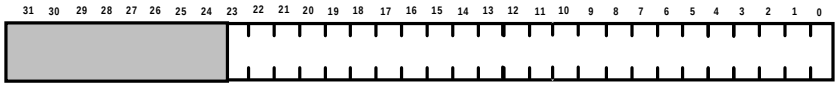
In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type>
Where：
<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value

<Access Type>:
RO = Read only
RW = Read/Write
RW/C = Read/Write and Clear
WO = Write only

Reserved bits are shaded and should be written with 0.
Reserved bits are undefined on read access.

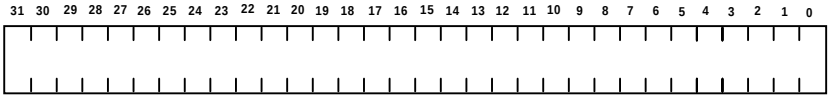
1. System Control Register (CR0)



Bit	Name	Default	Description
24:22	Reserved	0,RO	Reserved
21	MRM	0,RW	Memory Read Multiple When set, the DM9102A will use memory read multiple command (C/BE3~0 = 1100) when it initialize the memory read burst transaction as a master device. When reset, it will use memory read command (C/BE3 ~ 0 = 0110) for the same master operation.
20	Reserved	0,RO	Reserved
19:17	TXAP	000,RW	Transmit Automatic polling interval time When set, the DM9102A will poll transmit descriptor automatically when it is in the suspend state due to buffer unavailable. The polling interval time is programmable based on the table shown below. Bit 19 / Bit 18 / Bit 17 / Time Interval 0 / 0 / 0 / No polling 0 / 0 / 1 / 200us 0 / 1 / 0 / 800us 0 / 1 / 1 / 1.6ms 1 / 0 / 0 / 12.8us 1 / 0 / 1 / 25.6us 1 / 1 / 0 / 51.2us 1 / 1 / 1 / 102.4us
16	Reserved	0,RO	Reserved
15:14	ABA	00,RW	Address Boundary Alignment When set, the DM9102A will execute each burst cycles to stop at the programmed address boundary. The address boundary can be programmed to be 8, 16, or 32 doubleword as shown below. Bit 15 / Bit 14 / Alignment Boundary 0 / 0 / Reserved 0 / 1 / 8-double word 1 / 0 / 16-double word 1 / 1 / 32-double word
13:8	BL	000000, RW	Burst Length When reset, the DM9102A's burst length in one DMA transfer is limited by the amount of data in the receive FIFO (when receive) or the amount of free space in the transmit FIFO (when transmit). When set, the DMA's burst length is limited by the programmed value. The permissible values are 0, 1, 2, 4, 8, 16, or 32 doublewords.
7	Reserved	0,RO	Reserved
6:2	Reserved	00000	
1	Reserved	0,RO	Reserved

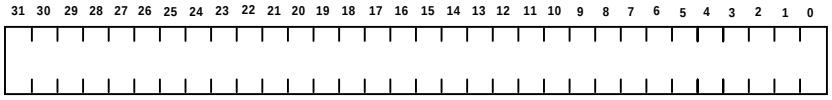
Bit	Name	Default	Description
0	SR	0,RW	Software Reset When set, the DM9102A will make a internal reset cycle. All consequent action to DM9102A2 should wait at least 32 PCI clock cycles to start and no necessary to reset this bit.

2. Transmit Descriptor Poll Demand (CR1)



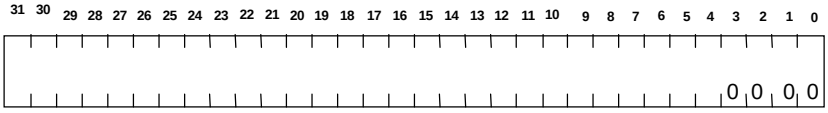
Bit	Name	Default	Description
31:0	TDP	FFFFFFFFh ,WO	Transmit Descriptor Polling Command Writing any value to this port will force DM9102A to poll the transmit descriptor. If the acting descriptor is not available, transmit process will return to suspend state. If the descriptor shows buffer available, transmit process will begin the data transfer.

3. Receive Descriptor Poll Demand (CR2)



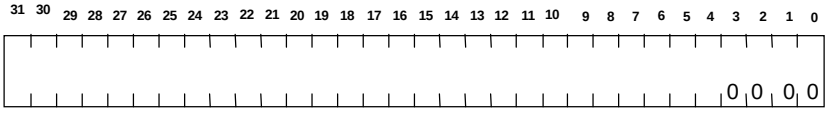
Bit	Name	Default	Description
31:0	RDP	FFFFFFFFh ,WO	Receive Descriptor Polling Command Writing any value to this port will force DM9102A to poll the receive descriptor. If the acting descriptor is not available, receive process will return to suspend state. If the descriptor shows buffer available, receive process will begin the data transfer.

4. Receive Descriptor Base Address (CR3)



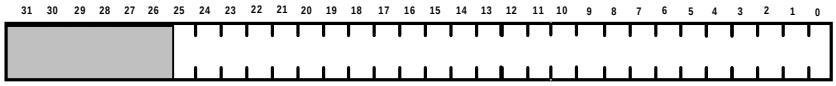
Bit	Name	Default	Description
31:0	RDBA	00000000h ,RW	Receive Descriptor Base Address This register defines base address of receive descriptor-chain. The receive descriptor- polling command after CR3 is set will make DM9102A to fetch the descriptor at the Base-Address.

5. Transmit Descriptor Base Address (CR4)



Bit	Name	Default	Description
31:0	TDBA	00000000h, RW	Transmit Descriptor Base Address This register defines base address of transmit descriptor-chain. The transmit descriptor- polling command after CR4 is set will make DM9102A to fetch the descriptor at the Base-Address.

6. Network Status Report Register (CR5)

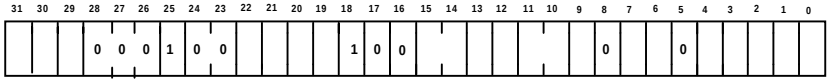


Bit	Name	Default	Description
25:23	SBEB	000,RO	System Bus Error Bits These bits are read only and used to indicate the type of system bus fetal error. Valid only when System Bus Error is set. The mapping bits are shown below. Bit25 Bit24 Bit23 Bus Error Type 0 0 0 Parity error 0 0 1 Master abort 0 1 0 Slave abort 0 1 1 Reserved 1 X X Reserved
22:20	TXPS	000,RO	Transmit Process State These bits are read only and used to indicate the state of transmit process. The mapping table is shown below. Bit22 Bit21 Bit20 Process State 0 0 0 Transmit process stopped 0 0 1 Fetch transmit descriptor 0 1 0 Move Setup Frame from the host memory 0 1 1 Move data from host memory to transmit FIFO 1 0 0 Close descriptor by clearing owner bit of descriptor 1 0 1 Waiting end of transmit 1 1 0 Transmit end and Close descriptor by writing status 1 1 1 Transmit process suspend
19:17	RXPS	000,RO	Receive Process State These bits are read only and used to indicate the state of receive process. The mapping table is shown below. Bit19 Bit18 Bit17 Process State 0 0 0 Receive process stopped 0 0 1 Fetch receive descriptor 0 1 0 Waiting for receive packet under buffer available 0 1 1 Move data from receive FIFO to host memory

			1 0 0 Close descriptor by clearing owner bit of descriptor 1 0 1 Close descriptor by writing status 1 1 0 Receive process suspended due to buffer unavailable 1 1 1 Purge the current frame from the receive FIFO because of unavailable receive buffer
16	NIS	0,RW	Normal Interrupt Summary Normal interrupt includes any of the three conditions : CR5<0> – TXCI : Transmit Complete Interrupt CR5<2> – TXDU : Transmit Buffer Unavailable CR5<6> – RXCI : Receive Complete Interrupt
15	AIS	0,RW	Abnormal Interrupt Summary Abnormal interrupt includes any interrupt condition as shown below excluding Normal Interrupt conditions. They are TXPS(bit1), TXJT(bit3), TXFU(bit5), RXDU(bit7), RXPS(bit8), RXWT(bit9), TXER(bit10), GPT(bit11), SBE(bit13).
14	ERI	0,RW	Early Receive Interrupt This bit will be set when early receive interrupt has happened.
13	SBE	0,RW	System Bus Error The PCI system bus errors will set this bit. The type of system bus error is shown in CR5<25:23>.
12	LCI	0,RW	Link Status Change Interrupt This bit will be set when link status change.
11	GPT	0,RW	General-purpose Timer Expired This bit is set to indicate the general-purpose timer (described in CR11) has expired.
10	TXER	0,RW	Transmit Early Interrupt Transmit Early Interrupt is set when the full packet data has been moved from host memory into transmit FIFO. It will inform the host to process next step before the transmission end. Transmit complete event CR5<0> will clear this bit automatically.
9	RXWT	0,RW	Receive Watchdog Timer Expired This bit is set to indicate receive watchdog timer has expired.
8	RXPS	0,RW	Receive Process Stopped This bit is set to indicate receive process enters the stopped state.
7	RXDU	0,RW	Receive Buffer Unavailable This bit is set when the DM9102A fetches the next receive descriptor that is still owned by the host. Receive process will be suspended until a new frame enters or the receive polling command is set.
6	RXCI	0,RW	Receive Complete Interrupt This bit is set when a received frame is fully moved into host memory and receive status has been written to descriptor. Receive process is still running and continues to fetch next descriptor.
5	TXFU	0,RW	Transmit FIFO Underrun This bit is set when transmit FIFO has underrun condition during the packet transmission. It may happen due to the heavy load on bus, receive process dominates in full-duplex operation, or transmit buffer unavailable before end of packet. In this case, transmit process is placed in the suspend state and underrun error TDES0<1> is set.
3	TXJT	0,RW	Transmit Jabber Timer Expired This bit is set when the jabber timer expired with the transmitter is still active. Transmit process will be aborted and placed in the stop state. It also causes transmit jabber timeout TDES0<14> to assert.
2	TXDU	0,RW	Transmit Buffer Unavailable

			This bit is set when the DM9102A fetches the next transmit descriptor that is still owned by the host. Transmit process will be suspended until the transmit polling command is set or auto-polling timer time-out.
1	TXPS	0,RW	Transmit Process Stopped This bit is set to indicate transmit process enters the stopped state.
0	TXCI	0,RW	Transmit Complete Interrupt This bit is set when a frame is fully transmitted and transmit status has been written to descriptor (the TDES1<31> is also asserted). Transmit process is still running and continues to fetch next descriptor.

7. Network Operation Mode Register (CR6)

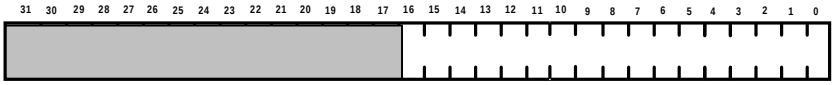


Bit	Name	Default	Description
30	RXA	0,RW	Receive All When set, all incoming packet will be received, regardless the destination address. The address match is checked according to theCR6<7>, CR6<6>, CR6<4>, CR6<2>, CR6<0>, and RDES0<30> will show this match.
29	NPFIFO	0,RW	Set to not purge RX FIFO if RX buffer unavailable
28:26	Reserved	000,RO	Must be Zero
25	Reserved	1,RO	Must be One
24:23	Reserved	00,RO	Must be Zero
22	TXTM	1,RW	Transmit Threshold Mode When set, the transmit threshold mode is 10Mb/s. When reset, the threshold mode is 100Mb/s. This bit is used together with CR6<15:14> to decide the exact threshold level.
21	SFT	0,RW	Store and Forward Transmit When set, the packet transmission from MAC will be started after a full frame has been moved from the host memory to transmit FIFO. When reset, the packet transmission's start will depend on the threshold value specified in CR6<15:14>
20	STI	0,RW	Start Transmission Immediately When this bit is set, the packet transmission from MAC will be started immediately after transmit FIFO's threshold level reaches 16 bytes, regardless of the setting in CR6<22> and CR6<15:14>. This mode will make transmit FIFO underrun condition to happen more easily.
19	Reserved	0,RO	Reserved
18	External MII_Mode	1,RW	1: Select external MII interface. 0: Select external SRL interface. In external MII mode that the pins TEST1, TEST2, and CLOCKRUN# are forced to low, the DM9102A bypasses internal PHY and uses external PHY, by setting this bit properly. See page 66 for details.
17	Reserved	0,RO	Reserved
16	1pkt	0,RW	One Packet Mode When this bit is set, only one packet is stored at TX FIFO.

15:14	TSB	0,RW	Threshold Bits These bits are set together with CR6<22> (chose 10Mb or 100Mb) and will decide the exact FIFO threshold level. The packet transmission will start after the data level exceeds the threshold value. Bit15 Bit14 Threshold(100M) Threshold(10M) 0 0 128 72 0 1 256 96 1 0 512 128 1 1 Reserved Reserved
13	TXSC	0,RW	Transmit Start/stop Command When set, transmit process will begin by fetching the transmit descriptor for available packet data to be transmitted (running state). If the fetched descriptor is owned by the host, transmit process will enter the suspend state and transmit buffer unavailable (CR5<2>) is set. Otherwise it will begin to move data from host to FIFO and transmit out after reaching threshold level. When reset, transmit process is placed in the stopped state after completing the transmission of the current frame.
12	FCM	0,RW	Force Collision Mode When set, the transmission process is forced to be the collision status. Meaningful only in the internal loopback mode.
11:10	LBM	0,RW	Loopback Mode These bits decide two loopback modes besides normal operation. External loopback mode expects transmitted data back to receive path and makes no collision detection. Bit11 Bit10 Loopback Mode 0 0 normal 0 1 internal loopback 1 0 internal PHY digital loopback 1 1 internal PHY analog loopback
9	FDM	0,RW	Full-duplex Mode This bit is set to make DM9102A operate in the full-duplex mode. Transmit and receive processes can work simultaneously. There is no collision detection needed during this mode operation.
8	Reserved	0,RO	Must be zero.
7	PAM	0,RW	Pass All Multicast When set, any packet with a multicast destination address is received by the DM9102A. The packet with a physical address will also be filtered based on the filter mode setting.
6	PM	1,RW	Promiscuous mode When set, any incoming valid frame is received by the DM9102A, and no matter what the destination address. The DM9102A is initialized to this mode after reset operation.
5	Reserved	0,RO	Must be Zero.
4	IAFM	0,RO	Inverse Address Filtering Mode It is set to indicate the DM9102A operate in a Inverse Filtering Mode. This is a read only bit and mapped from the setup frame together with CR6<2>, CR6<0> setting. That is, it is valid only during perfect filtering mode.

3	PBF	0,RW	Pass Bad Frame When set, the DM9102 is indicated to receive the bad frames including runt packets, truncated frames caused by the FIFO overflow. The bad frame also has to pass the address filtering if the DM9102A is not set in promiscuous mode.
2	HOFM	0,RO	Hash-only Filter Mode This is a read-only bit and mapped from the set-up frame together with bit4,0 of CR6. It is set to indicate the DM9102A operate in a Hash-only Filtering Mode.
1	RXRC	0,RW	Receive Start/Stop Command When set, receive process will begin by fetching the receive descriptor for available buffer to store the new-coming packet (placed in the running state). If the fetched descriptor is owned by the host (no descriptor is owned by the DM9102A), the receive process will enter the suspend state and receive buffer unavailable CR5<7> sets. Otherwise it runs to wait for the packet's income. When reset, receive process is placed in the stopped state after completing the reception of the current frame.
0	HPFM	0,RO	Hash/Perfect Filter Mode This is a read only bit and mapped from the setup frame together with CR6<4>, CR6<2>. When reset, the DM9102A does a perfect address filter of incoming frames according to the addresses specified in the setup frame. When set, the DM9102A does a imperfect address filtering for the incoming frame with a multicast address according to the hash table specified in the setup frame. The filtering mode (perfect / imperfect) for the frame with a physical address will depend on CR6<2>.

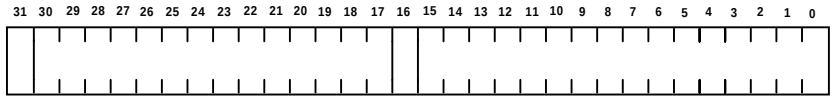
8. Interrupt Mask Register (CR7)



Bit	Name	Default	Description
16	NISE	0,RW	Normal Interrupt Summary Enable This bit is set to enable the interrupt for Normal Interrupt Summary. Normal interrupt includes three conditions : CR5<0> – TXCI : Transmit Complete Interrupt CR5<2> – TXDU : Transmit Buffer Unavailable CR5<6> – RXCI : Receive Complete Interrupt
15	AISE	0,RW	Abnormal Interrupt Summary Enable This bit is set to enable the interrupt for Abnormal Interrupt Summary. Abnormal interrupt includes all interrupt condition as shown below excluding Normal Interrupt conditions. They are TXPS(bit1), TXJT(bit3), TXFU(bit5), RXDU(bit7), RXPS(bit8), RXWT(bit9), TXER(bit10), GPT(bit11), SBE(bit13).
14	ERIE	0,RW	Early Receive Interrupt Enable This bit is set to enable the interrupt for Early Receive.
13	SBEE	0,RW	System Bus Error Enable When set together with CR7<15>, CR5<13>, it enables the interrupt for System Bus Error. The type of system bus error is shown in CR5<24:23>.
12	LCIE	0,RW	Link Status Change Interrupt Enable This bit is set to enable the interrupt for link status change.

11	GPTE	0,RW	General-purpose Timer Expired Enable This bit is set together with CR7<15>, CR5<11> then it will enable the interrupt for the condition of the general-purpose timer (described in CR11) expired.
10	TXERE	0,RW	Transmit Early Interrupt Enable This bit is set together with CR7<16>, CR5<10> then it enables the interrupt of the early transmit event.
9	RXWTE	0,RW	Receive Watchdog Timer Expired Enable When this bit and CR7<15>, (CR5<9> are set together, it enable the interrupt of the condition of the receive watchdog timer expired.
8	RXPSE	0,RW	Receive Process Stopped Enable When set together with CR7<15> and CR5<8>. This bit is set to enable the interrupt of receive process stopped condition.
7	RXDUE	0,RW	Receive Buffer Unavailable Enable When this bit and CR7<15>, CR5<7> are set together, it will enable the interrupt of receive buffer unavailable condition.
6	RXCIE	0,RW	Receive Complete Interrupt Enable When this bit and CR7<16>, CR5<6> are set together, it will enable the interrupt of receive process complete condition.
5	TXFUE	0,RW	Transmit FIFO Underrun Enable When set together with CR7<15>, CR5<5>, it will enable the interrupt of transmit FIFO underrun condition.
4	Reserved	0,RO	Reserved
3	TXJTE	0,RW	Transmit Jabber Timer Expired Enable When this bit and CR7<15>, CR5<3> are set together, it enables the interrupt of transmit Jabber Timer Expired condition.
2	TXDUE	0,RW	Transmit Buffer Unavailable Enable When this bit and CR7<16>, CR5<2> are set together, transmit buffer unavailable interrupt is enabled.
1	TXPSE	0,RW	Transmit Process Stopped Enable When this bit is set together with CR7<15> and CR5<1>, it will enable the interrupt of the transmit process stopped
0	TXCIE	0,RW	Transmit Complete Interrupt Enable When this bit and CR7<16>, CR5<0> are set, the transmit interrupt is enabled.

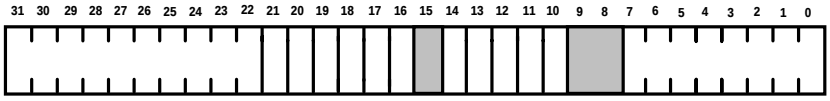
9. Statistical Counter Register (CR8)



Bit	Name	Default	Description
31	RXFU	0,RO	Receive Overflow Counter Overflow This bit is set when the Purged Packet Counter (RXDU) has an overflow condition. It is a read only register bit.
30:17	RXDU	0,RO	Receive Purged Packet Counter This is a statistic counter to indicate the purged received packet count upon FIFO overflow.

16	RXPS	0,RO	Receive Missed Counter Overflow This bit is set when the Receive Missed Frame Counter (RXCI) has an overflow condition. It is a read only register bit.
15:0	RXCI	0,RO	Receive Missed Frame Counter This is a statistic counter to indicate the Receive Missed Frame Count when there is a host buffer unavailable condition for receive process.

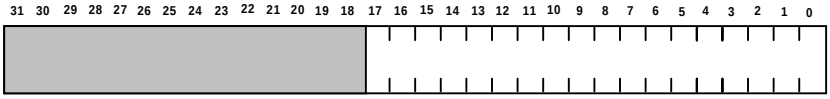
10. PROM & Management Access Register (CR9)



Bit	Name	Default	Description
31:22	Undefined	X,RO	Undefined
21	LES	0,RO	Load EEPROM status It is set to indicate the load of EEPROM is finished.
20	RLM	0,RW	Reload EEPROM It is set to reload the content of EEPROM.
19	MDIN	0,RO	MII Management Data_In This is read only bit to indicate the MDIO input data.
18	MRW	0,RW	MII Management Read/Write Mode Selection This bit defines the Read/Write Mode for MII management interface for PHY access.
17	MDOUT	0,RW	MII Management Data_Out This bit is used to generate the output data signal for the MDIO pin.
16	MDCLK	0,RW	MII Management Clock This bit is used to generate the output clock signal for the MDC pin.
15	MBO	1,RO	Must be One.
14	MRC	0,RW	Memory Read Control This bit is set to perform the read operation for the Boot PROM or EEPROM access.
13	EWC	0,RW	Memory Write Control This bit is set to perform the write operation for the Boot PROM (Multiplex mode) or EEPROM access.
12	BRS	1,RW	Boot ROM Selected This bit is set to select the Boot ROM access for memory interface.
11	ERS	0,RW	EEPROM Selected This bit is set to select the EEPROM access for memory interface.
10	XRS	1,RW	External Register Selected This bit is set to select an external register.
9:8	MBO	1,RO	Must be One
7:0	DATA	1,RW	Data input/output of Boot ROM This field contains the data which reads from or write to the Boot ROM when the Boot ROM mode is selected. (CR9<12> = 1) If EEPROM is selected (CR9<11> = 1), then CR9<3:0> are connected the serial ROM control pins.

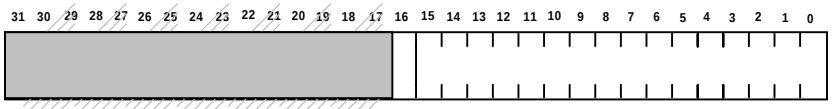
3	CRDOUT	1,RW	Data_Out from EEPROM This bit is set to reflect the signal status of EEDI pin when EEPROM mode is selected.
2	CRDIN	1,RW	Data_In to EEPROM This bit is set to generate the output signal to EEDO pin when EEPROM mode is selected.
1	CRCLK	1,RW	Clock to EEPROM This bit is set to generate the output clock to EECLK pin when EEPROM mode is selected.
0	CRCS	1,RW	Chip_Select to EEPROM This bit is set to generate the output signal to EECS pin when EEPROM mode is selected.

11. Programming ROM Address Register (CR10)



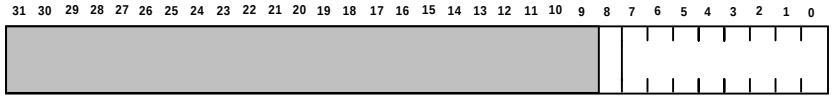
Bit	Name	Default	Description
17:0	BADR	Unpredictable	Boot ROM Address This field contains the address pointer for Boot ROM when the mode of programming by register is selected.

12. General Purpose Timer Register (CR11)



Bit	Name	Default	Description
16	TCON	0,RW	Continuous Mode of Timer When this bit is set, the timer will continuously re-initiated upon the set time is up. When reset, the timer will be one-shot response after BCLK value is programmed.
15:0	MBCLK	0000h,RW	Multiple of Base Clock This field set the iteration number of base clock. The base clock duration is defined to be 81.92us --- for MII port/100M is selected 2us --- for MII port/10M is selected

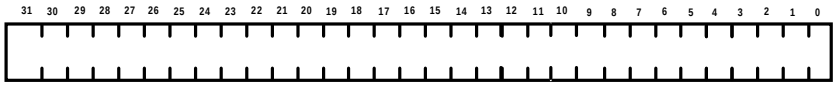
13. PHY Status Register (CR12)



Bit	Name	Default	Description

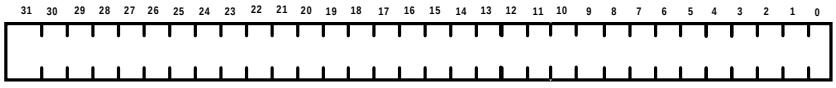
8	GEPC	X,RW	GEPD Bits Control When in initialization, this bit is set and the unique "80h" must be written to the GEPD(7:0). After initialization, this bit is reset and it controls the functional mode of GEPD in bit0~7.
7	GEPD(7)	X,RW	General PHY Reset Control It must be set to "1" if CR12<8> is set. When CR12<8> is reset, write "1" to this bit will reset the PHY of the DM9102A.
6:0	GEPD(6:0)	XXXXXXX ,RW	General PHY Status When CR12<8> is set at initialization, it operates the only write operation and write the unique "0000000" to these seven bits. After initialization, CR12<8> is reset, write operation is meaningless and read these seven bits to indicate the PHY status. These status bits are shown below. bit 6:Current Media Link Status bit 5:Signal Detection bit 4:RX-lock bit 3:Internal PHY Link status (the same as bit2 of PHY Register) bit 2:Full-duplex bit 1:Speed 100Mbps link bit 0:Speed 10Mbps link

14. Sample Frame Access Register (CR13) (reference to Power Management section)

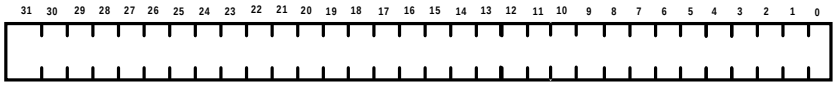


register	general definition	bit8 ~ 3	R/W
TxFIFO	transmit FIFO access port	32h	R/W
RxFIFO	receive FIFO access port	35h	R/W
DiagReset	general reset for diagnostic pointer port	38h	W

15. Sample Frame Data Register (CR14) (reference to Power Management section)



16. Watchdog and Jabber Timer Register (CR15)



Bit	Name	Default	Description
31:25	Reserved	0,RO	Reserved

24:22	ERIT	000,RW	Early Receive Interrupt Threshold These three bits determine the threshold of the received packet data from RX FIFO to host memory. bit24 bit 23 bit22 threshold (percentage) 0 0 0 Disable 0 0 1 12.5% 0 1 0 25.0% 0 1 1 37.5% 1 0 0 50.0% 1 0 1 62.5% 1 1 0 75.0% 1 1 1 87.5%
21:16	FIFOT	000000 ,RW	RX FIFO flow control threshold option The value of bit21~16 determine the threshold of RX FIFO overflow when in flow control mode. The exact threshold is 32bytes multiplied by this value.
15	TXPM	0,RW	Transmit pause packet condition control 1 = Indicate Transmit pause packet either CR15<11> or CR15<12> is set. 0 = Indicate Transmit pause packet both CR15<11> and CR15<12> are set.
14	TXP0	0,RW	Transmit pause packet Set to Transmit pause packet with pause timer = 0000h
13	TXPF	0,RW	Transmit pause packet Set to Transmit pause packet with pause timer = FFFFh, this bit will be cleared if packet had transmitted.
12	TXPE1	0,RW	Transmit pause packet enable Set to enable Transmit pause packet if descriptor unavailable
11	TXPE2	0.RW	Transmit pause packet enable Set to enable Transmit pause packet with time = FFFFh if FIFO near overflow, or with time = 0000h if FIFO empty.
10	FLCE	0,RW	Flow Control Enable Set to enable the decode of the pause packet.
9	RXPS	0,R/C	The latched status of the decode of the pause packet.
8	Reserved	0,RO	Reserved.
7	RXPCS	0,RO	Of the decode of the pause packet.
6	VLAN	0,RW	VLAN Capability Enable It is set to enable the VLAN mode.
5	TWDR	0,RW	Time Interval of Watchdog Release This bit is used to select the time interval between receive Watchdog timer expiration until re-enabling of the receive channel. When this bit is set, the time interval is 40~48 bits time. When this bit is reset, it is 16~24 bits time.
4	TWDE	0,RW	Watchdog Timer Disable When set, the Watchdog Timer is disabled. Otherwise it is enabled.
3	Reserved	0,RO	Reserved

2	JC	0,RW	Jabber Clock When set, the transmission is cut off after a range of 2048 bytes to 2560 bytes is transmitted. When resets, transmission for the 10Mbps port is cut off after a range of 26ms to 33ms. When resets, transmission for the 100Mbps port is cut off after a range of 2.6ms to 3.3ms.
1	TUNJ	0,RW	Transmit Unjabber Interval This bit is used to select the time interval between transmit jabber timer expiration until re-enabling of the transmit channel. When set, transmit channel is released right after the jabber expiration. When reset, the time interval is 365~420ms for 10Mb/s port and 36.5~42.0ms for 100Mb/s.
0	TJE	0,RW	Transmit Jabber Disable When set, the transmit Jabber Timer is disabled. Otherwise it is enabled.

CardBus Status Changed Registers

The DM9102A implements four status changed registers. These status changed registers are accessed by the CardBus systom software. These registers are mapped only to the memory address space and not to the I/O address space.

1. Function Event Register: (offset 80h)

Bit	Name	Default	Description
0:3	Reserved	R/W	Unpredictable on read
4	General Wake-up Event	R/WC	This bit is set when the DM9102A has detected a power management event. This bit is cleared upon power-up reset and by write 1. It is unaffected by either hardware or software reset. When the PME_Status bit in the PCI configuration is cleared, this bit is automatically cleared as well.
5:14	Reserved	R/W	Unpredictable on read
15	Interrupt	R/WC	This bit is set when there is an interrupt pending. This bit is cleared by write 1. This bit is cleared upon hardware or software reset.
16:31	Reserved	R/W	Unpredictable on read

2. Function Event Mask Register: (offset 84h)

Bit	Name	Default	Description
0:3	Reserved	R/W	Unpredictable on read
4	General Wake-up Event Enable	R/WC	When set together with the Wake-up Event Summary Enable bit (Function Event Mask Register<14>), enables the assertion of the CSTSCHG pin. To disable the assertion of the CSTSCHG, the PME_Enable bit in the PCI configuration register (PMC<8>) must be cleared as well. This bit is cleared upon power up reset.
5:13	Reserved	R/W	Unpredictable on read
14	Wake-up Event Summary Enable	R/W	When set together with the General Wake-up Event Enable bit (Function Event Mask Register<4>), enables the assertion of the CSTSCHG pin. To disable the assertion of the CSTSCHG pin, the PME_Enable bit in the PCI configuration register (PMC<8>) must be cleared as well. This is cleared upon power up reset.
15	Interrupt Register Enable	R/W	When set, enable the assertion of the interrupt pin (INT#). This bit is cleared upon hardware or software reset.
16:31	Reserved	R/W	Unpredictable on read

3. Function Present State Register: (offset 88h)

Bit	Name	Default	Description
0:3	Reserved	R/W	Unpredictable on read

4	General Wake-up Event	R	This bit reflects the current state of the wake-up event. It is cleared when either the General Wake-up Event in the Function Event Register is cleared or when the PME_Status in the PMC is cleared. This bit is cleared upon hardware or software reset.
5:14	Reserved	R/W	Unpredictable on read
15	Interrupt	R	This bit reflects the internal state of a function specific interrupt. It is cleared when the event that caused the interrupt was either masked in CSR7, or cleared in CSR5. This bit is cleared upon hardware or software reset.
16:31	Reserved	R/W	Unpredictable on read

4. Function Force Event Register: (offset 8Ch)

Bit	Name	Default	Description
0:3	Reserved	R/W	Unpredictable on read
4	Force Wake-up	W	Writing 1 to this bit sets the wake-up event field in the Function Event Register (Function Event Register<4>), but not in the Function Present State Register (Function Present State Register<4>). Writing 0 has no effect.
5:14	Reserved	R/W	Unpredictable on read
15	Force Interrupt	W	Writing 1 to this bit sets the interrupt field in the Function Event Register (Function Event Register<15>), but not in the Function Present State Register (Function Present State Register<15>). Writing 0 has no effect.
16:31	Reserved	R/W	Unpredictable on read

PHY Management Registers

Offset	Register Name	Description	Default value after reset
0	BMCR	Basic Mode Control Register	3100h
1	BMSR	Basic Mode Status Register	7809h
2	PHYIDR1	PHY Identifier Register #1	0181h
3	PHYIDR2	PHY Identifier Register #2	B840h
4	ANAR	Auto-Negotiation Advertisement Register	01E1h
5	ANLPAR	Auto-Negotiation Link Partner Ability Register	0000h
6	ANER	Auto-Negotiation Expansion Register	0000h
7-15	Reserved	Reserved	0000h
10h	DSCR	DAVICOM Specified Configuration Register	0000h
11h	DSCSR	DAVICOM Specified Configuration/Status Register	F010h
12h	10BTCSR	10BASE-T Configuration/Status Register	7800h
Others	Reserved	Reserved for future use, do not Read/Write to these Registers	0000h

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type> / <Attribute(s)>
Where：
<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value
(PIN#)	Value latched in from pin # at reset

<Access Type>:
RO = Read only
RW = Read/Write

<Attribute (s)>:
SC = Self clearing
P = Value permanently set
LL = Latching low
LH = Latching high

Basic Mode Control Register (BMCR) – 0

Bit	Name	Default	Description
0.15	Reset	0, RW/SC	Reset: 1=Software reset 0=Normal operation This bit sets the status and controls the PHY registers of the DM9102A to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed
0.14	Loopback	0, RW	Loopback: 1=Loop-back enabled 0=Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appear at the MII receive outputs
0.13	Speed Selection	1, RW	Speed Select: 1=100Mbps 0=10Mbps Link speed may be selected either by this bit or by Auto-negotiation. When Auto-negotiation is enabled and bit 12 is set, this bit will return Auto-negotiation selected media type.
0.12	Auto-negotiation Enable	1, RW	Auto-negotiation Enable: 1= Auto-negotiation enabled: bit 8 and 13 will be in Auto-negotiation status 0= Auto-negotiation disabled: bit 8 and 13 will determine the link speed and mode
0.11	Power Down	0, RW	Power Down: Setting this bit willpower down the whole chip except crystal / oscillator circuit. 1=Power Down 0=Normal Operation
0.10	Isolate	0,RW	Isolate: 1= Isolates the DM9102A from the MII with the exception of the serial management. 0= Normal Operation
0.9	Restart Auto-negotiation	0,RW/SC	Restart Auto-negotiation: 1= Restart Auto-negotiation. Re-initiates the Auto-negotiation process. When Auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning a value of 1 until Auto-negotiation is initiated by the DM9102A. The operation of the Auto-negotiation process will not be affected by the management entity that clears this bit. 0= Normal Operation
0.8	Duplex Mode	1,RW	Duplex Mode: 1= Full Duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With Auto-negotiation enabled, this bit reflects the duplex capability selected by Auto-negotiation. 0= Normal operation
0.7	Collision Test	0,RW	Collision Test: 1= Collision Test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN.

			0= Normal Operation
0.6:0.0	Reserved	<0000000>, RO	Reserved. Write as 0, ignore on read

Basic Mode Status Register (BMSR) – 1

Bit	Name	Default	Description
1.15	100BASE-T4	0,RO/P	100BASE-T4 Capable: 1=DM9102A is able to perform in 100BASE-T4 mode 0=DM9102A is not able to perform in 100BASE-T4 mode
1.14	100BASE-TX Full Duplex	1,RO/P	100BASE-TX FULL DUPLEX CAPABLE: 1= DM9102A able to perform 100BASE-TX in Full Duplex mode 0= DM9102A not able to perform 100BASE-TX in Full Duplex mode
1.13	100BASE-TX Half Duplex	1,RO/P	100BASE-TX Half Duplex Capable: 1=DM9102A is able to perform 100BASE-TX in Half Duplex mode 0=DM9102A is not able to perform 100BASE-TX in Half Duplex mode
1.12	10BASE-T Full Duplex	1,RO/P	10BASE-T Full Duplex Capable: 1=DM9102A is able to perform 10BASE-T in Full Duplex mode 0=DM9102A is not able to perform 10BASE-T in Full Duplex mode
1.11	10BASE-T Half Duplex	1,RO/P	10BASE-T Half Duplex Capable: 1=DM9102A is able to perform 10BASE-T in Half Duplex mode 0=DM9102A is not able to perform 10BASE-T in Half Duplex mode
1.10-1.7	Reserved	0000,RO	Reserved: Write as 0, ignore on read
1.6	MF Preamble Suppression	0,RO	MII Frame Preamble Suppression: 1=PHY will accept management frames with preamble suppressed 0=PHY will not accept management frames with preamble suppressed
1.5	Auto-negotiation Complete	0,RO	Auto-negotiation Complete: 1=Auto-negotiation process completed 0=Auto-negotiation process not completed
1.4	Remote Fault	0, RO/LH	Remote Fault: 1= Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM9102A implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0= No remote fault condition detected
1.3	Auto-negotiation Ability	1,RO/P	Auto Configuration Ability: 1=DM9102A able to perform Auto-negotiation 0=DM9102A not able to perform Auto-negotiation
1.2	Link Status	0,RO/LL	Link Status: 1=Valid link established (for either 10Mbps or 100Mbps operation) 0=Link not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the Link Status bit to be cleared and remain cleared until it is read via the management interface
1.1	Jabber Detect	0, RO/LH	Jabber Detect: 1=Jabber condition detected 0=No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management

			interface or a DM9102A reset. This bit works only in 10Mbps mode
1.0	Extended Capability	1,RO/P	Extended Capability: 1=Extended register capability 0=Basic register capability only

PHY ID Identifier Register #1 (PHYIDR1) – 2

The PHY Identifier Register#1 and Register#2 work together in a single identifier of the DM9102A. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Name	Default	Description
2.15-2.0	OUI_MSB	<0181H>	OUI Most Significant Bits: This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

PHY Identifier Register #2 (PHYIDR2) - 3

Bit	Name	Default	Description
3.15-3.10	OUI_LSB	<101110>, RO/P	OUI Least Significant Bits: Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
3.9-3.4	VNDR_MDL	<000100>, RO/P	Vendor Model Number: Six bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3.3-3.0	MDL_REV	<0000>, RO/P	Model Revision Number: Four bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 3)

Auto-negotiation Advertisement Register (ANAR) – 4

This register contains the advertised abilities of this DM9102A device as they will be transmitted to its link partner during Auto-negotiation.

Bit	Name	Default	Description
4.15	NP	0,RO/P	Next Page Indication: 0=No next page available 1=Next page available The DM9102A has no next page, so this bit is permanently set to 0
4.14	ACK	0,RO	Acknowledge: 1=Link partner ability data reception acknowledged 0=Not acknowledged The DM9102A's Auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the Auto-negotiation process. Software should not attempt to write to this bit.
4.13	RF	0, RW	Remote Fault:

			1=Local Device senses a fault condition 0=No fault detected
4.12-4.11	Reserved	00, RW	Reserved: Write as 0, ignore on read
4.10	FCS	0, RW	Flow Control Support: 1=Controller chip supports flow control ability 0=Controller chip doesn't support flow control ability
4.9	T4	0, RO/P	100BASE-T4 Support: 1=100BASE-T4 supported by the local device 0=100BASE-T4 not supported The DM9102A does not support 100BASE-T4 so this bit is permanently
4.8	TX_FDX	1, RW	100BASE-TX Full Duplex Support: 1=100BASE-TX Full Duplex supported by the local device
4.7	TX_HDX	1, RW	100BASE-TX Support: 1=100BASE-TX supported by the local device 0=100BASE-TX not supported
4.6	10_FDX	1, RW	10BASE-T Full Duplex Support: 1=10BASE-T Full Duplex supported by the local device 0=10BASE-T Full Duplex not supported
4.5	10_HDX	1, RW	10BASE-T Support: 1=10BASE-T supported by the local device 0=10BASE-T not supported
4.4-4.0	Selector	<00001>, RW	Protocol Selection Bits: These bits contain the binary encoded protocol selector supported by this node. <00001> indicates that this device supports IEEE 802.3 CSMA/CD.

Auto-negotiation Link Partner Ability Register (ANLPAR) – 5

This register contains the advertised abilities of the link partner when received during Auto-negotiation.

Bit	Name	Default	Description
5.15	NP	0, RO	Next Page Indication: 0= Link partner, no next page available 1= Link partner, next page available
5.14	ACK	0, RO	Acknowledge: 1=Link partner ability data reception acknowledged 0=Not acknowledged The DM9102A's Auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit.
5.13	RF	0, RO	Remote Fault: 1=Remote fault indicated by link partner 0=No remote fault indicated by link partner
5.12-5.10	Reserved	000, RO	Reserved: Write as 0, ignore on read
5.9	T4	0, RO	100BASE-T4 Support: 1=100BASE-T4 supported by the link partner 0=100BASE-T4 not supported by the link partner
5.8	TX_FDX	0, RO	100BASE-TX Full Duplex Support: 1=100BASE-TX Full Duplex supported by the link partner 0=100BASE-TX Full Duplex not supported by the link partner
5.7	TX_HDX	0, RO	100BASE-TX Support:

			1=100BASE-TX Half Duplex supported by the link partner 0=100BASE-TX Half Duplex not supported by the link partner
5.6	10_FDX	0, RO	10BASE-T Full Duplex Support: 1=10BASE-T Full Duplex supported by the link partner 0=10BASE-T Full Duplex not supported by the link partner
5.5	10_HDX	0, RO	10BASE-T Support: 1=10BASE-T Half Duplex supported by the link partner 0=10BASE-T Half Duplex not supported by the link partner
5.4-5.0	Selector	<00000>, RO	Protocol Selection Bits: Link partner's binary encoded protocol selector

Auto-Negotiation Expansion Register (ANER) – 6

Bit	Name	Default	Description
6.15-6.5	Reserved	0, RO	Reserved: Write as 0, ignore on read
6.4	PDF	0, RO/LH	Local Device Parallel Detection Fault: PDF=1: A fault detected via parallel detection function. PDF=0: No fault detected via parallel detection function
6.3	LP_NP_ABLE	0, RO	Link Partner Next Page Able: LP_NP_ABLE=1: Link partner, next page available LP_NP_ABLE=0: Link partner, no next page
6.2	NP_ABLE	0,RO/P	Local Device Next Page Able: NP_ABLE=1: DM9102A, next page available NP_ABLE=0: DM9102A, no next page DM9102A does not support this function, so this bit is always 0.
6.1	PAGE_RX	0, RO/LH	New Page Received: A new link code word page received. This bit will be automatically cleared when the register (Register 6) is read by management
6.0	LP_AN_ABLE	0, RO	Link Partner Auto-negotiation Able: A "1" in this bit indicates that the link partner supports Auto-negotiation.

DAVICOM Specified Configuration Register (DSCR) - 10h

Bit	Name	Default	Description
16.15:16.8	Reserved	0, RO	Reserved
16.7	F_LINK_100	0, RW	Force Good Link in 100Mbps: 0 = Normal 100Mbps operation 1 = Force 100Mbps good link status This bit is useful for diagnostic purposes.
16.6:16.4	Reserved	0,RO	Reserved
16.3	SMRST	0,RW	Reset State Machine: When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed.
16.2	MFPSC	0,RW	MF Preamble Suppression Control: MII frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off

16.1	SLEEP	0,RW	Sleep Mode: Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset
16.0	RLOUT	0,RW	Remote Loop out Control: When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing

DAVICOM Specified Configuration and Status Register (DSCSR) - 11h

Bit	Name	Default	Description
17.15	100FDX	1, RO	100M Full Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100Mbps Full Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
17.14	100HDX	1, RO	100M Half Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100Mbps Half Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
17.13	10FDX	1, RO	10M Full Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10Mbps Full Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
17.12	10HDX	1, RO	10M Half Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10Mbps Half Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
17.11-17.9	Reserved	000, RW	Reserved: Write as 0, ignore on read
17.8-17.4	PHYAD[4:0]	00001, RW	PHY Address Bit 4:0: The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY. A PHY address of <00000> will cause the isolate bit of the BMCR (bit 10, Register Address 00) to be set.
17.3-17.0	ANMB[3:0]	0000, RO	Auto-negotiation Monitor Bits: These bits are for debug only. The Auto-negotiation status will be written to these bits.

			b3 b2 b1 b0 0 0 0 0 In IDLE state 0 0 0 0 Ability match 0 0 1 0 Acknowledge match 0 0 1 1 Acknowledge match fail 0 1 0 0 Consistency match 0 1 0 1 Consistency match fail 0 1 1 0 Parallel detects signal_link_ready 0 1 1 1 Parallel detects signal_link_ready fail 1 0 0 0 Auto-negotiation completed successfully

10BASE-T Configuration/Status (10BTCSRCSR) - 12h

Bit	Name	Default	Description
18.15	Reserved	0, RO	Reserved: Write as 0, ignore on read
18.14	LP_EN	1, RW	Link Pulse Enable: 1=Transmission of link pulses enabled 0=Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation.
18.13	HBE	1,RW	Heartbeat Enable: 1=Heartbeat function enabled 0=Heartbeat function disabled When the DM9102A is configured for Full Duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in Full Duplex mode). It must set to be 1.
18.12	SQUELCH	1, RW	Squelch Enable 1 = normal squelch 0 = low squelch
18.11	JABEN	1, RW	Jabber Enable: Enables or disables the Jabber function when the DM9102A is in 10BASE-T Full Duplex or 10BASE-T Transceiver Loopback mode 1= Jabber function enabled 0= Jabber function disabled
18.10-18.0	Reserved	0, RO	Reserved

Functional Description

System Buffer Management

1.Overview

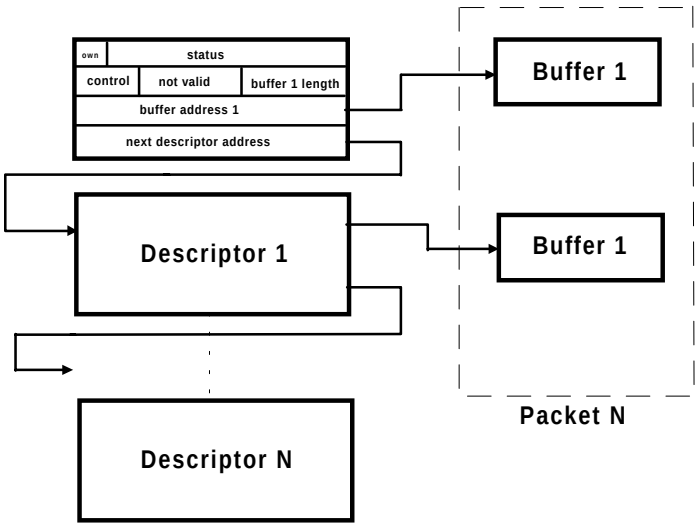
The data buffers for reception and transmission of data resides in the host memory. They are directed by the descriptor list that is located in another region of the host memory. All actions for the buffer management are operated by the DM9102A in conjunction with the driver. The data structures and processing algorithms are described in the following text.

2. Data Structure and Descriptor List

There are two types of buffers that reside in the host memory, the transmit buffer and the receive buffer. The buffers are composed of many distributed regions in the host memory. They are linked together and controlled by the descriptor lists that reside in another region of the host memory. The content of each descriptor includes pointer to the buffer, count of the buffer, command and status for the packet to be transmitted or received. Each descriptor list starts from the address setting of CR3 (receive descriptor base address) and CR4 (transmit descriptor base address). The descriptor list is Chain structure.

3. Buffer Management -- Chain Structure Method

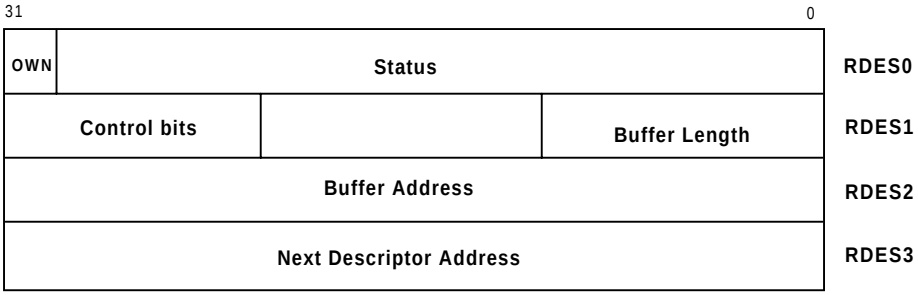
As the Chain structure depicted below, each descriptor contains two pointers, one point to a single buffer and the other to the next descriptor chained. The first descriptor is chained to the last descriptor under host driver's control. With this structure, a descriptor can be allocated anywhere in host memory and is chained to the next descriptor.



4. Descriptor List: Buffer Descriptor Format

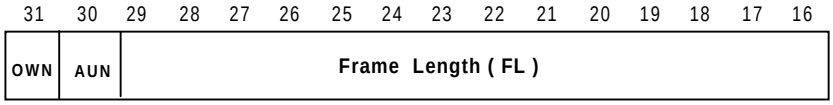
(a). Receive Descriptor Format

Each receive descriptor has four double-word entries and may be read or written by the host or the DM9102A. The descriptor format is shown below with a detailed functional description.



Receive Descriptor Format

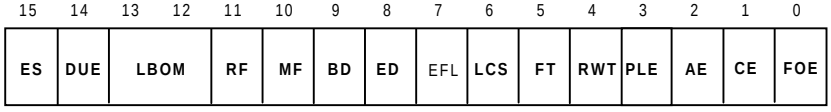
RDES0:



OWN: Owner bit of received status
1=owned by DM9102, 0=owned by host
This bit should be reset after packet reception is completed. The host will set this bit after received data is removed.

AUN: Received address unmatched.

FL: Frame Length
Frame length indicating total byte count of received packet.



This word-wide content includes status of received frame. They are loaded after the received buffer that belongs to the corresponding descriptor is full. All status bits are valid only when the last descriptor (End Descriptor) bit is set.

Bit 15: ES, Error Summary
It is set for the following error conditions:
Descriptor Unavailable Error (DUE =1), Runt Frame (RF=1), Excessive Frame Length (EFL=1), Late Collision Seen (LCS=1), CRC error (CE=1), FIFO Overflow error (FOE=1). Valid only when ED is set.

Bit 14: DUE, Descriptor Unavailable Error
It is set when the frame is truncated due to the buffer unavailable. It is valid only when ED is set.

Bit 13,12: LBOM, Loopback Operation Mode
These two bits show the received frame is derived from:
00 --- normal operation
01 --- internal loopback
10 --- PHY loopback
11 --- external loopback

Bit 11: RF, Runt Frame
It is set to indicate the received frame has the size smaller than 64 bytes. It is valid only when ED is set and FOE is reset.

Bit 10: MF, Multicast Frame
It is set to indicate the received frame has a multicast address. It is valid only when ED is set.

Bit 9: BD, Begin Descriptor
This bit is set for the descriptor indicating start of a received frame.

Bit 8: ED, Ending Descriptor
This bit is set for descriptor to indicate end of a received frame.

Bit 7: EFL, Excessive Frame Length
It is set to indicate the received frame length exceeds 1518 bytes. Valid only when ED is set.

Bit 6: LCS: Late Collision Seen
It is set to indicate a late collision found during the frame reception. Valid only when ED is set.

Bit 5: FT, Frame Type
It is set to indicate the received frame is the Ethernet-type. It is reset to indicate the received frame is the EEE802.3- type. Valid only when ED is set

Bit 4: RWT, Receive Watchdog Time-Out
It is set to indicate receive Watchdog time-out during the frame reception. CR5<9> will also be set. Valid only when ED is set.

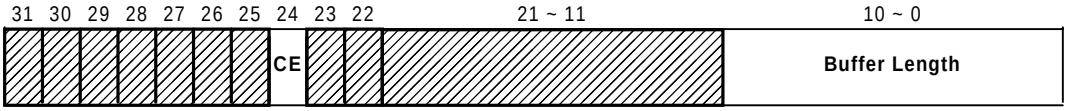
Bit 3: PLE, Physical Layer Error
It is set to indicate a physical layer error found during the frame reception.

Bit 2: AE, Alignment Error
It is set to indicate the received frame ends with a non-byte boundary.

Bit 1: CE, CRC Error
It is set to indicate the received frame ends with a CRC error. Valid only when ED is set.

Bit 0: FOE, FIFO Overflow Error
This bit is valid for Ending Descriptor is set. (ED = 1). It is set to indicate a FIFO Overflow error happens during the frame reception.

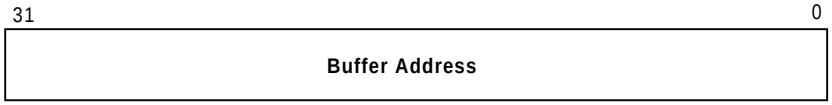
RDES1: Descriptor Status and Buffer Size



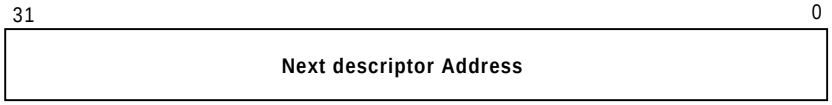
Bit 24: CE, Chain Enable
Must be 1.

Bit 10-0: Buffer Length
Indicates the size of the buffer.

RDES2: Buffer Starting Address
Indicates the physical starting address of buffer. This address must be double word alignment.

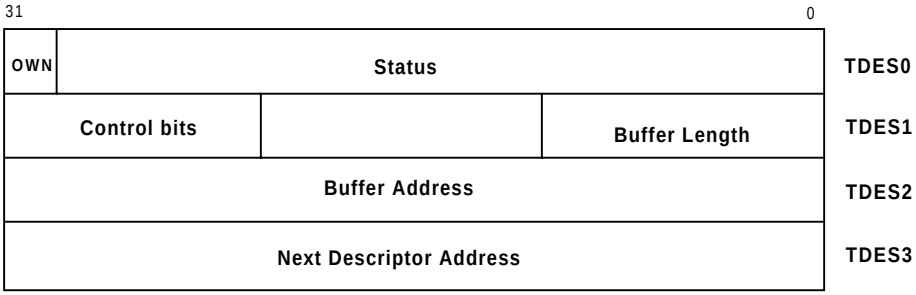


IRDES3: Next descriptor Address
Indicates the physical starting address of the chained descriptor under the Chain descriptor structure. This address must be eight word alignment.



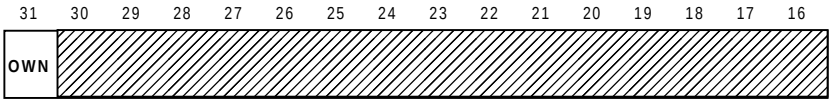
(b). Transmit Descriptor Format

Each transmit descriptor has four double-word content and may be read or written by the host or by the DM9102A. The descriptor format is shown below with detailed description

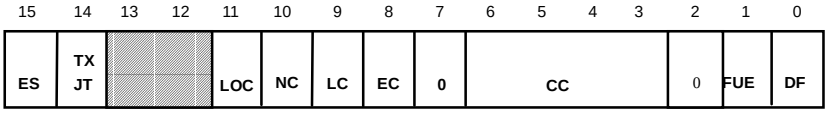


Transmit Descriptor Format

TDES0: Owner Bit with Transmit Status



Bit 31: OWN,
1=owned by DM9102A, 0=owned by host, this bit should be set when the transmitting buffer is filled with data and ready to be transmitted. It will be reset by DM9102A after transmitting the whole data buffer.



This word wide content includes status of transmitted frame. They are loaded after the data buffer that belongs to the corresponding descriptor is transmitted.

Bit 15: ES, Error Summary
It is set for the following error conditions:
Transmit Jabber Time-out (TXJT=1), Loss of Carrier (LOC=1), No Carrier (NC=1), Late Collision (LC=1), Excessive Collision (EC=1), FIFO Underrun Error (FUE=1).

Bit 14: TXJT, Transmit Jabber Time Out
It is set to indicate the transmitted frame is truncated due to transmit jabber time out condition. The transmit jabber time out interrupt CR5<3> is set.

Bit 11: LOC, Loss of Carrier
It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal loopback mode.

Bit 10: NC, No Carrier
It is set to indicate that no carrier signal from transceiver is found. It is not valid in internal loopback mode.

Bit 9: LC, Late Collision
It is set to indicate a collision occurs after the collision window of 64 bytes. Not valid if FUE is set.

Bit 8: EC, Excessive collision
It is set to indicate the transmission is aborted due to 16 excessive collisions.

Bit 7: Reserved
This bit is 0 when read.

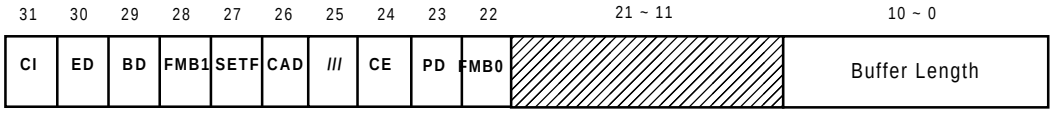
Bits 6-3: CC, Collision Count
These bits show the number of collision before transmission. Not valid if excessive collision bit is also set.

Bit 2: Reserved
This bit is 0 when read.

Bit 1: FUE, FIFO Underrun Error
It is set to indicate the transmission aborted due to transmit FIFO underrun condition.

Bit 0: DF, Deferred
It is set to indicate the frame is deferred before ready to transmit.

TDES1: Transmit buffer control and buffer size



Bit 31: CI, Completion Interrupt
It is set to enable transmit interrupt after the present frame has been transmitted. It is valid only when TDES1<30> is set or when it is a setup frame.

Bit 30: ED, Ending Descriptor
It is set to indicate the pointed buffer contains the last segment of a frame.

Bit 29: BD, Begin Descriptor
It is set to indicate the pointed buffer contains the first segment of a frame.

Bit 28: FMB1, Filtering Mode Bit 1
This bit is used with FMB0 to indicate the filtering type when the present frame is a setup frame.

Bit 27: SETF, Setup Frame
It is set to indicate the current frame is a setup frame.

Bit 26: CAD, CRC Append Disable
It is set to disable the CRC appending at the end of the transmitted frame. Valid only when TDES1<29> is set.

Bit 24: CE, Chain Enable
Must be "1".

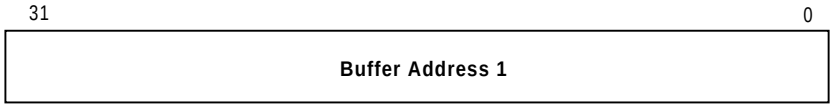
Bit 23: PD, Padding Disable
This bit is set to disable the padding field for a packet shorter than 64 bytes.

Bit 22: FMB0, Filtering Mode Bit 0
This bit is used with FMB1 to indicate the filtering type when the present frame is a setup frame.

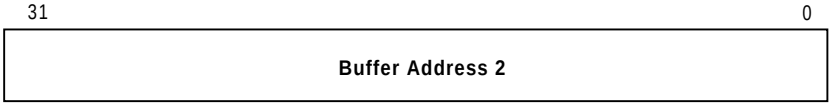
FMB1	FMB0	Filtering Type
0	0	Perfect Filtering
0	1	Hash Filtering
1	0	Inverse Filtering
1	1	Hash-Only Filtering.

Bit 10-0: Buffer 1 length
Indicates the size of buffer in Chain type structure.

TDES2: Buffer Starting Address indicates the physical starting address of buffer.



TDES3: Address indicates the next descriptor starting address
Indicates the physical starting address of the chained descriptor under the Chain descriptor structure. This address must be eight word alignment.



Initialization Procedure

After hardware or software reset, transmit and receive processes are placed in the state of STOP. The DM9102A

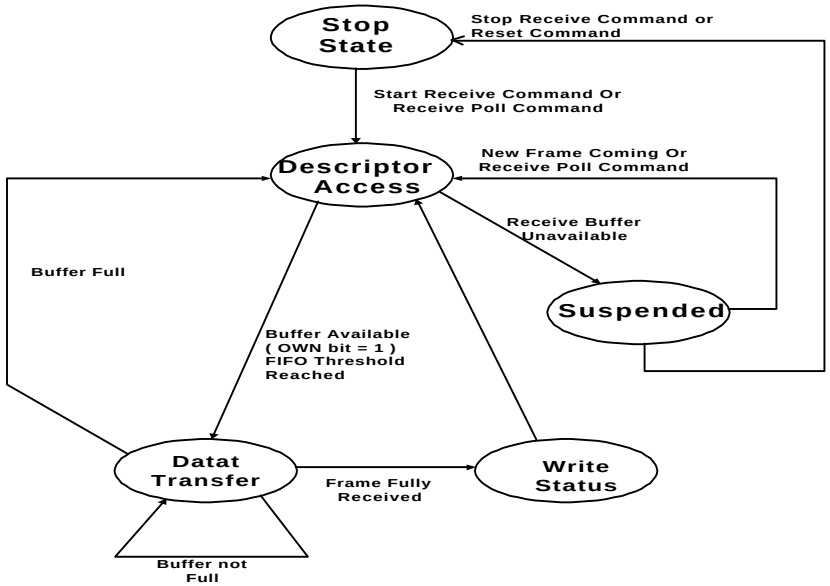
can accept the host commands to start operation. The general procedure for initialization is described below:
(1) Read/write suitable values for the PCI configuration registers.
(2) Write CR3 and CR4 to provide the starting address of each descriptor list.
(3) Write CR0 to set global host bus operation parameters.
(4) Write CR7 to mask causes of unnecessary interrupt.
(5) Write CR6 to set global parameters and start both receive and transmit processes. Receive and transmit processes will enter the running state and attempt to acquire descriptors from the respective descriptor lists.
(6) Wait for any interrupt.

Data Buffer Processing Algorithm

The data buffer process algorithm is based on the cooperation of the host and the DM9102A. The host sets CR3 (receive descriptor base address) and CR4 (transmit descriptor base address) for the descriptor list initialization. The DM9102A will start the data buffer transfer after the descriptor polling and get the ownership. For detailed processing procedure, please see below.

1. Receive Data Buffer Processing

The DM9102A always attempts to acquire an extra descriptor in anticipation of the incoming frames. Any incoming frame size covers a few buffer regions and descriptors. The following conditions satisfy the descriptor acquisition attempt:
When start/stop receive sets immediately after being placed in the running state.
When the DM9102A begins writing frame data to a data buffer pointed to by the current descriptor and the buffer ends before the frame ends.
When the DM9102A completes the reception of a frame and the current receiving descriptor is closed.
When receive process is suspended due to no free buffer for the DM9102A and a new frame is received.
When receive polling demand is issued. After acquiring the free descriptor, the DM9102A processes the incoming frame and places it in the acquired descriptor's data buffer. When whole the received frame data has been transferred, the DM9102A will write the status information to the last descriptor. The same process will repeat until it encounters a descriptor flagged as being owned by the host. If this occurs, receive process enters the suspended state and waits the host to service.

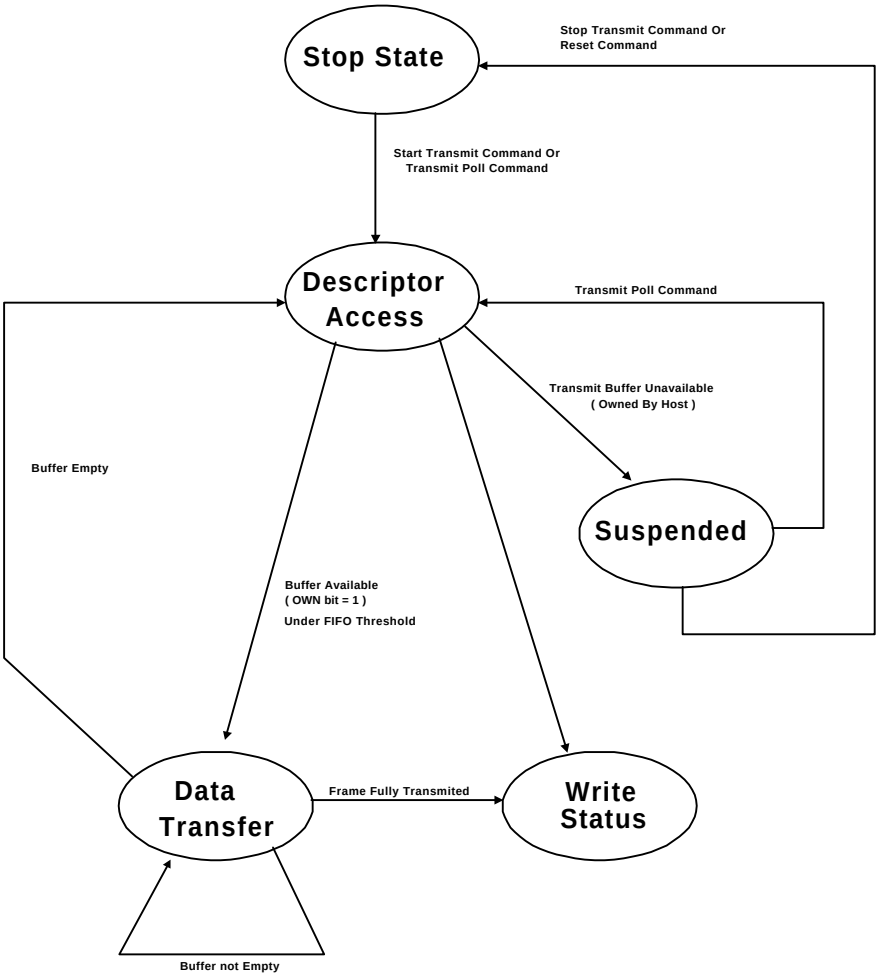


Receive Buffer Management State Transition

2. Transmit Data Buffer Processing

When start/stop transmit command is set and the DM9102A is in running state, transmit process polls transmit descriptor list for frames requiring transmission. When it completes a frame transmission, the status related to the transmitted frame will be written into the transmit descriptor. If the DM9102A detects a descriptor flagged as owned by the host and no transmit buffers are available, transmit process will be suspended. While in the running state, transmit process can simultaneously acquire two frames. As transmit process completes copying the first frame, it immediately polls transmit descriptor list for the second frame. If the second frame is valid, transmit process copies the frame before writing the status information of the first frame.

Both conditions will make transmit process suspend. (i) The DM9102A detects a descriptor owned by the host. (ii) A frame transmission is aborted when a locally induced error is detected. Under either condition, the host driver has to service the condition before the DM9102A can resume.



Transmit Buffer Management State Transition

Network Function

1. Overview

This chapter will introduce the normal state machine operation and MAC layer management like collision backoff algorithm. In transmit mode, the DM9102A initiates a DMA cycle to access data from a transmit buffer. It prefaces the data with the preamble, the SFD pattern, and it appends a 32-bit CRC. In receive mode, the data is de-serialized by receive mechanism and fed into the internal FIFO. For detailed process, please see below.

2. Receive Process and State Machine

a. Reception Initiation
As a preamble being detected on receive data lines, the DM9102A synchronizes itself to the data stream during the preamble and waits for the SFD. The synchronization process is based on byte boundary and the SFD byte is 10101011. If the DM9102A receives a 00 or a 11 after the first 8 preamble bits and before receiving the SFD, the reception process will be terminated.

b. Address Recognition
After initial synchronization, the DM9102A will recognize the 6-byte destination address field. The first bit of the destination address signifies whether it is a physical address (=0) or a multicast address (=1). The DM9102A filters the frame based on the node address of receive address filter setting. If the frame passes the filter, the subsequent serial data will be delivered into the host memory.

c. Frame Decapsulation
The DM9102A checks the CRC bytes of all received frames before releasing the frame along with the CRC to the host processor.

3. Transmit Process and State Machine

a. Transmission Initiation

Once the host processor prepares a transmit descriptor for the transmit buffer, the host processor signals the DM9102A to take it. After the DM9102A has been notified of this transmit list, the DM9102A will start to move the data bytes from the host memory to the internal transmit FIFO. When the transmit FIFO is adequately filled to the programmed threshold level, or when there is a full frame buffered into the transmit FIFO, the DM9102A begins to encapsulate the frame. The transmit encapsulation is performed by the transmit state machine, which delays the actual transmission onto the network until the network has been idle for a minimum inter frame gap time.

b. Frame Encapsulation
The transmit data frame encapsulation stream consists of two parts: Basic frame beginning and basic frame end. The former contains 56 preamble bits and SFD, the later, FCS. The basic frame read from the host memory includes the destination address, the source address, the type/length field, and the data field. If the data field is less than 46 bytes, the DM9102A will pad the frame with pattern up to 46 bytes.

c. Collision
When concurrent transmissions from two or more nodes occur (termed; collision), the DM9102A halts the transmission of data bytes and begins a jam pattern consisting of AAAAAAAA. At the end of the jam transmission, it begins the backoff wait time. If the collision was detected during the preamble transmission, the jam pattern is transmitted after completing the preamble. The backoff process is called truncated binary exponential backoff. The delay is a random integer multiple of slot times. The number of slot times of delay before the N^{th} retransmission attempt is chosen as a uniformly distributed random integer in the range:
$0 \le r < 2^k$
$k = \min (n, N)$ and $N=10$

4. Physical Layer Overview:

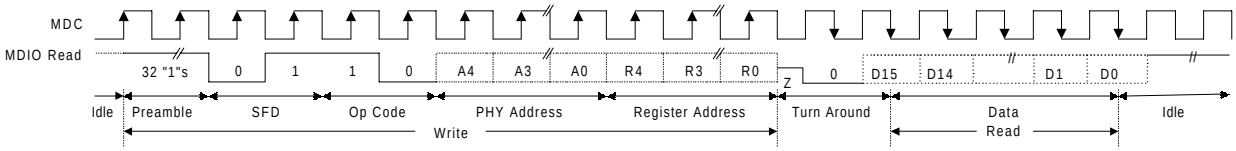
The DM9102A provides 100M/10Mbps dual port operation. It provides a direct interface either to Unshielded Twisted pair Cable UTP5 for 100BASE-TX Fast Ethernet, or UTP5/UTP3 Cable for 10BASE-T Ethernet. In physical level operation, it consists of the following blocks:
- PCS
- Clock generator
- NRE/NREI, MLT-3 encoder/decoder and driver
- MANCHESTER encoder/decoder
- 10BASE-T filter and driver

Serial Management Interface

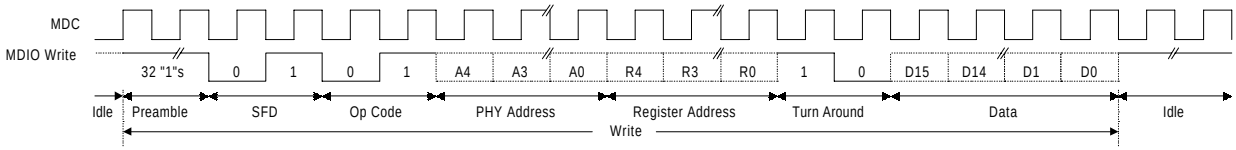
The serial management interface uses a simple, two-wired serial interface to obtain and control the status of PHY management register set through an MDC and MDIO. The Management Data Clock (MDC) is equipped with a maximum clock rate of 2.5MHz, while Management Data Input /Output (MDIO) works as a bi-directional, shared by up to 32 devices.

In read/write operation, the management data frame is 64-bit long start with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP):<10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) filing between Resistor Address field and Data field is provided for MDIO to avoid contention. "Z" stands for the state of high impedance. Following turnaround time, a 16-bit data is read from or written onto management registers.

Management Interface - Read Frame Structure



Management Interface - Write Frame Structure



Power Management

1. Overview

The DM9102A supports power management mechanism. It complies with the ACPI Specification Rev 1.0, the Network Device Class Power Management Specification Rev 1.0, and PCI Bus Power Management Interface Specification Rev 1.0. In addition, it also support Wake-On LAN (WOL) which is the features of the AMD's Magic Packet™ technology. With this function, it can wake-up a remote sleeping station.

2. PCI Function Power Management States

The DM9102A supports PCI function power states D0, D3(hot), D3(cold), and not supports D1, D2 states. Additional PCI signal PME# (power management event, open drain) to pin A19 of the standard PCI connector.

D0: normal & fully functional state

D3(hot) : For controller, configuration space can be accessed and wake-up on LAN circuit can be enabled. PME# operational circuit is active, full function is supported to detect the wake-up Frame & Link status. Because of functions in D3(hot) must respond to configuration space accesses as long as power and clock are supplied so that they can be returned to D0 state by software.

D3(cold) : If Vcc is removed from a PCI device, all of its PCI functions transition immediately to D3(cold), no bus transaction is active under no pci_clk condition and wake-up on LAN operation should be alive. PME# operational circuit is active. Full function is supported under auxiliary power to detect the wake-up Frame & Link status. When power restored, PCI RST# must be asserted and functions will return to D0 with a full PCI Spec. 2.2 compliant power-on reset sequence. The power required in D3(cold) must be provided by some auxiliary power source.

3. The Power Management Operation

It complies with the PCI Bus Power Management Interface Specification Rev. 1.0. The Power Management Event (PME#) signal is an optional open drain, active low signal that is intended to be driven low by a PCI function to request a change in its current power management state and/or to indicate that a power management event has occurred.

The PME# signal has been assigned to pin A19 of the standard PCI Connector configuration. The assertion and de-assertion of PME# is asynchronous to the PCI clock.

Software will enable its use by setting the PME_En bit in the PMCSR (write 1 to PMCSR<8>). When a PCI function generates or detects an event that requires the system to change its power state, the function will assert PME#. It must continue to assert PME# until software either clears the PME_En bit (PMCSR<8> is set to 0) or clears the PME_Status bit in the PMCSR (write 1 to PMCSR<15>).

DM9102A support three main categories of network device wake-up events specified in Network Device Class Power Management Rev1.0. That is, the DM9102A can monitor the network for a Link Change, Magic Packet or a Wake-up Frame and notify the system by generating PME# if any of three events occurs. Program the PCIUSR (offset = 40h) can select the PME# event, and write 1 to PMCSR<15> will clear the PME#.

a. Detect Network Link State Change
Any link status change will set the wake-up event.

1. Writes 1 into PMCSR<15>(54h) to clear previous PME# status
2. Writes 1 into PMCSR<8> to enable PME# function
3. Writes 1 into PCIUSR<29> to enable the link status change function

b. Active Magic Packet Function
Could be optionally enabled from EEPROM contents. Send a setup frame with a magic node address at first filter address using perfect address filtering mode.

1. Writes 1 into PMCSR<15> to clear previous PME status
2. Writes 1 into PMCSR<8> to enable PME# function
3. Writes 1 into PCIUSR<27> to enable magic packet function.

c. Active the Sample Frame Function
Could be optionally enabled from PCIUSR<28>. Sample frame data and corresponding byte mask are loaded into transmit FIFO & receive FIFO before entering D3(hot). The software driver has to stop the TX/RX process before setting the sample frame and byte mask into the FIFO. Transmit &

receive FIFO can be accessed from CR13 & CR14 by programming CR6<28:25> = 0011.

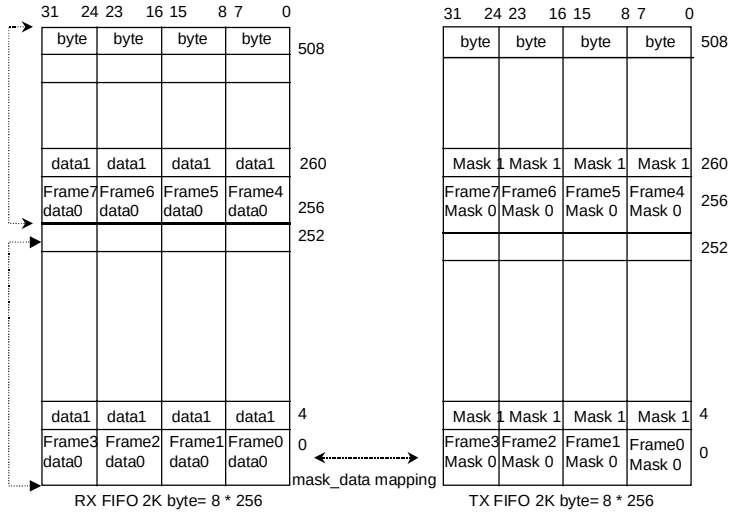
The operational sequence from D0 to D3 should be:
Stop TX/RX process → wait for entering stop state → set test mode, CR6<28:25> = 0011 → programming FIFO contents → exit test mode → enter D3(hot) state

The sample frame data comparison is completed when the received frame data has exceeded the programmed frame length or the full packet has been fully received. The operation procedure is shown below.

DM9102A can handle 8 sample frames.
The max byte count is 256 byte each sample frame.

bit1	bit0	description
0	0	this byte don't care
0	1	this byte musk check
1	0	this byte don't care
1	1	end of mask(sample frame)

Frame mask definition: only used bit0&bit1



RX FIFO 2K byte= 8 * 256 TX FIFO 2K byte= 8 * 256

CR13: Sample Frame Access Register

Name	General definition	Bit8:3	Type
TxFIFO	Transmit FIFO access port	32h	R/W
RxFIFO	Receive FIFO access port	35h	RW
DiagReset	General reset for diagnostic pointer port	38h	RW

In DiagReset port there are 7 bits:
Bit 0: clear TX FIFO write_address to 0.
Bit 1: clear TX FIFO read_address to 0.,
Bit 2: clear RX FIFO write_address to 0.
Bit 3: clear RX FIFO read_address to 0.,
Bit 4: reserved.
Bit 5: set TX FIFO write_address to 100H.,
Bit 6: set RX FIFO write_address to 100H.

Sample Frame Programming Guide:

1. Enter the sample frame access mode
   Let CR6<28:25>=0011

2.Reset the TX/RX FIFO, write pointer to offset 0
  Write 38h to CR13<8:3>
  Write 01h to CR14 (reset)
  Write 00h to CR14 (clear)

3. Write the sample frame 0-3 data to RX FIFO
  Write 35h to CR13<8:3>
  Write xxxxxxxxh to CR14 (Frame1~3 first byte)
  Write xxxxxxxxh to CR14 (Frame1~3 second byte)
      :
      :
  Repeat write until all frame data written to RX FIFO

4. RESET RX FIFO, write pointer to offset 100h
  Write 38h to CR13<8:3>
  Write 40h to CR14 (reset)
  Write 00h to CR14 (clear)

5. Write the sample frame 4-7 to RX FIFO
  Write 35h to CR13<8:3>
  Write xxxxxxxxh to CR14 (Frame4~7 first byte)
  Write xxxxxxxxh to CR14 (Frame4~7 second byte)
      :
      :
  Repeat write until all frame data written to RX FIFO

6. Write the sample frame 0-3 mask to TX FIFO
  Write 32h to CR13<8:3>
  Write xxxxxxxxh to CR14 (Frame0~3 first mask byte)
  Write xxxxxxxxh to CR14 (Frame0~3 second mask byte)
      :
      :
  Repeat write until all frame mask which is written to TX FIFO

7. RESET TX FIFO, write pointer to offset 100h
  Write 38h to CR13<8:3>
  Write 20h to CR14 (reset)
  Write 00h to CR14 (clear)

8. Write the sample frame 4-7 mask to TX FIFO
  Write 32h to CR13<8:3>
  Write xxxxxxxxh to CR14 (Frame4~7 first mask byte)
  Write xxxxxxxxh to CR14 (Frame4~7 second mask byte)
      :
      :
  Repeat write until all frame mask which is written to TX FIFO

Serial ROM Overview

The purpose of Configuration ROM (EEPROM) is to support the DM9102A information to the driver for the card. The SROM must support 64 words or more space for configuration data. The format of the SROM is as followed

The format of EEPROM

Field Name	Offset	Size
Subsystem ID block	0	18
CROM version	18	1
Controller count	19	1
Controller_0 Information	20	n
Controller_1 Information	20+n	m
: (depends on controller count)	:	:
CRC checksum	126	2

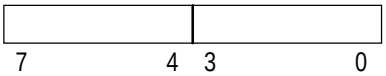
1. Subsystem ID Block

Every card must have a Subsystem ID to indicate the system vendor information. The content will be transferred into the PCI configuration space during hardware reset function.

Vendor ID & Device ID can be set in EEPROM content & auto-loaded to PCI configuration register after reset.(default value = 1282, 9102) This function must be selectable for enable/disable by Auto_Load_Control (offset 08 of EEPROM) setting to avoid damaging default value due to incorrectly auto-load operation. CRC check circuit of EEPROM contents to decide the auto-load operation of Vendor ID & Subsystem.

Subsystem ID Block		Byte Offset.
Subsystem Vendor ID		0
Subsystem ID		2
Reserved		4
Reserved		6
NCE	Auto_load_control	8
PCI Vender ID		10
PCI Device ID		12
PMCSR	PMC	14
Reserved	ID_block_CRC	17,16

Byte Offset (08): Auto_Load_Control



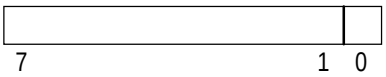
Bit3~0: “1010” to enable auto-load of PCI Vendor_ID & Device_ID, “0” to disable.

Bit7~4: “1X1X” to enable auto-load of NCE, PME & PMC & PMCSR to PCI configuration space. These four bits can also control the inverse of WOL or PULSE WOL..

If bit4 = 0, WOL is Active HIGH.
If bit4=1, WOL is Active LOW

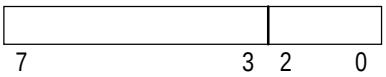
If bit6 = 0, WOL is PULSE signal
If bit6=1, WOL is DC LEVEL signal.

Byte Offset (09): New_Capabilities_Enable



Bit0: Directly mapping to bit20 (New Capabilities) of the PCICS

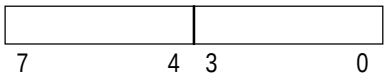
Byte Offset (14): PMC



Bit7~3: Directly mapping to bit15~11 of PMC (that is bit31~27 of Power Management Register)

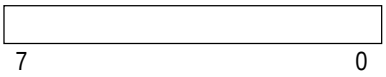
Bit2~0: Directly mapping to bit5~3 of PMC (that is bit21~19 of Power Management Register)

Byte Offset (15):



Bit7~4: Reserved
Bit3: Set to disable the output of PME# pin.
Bit2: Set to disable the output of WOL pin.
Bit1: Set to enable the link change wake up event.
Bit0: Set to enable the Magic packet wake up event.

Byte Offset (16): ID_BLOCK_CRC



This field is implemented to confirm the correct reading of the EEPROM contents.

2. SROM Version

Current version number is 03.

3. Controller Count

The configuration ROM supports multiple controllers in one board. Every controller has its unique controller information block. Controller count indicates the number of controllers put in the card.

4. Controller_X Information

Each controller has its information block to address its node ID, GPR control, supported connect media types (Media Information Block) and other application circuit information block.

Controller Information Header

ITEM	Offset	Size
Node Address	0	6
Controller_x Number	6	1
Controller_x Info. Block Offset	7	1

5. Controller Information Body Pointed By Controller_X Info Block Offset Item In Controller Information Header:

Item	Offset	Size
Connection Type Selected	0	2
GPR Control	2	1
Block Count	3	1
Block_1	4	n
:	4+n	m

* Connect Type Selected indicates the default connect media type selected.
* GPR Control defines the input or output direction of GPR.

There are three types of block:
1. PHY Information Block (type=01)
2. Media Information Block (type=00)
3. Delay Period Block (type=80)

PHY information Block: (type=01)

Item	Offset	Size
Block Length	0	1
Block Type(01)	1	1
PHY Number	2	1
GPR Initial Length(G_i)	3	1
GPR Initial Data	4	G_i
Reset Sequence Length(R_i)	4+G_i	1
Reset Data	5+G_i	R_i
Media Capabilities	5+G_i+R_i	2
Nway Advertisement	7+G_i+R_i	2
FDX Bit Map	9+G_i+R_i	2

TTM Bit Map	11+G_i+R_i	2

Note 1: The definition of Media Capabilities and Nway Advertisement is the same with 802.3U in terms of Auto-negotiation.

Media Information Block: (Type = 00)

ITEM	Offset	Size
Block Length	0	1
Block Type(00)	1	1
Media Code	2	1
GPR Data	3	1
Command	4	2

Note 1: Media Code: 10BASE_T Half Duplex 00
10 BASE_T Full Duplex 04
100 BASE_T Half Duplex 01
100 BASE_T Full Duplex 05

Note 2: Command Format

Delay Period Block (Type = 80): Define the delay time unit in us.

ITEM	Offset	Size
Block Length	0	1
Block Type(80)	1	1
Time Unit	2	2

6. Example of DM9102A SROM Format

Total Size: 128 Bytes

Field Name	Offset (Bytes)	Size (Bytes)	Value (Hex)	Commentary
Sub-Vendor ID	0	2	1282	ID Block
Sub-Device ID	2	2	9102	
Reserved1	4	4	00000000	
Auto_Load_Control	8	1	00	Auto-load function definition: Bit 3~0 = 1010 → Auto-Load PCI Vendor ID/Device ID enabled Bit 7~4 = 1x1x → Auto-Load NCE, PMC/PMCSR enabled
New_Capabilities_Enable (NCE)	9	1	00	Please refer to DM9102A Spec.
PCI Vendor ID	10	2	1282	If Auto-Load PCI Vendor ID/Device ID function disabled, the PCI Vendor ID/Device ID will use the default values (1282h, 9102h).
PCI Device ID	12	2	9102	
Power Management Capabilities (PMC)	14	1	00	Please refer to DM9102A Spec.
Power Management Control/Status (PMCSR)	15	1	00	Please refer to DM9102A Spec.
ID_BLOCK_CRC	16	1	-	Offset 0..15, 17 ID CRC
Reserved2	17	1	00	

Field Name	Offset (Bytes)	Size (Bytes)	Value (Hex)	Commentary
SROM Format Version	18	1	03	Version 3.0
Controller Count	19	1	01	
IEEE Network Address	20	6	-	Controller Info Header
Controller_0 Device Number	26	1	00	

Field Name	Offset (Bytes)	Size (Bytes)	Value (Hex)	Commentary
Controller_0 Info Leaf Offset	27	2	001E	Offset 30
Reserved3	29	1	00	
Selected Connected Type	30	2	0800	Controller_0 Info Leaf Block
General Purpose Control	32	1	80	MAC CR12 Register
Block Count	33	1	06	6 Blocks
F(1)+Length	34	1	8E	Block 1 (PHY Info Block)
Type	35	1	01	PHY Information Block
PHY Number	36	1	01	PHY Address
GPR Length	37	1	00	
Reset Sequence Length	38	1	02	
Reset Sequence	39	2	0080	
Media Capabilities	41	2	7800	
Nway Advertisement	43	2	01E0	
FDX Bit Map	45	2	5000	
TTM Bit Map	47	2	1800	
F(1)+Length	49	1	85	Block 2 (Delay Period Block)
Type	50	1	80	Delay Period Block
Delay Sequence	51	4	40002000	Micro-Second

Field Name	Offset (Bytes)	Size (Bytes)	Value (Hex)	Commentary
F(1)+Length	55	1	85	Block 3 (Media Info Block)
Type	56	1	00	Media Information Block
Media Code	57	1	00	10Base-T Half_Duplex
GPR Data	58	1	00	
Command	59	2	0087	
F(1)+Length	61	1	85	Block 4 (Media Info Block)
Type	62	1	00	Media Information Block
Media Code	63	1	01	100Base-TX Half_Duplex
GPR Data	64	1	00	
Command	65	2	0087	
F(1)+Length	67	1	85	Block 5 (Media Info Block)
Type	68	1	00	Media Information Block
Media Code	69	1	04	10Base-T Full_Duplex
GPR Data	70	1	00	
Command	71	2	0087	
F(1)+Length	73	1	85	Block 6 (Media Info Block)
Type	74	1	00	Media Information Block
Media Code	75	1	05	100Base-TX Full_Duplex
GPR Data	76	1	00	
Command	77	2	0087	
SROM_CRC	126	2	-	Offset 0..125 SROM CRC

External MII/SRL Interface

DM9102A provides one external MII/SRL interface sharing with all the pins with Boot ROM interface. This external MII/SRL interface can be connected with external PHYceiver such as Home Networking PHYceiver or other future technology applications. This external MII/SRL interface can be set up by hardware and software. The setup methods are listed as below:

	Test 1 (pin 75)	Test 2 (pin 71)	Clkrun# (pin 36)	MA8 (pin 84)	MA9 (pin 85)	
Normal Operation	0	1	X	X	X	
External MII mode	0	0	0	0	1/0	**Note 1**
External SRL mode	0	0	0	1	1/0	**Note 2**
Internal Test mode	1	X	X	X	X	

Note 1: External MII mode
MA9 = 1 (Set up by harware; Mode cannot be changed.)
MA9 = 0 & MII_Mode = 1 (Select external MII interface; Mode can be changed by software.)
Where MII_Mode is the bit 18 of CR6.

Note 2: External MII mode:
MA9 = 1 (Set up by harware; Mode cannot be changed.)
MA9 = 0 & MII_Mode = 0 (Select external SRL interface; Mode can be changed by software.)

The Sharing Pin Table (o): output, (i): input, (b): bi-direction

	Normal Operation		External MII/SRL Interface	
	Boot ROM Mux mode	Boot ROM Dir mode	External MII interface	External SRL interface
	MA6 = 0	MA6 = 1	MA8 = 0	MA8 = 1
Pin				
62	BPAD0	MD0/DI	MII_TXD3 (o)	BPAD0
63	BPAD1	MD1	MII_TXD2 (o)	BPAD1
64	BPAD2	MD2	MII_TXD1 (o)	BPAD2
65	BPAD3	MD3	MII_RXER (i)	BPAD3
66	BPAD4	MD4	MII_RXDV (i)	BPAD4
67	BPAD5	MD5	MII_RXD1 (i)	BPAD5
68	BPAD6	MD6	MII_RXD2 (i)	BPAD6
69	BPAD7	MD7	MII_MDIO (b)	BPAD7
72	BPCS#	ROMCS	MII_MDC (o)	BPCS#
73	BPA0	MA0	NC	BPA0
74	BPA1	MA1	MII_RXD (i)	BPA1
77	EEDI	MA2	EEDI (i)	EEDI (i)
78	EEDO	MA3/DO	EEDO (o)	EEDO (o)
79	EECK	MA4/CK	EECK (o)	EECK (o)
80	EECS	MA5	EECS (o)	EECS (o)
81		MA6	MII_COL (i)	SRL_COL (i)
83		MA7	MII_TXCLK (i)	SRL_TXC (i)
84		MA8	MII_TXEN (o)	SRL_TXE (o)

85		MA9	MII_TXD0 (o)	SRL_TXD (o)
87	TRFLED	MA10/TRF	NC	NC
88	FDXLED	MA11/FDX	OSC20 (o)	OSC20 (o)
89	SPD100	MA12/100	Link (i)	Link (i)
90	SPD10	MA13/10	NC	NC
91		MA14	MII_CRS (i)	SRL_CRS (i)
92		MA15	MII_RXCLK (i)	SRL_RXC (i)
93		MA16	MII_RXD0 (i)	SRL_RXD (i)
94	MA17	MA17	NC	NC

Where NC is no connection

Pin88 is 20MHz clock output for external PHY (such as DM9801)

Pin89 is link status input from external PHY for power management changed event and reflect at CR12 bit6.

Absolute Maximum Ratings

Absolute Maximum Ratings* (25°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVCC,AVCC	Supply Voltage	-0.3	3.6	V	
VIN	DC Input Voltage (VIN)	-0.5	5.5	V	
VOUT	DC Output Voltage(VOUT)	-0.3	3.6	V	
Tc	Case Temperature Range	0	85	°C	
Tstg	Storage Temperature Rang (Tstg)	-65	150	°C	
LT	Lead Temp. (TL, Soldering, 10 sec.)	---	220	°C	

Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVCC,AVCC	Supply Voltage	3.135	3.465	V	
Tc	Case Temperature	0	85	°C	
PD (Power Dissipation)	100BASE-TX	---	115	mA	3.3V
	100BASE-TX IDLE	---	115	mA	3.3V
	10BASE-T TX	---	125	mA	3.3V
	10BASE-T IDLE	---	45	mA	3.3V
	Auto-negotiation	---	76	mA	3.3V

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

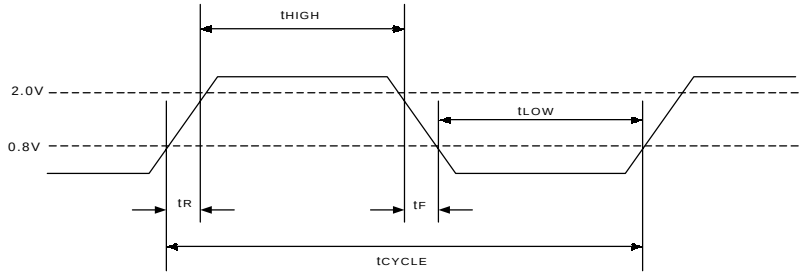
DC Electrical Characteristics

(0°C<Tc<85°C, 3.135V<VCC<3.465V, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
V_{IL}	Input Low Voltage	---	---	0.8	V	
V_{IH}	Input High Voltage	2.0	---	---	V	
I_{IL}	Input Low Leakage Current	---	---	5	uA	V_{IN} = 0V
I_{IH}	Input High Leakage Current	5	---	---	uA	V_{IN} = 3.3V
Outputs						
V_{OL}	Output Low Voltage	---	---	0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	2.4	---	---	V	I_{OH} = -4mA
Receiver						
V_{ICM}	RX+/RX- Common mode Input Voltage	---	0.9	---	V	100 Ω Termination Across
Transmitter						
V_{TD100}	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
V_{TD10}	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
I_{TD100}	100TX+/- Differential Output Current	19	20	21	mA	Absolute Value
I_{TD10}	10TX+/- Differential Output Current	44	50	56	mA	Absolute Value

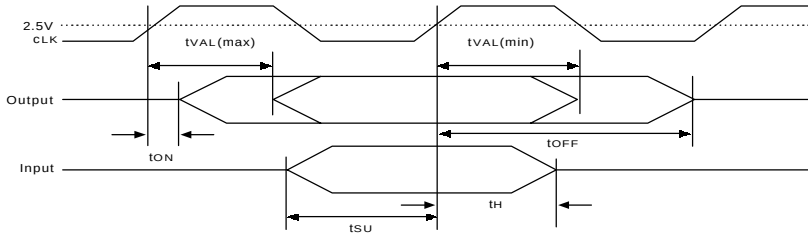
AC Electrical Characteristics & Timing Waveforms

PCI Clock Specifications Timing



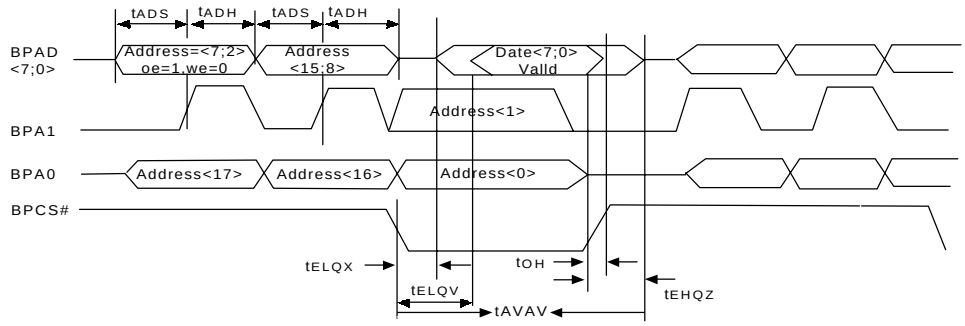
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tR	PCI_CLK rising time	-	-	4	ns	-
tF	PCI_CLK falling time	-	-	4	ns	-
tCYCLE	Cycle time	25	30	-	ns	-
tHIGH	PCI_CLK High Time	12	-	-	ns	-
tLOW	PCI_CLK Low Time	12	-	-	ns	-

Other PCI Signals Timing Diagram



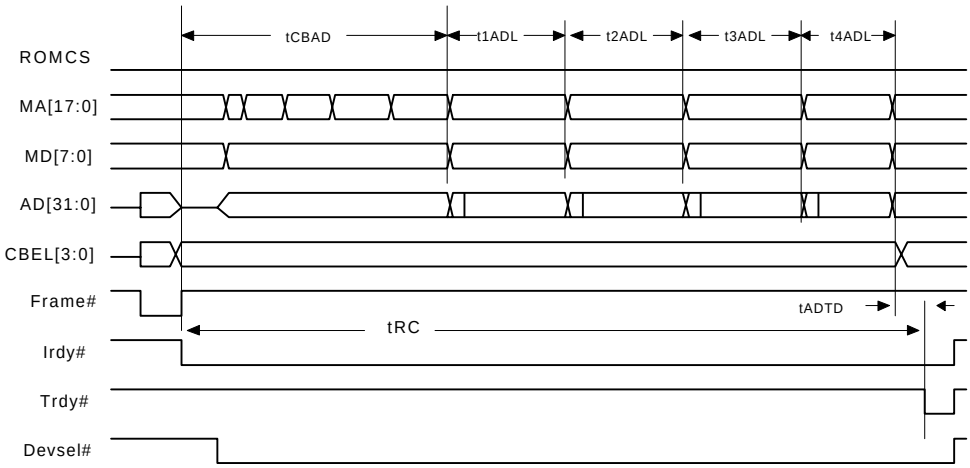
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tVAL	Clk-To-Signal Valid Delay	2	-	11	ns	Cload = 50 pF
tON	Float-To-Active Delay From Clk	2	-	-	ns	-
tOFF	Active-To-Float Delay From Clk	-	-	28	ns	-
tSU	Input Signal Valid Setup Time Before Clk	7	-	-	ns	-
tH	Input Signal Hold Time From Clk	0	-	-	ns	-

Multiplex Mode Boot ROM Timing



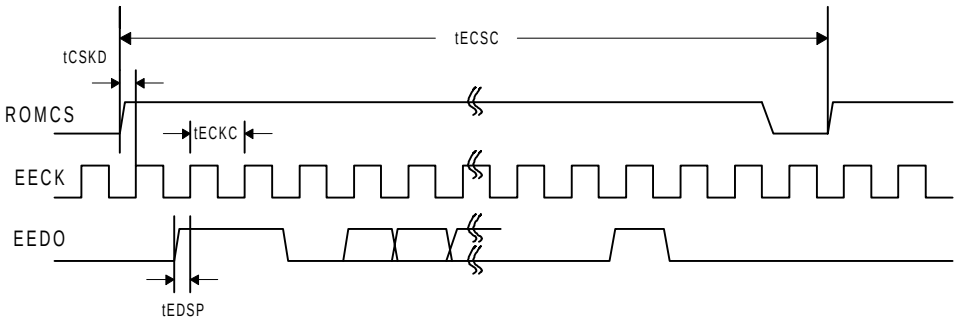
Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
tAVAV	Read Cycle Time	-	31	-	PCI clock	-
tELQV	BPCS# To Output Delay	0	-	7	PCI clock	-
tEHQZ	BPCS# Rising Edge To Output High Impedance	-	1	-	PCI clock	-
tOH	Output Hold From BPCS#	0	-	-	PCI clock	-
tADS	Address Setup To Latch Enable High	4	-	-	PCI clock	-
TADH	Address Hold From Latch Enable High	4	-	-	PCI clock	-

Direct Mode Boot ROM Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tRC	Read Cycle Time	-	50	-	PCI clock	-
tCBAD	Bus Command to first address delay	-	18	-	PCI clock	-
t1ADL	first address length	-	8	-	PCI clock	-
t2ADL	second address delay	-	8	-	PCI clock	-
t3ADL	third address delay	-	8	-	PCI clock	-
t4ADL	fourth address delay	-	7	-	PCI clock	-
tADTD	end of address to Tardy active	-	1	-	PCI clock	-

EEPROM Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tECKC	Serial ROM clock EECK period	64	-	-	PCI clock	-
tECSC	Read Cycle Time	1792	-	-	PCI clock	-
tCSKD	Delay from ROMCS High to EECK High	28	-	-	PCI clock	-
tEDSP	Setup Time of EEDO to EECK	24	-	-	PCI clock	-

TP Interface

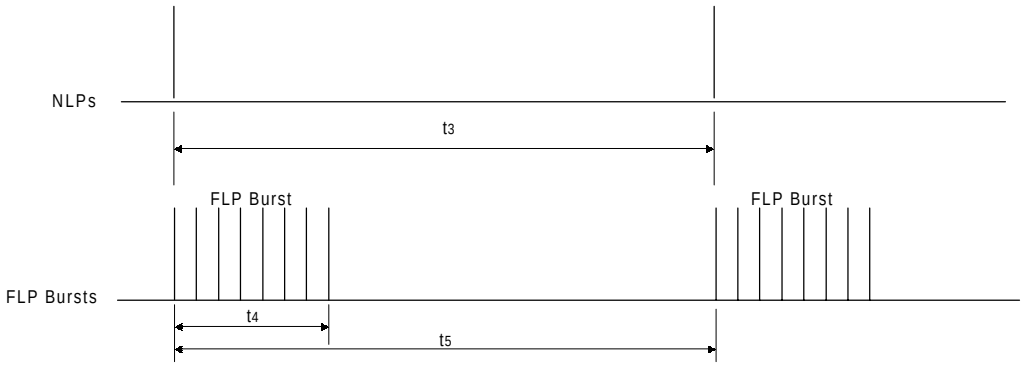
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_{TR/F}$	100TX+/- Differential Rise/Fall Time	3.0	---	5.0	ns	
t_{TM}	100TX+/- Differential Rise/Fall Time Mismatch	0	---	0.5	ns	
t_{TDC}	100TX+/- Differential Output Duty Cycle Distortion	0	0	0.5	ns	
$t_{T/T}$	100TX+/- Differential Output Peak-to-Peak Jitter	0	---	1.4	ns	
X_{OST}	100TX+/- Differential Voltage Overshoot	0	---	5	%	

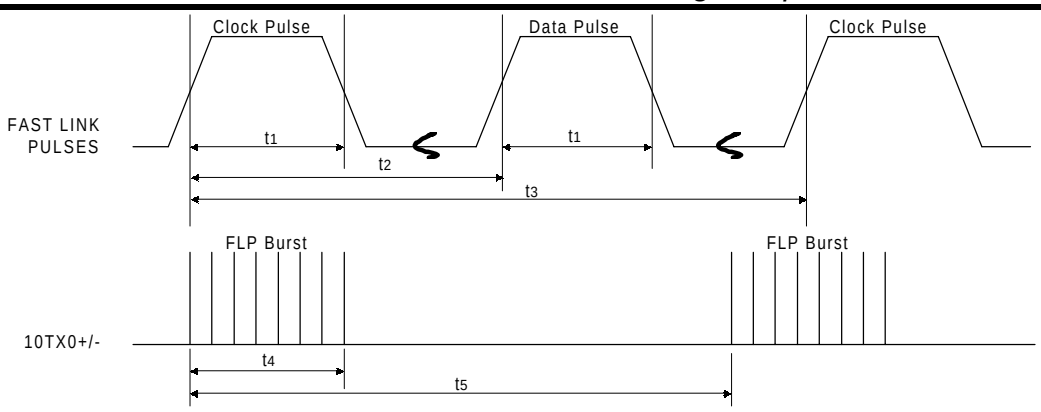
Oscillator/Crystal Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CKC}	OSC Cycle Time	39.996	40	40.004	ns	
T_{PWH}	OSC Pulse Width High	16	20	24	ns	
T_{PWL}	OSC Pulse Width Low	16	20	24	ns	

Auto-negotiation and Fast Link Pulse Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_1	Clock/Data Pulse Width	---	100	---	ns	
t_2	Clock Pulse To Data Pulse Period	55.5	62.5	69.5	us	DATA = 1
t_3	Clock Pulse To Clock Pulse Period	111	125	139	us	
t_4	FLP Burst Width	-	2	-	ms	
t_5	FLP Burst To FLP Burst Period	8	16	24	ms	
-	Clock/Data Pulses in a Burst	17		33	#	

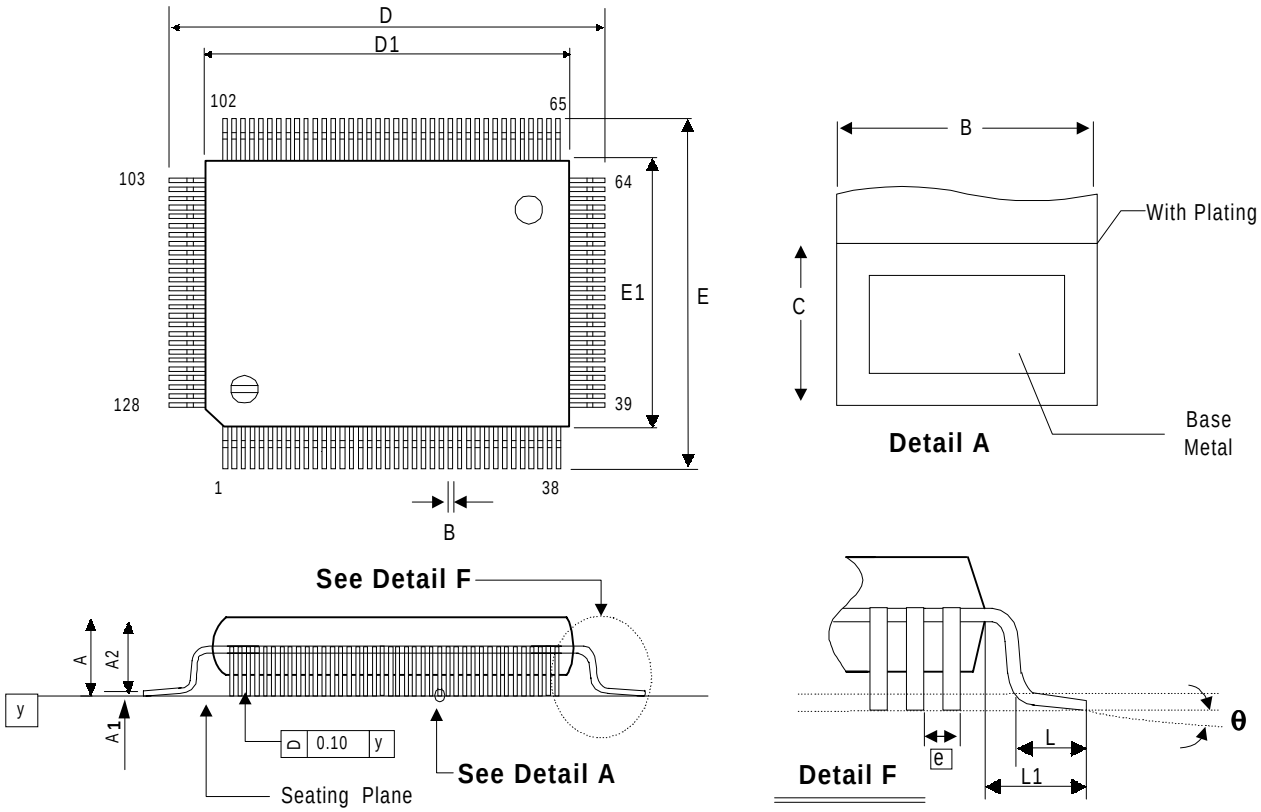



Clock Pulse
Data Pulse
Clock Pulse
FAST LINK PULSES
t1
t1
t2
t3
FLP Burst
FLP Burst
10TX0+/-
t4
t5

Package Information

QFP 128L Outline Dimensions

Unit: Inches/mm



Symbol	Dimension In Inch	Dimension In mm
A	0.134 Max.	3.40 Max.
A1	0.010 Min.	0.25 Min.
A2	0.112± 0.005	2.85± 0.12
B	0.009± 0.002	0.22±0.05
C	0.006± 0.002	0.145± 0.055
D	0.913± 0.007	23.20± 0.20
D1	0.787± 0.004	20.00 ± 0.10
E	0.677± 0.008	17.20± 0.20
E1	0.551± 0.004	14.00± 0.10
e	0.020 BSC	0.5 BSC
L	0.035± 0.006	0.88± 0.15
L1	0.063 BSC	1.60 BSC
y	0.004 Max.	0.10 Max.
θ	0°~12°	0°~12°

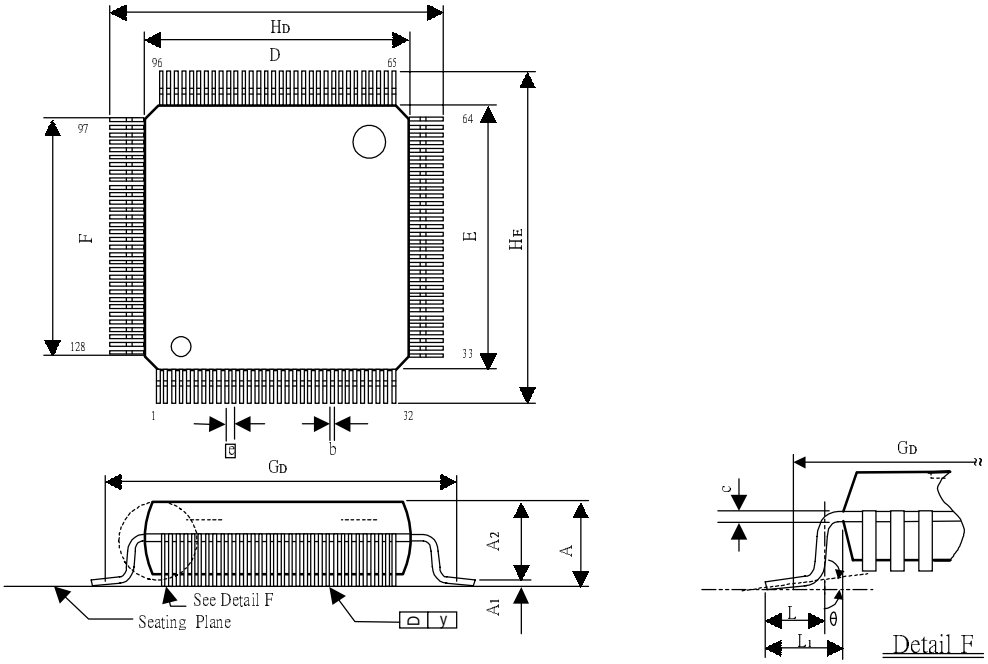
Note:

1. Dimension D1 and E1 do not include resin fins.
2. All dimensions are based on metric system.
3. General appearance spec. should base itself on final visual inspection spec.

Package Information

TQFP 128L Outline Dimensions

Unit: Inches/mm



Symbol	Dimensions In Inches	Dimensions In mm
A	0.047 Max.	1.20 Max.
A_1	0.004 ± 0.002	0.1 ± 0.05
A_2	0.039 ± 0.002	1.0 ± 0.05
b	$0.006\ ^{+0.003}_{-0.001}$	$0.16\ ^{+0.07}_{-0.03}$
c	0.006 ± 0.002	0.15 ± 0.05
D	0.551 ± 0.005	14.00 ± 0.13
E	0.551 ± 0.005	14.00 ± 0.13
e	0.016 BSC.	0.40 BSC.
F	0.494 NOM.	12.56 NOM.
G_D	0.606 NOM.	15.40 NOM.
H_D	0.630 ± 0.006	16.00 ± 0.15
H_E	0.630 ± 0.006	16.00 ± 0.15
L	0.024 ± 0.006	0.60 ± 0.15
L_1	0.039 Ref.	1.00 Ref.
y	0.003 Max.	0.08 Max.
θ	0° ~ 12°	0° ~ 12°

Note: 1. Dimension D & E do not include resin fins.
2. Dimension **e** is for PC Board surface mount, pad pitch design reference only.
3. All dimensions are based on metric system.

Ordering Information

Part Number	Pin Count	Package
DM9102AF	128	QFP
DM9102AT	128	TQFP

Disclaimer

The information appearing in this publication is believed to be accurate. Integrated circuits sold by DAVICOM Semiconductor are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. DAVICOM makes no warranty, express, statutory, implied or by description regarding the information in this publication or regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHER, DAVICOM MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. DAVICOM reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by DAVICOM for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

DAVICOM's terms and conditions printed on the order acknowledgment govern all sales by DAVICOM. DAVICOM will not be bound by any terms inconsistent with these unless DAVICOM agrees otherwise in writing. Acceptance of the buyer's orders shall be based on these terms.

Company Overview

DAVICOM Semiconductor, Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.

Contact Windows

For additional information about DAVICOM products, contact the sales department at:

Headquarters

Hsin-chu Office:
3F, No. 7-2, Industry E. Rd., IX,
Science-based Park,
Hsin-chu City, Taiwan, R.O.C.
TEL: 886-3-5798797
FAX: 886-3-5798858

Taipei Sales & Marketing Office:
8F, No. 3, Lane 235, Bao-chiao Rd.,
Hsin-tien City, Taipei, Taiwan, R.O.C.
TEL: 886-2-29153030
FAX: 886-2-29157575
Email: sales@davicom.com.tw

Davicom USA

Sunnyvale, California
1135 Kern Ave., Sunnyvale,
CA94085, U.S.A.
TEL: 1-408-7368600
FAX: 1-408-7368688
Email: sales@davicom8.com

WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.