General Description

The DM9101 is a physical-layer, single-chip, low-power transceiver for 100Base-TX, and 10Base-T operations. On the media side, it provides a direct interface either to Unshielded Twisted Pair Category 5 Cable (UTP5) for 100Base-TX Fast Ethernet, or UTP5/UTP3 Cable for 10Base-T Ethernet. Through the IEEE 802.3u Media Independent Interface (MII), the DM9101 connects to the Medium Access Control (MAC) layer, ensuring a high inter-operability among products from different vendors.

The DM9101 uses a low-power and high-performance CMOS process. It contains the entire physical layer functions of 100Base-TX as defined by IEEE 802.3u, including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), 100Base-TX Twisted Pair Physical Medium Dependent Sublayer (TP-PMD), and a 10Base-T Encoder/Decoder (ENC/DEC). The DM9101 provides strong support for the Auto-negotiation function utilizing automatic media speed and protocol selection. The DM9101 incorporates an internal wave-shaping filter to control rise/fall time, eliminating the need for external filtering on the 10/100Mbps signals.

Patent-Pending Circuitry Includes:

Smart adaptive receiver equalizer

Digital algorithm for high frequency clock/data recovery circuit

High speed wave-shaping circuit

Block Diagram

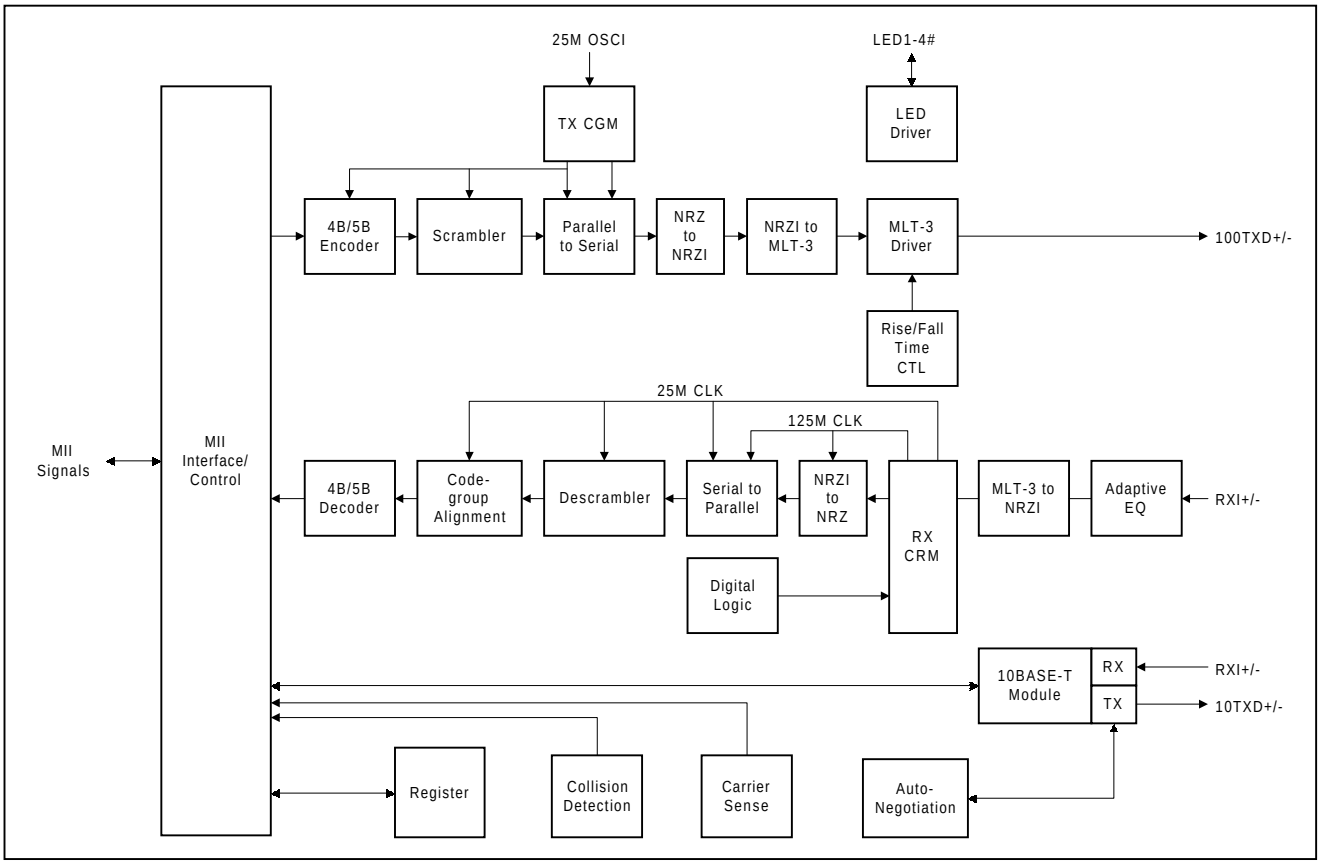
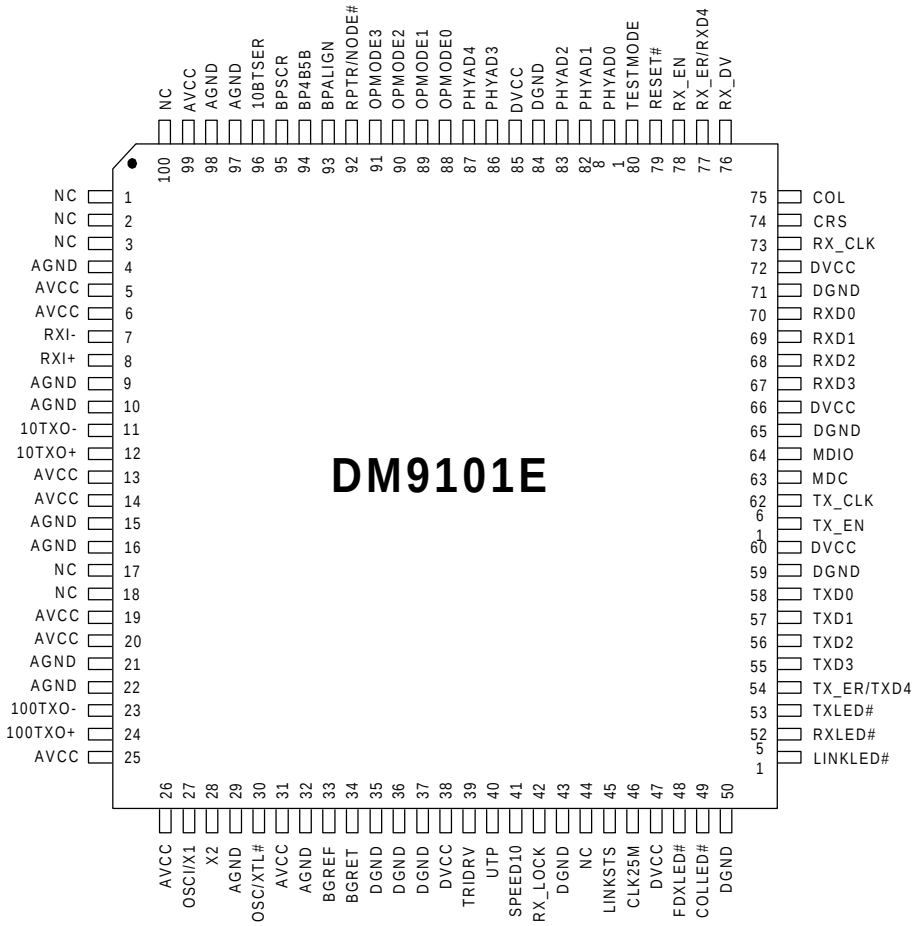


Table of Contents

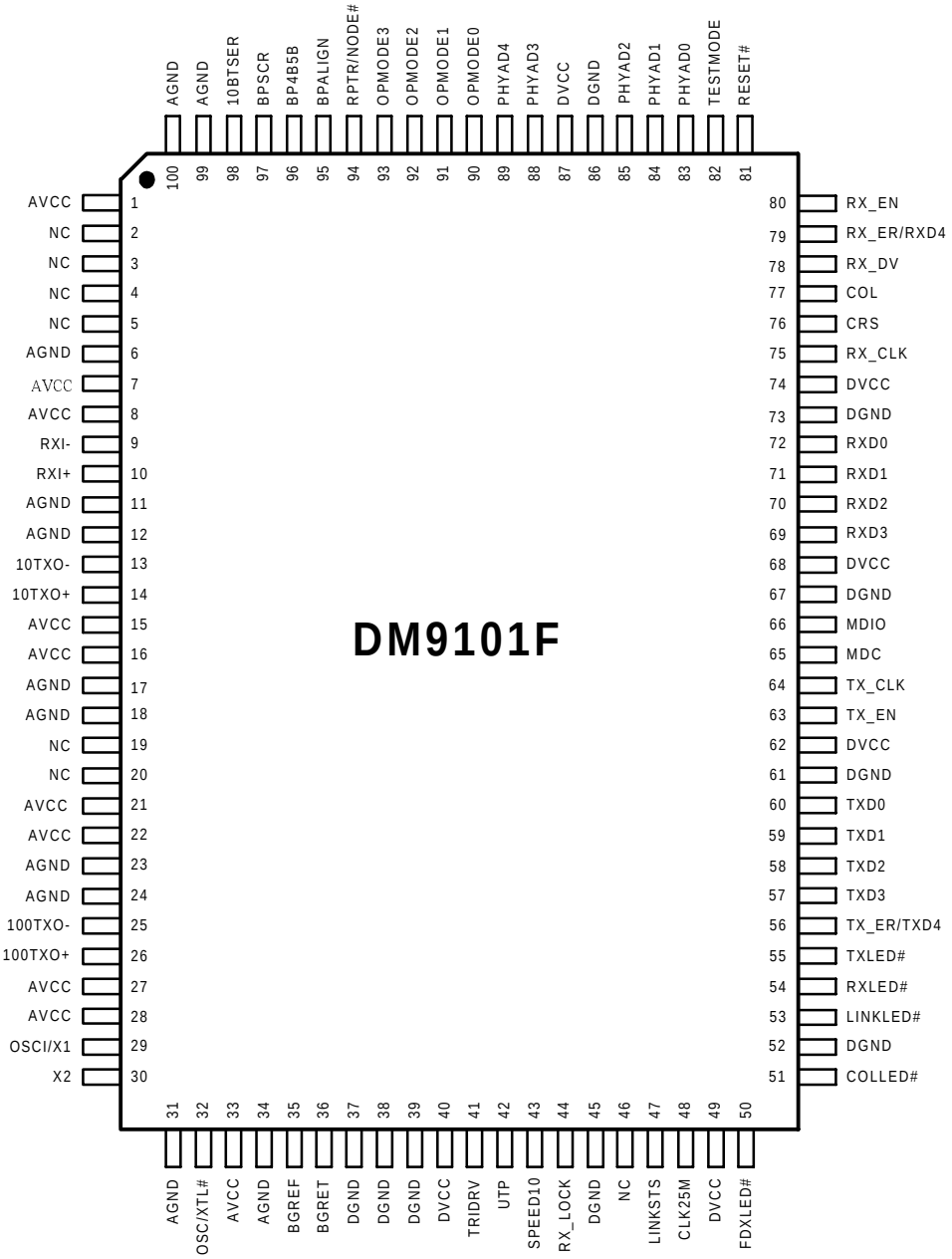
Features

- 10/100Base-TX physical-layer, single-chip transceiver
- Compliant with IEEE 802.3u 100Base-TX standard
- Compliant with ANSI X3T12 TP-PMD 1995 standard
- Compliant with IEEE 802.3u Auto-negotiation protocol for automatic link type selection
- Supports the MII with serial management interface
- Supports Full Duplex operation for 10 and 100Mbps
- High performance 100Mbps clock generator and data recovery circuitry
- Adaptive equalization circuitry for 100Mbps receiver
- Controlled output edge rates in 100Mbps
- Supports a 10Base-T interface without the need for an external filter
- Provides Loop-back mode for system diagnostics
- Includes Flexible LED configuration capability
- Digital clock recovery circuit using advanced digital algorithm to reduce jitter
- Low-power, high-performance CMOS process
- Available in both a 100 pin LQFP and a 100 QFP package

Pin Configuration: DM9101E LQFP



Pin Configuration: DM9101F QFP



Pin Description

Pin No.		Pin Name	I/O	Description
LQFP	QFP			
MII Interface				
54	56	TX_ER/ TXD4	I	**Transmit Error:** In 100Mbps mode, if this signal is asserted high and TX_EN is active, the HALT symbol is substituted for the actual data nibble. In 10Mbps mode, this input is ignored. In bypass modes (BP4B5B or BPALIGN), TX_ER becomes the TXD4 pin, the fifth TXD data bit.
55-58	57 - 60	TXD3 TXD2 TXD1 TXD0	I	**Transmit Data:** Transmit data input pins for nibble data from the MII in 100Mbps or 10Mbps nibble mode (25 MHz for 100Mbps mode, 2.5MHz for 10Mbps nibble mode). In 10Mbps serial mode, the TXD0 pin is used as the serial data input pin. TXD[3:1] are ignored.
61	63	TX_EN	I	**Transmit Enable:** Active high input indicates the presence of valid nibble data on TXD[3:0] for both 100Mbps or 10Mbps nibble mode. In 10Mbps serial mode, active high indicates the presence of valid 10Mbps data on TXD0.
62	64	TX_CLK	O,Z	**Transmit Clock:** Transmit clock output from the DM9101: - 25MHz nibble transmit clock derived from transmit Phase Locked Loop(TX PLL) in 100Base-TX mode - 2.5MHz transmit clock in 10Base-T nibble mode - 10MHz transmit clock in 10Base-T serial mode
63	65	MDC	I	**Management Data Clock:** Synchronous clock to the MDIO management data input/output serial interface which is asynchronous to transmit and receive clocks. The maximum clock rate is 2.5MHz.
64	66	MDIO	I/O	**Management Data I/O:** Bi-directional management instruction/data signal that may be driven by the station management entity or the PHY. This pin requires a 1.5KΩ pull-up resistor.
67-70	69 - 72	RXD3 RXD2 RXD1 RXD0	O,Z	**Receive Data:** Nibble wide receive data (synchronous to RX_CLK - 25MHz for 100Base-TX mode, 2.5MHz for 10Base-T nibble mode). Data is driven on the falling edge of RX_CLK. In 10Mbps serial mode, the RXD0 pin is used as the data output pin. RXD[3:1] are ignored.
73	75	RX_CLK	O,Z	**Receive Clock:** Provides the recovered receive clock for different modes of operation: - 25MHz nibble clock in 100Mbps mode - 2.5MHz nibble clock in 10Mbps nibble mode - 10MHz receive clock in 10Mbps serial mode

Pin Description (continued)

Pin No.		Pin Name	I/O	Description
LQFP	**QFP**			
MII Interface (continued)				
74	76	CRS	O,Z	**Carrier Sense:** This pin is asserted high to indicate the presence of carrier due to receive or transmit activities in 10Base-T or 100Base-TX Half Duplex modes. In Repeater, when Full Duplex or Loop-back mode is a logic 1, it indicates the presence of carrier due only to receive activity.
75	77	COL	O,Z	**Collision Detect:** Asserted high to indicate detection of collision conditions in 10Mbps and 100Mbps Half Duplex modes. In 10Base-T Half Duplex mode with Heartbeat set active (bit 13, register 18h), it is also asserted for a duration of approximately 1ms at the end of transmission to indicate heartbeat. In Full Duplex mode, this signal is always logic 0. There is no heartbeat function in Full-Duplex mode.
76	78	RX_DV	O,Z	**Receive Data Valid:** Asserted high to indicate that valid data is present on RXD[3:0].
77	79	RX_ER/ RXD4	O,Z	**Receive Error:** Asserted high to indicate that an invalid symbol has been detected inside a received packet in 100Mbps mode. In a bypass mode (BP4B5B or BPALIGN modes), RX_ER becomes RXD4, the fifth RXD data bit of the 5B symbols.
78	80	RX_EN	I	**Receive Enable:** Active high enabled for receive signals RXD[3:0], RX_CLK, RX_DV and RX_ER. A low on this input tri-states these output pins. For normal operation in a NODE application, this pin should be pulled high.
Media Interface				
7, 8	9, 10	RXI-, RXI+	I	**100/10Mbps Differential Input Pair:** These pins are the differential receive input for 10Base-T and 100Base-TX. They are capable of receiving 100Base-TX MLT-3 or 10Base-T Manchester encoded data.
11, 12	13, 14	10 TXO-, 10 TXO+	O	**10Base-T Differential Output Pair:** This output pair provides controlled rise and fall times designed to filter the transmitters output.
23, 24	25, 26	100 TXO-, 100 TXO+	O	**100Base-TX Differential Output Pair:** This output pair drives MLT-3 encoded data to the 100M twisted pair interface and provides controlled rise and fall times designed to filter the transmitter output, reducing any associated EMI.

Pin Description (continued)

Pin No.		Pin Name	I/O	Description
LQFP	QFP			
LED Interface : These outputs can directly drive LEDs or provide status information to a network management device.				
48	50	FDXLED# (POLLED)	O	**Polarity/Full Duplex LED:** Indicates Full Duplex mode status for 100Mbps and 10Mbps operation (Active low). If bit 4 of Register 16 (FDXLED_MODE) is set, the FDXLED# pin function will change to indicate the Polarity status for 10Mbps operation. If polarity is inverted, the POLLED will go ON.
49	51	COLLED#	O	**Collision LED:** Indicates the presence of collision activity for 10Mbps and 100Mbps operation. This LED has no meaning for 10Mbps or 100Mbps Full Duplex operation (Active low).
51	53	LINKLED# (TRAFFIC LED)	O	**Link LED:** Indicates Good Link status for 10Mbps and 100Mbps operation (Active low). It functions as the TRAFFIC LED when bit 5 of register 16 is set to 1. In TRAFFIC LED mode, it is always ON when the link is OK. The TRAFFIC LED flashes when transmitting or receiving.
52	54	RXLED#	OD	**Receive LED:** Indicates the presence of receive activity for 10Mbps and 100Mbps operation (Active low). The DM9101 incorporates a "monostable" function on the RXLED output. This ensures that even minimal receive activity will generate an adequate LED ON time.
53	55	TXLED#	OD	**Transmit LED:** Indicates the presence of transmit activity for 10Mbps and 100Mbps operation (Active low). The DM9101 incorporates a "monostable" function on the TXLED output. This ensures that even minimal transmit activity will generate an adequate LED ON time.
Device Configuration/Control/Status Interface				
40	42	UTP	O	**UTP Cable Indication:** UTP=1: Indicates UTP cable is used.
41	43	SPEED10	O	**Speed 10Mbps:** When set high, this bit indicates a 10Mbps operation, when set low 100Mbps operation. This pin can drive a low current LED to indicate that 100Mbps operation is selected.
42	44	RX_LOCK	O	**Lock for Clock/Data Recovery PLL:** When this pin is high it indicates that the receiver recovery PLL logic has locked to the input data stream.
45	47	LINKSTS	O	**Link Status Register Bit:** This pin reflects the status of bit 2 register 1.

Pin Description (continued)

<table>
<tr><th colspan="2">Pin No.</th><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><th>LQFP</th><th>QFP</th><th></th><th></th><th></th></tr>
<tr><td colspan="5">Device Configuration/Control/Status Interface (continued)</td></tr>
<tr><td>88-91</td><td>90 - 93</td><td>OPMODE0
OPMODE1
OPMODE2
OPMODE3</td><td>I</td><td>OPMODE0 - OPMODE3:
These pins are used to control the forced or advertised operating mode of the DM9101 (see table below). The value is latched into the DM9101 registers at power-up/reset.
<table>
<tr><th>OPMODE3</th><th>OPMODE2</th><th>OPMODE1</th><th>OPMODE0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Auto-neg enable with all capabilities with Flow Control</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Auto-neg enable without all capabilities without Flow Control</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Auto-neg 100TX FDX with Flow Control only</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Auto-neg 100TX FDX/HDX without Flow Control</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Auto-neg 10TP FDX with Flow Control only</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Auto-neg 10TX FDX/HDX without Flow Control</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Manual select 100TX FDX</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Manual select 100TX HDX</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Manual select 10TX FDX</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Manual select 10TX HDX</td></tr>
</table></td></tr>
<tr><td>92</td><td>94</td><td>RTPR/NODE#</td><td>I</td><td>Repeater/Node Mode:
When set high, this bit selects REPEATER mode; when set low, it selects NODE. In REPEATER mode or NODE mode with Full Duplex configured, the Carrier Sense (CRS) output from the DM9101 will be asserted only during receive activity. In NODE mode or a mode not configured for Full Duplex operation, CRS will be asserted during receive or transmit activity. At power-up/reset, the value on this pin is latched into Register 16, bit 11.</td></tr>
<tr><td>93</td><td>95</td><td>BPALIGN</td><td>I</td><td>Bypass Alignment:
Allows 100Mbps transmit and receive data streams to bypass all of the transmit and receive operations when set high.
At power-up/reset, the value on this pin is latched into bit Register 16 ,bit 13.</td></tr>
</table>

Pin Description (continued)

Pin No.		Pin Name	I/O	Description
LQFP	QFP			
Device Configuration/Control/Status Interface (continued)				
94	96	BP4B5B	I	**Bypass 4B5B Encoder/Decoder:** Allows 100Mbps transmit and receive data streams to bypass the 4B to 5B encoder and 5B to 4B decoder circuits when set high At power-up/reset, the value on this pin is latched into Register 16, bit 15.
95	97	BPSCR	I	**Bypass Scrambler/Descrambler:** Allows 100Mbps transmit and receive data streams to bypass the scrambler and descrambler circuits when set high. At power-up/reset, the value on this pin is latched into Register 16, bit 14.
96	98	10BTSER	I	**Serial/Nibble Select:** 10Mbps Serial Operation: When set high, this input selects a serial data transfer mode. Manchester encoded transmit and receive data is exchanged serially with a 10MHz clock rate on the least significant bits of the nibble-wide MII data buses, pin TXD[0] and RXD[0] respectively. This mode is intended for use with the DM9101 connected to a device (MAC or Repeater) that has a 10Mbps serial interface. Serial operation is not supported in 100Mbps mode. For 100Mbps, this input is ignored. 10 and 100Mbps Nibble Operation: When set low, this input selects the MII compliant nibble data transfer mode. Transmit and receive data is exchanged in nibbles on the TXD[3:0] and RXD[3:0] pins respectively. At power-up/reset, the value on this pin is latched into Register 18, bit 10.
Clock Interface				
27	29	OSCI/X1	I	**Crystal or Oscillator Input:** This pin should be connected to a 25MHz (±50 ppm) crystal if OSC/XTL#=0 or a 25MHz (±50ppm) external TTL oscillator input, if OSC/XTLB=1.
28	30	X2	O	**Crystal Oscillator Output:** An external 25MHz (±50 ppm) crystal should be connected to this pin if OSC/XTL#=0, or left unconnected if OSC/XTL#=1.
30	32	OSC/XTL#	I	**Crystal or Oscillator Selector Pin:** OSC/XTL#=0: An external 25MHz (±50ppm) crystal should be connected to X1 and X2 pins. OSC/XTL#=1: An external 25MHz (±50ppm) oscillator should be connected to X1 and X2 should be left unconnected.
46	48	CLK25M	O,Z	**25MHz Clock Output:.** This clock is derived directly from the crystal circuit.

Pin Description (continued)

Pin No.		Pin Name	I/O	Description
LQFP	**QFP**			
PHY Address Interface: PHYAD[4:0] provides up to 32 unique PHY address. An address selection of all zeros (00000) will result in a PHY isolation condition. See the isolate bit description in the BMCR, address 00.				
81	83	PHYAD0	I	**PHY Address 0:** PHY address bit 0 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 8 during power up/reset.
82	84	PHYAD1	I	**PHY Address 1:** PHY address bit 1 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 7 during power up/reset.
83	85	PHYAD2	I	**PHY Address 2:** PHY address bit 2 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 6 during power up/reset.
86	88	PHYAD3	I	**PHY Address 3:** PHY address bit 3 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 5 during power up/reset.
87	89	PHYAD4	I	**PHY Address 4:** PHY address bit 4 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 4 during power up/reset.
Miscellaneous				
1-3, 17, 18, 44, 100	2 - 5, 19, 20, 46	NC		**No Connect:** Leave these pins unconnected (floating).
33	35	BGREF	I	**Bandgap Voltage Reference:** Connect a 6.01KΩ, 1% resistor between this pin and the BGRET pin to provide an accurate current reference for the DM9101.
34	36	BGRET	I	**Bandgap Voltage Reference Return:** Return pin for 6.01KΩ resistor connection.
39	41	TRIDRV	I	**Tri-state Digital Output Pins:** When set high, all digital output pins are set to a high impedance state, and I/O pins, go to input mode.
79	81	RESET#	I	**Reset:** Active Low input that initializes the DM9101. It should remain low for 30ms after VCC has stabilized at 5Vdc (normal) before it transitions high.
80	82	TESTMODE	I	**Test Mode Control Pin:** TESTMODE=0: Normal operating mode. TESTMODE=1: Enable test mode.

Pin Description (continued)

Power and Ground Pins :
The power (VCC) and ground (GND) pins of the DM9101 are grouped in pairs of two categories - Digital Circuitry Power/Ground Pairs and Analog Circuitry Power/Ground Pair.

Pin No.		Pin Name	I/O	Description
LQFP	**QFP**			
Group A - Digital Supply Pairs				
35, 36, 37, 43, 50, 59, 65, 71, 84	37, 38, 39, 45, 52, 61, 67, 73, 86	DGND	P	Digital Logic Ground.
Group A - Digital Supply Pairs (continued)				
38, 47, 60, 72, 66, 85	40, 49, 62, 74, 68, 87	DVCC	P	Digital Logic power supply
Group B - Analog Circuit Supply Pairs				
4, 9, 10, 15, 16, 21, 22, 29, 32, 97, 98	6, 11, 12, 18, 17, 23, 24, 31, 34, 99, 100	AGND	P	Analog circuit ground
5, 6, 13, 14, 19, 20, 25, 26, 31, 99	1, 7, 8, 15, 16, 21, 22, 27, 28, 33	AVCC	P	Analog circuit power supply

Functional Description

The DM9101 Fast Ethernet single-chip transceiver, provides the functionality as specified in IEEE 802.3u, integrates a complete 100Base-TX module and a complete 10Base-T module. The DM9101 provides a Media Independent Interface (MII) as defined in the IEEE 802.3u standard (Clause 22).

The DM9101 performs all PCS (Physical Coding Sublayer), PMA (Physical Media Access), TP-PMD (Twisted Pair Physical Medium Dependent) sublayer, 10Base-T Encoder/Decoder, and Twisted Pair Media Access Unit (TPMAU) functions. Figure 1 shows the major functional blocks implemented in the DM9101.

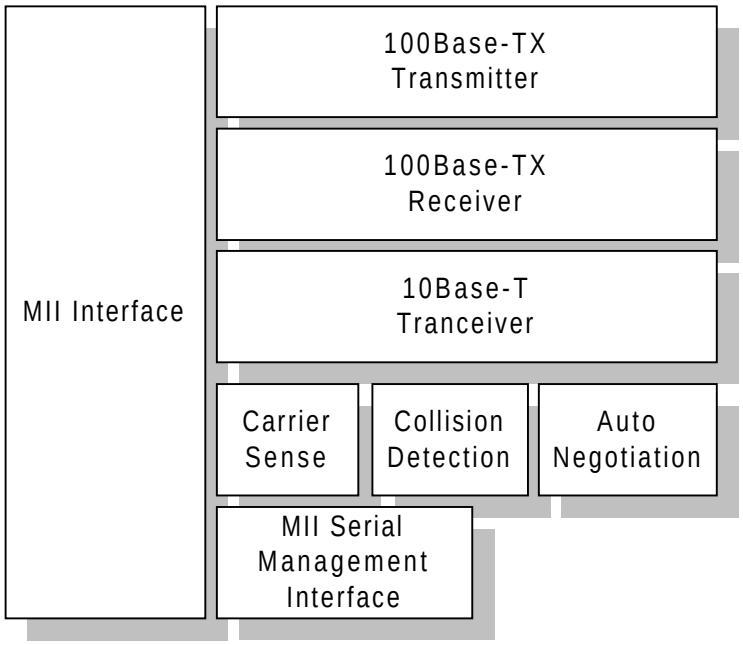


Figure 1

MII Interface

The DM 9101 provides a Media Independent Interface (MII) as defined in the IEEE 802.3u standard (Clause 22).
The purpose of the MII interface is to provide a simple, easy to implement connection between the MAC Reconciliation layer and the PHY. The MII is designed to make the differences between various media transparent to the MAC sublayer.
The MII consists of a nibble wide receive data bus, a nibble wide transmit data bus, and control signals to facilitate data transfers between the PHY and the Reconciliation layer.

- TXD (transmit data) is a nibble (4 bits) of data that are driven by the reconciliation sublayer synchronously with respect to TX_CLK. For each TX_CLK period which TX_EN is asserted, TXD (3:0) are accepted for transmission by the PHY.
- TX_CLK (transmit clock) output to the MAC reconciliation sublayer is a continuous clock that provides the timing reference for the transfer of the TX_EN, TXD, and TX_ER signals.
- TX_EN (transmit enable) input from the MAC reconciliation sublayer to indicate nibbles are being presented on the MII for transmission on the physical medium.

- **MII Interface** (continued)
- TX_ER (transmit coding error) transitions synchronously with respect to TX_CLK. If TX_ER is asserted for one or more clock periods, and TX_EN is asserted, the PHY will emit one or more symbols that are not part of the valid data delimiter set somewhere in the frame being transmitted.
- RXD (receive data) is a nibble (4 bits) of data that are sampled by the reconciliation sublayer synchronously with respect to RX_CLK. For each RX_CLK period which RX_DV is asserted, RXD (3:0) are transferred from the PHY to the MAC reconciliation sublayer.
- RX_CLK (receive clock) output to the MAC reconciliation sublayer is a continuous clock that provides the timing reference for the transfer of the RX_DV, RXD, and RX_ER signals.
- RX_DV (receive data valid) input from the PHY to indicate the PHY is presenting recovered and decoded nibbles to the MAC reconciliation sublayer. To interpret a receive frame correctly by the reconciliation sublayer, RX_DV must encompass the frame starting no later than the Start-of-Frame delimiter and excluding any End-Stream delimiter.
- RX_ER (receive error) transitions synchronously with respect to RX_CLK. RX_ER will be asserted for 1 or more clock periods to indicate to the reconciliation sublayer that an error was detected somewhere in the frame being transmitted from the PHY to the reconciliation sublayer.
- CRS (carrier sense) is asserted by the PHY when either the transmit or receive medium is non-idle and deasserted by the PHY when the transmit and receive medium are idle. Figure 2 depicts the behavior of CRS during 10Base-T and 100Base-TX transmission.

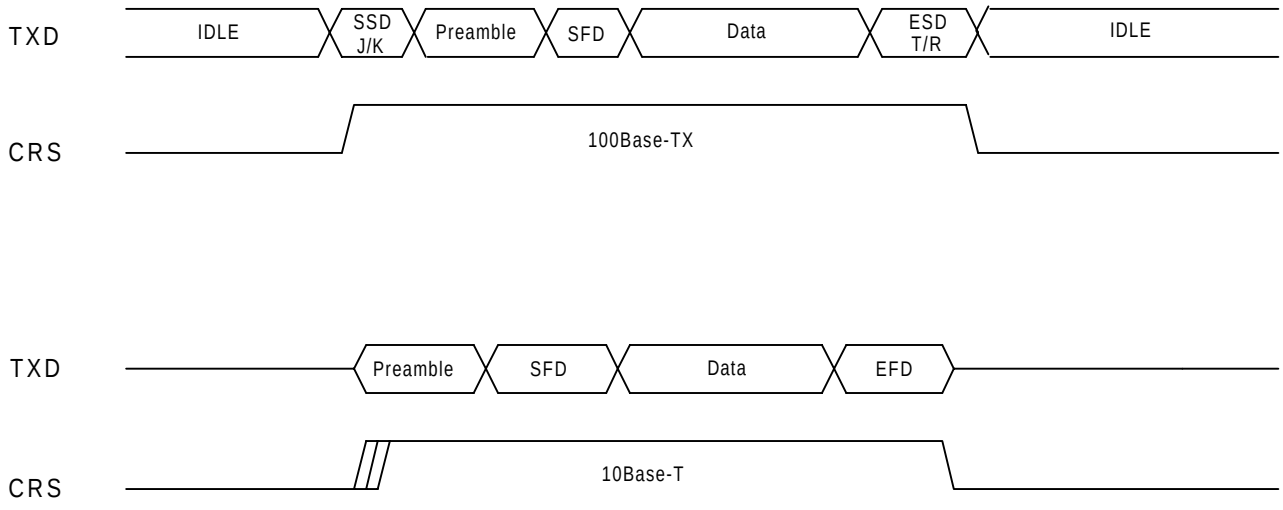


Figure 2

100Base-TX Operation

The 100Base-TX transmitter receives 4-bit nibble data clocked in at 25MHz at the MII, and outputs a scrambled 5-bit encoded MLT-3 signal to the media at 100Mbps. The on-chip clock circuit converts the 25MHz clock into a 125MHz clock for internal use.

The IEEE 802.3u specification defines the Media Independent Interface. The interface specification defines a dedicated receive data bus and a dedicated transmit data bus.

These two busses include various controls and signal indications that facilitate data transfers between the DM9101 and the Reconciliation layer.

100Base-TX Transmit

The 100Base-TX transmitter consists of the functional blocks shown in figure 3. The 100Base-TX transmit section converts 4-bit synchronous data provided by the MII to a scrambled MLT-3 125 million symbols per second serial data stream.

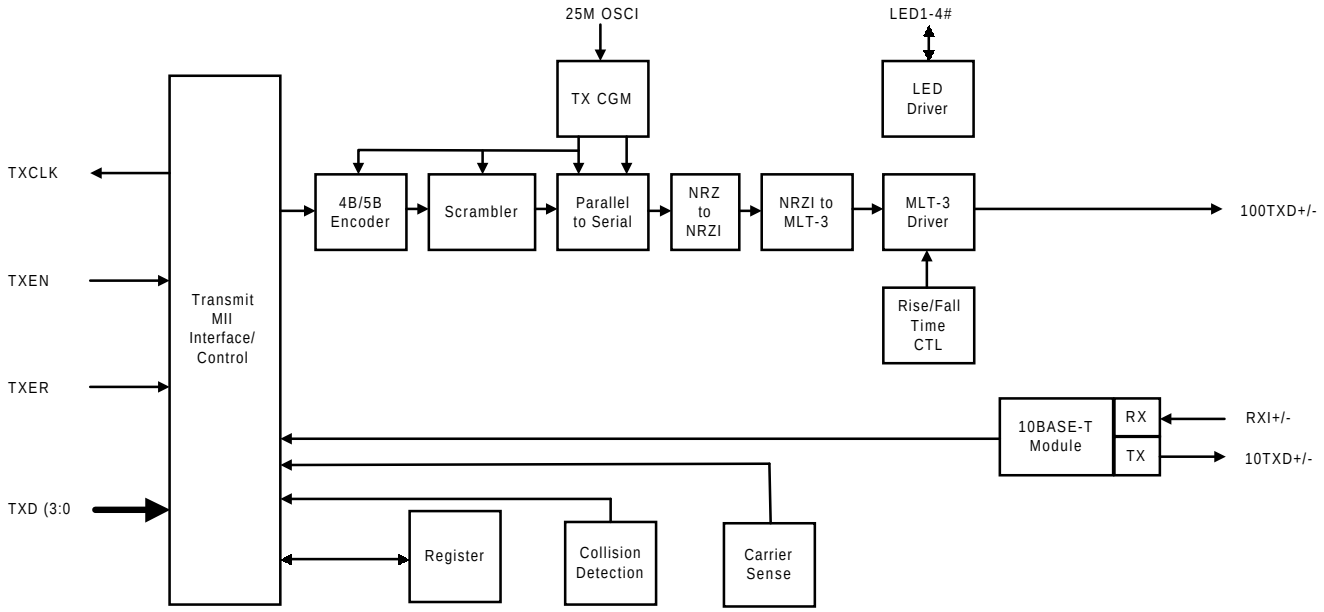


Figure 3

100Base-TX Operation

The block diagram in figure 3 provides an overview of the functional blocks contained in the transmit section. The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Converter
- NRZI to MLT-3
- MLT-3 Driver

4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

The DM9101 includes a Bypass 4B5B conversion option within the 100Base-TX Transmitter for support of applications like 100 Mbps repeaters which do not require 4B5B conversion.

Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to repeated 5B sequences like continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI Encoder block

NRZ to NRZI Encoder

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable.

MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events.

MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver which converts these streams to current sources and alternately drives either side of the transmit transformer primary winding resulting in a minimal current MLT-3 signal. Refer to figure 4 for the block diagram of the MLT-3 converter.

4B5B Code Group

Symbol	Meaning	4B code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Table 1

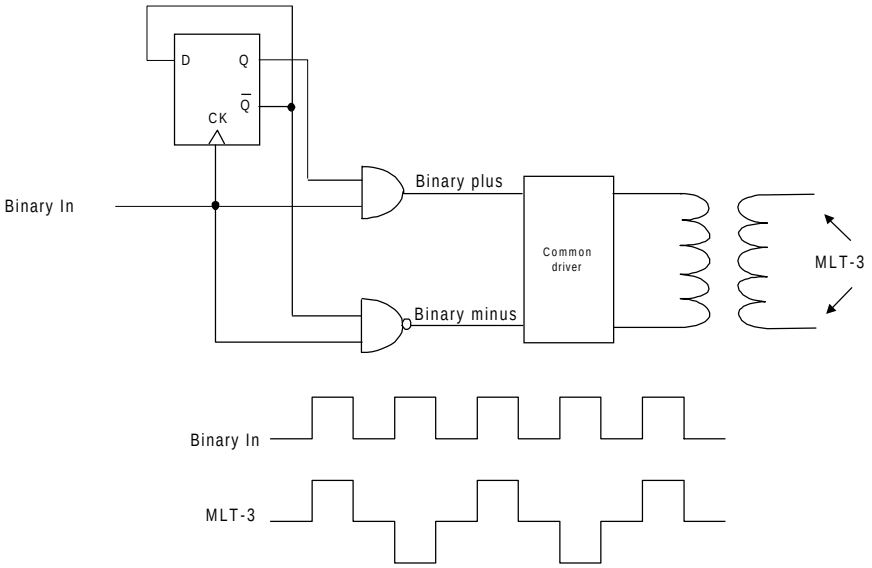


Figure 4

100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data that is then provided to the MII.
The receive section contains the following functional blocks:

- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

Signal Detect

The signal detect function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX Standards for both voltage thresholds and timing parameters.

Digital Adaptive Equalization

When transmitting data at high speeds over copper twisted pair cable, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation caused by frequency variations must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation, requires significant compensation which will be over-kill in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

MLT-3 to NRZI Decoder

The DM9101 decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data. The relationship between NRZI and MLT-3 data is shown in figure 4.

Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125Mhz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ Decoder.

NRZI to NRZ

The transmit data stream is required to be NRZI encoded in for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder, receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter, and converts the data stream to parallel data to be presented to the descrambler.

Descrambler

Because of the scrambling process required to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, descrambles the data streams, and presents the data streams to the Code Group alignment block.

Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected, and subsequent data is aligned on a fixed boundary.

4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups received are the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R symbols). The T/R symbol pair is also stripped from the nibble presented to the Reconciliation layer.

10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM9101 is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented to the MII interface in nibble format, converted to a serial bit stream, then Manchester encoded. When receiving, the Manchester encoded bit stream is decoded and converted into nibble format for presentation to the MII interface.

Collision Detection

For half-duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. When a collision has been detected, it will be reported by the COL signal on the MII interface. Collision detection is disabled in Full Duplex operation.

Carrier Sense

Carrier Sense (CRS) is asserted in half-duplex operation during transmission or reception of data. During full-duplex mode, CRS is asserted only during receive operations.

Auto-Negotiation

The objective of Auto-negotiation is to provide a means to exchange information between segment linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-negotiation does not test the link segment characteristics. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

Auto-Negotiation (continued)

Auto-negotiation also provides a parallel detection function for devices that do not support the Auto-negotiation feature. During Parallel detection there is no exchange of configuration information, instead, the receive signal is examined. If it is discovered that the signal matches a technology that the receiving device supports, a connection will be automatically established using that technology. This allows devices that do not support Auto-negotiation but support a common mode of operation to establish a link.

MII Serial Management

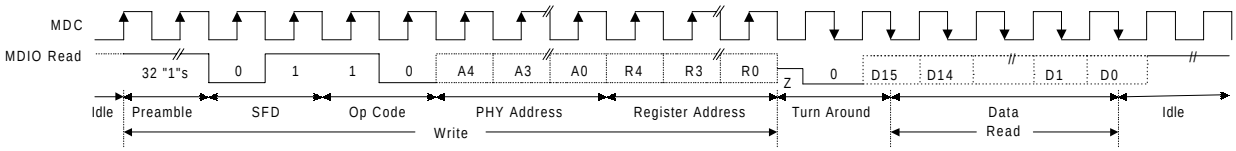
The MII serial management interface consists of a data interface, basic register set, and a serial management interface to the register set. Through this interface it is possible to control and configure multiple PHY devices, get status and error information, and determine the type and capabilities of the attached PHY device(s).
The DM9101 management functions correspond to MII specification for IEEE 802.3u-1995 (Clause 22) for registers 0 through 6 with vendor-specific registers 16,17, and 18.

In read/write operation, the management data frame is 64-bits long and starts with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP):<10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) filing between Register Address field and Data field is provided for MDIO to avoid contention. Following the turnaround time, 16-bit data is read from or written onto management registers.

Serial Management Interface

The serial control interface uses a simple two-wired serial interface to obtain and control the status of the physical layer through the MII interface. The serial control interface consists of MDC (Management Data Clock), and MDI/O (Management Data Input/Output) signals.
The MDIO pin is bi-directional and may be shared by up to 32 devices.

Management Interface - Read Frame Structure



Management Interface - Write Frame Structure

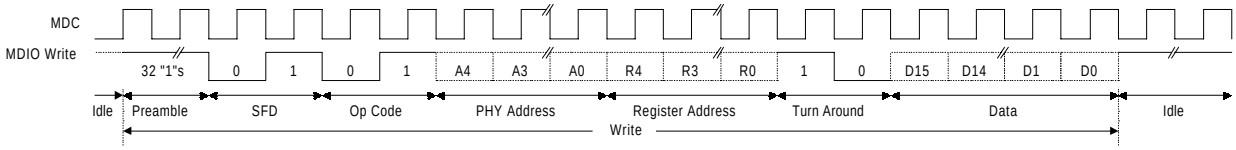


Figure 5

Register Description

Register Address	Register Name	Description
0	BMCR	Basic Mode Control Register
1	BMSR	Basic Mode Status Register
2	PHYIDR1	PHY Identifier Register #1
3	PHYIDR2	PHY Identifier Register #2
4	ANAR	Auto-Negotiation Advertisement Register
5	ANLPAR	Auto-Negotiation Link Partner Ability Register
6	ANER	Auto-Negotiation Expansion Register
16	DSCR	DAVICOM Specified Configuration Register
17	DSCSR	DAVICOM Specified Configuration/Status Register
18	10BTCSR	10Base-T Configuration/Status Register
Others	Reserved	Reserved For Future Use-Do Not Read/Write To These Registers

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type> / <Attribute(s)>
Where
<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value
(PIN#)	Value latched in from pin # at reset

<Access Type>:
RO = Read only
RW = Read/Write

<Attribute (s)>:
SC = Self clearing
P = Value permanently set
LL = Latching low
LH = Latching high

Basic Mode Control Register (BMCR) - Register 0

Bit	Bit Name	Default	Description
0.15	Reset	0, RW/SC	**Reset:** 1=Software reset 0=Normal operation When set this bit configures the PHY status and control registers to their default states. This bit will return a value of one until the reset process is complete
0.14	Loopback	0, RW	**Loopback:** Loopback control register 1=Loopback enabled 0=Normal operation When in 100M operation is selected, setting this bit will cause the descrambler to lose synchronization. A 720ms "dead time" will occur before any valid data appears at the MII receive outputs
0.13	Speed Selection	1, RW	**Speed Select:** 1=100Mbps 0=10Mbps Link speed may be selected either by this bit or by Auto-negotiation if bit 12 of this register is set. When Auto-negotiation is enabled, this bit will return Auto-negotiation link speed.
0.12	Auto-negotiation Enable	1, RW	**Auto-negotiation Enable:** 1= Auto-negotiation enabled: 0= Auto-negotiation disabled: When auto-negotiation is enabled bits 8 and 13 will contain the Auto-negotiation results. When Auto-negotiation is disabled bits 8 and 13 will determine the duplex mode and link speed
0.11	Power Down	0, RW	**Power Down:** 1=Power Down 0=Normal Operation Setting this bit will power down the DM9101 with the exception of the crystal oscillator circuit
0.10	Isolate	(PHYAD= 00000), RW	**Isolate:** 1= Isolate 0= Normal Operation When this bit is set the data path will be isolated from the MII interface. TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL and CRS will be placed in a high impedance state. The management interface is not effected by this bit. When the PHY Address is set to 00000 the isolate bit will be set upon power-up/reset

Basic Mode Control Register (BMCR) - Register 0 (continued)

Bit	Bit Name	Default	Description
0.9	Restart Auto-negotiation	0,RW/SC	**Restart Auto-negotiation:** 1= Restart Auto-negotiation. 0= Normal Operation When this bit is set the Auto-negotiation process is re-initiated. When Auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and will return a value of 1 until Auto-negotiation is initiated. The operation of the Auto-negotiation process will not be affected by the management entity that clears this bit
0.8	Duplex Mode	1,RW	**Duplex Mode:** 1= Full Duplex operation. 0= Normal operation If Auto-negotiation is disabled, setting this bit will cause the DM9101 to operate in full duplex mode. When Auto-negotiation is enabled, this bit reflects the duplex selected by Auto-negotiation
0.7	Collision Test	0,RW	**Collision Test:** 1= Collision Test enabled. 0= Normal Operation When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN
0.6	Reserved	0,RO	**Reserved:** Write as 0, ignore on read

Basic Mode Status Register (BMSR) - Register 1

Bit	Bit Name	Default	Description
1.15	100Base-T4	0,RO/P	**100Base-T4 Capable:** 1=DM9101 is able to perform in 100Base-T4 mode 0=DM9101 is not able to perform in 100Base-T4 mode
1.14	100Base-TX Full Duplex	1,RO/P	**100Base-TX Full Duplex Capable:** 1= DM9101 is able to perform 100Base-TX in Full Duplex mode 0= DM9101 is not able to perform 100Base-TX in Full Duplex mode
1.13	100Base-TX Half Duplex	1,RO/P	**100Base-TX Half Duplex Capable:** 1=DM9101 is able to perform 100Base-TX in Half Duplex mode 0=DM9101 is not able to perform 100Base-TX in Half Duplex mode
1.12	10Base-T Full Duplex	1,RO/P	**10Base-T Full Duplex Capable:** 1=DM9101 is able to perform 10Base-T in Full Duplex mode 0=DM9101 is not able to perform 10Base-T in Full Duplex mode
1.11	10Base-T Half Duplex	1,RO/P	**10Base-T Half Duplex Capable:** 1=DM9101 is able to perform 10Base-T in Half Duplex mode 0=DM9101 is not able to perform 10Base-T in Half Duplex mode.
1.10-1.7	Reserved	0,RO	**Reserved:** Write as 0, ignore on read

Basic Mode Status Register (BMSR) - Register 1 (continued)

Bit	Bit Name	Default	Description
1.6	MF Preamble Suppression	0,RO	**MII Frame Preamble Suppression:** 1=PHY will accept management frames with preamble suppressed 0=PHY will not accept management frames with preamble suppressed
1.5	Auto-negotiation Complete	0,RO	**Auto-negotiation Complete:** 1=Auto-negotiation process completed 0=Auto-negotiation process not completed
1.4	Remote Fault	0, RO/LH	**Remote Fault:** 1= Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM9101 implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0= No remote fault condition detected
1.3	Auto-negotiation Ability	1,RO/P	**Auto Configuration Ability:** 1=DM9101 able to perform Auto-negotiation 0=DM9101 not able to perform Auto-negotiation
1.2	Link Status	0,RO/LL	**Link Status:** 1=Valid link established (for either 10Mbps or 100Mbps operation) 0=Link not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the Link Status bit to be cleared and remain cleared until it is read via the management interface
1.1	Jabber Detect	0, RO/LH	**Jabber Detect:** 1=Jabber condition detected 0=No jabber condition detected This bit is implemented with a latching function. Once Jabber conditions are detected this bit will remain set until a read operation is completed through a management interface or a DM9101 reset. This bit works only in 10Mbps mode
1.0	Extended Capability	1,RO/P	**Extended Capability:** 1=Extended register capable 0=Basic register capable only

PHY ID Identifier Register #1 (PHYIDR1) - Register 2

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9101. The Identifier consists of a concatenation of the **Organizationally Unique Identifier** (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Bit Name	Default	Description
2.15-2.0	OUI_MSB	<0181H>	**OUI Most Significant Bits:** This register stores bits 3 - 18 of the OUI (00606E) to bits 15 - 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

PHY Identifier Register #2 (PHYIDR2) - Register 3

Bit	Bit Name	Default	Description
3.15-3.10	OUI_LSB	<101110>,RO/P	**OUI Least Significant Bits:** Bits 19 - 24 of the OUI (00606E) are mapped to bits 15 - 10 of this register respectively
3.9-3.4	VNDR_MDL	<000000>,RO/P	**Vendor Model Number:** Six bits of the vendor model number mapped to bits 9 - 4 (most significant bit to bit 9)
3.3-3.0	MDL_REV	<0010>,RO/P	**Model Revision Number:** Four bits of the vendor model revision number mapped to bits 3 - 0 (most significant bit to bit 3)

Auto-negotiation Advertisement Register (ANAR) - Register 4

This register contains the advertised abilities of the DM9101 device as they will be transmitted to link partners during Auto-negotiation.

Bit	Bit Name	Default	Description
4.15	NP	0,RO/P	**Next Page Indication:** 0=No next page available 1=Next page available The DM9101 does not support the next page function. This bit is permanently set to 0
4.14	ACK	0,RO	**Acknowledge:** 1=Link partner ability data reception acknowledged 0=Not acknowledged The DM9101's Auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the Auto-negotiation process. Software should not attempt to write to this bit.
4.13	RF	0, RW	**Remote Fault:** 1=Local Device senses a fault condition 0=No fault detected
4.12-4.11	Reserved	X, RW	**Reserved:** Write as 0, ignore on read
4.10	FCS	0, RW	**Flow Control Support:** 1=Controller chip supports flow control ability 0=Controller chip doesn't support flow control ability
4.9	T4	0, RO/P	**100Base-T4 Support:** 1=100Base-T4 supported by the local device 0=100Base-T4 not supported The DM9101 does not support 100Base-T4 so this bit is permanently set to 0
4.8	TX_FDX	1, RW	**100Base-TX Full Duplex Support:** 1=100Base-TX Full Duplex supported by the local device 0=100Base-TX Full Duplex not supported
4.7	TX_HDX	1, RW	**100Base-TX Support:** 1=100Base-TX supported by the local device 0=100Base-TX not supported

Auto-negotiation Advertisement Register (ANAR) - Register 4 (continued)

Bit	Bit Name	Default	Description
4.6	10_FDX	1, RW	**10Base-T Full Duplex Support:** 1=10Base-T Full Duplex supported by the local device 0=10Base-T Full Duplex not supported
4.5	10_HDX	1, RW	**10Base-T Support:** 1=10Base-T supported by the local device 0=10Base-T not supported
4.4-4.0	Selector	<00001>, RW	**Protocol Selection Bits:** These bits contain the binary encoded protocol selector supported by this node. <00001> indicates that this device supports IEEE 802.3 CSMA/CD.

Auto-negotiation Link Partner Ability Register (ANLPAR) - Register 5

This register contains the advertised abilities of the link partner as they are received during Auto-negotiation.

Bit	Bit Name	Default	Description
5.15	NP	0, RO	**Next Page Indication:** 0= Link partner, no next page available 1= Link partner, next page available
5.14	ACK	0, RO	**Acknowledge:** 1=Link partner ability data reception acknowledged 0=Not acknowledged The DM9101's Auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit.
5.13	RF	0, RO	**Remote Fault:** 1=Remote fault indicated by link partner 0=No remote fault indicated by link partner
5.12-5.10	Reserved	X, RO	**Reserved:** Write as 0, ignore on read
5.9	T4	0, RO	**100Base-T4 Support:** 1=100Base-T4 supported by the link partner 0=100Base-T4 not supported by the link partner
5.8	TX_FDX	0, RO	**100Base-TX Full Duplex Support:** 1=100Base-TX Full Duplex supported by the link partner 0=100Base-TX Full Duplex not supported by the link partner
5.7	TX_HDX	0, RO	**100Base-TX Support:** 1=100Base-TX Half Duplex supported by the link partner 0=100Base-TX Half Duplex not supported by the link partner
5.6	10_FDX	0, RO	**10Base-T Full Duplex Support:** 1=10Base-T Full Duplex supported by the link partner 0=10Base-T Full Duplex not supported by the link partner
5.5	10_HDX	0, RO	**10Base-T Support:** 1=10Base-T Half Duplex supported by the link partner 0=10Base-T Half Duplex not supported by the link partner
5.4-5.0	Selector	<00000>, RO	**Protocol Selection Bits:** Link partner binary encoded protocol selector

Auto-negotiation Expansion Register (ANER) - Register 6

Bit	Bit Name	Default	Description
6.15-6.5	Reserved	X, RO	**Reserved:** Write as 0, ignore on read
6.4	PDF	0, RO/LH	**Local Device Parallel Detection Fault:** PDF=1: A fault detected via parallel detection function. PDF=0: No fault detected via parallel detection function
6.3	LP_NP_ABLE	0, RO	**Link Partner Next Page Able:** LP_NP_ABLE=1: Link partner, next page available LP_NP_ABLE=0: Link partner, no next page
6.2	NP_ABLE	0,RO/P	**Local Device Next Page Able:** NP_ABLE=1: DM9101, next page available NP_ABLE=0: DM9101, no next page DM9101 does not support this function, so this bit is always 0.
6.1	PAGE_RX	0, RO/LH	**New Page Received:** A new link code word page received. This bit will be automatically cleared when the register (Register 6) is read by management.
6.0	LP_AN_ABLE	0, RO	**Link Partner Auto-negotiation Able:** LP_AN_ABLE=1 indicates that the link partner supports Auto-negotiation.

DAVICOM Specified Configuration Register (DSCR) - Register 16

Bit	Bit Name	Default	Description
16.15	BP_4B5B	Pin96, RW	**Bypass 4B5B Encoding and 5B4B Decoding:** 1=4B5B encoder and 5B4B decoder function bypassed 0=Normal 4B5B and 5B4B operation The value of the pin is latched into this bit at power-up/reset.
16.14	BP_SCR	Pin97, RW	**Bypass Scrambler/Descrambler Function:** 1=Scrambler and descrambler function bypassed 0=Normal scrambler and descrambler operation The value of the input pin is latched into this bit at power-up/reset.
16.13	BP_ALIGN	Pin95, RW	**Bypass Symbol Alignment Function:** 1= Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0= Normal operation The value of the BPALIGN input pin is latched into this bit at power-up/reset.
16.12	Reserved	0, RW	**Reserved:** This bit must be set as 0.

DAVICOM Specified Configuration Register (DSCR) - Register 16 (continued)

Bit	Bit Name	Default	Description
16.11	REPEATER	0, RW	**Repeater/Node Mode:** 1=Repeater mode 0=Node mode In Repeater mode, the Carrier Sense (CRS) output from the DM9101 will be asserted only by receive activity. In NODE mode, or a mode not configured for Full Duplex operation, CRS will be asserted by either receive or transmit activity. The value of the RPTR/NODE input pin is latched into this bit at power-up reset.
16.10	TX	1, RW	**100Base-TX or FX Mode Control:** 1=100Base-TX operation 0=100Base-FX operation
16.9	UTP	1, RW	**UTP Cable Control:** 1=The media is a UTP cable, 0=STP
16.8	CLK25MDIS	0, RW	**CLK25M Disable:** 1=CLK25M output clock signal tri-stated 0=CLK25M enabled This bit should be set to 1 to disable the 25Mhz output and reduce ground bounce and power consumption. For applications requiring the CLK25M output, set this bit to 0.
16.7	F_LINK_100	0, RW	**Force Good Link in 100Mbps:** 0=Normal 100Mbps operation 1=Force 100Mbps good link status This bit is useful for diagnostic purposes.
16.6	Reserved	1, RW	**Reserved:**
16.5	LINKLED_CTL	0, RW	**LINKLED Mode Select:** 0= Link LED output configured to indicate link status only 1= Link LED output configured to indicate traffic status: When the link status is OK, the LED will be on. When the chip is in transmitting or receiving, it flashes.
16.4	FDXLED_MODE	0, RW	**FDXLED Mode Select:** 1= FDXLED output configured to indicate polarity in 10Base-T mode 0= FDXLED output configured to indicate Full Duplex mode status for 10Mbps and 100Mbps operation
16.3	SMRST	0, RW	**Reset State Machine:** When this bit is set to 1, all state internal machines will be reset. This bit will clear after reset is completed.
16.2	MFPSC	0, RW	**MF Preamble Suppression Control:** 1= MF preamble suppression on 0= MF preamble suppression off MII frame preamble suppression control bit

DAVICOM Specified Configuration Register (DSCR) - Register 16 (continued)

Bit	Bit Name	Default	Description
16.1	SLEEP	0, RW	**Sleep Mode:** Writing a 1 to this bit will cause DM9101 to enter Sleep mode and power down all circuits except the oscillator and clock generator circuit. To exit Sleep mode, write 0 to this bit position. The prior configuration will be retained when the sleep state is terminated, but the state machine will be reset
16.0	RLOUT	0, RW	**Remote Loopout Control:** When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing

DAVICOM Specified Configuration and Status Register (DSCSR) - Register 17

Bit	Bit Name	Default	Description
17.15	100FDX	1, RO	**100M Full Duplex Operation:** After Auto-negotiation is completed, the results will be written to this bit. A “1” in this bit position indicates 100M Full Duplex operation. The software can read bits [15:12] to determine which mode is selected after Auto-negotiation. This bit is invalid when Auto-negotiation is disabled.
17.14	100HDX	1, RO	**100M Half Duplex Operation:** After Auto-negotiation is completed, the results will be written to this bit. A “1” in this bit position indicates 100M Half Duplex operation. The software can read bits [15:12] to determine which mode is selected after Auto-negotiation. This bit is invalid when Auto-negotiation is disabled.
17.13	10FDX	1, RO	**10M Full Duplex Operation:** After Auto-negotiation is completed, the results will be written to this bit. A “1” in this bit position indicates 10M Full Duplex operation. The software can read bits [15:12] to determine which mode is selected after Auto-negotiation. This bit is invalid when Auto-negotiation is disabled.
17.12	10HDX	1, RO	**10M Half Duplex Operation:** After Auto-negotiation is completed, the results will be written to this bit. A “1” in this bit position indicates 10M Half Duplex operation. The software can read bits [15:12] to determine which mode is selected after Auto-negotiation. This bit is invalid when Auto-negotiation is disabled.
17.11-17.10	Reserved	0, RW	**Reserved:** Write as 0, ignore on read
17.8-17.4	PHYAD[4:0]	(PHYAD), RW	**PHY Address Bit 4:0:** The values of the PHYAD[4:0] pins are latched to this register at power-up/reset. The first PHY address bit transmitted or received is the MSB (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY. A PHY address of <00000> will cause the isolate bit of the BMCR (bit 10, Register Address 00) to be set.

DAVICOM Specified Configuration and Status Register (DSCSR) - Register 17 (continued)

Bit	Bit Name	Default	Description
17.3-17.0	ANMB[3:0]	0, RO	**Auto-negotiation Monitor Bits:** These bits are for debug only. The Auto-negotiation status will be written to these bits.

b3	b2	b1	b0	
0	0	0	0	In IDLE state
0	0	0	0	Ability match
0	0	1	0	Acknowledge match
0	0	1	1	Acknowledge match fail
0	1	0	0	Consistency match
0	1	0	1	Consistency match fail
0	1	1	0	Parallel detect signal_link_ready
0	1	1	1	Parallel detect signal_link_ready fail
1	0	0	0	Auto-negotiation completed successfully

10Base-T Configuration/Status (10BTCSRCSR) - Register 18

Bit	Bit Name	Default	Description
18.15	Reserved	0, RO	**Reserved:** Write as 0, ignore on read
18.14	LP_EN	1, RW	**Link Pulse Enable:** 1=Transmission of link pulses enabled 0=Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation.
18.13	HBE	(inverse Pin94),RW	**Heartbeat Enable:** 1=Heartbeat function enabled 0=Heartbeat function disabled When the DM9101 is configured for Full Duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in Full Duplex mode). The initial state of this bit is the inverse value of RPTR/NODE input pin at power on reset.
18.12	Reserved	0, RO	**Reserved:** Write as 0, ignore on read
18.11	JABEN	1, RW	**Jabber Enable:** 1= Jabber function enabled 0= Jabber function disabled Enables or disables the Jabber function when the DM9101 is in 10Base-T Full Duplex or 10Base-T Transceiver Loop-back mode
18.10	10BT_SER	Pin98, RW	**10Base-T Serial Mode:** 1=10Base-T serial mode selected 0=10Base-T nibble mode selected The value on the 10BTSER input pin is latched into this bit at power-up/reset Serial mode not supported for 100Mbps operation.
18.9-18.1	Reserved	0, RO	**Reserved:** Write as 0, ignore on read

10Base-T Configuration/Status (10BTCSRCSR) - Register 18 (continued)

Bit	Bit Name	Default	Description
18.0	POLR	0, RO	**Polarity Reversed:** When this bit is set to 1, it indicates that the 10M cable polarity is reversed. This bit is set and cleared by 10Base-T module automatically.

Absolute Maximum Ratings*

Operating Voltage (VCC) 4.75V to 5.25V
Non-Operating Voltage (VCC) -0.5V to 7.00V
DC Input Voltage (VIN) -0.5V to VCC +0.5V
DC Output Voltage (VOUT) -0.5V to VCC +0.5V
Storage Temperature Range (Tstg) -65 to +150℃
Operating Ambient Temperature Range 0 to 70℃
Lead Temp (TL) (Soldering 10 sec.) 235℃
ESD rating (Rzap=1.5K, Czap=100pF) 4000V

Power Consumption:

100Base-TX Full Duplex 185 mA
(Measured using Unscrambled IDLE transmission looped back to RXIN, includes external termination circuitry)

10Base-T Full Duplex 222 mA
(Measured using Maximum packet size, minimum I.P.G. transmission looped back to RXIN, includes external termination circuitry).

Power Consumption: (continued)

Auto-Negotiation 165mA
(Measured during Parallel Detect until link established)
Idle 120mA
(Measured with no link established)
Power Down Mode 40mA
(Measured while MII Register 0 Bit 11 set true)

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

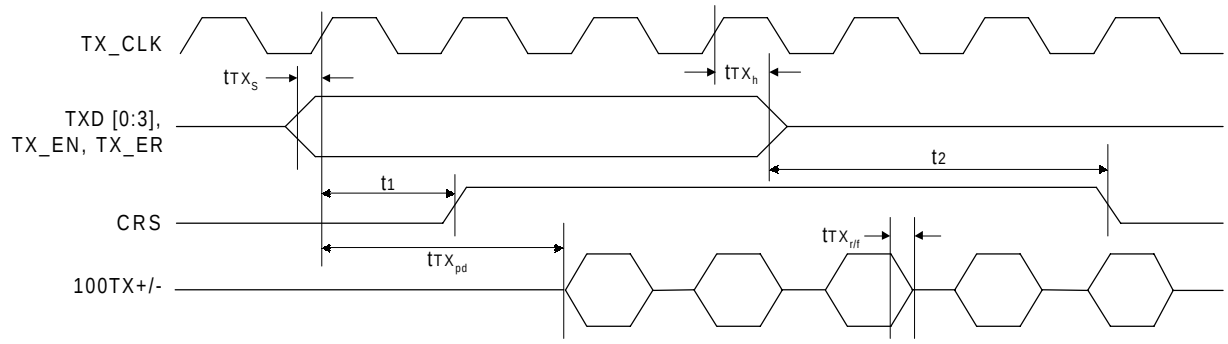
DC Electrical Characteristics (VCC = 5Vdc, ±5%, TA = 0 to 70, unless specified otherwise)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{100TX}	Supply Current 100Base-TX active		180	185	mA	V_{CC} = 5.0V
I_{10TTP}	Supply Current 10Base-TX active (Random data, Random IPG and Random size)		120		mA	V_{CC} = 5.0V
I_{10TWC}	Supply Current 10Base-TX active (Max. Packet size, Min. IPG and Worst case data patern)			220	mA	V_{CC} = 5.0V
I_{PDM}	Supply Current Power Down Mode			40	mA	V_{CC} = 5.0V
I_{AN}	Supply Current during Auto-Neg.			165	mA	V_{CC} = 5.0V
I_{RST}	Supply Current during Reset.			115	mA	V_{CC} = 5.0V
TTL Inputs (TXD0-TXD3, TX_CLK, MDIO, TX_EN, TX_DV, TX_ER, TESTMODE, PHYAD0-4, OPMODE0-4, RPTR, BPALIGN, BP4B5B, BPSCR, 10BTSER, RESET#)						
V_{IL}	Input Low Voltage			0.8	V	I_{IL} = -400uA
V_{IH}	Input High Voltage	2.0			V	I_{IH} = 100uA
I_{IL}	Input Low Current	-200			uA	V_{IN} = 0.4V
I_{IH}	Input High Current			100	uA	V_{IN} = 2.7V
MII TTL Outputs (RXD0-3, RX_EN, RX_DV, RX_ER, CRS, COL, MDIO)						
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -4mA
Non-MII TTL Outputs (TXLED#, RXLED#, LINKLED#, COLLED#, FDXLED#, RX_LOCK)						
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -0.1mA
Receiver						
V_{ICM}	RXI+/RXI- Input Common-Mode Voltage	1.5	2.0	2.5	V	100 Ω Termination Across
Transmitter						
ITD100	100TXO+/- 100Base-TX Mode Differential Output Current	19		21	mA	
ITD10	10TX+/- 10Base-T Differential Output Current	44	50	56	mA	

AC Electrical Characteristics (Over full range of operating condition unless specified otherwise)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Transmitter						
$t_{TR/F}$	100TXO+/- Differential Rise/Fall Time	3.0		5.0	ns	
t_{TM}	100TXO+/- Differential Rise/Fall Time Mismatch	-0.5		0.5	ns	
t_{TDC}	100TXO+/- Differential Output Duty Cycle Distortion	-0.5		0.5	ns	
$t_{T/T}$	100TXO+/- Differential Output Peak-to-Peak Jitter		300		ps	
XOST	100TXO+/- Differential Voltage Overshoot			5	%	
MII (Media-Independent Interface)						
XNTOL	TX Input Clock Frequency Tolerance				ppm	25MHz Frequency
XBTOL	TX Output Clock Frequency Tolerance	-100		+100	ppm	25MHz Frequency
t_{PWH}	OSC Pulse Width High	14			ns	
t_{PWL}	OSC Pulse Width Low	14			ns	
t_{RPWH}	RX_CLK Pulse Width High	14			ns	
t_{RPWL}	RX_CLK Pulse Width Low	14			ns	

MII-100Base-TX Transmit Timing Diagram



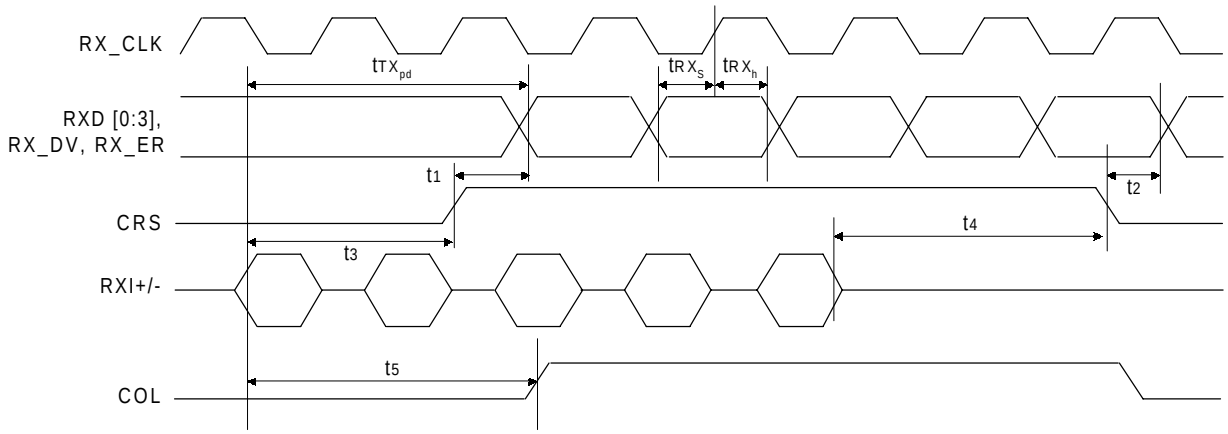
MII-100Base-TX Transmit Timing Parameters

(Half Duplex)

Symbol	Parameter	Min.	Typ[1].	Max.	Unit	Conditions
tTX_s	TXD[0:3], TX_EN, TX_ER Setup To TX_CLK High	11	-	-	ns	
tTX_h	TXD[0:3], TX_EN, TX_ER Hold From TX_CLK High	0	-	-	ns	
t1	TX_EN Sampled To CRS Asserted	-	4	-	BT	
t2	TX_EN Sampled To CRS De-asserted	-	4	-	BT	
tTX_{pd}	TX_EN Sampled To TPO Out (Tx Latency)	-	8	-	BT	
$tTX_{r/f}$	100TX Driver Rise/Fall Time	3	4	5	ns	90% To 10%, Into 100ohm Differential

1. Typical values are at 25 and are for design aid only; not guaranteed and not subject to production testing.

MII-100Base-TX Receive Timing Diagram

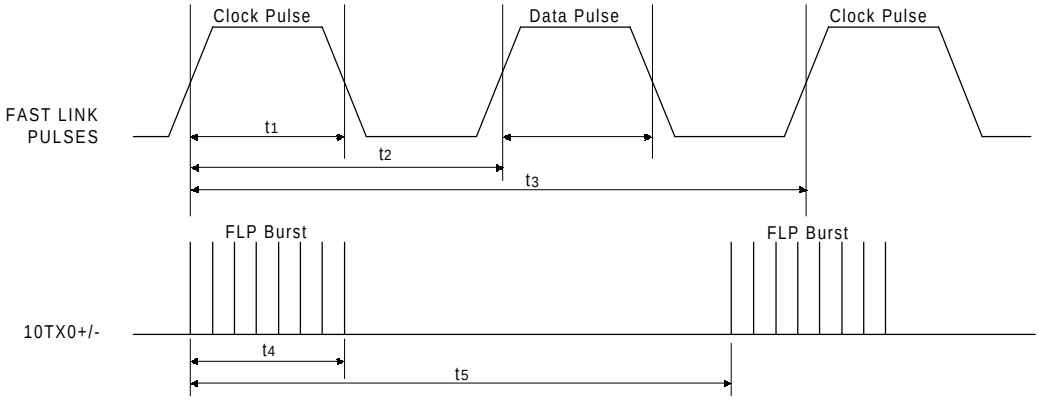


MII-100Base-TX Receive Timing Parameter

(Half Duplex)

Symbol	Parameter	Min.	Typ[1].	Max.	Unit	Conditions
tRX_s	RXD[0:3], RX_DV, RX_ER Setup To RX_CLK High	10	-	-	ns	
tRX_h	RXD[0:3], RX_DV, RX_ER Hold From RX_CLK High	10	-	-	ns	
tRX_{pd}	RXI In To RXD[0:3] Out (Rx Latency)	-	15	-	BT	
t1	CRS Asserted To RXD[0:3], RX_DV, RX_ER	-	4	-	BT	
t2	CRS De-asserted To RXD[0:3], RX_DV, RX_ER	-	0	-	BT	
t3	RXI In To CRS Asserted	10	-	14	BT	
t4	RXI Quiet To CRS De-asserted	14	-	18	BT	
t5	RXI In To COL De-Asserted	14	-	18	BT	
1. Typical values are at 25and are for design aid only; not guaranteed and not subject to production testing.						

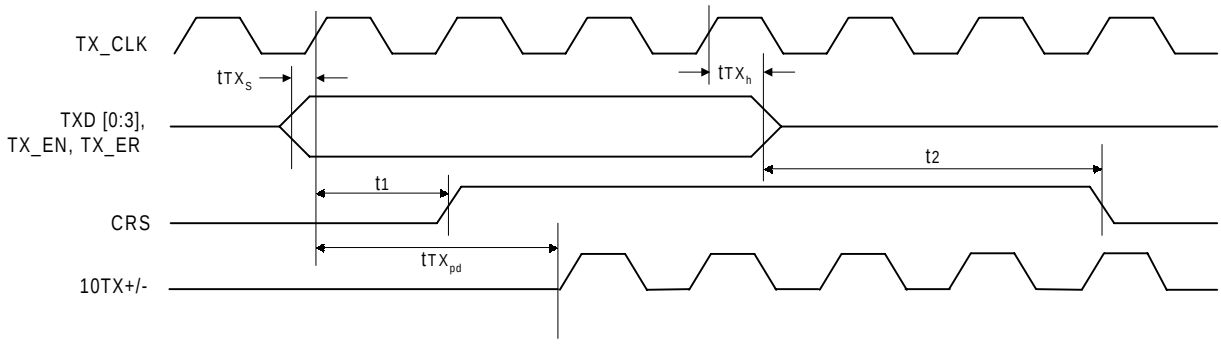
Auto-negotiation and Fast Link Pulse Timing Diagram



Auto-negotiation and Fast Link Pulse Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t1	Clock/Data Pulse Width	-	100	-	ns	
t2	Clock Pulse To Data Pulse Period	-	62.5	-	us	DATA = 1
t3	Clock Pulse To Clock Pulse Period	-	125	-	us	
t4	FLP Burst Width	-	2	-	ms	
t5	FLP Burst To FLP Burst Period	-	13.93	-	ms	
-	Clock/Data Pulses Per Burst	33	33	33	ea	

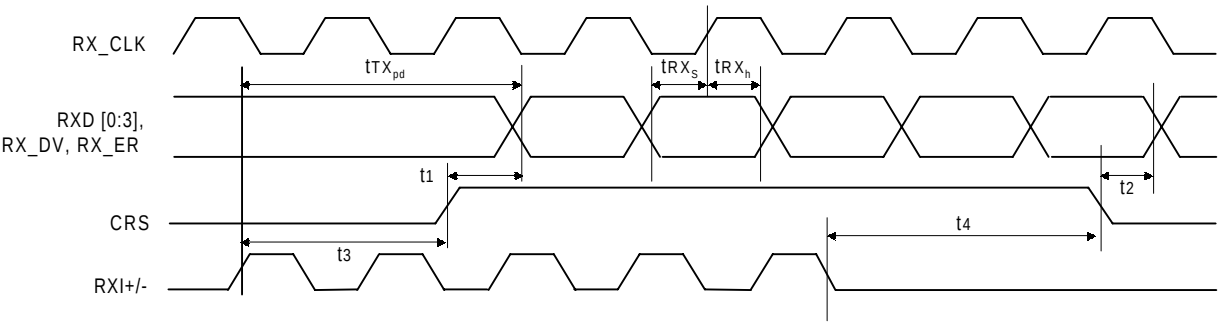
MII-10Base-T Nibble Transmit Timing Diagram



MII-10Base-T Nibble Transmit Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tTX_s	TXD[0:3), TX_EN, TX_ER Setup To TX_CLK High	11	-	-	ns	
tTX_h	TXD[0:3], TX_EN, TX_ER Hold From TX_CLK High	0	-	-	ns	
t1	TX_EN Sampled To CRS Asserted	-	2	4	BT	
t2	TX_EN Sampled To CRS De-asserted	-	15	20	BT	
tTX_{pd}	TX_EN Sampled To 10TXO Out (Tx Latency)	-	2	4	BT	

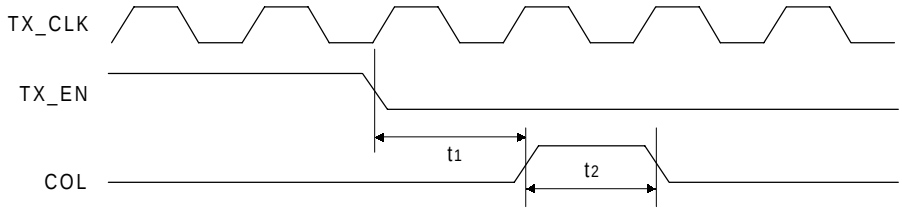
MII-10Base-T Receive Nibble Timing Diagram



MII-10Base-T Receive Nibble Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tRX_s	RXD[0:3], RX_DV, RX_ER Setup To RX_CLK High	10	-	-	ns	
tRX_h	RXD[0:3], RX_DV, RX_ER Hold From RX_CLK High	10	-	-	ns	
tRX_{pd}	RXI In To RXD[0:3] Out (Rx Latency)	-	7	-	BT	
t_1	CRS Asserted To RXD[0:3], RX_DV, RX_ER	1	14	20	BT	
t_2	CRS De-asserted To RXD[0:3], RX_DV, RX_ER	-	-	3	BT	
t_3	RXI In To CRS Asserted	1	2	4	BT	
t_4	RXI Quiet To CRS De-asserted	1	10	15	BT	

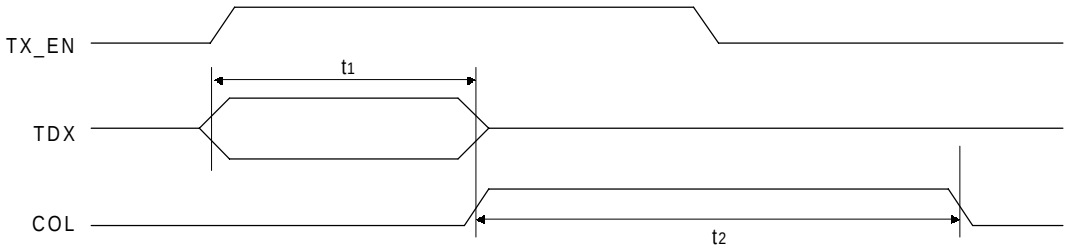
10Base-T SQE (Heartbeat) Timing Diagram



10Base-T SQE (Heartbeat) Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_1	COL (SQE) Delay After TX_EN Off	0.65	1.3	1.6	ms	
t_2	COL (SQE) Pulse Duration	0.5	1.1	1.5	ms	

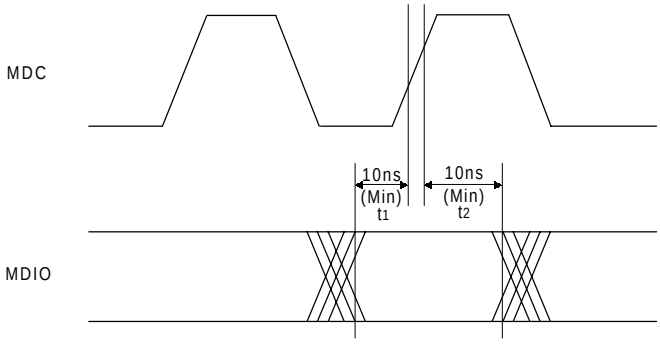
10Base-T Jab and Unjab Timing Diagram



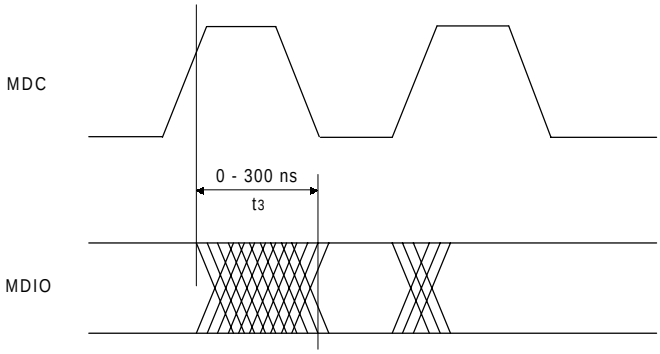
10Base-T Jab and Unjab Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_1	Maximum Transmit Time	20	48	150	ms	
t_2	Unjab Time	250	505	1500	ms	

MDIO Timing when OUTPUT by STA



MDIO Timing when OUTPUT by DM9101



MII Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_1	MDIO Setup Before MDC	10	-	-	ns	When OUTPUT By STA
t_2	MDIO Hold After MDC	10	-	-	ns	When OUTPUT By STA
t_3	MDC To MDIO Output Delay	0	-	100	ns	When OUTPTU By DM9101

Magnetics Selection Guide

The DM9101 requires a 1:1 ratio for both the receive and the transmit transformers. Refer to Table 2 for transformer requirements. Transformers meeting these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetics before using them in an application. The transformers listed in Table 2 are electrical equivalent, but may not be pin-to-pin equivalent.

Manufacturer	Part Number
Bel Fuse	S558-5999-01
Delta	LF8200, LF8221
Fil-Mag	PT41715
Halo	TG22-3506ND, TD22-3506G1, TG22-S010ND TG22-S012ND
Nano Pulse Inc.	NPI 6181-37, NPI 6120-30, NPI 6120-37 NPI 6170-30
Pulse Engineering	PE-68517, PE-68515, H1019, H1012 ----Single Port H1027, H1028 ---- Dual Port PE-69037, H1001, H1036, H1044 ---- Quad Port
Valor	ST6114, ST6118
YCL	20PMT04, 20PMT05

Table 2

Crystal Selection Guide

A crystal can be used to generate the 25Mhz reference clock instead of a crystal oscillator. An M-TRON crystal, part number is 00301-00169, MP-1 Fund, @ 25.000000Mhz, ±50ppm or equivalent may be used. The crystal must be a fundamental type, parallel resonant. Connect to X1 and X2, shunt each crystal lead to ground with an 18pf capacitor (see figure 6).

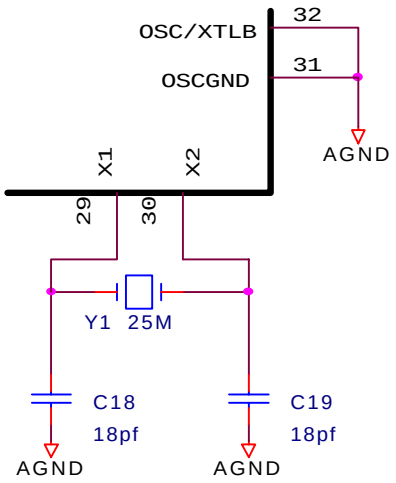
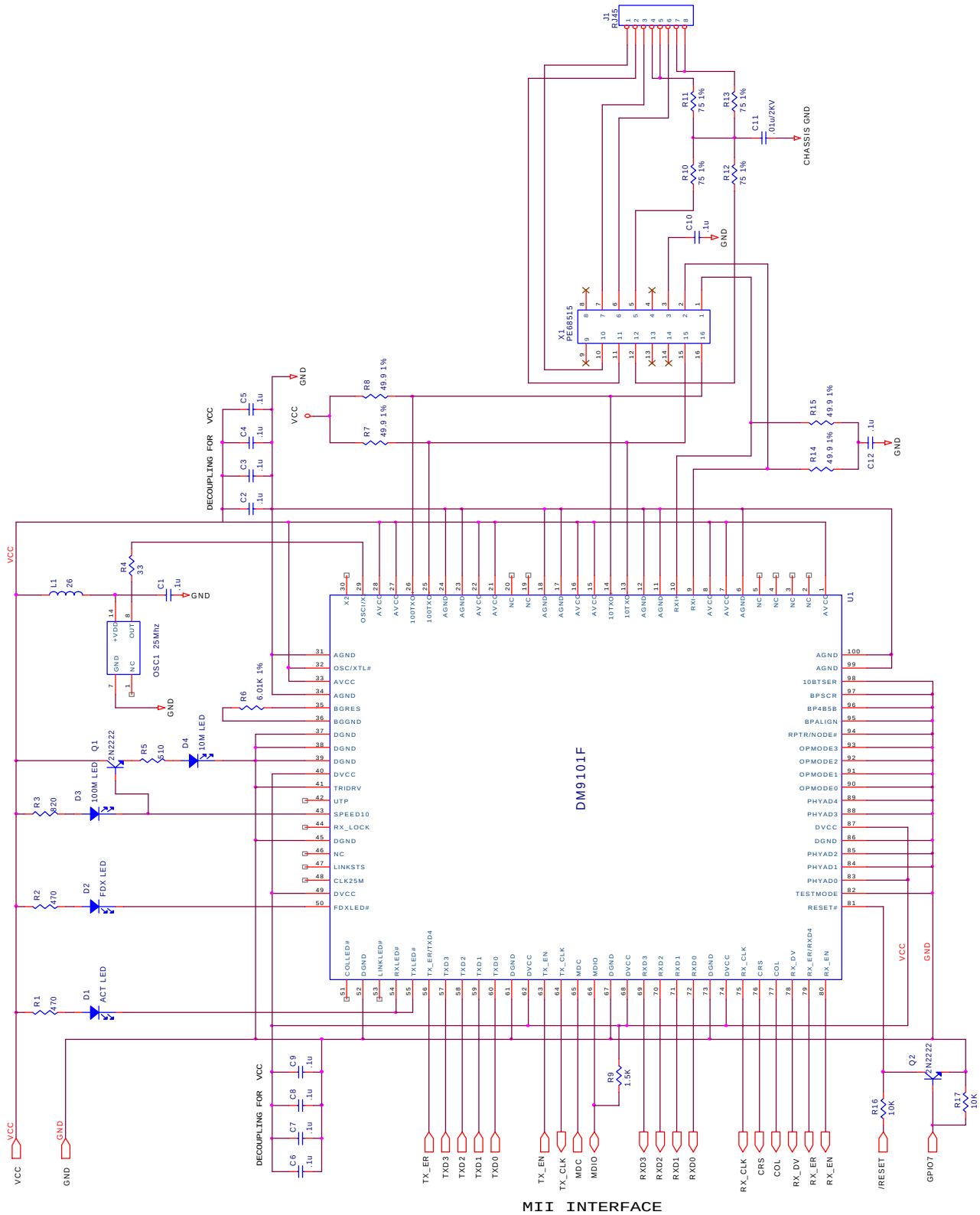


Figure 6
Crystal Circuit Diagram

Item No.	Qty.	Reference Number	Part Description
1	11	C1,C2,C3,C4,C5,C6,C7,C8,C9, C10,C11	Capacitor, Decoupling, 0.1uf, 50V
2	1	C12	Capacitor,.01uf,2KV
3	4	D1,D2,D3,D4	LED, General Purpose
4	1	J1	Connector, RJ45
5	1	L1	Ferrite, PanasonicEXCCL4532U
6	1	OSC1	Oscillator, Crystal, 25Mhz, ±50ppm
7	2	Q2,Q1	Transistor, NNP, General Purpose, 2N2222
8	2	R1,R2	Resistor, 470Ω, 5%
9	1	R3	Resistor, 820Ω, 5%
10	1	R4	Resistor, 33Ω, 5%
11	1	R5	Resistor, 510Ω, 5%
12	1	R6	Resistor, 6.01KΩ, 1%
13	4	R7,R8,R14,R15	Resistor, 49.9Ω, 1%
14	1	R9	Resistor, 1.5KΩ, 5%
15	4	R10,R11,R12,R13	Resistor, 75Ω, 1%
16	2	R17,R16	Resistor, 10KΩ, 5%
17	1	U1	DM9101F, PHY/Transceiver, 100pin QFP
18	1	U2	Magnetics, Pulse Engineering, PE68515

Table 3
Parts List for Example Design

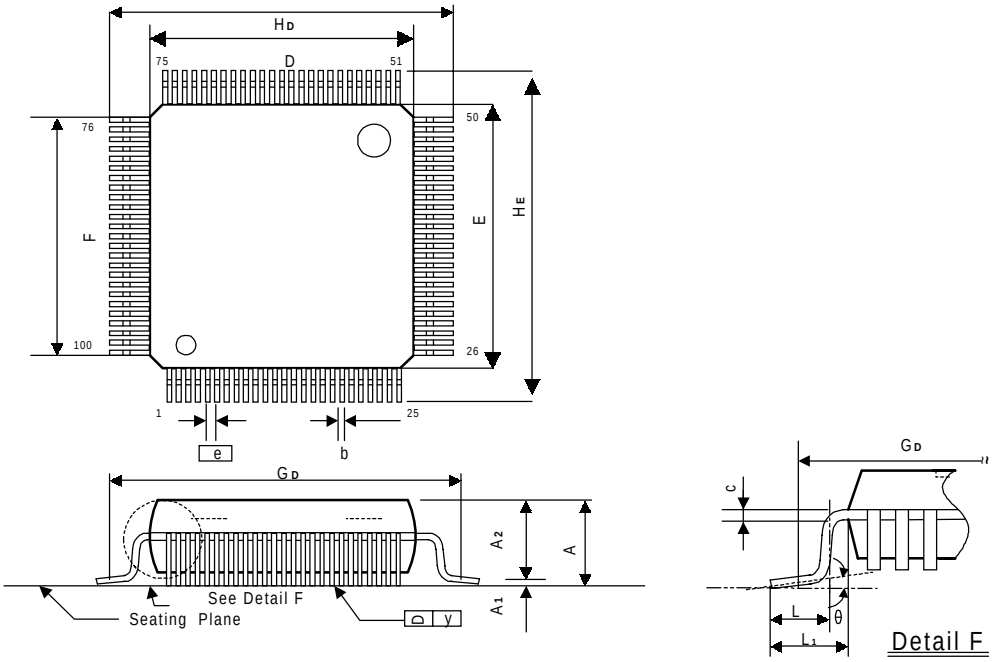
Table 3 is a list of materials used in the design example shown on the next page. Where a specific vendor name has been called out, the designer can substitute an equivalent part.


DM9101 MII Example Schematic
DM9101F
MII INTERFACE
DECOUPLING FOR VCC
OSC1 25Mhz
CHASSIS GND
VCC
GND

Package Information

LQFP 100L Outline Dimensions

Unit: Inches/mm



Symbol	Dimensions In Inches	Dimensions In mm
A	0.063 Max.	1.60 Max.
A_1	0.004 ± 0.002	0.1 ± 0.05
A_2	0.055 ± 0.002	1.40 ± 0.05
b	0.009 ± 0.002	0.22 ± 0.05
c	0.006 ± 0.002	0.15 ± 0.05
D	0.551 ± 0.005	14.00 ± 0.13
E	0.551 ± 0.005	14.00 ± 0.13
e	0.020 BSC.	0.50 BSC.
F	0.481 NOM.	12.22 NOM.
GD	0.606 NOM.	15.40 NOM.
HD	0.630 ± 0.006	16.00 ± 0.15
HE	0.630 ± 0.006	16.00 ± 0.15
L	0.024 ± 0.006	0.60 ± 0.15
L_1	0.039 Ref.	1.00 Ref.
y	0.004 Max.	0.1 Max.
θ	0° ~ 12°	0° ~ 12°

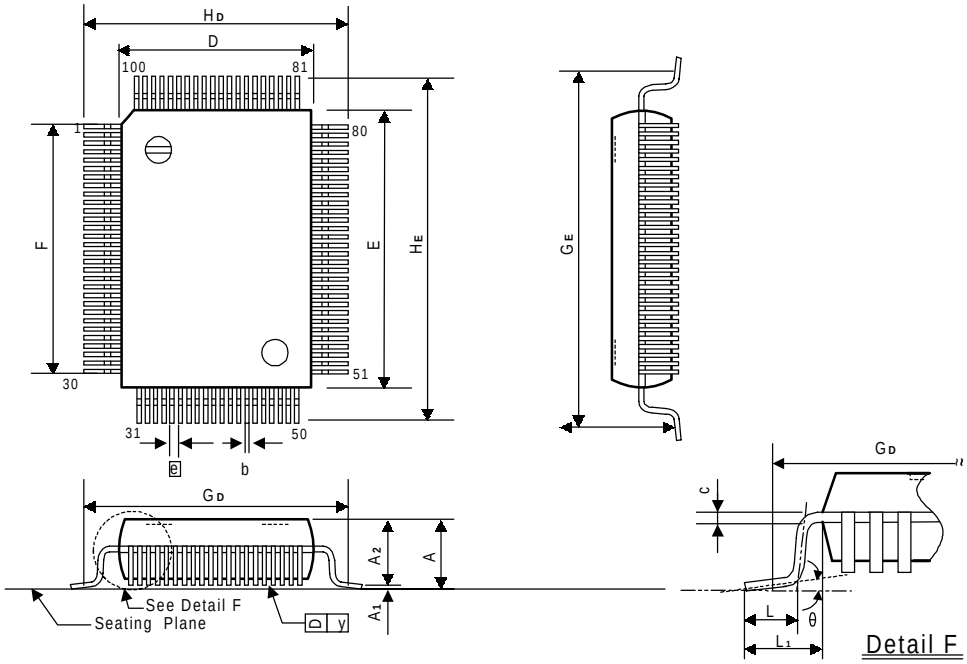
Notes:

1. Dimension D & E do not include resin fins.
2. Dimension GD is for PC Board surface mount pad pitch design reference only.
3. All dimensions are based on metric system.

Package Information

QFP 100L Outline Dimensions

Unit: Inches/mm



Symbol	Dimensions In Inches	Dimensions In mm
A	0.130 Max.	3.30 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.1120.005	2.850.13
b	0.012 +0.004 -0.002	0.31 +0.10 -0.05
c	0.006 +0.004 -0.002	0.15 +0.10 -0.05
D	0.5510.005	14.000.13
E	0.7870.005	20.000.13
e	0.026 0.006	0.650.15
F	0.742 NOM.	18.85 NOM.
G_D	0.693 NOM.	17.60 NOM.
G_E	0.929 NOM.	23.60 NOM.
H_D	0.7400.012	18.800.31
H_E	0.9760.012	24.790.31
L	0.0470.008	1.190.20
L_1	0.0950.008	2.410.20
y	0.006 Max.	0.15 Max.
θ	0° ~ 12°	0° ~ 12°

Note:

1. Dimension D & E do not include resin fins.
2. Dimension GD & GE are for PC Board surface mount pad pitch design reference only.
3. All dimensions are based on metric system.

Ordering Information

Part Number	Pin Count	Package
DM9101E	100	LQFP
DM9101F	100	QFP

Disclaimer

The information appearing in this publication is believed to be accurate. Integrated circuits sold by DAVICOM Semiconductor are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. DAVICOM makes no warranty, express, statutory, implied or by description regarding the information in this publication or regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHER, DAVICOM MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. DAVICOM reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by DAVICOM for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

DAVICOM's terms and conditions printed on the order acknowledgment govern all sales by DAVICOM. DAVICOM will not be bound by any terms inconsistent with these unless DAVICOM agrees otherwise in writing. Acceptance of the buyer's orders shall be based on these terms.

Company Overview

DAVICOM Semiconductor, Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.

Contact Windows

For additional information about DAVICOM products, contact the sales department at:

Headquarters:

Hsin-chu Office:
4F, No. 17, Park Avenue II,
Science-based Park,
Hsin-chu City, Taiwan, R.O.C.
TEL: 886-3-579-8797
FAX: 886-3-579-8858

Taipei Sales Office:
8F, No. 3, Lane 235, Bao-chiao Road,
Hsin-tien City, Taipei, Taiwan, R.O.C.
TEL: 886-2-2915-3030
FAX: 886-2-2915-7575
Email: sales@davicom.com.tw

WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.