

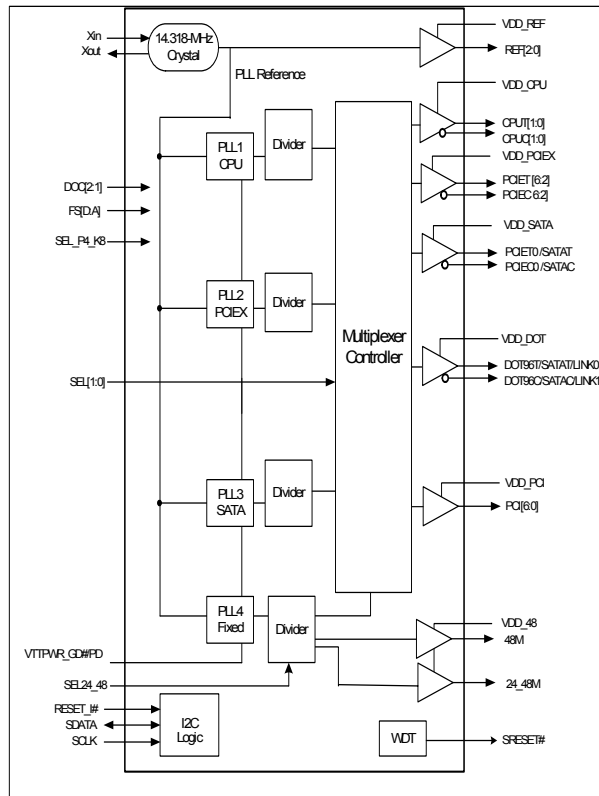
# Universal Clock Generator for Intel, VIA and SIS®

## Features

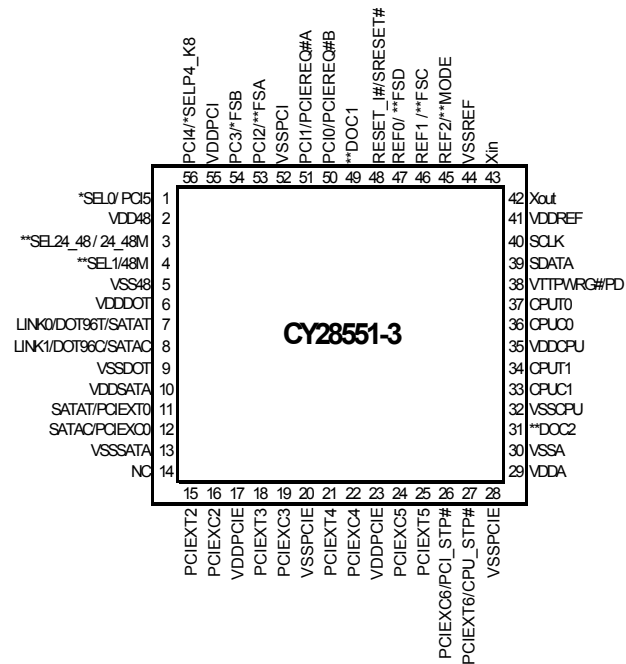
- Compliant to Intel® CK505
- Selectable CPU clock buffer type for Intel P4 or K8 selection
- Selectable CPU frequencies
- Universal clock to support Intel, SiS and VIA platform
- 0.7V Differential CPU clock for Intel CPU
- 3.3V Differential CPU clock for AMD K8
- 100-MHz differential SRC clocks
- 96-MHz differential dot clock
- 133-MHz Link clock
- 48-MHz USB clocks
- 33-MHz PCI clock
- Dynamic Frequency Control
- Dial-A-Frequency®
- WatchDog Timer
- Two Independent Overclocking PLLs
- Low-voltage frequency select input
- I<sup>2</sup>C support with readback capabilities
- Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V power supply
- 56-pin QFN packages

CPU	SRC	SATA	PCI	REF	LINK	DOT96	24_48M	48M
x 2	x 6	x 1	x 6	x 3	x 2	x 1	x 1	x 1

## Block Diagram



## Pin Configuration



\* Indicates internal pull-up  
\*\* indicates internal pull-down

**Pin Description**

Pin No.	Name	Type	Description
1	*SEL0/PCI5	I/O, PU	3.3V-tolerant input for output selection/33-MHz clock output. Refer to <i>Figure 1</i> for selection options. Internal 150k pull-up
2	VDD48	PWR	3.3V power supply for outputs.
3	**SEL24_48#/24_48M	I/O, PD	3.3V-tolerant input for 24-MHz, 48-MHz selection/24_48MHz clock output. Internal 150k pull-down 1 = 24 MHz, 0 = 48 MHz Intel Type-3A output buffer
4	**SEL1/48MHz	I/O, PD	3.3V-tolerant input for output selection/48-MHz clock output. Refer to <i>Figure 1</i> for selection options Internal 150k pull-down
5	VSS48	GND	Ground for outputs
6	VDDDOT	PWR	3.3V power supply for outputs
7	LINK0/DOT96T/SATAT	O, SE/DiF	Link output for VIA and SIS, Differential 96-MHz True clock and 100-MHz differential True clock. The output was selected by SEL[0:1]
8	LINK1/DOT96C/SATAC	O, SE/DiF	Link output for VIA and SIS, Differential 96-MHz Complement clock output and 100-MHz differential Complement clock. The output was selected by SEL[0:1]
9	VSSDOT	GND	Ground for outputs
10	VDDSAATA	PWR	3.3V power supply for outputs
11	PCIEXT0/SATAT	O, DIF	True differential SRC clock output/True differential SATA SRC clock output. Intel type SR output buffer
12	PCIEXC0/SATAC/	O, DIF	Complement differential SRC clock output/Complement differential SATA SRC clock output. Intel type SR output buffer
13	VSSSAATA	GND	Ground for outputs
14	VSS	GND	Ground for outputs
15	PCIEXT2	O, DIF	True 100-MHz Differential Serial reference clock. Intel type SR output buffer
16	PCIEXC2	O, DIF	Complement 100-MHz Differential Serial reference clock. Intel type SR output buffer
17	VDDPCIE	PWR	3.3V power supply for outputs.
18	PCIEXT3	O, DIF	True 100-MHz Differential Serial reference clock. Intel type SR output buffer
19	PCIEXC3	O, DIF	Complement 100-MHz Differential Serial reference clock. Intel type SR output buffer
20	VSSPCIE	GND	Ground for outputs.
21	PCIEXT4	O, DIF	True 100-MHz Differential Serial reference clock. Intel type SR output buffer
22	PCIEXC4	O, DIF	Complement 100-MHz Differential Serial reference clock. Intel type SR output buffer
23	VDDPCIE	PWR	3.3V power supply for outputs.
24	PCIEXC5	O, DIF	Complement 100-MHz Differential Serial reference clock. Intel type SR output buffer
25	PCIEXT5	O, DIF	True 100-MHz Differential Serial reference clock. Intel type SR output buffer
26	PCIEXC6/PCI_ST OP#	I/O, DIF	3.3V-tolerant input for stopping PCI and SRC outputs/Complement 100-MHz Differential serial reference clocks. The two multifunction pins are selected by MODE. Default PCIEX6. Intel type SR output buffer
27	PCIEXT6/CPU_ST OP#	I/O, DIF	3.3V-tolerant input for stopping CPU outputs/True 100-MHz Differential serial reference clocks. The two multifunction pins are selected by MODE. Default PCIEX6. Intel type SR output buffer
28	VSSPCIE	GND	Ground for outputs.
29	VDDA	PWR	3.3V power supply for PLL.

**Pin Description** (continued)

Pin No.	Name	Type	Description
30	VSSA	GND	Ground for PLL.
31	**DOC2	I, PD	Dynamic Over Clocking pin 0 = normal, 1 = Frequency will be changed depend on DOC register. Internal 150k pull-down.
32	VSSCPU	GND	Ground for outputs.
33	CPUC1	O, DIF	Complement Differential CPU clock output. Intel type SR output buffer.
34	CPUT1	O, DIF	True Differential CPU clock output. Intel type SR output buffer.
35	VDDCPU	PWR	3.3V power supply for outputs.
36	CPUC0	O, DIF	Complement Differential CPU clock output. Intel type SR output buffer.
37	CPUT0	O, DIF	True Differential CPU clock output. Intel type SR output buffer.
38	VTT_PWRGD#/PD	I	3.3V LVTTTL input. This pin is a level-sensitive strobe used to latch the HW strapping pin inputs. After asserting VTT_PWRGD# (active LOW), this pin becomes a real-time input for asserting power-down (active HIGH)
39	SDATA	I/O	SMBus compatible SDATA
40	SCLK	I	SMBus compatible SCLOCK.
41	VDDREF	PWR	3.3V power supply for outputs.
42	XOUT	O	14.318-MHz Crystal Output
43	XIN	I	14.318-MHz Crystal Input
44	VSSREF	GND	Ground for outputs.
45	**MODE/REF2	I/O, SE, PD	3.3V-tolerant input for selecting output/14.318-MHz REF clock output. Internal 150k pull-down 0 = Desktop, 1 = Notebook Intel Type-5 output buffer
46	**FSC/REF1	I/O, PD, SE	3.3V-tolerant input for CPU frequency selection/14.318-MHz REF clock output. Internal 150k pull-down Intel Type-5 output buffer Refer to DC Electrical Specifications table for $V_{il\_FS}$ and $V_{ih\_FS}$ specifications.
47	**FSD/REF0	I/O, PD, SE	3.3V-tolerant input for CPU frequency selection/14.318-MHz REF clock output. Internal 150k pull-down Intel Type-5 output buffer Refer to DC Electrical Specifications table for $V_{il\_FS}$ and $V_{ih\_FS}$ specifications.
48	RESET_I#/SRESET#	I/O, OD	3.3V-tolerant input for reset all of registers to default setting. 3.3V LVTTTL output for watchdog reset signal
49	**DOC1	I, PD	Dynamic Over Clocking pin 0 = normal, 1 = Frequency will be changed depend on DOC register. Internal 150k pull-down
50	**CLKREQ#B/PCI0	I/O, SE, PD	3.3V tolerant LVTTTL input for Output enable of PCIEX 4,5 via register selection/33-MHz clock output. Internal 150k pull-down Intel Type-3A output buffer
51	**CLKREQ#A/PCI1	I/O, SE, PD	3.3V-tolerant LVTTTL input for Output enable of PCIEX 6,7 via register selection/33-MHz clock output. Internal 150K pull-down Intel Type-3A output buffer
52	VSSPCI	GND	Ground for outputs.

**Pin Description** (continued)

Pin No.	Name	Type	Description
53	**FSA/PCI2	I/O, PD	3.3V-tolerant input for CPU frequency selection/33-MHz clock output. Internal 150k pull-down Intel Type-3A output buffer Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications
54	*FSB/PCI3	I/O, PU	3.3V-tolerant input for CPU frequency selection/33-MHz clock output. Internal 150k pull-up Intel Type-3A output buffer Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications
55	VDDPCI	PWR	3.3V power supply for outputs.
56	*SELP4_K8/PCI3	I/O, PU	3.3V-tolerant input for CPU clock output buffer type selection/33-MHz clock output. Internal 150k pull-up Intel Type-3A output buffer Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications 0 = K8 CPU buffer type, 1=P4 CPU buffer type.

**Frequency Select Pins (FS[D:A])**

Host clock frequency selection is achieved by applying the appropriate logic levels to FS\_A, FS\_B, FS\_C, and FS\_D inputs prior to VTT\_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT\_PWRGD# being sampled LOW by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS\_A, FS\_B, FS\_C, and FS\_D input values. For all logic levels of FS\_A, FS\_B, FS\_C, FS\_D and FS\_E, VTT\_PWRGD# employs a one-shot functionality in that once a valid LOW on VTT\_PWRGD# has been sampled, all further VTT\_PWRGD#, FS\_A, FS\_B, FS\_C, and FS\_D transitions will be ignored, except in test mode.

**Serial Data Interface**

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual

clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

**Data Protocol**

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

**Figure 1. CPU and SRC Frequency Select Tables**

FSD				Frequency Table (ROM)												
FSEL3	FSEL2	FSEL1	FSEL0	CPU0	CPU1	SRC	LINK	PCI	CPU VCO	CPU PLL Gear Constant (G)	CPU M	CPU N	PCIE VCO	SRC PLL Gear Constant	PCIE M	PCIE N
0	0	0	0	266.667	266.667	100	66.6667	33.3333	800	80	60	200	800	30	60	200
0	0	0	1	133.333	133.333	100	66.6667	33.3333	800	40	60	200	800	30	60	200
0	0	1	0	200	200	100	66.6667	33.3333	800	60	60	200	800	30	60	200
0	0	1	1	166.667	166.667	100	66.6667	33.3333	666.67	60	63	175	800	30	60	200
0	1	0	0	333.333	333.333	100	66.6667	33.3333	666.67	120	63	175	800	30	60	200
0	1	0	1	100	100	100	66.6667	33.3333	800	30	60	200	800	30	60	200
0	1	1	0	400	400	100	66.6667	33.3333	800	120	60	200	800	30	60	200
0	1	1	1	200	250	100	66.6667	33.3333	1000	60	60	250	800	30	60	200
1	0	0	0	266.667	266.667	100	133.333	33.3333	800	80	60	200	800	30	60	200
1	0	0	1	133.333	133.333	100	133.333	33.3333	800	40	60	200	800	30	60	200
1	0	1	0	200	200	100	133.333	33.3333	800	60	60	200	800	30	60	200
1	0	1	1	166.667	166.667	100	133.333	33.3333	666.67	60	63	175	800	30	60	200
1	1	0	0	333.333	333.333	100	133.333	33.3333	666.67	120	63	175	800	30	60	200
1	1	0	1	100	100	100	133.333	33.3333	800	30	60	200	800	30	60	200
1	1	1	0	400	400	100	133.333	33.3333	800	120	60	200	800	30	60	200
1	1	1	1	200	250	100	133.333	33.3333	1000	60	60	250	800	30	60	200

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 1. Command Code Definition**

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

**Table 2. Block Read and Block Write Protocol**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count – 8 bits (Skip this step if I <sup>2</sup> C_EN bit set)	20	Repeat start
28	Acknowledge from slave	27:21	Slave address – 7 bits
36:29	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2 – 8 bits	37:30	Byte Count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte/Slave Acknowledges	46:39	Data byte 1 from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave – 8 bits
		....	NOT Acknowledge
		....	Stop

**Table 3. Byte Read and Byte Write Protocol**

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte – 8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address – 7 bits
29	Stop	28	Read

Table 3. Byte Read and Byte Write Protocol (continued)

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
		29	Acknowledge from slave
		37:30	Data from slave – 8 bits
		38	NOT Acknowledge
		39	Stop

**Control Registers**

**Byte 0: Control Register 0**

Bit	@Pup	Type	Name	Description
7	1	R/W	Reserved	Reserved
6	1	R/W	PCIEX[T/C]6	PCIEX[T/C]6 Output Enable 0 = Disable (Tri-state), 1 = Enable
5	1	R/W	PCIEX[T/C]5	PCIEX[T/C]5 Output Enable 0 = Disable (Tri-state), 1 = Enable
4	1	R/W	PCIEX[T/C]4	PCIEX[T/C]4 Output Enable 0 = Disable (Tri-state), 1 = Enable
3	1	R/W	PCIEX[T/C]3	PCIEX[T/C]3 Output Enable 0 = Disable (Tri-state), 1 = Enable
2	1	R/W	PCIEX[T/C]2	PCIEX[T/C]2 Output Enable 0 = Disable (Tri-state), 1 = Enable
1	1	R/W	Reserved	Reserved
0	1	R/W	SATA/PCIEX[T/C]0	SATA/PCIEX[T/C]0 Output Enable 0 = Disable (Tri-state), 1 = Enable

**Byte 1: Control Register 1**

Bit	@Pup	Type	Name	Description
7	1	R/W	SATA/DOT96]	SATA/DOT96Output Enable 0 = Disable (Tri-state), 1 = Enable
6	1	R/W	24_48M	24_48M Output Enable 0 = Disabled, 1 = Enabled
5	1	R/W	48M	48M Output Enable 0 = Disabled, 1 = Enabled
4	1	R/W	REF2	REF2 Output Enable 0 = Disabled, 1 = Enabled
3	1	R/W	REF1	REF1 Output Enable 0 = Disabled, 1 = Enabled
2	1	R/W	REF0	REF0 Output Enable 0 = Disabled, 1 = Enabled
1	1	R/W	CPU[T/C]1	CPU[T/C]1 Output Enable 0 = Disable (Tri-state), 1 = Enabled
0	1	R/W	CPU[T/C]0	CPU[T/C]0 Output Enable 0 = Disable (Tri-state), 1 = Enabled

**Byte 2: Control Register 2**

Bit	@Pup	Type	Name	Description
7	1	R/W	Reserved	Reserved
6	1	R/W	Reserved	Reserved

**Byte 2: Control Register 2** (continued)

Bit	@Pup	Type	Name	Description
5	1	R/W	PCI5	PCI5 Output Enable 0 = Disabled, 1 = Enabled
4	1	R/W	PCI4	PCI4 Output Enable 0 = Disabled, 1 = Enabled
3	1	R/W	PCI3	PCI3 Output Enable 0 = Disabled, 1 = Enabled
2	1	R/W	PCI2	PCI2 Output Enable 0 = Disabled, 1 = Enabled
1	1	R/W	PCI1	PCI1 Output Enable 0 = Disabled, 1 = Enabled
0	1	R/W	PCI0	PCI0 Output Enable 0 = Disabled, 1 = Enabled

**Byte 3: Control Register 3**

Bit	@Pup	Type	Name	Description
7	1	R/W	LINK1	LINK1 Output Enable 0 = Disabled, 1 = Enabled
6	1	R/W	LINK0	LINK0 Output Enable 0 = Disabled, 1 = Enabled
5	1	R/W	Reserved	Reserved
4	1	R/W	Reserved	Reserved
3	0	R/W	Reserved	Reserved
2	1	R/W	PCI	33-MHz Output Drive Strength 0 = 2x, 1 = 1x
1	1	R/W	REF	REF Output Drive Strength 0 = 2x, 1 = 1x
0	0	R/W	48M, 24_48M	48-MHz and 24_48M Output Drive Strength 0 = 2x, 1 = 1x

**Byte 4: Control Register 4**

Bit	@Pup	Type	Name	Description
7	0	R/W	CPU1	Allow control of CPU1 with assertion of CPU_STP# 0 = Free Running 1 = Stopped with CPU_STP#
6	0	R/W	CPU0	Allow control of CPU0 with assertion of CPU_STP# 0 = Free Running 1 = Stopped with CPU_STP#
5	0	R/W	Reserved	Reserved
4	0	R/W	PCIEX	Allow control of PCIEX with assertion of PCI_STP# 0 = Free Running 1 = Stopped with PCI_STP#
3	0	R/W	FSEL_D	SW Frequency selection bits. See <i>Figure 1</i> .
2	0	R/W	FSEL_C	
1	0	R/W	FSEL_B	
0	0	R/W	FSEL_A	

**Byte 5: Control Register 5**

Bit	@Pup	Type	Name	Description
7	0	R/W	CPU_SS1	CPU (PLL1) Spread Spectrum Selection
6	0	R/W	CPU_SS0	00: -0.5% (peak to peak) 01: ±0.25% (peak to peak) 10: -1.0% (peak to peak) 11: ±0.5% (peak to peak)
5	0	R/W	CPU_SS_OFF	PLL1 (CPUPLL) Spread Spectrum Enable 0 = Spread off, 1 = Spread on.
4	0	R/W	PCIE_SS0	PLL2 (PCIEPLL) Spread Spectrum Selection 0: -0.5% (peak to peak) 0: -1.0% (peak to peak)
3	0	R/W	PCIE_SS_OFF	PLL2 (PCIEPLL) Spread Spectrum Enable 0: SRC spread off, 1: SRC spread on.
2	0	R/W	SATA_SS_OFF	PLL3 (SATAPLL) Spread Spectrum Enable 0 = Spread off, 1 = Spread on
1	HW	R/W	SEL24_48	24M/48-MHz output selection 0 = 48 MHz, 1 = 24 MHz
0	0	R/W	Reserved	Reserved

**Byte 6: Control Register 6**

Bit	@Pup	Type	Name	Description
7	0	R/W	SW_RESET	Software Reset. When set, the device will assert a reset signal on SRESET# upon completion of the block/word/byte write that set it. After asserting and deasserting the SRESET# this bit will self clear (set to 0).
6	0	R/W	Reserved	Reserved
5	0	R/W	FIX_LINK_PCI	LINK and PCI clock source selection 0 = PLL2(SRCPLL), 1 = PLL3 (SATAPLL)
4	HW	R	FSD	FSD Reflects the value of the FSD pin sampled on power-up. 0 = FSD was low during VTT_PWRGD# assertion.
3	HW	R	FSC	FSC Reflects the value of the FSC pin sampled on power-up. 0 = FSC was low during VTT_PWRGD# assertion.
2	HW	R	FSB	FSB Reflects the value of the FSB pin sampled on power-up 0 = FSB was LOW during VTT_PWRGD# assertion.
1	HW	R	FSA	FSA Reflects the value of the FSA pin sampled on power-up. 0 = FSA was LOW during VTT_PWRGD# assertion
0	HW	R	POWERGOOD	Power Status bit: 0 = Internal power or Internal resets are NOT valid 1 = Internal power and Internal resets are valid Read only Bit 7 sets to 0 when Bit 7 =0

**Byte 7: Vendor ID**

Bit	@Pup	Type	Name	Description
7	0	R	Revision Code Bit 3	Revision Code Bit 3
6	0	R	Revision Code Bit 2	Revision Code Bit 2
5	0	R	Revision Code Bit 1	Revision Code Bit 1
4	0	R	Revision Code Bit 0	Revision Code Bit 0
3	1	R	Vendor ID Bit 3	Vendor ID Bit 3
2	0	R	Vendor ID Bit 2	Vendor ID Bit 2
1	0	R	Vendor ID Bit 1	Vendor ID Bit 1



Byte 7: Vendor ID (continued)

Bit	@Pup	Type	Name	Description
0	0	R	Vendor ID Bit 0	Vendor ID Bit 0

Byte 8: Control Register 8

Bit	@Pup	Type	Name	Description
7	0	R/W	RESERVED	RESERVED, Set = 0
6	0	R/W	CR1_PCIEX6	PCIEX[T/C]6 CLKREQ#A Control 1 = PCIEX [T/C]6 stoppable by CLKREQ#A pin 0 = Free running
5	0	R/W	CR1_PCIEX5	PCIEX[T/C]5 CLKREQ#B Control 1 = PCIEX [T/C]5 stoppable by CLKREQ#B pin 0 = Free running
4	0	R/W	CR1_PCIEX4	PCIEX[T/C]4 CLKREQ#B Control 1 = PCIEX [T/C]4 stoppable by CLKREQ#B pin 0 = Free running
3	0	R/W	RESERVED	RESERVED, Set = 0
2	0	R/W	RESERVED	RESERVED, Set = 0
1	0	R/W	RESERVED	RESERVED, Set = 0
0	0	R/W	RESERVED	RESERVED, Set = 0

Byte 9: Control Register 9

Bit	@Pup	Type	Name	Description
7	0	R/W	DF3_N8	The DF3_N[8:0] will be used to configure CPU frequency for Dynamic Frequency. DOC[1:2] =11
6	0	R/W	DF2_N8	The DF2_N[8:0] will be used to configure CPU frequency for Dynamic Frequency. DOC[1:2] =10
5	0	R/W	DF1_N8	The DF1_N[8:0] will be used to configure CPU frequency for Dynamic Frequency. DOC[1:2] =01
4	0	R/W	RESERVED	RESERVED, Set = 0
3	0	R/W	RESERVED	RESERVED, Set = 0
2	0	R/W	SMSW_Bypass	Smooth switch Bypass 0: Activate SMSW block 1: Bypass and de-activate SMSW block.
1	0	R/W	SMSW_SEL	Smooth switch select 0: select CPU_PLL 1: select SRC_PLL.
0	0	R/W	RESERVED	RESERVED, Set = 0

Byte 10: Control Register 10

Bit	@Pup	Type	Name	Description
7	0	R/W	DF1_N7	The DF1_N[8:0] will be used to configure CPU frequency for Dynamic Frequency. DOC[1:2] =01.
6	0	R/W	DF1_N6	
5	0	R/W	DF1_N5	
4	0	R/W	DF1_N4	
3	0	R/W	DF1_N3	
2	0	R/W	DF1_N2	
1	0	R/W	DF1_N1	
0	0	R/W	DF1_N0	

**Byte 11: Control Register 11**

Bit	@Pup	Type	Name	Description
7	0	R/W	DF2_N7	The DF2_N[8:0] will be used to configure CPU frequency for Dynamic Frequency. DOC[1:2] =10
6	0	R/W	DF2_N6	
5	0	R/W	DF2_N5	
4	0	R/W	DF2_N4	
3	0	R/W	DF2_N3	
2	0	R/W	DF2_N2	
1	0	R/W	DF2_N1	
0	0	R/W	DF2_N0	

**Byte 12: Control Register 12**

Bit	@Pup	Type	Name	Description
7	0	R/W	DF3_N7	The DF3_N[8:0] will be used to configure CPU frequency for Dynamic Frequency. DOC[1:2] =11
6	0	R/W	DF3_N6	
5	0	R/W	DF3_N5	
4	0	R/W	DF3_N4	
3	0	R/W	DF3_N3	
2	0	R/W	DF3_N2	
1	0	R/W	DF3_N1	
0	0	R/W	DF3_N0	

**Byte 13: Control Register 13**

Bit	@Pup	Type	Name	Description
7	0	R/W	Recovery_Frequency	This bit allows selection of the frequency setting that the clock will be restored to once the system is rebooted 0: Use HW settings, 1: Recovery N[8:0]
6	0	R/W	Timer_SEL	Timer_SEL selects the WD reset function at the SRESET pin when WD times out. 0 = Reset and Reload Recovery_Frequency 1 = Only Reset
5	1	R/W	Time_Scale	Time_Scale allows selection of WD time scale 0 = 294 ms 1 = 2.34 s
4	0	R/W	WD_Alarm	WD_Alarm is set to "1" when the watchdog times out. It is reset to "0" when the system clears the WD_TIMER time stamp.
3	0	R/W	WD_TIMER2	Watchdog timer time stamp selection 000: Reserved (test mode) 001: 1 * Time_Scale 010: 2 * Time_Scale 011: 3 * Time_Scale 100: 4 * Time_Scale 101: 5 * Time_Scale 110: 6 * Time_Scale 111: 7 * Time_Scale
2	0	R/W	WD_TIMER1	
1	0	R/W	WD_TIMER0	
0	0	R/W	WD_EN	Watchdog timer enable, when the bit is asserted, Watchdog timer is triggered and time stamp of WD_Timer is loaded 0 = Disable, 1 = Enable

**Byte 14: Control Register 14**

Bit	@Pup	Type	Name	Description
7	0	R/W	CPU_DAF_N7	If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] will be used to determine the CPU output frequency. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[E:A] register will be used. When it is set, the frequency ratio stated in the FSEL[3:0] register will be used.
6	0	R/W	CPU_DAF_N6	
5	0	R/W	CPU_DAF_N5	
4	0	R/W	CPU_DAF_N4	
3	0	R/W	CPU_DAF_N3	
2	0	R/W	CPU_DAF_N2	
1	0	R/W	CPU_DAF_N1	
0	0	R/W	CPU_DAF_N0	

**Byte 15: Control Register 15**

Bit	@Pup	Type	Name	Description
7	0	R/W	CPU_DAF_N8	If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] will be used to determine the CPU output frequency. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[E:A] register will be used. When it is set, the frequency ratio stated in the FSEL[3:0] register will be used.
6	0	R/W	CPU_DAF_M6	
5	0	R/W	CPU_DAF_M5	
4	0	R/W	CPU_DAF_M4	
3	0	R/W	CPU_DAF_M3	
2	0	R/W	CPU_DAF_M2	
1	0	R/W	CPU_DAF_M1	
0	0	R/W	CPU_DAF_M0	

**Byte 16: Control Register 16**

Bit	@Pup	Type	Name	Description
7	0	R/W	PCIE_DAF_N7	The PCIE_DAF_N[8:0] will be used to configure PCIE frequency for Dial-A Frequency
6	0	R/W	PCIE_DAF_N6	
5	0	R/W	PCIE_DAF_N5	
4	0	R/W	PCIE_DAF_N4	
3	0	R/W	PCIE_DAF_N3	
2	0	R/W	PCIE_DAF_N2	
1	0	R/W	PCIE_DAF_N1	
0	0	R/W	PCIE_DAF_N0	

**Byte 17: Control Register 17**

Bit	@Pup	Type	Name	Description
7	0	R/W	Recovery N7	Watchdog Recovery Bit
6	0	R/W	Recovery N6	Watchdog Recovery Bit
5	0	R/W	Recovery N5	Watchdog Recovery Bit
4	0	R/W	Recovery N4	Watchdog Recovery Bit
3	0	R/W	Recovery N3	Watchdog Recovery Bit
2	0	R/W	Recovery N2	Watchdog Recovery Bit
1	0	R/W	Recovery N1	Watchdog Recovery Bit
0	0	R/W	Recovery N0	Watchdog Recovery Bit

**Byte 18: Control Register 18**

Bit	@Pup	Type	Name	Description
7	0	R/W	PCIE_N8	PCI-E Dial-A-Frequency Bit N8
6	0	R/W	FS[D:A]	FS_Override 0 = Select operating frequency by FS(D:A) input pins 1 = Select operating frequency by FSEL_(3:0) settings
5	0	R/W	DF_EN	Dynamic Frequency for CPU frequency Enable 0 = Disable, 1 = Enable
4	0	R/W	RESET_I_EN	RESET_I# Enable 0: Disable, 1: Enable.
3	0	R/W	Prog_PCIE_EN	Programmable SRC frequency enable 0 = Disabled, 1 = Enabled.
2	0	R/W	Prog_CPU_EN	Programmable CPU frequency enable 0 = Disabled, 1 = Enabled.
1	0	R/W	Watchdog Autorecovery	Watchdog Autorecovery Mode 0 = Disable (Manual), 1= Enable (Auto)
0	0	R/W	Recovery N8	Watchdog Recovery Bit

**Table 4. Crystal Recommendations**

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

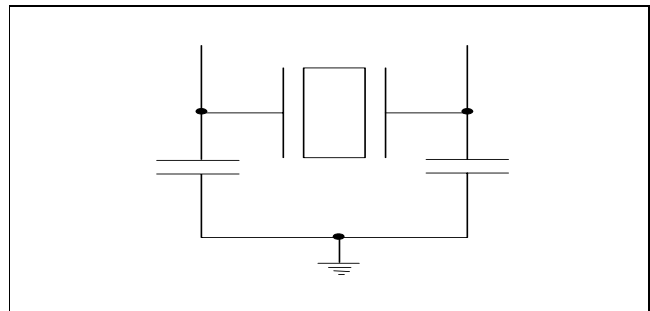
**Crystal Recommendations**

The CY28551-3 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the CY28551-3 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

**Crystal Loading**

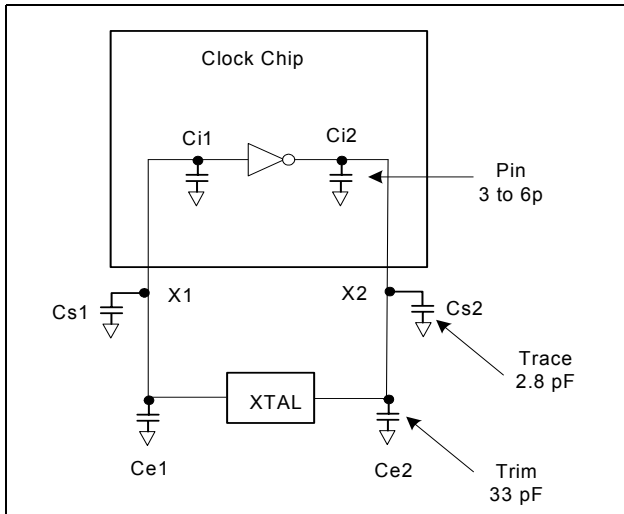
Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure 2 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

**Figure 2. Crystal Capacitive Clarification**

**Calculating Load Capacitors**

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

Figure 3. Crystal Loading Example



Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

**Load Capacitance (each side)**

$$C_e = 2 * CL - (C_s + C_i)$$

**Total Capacitance (as seen by the crystal)**

$$CL_e = \frac{1}{\left( \frac{1}{C_{e1} + C_{s1} + C_{i1}} + \frac{1}{C_{e2} + C_{s2} + C_{i2}} \right)}$$

- CL ..... Crystal load capacitance
- CL<sub>e</sub> ..... Actual loading seen by crystal using standard value trim capacitors
- C<sub>e</sub> ..... External trim capacitors
- C<sub>s</sub> ..... Stray capacitance (terraced)
- C<sub>i</sub> ..... Internal capacitance (lead frame, bond wires etc.)

**Multifunction Pin Selection**

In CY28551-3, some of the pins can provide different types of frequency, depending on the SEL[1:0] HW strapping pin setting, to support different chipset vendors. The configuration is shown as follows:

SEL[1:0]	LINK/DOT/SATA	SATA/PCIE	Platform
00	LINK	SATA	SIS
01	DOT	SATA	Intel W/Gfx
10	LINK	PCIEX	VIA
11	SATA	PCIEX	Intel

**Dynamic Frequency**

Dynamic Frequency - Dynamic Frequency (DF) is a technique to increase CPU frequency or SRC frequency dynamically from any starting value. The user selects the starting point, either by HW, FSEL, or DAF, then enables DF. After that, DF will dynamically change as determined by DF-N registers.

DF Pin - There are two pins to be used for Dynamic Frequency (DF). When used as DF, these two pins will map to four DF-N registers that correspond to different “N” values for Dynamic Frequency. Any time there is a change in DF, it should load the new value.

DOC[2:1]	DOC N register
00	Original Frequency
01	DF1_N
10	DF2_N
11	DF3_N

DF\_EN bit - This bit enables the DF mode. By default, it is not set. When set, the operating frequency is determined by DF[2:0] pins. Default = 0, (No DF)

**Dial-A-Frequency (CPU & PCIEX)**

This feature allows the user to over clock their system by slowly stepping up the CPU or SRC frequency. When the programmable output frequency feature is enabled, the CPU and SRC frequencies are determined by the following equation:

$$F_{cpu} = G * N/M \text{ or } F_{cpu} = G2 * N, \text{ where } G2 = G/M.$$

“N” and “M” are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively. “G” stands for the PLL Gear Constant, which is determined by the programmed value of FS[E:A]. See Figure 1 for the Gear Constant for each Frequency selection. The PCI Express only allows user control of the N register, the M value is fixed and documented in Figure 1.

In this mode, the user writes the desired N and M value into the DAF I2C registers. The user cannot change only the M value and must change both the M and the N values at the same time, if they require a change to the M value. The user may change only the N value if required.

**Associated Register Bits**

CPU\_DAF Enable – This bit enables CPU DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the CPU\_DAF\_N register. **Note:** the CPU\_DAF\_N and M register must contain valid values before CPU\_DAF is set. Default = 0, (No DAF).

CPU\_DAF\_N – There are nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in the frequency select table in Figure 1.

CPU DAF M – There are 7 bits (for 128 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, the allowable values for M are detailed in the frequency select table in Figure 1.

**SRC\_DAF Enable** – This bit enables SRC DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the SRC\_DAF\_N register. **Note:** the SRC\_DAF\_N register must contain valid values before SRC\_DAF is set. Default = 0, (No DAF).

**SRC\_DAF\_N** – There are nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in the frequency select table in *Figure 1*.

**Recovery** – The recovery mechanism during CPU DAF when the system locks up and the watchdog timer is enabled is determined by the “Watchdog Recovery Mode” and “Watchdog Auto recovery Enable” bits. The possible recovery methods are (A) Auto, (B) Manual (by Recovery N), (C) HW, and (D) No recovery - just send reset signal.

There is no recovery mode for SRC Dial a frequency.

## Software Frequency Select

This mode allows the user to select the CPU output frequencies using the Software Frequency select bits in the SMBUS register.

**FSEL** – There will be four bits (for 16 combinations) to select predetermined CPU frequencies from a table. The table selections are detailed in *Figure 1*.

**FS\_Override** – This bit allows the CPU frequency to be selected from HW or FSEL settings. By default, this bit is not set and the CPU frequency is selected by HW. When this bit is set, the CPU frequency is selected by the FSEL bits. Default = 0.

**Recovery** – The recovery mechanism during FSEL when the system locks up is determined by the “Watchdog Recovery Mode” and “Watchdog Auto recovery Enable” bits. The only possible recovery method is to Hardware Settings. Auto recovery or manual recovery can cause a wrong output frequency because the output divider may have changed with the selected CPU frequency and these recovery methods will not recover the original output divider setting.

## Smooth Switching

The device contains 1 smooth switch circuit that is shared by the CPU PLL and SRC PLL. The smooth switch circuit ensures that when the output frequency changes by overclocking, the transition from the old frequency to the new frequency is a slow, smooth transition containing no glitches. The rate of change of output frequency when using the smooth switch circuit is less than 1 MHz/0.667  $\mu$ s. The frequency overshoot and undershoot will be less than 2%.

The Smooth Switch circuit can be assigned auto or manual. In Auto mode, clock generator will assign smooth switch automatically when the PLL will do overclocking. For manual mode, the smooth switch circuit can be assign to either PLL via Smbus. By default the smooth switch circuit is set to auto mode. Either PLL can still be over-clocked when it does not have control of the smooth switch circuit but it is not guaranteed to transition to the new frequency without large frequency glitches.

It is not recommended to enable over-clocking and change the N values of both PLLs in the same SMBUS block write and use smooth switch mechanism on spread spectrum on/off.

## Watchdog Timer

The Watchdog timer is used in the system in conjunction with overclocking. It is used to provide a reset to a system that has hung up due to overclocking the CPU and the Front side bus. The watchdog is enabled by the user and if the system completes its checkpoints, the system will clear the timer. However, when the timer runs out, there will be a reset pulse generated on the SRESET# pin for 20 ms that is used to reset the system.

When the Watchdog is enabled (WD\_EN = 1) the Watchdog timer will start counting down from a value of Watchdog\_timer \* time scale. If the Watchdog timer reaches 0 before the WD\_EN bit is cleared then it will assert the SRESET# signal and set the Watchdog Alarm bit to 1.

To use the watchdog the SRESET# pin must be enabled by SRESET\_EN pin being sampled LOW by VTTPWRGD# assertion during system boot up.

At any point if during the Watchdog timer countdown, if the time stamp or Watchdog timer bits are changed the timer will reset and start counting down from the new value.

After the Reset pulse, the watchdog will stay inactive until either:

1. A new time stamp or watchdog timer value is loaded.
2. The WD\_EN bit is cleared and then set again.

## Watchdog Register Bits

The following register bits are associated with the Watchdog timer:

**Watchdog Enable** – This bit (by default) is not set, which disables the Watchdog. When set, the Watchdog is enabled. Also, when there is a transition from LOW to HIGH, the timer reloads. Default = 0, disable

**Watchdog Timer** – There will be three bits (for seven combinations) to select the timer value. Default = 000, the value '000' is a reserved test mode.

**Watchdog Alarm** – This bit is a flag and when it is set, it indicates that the timer has expired. This bit is not set by default. When the bit is set, the user is allowed to clear. Default = 0.

**Watchdog Time Scale** – This bit selects the multiplier. When this bit is not set, the multiplier will be 250 ms. When set (by default), the multiplier will be 3s. Default = 1

**Watchdog Reset Mode** – This selects the Watchdog Reset Mode. When this bit is not set (by default), the Watchdog will send a reset pulse and reload the recovery frequency depends on Watchdog Recovery Mode setting. When set, it just send a reset pulse. Default = 0, Reset & Recover Frequency.

**Watchdog Recovery Mode** – This bit selects the location to recover from. One option is to recover from the HW settings (already stored in SMBUS registers for readback capability) and the second is to recover from a register called “Recovery N”. Default = 0 (Recover from the HW setting)

Watchdog Autorecovery Enable – This bit by default is set and the recovered values are automatically written into the “Watchdog Recovery Register” and reloaded by the Watchdog function. When this bit is not set, the user is allowed to write to the “Watchdog Recovery Register”. The value stored in the “Watchdog Recovery Register” will be used for recovery. Default = 1, Autorecovery.

Watchdog Recovery Register – This is a nine-bit register to store the watchdog N recovery value. This value can be written by the Auto recovery or User depending on the state of the “Watchdog Auto Recovery Enable bit”.

## Watchdog Recovery Modes

There are three operating modes that require Watchdog recovery. The modes are Dial-A-Frequency (DAF), Dynamic Clocking (DF), or Frequency Select. There are 4 different recovery modes: the following sections list the operating mode and the recovery mode associated with it.

### *Recover to Hardware M, N, O*

When this recovery mode is selected, in the event of a Watchdog timeout, the original M, N, and O values that were latched by the HW FSEL pins at chip boot-up should be reloaded.

### *Autorecovery*

When this recovery mode is selected, in the event of a Watchdog timeout, the M and N values stored in the Recovery M and N registers should be reloaded. The current values of M and N will be latched into the internal recovery M and N registers by the WD\_EN bit being set.

### *Manual Recovery*

When this recovery mode is selected, in the event of a Watchdog timeout, the N value as programmed by the user in the N recovery register, and the M value that is stored in the Recovery M register (not accessible by the user) should be restored. The current M value should be latched M recovery register by the WD\_EN bit being set.

### *No Recovery*

If no recovery mode is selected, in the event of a Watchdog time out, the device should just assert the SRESET# and keep the current values of M and N

## Software Reset

Software reset is a reset function that is used to send out a pulse from the SRESET# pin. It is controlled by the SW\_RESET enable register bit. Upon completion of the byte/word/block write in which the SW\_RESET bit was set, the device will send a RESET pulse on the SRESET# pin. The duration of the SRESET# pulse should be the same as the duration of the SRESET# pulse after a Watchdog timer time out.

After the SRESET# pulse is asserted the SW\_RESET bit should be automatically cleared by the device.

## PD Clarification

The VTT\_PWRGD#/PD pin is a dual-function pin. During initial power-up, the pin functions as VTT\_PWRGD#. Once VTT\_PWRGD# has been sampled LOW by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous active HIGH input used to shut off all clocks cleanly prior to shutting off power to the device. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted HIGH, all clocks need to be driven to a LOW value and held prior to turning off the VCOs and the crystal oscillator

## PD Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs must be held LOW on their next HIGH-to-LOW transition and differential clocks must held HIGH or tri-stated (depending on the state of the control register drive mode bit) on the next diff clock# HIGH-to-LOW transition within 4 clock periods. When the SMBus PD drive mode bit corresponding to the differential (CPU, SRC, and DOT) clock output of interest is programmed to '0', the clock output must be held with “Diff clock” pin driven HIGH at  $2 \times I_{ref}$ , and “Diff clock#” tri-state. If the control register PD drive mode bit corresponding to the output of interest is programmed to “1”, then both the “Diff clock” and the “Diff clock#” are tri-state. Note *Figure 4* shows CPUT = 133 MHz and PD drive mode = '1' for all differential outputs. This diagram and description is applicable to valid CPU frequencies 100, 133, 166, and 200 MHz. In the event that PD mode is desired as the initial power-on state, PD must be asserted HIGH in less than 10  $\mu$ s after asserting Vtt\_PwrGd#.

## PD Deassertion

The power-up latency needs to be less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a tri-state condition resulting from power-down must be driven HIGH in less than 300  $\mu$ s of PD deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are to be enabled within a few clock cycles of each other. *Figure 5* is an example showing the relationship of clocks coming up. Unfortunately, we can not show all possible combinations, designers need to insure that from the first active clock output to the last takes no more than two full PCI clock cycles.

## CPU\_STP# Clarification

The CPU\_STP# signal is an active low input used for cleanly stopping and starting the CPU outputs while the rest of the clock generator continues to function. Note that the assertion and de-assertion of this signal is absolutely asynchronous.

## CPU\_STP# Assertion

The CPU\_STP# signal is an active low input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU\_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU\_STP# will be stopped after being sampled by 2-6 rising edges of the internal CPUC clock. The final state of the

Figure 4. PD Assertion Timing Waveform

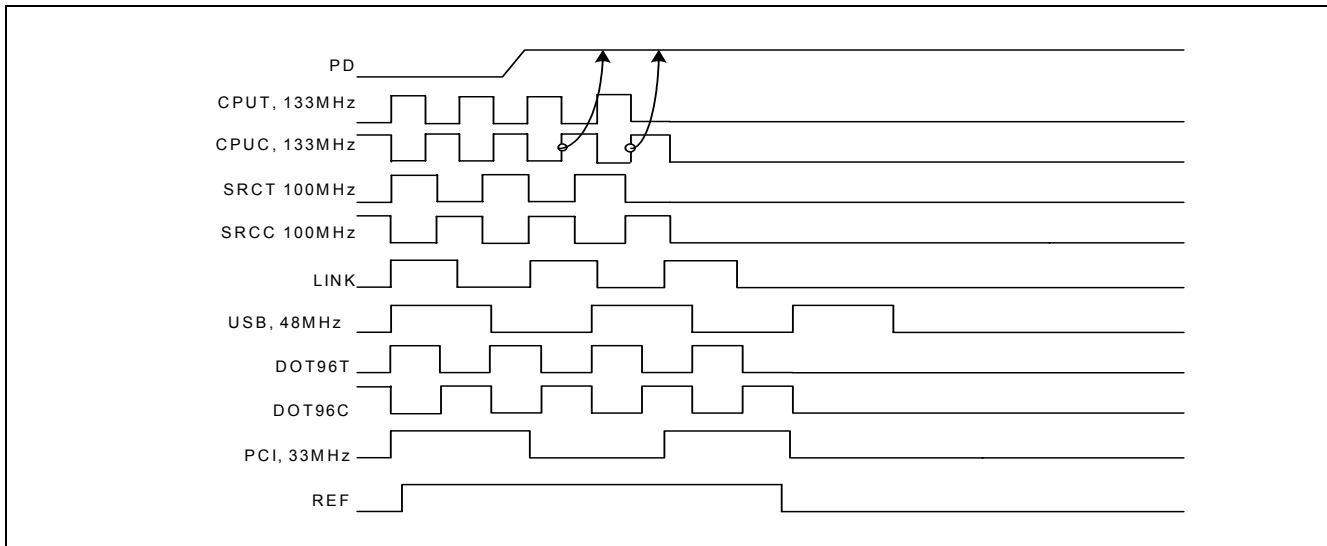
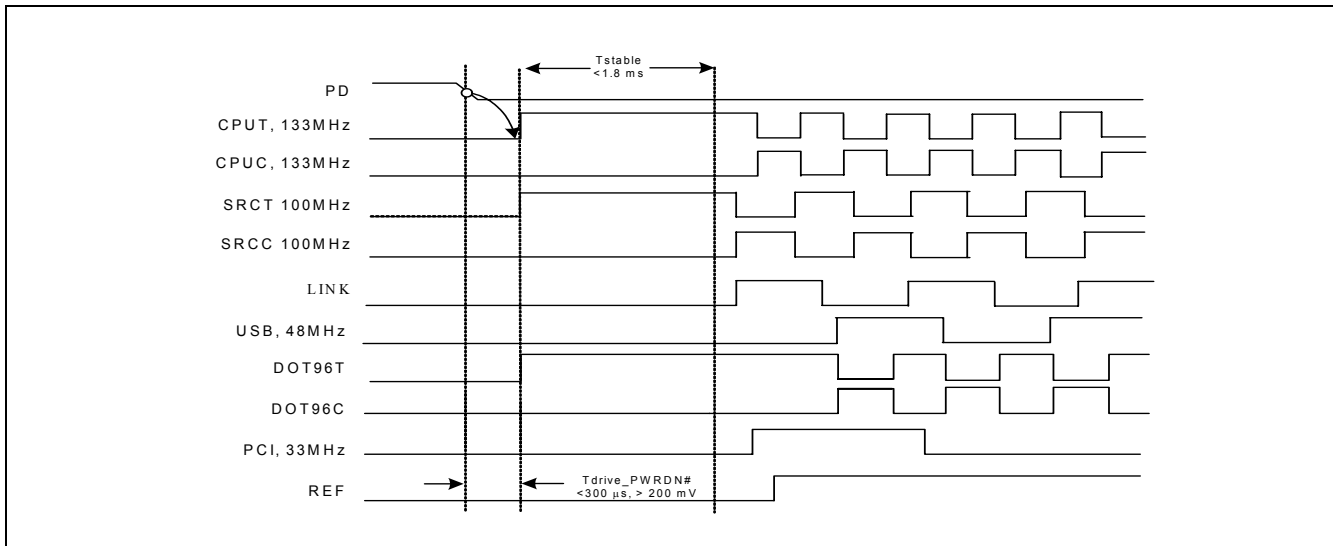


Figure 5. PD Deassertion Timing Waveform



stopped CPU clock is Low due to tristate, both CPUT and CPUC outputs will not be driven.

**PU\_STP# De-Assertion**

The de-assertion of the CPU\_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produce when the clock resumes. The maximum latency from the de-assertion to active outputs is between 2-6 CPU clock periods (2 clocks are shown). If the control register tristate bit corresponding to the output of interest is programmed to '1', then the stopped CPU outputs will be driven high within 10ns of CPU\_Stop# de-assertion to a voltage greater than 200mV

**PCI\_STP# Clarification**

The PCI\_STP# signal is an active low input used for cleanly stopping and starting the PCI and PCIEX outputs while the rest of the clock generator continues to function. The PCIF and PCIEX clocks are special in that they can be programmed to ignore PCI\_STP# by setting the register bit corresponding to the output of interest to free running. Outputs set to free running will ignore both the PCI\_STP# pin.

**PCI\_STP# Assertion**

The impact of asserting the PCI\_STP# signal will be the following. The clock chip is to sample the PCI\_STP# signal on a rising edge of PCIF clock. After detecting the PCI\_STP# assertion low, all PCI and stoppable PCIF clocks will latch low



on their next high to low transition. After the PCI clocks are latched low, the stoppable PCIEX clocks will latch to low due to tristate as show below. The one PCI clock latency as shown is critical to system functionality, any violation of this may result in system failure. The  $T_{su\_pci\_stp\#}$  is the setup time required by the clock generator to correctly sample the  $PCI\_STP\#$  assertion, this time is 10 ns minimum.

**PCI\_STP# De-Assertion**

The de-assertion of the  $PCI\_STP\#$  signal is to function as follows. The de-assertion of the  $PCI\_STP\#$  signal is to be sampled on the rising edge of the PCIF free running clock domain. After detecting  $PCI\_STP\#$  de-assertion, all PCI, stoppable PCIF and Stoppable PCIEX clocks will resume in a glitch free manner. The PCI and PCIEX clock resume latency should exactly match the 1 PCI clock latency required for  $PCI\_STP\#$  entry. The stoppable PCIEX clocks must be driven high within 15ns of  $PCI\_STP\#$  de-assertion. The drawing below shows the appropriate relationship. The  $T_{su\_cpu\_stp\#}$  is the setup time required by the clock generator to correctly sample the  $PCI\_STP\#$  de-assertion, this time is 10 ns minimum.

**CLKREQ# Clarification**

The  $CLKREQ\#$  signals are active low input used for clean stopping and starting selected SRC outputs. The outputs controlled by  $CLKREQ\#$  are determined by the settings in register bytes 10 and 11. The  $CLKREQ\#$  signal is a

de-bounced signal in that its state must remain unchanged during two consecutive rising edges of DIFC to be recognized as a valid assertion or de-assertion. (The assertion and de-assertion of this signal is absolutely asynchronous)

**CLKREQ# Assertion**

All differential outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the de-assertion to active outputs is between 2-6 PCIEX clock periods (2 clocks are shown) with all  $CLKREQ\#$  outputs resuming simultaneously. If the  $CLKREQ\#$  drive mode is tristate, the all stopped PCIEX outputs must be driven high within 10 ns of  $CLKREQ\#$  de-assertion to a voltage greater than 200mV

**CLKREQ# De-Assertion**

The impact of asserting the  $CLKREQ\#$  pins is all DIF outputs that are set in the control registers to stoppable via assertion of  $CLKREQ\#$  are to be stopped after their next transition. When the control register  $CLKREQ\#$  drive mode bit is programmed to '0', the final state of all stopped PCIEX signals is  $PCIEXT$  clock = High and  $PCIEXC$  = Low. There is to be no change to the output drive current values,  $SRCT$  will be driven high with a current value equal  $6 \times I_{ref}$ , When the control register  $CLKREQ\#$  drive mode bit is programmed to '1', the final state of all stopped DIF signals is low, both  $PCIEXT$  clock and  $PCIEXC$  clock outputs will not be driven.

Figure 6. CPU\_STP# Assertion Timing waveform

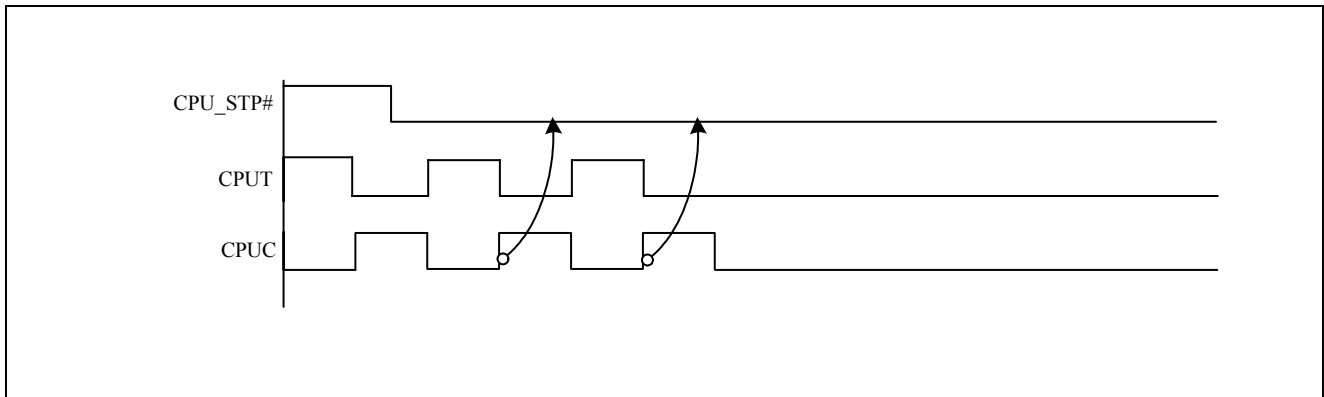


Figure 7. CPU\_STP# De-Assertion

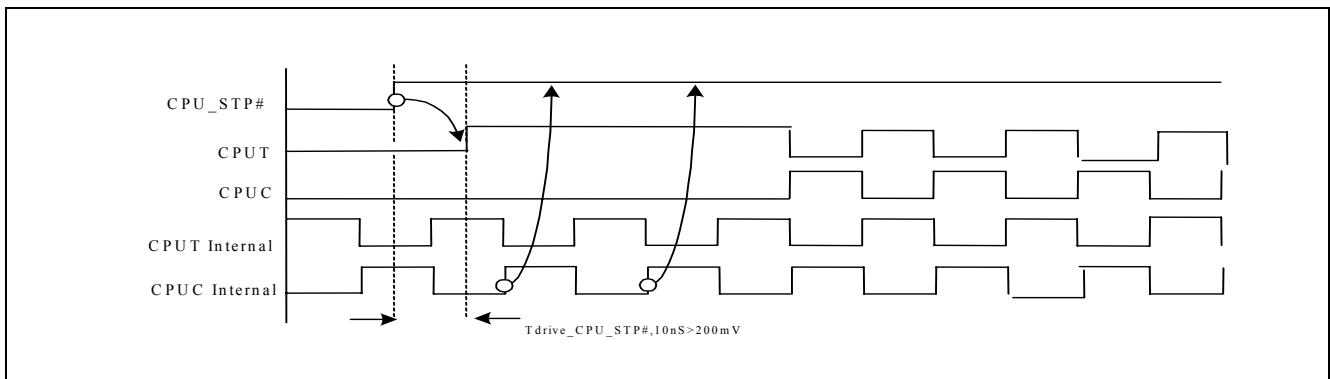


Figure 8. PCI\_STP# Assertion

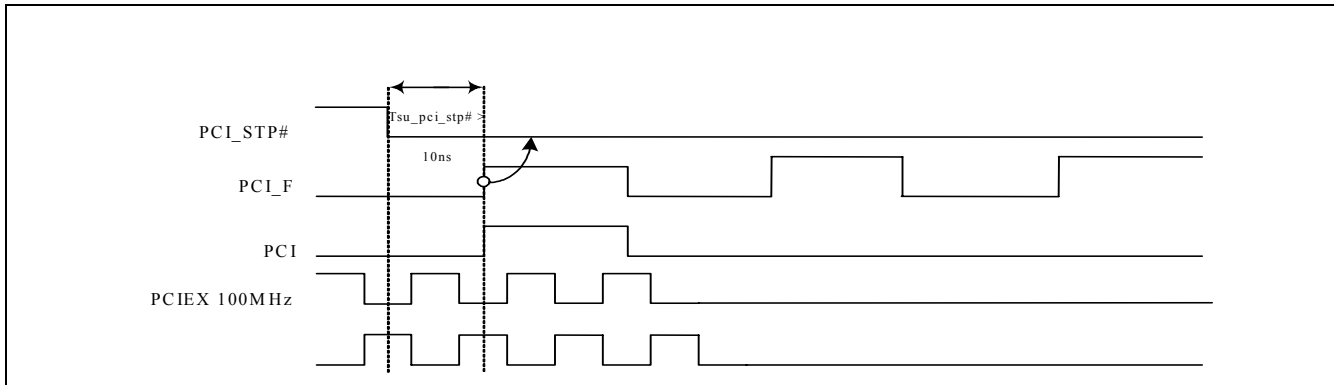


Figure 9. PCI\_STP# De-Assertion

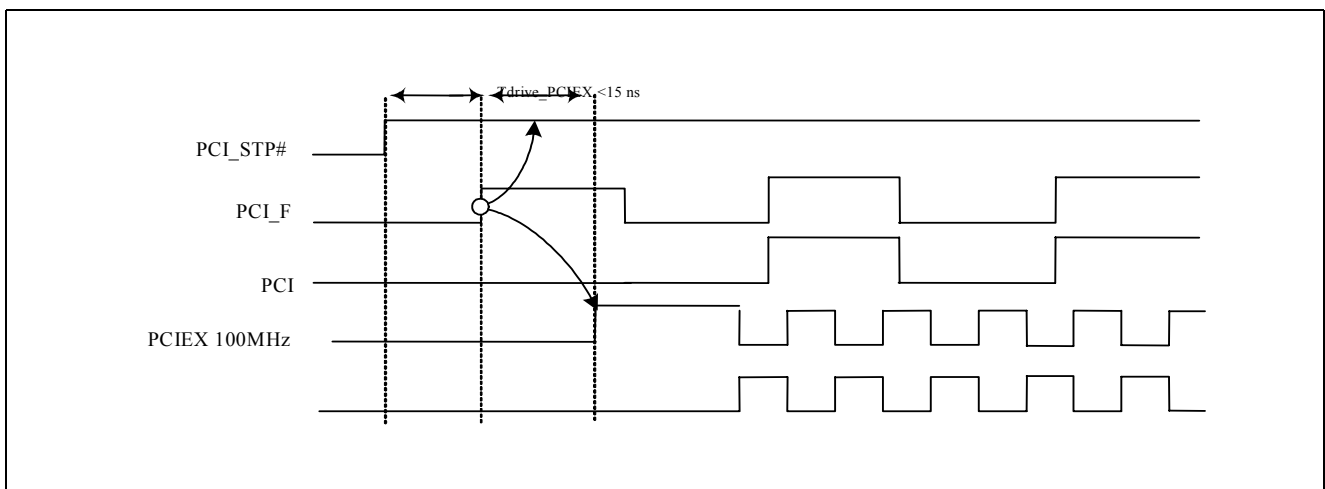


Figure 10. CLKREQ# De-Assertion

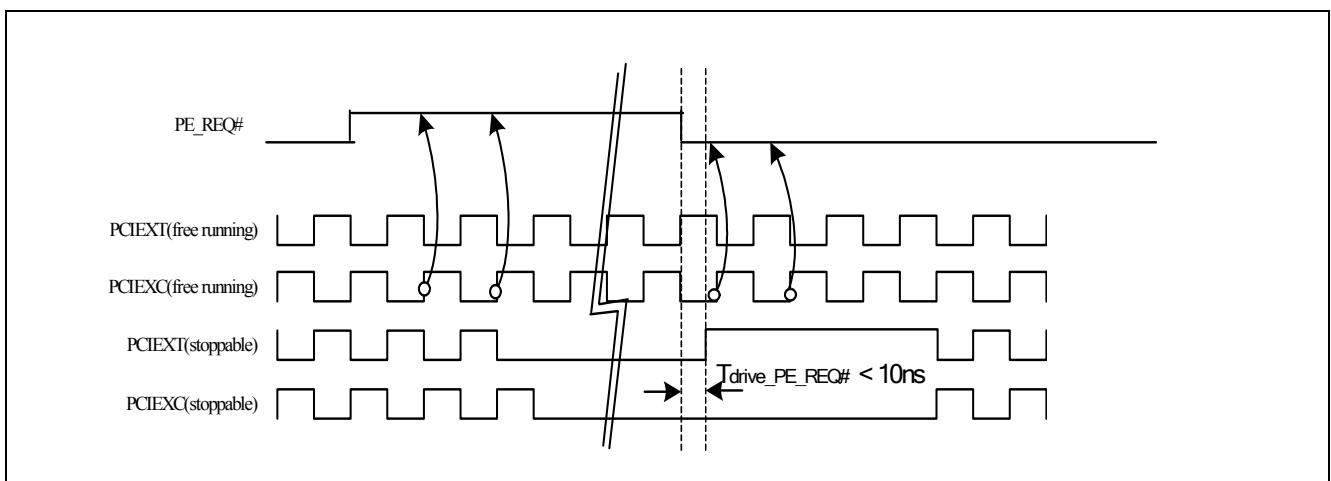


Figure 11. VTT\_PWRGD# Timing Diagram

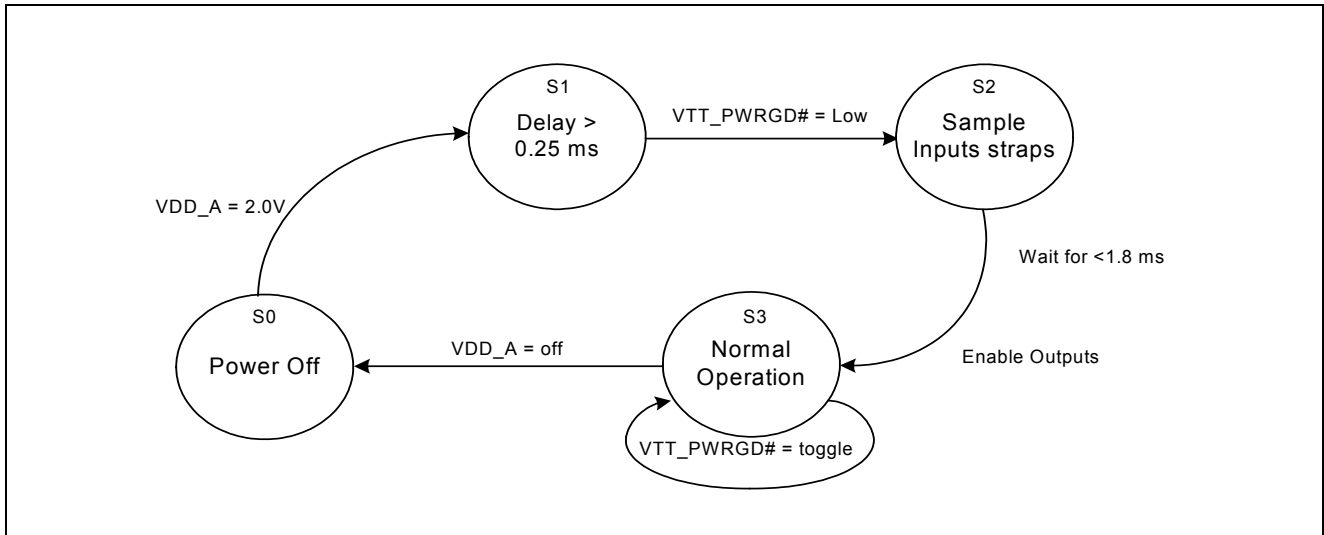
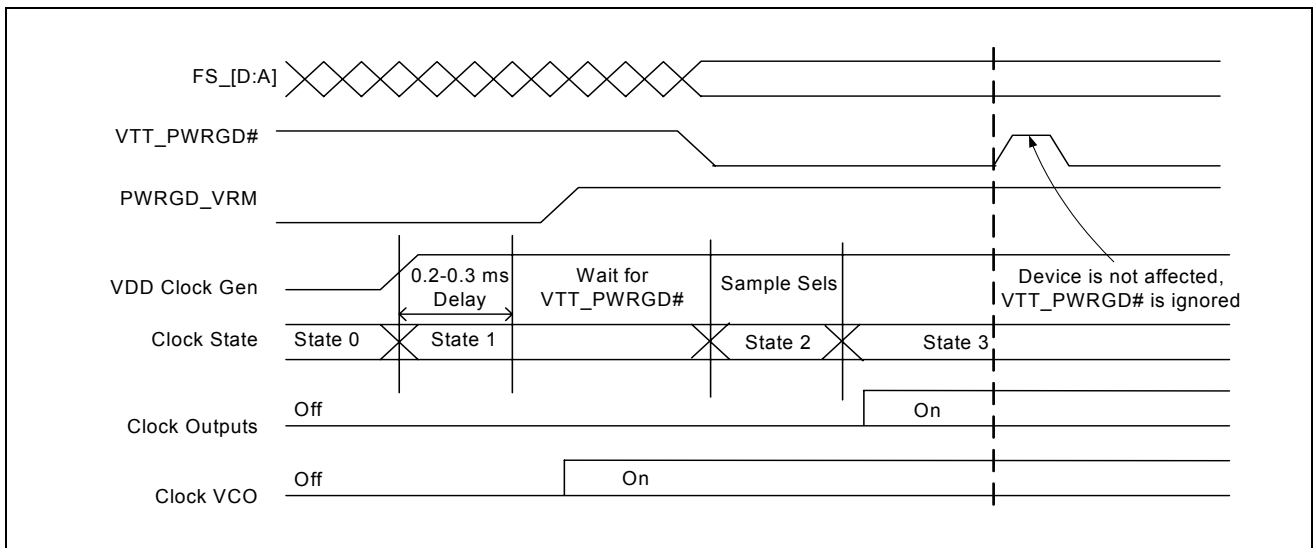


Figure 12. VTT\_PWRGD# Timing Diagram



**Absolute Maximum Conditions**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage		-0.5	4.6	V
V <sub>DD_A</sub>	Analog Supply Voltage		-0.5	4.6	V
V <sub>IN</sub>	Input Voltage	Relative to V <sub>SS</sub>	-0.5	V <sub>DD</sub> + 0.5	VDC
T <sub>S</sub>	Temperature, Storage	Non-functional	-65	150	°C
T <sub>A</sub>	Temperature, Operating Ambient	Functional	0	70	°C
T <sub>J</sub>	Temperature, Junction	Functional	-	150	°C
∅ <sub>JC</sub>	Dissipation, Junction to Case	Mil-STD-883E Method 1012.1	-	20	°C/W
∅ <sub>JA</sub>	Dissipation, Junction to Ambient	JEDEC (JESD 51)	-	60	°C/W
ESD <sub>HBM</sub>	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	-	V
UL-94	Flammability Rating	At 1/8 in.	V-0		
MSL	Moisture Sensitivity Level		1		

**Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**DC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
All V <sub>DDs</sub>	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V <sub>IL2C</sub>	Input Low Voltage	SDATA, SCLK	-	1.0	V
V <sub>IH2C</sub>	Input High Voltage	SDATA, SCLK	2.2	-	V
V <sub>IL_FS</sub>	FS_[A:D] Input Low Voltage		V <sub>SS</sub> - 0.3	0.35	V
V <sub>IH_FS</sub>	FS_[A:D] Input High Voltage		0.7	V <sub>DD</sub> + 0.5	V
V <sub>IL</sub>	3.3V Input Low Voltage		V <sub>SS</sub> - 0.3	0.8	V
V <sub>IH</sub>	3.3V Input High Voltage		2.0	V <sub>DD</sub> + 0.3	V
I <sub>IL</sub>	Input Low Leakage Current	Except internal pull-up resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>	-5	-	μA
I <sub>IH</sub>	Input High Leakage Current	Except internal pull-down resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>	-	5	μA
V <sub>OL</sub>	3.3V Output Low Voltage	I <sub>OL</sub> = 1 mA	-	0.4	V
V <sub>OH</sub>	3.3V Output High Voltage	I <sub>OH</sub> = -1 mA	2.4	-	V
I <sub>OZ</sub>	High-impedance Output Current		-10	10	μA
C <sub>IN</sub>	Input Pin Capacitance		3	5	pF
C <sub>OUT</sub>	Output Pin Capacitance		3	5	pF
L <sub>IN</sub>	Pin Inductance		-	7	nH
V <sub>XIH</sub>	Xin High Voltage		0.7V <sub>DD</sub>	V <sub>DD</sub>	V
V <sub>XIL</sub>	Xin Low Voltage		0	0.3V <sub>DD</sub>	V
I <sub>DD3.3V</sub>	Dynamic Supply Current	At max. load and freq. per <i>Figure 15</i>	-	500	mA
I <sub>PT3.3V</sub>	Power-down Supply Current	PD asserted, Outputs Tri-state	-	12	mA

**AC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
<b>Crystal</b>					
T <sub>DC</sub>	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T <sub>PERIOD</sub>	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T <sub>R</sub> /T <sub>F</sub>	XIN Rise and Fall Times	Measured between 0.3V <sub>DD</sub> and 0.7V <sub>DD</sub>	–	10.0	ns
T <sub>CCJ</sub>	XIN Cycle to Cycle Jitter	As an average over 1-μs duration	–	500	ps
L <sub>ACC</sub>	Long-term Accuracy	Over 150 ms	–	300	ppm
<b>CPU at 0.7V (SSC refers to –0.5% spread spectrum)</b>					
T <sub>DC</sub>	CPUT and CPUC Duty Cycle	Measured at crossing point V <sub>OX</sub> @ 0.1s	45	55	%
T <sub>PERIOD</sub>	100-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub> @ 0.1s	9.99900	10.0100	ns
T <sub>PERIOD</sub>	133-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub> @ 0.1s	7.49925	7.50075	ns
T <sub>PERIOD</sub>	166-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub> @ 0.1s	5.99940	6.00060	ns
T <sub>PERIOD</sub>	200-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub> @ 0.1s	4.99950	5.00050	ns
T <sub>PERIOD</sub>	266-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub> @ 0.1s	3.74963	3.75038	ns
T <sub>PERIOD</sub>	333-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub> @ 0.1s	2.99970	3.00030	ns
T <sub>PERIOD</sub>	400-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub> @ 0.1s	2.49975	2.50025	ns
T <sub>PERIODSS</sub>	100-MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub> @ 0.1s	9.99900	10.0100	ns
T <sub>PERIODSS</sub>	133-MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub> @ 0.1s	7.49925	7.50075	ns
T <sub>PERIODSS</sub>	166-MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub> @ 0.1s	5.99940	6.00060	ns
T <sub>PERIODSS</sub>	200-MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub> @ 0.1s	4.99950	5.00050	ns
T <sub>PERIODSS</sub>	266-MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub> @ 0.1s	3.74963	3.75038	ns
T <sub>PERIODSS</sub>	333-MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub> @ 0.1s	2.99970	3.00030	ns
T <sub>PERIODSS</sub>	400-MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub> @ 0.1s	2.49975	2.50025	ns
T <sub>PERIODAbs</sub>	100-MHz CPUT and CPUC Absolute period	Measured at crossing point V <sub>OX</sub> @ 1 clock	9.91400	10.0860	ns
T <sub>PERIODAbs</sub>	133-MHz CPUT and CPUC Absolute period	Measured at crossing point V <sub>OX</sub> @ 1 clock	7.41425	7.58575	ns
T <sub>PERIODAbs</sub>	166-MHz CPUT and CPUC Absolute period	Measured at crossing point V <sub>OX</sub> @ 1 clock	5.91440	6.08560	ns
T <sub>PERIODAbs</sub>	200-MHz CPUT and CPUC Absolute period	Measured at crossing point V <sub>OX</sub> @ 1 clock	4.91450	5.08550	ns
T <sub>PERIODAbs</sub>	266-MHz CPUT and CPUC Absolute period	Measured at crossing point V <sub>OX</sub> @ 1 clock	3.66463	3.83538	ns
T <sub>PERIODAbs</sub>	333-MHz CPUT and CPUC Absolute period	Measured at crossing point V <sub>OX</sub> @ 1 clock	2.91470	3.08530	ns
T <sub>PERIODAbs</sub>	400-MHz CPUT and CPUC Absolute period	Measured at crossing point V <sub>OX</sub> @ 1 clock	2.41475	2.58525	ns
T <sub>PERIODSSAbs</sub>	100-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V <sub>OX</sub> @ 1 clock	9.91400	10.1363	ns
T <sub>PERIODSSAbs</sub>	133-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V <sub>OX</sub> @ 1 clock	7.41425	7.62345	ns
T <sub>PERIODSSAbs</sub>	166-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V <sub>OX</sub> @ 1 clock	5.91440	6.11576	ns

**AC Electrical Specifications** (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T <sub>PERIODSSAbs</sub>	200-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V <sub>OX</sub> @ 1 clock	4.91450	5.11063	ns
T <sub>PERIODSSAbs</sub>	266-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V <sub>OX</sub> @ 1 clock	3.66463	3.85422	ns
T <sub>PERIODSSAbs</sub>	333-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V <sub>OX</sub> @ 1 clock	2.91470	3.10038	ns
T <sub>PERIODSSAbs</sub>	400-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V <sub>OX</sub> @ 1 clock	2.41475	2.59782	ns
T <sub>SKEW</sub>	CPU0 to CPU1	Measured at crossing point V <sub>OX</sub>	–	100	ps
T <sub>CCJ</sub>	CPUT/C Cycle to Cycle Jitter	Measured at crossing point V <sub>OX</sub>	–	85	ps
L <sub>ACC</sub>	Long Term accuracy	Measured at crossing point V <sub>OX</sub>	–	100	ppm
T <sub>R</sub> /T <sub>F</sub>	CPUT and CPUC Rise and Fall Times	Measured differentially from ±150 mV	2.5	8	V/ns
T <sub>RFM</sub>	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V <sub>max</sub>	Max output Voltage	Math averages <i>Figure 15</i>	–	1.15	V
V <sub>min</sub>	Min output Voltage	Math averages <i>Figure 15</i>	–0.3	–	V
V <sub>OX</sub>	Crossing Point Voltage at 0.7V Swing		300	550	mV
<b>CPU at 3.3V (SSC refers to –0.5% spread spectrum)</b>					
T <sub>R</sub>	Output Rise Edge Rate	Measured @ K8 test load using VO <sub>CM</sub> ± 400 mV, 0.850V to 1.650V	2	7	V/ns
T <sub>F</sub>	Output Fall Edge Rate	Measured @ K8 test load using VO <sub>CM</sub> ± 400 mV, 1.650V to 0.850V	2	7	V/ns
V <sub>DIFF</sub>	Differential Voltage	Measured @ K8 test load (single-ended)	0.4	2.3	V
Δ <sub>DIFF</sub>	Change in V <sub>DIFF</sub> _DC Magnitude	Measured @ K8 test load (single-ended)	–150	150	mV
V <sub>CM</sub>	Common Mode Voltage	Measured @ K8 test load (single-ended)	1.05	1.45	V
ΔV <sub>CM</sub>	Change in V <sub>CM</sub>	Measured @ K8 test load (single-ended)	–200	200	mV
T <sub>DC</sub>	Duty Cycle	Measured at V <sub>OX</sub>	45	53	%
T <sub>CYC</sub>	Jitter, Cycle to Cycle	Measured at V <sub>OX</sub>	0	200	ps
T <sub>ACCUM</sub>	Jitter, Accumulated	Measured at V <sub>OX</sub>	–1000	1000	ps
<b>PCIEX</b>					
T <sub>DC</sub>	PCIEXT and PCIEXC Duty Cycle	Measured at crossing point V <sub>OX</sub>	45	55	%
T <sub>PERIOD</sub>	100-MHz PCIEXT and PCIEXC Period	Measured at crossing point V <sub>OX</sub> @ 0.1s	9.99900	10.0010	ns
T <sub>PERIODSS</sub>	100-MHz PCIEXT and PCIEXC Period, SSC	Measured at crossing point V <sub>OX</sub> @ 0.1s	9.99900	10.0010	ns
T <sub>PERIODAbs</sub>	100-MHz PCIEXT and PCIEXC Absolute Period	Measured at crossing point V <sub>OX</sub> @ 1 clock	9.87400	10.1260	ns
T <sub>PERIODSSAbs</sub>	100-MHz PCIEXT and PCIEXC Absolute Period, SSC	Measured at crossing point V <sub>OX</sub> @ 1 clock	9.87400	10.1763	ns
T <sub>SKEW</sub>	Any PCIEXT/C to PCIEXT/C Clock Skew	Measured at crossing point V <sub>OX</sub>	–	250	ps
T <sub>CCJ</sub>	PCIEXT/C Cycle to Cycle Jitter	Measured at crossing point V <sub>OX</sub>	–	125	ps
L <sub>ACC</sub>	PCIEXT/C Long Term Accuracy	Measured at crossing point V <sub>OX</sub>	–	100	ppm
T <sub>R</sub> /T <sub>F</sub>	PCIEXT and PCIEXC Rise and Fall Times	Measured differentially from ±150 mV	2.5	8	V/ns
T <sub>RFM</sub>	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V <sub>max</sub>	Max output Voltage	Math averages <i>Figure 15</i>	–	1.15	V
V <sub>min</sub>	Min output Voltage	Math averages <i>Figure 15</i>	–0.3	–	V

**AC Electrical Specifications** (continued)

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>OX</sub>	Crossing Point Voltage at 0.7V Swing		300	550	mV
<b>DOT</b>					
T <sub>DC</sub>	DOT96T and DOT96C Duty Cycle	Measured at crossing point V <sub>OX</sub>	45	55	%
T <sub>PERIOD</sub>	DOT96T and DOT96C Period	Measured at crossing point V <sub>OX</sub> @ 0.1s	10.4156	10.4177	ns
T <sub>PERIODAbs</sub>	DOT96T and DOT96C Absolute Period	Measured at crossing point V <sub>OX</sub> @ 0.1s	10.1656	10.6677	ns
T <sub>CCJ</sub>	DOT96T/C Cycle to Cycle Jitter	Measured at crossing point V <sub>OX</sub>	–	250	ps
L <sub>ACC</sub>	DOT96T/C Long Term Accuracy	Measured at crossing point V <sub>OX</sub>	–	300	ppm
T <sub>LTJ</sub>	Long Term jitter	Measurement taken from cross point V <sub>OX</sub> @ 10 μs	–	700	ps
T <sub>R</sub> /T <sub>F</sub>	SRCT and SRCC Rise and Fall Time	Measured differentially from ±150 mV	2.5	8	V/ns
T <sub>RFM</sub>	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V <sub>max</sub>	Max output Voltage	Math averages <i>Figure 15</i>	–	1.15	V
V <sub>min</sub>	Min output Voltage	Math averages <i>Figure 15</i>	–0.3	–	V
V <sub>OX</sub>	Crossing Point Voltage at 0.7V Swing		300	550	mV
<b>LINK - 133 MHz</b>					
T <sub>DC</sub>	LINK (133 MHz) Duty Cycle	Measurement at 1.5V	45	55	%
T <sub>PERIOD</sub>	Spread Disabled LINK (133 MHz) Period	Measurement at 1.5V	7.50	7.56	ns
T <sub>PERIODSS</sub>	Spread Enabled LINK (133 MHz) Period, SSC	Measurement at 1.5V	7.50	7.56	ns
T <sub>R</sub> /T <sub>F</sub>	LINK (133 MHz) rising and falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T <sub>CCJ</sub>	LINK (133 MHz) Cycle to Cycle Jitter	Measurement at 1.5V	–	250	ps
T <sub>SKEW</sub>	Any LINK Clock Skew	Measurement at 1.5V	–	175	ps
L <sub>ACC</sub>	LINK (133 MHz) Long Term Accuracy	Measured at crossing point V <sub>OX</sub>	–	300	ppm
<b>LINK - 66 MHz</b>					
T <sub>DC</sub>	LINK (66 MHz) Duty Cycle	Measurement at 1.5V	45	55	%
T <sub>PERIOD</sub>	Spread Disabled LINK (66 MHz) Period	Measurement at 1.5V	14.9955	15.0045	ns
T <sub>PERIODSS</sub>	Spread Enabled LINK (66 MHz) Period, SSC	Measurement at 1.5V	14.9955	15.0045	ns
T <sub>R</sub> /T <sub>F</sub>	LINK (66 MHz) rising and falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T <sub>CCJ</sub>	LINK (66 MHz) Cycle to Cycle Jitter	Measurement at 1.5V	–	250	ps
T <sub>SKEW</sub>	Any LINK Clock Skew	Measurement at 1.5V	–	175	ps
L <sub>ACC</sub>	LINK (66 MHz) Long Term Accuracy	Measured at crossing point V <sub>OX</sub>	–	300	ppm
<b>PCI</b>					
T <sub>DC</sub>	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T <sub>PERIOD</sub>	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.99100	30.00900	ns
T <sub>PERIODSS</sub>	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	29.9910	30.15980	ns
T <sub>PERIODAbs</sub>	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.49100	30.50900	ns
T <sub>PERIODSSAbs</sub>	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	29.49100	30.65980	ns
T <sub>HIGH</sub>	PCIF and PCI high time	Measurement at 2.4V	12.0	–	ns
T <sub>LOW</sub>	PCIF and PCI low time	Measurement at 0.4V	12.0	–	ns
T <sub>R</sub> /T <sub>F</sub>	PCIF and PCI rising and falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns

**AC Electrical Specifications** (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T <sub>SKEW</sub>	Any PCI clock to Any PCI clock Skew	Measurement at 1.5V	–	500	ps
T <sub>CCJ</sub>	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
<b>USB</b>					
T <sub>DC</sub>	Duty Cycle	Measurement at 1.5V. <i>In High Drive mode</i>	45	55	%
T <sub>PERIOD</sub>	Period	Measurement at 1.5V	20.83125	20.83542	ns
T <sub>PERIODAbs</sub>	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T <sub>HIGH</sub>	USB high time	Measurement at 2.4V	8.094	10.5	ns
T <sub>LOW</sub>	USB low time	Measurement at 0.4V	7.694	10.5	ns
T <sub>R</sub> /T <sub>F</sub>	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	2.0	V/ns
T <sub>CCJ</sub>	Cycle to Cycle Jitter	Measurement at 1.5V	–	350	ps
L <sub>ACC</sub>	48M Long Term Accuracy	Measured at crossing point V <sub>OX</sub>	–	100	ppm
T <sub>LTJ</sub>	Long Term jitter	Measurement taken from cross point V <sub>OX</sub> @1 μs	–	1.0	ns
<b>24M</b>					
T <sub>DC</sub>	Duty Cycle	Measurement at 1.5V. <i>In High Drive mode</i>	45	55	%
T <sub>PERIOD</sub>	Period	Measurement at 1.5V	41.6646	41.6688	ns
T <sub>HIGH</sub>	USB high time	Measurement at 2.4V	18.8323	18.8323	ns
T <sub>LOW</sub>	USB low time	Measurement at 0.4V	18.8323	18.8323	ns
T <sub>R</sub> /T <sub>F</sub>	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T <sub>CCJ</sub>	Cycle to Cycle Jitter	Measurement at 1.5V	–	350	ps
L <sub>ACC</sub>	48M Long Term Accuracy	Measured at crossing point V <sub>OX</sub>	–	100	ppm
T <sub>LTJ</sub>	Long Term jitter	Measurement taken from cross point V <sub>OX</sub> @1 μs	–	1.0	ns
<b>REF</b>					
T <sub>DC</sub>	REF Duty Cycle	Measurement at 1.5V	45	55	%
T <sub>PERIOD</sub>	REF Period	Measurement at 1.5V	69.8203	69.8622	ns
T <sub>PERIODAbs</sub>	REF Absolute Period	Measurement at 1.5V	68.82033	70.86224	ns
T <sub>R</sub> /T <sub>F</sub>	REF Rise and Fall Times Edge rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T <sub>CCJ</sub>	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
T <sub>SKEW</sub>	REF Clock to REF Clock	Measurement at 1.5V	–	500	ps
L <sub>ACC</sub>	Long Term Accuracy	Measurement at 1.5V	–	300	ppm
<b>ENABLE/DISABLE and SET-UP</b>					
T <sub>STABLE</sub>	Clock Stabilization from Power-up		–	1.8	ms

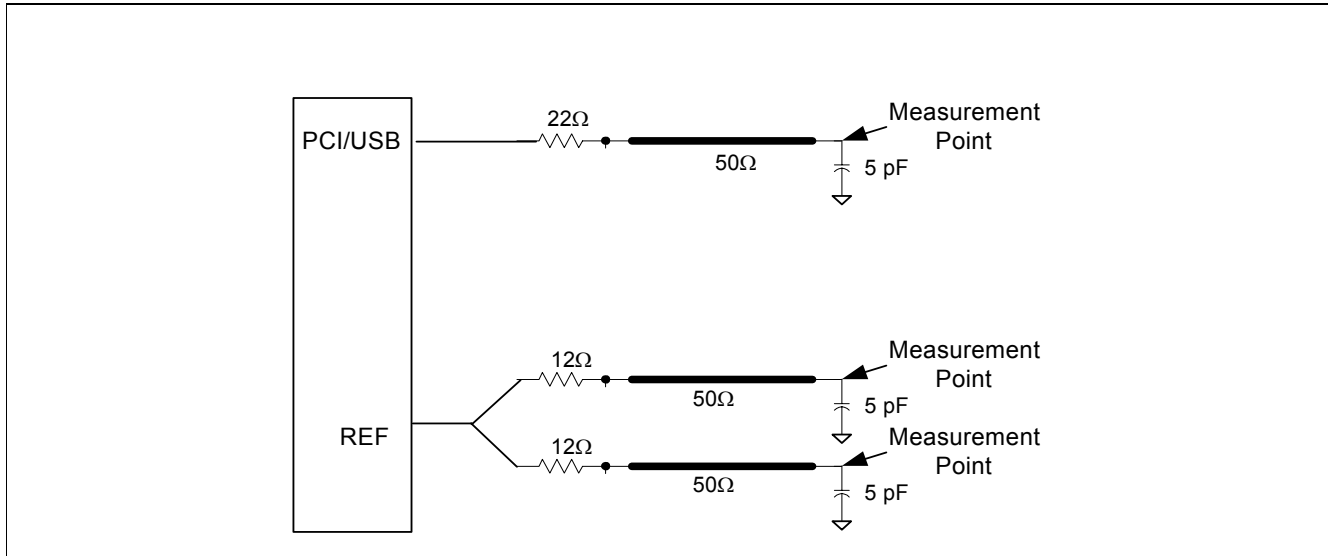


### Test and Measurement Set-up

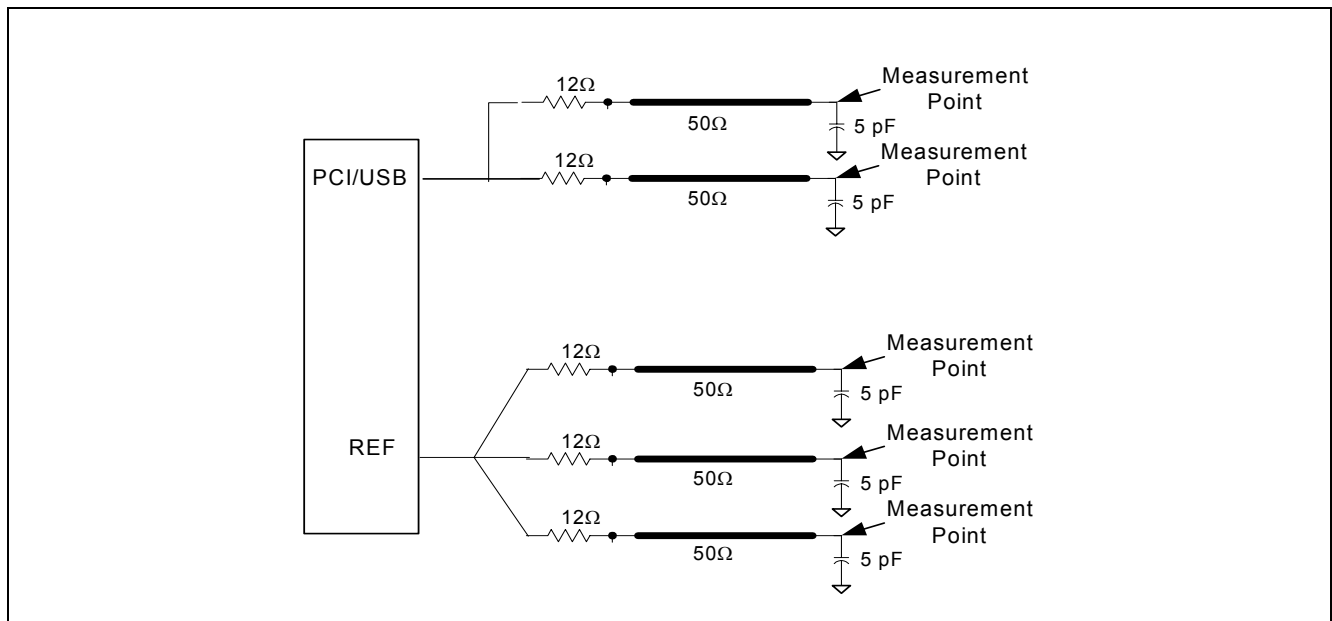
#### For PCI/USB and 24M Single-ended Signals and Reference

The following diagrams show the test load configurations for the single-ended PCI, USB, 24M, and REF output signals.

**Figure 13. Single-ended Load Configuration**



**Figure 14. Single-ended Load Configuration HIGH DRIVE OPTION**



The following diagrams show the test load configuration for the differential CPU and PCIeX outputs.

Figure 15. Differential Load Configuration for 0.7 Push Pull Clock

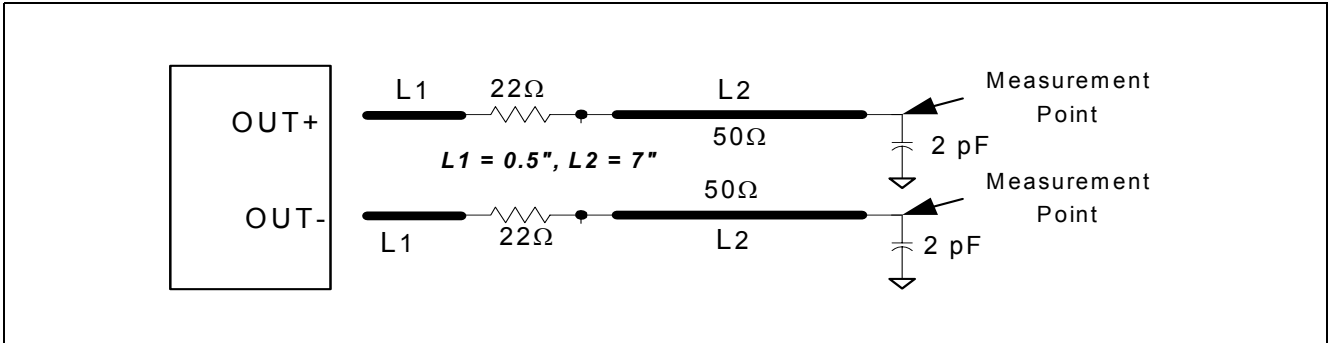


Figure 16. Differential Load Configuration for 3.3 Push Pull Clock

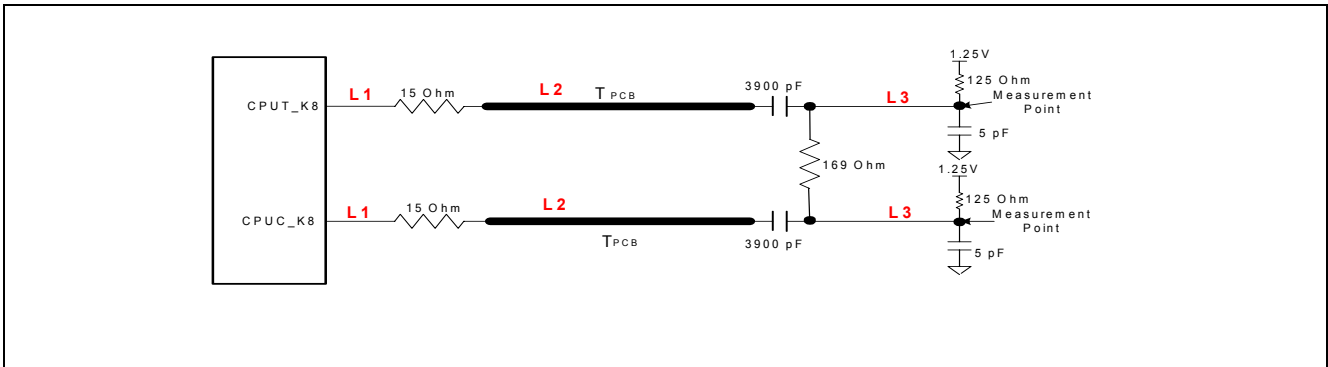


Figure 17. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

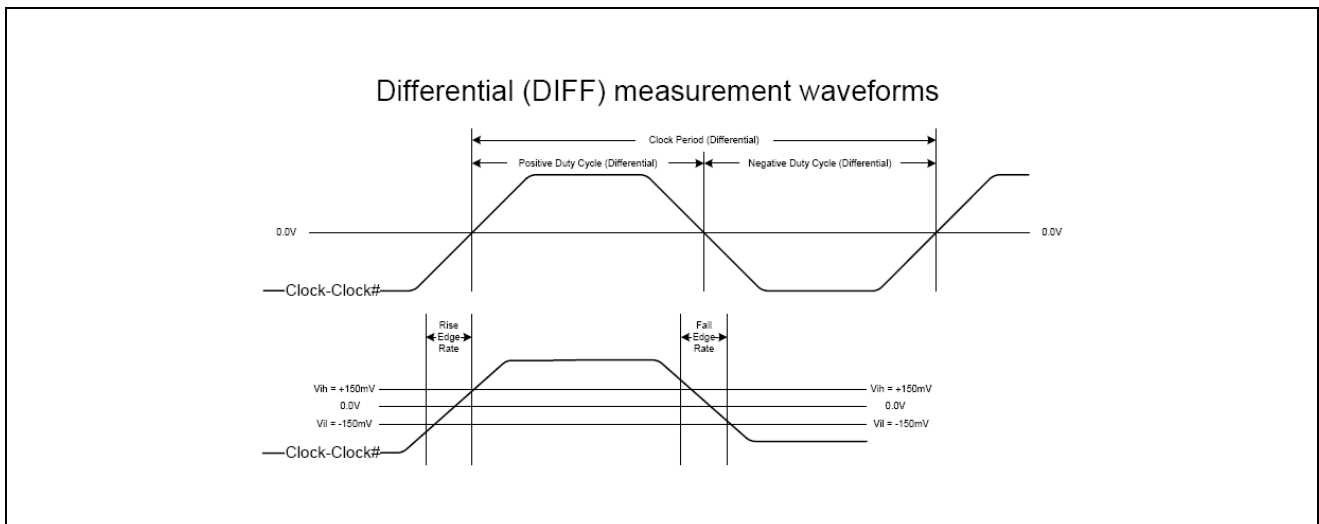


Figure 18. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

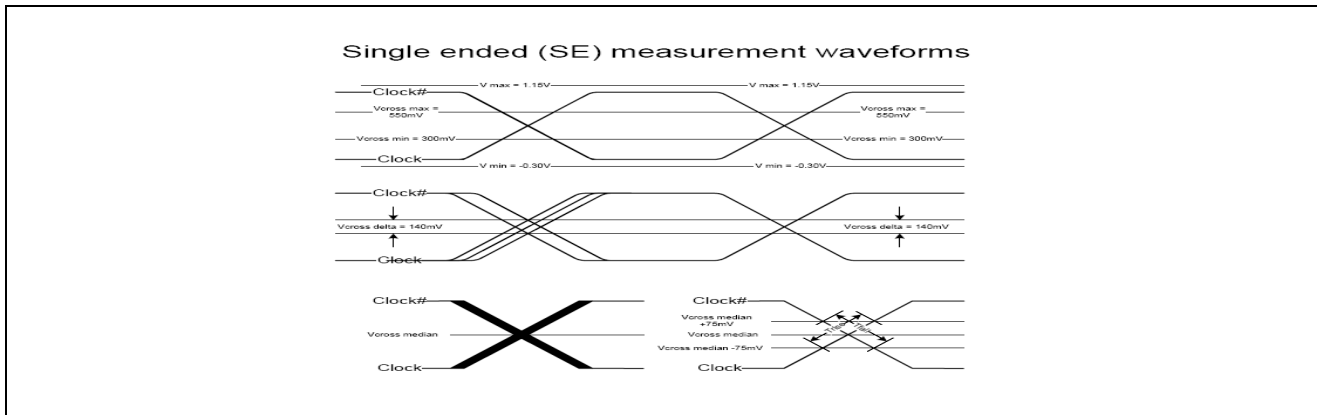
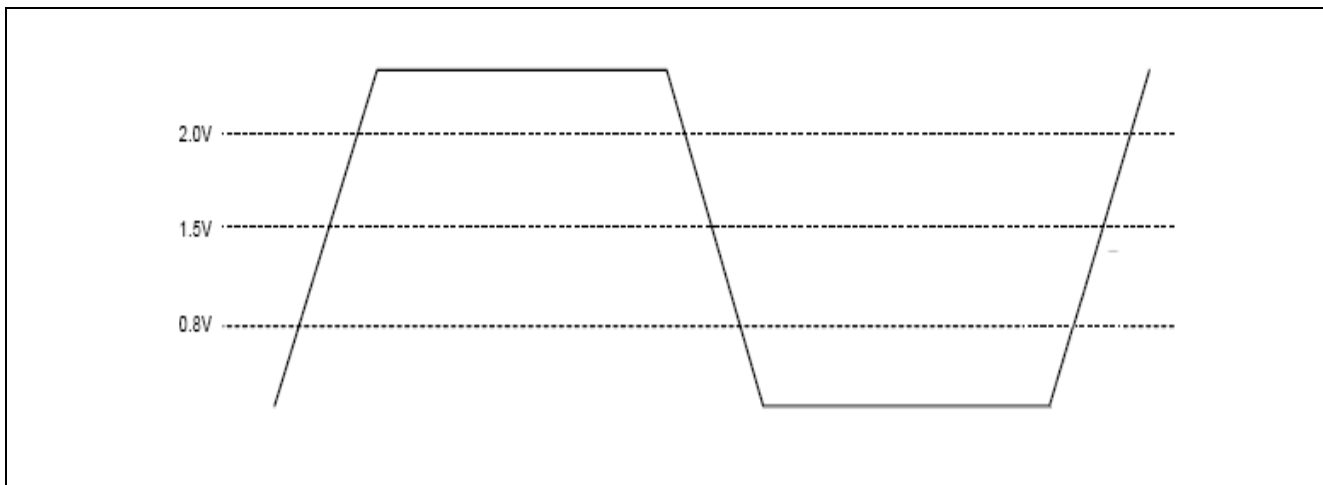


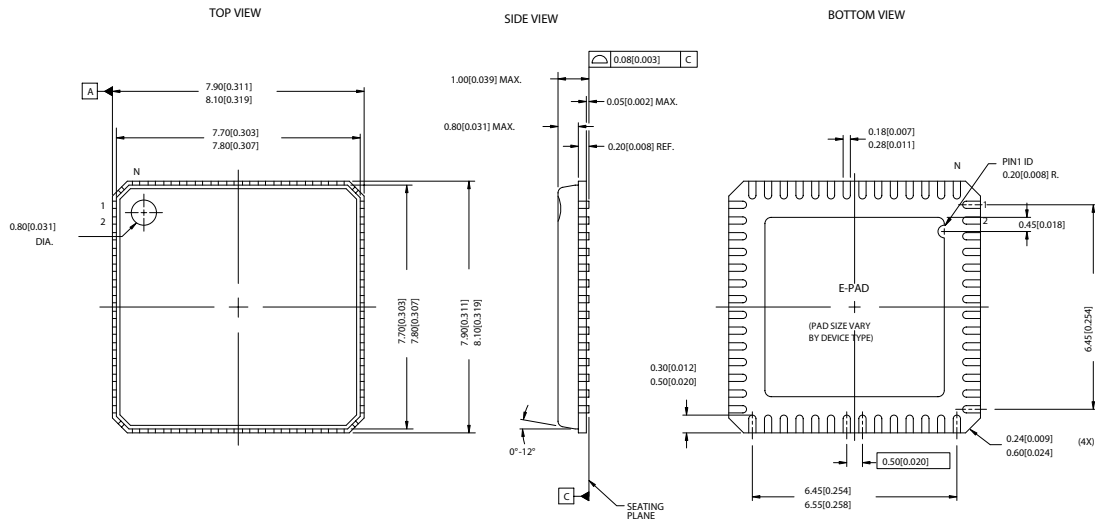
Figure 19. Single-ended Output Signals (for AC Parameters Measurement)



### Ordering Information

Part Number	Package Type	Product Flow
<b>Lead-free</b>		
CY28551LFXC-3	56-pin QFN	Commercial, 0° to 85°C
CY28551LFXC-3T	56-pin QFN – Tape and Reel	Commercial, 0° to 85°C

**Package Diagram**  
**Figure 20. 56-Lead QFN 8 x 8 MM LF56A**



51-85144-\*D

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**Document History Page**

Document Title: CY28551-3 Universal Clock Generator for Intel, VIA and SIS <sup>®</sup>				
Document Number: 001-05677				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	409135	See ECN	HGS	New Data Sheet
*A	417501	See ECN	HGS	1. Register alignment changed -BYTE 9 contains DF3_N8,DF2_N8,DF1_N8 -BYTE 10 contains DF1_N<7:0> -BYTE 11 contains DF2_N<7:0> -BYTE 12 contains DF3_N<7:0> 2. Add POWERGOOD status bit at BYTE6 [0] 3. Add CPU_STP#, PCI_STP# and CLKREQ# description
*B	460525	See ECN	RGL	Minor Change: To post on web
*C	491623	See ECN	HGS	1. Change 48M/24_48M driving strength to high by default. 2. Change Revision ID (BYTE7[7:4]) to 0010.
*D	492449	See ECN	FRA	Minor Change: Corrected revision on spec footer & history page.