CY2265

Pentium®, Pentium Pro®, and Cyrix® 6x86 Compatible Frequency Timing Generator with SDRAM Support

Features

- **Complete clock solution to meet requirements of Pentium®, Pentium Pro®, or Cyrix® 6x86 motherboards with SDRAM support**
  - **— 12 CPU clocks up to 83.33 MHz (see Function Table)**
  - **— Six PCI clocks, synchronous or asynchronous mode, pin-selectable by Bus Select input**
  - **— One USB clock at 48 MHz, meets Intel® jitter, accuracy, as well as rise and fall time requirements**
  - **— One I/O clock at 24 MHz**
  - **— Two Ref. clocks at 14.318 MHz**
- **Innovative SmartLatch™ technology**
  - **— Latches Select inputs only when PLLs are locked, ensuring proper input levels are latched**
  - **— Power-up stabilization time = 2 ms on all CPU and PCI clocks, which meets Intel Pentium and Pentium Pro power-up requirements**
- **Low CPU and PCI clock jitter ≤ 200 ps cycle-to-cycle**
- **Low skew outputs**
  - **— ≤ 250 ps between CPU clocks**
  - **— ≤ 250 ps between PCI clocks**
  - **— 1 ns–4 ns skew between CPU and PCI clocks (in synchronous mode) for compatibility with Intel 82430VX and SiS 55XX chipsets (CY2265-1)**
  - **— ≤ 500 ps skew between CPU and PCI clocks (in synchronous mode) for compatibility with ALI Aladdin III and other chipsets (CY2265-2)**
- **Improved output drivers are designed for low EMI**
- **Test mode support**
- **3.3V operation, 5V tolerant inputs**
- **Space saving and low cost 34-pin SSOP package**

Functional Description

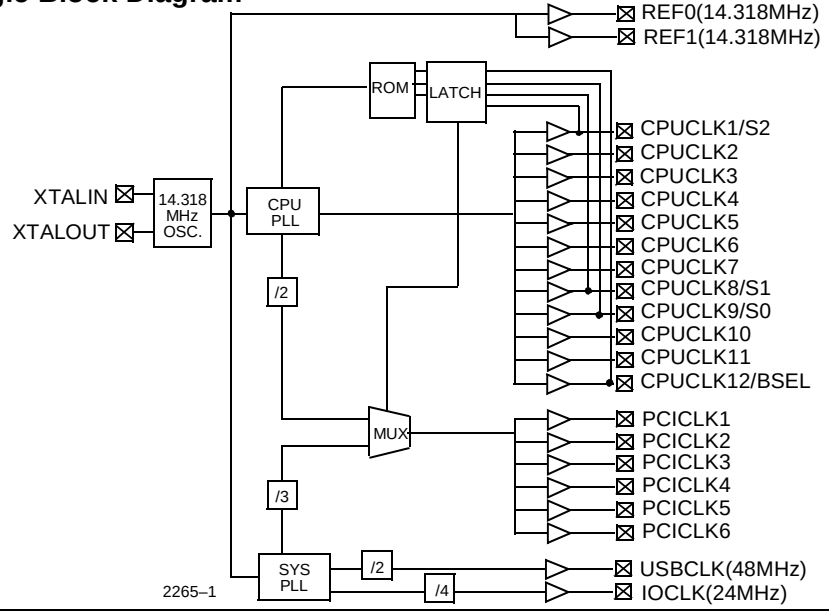
The CY2265 is a Frequency Timing Generator chip for Pentium, Pentium Pro, or Cyrix 6x86-based motherboards using Synchronous DRAM (SDRAM).

The CY2265 features four dual purpose I/O pins which provide extra CPU clocks, and enable the part to be packaged in a low-cost 34-pin SSOP package. These four pins feature innovative SmartLatch technology, which latches the select inputs only when all PLLs are locked, ensuring proper operation. Additionally, the device meets the Pentium and Pentium Pro power-up stabilization specifications, which require that CPU and PCI clocks be stable within 2 ms after power-up.

The CY2265 clock outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY2265 to have lower EMI than clock devices from other manufacturers. Please refer to the application note “Layout and Termination Techniques for Cypress Clock Generators” for more information on recommended system layout techniques.

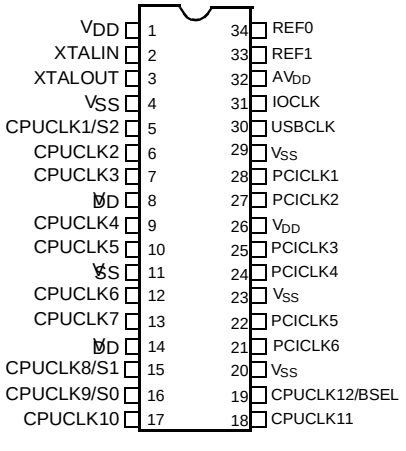
The CY2265 accepts a 14.318 MHz reference crystal or clock as its input and runs off a 3.3V supply. It is available in a 34-pin SSOP package, and is upwardly compatible with the CY2264.

Logic Block Diagram



Pin Configuration

Top View
SSOP



2265–2

Pin Summary

Name	Pin	Description
V_{DD}	1	Voltage supply
XTALIN[1, 2]	2	Reference crystal input
XTALOUT[1]	3	Reference crystal feedback
V_{SS}	4	Ground
CPUCLK1 / S2	5	CPU clock output CPU clock select input, bit 2
CPUCLK2	6	CPU clock output
CPUCLK3	7	CPU clock output
V_{DD}	8	Voltage supply
CPUCLK4	9	CPU clock output
CPUCLK5	10	CPU clock output
V_{SS}	11	Ground
CPUCLK6	12	CPU clock output
CPUCLK7	13	CPU clock output
V_{DD}	14	Voltage supply
CPUCLK8 / S1	15	CPU clock output CPU clock select input, bit 1
CPUCLK9 / S0	16	CPU clock output CPU clock select input, bit 0
CPUCLK10	17	CPU clock output
CPUCLK11	18	CPU clock output
CPUCLK12 / BSEL	19	CPU clock output Bus Select Input, selects asynchronous or synchronous PCI clocks. See Function Table.
V_{SS}	20	Ground
PCICLK1	21	PCI clock output
PCICLK2	22	PCI clock output
V_{SS}	23	Ground
PCICLK3	24	PCI clock output
PCICLK4	25	PCI clock output
V_{DD}	26	Voltage supply
PCICLK5	27	PCI clock output
PCICLK6	28	PCI clock output
V_{SS}	29	Ground
USBCLK	30	USB clock output, 48 MHz
IOCLK	31	I/O clock output, 24 MHz
AV_{DD}	32	Analog voltage supply
REF1	33	Reference clock output (14.318 MHz)
REF0	34	Reference clock output (14.318 MHz) for ISA slots (drives C_{LOAD} = 45 pF)

Notes:

1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 12 pF.
2. TCLK is a test clock on the XTALIN input during test mode.

Function Table (-1 and -2)

S2	S1	S0	XTALIN	CPUCLK[1-12]	PCICLK[1-6] BSEL = 1	PCICLK[1:6] BSEL = 0	REF[0-1]	USBCLK	IOCLK
0	0	0	14.318 MHz	33.33 MHz	16.67 MHz	32 MHz	14.318 MHz	48 MHz	24 MHz
0	0	1	14.318 MHz	75.0 MHz	37.5 MHz	32 MHz	14.318 MHz	48 MHz	24 MHz
0	1	0	14.318 MHz	55.0 MHz	27.5 MHz	32 MHz	14.318 MHz	48 MHz	24 MHz
0	1	1	14.318 MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0	0	14.318 MHz	50.0 MHz	25.0 MHz	32 MHz	14.318 MHz	48 MHz	24 MHz
1	0	1	14.318 MHz	66.67 MHz	33.33 MHz	32 MHz	14.318 MHz	48 MHz	24 MHz
1	1	0	14.318 MHz	60.0 MHz	30.0 MHz	32 MHz	14.318 MHz	48 MHz	24 MHz
1	1	1	TCLK[3]	TCLK/2[4]	TCLK/4	TCLK/3	TCLK	TCLK/2	TCLK/4

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	33.33	33.28	–1597
CPUCLK	75.0	75.0	0
CPUCLK	55.0	54.98	–331
CPUCLK	50.0	49.93	–1399
CPUCLK	66.67	66.56	–1597
CPUCLK	60.0	60.0	0
PCICLK[5]	32.0	32.005	167
USBCLK[6]	48.0	48.008	167
IOCLK	24.0	24.004	167

Notes:
3. TCLK is supplied on XTALIN pin.
4. Bidirectional CPUCLK I/O pins are High-Z in Test mode
5. If BSEL = 1, the PPM on PCICLK will be the same as on CPUCLK.
6. Meets Intel USB clock requirements.

CPU and PCI Clock Driver Strengths

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage..... –0.5 to +7.0V

Input Voltage.....–0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation 1W

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[7]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.6	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK PCICLK USBCLK IOCLK REF0 REF1		 30 30 20 20 45 15	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics V_{DD} = 3.135V to 3.6V, T_A = 0°C to +70°C

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}	High-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OH} = 12 mA	CPUCLK	2.4		V
			I_{OH} = 12 mA	PCICLK			
			I_{OH} = 8 mA	USBCLK			
			I_{OH} = 8 mA	IOCLK			
			I_{OH} = 12 mA	REF0			
			I_{OH} = 8 mA	REF1			
V_{OL}	Low-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OL} = 12 mA	CPUCLK		0.4	V
			I_{OL} = 12 mA	PCICLK			
			I_{OL} = 8 mA	USBCLK			
			I_{OL} = 8 mA	IOCLK			
			I_{OL} = 12 mA	REF0			
			I_{OL} = 8 mA	REF1			
I_{IH}	Input High Current	V_{IH} = V_{DD}				5	µA
I_{IL}	Input Low Current	V_{IL} = 0V				5	µA
I_{OZ}	Output Leakage Current	Three-state			–10	+10	µA
I_{DD}	Power Supply Current	V_{DD} = 3.6V, V_{IN} = 0 or V_{DD}, Loaded Outputs				175	mA
I_{DD}	Power Supply Current	V_{DD} = 3.6V, V_{IN} = 0 or V_{DD}, Unloaded Outputs				95	mA

Note:

7. Electrical parameters are guaranteed with these operating conditions.

Switching Characteristics[8]

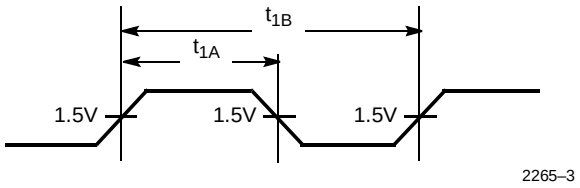
Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle[9]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t_{1C}	CPUCLK	CPU Clock HIGH Time	Measured at 2.4V, 66.67 MHz	5.0			ns
t_{1C}	PCICLK	PCI Clock HIGH Time[10]	Measured at 2.4V, 33.33 MHz	12.0			ns
t_{1D}	CPUCLK	CPU Clock LOW Time	Measured at 0.4V, 66.67 MHz	5.0			ns
t_{1D}	PCICLK	PCI Clock LOW Time[10]	Measured at 0.4V, 33.33 MHz	12.0			ns
t_2	CPUCLK	CPU Clock Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0		4.0	V/ns
t_2	PCICLK	PCI Clock Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0		4.0	V/ns
t_2	REF0, REF1	Reference Clock Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	0.5			V/ns
t_3	CPUCLK	CPU Clock Rise Time	Measured between 0.8V and 2.0V	0.3		1.2	ns
t_3	USBCLK, IOCLK	USB Clock and I/O Clock Rise Time	Measured between 0.8V and 2.0V			1.2	ns
t_4	CPUCLK	CPU Clock Fall Time	Measured between 2.0V and 0.8V	0.3		1.2	ns
t_4	USBCLK, IOCLK	USB Clock and I/O Clock Fall Time	Measured between 2.0V and 0.8V			1.2	ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.5V		100	250	ps
t_6	PCICLK	PCI-PCI Clock Skew	Measured at 1.5V		100	250	ps
t_7	CPUCLK, PCICLK	CPU-PCI Clock Skew (-1)	Measured at 1.5V[11]	1	2.5	4	ns
t_7	CPUCLK, PCICLK	CPU-PCI Clock Skew (-2)	Measured at 1.5V[11]	100	500	900	ps
t_8	CPUCLK	Cycle-Cycle Clock Jitter	CPU Clock jitter			200	ps
t_8	USBCLK, IOCLK, PCICLK	Cycle-Cycle Clock Jitter	USB Clock, I/O Clock, and PCI Clock jitter			500	ps
t_9	CPUCLK	Power-up Time	CPU clock stabilization from power-up			2	ms
t_{10}	PCICLK	Power-up Time	PCI clock stabilization from power-up			2	ms
t_{11}	CPUCLK	Frequency Slew Rate	Rate of change of frequency	0.1	2	10	MHz/ ms

Notes:

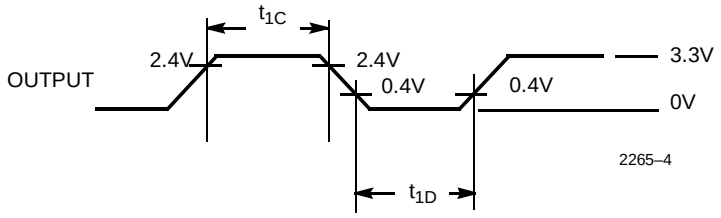
8. All parameters specified with loaded outputs.
9. Duty cycle is measured at 1.5V.
10. A LOW and HIGH time of 12 ns corresponds to a PCICLK frequency of 33.33 MHz. For PCICLK frequencies of 30 MHz and 25 MHz, the LOW and HIGH times are each respectively 13.33 ns and 16 ns.
11. Synchronous PCI mode only.

Switching Waveforms

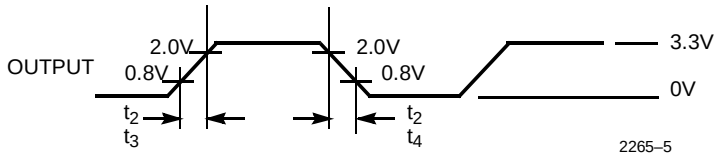
Duty Cycle Timing



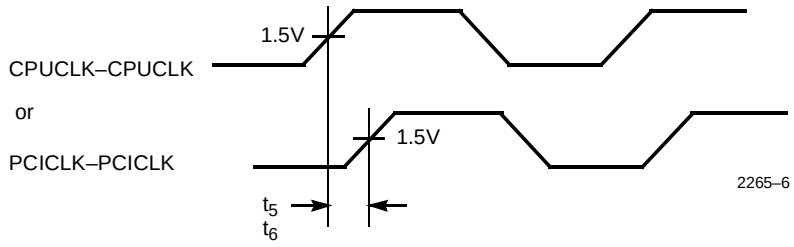
CPUCLK/PCICLK HIGH/LOW Times



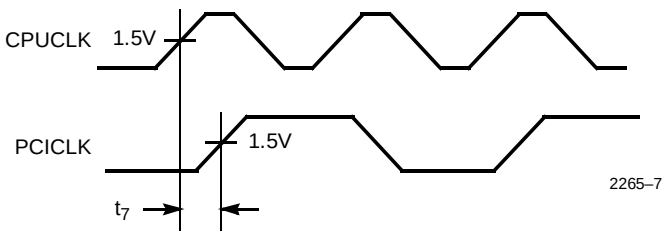
All Outputs Rise/Fall Time



Clock Skew



CPU-PCI Clock Skew



Application Information

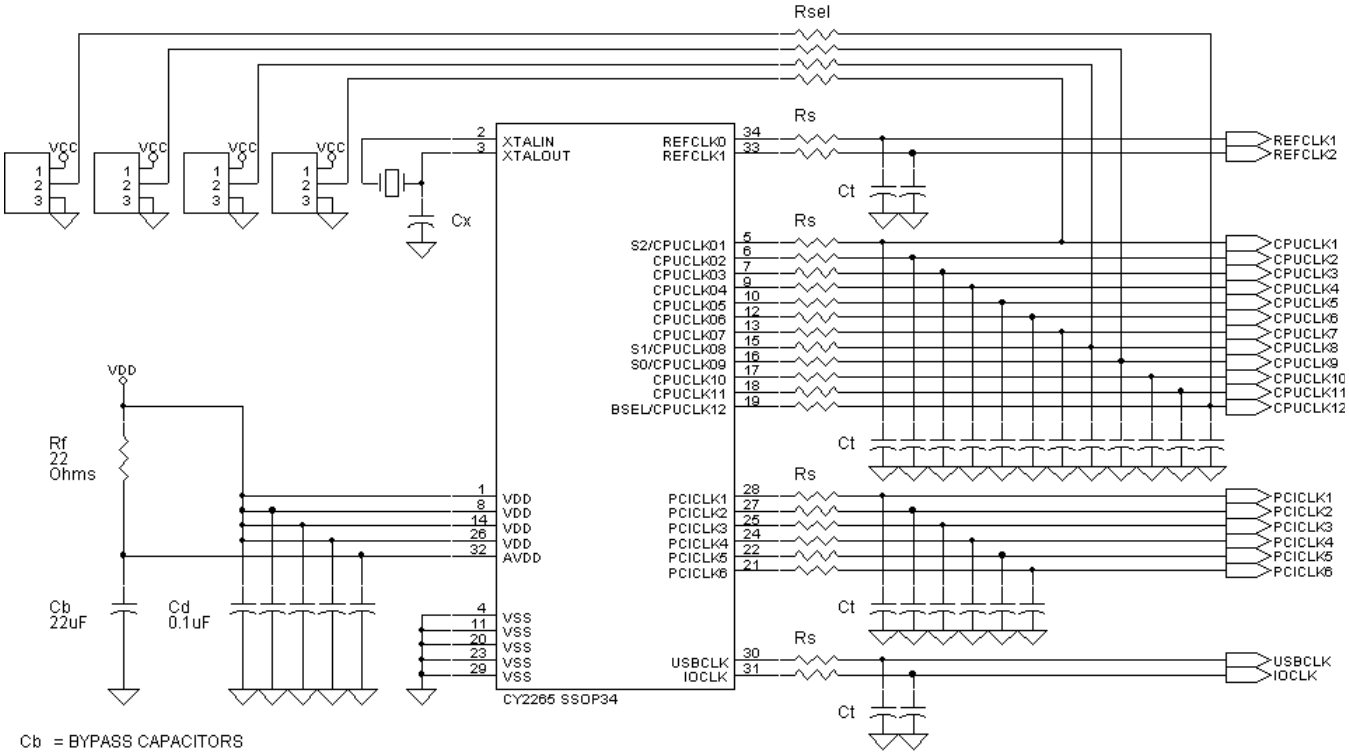
The CY2265 features SmartLatch technology which latches the select inputs only when both PLLs are locked. This eliminates spurious latching caused by noise on the power supply pins during ramp-up.

To use the SmartLatch feature, the four select inputs (S2, S1, S0, and BSEL) must be tied to either V_{CC} or V_{SS} through 10KΩ resistors. This will enable the user to select the appropriate CPUCLK and PCICLK frequencies from the Function Table.

Clock traces must be terminated with either series or parallel termination, as they are normally done.

The Application Circuit is shown below.

Application Circuit



Cb = BYPASS CAPACITORS

Cd = DECOUPLING CAPACITORS

Ct = OPTIONAL EMI-REDUCING CAPACITORS

Cx = OPTIONAL LOAD MATCHING CAPACITOR

Rf = FILTERING RESISTOR

Rs = SERIES TERMINATING RESISTORS

Rsel = STRAPPING RESISTERS (INSTALLED TO PULL EITHER UP OR DOWN)
TYPICAL VALUE = 10K OHMS

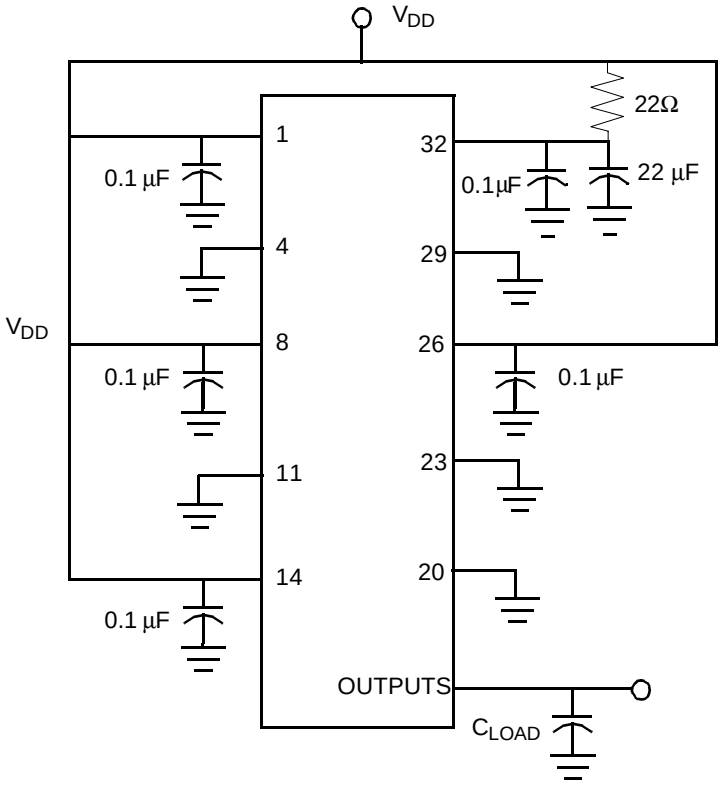
Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and C_{LOAD} of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different C_{LOAD} is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the clock generator (specified in the data sheet), and R_{series} is the series terminating resistor.

  $$R_{series} \geq R_{trace} - R_{out}$$

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note “Layout and Termination Techniques for Cypress Clock Generators” for more details.
- If a Ferrite Bead is used, a 10 µF– 22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2265PVC–1	O34	34-Pin SSOP	Commercial
CY2265PVC–2	O34	34-Pin SSOP	Commercial

Document #: 38–00527–A

Package Diagram

34-Pin Shrunk Small Outline Package