



PRELIMINARY

CY2264

Pentium™, Pentium Pro™, and Cyrix 6x86 Compatible Clock Synthesizer/Driver

Features

- Complete clock solution to meet requirements of Pentium™, Pentium Pro™, or Cyrix 6x86 motherboards including dual-processor and SDRAM designs
 - Eight CPU clock outputs, up to 75 MHz (see Function Table)
 - Six PCI clock outputs, synchronous or asynchronous mode, pin-selectable by Bus Select input
 - One USB clock at 48 MHz, meets Intel's accuracy, jitter, as well as rise and fall time requirements
 - One I/O clock at 24 MHz
 - Two Ref. clocks at 14.318 MHz
- Three dedicated, independent Frequency Select inputs (internal pull-up) ease system design, enable in-system frequency changes, and support OE control and Test Mode
- Low CPU clock jitter ≤ 200 ps cycle-to-cycle
- Low skew outputs
 - ≤ 250 ps between CPU clocks
 - ≤ 250 ps between PCI clocks
 - 1ns–4ns skew between CPU and PCI clocks (in synchronous mode) for compatibility with SIS 55XX and Intel 82430HX and 82430VX chipsets (CY2264–1)
 - 500 ps typ. skew between CPU and PCI clocks (in synchronous mode) for compatibility with ALI Aladdin III and other chipsets (CY2264–2)
- Improved output drivers are designed for low EMI
- Meets Pentium and Pentium Pro power-up stabilization requirements

- Smooth slewing in-system frequency changes (2 MHz/ms typical)
- Doze Mode support, CPUCLK = 33.33 MHz
- 3.3V operation, 5V tolerant inputs
- Available in space-saving 34-pin SSOP package

Functional Description

The CY2264 is a low-cost Clock Synthesizer/Driver chip for a Pentium, Pentium Pro, or Cyrix 6x86-based motherboard.

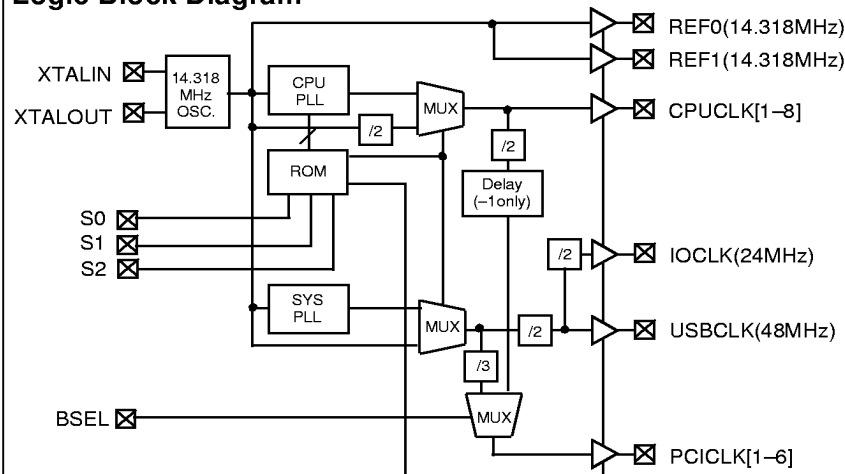
The CPU clocks of the CY2264 have less than 200 ps cycle-to-cycle jitter. Both the CPU and PCI clocks have a slew rate of greater than 1V/ns. The USB clock meets Intel's accuracy, jitter, and rise and fall time requirements.

All CPU clocks have a unique dual-speed frequency change logic to support fast clock stabilization on power-up (< 2 ms) and slow frequency changes during operation (2 MHz/ms typical). Three dedicated Frequency Select inputs facilitate the latter, and support OE, Test Mode, and Doze Mode functionality.

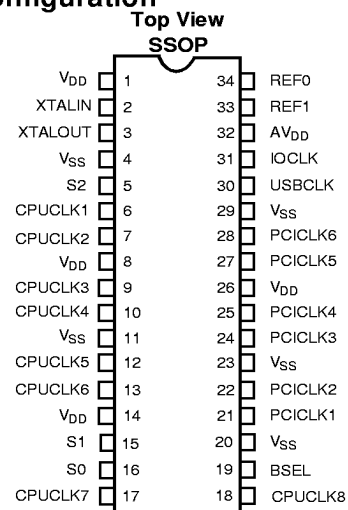
The CY2264 clock outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY2264 to have lower EMI than clock devices from other manufacturers. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more information on recommended system layout techniques.

The CY2264 accepts a 14.318 MHz reference crystal or clock as its input and runs off a 3.3V supply. The CY2264 is available in a space-saving, low-cost 34-pin SSOP package and is pin-compatible with the CY2265 for designs requiring additional SDRAM support.

Logic Block Diagram



Pin Configuration



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Pin Summary

Name	Pin	Description
V _{DD}	1	Voltage supply
XTALIN ^[1, 2]	2	Reference crystal input
XTALOUT ^[1]	3	Reference crystal feedback
V _{SS}	4	Ground
S2	5	CPU clock select input, bit 2 (internal pull-up resistor to V _{DD})
CPUCLK1	6	CPU clock output
CPUCLK2	7	CPU clock output
V _{DD}	8	Voltage supply
CPUCLK3	9	CPU clock output
CPUCLK4	10	CPU clock output
V _{SS}	11	Ground
CPUCLK5	12	CPU clock output
CPUCLK6	13	CPU clock output
V _{DD}	14	Voltage supply
S1	15	CPU clock select input, bit 1 (internal pull-up resistor to V _{DD})
S0	16	CPU clock select input, bit 0 (internal pull-up resistor to V _{DD})
CPUCLK7	17	CPU clock output
CPUCLK8	18	CPU clock output
BSEL	19	Bus Select Input, selects asynchronous or synchronous PCI clocks. See Function Table. (internal pull-up resistor to V _{DD})
V _{SS}	20	Ground
PCICLK1	21	PCI clock output
PCICLK2	22	PCI clock output
V _{SS}	23	Ground
PCICLK3	24	PCI clock output
PCICLK4	25	PCI clock output
V _{DD}	26	Voltage supply
PCICLK5	27	PCI clock output
PCICLK6	28	PCI clock output
V _{SS}	29	Ground
USBCLK	30	USB clock output, 48 MHz
IOCLK	31	I/O clock output, 24 MHz
AV _{DD}	32	Analog voltage supply
REF1	33	Reference clock output (14.318 MHz)
REF0	34	Reference clock output (14.318 MHz) for ISA slots (drives C _{LOAD} = 45 pF)

Notes:

1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 12 pF.
2. TCLK is a test clock on the XTALIN input during test mode.



Function Table

S2	S1	S0	XTALIN	CPUCLK[1-8]	PCICLK[1-6] BSEL = 1	PCICLK[1:6] BSEL = 0	REF[0-1]	USBCLK	IOCLK
0	0	0	14.318 MHz	33.33 MHz	16.67 MHz	32 MHz	14.318 MHz	48 MHz	24 MHz
0	0	1	14.318 MHz	75.0 MHz	37.5 MHz	32 MHz	14.318 MHz	48 MHz	24 MHz
0	1	0	14.318 MHz	55.0 MHz	27.5 MHz	32 MHz	14.318 MHz	48 MHz	24 MHz
0	1	1	14.318 MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0	0	14.318 MHz	50.0 MHz	25.0 MHz	32 MHz	14.318 MHz	48 MHz	24 MHz
1	0	1	14.318 MHz	66.67 MHz	33.33 MHz	32 MHz	14.318 MHz	48 MHz	24 MHz
1	1	0	14.318 MHz	60.0 MHz	30.0 MHz	32 MHz	14.318 MHz	48 MHz	24 MHz
1	1	1	TCLK ^[3]	TCLK/2	TCLK/4	TCLK/3	TCLK	TCLK/2	TCLK/4

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	33.33	33.28	-1597
CPUCLK	75.0	75.0	0
CPUCLK	55.0	54.98	-331
CPUCLK	50.0	49.93	-1399
CPUCLK	66.67	66.56	-1597
CPUCLK	60.0	60.0	0
PCICLK ^[4]	32.0	32.005	167
USBCLK ^[5]	48.0	48.008	167
IOCLK	24.0	24.004	167

Notes:

- 3. TCLK is supplied on XTALIN pin.
- 4. If BSEL = 1, the PPM on PCICLK will be the same as on CPUCLK.
- 5. Meets Intel USB clock requirements.

CPU and PCI Clock Driver Strengths

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage	-0.5 to +7.0V
Input Voltage	-0.5V to V _{DD} +0.5
Storage Temperature (Non-Condensing) ...	-65°C to +150°C
Max. Soldering Temperature (10 sec)	+260°C
Junction Temperature	+150°C
Package Power Dissipation	1W
Static Discharge Voltage	>2000V (per MIL-STD-883, Method 3015)



Operating Conditions^[6]

Parameter	Description	Min.	Max.	Unit
V _{DD}	Supply Voltage	3.135	3.6	V
T _A	Operating Temperature, Ambient	0	70	°C
C _L	Max. Capacitive Load on CPUCLK PCICLK USBCLK IOCLK REF0 REF1		30 30 20 20 45 15	pF
f _(REF)	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics V_{DD} = 3.135V to 3.6V, T_A = 0°C to +70°C

Parameter	Description	Test Conditions			Min.	Max.	Unit
V _{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V _{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V _{OH}	High-level Output Voltage	V _{DD} = V _{DD} Min.	I _{OH} = 12 mA	CPUCLK	2.4		V
			I _{OH} = 12 mA	PCICLK			
			I _{OH} = 8 mA	USBCLK			
			I _{OH} = 8 mA	IOCLK			
			I _{OH} = 12 mA	REF0			
			I _{OH} = 8 mA	REF1			
V _{OL}	Low-level Output Voltage	V _{DD} = V _{DD} Min.	I _{OL} = 12 mA	CPUCLK		0.4	V
			I _{OL} = 12 mA	PCICLK			
			I _{OL} = 8 mA	USBCLK			
			I _{OL} = 8 mA	IOCLK			
			I _{OL} = 12 mA	REF0			
			I _{OL} = 8 mA	REF1			
I _{IH}	Input High Current	V _{IH} = V _{DD}				5	μA
I _{IL}	Input Low Current	V _{IL} = 0V				100	μA
I _{OZ}	Output Leakage Current	Three-state			-10	+10	μA
I _{DD}	Power Supply Current	V _{DD} = 3.6V, V _{IN} = 0 or V _{DD} , Loaded Outputs, CPU clocks = 66.67 MHz				140	mA
I _{DD}	Power Supply Current	V _{DD} = 3.6V, V _{IN} = 0 or V _{DD} , Unloaded Outputs				90	mA

Note:

6. Electrical parameters are guaranteed with these operating conditions.

Switching Characteristics (CY2264-1) [7]

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t ₁	All	Output Duty Cycle ^[8]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t _{1C}	CPUCLK	CPU Clock HIGH Time	Measured at 2.4V, 66.67 MHz	5.0			ns
t _{1C}	PCICLK	PCI Clock HIGH Time ^[9]	Measured at 2.4V, 33.33 MHz	12.0			ns
t _{1D}	CPUCLK	CPU Clock LOW Time	Measured at 0.4V, 66.67 MHz	5.0			ns
t _{1D}	PCICLK	PCI Clock LOW Time ^[9]	Measured at 0.4V, 33.33 MHz	12.0			ns
t ₂	CPUCLK	CPU Clock Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0		4.0	V/ns
t ₂	PCICLK	PCI Clock Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0		4.0	V/ns
t ₂	REF0, REF1	Reference Clock Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	0.5			V/ns
t ₃	CPUCLK	CPU Clock Rise Time	Measured between 0.8V and 2.0V	0.3		1.2	ns
t ₃	USBCLK, IOCLK	USB Clock and I/O Clock Rise Time	Measured between 0.8V and 2.0V			1.2	ns
t ₄	CPUCLK	CPU Clock Fall Time	Measured between 2.0V and 0.8V	0.3		1.2	ns
t ₄	USBCLK, IOCLK	USB Clock and I/O Clock Fall Time	Measured between 2.0V and 0.8V			1.2	ns
t ₅	CPUCLK	CPU-CPU Clock Skew	Measured at 1.5V		100	250	ps
t ₆	PCICLK	PCI-PCI Clock Skew	Measured at 1.5V		100	250	ps
t ₇	CPUCLK, PCICLK	CPU-PCI Clock Skew ^[10] (CY2264-1)	Measured at 1.5V	1.0	2.5	4.0	ns
t ₈	CPUCLK	Cycle-Cycle Clock Jitter	CPU Clock jitter			200	ps
t ₈	USBCLK, IOCLK, PCICLK	Cycle-Cycle Clock Jitter	USB Clock, I/O Clock, and PCI Clock jitter			500	ps
t ₉	CPUCLK	Power-up Time	CPU clock stabilization from power-up			2	ms
t ₁₀	PCICLK	Power-up Time	PCI clock stabilization from power-up			2	ms
t ₁₁	CPUCLK	Frequency Slew Rate	Rate of change of frequency	0.1	2	10	MHz/ms

Notes:

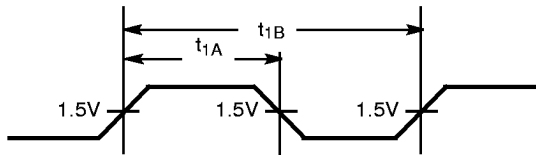
7. All parameters specified with loaded outputs.
8. Duty cycle is measured at 1.5V.
9. A LOW and HIGH time of 12 ns corresponds to a PCICLK frequency of 33.33 MHz. For PCICLK frequencies of 30 MHz and 25 MHz, the LOW and HIGH times are each respectively 13.33 ns and 16 ns.
10. Synchronous PCI Mode only.

Switching Characteristics (CY2264-2) [7]

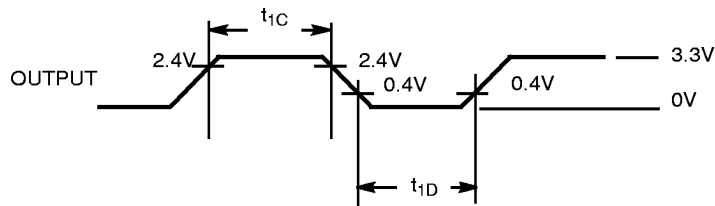
Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t ₁	All	Output Duty Cycle ^[8]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t _{1C}	CPUCLK	CPU Clock HIGH Time	Measured at 2.4V, 66.67 MHz	5.0			ns
t _{1C}	PCICLK	PCI Clock HIGH Time ^[9]	Measured at 2.4V, 33.33 MHz	12.0			ns
t _{1D}	CPUCLK	CPU Clock LOW Time	Measured at 0.4V, 66.67 MHz	5.0			ns
t _{1D}	PCICLK	PCI Clock LOW Time ^[9]	Measured at 0.4V, 33.33 MHz	12.0			ns
t ₂	CPUCLK	CPU Clock Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0		4.0	V/ns
t ₂	PCICLK	PCI Clock Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0		4.0	V/ns
t ₂	REF0, REF1	Reference Clock Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	0.5			V/ns
t ₃	CPUCLK	CPU Clock Rise Time	Measured between 0.8V and 2.0V	0.3		1.2	ns
t ₃	USBCLK, IOCLK	USB Clock and I/O Clock Rise Time	Measured between 0.8V and 2.0V			1.2	ns
t ₄	CPUCLK	CPU Clock Fall Time	Measured between 2.0V and 0.8V	0.3		1.2	ns
t ₄	USBCLK, IOCLK	USB Clock and I/O Clock Fall Time	Measured between 2.0V and 0.8V			1.2	ns
t ₅	CPU-CLK[1:6]	CPU-CPU Clock Skew	Measured at 1.5V		100	150	ps
t ₅	CPU-CLK[7:8]	CPU-CPU Clock Skew	Measured at 1.5V			100	ps
t ₅	CPUCLK	CPU[1:6] - CPU[7:8] Clock Skew	Measured at 1.5V	100	200	300	ps
t ₆	PCICLK	PCI-PCI Clock Skew	Measured at 1.5V		100	250	ps
t ₇	CPUCLK, PCICLK	CPU-PCI Clock Skew ^[10]	Measured at 1.5V	100	500	900	ps
t ₈	CPUCLK	Cycle-Cycle Clock Jitter	CPU Clock jitter			200	ps
t ₈	USBCLK, IOCLK, PCICLK	Cycle-Cycle Clock Jitter	USB Clock, I/O Clock, and PCI Clock jitter			500	ps
t ₉	CPUCLK	Power-up Time	CPU clock stabilization from power-up			2	ms
t ₁₀	PCICLK	Power-up Time	PCI clock stabilization from power-up			2	ms
t ₁₁	CPUCLK	Frequency Slew Rate	Rate of change of frequency	0.1	2	10	MHz/ ms

Switching Waveforms

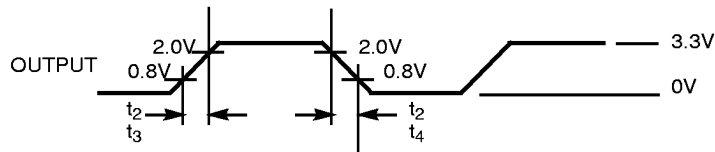
Duty Cycle Timing



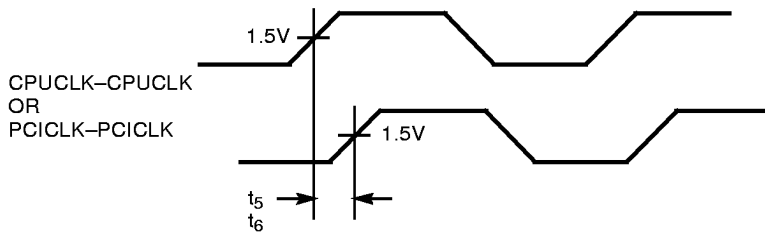
CPUCLK Outputs HIGH/LOW Time



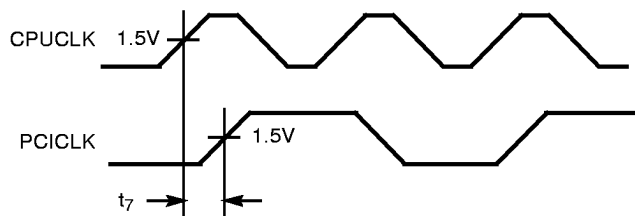
All Outputs Rise/Fall Time



Clock Skew



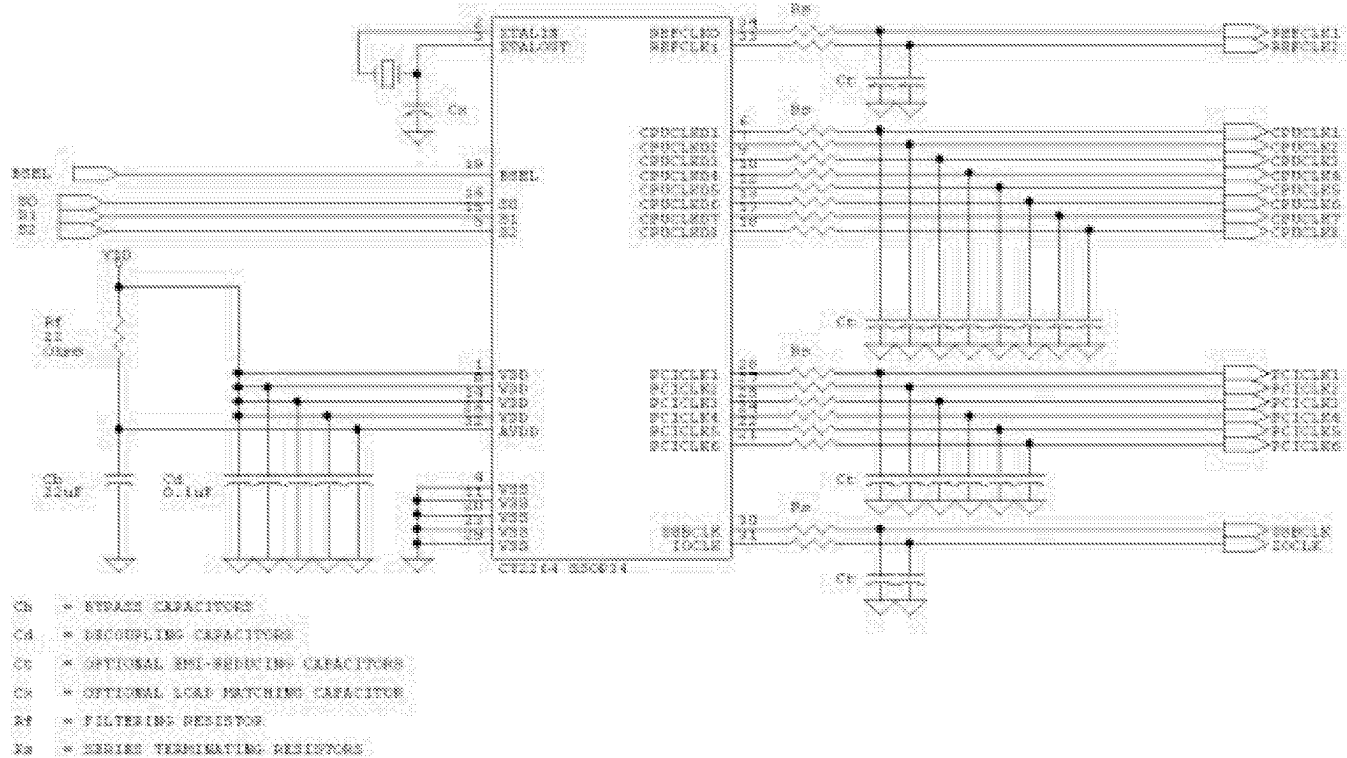
CPU-PCI Clock Skew



Application Information

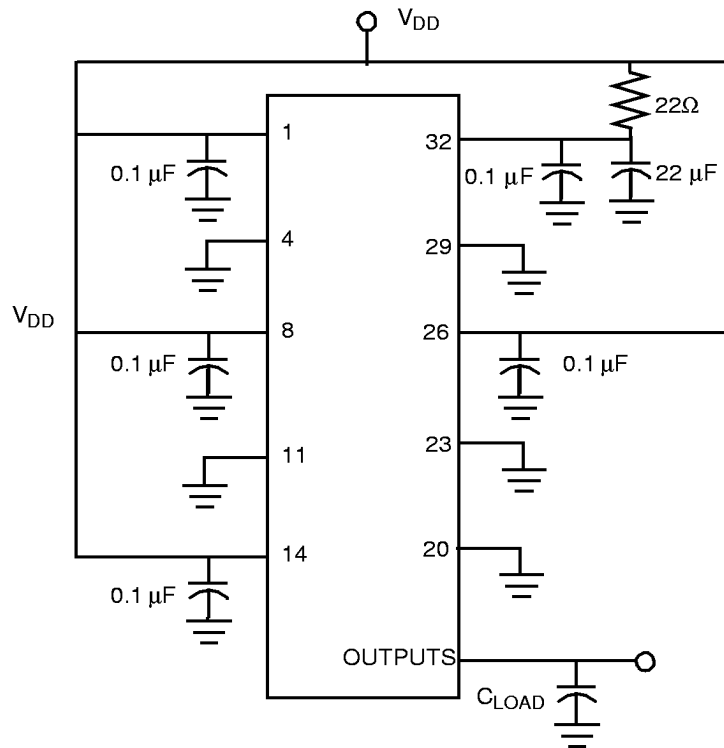
The Application Circuit is shown below.

Clock traces must be terminated with either series or parallel termination, as they are normally done.

Application Circuit

Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and C_{LOAD} of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different C_{LOAD} is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 μF . In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the clock generator (specified in the data sheet), and R_{series} is the series terminating resistor.

$$R_{series} \geq R_{trace} - R_{out}$$
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50 Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10 μF – 22 μF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit


Note: All capacitors should be placed as close to each pin as possible.

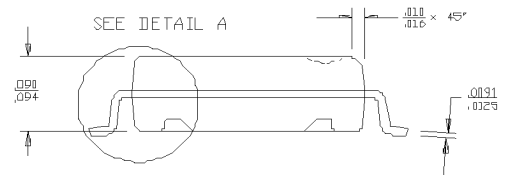
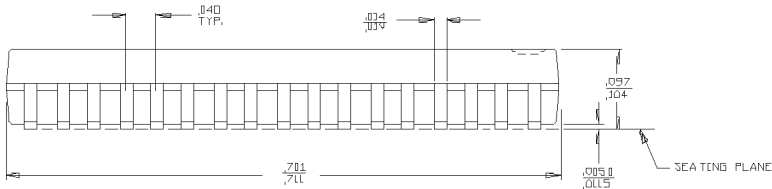
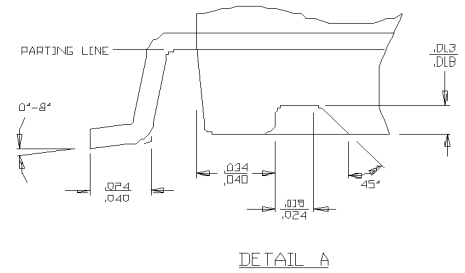
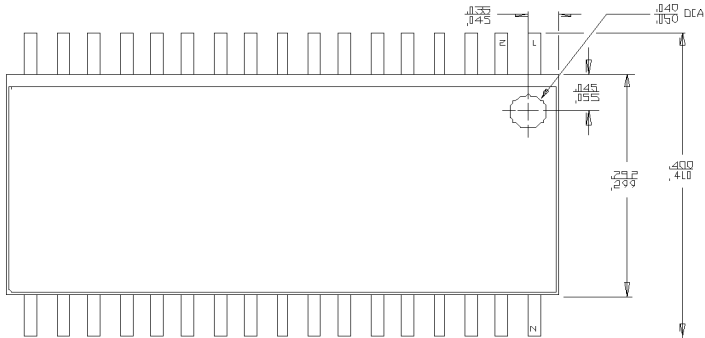
Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2264PVC-1	O34	34-Pin SSOP	Commercial
CY2264PVC-2	O34	34-Pin SSOP	Commercial

Document #: 38-00520-A

Package Diagram

34-Pin Shrunk Small Outline Package



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