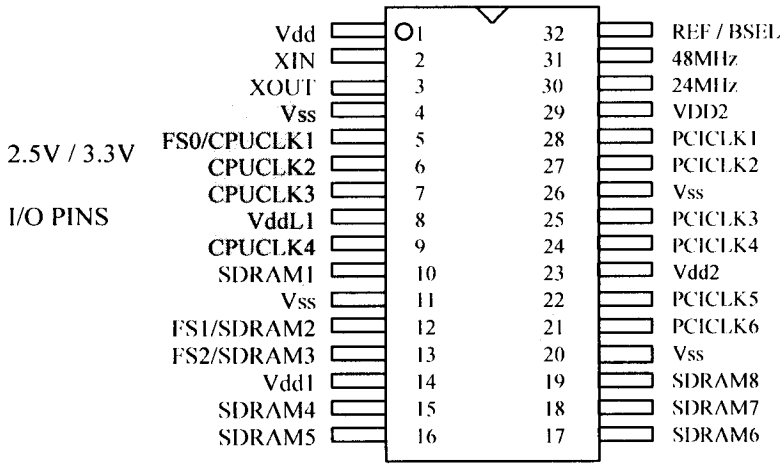
C-MEDIA ELECTRONICS INC.
Ver. A1.1
4F, No. 1, Sec. 1, Tun-Hwa S. RD., Taipei, Taiwan
TEL : (02)577-8140
FAX : 886-2-578-8138
E-Mail : cmedia@ms4.hinet.net

CMA8865-27 · Mixed Voltage clock Synthesizer with Buffer for PENTIUM™ & II CPU/PCI system

FEATURES

- Supports Pentium and Pentium II CPUs.
- 4 Copies of CPU clock, Usable as AGP clocks.
- 8 copies of SDRAM clocks.
- 6 PCI clock (Synchronous w/ CPU Clock/2 or 2/5 CPU clock)
- 1 REF. Clock @14.31818MHz
- 24MHz clock for FD, 48MHz clock for USB.
- <250ps skew between CPUCLK buffers.
- <500ps skew between PCICLK buffers.
- CPU leads PCI 1 to 4 ns.
- Optional common or mixed power supply mode.
  - ✧ Vdd = Vdd1, 2 = VddL1 = 3.3V
  - ✧ Vdd = Vdd1, 2 = 3.3V; VddL1 = 2.5V
- 60mA buffer switching current @3.3V
- Logic input latched at power-up for frequency selection, saving Input/Output Pins.
- 32 pins SOJ package.

PIN CONFIGURATIONS



SELECTED LOGIC INPUT LATCHED FOR POWER-ON CONDITION

Logic Latched	PIN# 32 BSEL	PIN# 13 SEL2	PIN# 12 SEL1	PIN# 5 SEL0
0	Asyn. PCICLK	LOW	LOW	LOW
1	Syn. PCICLK	HIGH	HIGH	HIGH

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PIN DESCRIPTION

NAME	TYPE	NO.	DESCRIPTION
Vdd	P	1	Analog power supply 3.3V
XIN	I	2	14.318MHz Clock Input.
XOUT	O	3	14.318MHz Clock Output.
Vss	G	4	Ground
FS0 CPUCLK1	bi-dir	5	Frequency Select pin 1 CPUCLK output 2.5V/3.3V outputs
CPUCLK2	O	6	CPUCLK outputs 2.5V/3.3V outputs.
CPUCLK3	O	7	CPUCLK outputs 2.5V/3.3V outputs.
VDDL1	P	8	2.5V/3.3V I/O Power Supply
CPUCLK4	O	9	CPUCLK outputs 2.5V/3.3V outputs.
SDRAM1	O	10	SDRAM output clock
Vss	G	11	Ground
FS1 SDRAM2	bi-dir	12	Frequency Select pin 1 SDRAM output clock
FS2 SDRAM3	bi-dir	13	Frequency Select pin 2 SDRAM output clock
Vdd1	P	14	3.3V I/O Power supply
SDRAM4	O	15	SDRAM output clock
SDRAM5	O	16	SDRAM output clock
SDRAM6	O	17	SDRAM output clock
SDRAM7	O	18	SDRAM output clock
SDRAM8	O	19	SDRAM output clock
Vss	G	20	Ground
PCICLK6	O	21	PCI output clock
PCICLK5	O	22	PCI output clock
Vdd2	P	23	3.3V I/O Power supply
PCICLK4	O	24	PCI output clock
PCICLK3	O	25	PCI output clock
Vss	G	26	Ground
PCICLK2	O	27	PCI output clock
PCICLK1	O	28	PCI output clock
Vdd2	P	29	3.3V I/O Power supply
24MHz	I	30	24MHz clock output 3.3V for FD.
48MHz	I	31	48MHz clock output 3.3V for USB.
REF BSEL	bi-dir	32	14,318MHz clock output. Select synchronous (1/2 CPU) or asynchronous (2/5 CPU) PCICLK

BUFFER SPECIFICATIONS

Buffer Name	Vcc Range(V)	Impedance (ohms)	Buffer Type
CPU	2.375 - 2.9	15 -45	1
48/24 MHz, REF	3.315 - 3.465	20 - 60	3
SDRAM	3.315 - 3.465	10 - 24	4
PCI	3.315 - 3.465	12 - 55	5

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Type 1 : CPU Clock Buffer Operating Characteristics

Symbol	Parameter	Condition	Min.	Max.	Units
Iohmin	Pull-up Current	Vout=1.0V	-27		mA
Iohmax	Pull-up Current	Vout=2.6V		-27	mA
Iolmin	Pull-down Current	Vout=1.2V	27		mA
Iolmax	Pull-down Current	Vout=0.3V		27	mA
trh	2.5V Type 1 Output Rise Edge Rate	2.5V @0.4V-2.0V 10pF Load	1/1	4/1	V/ns
tfh	2.5V Type 1 Output Fall Edge Rate	2.5V @2.0V-0.4V 20pF Load	1/1	4/1	V/ns

Type 3 : FD, USB, REF (3.3V) Clock Buffer Operating Characteristics

Symbol	Parameter	Condition	Min.	Max.	Units
Iohmin	Pull-up Current	Vout=1.0V	-29		mA
Iohmax	Pull-up Current	Vout=3.315V		-23	mA
Iolmin	Pull-down Current	Vout=1.95V	29		mA
Iolmax	Pull-down Current	Vout=0.4V		27	mA
trh	3.3V Type 3 Output Rise Edge Rate	3.3V @0.4V-2.4V 10pF Load	0.5	2.0	V/ns
tfh	3.3V Type 3 Output Fall Edge Rate	3.3V @2.4V-0.4V 20pF Load	0.5	2.0	V/ns

Type 4 : SDRAM (3.3V) Clock Buffer Operating Characteristics

Symbol	Parameter	Condition	Min.	Max.	Units
Iohmin	Pull-up Current	Vout=2.0V	-54		mA
Iohmax	Pull-up Current	Vout=3.315V		-46	mA
Iolmin	Pull-down Current	Vout=1.0V	54		mA
Iolmax	Pull-down Current	Vout=0.4V		53	mA
trh	3.3V Type 4 Output Rise Edge Rate	3.3V @0.4V-2.4V 20pF Load	1.5	4/1	V/ns
tfh	3.3V Type 4 Output Fall Edge Rate	3.3V @2.4V-0.4V 30pF Load	1.5	4/1	V/ns

Type 5 : PCI Clock Buffer Operating Characteristics

Symbol	Parameter	Condition	Min.	Max.	Units
Iohmin	Pull-up Current	Vout=1.0V	-33		mA
Iohmax	Pull-up Current	Vout=3.315V		-33	mA
Iolmin	Pull-down Current	Vout=1.95V	30		mA
Iolmax	Pull-down Current	Vout=0.4V		38	mA
trh	3.3V Type 5 Output Rise Edge Rate	3.3V @0.4V-2.4V 20pf Load	1/1	4/1	V/ns
tfh	3.3V Type 5 Output Fall Edge Rate	3.3V @2.4V-0.4V 30pf Load	1/1	4/1	V/ns

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CPU CLOCK FREQUENCY TABLE (in MHz)

SEL2	SEL1	SEL0	CPU, SDRAM	PCICLK BSEL=1	PCICLK BSEL=0	48MHz	24MHz
0	0	0	50.0	1/2	2/5	48	24
0	0	1	60.0	1/2	2/5	48	24
0	1	0	66.8	1/2	2/5	48	24
0	1	1	REF/2	REF/4	REF 2/5	REF/2	REF/4
1	0	0	55.0	1/2	2/5	48	24
1	0	1	75.0	1/2	2/5	48	24
1	1	0	83.3	1/2	2/5	48	24
1	1	1	Tristate	Tristate	Tristate	Tristate	Tristate

AC / DC SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Power Supply Voltage	Vdd = Vdd1, 2 =3.3V±5% VddL1= 3.3V±5% VddL1=2.5V+16%,-5%
Applied Input Voltage (VSS)	-0.3V
Ambient Temperature	55 to 125°C
Storage Temperature	-65 to 150°C
Maximum Power Supply	7V

NOTICE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITION
Idd	Dynamic Supply Current	-	TBD	mA	CPU=66.6MHz,PCI=33.3MHz
Vil	Input Low Voltage	Vss-0.3	0.8	VDC	
Vih	Input High Voltage	2.0	Vdd-0.3	VDC	Vdd=3.3V+/-5%
Iil	Input Leakage Current	-5	+5	uA	0<Vin<VddL1
Voh2	2.5V Output High Voltage	2.0	-	V	VddL1=2.375V to 2.9V,Ioh=-1mA
Vol2	2.5V Output Low Voltage	-	0.4	V	VddL1=2.375V to 2.9V, Iol=1mA
Voh3	3.3V Output High Voltage	2.4	-	V	Vdd1=3.3V+/-5%, Ioh=-1mA
Vol3	3.3V Output Low Voltage	-	0.4	V	Vdd1=3.3V+/-5%, Iol=1mA
Vpoh	PCI bus Output High Voltage	2.4	-	V	Vdd2=3.3V+/-5%, Ioh=-1mA
Vpol	PCI bus Output Low Voltage	-	0.55	V	Vdd2=3.3V+/-5%, Ioh=-1mA
Ioz	Tri-state leakage Current	-	10	uA	
Isc	Short Circuit Current	25	-	mA	1 output at a time -30 seconds

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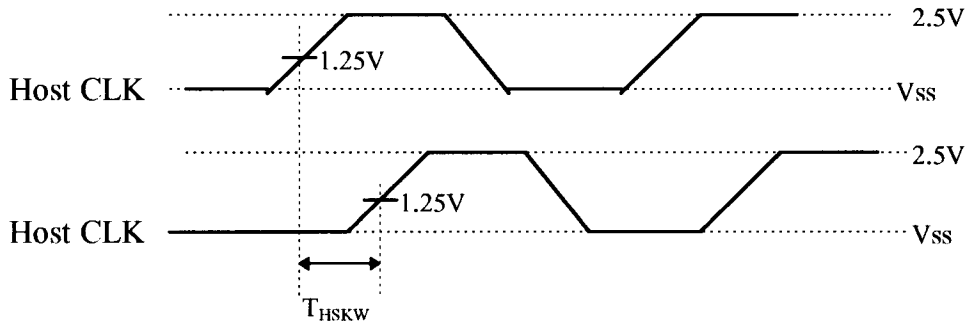
AC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITION
T_{Hrise}, T_{Hfall}	Host Clock Rise and Fall time	0.4	-	1.6	ns	20pf load/CPU and PCI outputs
T_{HCP}	Host Clock Period	15/16.7	-	-	ns	Measured at 1.25V, 66/60MHz
T_{HCH}	Host Clock High time	5.2/6.0	-	-	ns	Measured at 2.0V, 66/60MHz
T_{HCL}	Host Clock Low time	5.0/5.8	-	-	ns	Measured at 0.4V, 66/60MHz
Duty Cycle	Duty cycle	45	50	55	%	Measured at 1.25V
T_{HSKW}	Buffer out Skew All Host CLK	-	-	250	ps	Refer to Notes below
T_{JAB}	Jitter Absolute, Host clock	-	-	500	ps	
T_{STB}	Host/PCI clock stabilization from power-up	-	-	3	ms	Vdd=3.3V
Toff	Host to PCI Offset	1	-	4	ns	Refer to Notes below
T_{HSSKW}	Host to SDRAM Skew	-	-	500	ps	Refer to Notes below
T_{PCP}	PCI Clock Period	30/33.3	-	-	ns	Measured at 1.5V, 66/60MHz
T_{PCH}	PCI Clock High time	12/13.3	-	-	ns	Measured at 2.4V, 66/60MHz
T_{PCL}	PCI Clock Low time	12/13.3	-	-	ns	Measured at 0.4V, 66/60MHz
T_{PSKW}	Buffer out Skew All PCI CLK	-	-	500	ps	Refer to Notes below
Iol	Switching Current Low	TBD	60	TBD	mA	Vol=1.5V
Ioh	Switching Current High	TBD	60	TBD	mA	Voh=1.5V

Notes : Clock period, jitter, offset and skew are measured on the rising edge CLKs at 1.25V for the 2.5V clocks and at 1.5V for the 3.3V clocks.

HOST CLK TO HOST CLK SKEW



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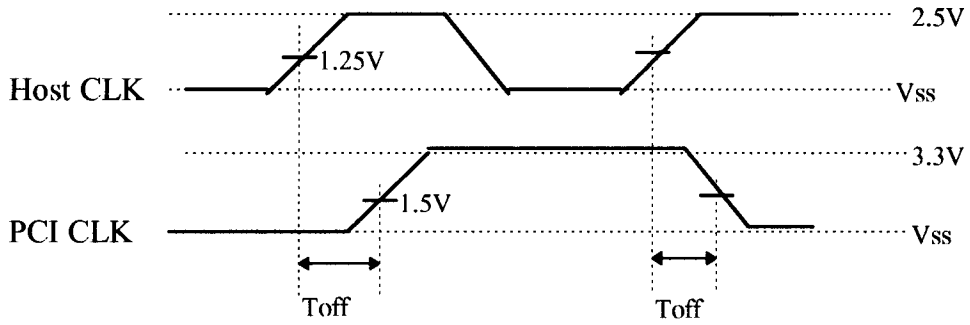
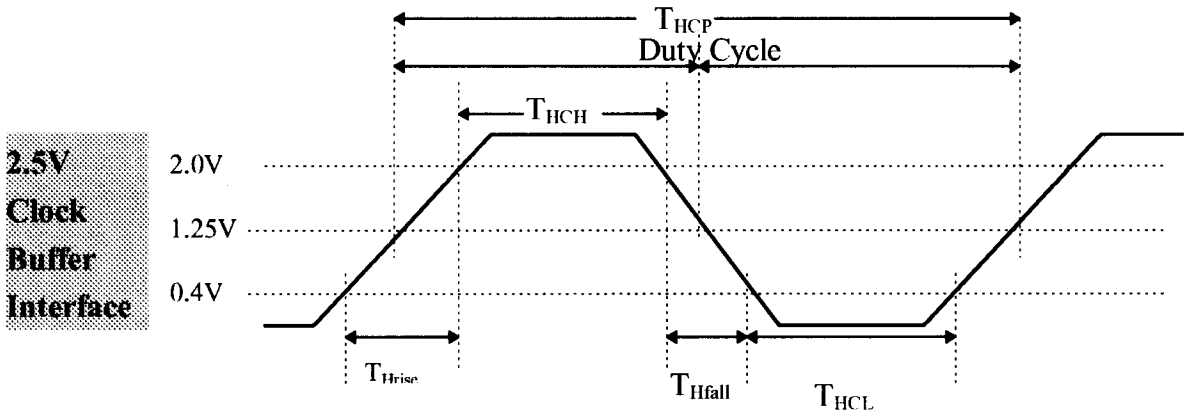
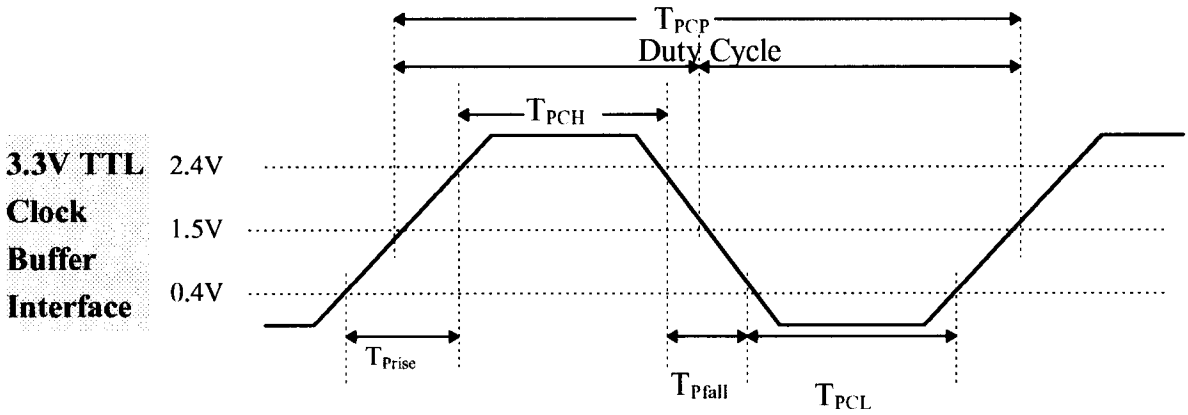
HOST CLK TO PCI CLK OFFSET



CLOCK OUTPUT WAVE FORM





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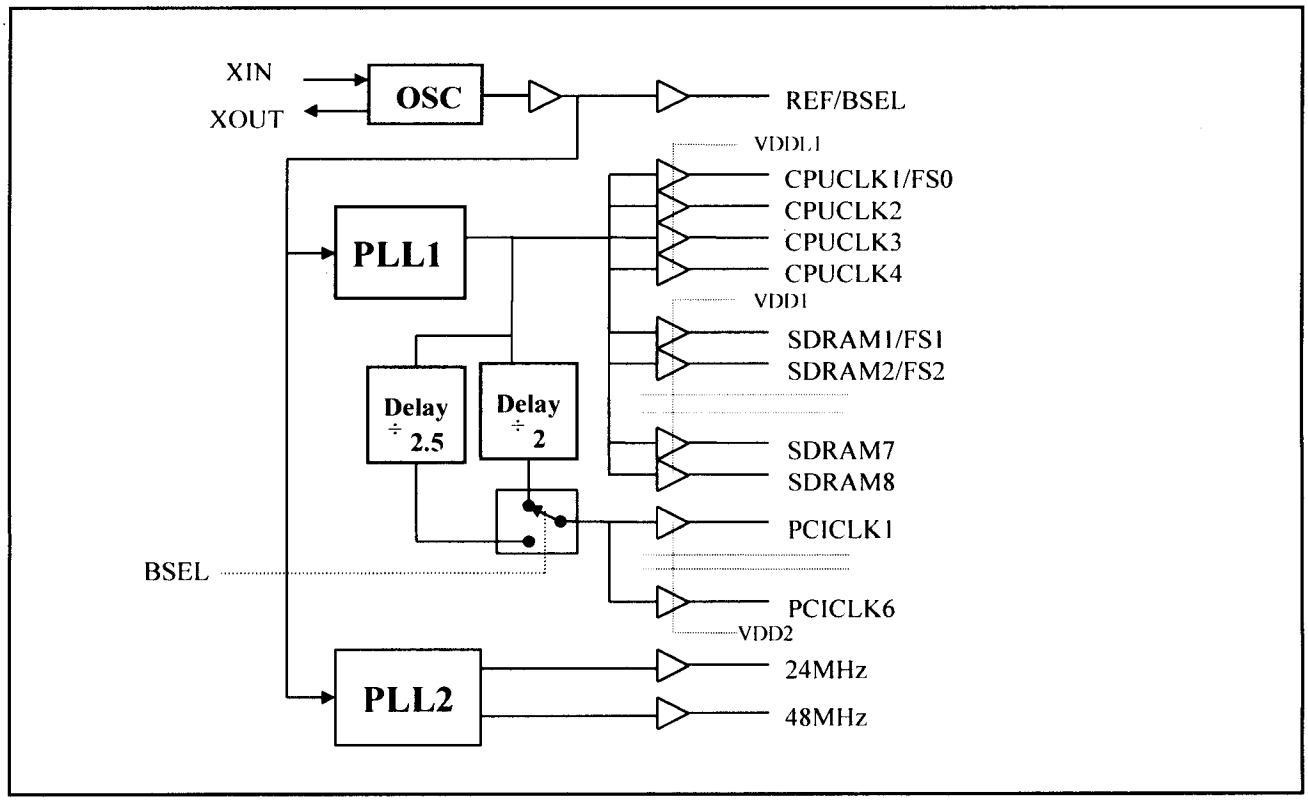
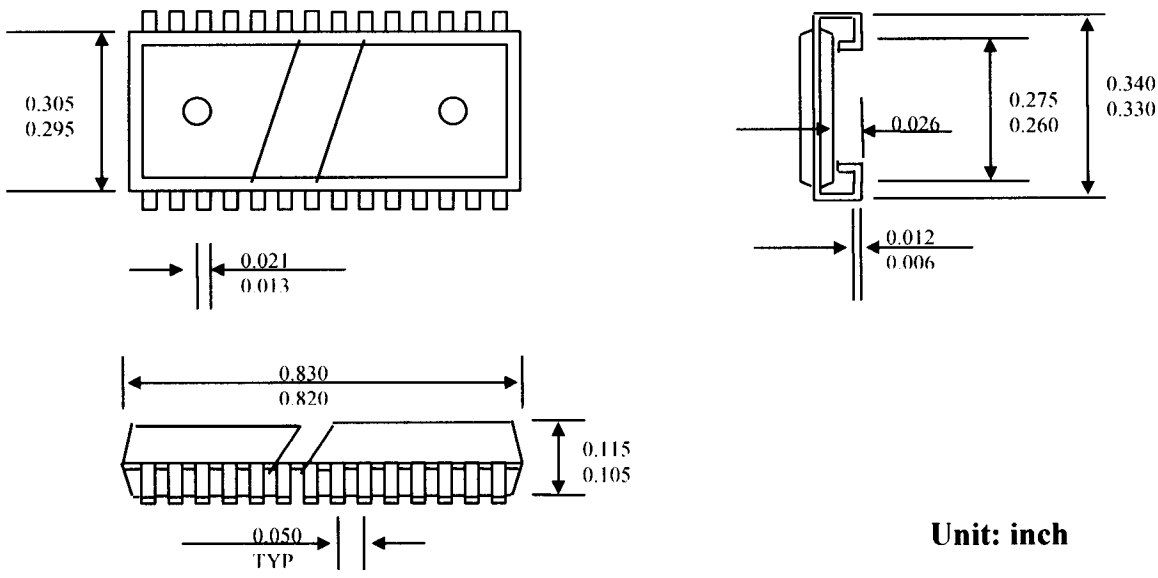
BLOCK DIAGRAM



PACKAGE DIMENSION

32 PIN SOJ



Unit: inch

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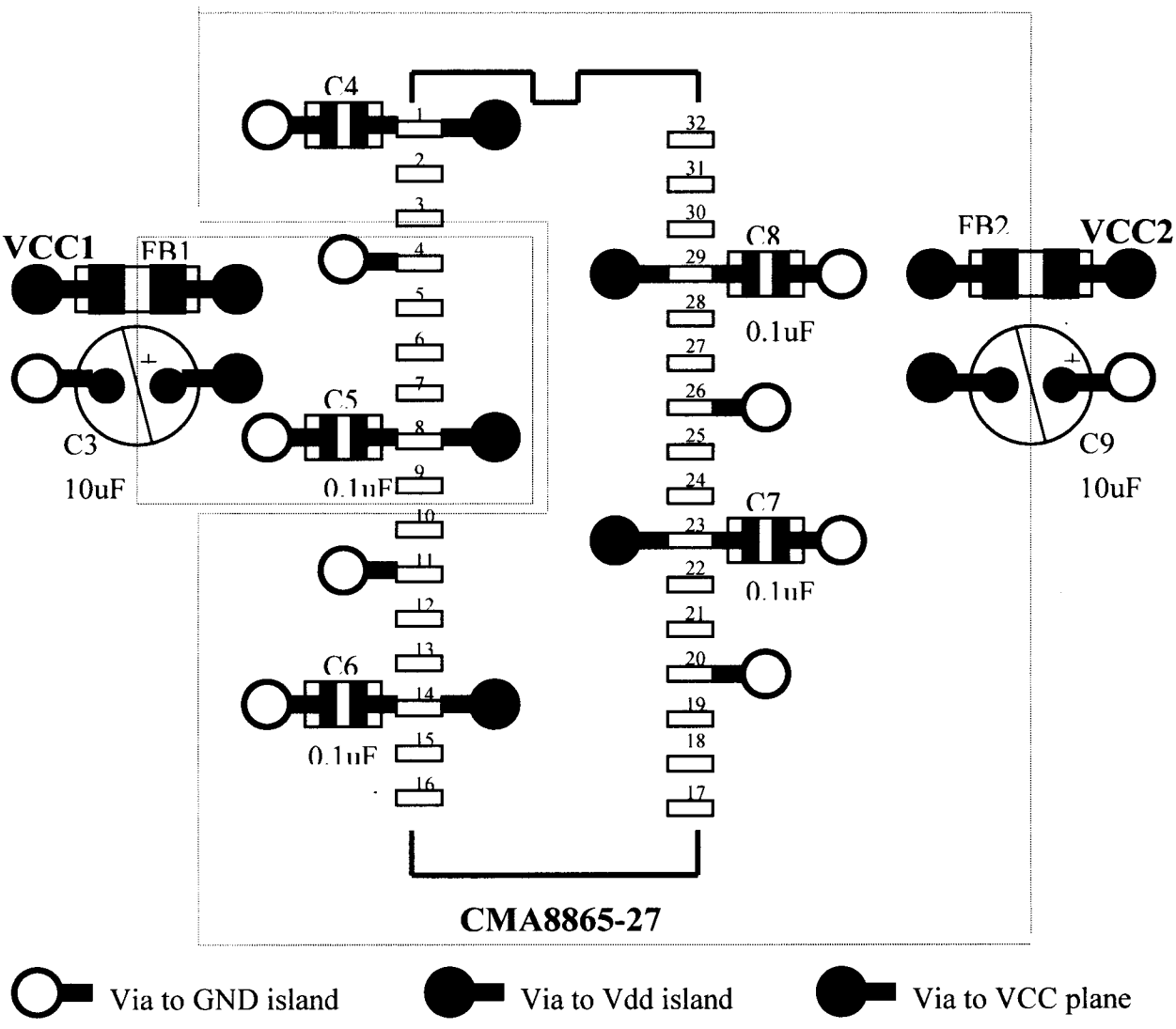
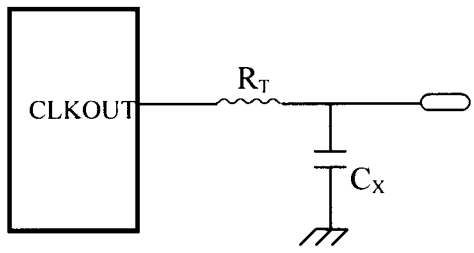
PCB LAYOUT RECOMMENDATION



Notes : We recommend that C4, C5, C6, C7, C8(0.1uF) should have to be placed and connected as close Vdd pins as possible.

OUTPUT CIRCUIT RECOMMENDATION :



R_T : Series Terminating Resistor
C_X : Optional Load Matching Capacitor

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POWER-ON RESET CONFIGURATION INPUT/OUTPUT PINS

The pins 5, 12, 13 and 32 on the CMA8865-27 serve as dual signal functions to the device. During power-on, they act as input pins. The logic level (voltage) that present on these pins at this time is read and stored into internal data latch. At the end of power-on reset, the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal cofiguration register for these pinsm a resistor is connected to either the VDD (logic 1) power supplu or the GND (logic 0) voltage potential. A 4.7 kilohm (4.7k) resistor is used to provide both thesolid CMOS programming voltage needed during the power-on programming period and to provide an insignificant load on the output clock during the subsequent operating period.

The figure as showed below is the recommended application.