Bt451
Bt457
Bt458

125 MHz / 165 MHz Monolithic CMOS 256 Color Palette RAMDAC™

Distinguishing Features

- 165, 125, 110, 80 MHz Operation
- 4:1 or 5:1 Input MUX
- 256-Word Dual Port Color Palette
- 4 Dual Port Overlay Registers
- RS-343A Compatible Outputs
- Bit Plane Read and Blink Masks
- Standard MPU Interface
- 84-pin PLCC or PGA Package
- +5 V CMOS Monolithic Construction

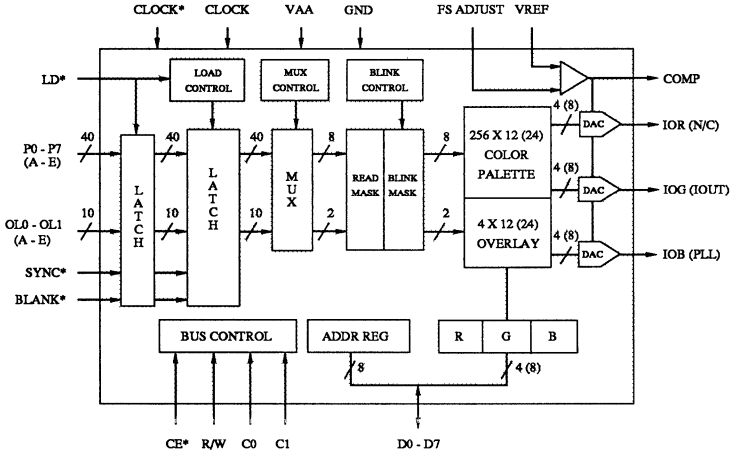
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438, Bt439
- Bt459, Bt460, Bt462, Bt468

Functional Block Diagram



Product Description

The Bt451, Bt457, and Bt458 are pin-compatible and software-compatible RAMDACs designed specifically for high-performance, high-resolution color graphics. The architecture enables the display of 1280 x 1024 bit-mapped color graphics (up to 8 bits per pixel plus up to 2 bits of overlay information), minimizing the use of costly ECL interfacing, as most of the high speed (pixel clock) logic is contained on chip. The multiple pixel ports and internal multiplexing enable TTL-compatible interfacing (up to 32 MHz) to the frame buffer, while maintaining the 165 MHz video data rates required for sophisticated color graphics.

The Bt451 has a 256 x 12 color lookup table with triple 4-bit video D/A converters.

The Bt458 contains a 256 x 24 color lookup table with triple 8-bit video D/A converters.

The Bt457 is a single-channel version of the Bt458 and has a 256 x 8 color lookup table with a single 8-bit video D/A converter. It includes a PLL output to enable sub-pixel synchronization of multiple Bt457s.

On-chip features include programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port color palette RAM.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L458001 Rev. K

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt451/457/458 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and dual-port overlay registers allow color updating without contention with the display refresh process.

As illustrated in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register, color palette RAM entry, or overlay register will be accessed by the MPU.

The 8-bit address register (ADDR0–7) is used to address the internal RAM and registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Bt451/458 Reading/Writing Color Data

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word (12-bit word for the Bt451) and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. Note that the Bt451 uses only the four most significant bits of color data (D4–D7) and ignores D0–D3.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location, which the MPU may read by simply reading another sequence of red, green, and blue data. Note that the Bt451 outputs only 4 bits of color data onto D4–D7 and forces D0–D3 to a logical zero.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU.

ADDR0–7	C1	C0	Addressed by MPU
$xx	0	0	address register
$00–,$FF	0	1	color palette RAM
$00	1	1	overlay color 0
$01	1	1	overlay color 1
$02	1	1	overlay color 2
$03	1	1	overlay color 3
$04	1	0	read mask register
$05	1	0	blink mask register
$06	1	0	command register
$07	1	0	control/test register

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Bt457 Reading/Writing Color Data (Normal Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs a color write cycle, using C0 and C1 to select either the color palette RAM or the overlay registers. The address register then increments to the next location, which the MPU may modify by simply writing another color.

Reading color data is similar to writing, except the MPU executes read cycles.

This mode is useful if a 24-bit data bus is available, as 24 bits of color information (8 bits each of red, green, blue) may be read or written to three Bt457s in a single MPU cycle. In this application, the CE* inputs of all three Bt457s are connected together. If only an 8-bit data bus is available, the CE* inputs must be individually selected during the appropriate color write cycle (red CE* during red write cycle, blue CE* during blue write cycle, etc.).

When accessing the color palette RAM, the address register resets to $00 after a read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a read or write cycle to overlay register 3.

Bt457 Reading/Writing Color Data (RGB Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or the overlay registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. Reading color data is similar to writing, except the MPU executes read cycles.

This mode is useful if only an 8-bit data bus is available. Each Bt457 is programmed to be a red, green, or blue RAMDAC, and will respond only to the assigned color read or write cycle. In this application, the Bt457s share a common 8-bit data bus. The CE* inputs of all three Bt457s must be asserted simultaneously only during color read/write cycles and address register write cycles.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8t bits of the address register (ADDR0–7) are accessible to the MPU.

Additional Information

Although the color palette RAM and overlay registers are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers is also done through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt451/457/458 incorporate internal latches and multiplexers. As illustrated in Figure 1, on the rising edge of LD*, sync and blank information, color (up to 8 bits per pixel), and overlay (up to 2 bits per pixel) information, for either four or five consecutive pixels, are latched into the device. Note that, with this configuration, the sync and blank timing will be recognized only with four- or five-pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing.

Each clock cycle, the Bt451/457/458 outputs color information based on the {A} inputs, followed by the {B} inputs, etc., until all four or five pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character or cursor generation logic.

To simplify the frame buffer interface timing, LD* may be phase shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by four or five, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than four, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

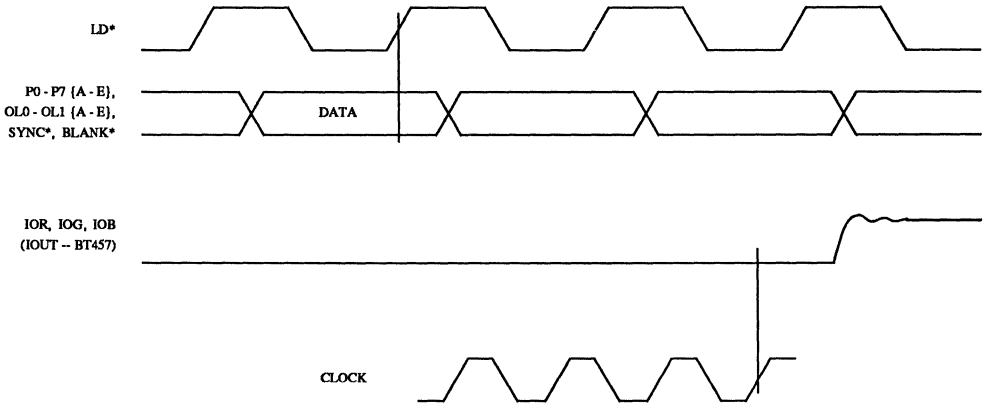


Figure 1. Video Input/Output Timing.

Circuit Description (continued)

Color Selection

Each clock cycle, 8 bits of color information (P0–P7) and 2 bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt451/457/458 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining that BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAM. Table 2 illustrates the truth table used for color selection.

Video Generation

Every clock cycle, the selected color information from the color palette RAMs or overlay registers is presented to the D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) on the Bt451 and Bt458 contains sync information. Table 3 details how the SYNC* and BLANK* inputs modify the output levels.

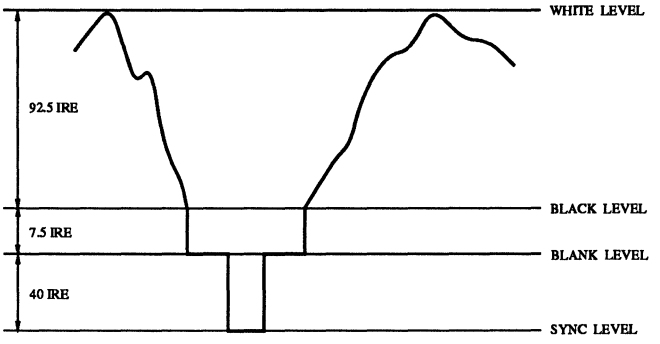
The D/A converters on the Bt451, Bt457, and Bt458 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current-steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full scale output current against temperature and power supply variations.

CR6	OL1	OL0	P0–P7	Addressed by frame buffer
1	0	0	$00	color palette entry $00
1	0	0	$01	color palette entry $01
:	:	:	:	:
1	0	0	$FF	color palette entry $FF
0	0	0	$xx	overlay color 0
x	0	1	$xx	overlay color 1
x	1	0	$xx	overlay color 2
x	1	1	$xx	overlay color 3

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)

IOR, IOB		IOG (IOUT)	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly terminated load, RSET = 523 Ω, VREF = 1.235 V. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms.

Description	IOG (IOUT) (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 523 Ω, VREF = 1.235 V. Note that the Bt451 uses only the upper four DAC input data bits.

Table 3. Video Output Truth Table.

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. CR0 corresponds to data bus bit D0.

CR7	Multiplex select (0) 4:1 multiplexing (1) 5:1 multiplexing	This bit specifies whether 4:1 or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and {E} overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/4 the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be 1/5 the CLOCK rate. Note that it is possible to reset the pipeline delay of the Bt457/458 to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt457/458 must again be reset to a fixed pipeline delay.
CR6	RAM enable (0) use overlay color 0 (1) use color palette RAM	When the overlay select bits are 00, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.
CR5, CR4	Blink rate selection (00) 16 on, 48 off (25/75) (01) 16 on, 16 off (50/50) (10) 32 on, 32 off (50/50) (11) 64 on, 64 off (50/50)	These 2 bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off).
CR3	OL1 blink enable (0) disable blinking (1) enable blinking	If a logical one, this bit forces the OL1 {A–E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL1 {A–E} inputs. In order for overlay 1 bit plane to blink, bit CR1 must be set to a logical one.
CR2	OL0 blink enable (0) disable blinking (1) enable blinking	If a logical one, this bit forces the OL0 {A–E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL0 {A–E} inputs. In order for overlay 0 bit plane to blink, bit CR0 must be set to a logical one.

Internal Registers (continued)

Command Register (continued)

CR1	OL1 display enable (0) disable (1) enable	If a logical zero, this bit forces the OL1 {A–E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL1 {A–E} inputs.
CR0	OL0 display enable (0) disable (1) enable	If a logical zero, this bit forces the OL0 {A–E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL0 {A–E} inputs.

Read Mask Register

The read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. D0 corresponds to bit plane 0 (P0 {A–E}) and D7 corresponds to bit plane 7 (P7 {A–E}). Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized.

Blink Mask Register

The blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by the command register. D0 corresponds to bit plane 0 (P0 {A–E}) and D7 corresponds to bit plane 7 (P7 {A–E}). In order for a bit plane to blink, the corresponding bit in the read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized.

Internal Registers (continued)

Bt451/458 Test Register

The test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read by the MPU at any time, and is not initialized. When writing to the register, the upper 4bits (D4–D7) are ignored.

The contents of the test register are defined as follows:

D7–D4	color information (4 bits of red, green, or blue)
D3	low (logical one) or high (logical zero) nibble
D2	blue enable
D1	green enable
D0	red enable

To use the test register, the host MPU writes to it, setting one, and only one, of the (red, green, blue) enable bits. These bits specify which 4 bits of color information the MPU wishes to read (R0–R3, G0–G3, B0–B3, R4–R7, G4–G7, or B4–B7). When the MPU reads the test register, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits, and the lower 4 bits contain the (red, green, blue, low or high nibble) enable information previously written. Note that either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper 4 bits of red color information being presented to the D/A converters, the MPU writes to the test register, setting only the red enable bit. The MPU then proceeds to read the test register, keeping the pixel data stable, which results in D4–D7 containing R4–R7 color bits, and D0–D3 containing (red, green, blue, low or high nibble) enable information, as illustrated below:

D7	R7
D6	R6
D5	R5
D4	R4
D3	0
D2	0
D1	0
D0	1

Note that since the Bt451 has 4-bit D/A converters, bit D3 of the test register will always be a logical zero.

Internal Registers (continued)

Bt457 Control/Test Register

The control/test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converter. It may be written to or read by the MPU at any time, and is not initialized. When writing to the register, the upper 4 bits (D4–D7) are ignored.

The contents of the test register are defined as follows:

D7–D4	color information
D3	low (logical one) or high (logical zero) nibble
D2	blue channel enable
D1	green channel enable
D0	red channel enable

To use the control/test register, the MPU writes to it, specifying the low or high nibble of color information. When the MPU reads the register, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits, and the lower 4 bits contain whatever was previously written to the register. Note that either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

The red, green, and blue enable bits are used to specify the mode of writing color data to, and reading color data from, the Bt457. If all three enable bits are a logical zero, each write cycle to the color palette RAM or overlay registers loads 8 bits of color data. During each read cycle of the color palette RAM or overlay registers, 8 bits of color data are output onto the data bus. If a 24-bit data bus is available, this enables three Bt457s to be accessed simultaneously.

If any of the red, green, blue enable bits are a logical one, the Bt457 assumes the MPU is reading and writing color information using red, green, blue cycles, such as are used on the Bt451 and Bt458. Setting the appropriate enable bit configures the Bt457 to output or input color data only for the color read/write cycle corresponding to the enabled color. Thus, if the green enable bit is a logical one, and a red, green, blue write cycle occurred, the Bt457 would input data only during the green write cycle. If a red, green, blue read cycle occurred, the Bt457 would output data only during the green read cycle. Note that CE* must be a logical zero during each of the red, green, blue cycles. One, and only one, of the enable bits must be a logical one. This mode of operation is useful where only an 8-bit data bus is available, and the software drivers are written for RGB operation.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Table 3. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 3; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LD*. If sync information is not to be generated on the IOG output, this pin should be connected to GND.
LD*	Load control input (TTL compatible). The P0–P7 {A–E}, OL0–OL1 {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is either 1/4 or 1/5 the CLOCK rate, may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the AC Characteristics section.
P0–P7 {A–E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. Either four or five consecutive pixels (up to 8 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that the {A} pixel is output first, followed by the {B} pixel, etc., until all four or five pixels have been output, at which point the cycle repeats.
OL0–OL1 {A–E}	Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LD*, and in conjunction with bit 6 of the command register, specify which palette is to be used for color information, as follows:

OL1	OL0	CR6 = 1	CR6 = 0
0	0	color palette RAM	overlay color 0
0	1	overlay color 1	overlay color 1
1	0	overlay color 2	overlay color 2
1	1	overlay color 3	overlay color 3

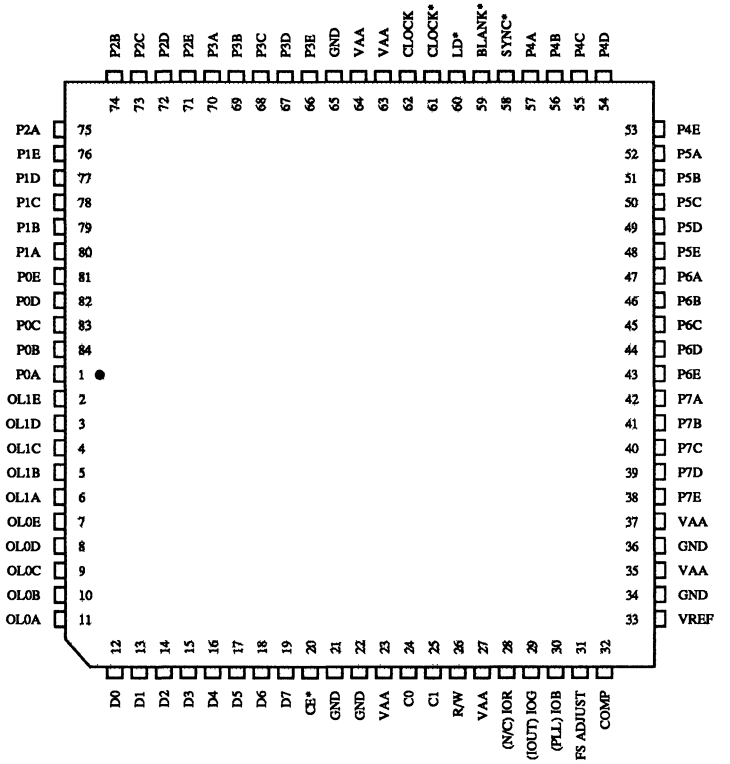
When accessing the overlay palette, the P0–P7 {A–E} inputs are ignored. Overlay information bits (up to 2 bits per pixel) for either four or five consecutive pixels are input through this port. Unused inputs should be connected to GND.

IOR, IOG, IOB, IOUT	Red, green, and blue video current outputs. These high -mpedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 3). The Bt457 outputs IOUT rather than IOR, IOG, and IOB.
PLL	Phase lock loop current output—Bt457 only. This high-impedance current source is used to enable multiple Bt457s to be synchronized with sub-pixel resolution when used with an external PLL. A logical one on the BLANK* input results in no current being output onto this pin, while a logical zero results in the following current being output: PLL (mA) = 3,227 * VREF (V) / RSET (Ω) If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 3). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. *Refer to PC Board Layout Considerations for critical layout criteria.*
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 3). Note that the IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG (or IOUT for the Bt457) is: RSET (Ω) = 11,294 * VREF (V) / IOG (mA) The full scale output current on IOR and IOB (for the Bt451 and Bt458) for a given RSET is: IOR, IOB (mA) = 8,067 * VREF (V) / RSET (Ω)
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 3. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)—84-Pin J-Lead Package



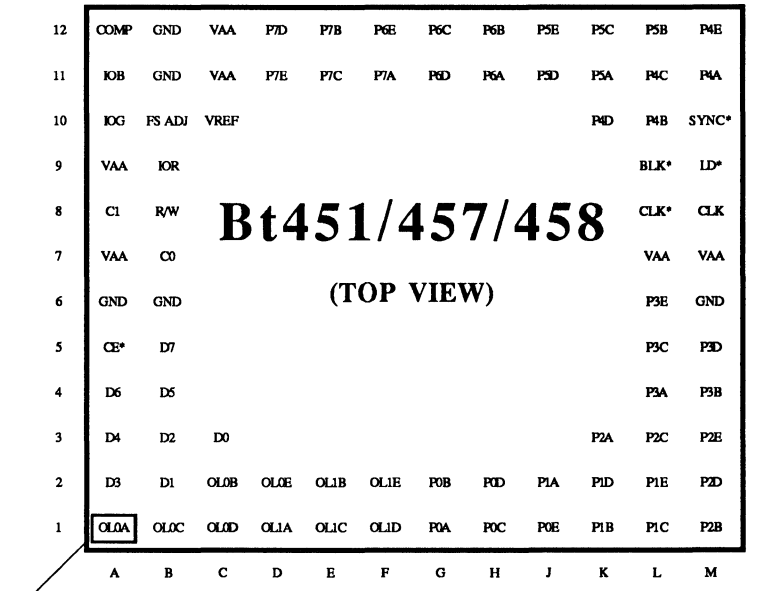
Note: Bt457 pin names are in parentheses.

Pin Descriptions (continued)—84-pin PGA Package

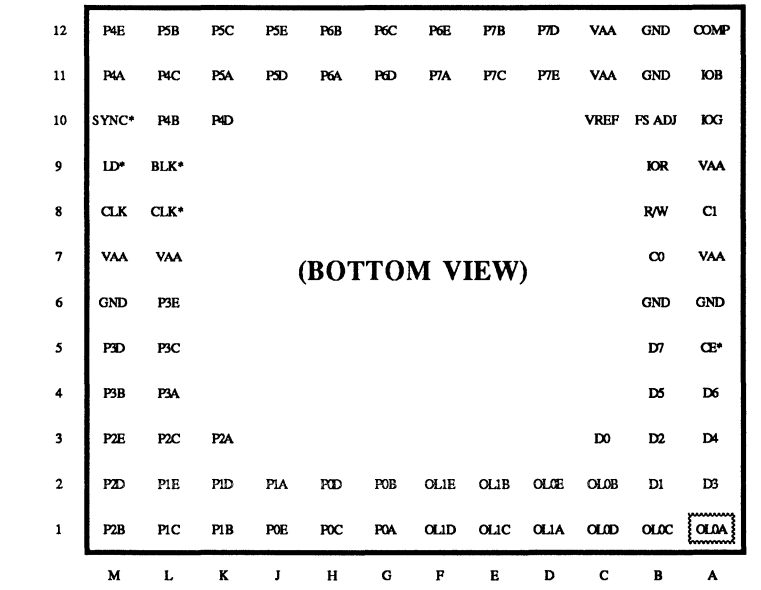
Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	L9	P5A	K11	VAA	C12
SYNC*	M10	P5B	L12	VAA	C11
LD*	M9	P5C	K12	VAA	A9
CLOCK*	L8	P5D	J11	VAA	L7
CLOCK	M8	P5E	J12	VAA	M7
				VAA	A7
P0A	G1	P6A	H11		
P0B	G2	P6B	H12	GND	B12
P0C	H1	P6C	G12	GND	B11
P0D	H2	P6D	G11	GND	M6
P0E	J1	P6E	F12	GND	B6
				GND	A6
P1A	J2	P7A	F11		
P1B	K1	P7B	E12	COMP	A12
P1C	L1	P7C	E11	FS ADJUST	B10
P1D	K2	P7D	D12	VREF	C10
P1E	L2	P7E	D11		
				CE*	A5
P2A	K3	OL0A	A1	R/W	B8
P2B	M1	OL0B	C2	C1	A8
P2C	L3	OL0C	B1	C0	B7
P2D	M2	OL0D	C1		
P2E	M3	OL0E	D2	D0	C3
				D1	B2
P3A	L4	OL1A	D1	D2	B3
P3B	M4	OL1B	E2	D3	A2
P3C	L5	OL1C	E1	D4	A3
P3D	M5	OL1D	F1	D5	B4
P3E	L6	OL1E	F2	D6	A4
				D7	B5
P4A	M11	IOG (IOUT)	A10		
P4B	L10	IOB (PLL)	A11		
P4C	L11	IOR (N/C)	B9		
P4D	K10				
P4E	M12				

Note: Bt457 pin names are in parentheses.

Pin Descriptions (continued)—84-pin PGA Package



alignment marker (on top)



Pin	Bt451/458	Bt457
A10	IOG	IOUT
A11	IOB	PLL
B9	IOR	N/C

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in *Bt451/457/458 Evaluation Module Operation and Measurements,* application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt451/457/458 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a 6-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferable analog ground plane), layer 3 the analog power plane, using the remaining layers for digital traces and digital power supplies.

The optimum layout enables the Bt451/457/458 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8" inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground partitioning isolation technique is constrained by the noise margin degradation during digital readback of the Bt451/457/458.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and VREF circuitry should be used, as shown in Figure 3. Another isolated ground plane is used for the GND pins of the Bt451/457/458 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt451/457/458 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt451/457/458 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of three groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 33 µF capacitor is for low frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low frequency supply noise will require a larger value. Lead lengths should be minimized for best performance so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may helpto fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt451/457/458 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit by using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt451/457/458 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt451/457/458 to minimize reflections. Unused analog outputs should be connected to GND.

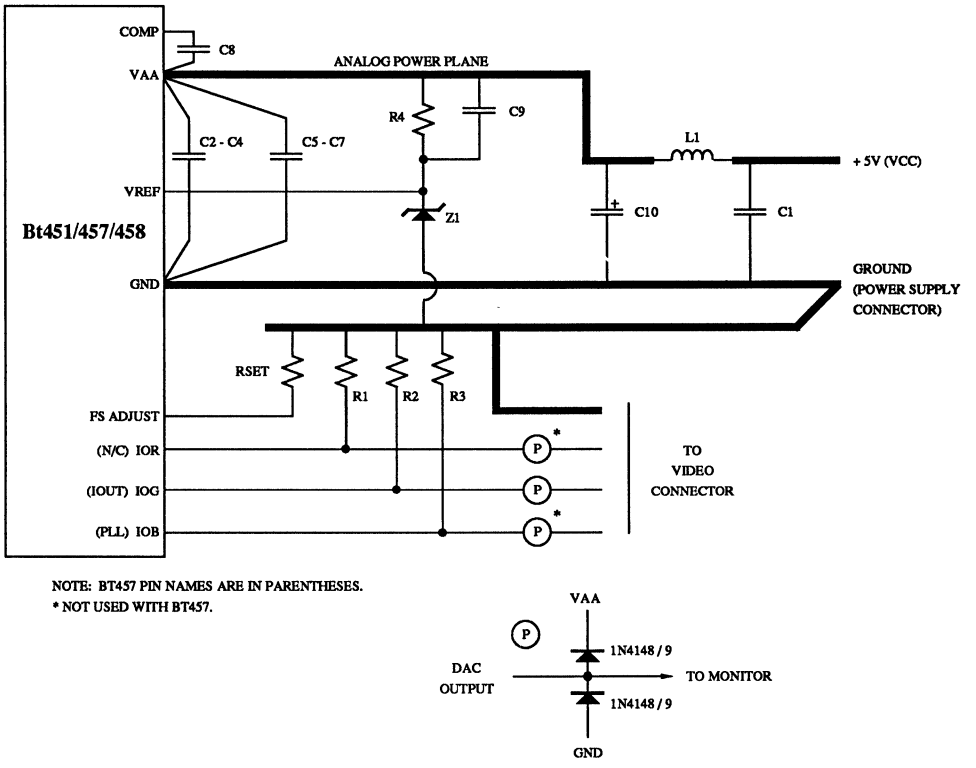
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

Analog Output Protection

The Bt451/457/458 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1–C4, C8, C9	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5–C7	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C10	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt451/457/458. R3 not used with Bt457 (see Application Information section).

Figure 3. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Due to the high clock rates at which the Bt451/457/458 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (typically a 220 Ω resistor to VCC and a 330 Ω resistor to GND). The termination resistors should be as close as possible to the Bt451/457/458.

165 MHz applications require robust ECL clock signals with strong pull-down (~20 mA at VOH) and double termination for clock trace lengths greater than 2 inches.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt451/457/458 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by four or five (depending on whether 4:1 or 5:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase-shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

It is recommended that the Bt438 or Bt439 Clock Generator Chips be used to generate the clock and load signals. Both support the 4:1 and 5:1 input multiplexing of the Bt451/457/458, and set the pipeline delay of the Bt457 and Bt458 to eight clock cycles. Figures 4 and 5 illustrate using the Bt438 with the Bt451/457/458.

In applications using a single Bt457, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 Ω).

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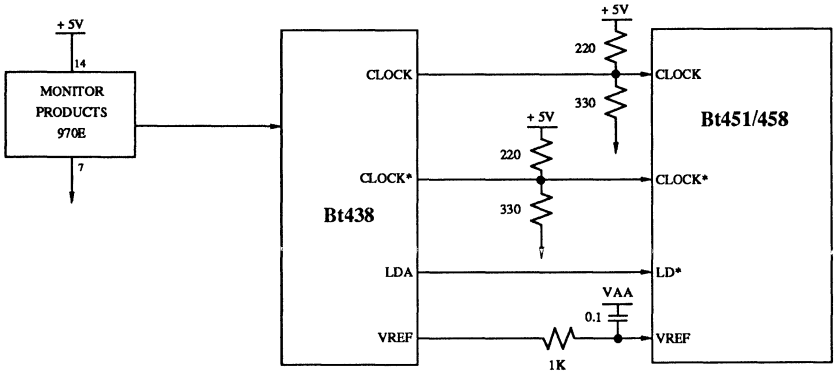

Figure 4. Generating the Bt451/458 Clock Signals.

Application Information (continued)

Setting the Pipeline Delay (Bt457, Bt458)

The pipeline delay of the Bt457/458, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt457/458 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt457/458.

To reset the Bt457/458, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for **at least** three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than one clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

The resetting of the Bt457/458 to an eight clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if the multiple Bt457/458s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

In standard operation, the Bt457/458 need be reset only following a power-up or reset condition. Under these circumstances the on-chip blink circuitry may be used.

Bt457 Color Display Applications

For color display applications where up to four Bt457s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1, and 5:1 input multiplexing of the Bt457, synchronizes them to sub-pixel resolution, and sets the pipeline delay of the Bt457 to eight clock cycles. The Bt439 may also be used to interface the Bt457 to a TTL clock. Figure 6 illustrates using the Bt439 with the Bt457.

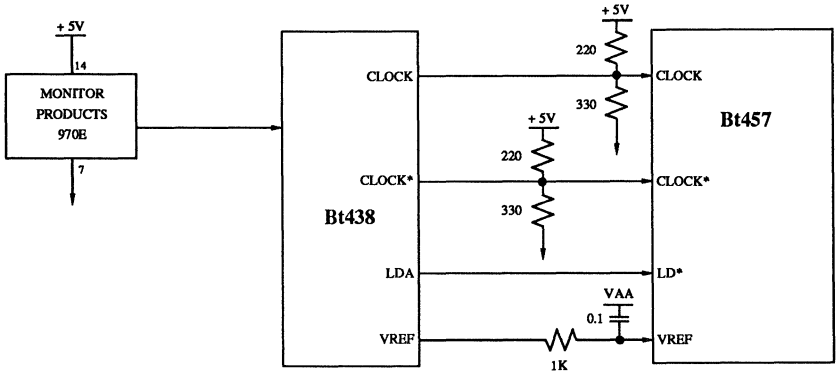

Figure 5. Generating the Bt457 Clock Signals (Monochrome Application).

Application Information (continued)

Sub-pixel synchronization is supported via the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt457, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt457s, and adjusts the phase of each of the CLOCK and CLOCK* signals to the Bt457s to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to assure proper clock alignment.

If sub-pixel synchronization of multiple Bt457s is not necessary, the Bt438 Clock Generator Chip may be used instead of the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt457s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The VREF inputs of the Bt457s must still have a 0.1 µF bypass capacitor to VAA. The PLL outputs would not be used and should be connected to GND (either directly or through a resistor up to 150 Ω).

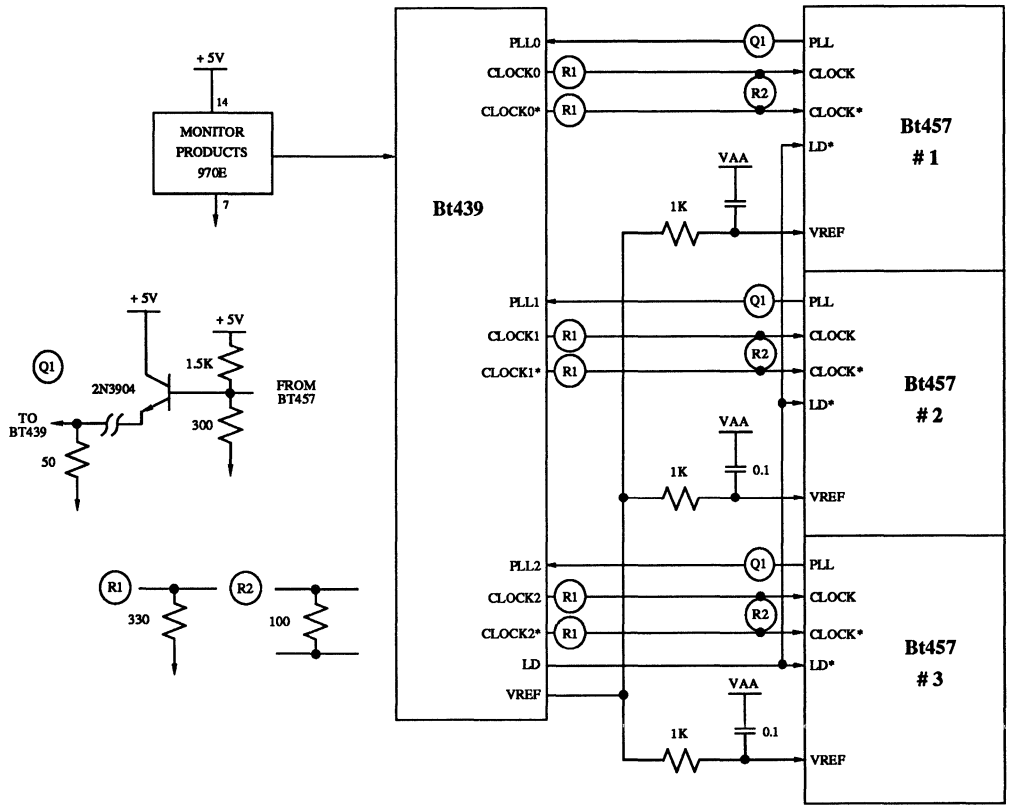

Figure 6. Generating the Bt457 Clock Signals (Color Application).

Application Information (continued)

Using Multiple Devices

When using multiple RAMDACs, each RAMDAC should have its own power plane ferrite bead. In addition, a single voltage reference may drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance may be obtained if each RAMDAC has its own voltage reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each RAMDAC must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

Bt457 Non-Video Applications

The Bt457 may be used in non-video applications by disabling the video-specific control signals. SYNC* should be a logical zero and BLANK* should be a logical one.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$RSET\ (\Omega) = 7{,}457 * VREF\ (V) / Iout\ (mA)$$

With the DAC data inputs at $00, there is a DC offset current (Imin) defined as follows:

$$Imin\ (mA) = 610 * VREF\ (V) / RSET\ (\Omega)$$

Therefore, the total full-scale output current will be Iout + Imin.

Initializing the Bt451/458

Following a power-on sequence, the Bt451/458 must be initialized. If controlling the clock/LD* sequence to reset the pipeline delay of the Bt458 to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be re-initialized any time the multiplex selection is changed (i.e., from 4:1 to 5:1 input multiplexing).

This sequence will configure the Bt451/458 as follows:

4:1 multiplexed operation
no overlays
no blinking

Control Register Initialization	C1, C0
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10

Color Palette RAM Initialization	
Write $00 to address register	00
Write red data to RAM (location $00)	01
Write green data to RAM (location $00)	01
Write blue data to RAM (location $00)	01
Write red data to RAM (location $01)	01
Write green data to RAM (location $01)	01
Write blue data to RAM (location $01)	01
:	:
Write red data to RAM (location $FF)	01
Write green data to RAM (location $FF)	01
Write blue data to RAM (location $FF)	01

Overlay Color Palette Initialization	
Write $00 to address register	00
Write red data to overlay (location $00)	11
Write green data to overlay (location $00)	11
Write blue data to overlay (location $00)	11
Write red data to overlay (location $01)	11
Write green data to overlay (location $01)	11
Write blue data to overlay (location $01)	11
:	:
Write red data to overlay (location $03)	11
Write green data to overlay (location $03)	11
Write blue data to overlay (location $03)	11

Application Information (continued)

Initializing the Bt457 (Monochrome)

Following a power-on sequence, the Bt457 must be initialized. If controlling the clock/LD* sequence to reset the pipeline delay of the Bt457 to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be re-initialized any time the multiplex selection is changed (i.e., from 4:1 to 5:1 input multiplexing).

This sequence will configure the Bt457 as follows:

4:1 multiplexed operation
no overlays
no blinking
color data written/read every cycle

Control Register Initialization	C1, C0
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10

Color Palette RAM Initialization	
Write $00 to address register	00
Write data to RAM (location $00)	01
Write data to RAM (location $01)	01
:	:
Write data to RAM (location $FF)	01

Overlay Color Palette Initialization	
Write $00 to address register	00
Write data to overlay (location $00)	11
Write data to overlay (location $01)	11
:	:
Write data to overlay (location $03)	11

Initializing the Bt457 (Color) 24-bit MPU Data Bus

In this example, three Bt457s are being used in parallel to generate true color. A 24-bit MPU data bus is available for accessing all three Bt457s in parallel.

The operation and initialization are the same as for the Bt457 being used in a monochrome application.

Initializing the Bt457 (Color) 8-bit MPU Data Bus

In this example, three Bt457s are being used in parallel to generate true color. An 8-bit MPU data bus is available for accessing the Bt457s.

Note that while accessing the command, read mask, blink mask, and control/test, and address register, each Bt457 must be accessed individually. While accessing the color palette RAM or overlay registers, all three Bt457s are accessed simultaneously.

Following a power-on sequence, the Bt457s must be initialized. If controlling the clock/LD* sequence to reset the pipeline delay of the Bt457s to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be re-initialized any time the multiplex selection is changed (i.e., from 4:1 to 5:1 input multiplexing).

This sequence will configure the Bt457s as follows:

4:1 multiplexed operation
no overlays
no blinking
initialize each Bt457 as a red, green, or blue device

Control Register Initialization	C1, C0
Red Bt457	
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $01 to test register	10
Green Bt457	
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $02 to test register	10

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Application Information (continued)

Blue Bt457

Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $04 to test register	10

Color Palette RAM Initialization

Write $00 to all three address registers	00
Write red data to RAM (location $00)	01
Write green data to RAM (location $00)	01
Write blue data to RAM (location $00)	01
Write red data to RAM (location $01)	01
Write green data to RAM (location $01)	01
Write blue data to RAM (location $01)	01
:	:
Write red data to RAM (location $FF)	01
Write green data to RAM (location $FF)	01
Write blue data to RAM (location $FF)	01

Overlay Color Palette Initialization

Write $00 to all three address registers	00
Write red data to overlay (location $00)	11
Write green data to overlay (location $00)	11
Write blue data to overlay (location $00)	11
Write red data to overlay (location $01)	11
Write green data to overlay (location $01)	11
Write blue data to overlay (location $01)	11
:	:
Write red data to overlay (location $03)	11
Write green data to overlay (location $03)	11
Write blue data to overlay (location $03)	11

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		523		Ω

Absolute Maximum Ratings

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Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8 (4)	8 (4)	8 (4)	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1 (1/8)	LSB
Differential Linearity Error	DL			±1 (1/16)	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	Volts
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –800 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG or IOUT		6.29	7.62	8.96	mA
Sync Level on IOG or IOUT		0	5	50	µA
LSB Size					
Bt451			1.175		mA
Bt457, Bt458			69.1		µA
DAC to DAC Matching*			2	5	%
Output Compliance	VOC	-1.0		+1.2	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.5		%/% ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Does not apply to the Bt457.

AC Characteristics

		165 MHz Devices			125 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			165			125	MHz
LD* Rate	LDmax			41.25			31.25	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	50			50			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	3			3			ns
Pixel and Control Setup Time	10	3			3			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	6.06			8			ns
Clock Pulse Width High Time	13	2.6			3.2			ns
Clock Pulse Width Low Time	14	2.6			3.2			ns
LD* Cycle Time	15	24.24			32			ns
LD* Pulse Width High Time	16	10			13			ns
LD* Pulse Width Low Time	17	10			13			ns
Analog Output Delay	18		12			12		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time	20			8			8	ns
Clock and Data Feedthrough*			35			35		pV–sec
Glitch Impulse*			50			50		pV–sec
Analog Output Skew**			0	2		0	2	ns
Pipeline Delay		6		10	6		10	Clocks
VAA Supply Current***	IAA							
Bt451			n/a	n/a		310	400	mA
Bt458			310	370		225	330	mA
Bt457			n/a	n/a		200	250	mA

See test conditions on next page.

AC Characteristics (continued)

Parameter	Symbol	110 MHz Devices Min	110 MHz Devices Typ	110 MHz Devices Max	80 MHz Devices Min	80 MHz Devices Typ	80 MHz Devices Max	Units
Clock Rate	Fmax			110			80	MHz
LD* Rate	LDmax			27.5			20	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	50			50			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	3			3			ns
Pixel and Control Setup Time	10	3			4			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	9.09			12.5			ns
Clock Pulse Width High Time	13	4			5			ns
Clock Pulse Width Low Time	14	4			5			ns
LD* Cycle Time	15	36.36			50			ns
LD* Pulse Width High Time	16	15			20			ns
LD* Pulse Width Low Time	17	15			20			ns
Analog Output Delay	18		12			12		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time	20			8			8	ns
Clock and Data Feedthrough*			35			35		pV–sec
Glitch Impulse*			50			50		pV–sec
Analog Output Skew**			0	2		0	2	ns
Pipeline Delay		6		10	6		10	Clocks
VAA Supply Current***	IAA							
Bt451			295	385		265	355	mA
Bt458			210	315		200	285	mA
Bt457			190	240		170	220	mA

See test conditions on next page.

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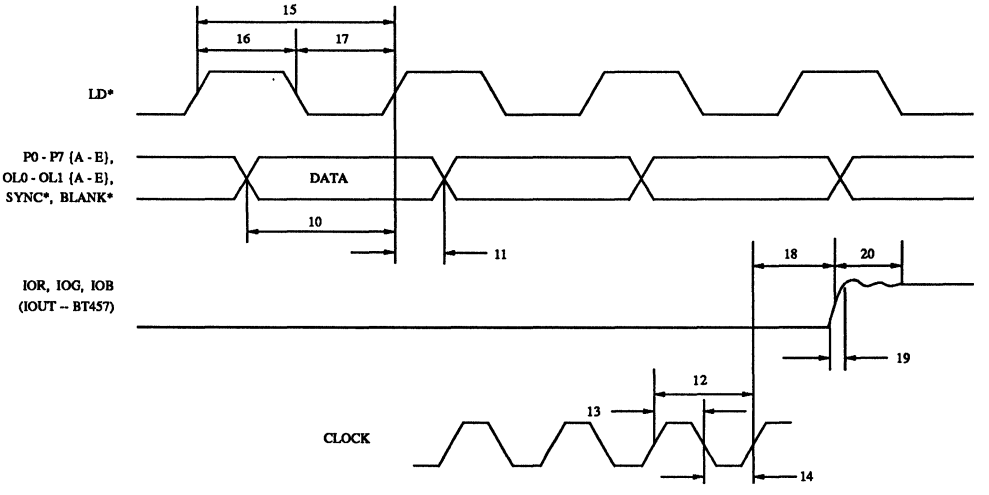
AC Characteristics (continued)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA–0.8 to VAA–1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 7. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 k-Ω resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**Does not apply to the Bt457.

***At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C IAA (max) at VAA = 5.25 V, TA = 0° C



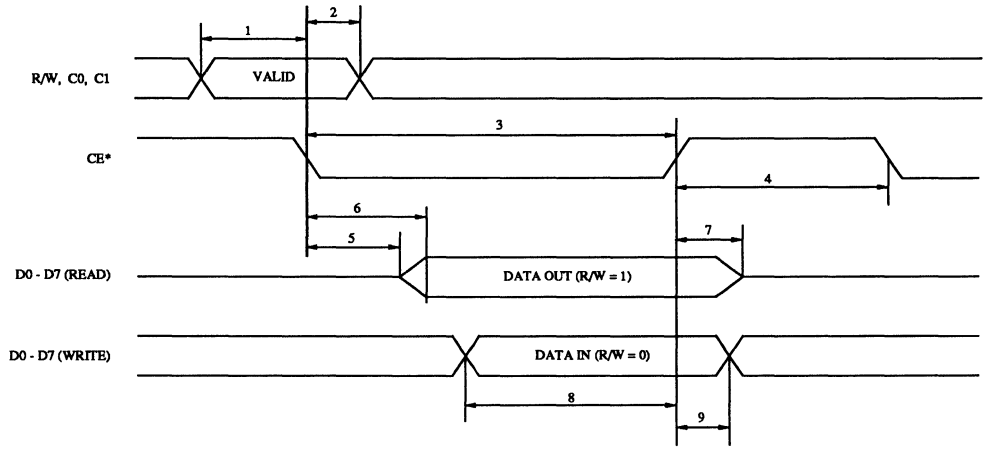
Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full-scale transition.

Note 2: Output settling time measured from 50% point of full-scale transition to output settling within ±1 LSB for the Bt457/458 or ± 1/8LSB for the Bt451.

Note 3: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 7. Video Input/Output Timing.

Timing Waveforms (continued)



MPU Read/Write Timing.

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Ordering Information

Model Number	RAM	DACs	Speed	Package	Ambient Temperature Range
Bt458LG165	256 x 24	triple 8-bit	165 MHz	84-pin Ceramic PGA	0° to +70° C
Bt458KG125	256 x 24	triple 8-bit	125 MHz	84-pin Ceramic PGA	0° to +70° C
Bt458KG110	256 x 24	triple 8-bit	110 MHz	84-pin Ceramic PGA	0° to +70° C
Bt458KG80	256 x 24	triple 8-bit	80 MHz	84-pin Ceramic PGA	0° to +70° C.

Ordering Information (continued)

Model Number	RAM	DACs	Speed	Package	Ambient Temperature Range
Bt458LPJ165	256 x 24	triple 8-bit	165 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt458LPJ125	256 x 24	triple 8-bit	125 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt458LPJ110	256 x 24	triple 8-bit	110 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt458LPJ80	256 x 24	triple 8-bit	80 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt451KG125	256 x 12	triple 4-bit	125 MHz	84-pin Ceramic PGA	0° to +70° C
Bt451KG110	256 x 12	triple 4-bit	110 MHz	84-pin Ceramic PGA	0° to +70° C
Bt451KG80	256 x 12	triple 4-bit	80 MHz	84-pin Ceramic PGA	0° to +70° C
Bt451KPJ125	256 x 12	triple 4-bit	125 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt451KPJ110	256 x 12	triple 4-bit	110 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt451KPJ80	256 x 12	triple 4-bit	80 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt457KG125	256 x 8	single 8-bit	125 MHz	84-pin Ceramic PGA	0° to +70° C
Bt457KG110	256 x 8	single 8-bit	110 MHz	84-pin Ceramic PGA	0° to +70° C
Bt457KG80	256 x 8	single 8-bit	80 MHz	84-pin Ceramic PGA	0° to +70° C
Bt457KPJ125	256 x 8	single 8-bit	125 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt457KPJ110	256 x 8	single 8-bit	110 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt457KPJ80	256 x 8	single 8-bit	80 MHz	84-Pin Plastic J-Lead	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
I	Expanded PCB layout section, changed AC parameter "CE* asserted to data bus driven" from 10 ns to 7 ns minimum.
J	Revised AC parameter "VAA Supply Current (Max)" for the Bt457: 80 MHz changed from 190 mA to 220 mA, 110 MHz changed from 210 mA to 240 mA and 125 MHz changed from 220 mA to 250 mA.
K	Changed speed grade from 170 MHz to 165 MHz, changed PLL feedback circuitry, consolidated Bt458 power specs. Changed AC Characteristics CLOCK, Load Cycle, and Pulse Width times, changed typical analog output delay times.