Bt438

250 MHz Clock Generator Chip for CMOS RAMDACs™

Distinguishing Features

- 250 MHz Operation
- Differential ECL Clock Generation
- Divide by 3, 4, 5, or 8 of the Clock
- Divide by 2 and 4 of the Load
- Resets Pipeline Delay of the RAMDAC
- 1.2 V Voltage Reference Output
- Single +5 V Power Supply
- 20-pin DIP or 28-pin PLCC Package
- Typical Power Dissipation: 325 mW

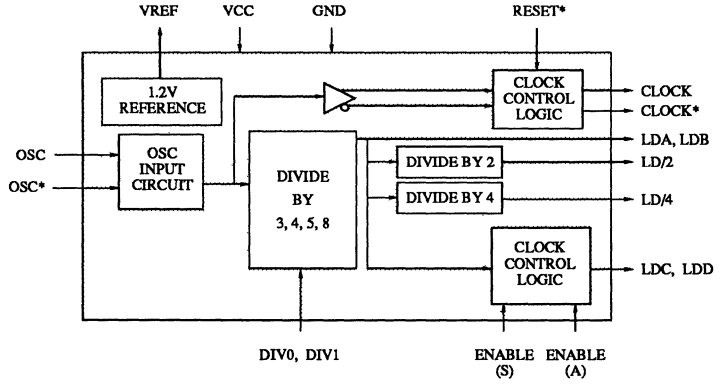
Customer Benefits

- Reduces PC Board Area
- Simplifies RAMDAC Design
- Cost Reduction over Discretes
- Increases System Reliability

Related Products

- Bt439

Functional Block Diagram



Product Description

The Bt438 is a clock generator for the high-speed Brooktree CMOS RAMDACs. It interfaces a 10KH ECL oscillator operating from a single +5 V supply to the RAMDAC, generating the necessary clock and control signals.

The clock output may be divided by three, four, five, or eight to generate the load signal. The load signal is also divided by two and four for clocking video timing logic, etc.

A second load signal may be synchronously or asynchronously controlled to enable starting and stopping the clocking of the video DRAMs.

The Bt438 also optionally configures the pipeline delay of the RAMDAC to a fixed pipeline delay.

An on-chip 1.2 V voltage reference is also provided, and may be used to provide the reference voltage for up to four RAMDACs.

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Circuit Description

The Bt438 is designed to interface to a 10KH ECL crystal oscillator and generate the clock signals required by the RAMDACs. The OSC and OSC* inputs are designed to interface to a 10KH ECL oscillator operating from a single +5 V power supply.

The CLOCK and CLOCK* outputs are designed to interface directly to the CLOCK and CLOCK* inputs of the RAMDACs. The output levels are compatible with 10KH ECL logic operating from a single +5 V power supply.

DIV0 and DIV1 are used to specify whether the pixel clock is to be divided by three, four, five, or eight to generate the LDA and LDB signals. LDA is also divided by two and four to generate the LD/2 and LD/4 signals, respectively.

ENABLE (S) is internally synchronized to LDA and may be used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be a logical zero.

ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the state they were when the ENABLE (A) input went to a logical zero.

Note that both ENABLE (A) and ENABLE (S) should not be a logical zero simultaneously. If this occurs, synchronous control of LDC and LDD, via ENABLE (S), is not guaranteed.

While both ENABLE (S) and ENABLE (A) are a logical one, LDC and LDD will be free-running and in phase with LDA and LDB. This architecture allows the shift registers of the video DRAMs to be optionally non-clocked during the retrace intervals. Figure 1 illustrates the ENABLE implementation within the Bt438, while Figure 2 shows the load output timing.

The RESET* input is designed to enable the Bt438 to set the pipeline delay of the RAMDACs to a specified number of clock cycles (the exact number is dependent on the RAMDAC). Following the first rising edge of LD/4 after the rising edge of RESET*, the CLOCK and CLOCK* outputs are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are restarted. Figure 3 shows the operation of the RESET* input.

The Bt438 also generates a 1.2 V (typical) voltage reference, which may be used to drive the VREF input of up to four RAMDACs.

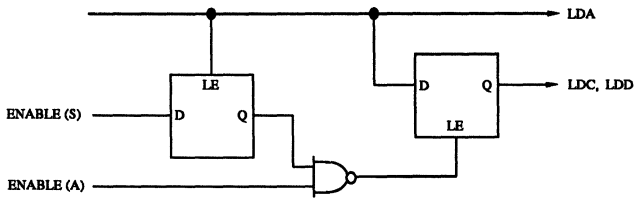


Figure 1. ENABLE Control Implementation.

Circuit Description (continued)

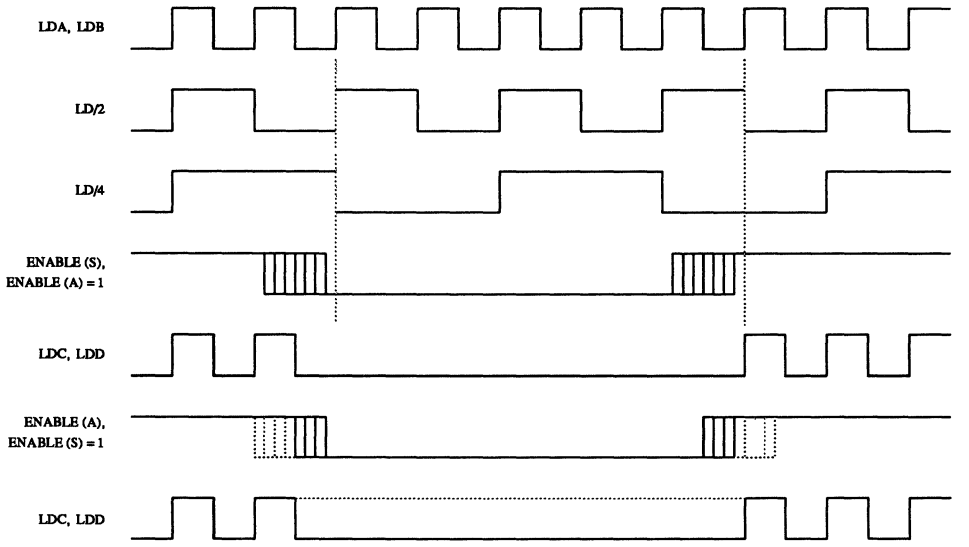


Figure 2. Load Output Timing.

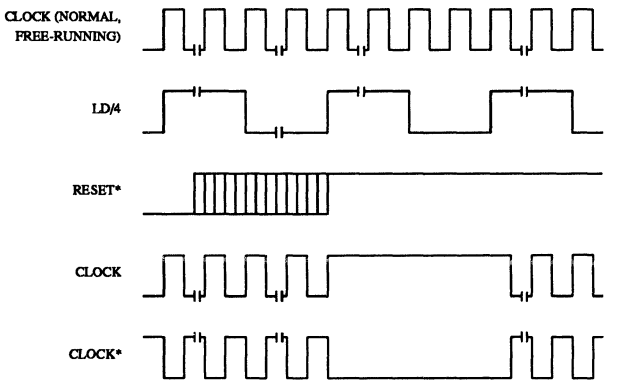


Figure 3. RESET Timing.*

Pin Descriptions

Pin Name	Description
VREF	Voltage reference output. This output provides a 1.2 V (typical) reference, and may be used to drive the VREF input of up to four RAMDACs.
OSC, OSC*	Differential ECL oscillator inputs. These inputs are designed to interface to a 10KH ECL crystal oscillator operating from a single +5 V supply.
CLOCK, CLOCK*	Differential clock outputs. These outputs connect directly to the CLOCK and CLOCK* inputs of the RAMDAC. The clock rate is equal to the OSC rate, and they are capable of driving up to four RAMDACs directly. The output levels are equivalent to 10KH ECL logic operating from a single +5 V supply.
DIV0, DIV1	Divide control inputs (TTL compatible). These inputs specify the division factor (3, 4, 5, or 8) for the generation of the LDA and LDB signals, as specified in below:

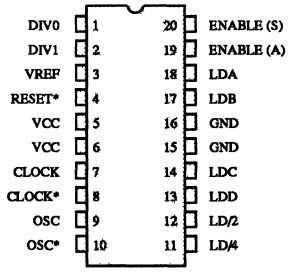
DIV1	DIV0	Division Factor	Clock Cycles Low	Clock Cycles High
0	0	+3	1	2
0	1	+4	2	2
1	0	+5	2	3
1	1	+8	4	4

LDA, LDB	Load outputs (TTL compatible). LDA and LDB are generated by dividing CLOCK by three, four, five, or eight as determined by the DIV0 and DIV1 inputs. Each output may drive up to 20 video DRAMs without external buffering.
LD/2	Load output (TTL compatible). LD/2 is generated by dividing LDA by two. This output may drive up to 20 video DRAMs without external buffering.
LD/4	Load output (TTL compatible). LD/4 is generated by dividing LDA by four. This output may drive up to 20 video DRAMs without external buffering.
LDC, LDD	Load outputs (TTL compatible). When both ENABLE inputs are a logical one, these outputs have the same timing as the LDA and LDB outputs. Each output may drive up to 20 video DRAMs without external buffering.
ENABLE (S)	Synchronous load enable control input (TTL compatible). ENABLE (S) is internally synchronized to LDA and is used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be a logical zero. While both ENABLE (A) and ENABLE (S) are a logical one, LDC and LDD are free-running and in phase with the LDA and LDB outputs.
ENABLE (A)	Asynchronous load enable control input (TTL compatible). ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the state they were when the ENABLE (A) input went to a logical zero. While both ENABLE (A) and ENABLE (S) are a logical one, LDC and LDD are free-running and in phase with the LDA and LDB outputs. Care should be taken to avoid glitches on this asynchronous input.

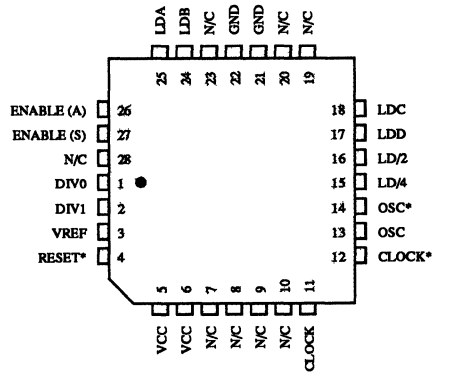
Pin Descriptions (continued)

Pin Name	Description
RESET*	Reset control input (TTL compatible). Following the first rising edge of LD/4 after the rising edge of RESET*, CLOCK and CLOCK* are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are set to be free-running. Care must be taken to avoid glitches on this edge-triggered input.
VCC	Device power. All VCC pins must be connected.
GND	Device ground. All GND pins must be connected.

20-pin DIP Package



28-pin Plastic J-Lead (PLCC) Package



Note: N/C pins may be left floating without affecting the performance of the Bt438.

Application Information

Interfacing to the RAMDAC

Figure 4 illustrates interfacing the Bt438 to the RAMDAC when using a differential crystal oscillator. The Bt438 should be located as close as possible to the RAMDAC. The termination resistors for the OSC and OSC* inputs should be located as close as possible to the Bt438.

Termination resistors are also required on the CLOCK and CLOCK* lines, located as close as possible to the RAMDAC.

Figure 5 illustrates interfacing to a single-ended crystal oscillator, while Figure 6 shows interfacing to a TTL clock for applications less than 75 MHz.

The Bt438 may drive the CLOCK and CLOCK* inputs of up to four RAMDACs if they are located as close as possible to each other. Only one set of 220/330 termination resistors should be used, and these positioned at the RAMDAC furthest away from the Bt438.

Due to the inability to insure proper synchronization between Bt438s, multiple devices should not be used in applications where multiple RAMDACs drive the same monitor.

A 1 kΩ (typical) resistor must be used to isolate the VREF output of the Bt438 from the VREF input of the RAMDAC. This isolates noise from the Bt438 voltage reference from being coupled onto the RAMDAC VREF pin. The VREF input of the RAMDAC must still have a decoupling capacitor to VAA, as specified in the data sheet.

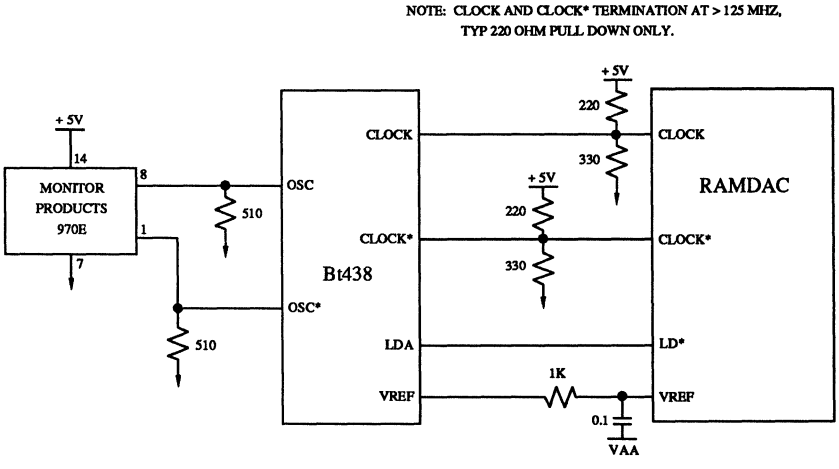


Figure 4. Interfacing to a Differential Crystal Oscillator.

Application Information (continued)

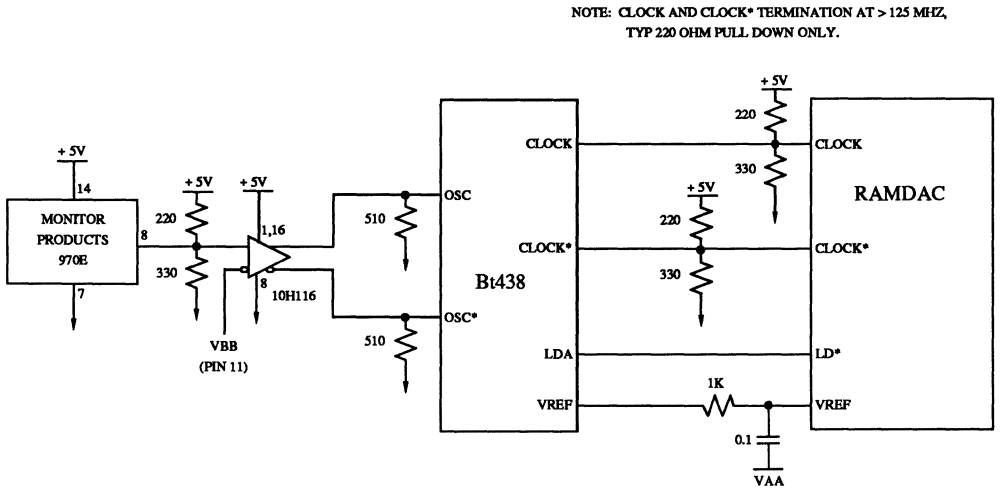


Figure 5. Interfacing to a Single-Ended Crystal Oscillator.

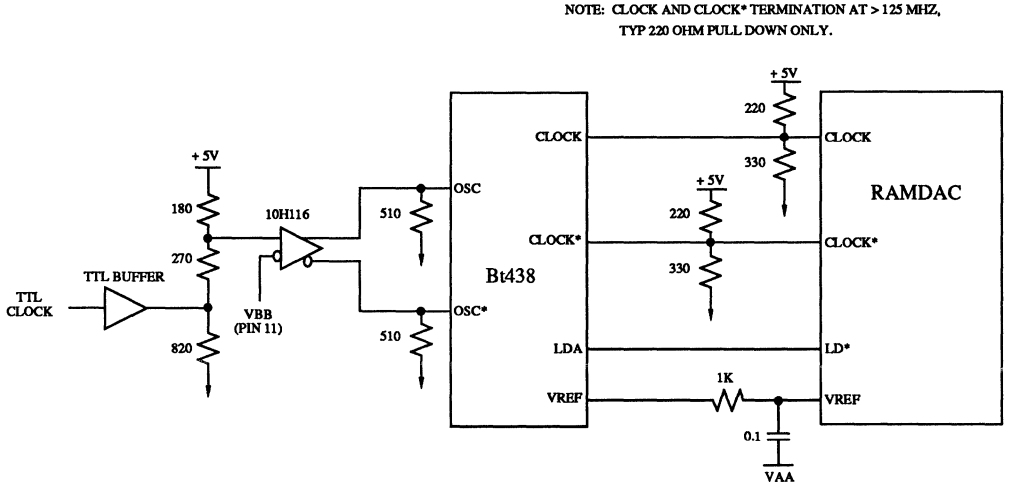


Figure 6. Interfacing to a TTL Clock.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
OSC/OSC* Duty Cycle		40			%

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on any Pin		GND–0.5		VCC + 0.5	Volts
CLOCK, CLOCK* Output Current				30	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C
Air Flow		0			l.f.p.m.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Inputs					
Input High Voltage (other pins)	VIH	2.0		VCC + 0.5	Volts
DIV0, DIV1		2.2		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			10	µA
Input Low Current (Vin = 0.4 V)	IIL			–0.7	mA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4		pF
ECL Inputs (at 25° C.)					
Input High Voltage	VIH	VCC–1.1		VCC–0.8	Volts
Input Low Voltage	VIL	GND–0.5		VCC–1.5	Volts
Input High Current (Vin = 4.0 V)	IIH			15	µA
Input Low Current (Vin = 0.4 V)	IIL			15	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CIN		4		pF
Load Outputs					
Output High Voltage (IOH =–2 mA)	VOH	2.4			Volts
Output Low Voltage (IOL = 20 mA)	VOL			0.8	Volts
Output Capacitance			10		pF
Clock Outputs (at 25° C)					
Differential Output Voltage	ΔVOUT	.6			Volts
Output Capacitance	COUT		7		pF
Voltage Reference					
Output Voltage (Bt438 Rev. C)*	VREF	1.12	1.2	1.27	Volts
Output Current	IREF		100		µA
VCC Supply Current**	ICC		65	85	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." CLOCK and CLOCK* have 50 Ω to VCC–2 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*RSET of the RAMDAC should be adjusted due to the output voltage of the Bt438 Rev. C being lower than the recommended VREF for the RAMDAC. IOG (mA) = $\frac{11294 \text{ VREF}}{\text{RSET}}$, IOG (typ) = 26.7 mA.

**Measured without 50 Ω to VCC–2 V on CLOCK and CLOCK*.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
OSC, OSC* Clock Rate	Fmax			250	MHz
LDA Output Delay (note 1)	1		4	10	ns
LDA, LDB Pulse Width Low (note 3)		5			ns
LDA to LDB Output Skew (note 2)		–2.0	0	2.0	ns
LDA to LDC Output Skew (note 2)		–1.0	1.5	4.0	ns
LDA to LD/2 Output Skew (note 2)		0	1.5	5.0	ns
LDA to LD/4 Output Skew (note 2)		0	1.5	6.0	ns
LDC to LDD Output Skew (note 2)		–2.0	0	2.0	ns
RESET* Active Low Time	2	15			ns
RESET* Setup Time	3	12			ns
ENABLE (S) Setup Time	4	12			ns
ENABLE (S) Hold Time	5	–2			ns
ENABLE (A) Setup Time	6	12			ns
ENABLE (A) Hold Time	7	–2			ns

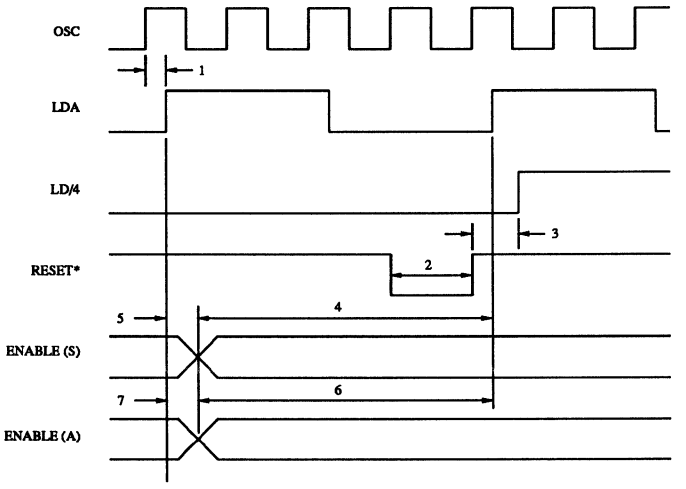
Test conditions (unless otherwise specified): "Recommended Operating Conditions". CLOCK and CLOCK* have 50 Ω to VCC–2 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between 10% and 90% points. ECL input values are 3.2–4.2 V, with input rise/fall times ≤ 1 ns, measured between 20% and 80% points. Timing reference points at 50% for inputs and outputs. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note 1: Output load = 50 pF.
Note 2: LD outputs equally loaded with 50 pF. Unequal loading may result in additional output skew.
Note 3: LD outputs not used in +3 over 200 MHz.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt438KC	20-pin 0.3" CERDIP	0° to +70° C
Bt438KPJ	28-pin Plastic J-Lead	0° to +70° C

Timing Waveforms



Input/Output Timing.

Revision History

Datasheet Revision	*Change from Previous Revision*
H	Thermal equilibrium notes added to Recommended Operating Conditions and DC Characteristics.
I	Rev. B silicon voltage reference limits changed.
J	Rev. C silicon voltage reference limits changed.
K	Upgraded datasheet status to Final. Added DIV0 and DIV1 to DC Characteristics.

Device Revision	
C	Changed VREF limits.