RadiSys R380 Core Logic ASIC
BIOS Adaptation
Implementation Notes

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Notation Conventions

Two hexadecimal numbering conventions are utilized in this document. Hex numbers are expressed as either 0*nn*h or 0x*nn* where *nn* represents a hexadecimal number of arbitrary length. In addition, groups of hex digits which are larger than four digits in length are separated with an underscore for readability (example: 0A_0000h).

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1. Introduction

1.1. Document Scope and Intended Audience

This document describes the software and general architectural requirements of a BIOS Chipset adaptation of the RadiSys R380 core logic ASIC. The scope of this document is to define the software requirements encompassing the necessary BIOS software modification or generation in order to support the RadiSys R380 ASIC.

1.2. Overview

Chapter 1 of this document introduces the BIOS Adaptation for the RadiSys R380 Core Logic ASIC, whose software requirements are described in this document. Terms that may warrant a definition are introduced in Chapter 1.4.

Chapter 2 examines the Chipset-specific component of the BIOS and the tasks within the component in greater detail.

With a thorough introduction to the core-logic related components of the BIOS, an overview of the core logic and processor elements that will be supported in the BIOS is given in Chapter 3. The RadiSys R380 Core Logic ASIC and the Intel386EX Microprocessor are presented here from the viewpoint of the BIOS programmer to provide a more concrete picture of what hardware capabilities will need to be supported by this Chipset adaptation.

Chapter 4 builds on the information introduced in Chapter 3 with regard to the Chipset adaptation. Specific tasks that need to be accomplished in order to provide the Chipset adaptation to the BIOS vendor for deployment are outlined.

The two appendices occupy Chapter 6. Appendix A contains a one page synopsis of the functional units of both the Radisys R380 Core Logic ASIC and the Intel386EX Microprocessor. Appendix

Chapter 7 provides the reader with a list of cited references that were used in the composition of this document.

1.3. Concept

To better support the embedded PC architecture, the Intel386EX Microprocessor, and to fill the need for long lifecycle core logic components required for embedded PCs, RadiSys has developed the R380. The R380 is a single-chip ISA core logic ASIC. The major objectives of the R380 are flexibility, ease of use, and low system cost. The R380 incorporates directly the features needed in most or all embedded PC designs, and provides simple, low-cost, “glueless” interfaces to additional components to support added functionality, such as SVGA or PC-CARD Controllers.

More complete information on the R380 ASIC can be found in the *RadiSys R380 Product Development Specification*. Section 3.3.1 of this document contains a top-level, BIOS Programmer-oriented description of the R380.

1.4. Terms and Acronyms Defined

The following table contains selected terms and acronyms utilized in this document with a brief definition and section reference.

Table 1-1: Terms and Acronyms Defined

Term or Acronym	Definition	See Section
FBD	Flash Boot Device: A Flash EEPROM that occupies the address space on the Local bus. This Flash EEPROM contains Video and Main BIOS code as	

	well as BIOS extensions.	
RFA	Resident Flash Array: One or more Flash EEPROM devices that are typically used as a mass storage device.	

2. Chipset Firmware Overview

2.1. 386EX Processor Support

While this chapter deals with the tasks associated with the chipset component specifically, the 386EX processor presents a special case in that it is a highly integrated processor with many on-board peripherals and functional units that perform core system support. This is a point of distinction between x86 architecture processors that are targeted for desktop applications, such as the Intel486DX and those targeted for embedded applications, such as the Intel386EX. In a typical desktop BIOS implementation, the core system support functions, such as DRAM Refresh, would be handled primarily by a chipset, and thus, the support functions to handle initialization and control of these functional units resides in the chipset component.

2.2. R380 DRAM Configuration Considerations

The R380 DRAM Controller will be discussed in more detail in chapter 4, but it is worth examining how memory is configured using the R380 at this point because modifications to the DRAM Autosizing routines are required to support the R380.

The R380 supports up to two independent banks of DRAM. Each bank can consist of two “components.” If two components are present within a single bank, however, they must both be the same size. Thus the DRAM Autosizing routine must take this into account and size the first component of a bank if it is present. After the first component is sized, the second component can be turned on in the chipset and the presence of this memory checked for. The “second component” bit would then be set or cleared accordingly on a per-bank basis.

2.3. Extended Data Out/Fast Page Mode DRAM Determination

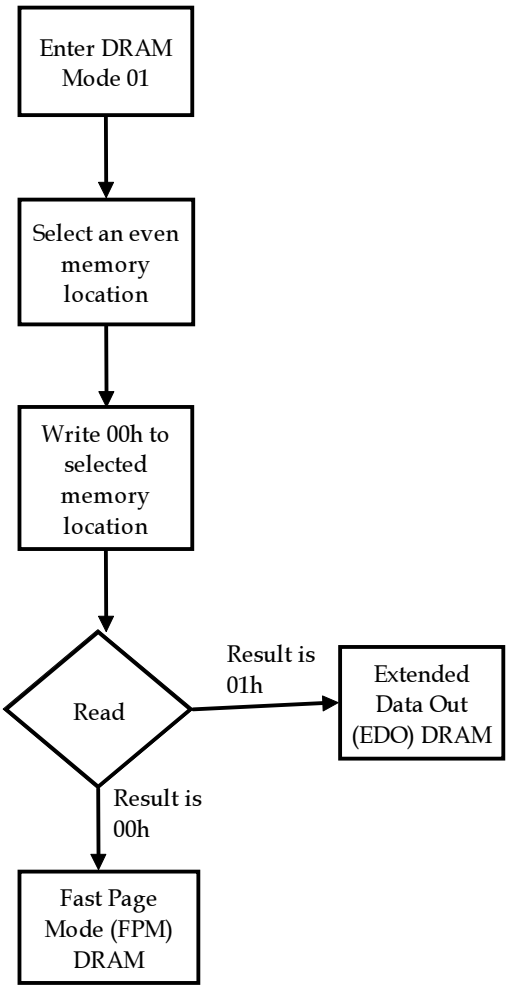

Figure 2-1: EDO/FPM Detection Algorithm

The R380 has the capability to allow the BIOS to determine whether Fast Page Mode (FPM) or Extended Data Out (EDO) memory is present. The EDO/FPM determination routine must run out of ROM because DRAM behavior is not deterministic after the testing has begun. The determination routine must also run before the DRAM is sized. The algorithm utilized in DRAM type detection operates on each of the R380's DRAM banks separately.

The algorithm is illustrated in Figure 2-1. It utilizes a special memory access mode of the R380, which is used for the purpose of detecting EDO memory. This mode is referred to in the above diagram as "Mode 01." The "01" refers to the value which is programmed into the MODE field of the DRAM Timing Register of the R380. Once this mode is entered, an even memory location is cleared by the detection routine. The same location is then read back. If EDO memory is present, the special access mechanism will cause the least significant data bit of the memory location to remain a logic "1" despite the fact it was written as a logic "0." Hence a 01h will be read back, and it can be concluded that EDO memory is present. If the same value, that is 00h, is read back, then it may be concluded that EDO memory is not present, and the R380 is to be configured for Fast Page Mode (FPM) DRAM.

2.4. Chip Select Unit Programming

Both the R380 and the 386EX contain Chip Select Units to allow the selection of various peripherals within the X-Bus (ISA Bus) address space. Usage of either set of Chip Select Units is based on the peripherals that are designed into a R380-based system.

The R380 also provides functionality for relocating the System BIOS and Video BIOS by specifying where in the address space above 1MB the FBD chip select is asserted, and this is configured during the Early POST phase of BIOS initialization.

2.5. BIOS Shadowing Control

A significant capacity in the R380 is the ability to shadow BIOS and Option ROM code. Shadowing involves, fundamentally, the relocation of BIOS and Option ROM code from ISA and Local Bus Resident Memory Spaces to

the Upper Memory Blocks present in DRAM above A_0000h. This enables this code to run out of DRAM rather than EEPROM or Flash, which results in a significant execution speed improvement

3. Core Logic and Processor Overview

3.1. Introduction

The functional units within the RadiSys R380 Core Logic Support ASIC and the Intel 386EX Microprocessor that provide support for the software features outlined above, are presented here from the viewpoint of the BIOS Software Engineer to serve as a framework for the BIOS customization and chipset adaptation work to be done.

The next chapter then builds on this information and discusses the specific tasks required to support the R380 Core Logic ASIC and the 386EX Processor in the chipset component.

Both the RadiSys R380 ASIC and the Intel 386EX Microprocessor are highly integrated and optimized for embedded applications. Each chip includes a number of functional units, each performing a core system support function, such as DRAM Refresh Control, or providing a peripheral device, such as a Chip Select Unit.

In Appendix A, a summary of the functional units between the R380 Core Logic and the 386EX Processor is presented in tabular format. Two noteworthy aspects of the table are that it is a summary of the physical hardware, and that some functional units are duplicated and others are replicated on both elements. For example, both the R380 and the 386EX have DRAM Refresh Controllers. Whereas only one of these resources could be utilized in a system, resources that are replicated on both elements, such as Chip Select Units, can be used concurrently.

Functional Units are also shown by type in the table. The functional units of the 386EX that are peripherals can be classified by whether the peripheral is PC-compatible or is optimized for embedded applications. In the same way, the R380 has peripherals that are compatible with the PC architecture, and other functional units that provide core system functionality, such as DRAM Refresh Control and Power Management Support. We begin with the Intel 386EX Processor.

3.2. Intel 386EX Embedded Microprocessor

3.2.1. Functional Unit Overview

The feature set of the 386EX can be thought of in terms of two groups of features: those that are standard PC-compatible peripherals (compatibility level is shown in description field of the Functional Unit Table in Appendix A), and peripherals that are optimized for embedded applications.

In the arena of PC-compatible peripherals, the 386EX provides two interrupt controllers, which are operated in a master/slave fashion. Programmable Interval Timers are also present, and can be used as an interrupt source. Lastly, two UARTs are present that are located at the standard addresses of 03F8h and 02F8h for COM1 and COM2 respectively.

In addition to the PC-compatible peripherals, the 386EX contains a number of functional units that both support embedded applications and provide core system support functions.

3.2.2. Expanded IO Address Space

The 386EX processor's I/O address space is 64 Kbytes. Included in this region are the 1024 addresses from 0h to 3FFh which comprise the "standard" ISA IO Space, where most core peripherals, such as the DMA controller and Real-time Clock normally reside in a PC-Compatible system. In the case of the 386EX, these peripherals reside physically in what is called the Expanded IO address space located at F000h - F8FFh in the EX's IO space. A control bit allows the peripherals to be re-mapped down into the "standard" ISA IO Space.

A 16-bit control register called REMAPCFG, occupying IO locations 022h and 023h performs two functions: first, it enables the expanded IO Space. If expanded IO space is not enabled, only the 10 least significant address lines are decoded, limiting operations to the first 1024 locations. Once enabled, all

65536 locations in the expanded IO space can be accessed. Secondly, the REMAPCFG register controls whether some, all, or none of the integrated peripherals are re-mapped from the expanded IO space down into the “standard” ISA IO Space. This same mechanism can allow the peripherals to remain “hidden” in expanded IO space, by not remapping them to the standard low 1024 ISA IO Space locations. These peripherals include the two asynchronous serial ports, the two 8259A-compatible PICs, the DMA Controller, and the On-chip Timer unit.

3.2.3. Intel 386EX Register Groups

In this section, the register groups of the 386EX are examined from the viewpoint of a BIOS Software Engineer.

3.2.3.1. Pin Configuration Registers

A feature of the 386EX that is helpful in implementing embedded designs is pin multiplexing. Pin multiplexing allows logical binding of internal functional units or registered General Purpose IO (GPIO) bits to physical input/output pins on the 386EX. Pin Configuration registers specify which peripheral or registered bit is logically bound to the pin. This feature affords increased flexibility as the GPIO pins can be configured into a system as needed, otherwise, the default peripheral signal binding is utilized.

Three registers are utilized to control the binding of the multiplexed pins: P1CFG, P2CFG, and P3CFG. These registers are discussed in detail from a BIOS implementation perspective in section 5.2.1. Signal bindings are very application specific, based on the need for GPIO signals. Thus these registers would be modified in an application-specific manner.

A fourth register, called PINCFG, allows controls the multiplexing of different peripheral component signals onto common pins. The PINCFG register is discussed in further detail in section 5.2.2.4.

3.2.3.2. A20GATE and Fast CPU Reset

The A20GATE and Fast CPU Reset Register, PORT92, resides at IO address 092h for PC-compatibility as well as the extended IO address 0F092h in the expanded IO Space. This register allows the A20 line to be enabled or forced to zero. The PORT92 Register can also perform a Fast CPU Reset by resetting the processor core in a synchronized fashion without resetting any of the peripherals.

The A20GATE bit of the PORT92 Register is bit 0. If this bit is set, then address line A20 is forced to 0. This generates address wraparound above 0F_FFFFh, which is utilized by some legacy applications. If this bit is clear, the A20 value generated by the Address Unit of the 386EX is left unchanged.

Fast CPU Reset may be engaged by setting bit 1 of the PORT 92 register.

3.2.3.3. Refresh Control Unit

The Refresh Control Unit of the 386EX provides a functional unit to generate periodic refresh requests and refresh addresses. The Refresh Control Unit includes an interval timer unit, a control unit, and an address generation unit. The Refresh Control Unit is controlled by four registers in the 386EX. To accomplish this, bit 15 in the Refresh Control (RFSCON) Register at address F4A4h must be zero.

In this BIOS implementation, the DRAM Refresh Control Unit of the R380 will be utilized in lieu of the Refresh Unit on the 386EX.

3.2.3.4. Watchdog Timer Unit

The watchdog timer is a general-purpose 32-bit timer that can be used as a software watchdog timer, bus monitor, or a general-purpose timer. The watchdog defaults to a general-purpose timer mode after reset. At reset, the timer, or down-counter begins decrementing once every clock cycle from the initial value of 0000_FFFFh, which means the timer will timeout after 65536 clock cycles. Before this timeout, the values of the two count registers, WDTCNTH and WDTCNTL, can be read at any time to determine the current number of clock ticks left on the timer. This can also be useful for calculating the elapsed time between two events.

3.2.3.5.Clock Generation and Power Management Unit

The Clock and Power Management Unit in the 386EX provides the processor core and integrated peripherals with uniform, non-overlapping clock signals, and provides features to facilitate the control of clock signals for power conservation.

3.2.3.5.1. Clock Generation Logic

An external oscillator provides the 386EX with an input signal to CLK2. The 386EX Clock and Power Management Unit takes this clock and generates a separate clock for the processor core and the internal peripherals. This clock is derived by dividing CLK2 and generating a 50% duty cycle clock signal. This signal is then divided by 2 again to generate a clock input, SERCLK, which is used by the baud-rate generators of the asynchronous and synchronous Serial IO units.

CLK2 is also utilized by the Clock and Power Management Unit to generate a pre-scaled clock (PSCLK) input for the timer/counter and synchronous serial IO units. PSCLK frequency can range from (CLK2/4) to (CLK2/1026). The prescaler value is set in the CLKPRS register, which resides only in the expanded IO space of the 386EX at address F804h. Bits [8:0] in this register specify the divisor value less 2. The Clock and Power Management Unit is currently initialized to expect a CLK2 frequency of 50 MHz and provide a prescaled clock output of 1.190 MHz.

3.2.3.5.2. Power Management Control

The second register in the Clock and Power Management Unit which governs core operation with regard to clock signals is the PWRCON register located at expanded IO space location F800h. This register specifies what power conservation mode the 386EX is to enter upon execution of a HALT instruction. The PWRCON Register is currently initialized to cause a normal halt when the HALT instruction is executed, and the 386EX remains in active mode.

3.2.3.6.Device Configuration Registers

Device Configuration Registers control the Pin Multiplexing functionality of the 386EX in a manner similar to the Pin Configuration Registers described above in section 3.2.3.1. Pin Configuration Registers allow three sets of 8 registered bits in the 386EX to be bound to physical pins on the EX and utilized as GPIO signals. Otherwise the default control signals, typically from internal peripherals are bound to the physical pins.

With the Device Configuration Registers, there is one register allocated to a peripheral that controls different physical pin bindings associated with that peripheral. These registers are DMACFG (DMA Controller), TMRCFG(Timer/Counter Unit), INTCFG (Interrupt Control Unit), and SIOCFG.

3.3. RadiSys R380 Core Logic ASIC

To the group of peripherals on the 386EX that support the standard PC architecture, the RadiSys R380 ASIC adds a Real-time Clock with battery-backed CMOS memory, a 8042-compatible Keyboard Controller, and PS/2 Mouse Controller. The R380 Supports core system functions through a DRAM Refresh Controller, Power Management

Support, and a ROM/Flash Controller. The R380 also augments the embedded features of the 386EX by adding four more programmable chip select units, and 16 additional General Purpose IO (GPIO) bits. In Appendix A, the Functional Units of each element are presented in a tabular format for easy reference.

3.3.1. RadiSys R380 Register Groups

The R380 Register set provides control for core system support functions, such as BIOS ROM Decode and Control, Shadowing Operation, General Purpose I/O pin control, SMM (System Management Mode) function control, Chip Select Unit control, Clock/Reset Control, and DRAM Configuration. The register set is described below.

3.3.1.1. Index/Data and PC-Compatible Registers

The R380 is accessed in an index/data fashion through an index and data register at addresses 024h and 026h respectively. PC-Compatible Keyboard data and control registers are provided at the standard addresses: 060h for the data register and 064h for the control register. The PortB (Speaker) port is provided at address 061h. and the CMOS memory is accessed in an index/data fashion also with index and data registers at 070h and 071h respectively.

3.3.1.2. ID Register

The Upper 12 bits of the ID Register are set to 380h on power up. The lower order nibble can be utilized by the BIOS to indicate revision information. These bits are reset to `0h` upon power-up of the chip.

3.3.1.3. Powerup Options

This is a read-only register that provides access to the latched power-up configuration bits MA[10:0]. This register should not be initialized or written to by the BIOS.

3.3.1.4. BIOS Control Register

This register is used to control access to the Flash Boot Device. It is used to specify when the CE_BIOS chip select is asserted and thus where the FBD is chip-selected in the correct ISA Memory region. Also specified are the number of wait states inserted into a FBD read access. Advanced write-enable capability for use with boot block Flash is also included.

3.3.1.5. Shadow Control Registers

The Shadow Control Registers are two registers that control access to both the ISA Memory Space and the Upper Memory Blocks above A_0000h in DRAM. This allows the BIOS to copy code from devices residing in the ISA Memory space, such as a Flash EEPROM and store the code in DRAM. Four types of access are available, and thus each region requires two bits. The four types of access are detailed in the table below.

Table 3-1: R380 Shadow Register Encoding

R380 Shadow Register Encoding	Operational Characteristics
00	Read ISA Bus / Write ISA Bus
01	Read ISA Bus / Write DRAM
10	Read DRAM / Write generates no ISA Bus or DRAM cycles (read-only DRAM)
11	Read DRAM / Write DRAM

Regions in the vary in the degree of granularity that is available for each page. The A and B pages have the least granularity, while the C, D, and E pages have the most granularity. A summary of the granularity that is available when shadowing upper memory regions is presented in Table 3-2 below.

Table 3-2: R380 Shadow Region Granularity

Shadow DRAM Region Start Address	Shadow Control Register Granularity (Kbytes)	Shadowable Regions	Comments
A_0000h	64	1	A Page
B_0000h	64	1	B Page
C_0000h	16	4	C Page - Video BIOS (by Convention)
D_0000h	16	4	D Page
E_0000h	16	4	E Page - Alternate Video BIOS / Extended Main BIOS
F_0000h	32	2	F Page - System BIOS

The power-on default for all regions is shaded in the table above, Read ISA Bus / Write ISA Bus, which allows access to the FBD upon power-on.

3.3.1.6. Digital IO (DIO) Registers

These Registers provide control and data for general purpose I/O pins on the R380. All DIO Pins are configured as inputs at Power-on because the DIO Direction Register is cleared. In order for DIO Pins to drive the corresponding external pin, the appropriate bit in the DIO Direction register must be set to a 1.

If the pins are designated as inputs, then the sense of the pins may be determined by reading the DIO Input Register.

The external pin configuration of the R380 is determined by the DIO Configuration Register. If a 1 is set in the bit corresponding to the DIO Pin, then the pin is a General Purpose I/O pin. The behavior of this register at Power-on is determined by three bootstrap pins: MA5, MA6, and MA7. For more information, please consult the *R380 Product Development Specification*.

No additional BIOS-level support is required other than that provided in the Early POST and CMOS Enhanced chipset configuration.

3.3.2. System Management Mode Support

System Management Mode (SMM) Support Registers on the R380 consist of a SMI Timer Control Register and a SMI Control/Status Register. The Timer Control Register controls a 12-bit timer. Specifically, the least significant 12 bits of the SMI Timer Control Register act as a Idle Timer latch. When written to, the Idle Timer latch value is set and written through to the 12-bit timer. This functionality is useful for implementing Power Management functionality which will be discussed in greater depth in a future document.

It is worth noting that the R380 has a single idle timer, whereas some chipsets with Power Management capability have multiple timers (i.e. the Pico Power Sequoia chipset). Multiple timers add to the complexity of Power Management firmware, but allow a single timer to be devoted to each Power-Managed resource. A single timer must be managed with firmware. When there are multiple Power-Managed devices, each will have a “software” timer, while the hardware timer will be utilized in a multiplexed fashion.

3.3.3. Chip Select Units

The R380 includes four Programmable Chip Selects (PCSs). Each PCS has a corresponding Compare/Mask register. The lower order 10 bits of each Compare/Mask register are compared based on an operational mode specified in the Compare/Mask register as well. If the comparison is true, based on the constraints specified in the MODE field of the register, then the corresponding chip select will be asserted.

BIOS-level support is dependent upon what peripherals are present on the ISA Bus, and if the peripherals present have or do not have internal address decoding capability. This is very implementation specific, and is not discussed in much detail here.

3.3.4. DRAM Controller

The DRAM Refresh Controller on the R380 is controlled by two registers -- the DRAM Control Register and the DRAM Timing Register. Fundamentally, The DRAM Control Register specifies on a per-bank basis the size of the DRAM that is contained in either of the two banks that the R380 supports. The DRAM Control Register also contains extra bits for performing address remapping of the DRAM, which is related to the use of DRAM Flash Memory.

The DRAM Timing Register allows configuration of many DRAM timing parameters including RAS and CAS assertion widths, RAS to CAS delay, RAS & CAS precharge time, and also refresh parameters of both DRAM and the ISA Bus. Selected parameters in the DRAM Timing Control will be put under CMOS Setup Control to allow the system user to configure the system to accept a wide range of DRAM components.

The DRAM Controller also features a mechanism that allows the BIOS to determine if Fast Page Mode (FPM) or Extended Data Out (EDO) memory is present in either of the R380's two banks. This is accomplished by the use of an extended ISA Bus read cycle. Implementation details for the use of this feature to distinguish between FPM and EDO DRAM is given in section 2.3.

As alluded to earlier, in section 2.2, The R380 supports two banks of DRAM, and these banks can be further specified as one or two components within a bank.

4. Chipset Firmware Implementation

4.1. Register Setup

The Chipset initialization information is summarized in Table 4-3 below. The Register Name/Function is taken from the R380 Product Specification. The register index is given next, followed by the Power-On reset value of the particular register. The next two fields describe how the particular register will be written when initialized by the Early POST chipset initialization routine. The first of the two fields, "Register Value" is combined with the "Register Mask" value. Only the bits whose corresponding mask bit in the Register Mask is 1 will be changed to the value specified in the "Register Value" field. Registers where either the Register Value or the Register Mask field is blank, are not written by as part of the Early POST chipset initialization. The "Read Modify Write" field specifies whether a register is modified by a write mechanism (W) or Read/Modify/Write (RMW) mechanism. All numeric values below are in hexadecimal notation.

Table 4-3: R380 Register Initialization Synopsis

R380 Register Name/Function	Register Index	Power-On Reset Value	Register Value	Register Mask	Notes
Core Logic Revision / BIOS Revision	000	3800		0000	Not modified
Powerup Options Register	001	0000		0000	Not modified
BIOS Control Register	002	70F0		0000	Not modified
Shadow 1 Register	003	0000	0000	FFFF	
Shadow 2 Register	004	0000	0000	FFFF	
DIO Data Output Register	005	000X	0000	FFFF	
DIO Data Input Register	006	N/A		0000	Not modified
DIO Data Direction Register	007	0000	0000	FFFF	
DIO Configuration Register	008	0000		0000	Not modified
DO Configuration Register	009	0000		0000	Not modified
Output Configuration Register	00A	0000	0000	001F	
SMI Timer Control Register	00B	000X	0000	8FFF	
SMI Control / Status Register	00C	4000	0000	01FF	
Chip Select 0 Compare/Mask Register	00D	0000	81F3	FFFF	PCS0: PowerOf2 Select on range [1F0..1F7h], 8-bit, C15=0
Chip Select 1 Compare/Mask Register	00E	0000	83F6	FFFF	PCS1: PowerOf2 Select on range [3F6..3F7h], 8-bit, C15=0
Chip Select 2 Compare/Mask Register	00F	0000	0000	FFFF	PCS2: Disabled
Chip Select 3 Compare/Mask Register	010	0000	0000	FFFF	PCS3: Disabled
LED Control Register	011	0010		0000	Not modified
Clock/Reset Control Register	012	0002	Table 4-4	01FF	See Table 4-4
DRAM Control Register	013	0001	000B	03FF	
DRAM Timing Register	014	0BFF	0BFF	FFFF	

The values for Register 012h varies with the CLK2 value which is input to the R380. The values of Register 012h which correspond to particular values of CLK2 are shown below in Table 4-4.

Table 4-4: R380 Register 12: CLK2 Value Variances

CLK2 Speed (MHz)	386EX Clock Speed (MHz)	ISA Bus Clock Divider	ISA Bus Speed (MHz)	Register 12 Value	Notes

50	25	6	8.333	0006h	Current B-Step 386EX
66	33	8	8.250	0002h	C-Step 386EX Silicon supports 33 MHz
40	20	6	6.667	0006h	ISA Bus speed below 8 MHz lower limit
32	16	4	8.000	000Ah	

4.2. DRAM Bank Configuration

The R380 can control two banks of DRAM. Within each bank of DRAM, two modules with independently controllable RAS and CAS signals can be resident. Shown below are the different memory combinations that are possible in a single bank in the R380. The 4-bit configuration value given below in the table is used on a per-bank basis for each bank in the DRAM Control Register.

Table 4-5: R380 Memory Bank Configuraiton Description

R380 Bank Size Value	Memory Form Factor Description	Number of Modules Per Bank	Bank Memory Size (Kbytes)
00h	No SIMMs in bank	-	0
01h	256K x 16 SIMM	1	512
02h	512K x 16 SIMM	1	1024
09h	256K x 16 SIMM	2	1024
03h	1024K x 16 SIMM	1	2048
0Ah	512K x 16 SIMM	2	2048
04h	2048K x 16 SIMM	1	4096
0Bh	1024K x 16 SIMM	2	4096
05h	4096K x 16 SIMM	1	8192
0Ch	2048K x 16 SIMM	2	8192
06h	8192K x 16 SIMM	1	16384
0Dh	4096K x 16 SIMM	2	16384
07h	16384K x 16 SIMM	1	32768
0Eh	8192K x 16 SIMM	2	32768
0Fh	16384K x 16 SIMM	1	65536

4.3. Shadow Region Setup

Shadow Operation is controlled principally through the Shadow 1 and Shadow 2 Registers. These registers contain 2-bit wide bitfields describing the attributes for each shadowed region. These attributes are shown below in Table 4-6.

Table 4-6: R380 Shadow Region Encoding

R380 Shadow Register Encoding	Operational Characteristics of Shadowing access primitives	Shadow Region Attribute
00	Read ISA Bus / Write ISA Bus	Shadow Region Disable
01	Read ISA Bus / Write DRAM	Shadow Region ISA Copy
10	Read DRAM / Write generates no ISA Bus or DRAM cycles (read-only DRAM)	Shadow Region Read Only
11	Read DRAM / Write DRAM	Shadow Region

		Read Write

Although the R380 supports varying degrees of granularity in the Shadow *n* Registers, Shadow Regions were chosen such that the granularity matched the minimum granularity available in the BIOS Control Register, since that register controls shadowing operations also. Thus eight regions of 32 Kbytes each were chosen. The following table shows register setups for three of the four region attributes given above: Shadow Read Only, Shadow Read/Write, and Shadow Disable.

Table 4-7: R380 Shadowing Register Detail

Shadow Region Start Paragraph	Shadow Region Size (Kbytes)	R380 Register	Shadow Region Read-Only	Shadow Region Read-Write	Shadow Region Disable	R380 Register Mask
C000	32	3 2	00A0 0000	00F0 0000	0000 0001	00F0 0001
C800	32	3 2	0A00 0000	0F00 0000	0000 0002	0F00 0002
D000	32	3 2	A000 0000	F000 0000	0000 0004	F000 0004
D800	32	4 2	000A 0000	000F 0000	0000 0008	000F 0008
E000	32	4 2	00A0 0000	00F0 0000	0000 0010	00F0 0010
E800	32	4 2	0A00 0000	0F00 0000	0000 0020	0F00 0020
F000	32	4 2	2000 0000	3000 0000	0000 0040	3000 0040
F800	32	4 2	8000 0000	C000 0000	0000 0080	C000 0080

5. 386EX Processor Initialization

5.1. 386EX Processor Initialization

Intel386EX Processor initialization is performed in several stages. First, the REMAPCFG register, introduced in section 3.2.2, must be written to allow access to integrated peripherals that are resident in the 386EX expanded IO Space, and the Watchdog Timer is disabled. Normally, the Refresh Control Unit would be started next, so that DRAM can be utilized for the recovery process if necessary, but the R380 DRAM Control Unit will be programmed to perform this task later in the Boot block if needed.

Multiplexed pin configuration and peripheral pin configuration followed by Chipset Unit setup are done next. These operations are described in more detail in section 5.2.1 below. Final initialization tasks include initializing the 386EX Clock and Power Management Unit and checking the operation of the Real-time Clock.

At this point, Boot block initialization will continue with the initialization of the R380. If full Boot block functionality is not present, R380 initialization can be delayed until the normal POST task. Please see the previous chapter for complete details of the initialization of the R380.

5.2. 386EX Processor Configuration Registers

Table 5-1 details the initialization of the 386EX Processor Configuration Registers. The table includes Intel Register Symbols for easy cross reference. The Power-On reset value of each register is given, along with the initial value that is put into the register and the mask used to modify the register.

Table 5-1: 386EX Configuration Register Synopsis

386EX Register Name/Function	Intel Register Pneumonic	386EX Address	Power-On Reset Value	Initial Value	Initial Mask	Description
Address Configuration Register	REMAPCFG	0022	0000	*	*	See Section 5.2.1
Port 92 and Fast CPU Reset	PORT92	F092	00	02	03	Clear PORT92 Reset
GCS0 Low Address	CS0ADL	F400	0000	0000	F9FF	
GCS0 High Address	CS0ADH	F402	0000	0000	03FF	
GCS0 Low Mask	CS0MSKL	F404	0000	0000	FC01	
GCS0 High Mask	CS0MSKH	F406	0000	0000	03FF	
GCS1 Low Address	CS1ADL	F408	0000	0000	F9FF	
GCS1 High Address	CS1ADH	F40A	0000	0000	03FF	
GCS1 Low Mask	CS1MSKL	F40C	0000	0000	FC01	
GCS1 High Mask	CS1MSKH	F40E	0000	0000	03FF	
GCS2 Low Address	CS2ADL	F410	0000	0000	F9FF	
GCS2 High Address	CS2ADH	F412	0000	0000	03FF	
GCS2 Low Mask	CS2MSKL	F414	0000	0000	FC01	
GCS2 High Mask	CS2MSKH	F416	0000	0000	03FF	
GCS3 Low Address	CS3ADL	F418	0000	0000	F9FF	
GCS3 High Address	CS3ADH	F41A	0000	0000	03FF	
GCS3 Low Mask	CS3MSKL	F41C	0000	0000	FC01	
GCS3 High Mask	CS3MSKH	F41E	0000	0000	03FF	
GCS4 Low Address	CS4ADL	F420	0000	0000	F9FF	
GCS4 High Address	CS4ADH	F422	0000	0000	03FF	
GCS4 Low Mask	CS4MSKL	F424	0000	0000	FC01	
GCS4 High Mask	CS4MSKH	F426	0000	0000	03FF	
GCS5 Low Address	CS5ADL	F428	0000	0000	F9FF	
GCS5 High Address	CS5ADH	F42A	0000	0000	03FF	

GCS5 Low Mask	CS5MSKL	F42C	0000	0000	FC01	
GCS5 High Mask	CS5MSKH	F42E	0000	0000	03FF	
GCS6 Low Address	CS6ADL	F430	0000	0000	F9FF	
GCS6 High Address	CS6ADH	F432	0000	0000	03FF	
GCS6 Low Mask	CS6MSKL	F434	0000	0000	FC01	
GCS6 High Mask	CS6MSKH	F436	0000	0000	03FF	
UCS Low Address	UCSADL	F438	FFEF	0302	F9FF	Provide UCS in addition to CE_BIOS on R380 for E/F-Page EEPROM Chip Select
UCS High Address	UCSADH	F43A	FFFF	03F8	03FF	
UCS Low Mask	UCSMSKL	F43C	FFFF	FC01	FC01	
UCS High Mask	UCSMSKH	F43E	FFFF	0007	03FF	
Refresh Base Address Register	RFSBAD	F4A0	0000	0000	0FFF	
Refresh Clock Interval Register	RFSCIR	F4A2	0000	0000	03FF	
Refresh Control Register	RFSCON	F4A4	0000	0000	83FF	
Refresh Address Register	RFSADD	F4A6	00FF	0000	03FF	
WDT Reload High	WDTRLDH	F4C0				Not Modified
WDT Reload Low	WDTRLDL	F4C2				Not Modified
WDT Control High	WDTCNTH	F4C4				Not Modified
WDT Control Low	WDTCNTL	F4C6				Not Modified
WDT Clear	WDTCLR	F4C8				Not Modified
WDT Status	WDTSTATUS	F4CA	00	01	83	Disable Watchdog Unit
Power Control Register	PWRCON	F800	00	00	03	
Clock Prescale Register	CLKPRS	F804	0000	0013	01FF	
Port 1 Mode Configuration	P1CFG	F820	00	FF	FF	
Port 2 Mode Configuration	P2CFG	F822	00	F0	FF	
Port 3 Mode Configuration	P3CFG	F824	00	BF	FF	
Pin Configuration	PINCFG	F826	00	27	7F	
DMA Configuration	DMACFG	F830	00	80	FF	
Interrupt Configuration	INTCFG	F832	00	0F	8F	
Timer Configuration	TMRCFG	F834	00	20	BF	
SIO and SSIO Configuration	SIOCFG	F836	00	04	C7	
Port 1 Pin State	P1PIN	F860				Read-Only Register
Port 1 Data Latch	P1LTC	F862	FF	FF	FF	
Port 1 Direction	P1DIR	F864	FF	00	FF	
Port 2 Pin State	P2PIN	F868				Read-Only Register
Port 2 Data Latch	P2LTC	F86A	FF	00	FF	
Port 2 Direction	P2DIR	F86C	FF	0F	FF	
Port 3 Pin State	P3PIN	F870				Read-Only Register
Port 3 Data Latch	P3LTC	F872	FF	40	FF	
Port 3 Direction	P3DIR	F874	FF	40	FF	

5.2.1. Enabling Expanded I/O Space

Expanded I/O Space is enabled by the following consecutive operations on the Address Configuration Register.

1. An 8-bit write of 00h to 23h
2. An 8-bit write of 80h to 22h
3. A 16-bit write of 0080h to 23h

After this series of operations are complete, standard AT peripherals can be accessed at standard ISA addresses.

5.2.2. Pin Configuration Registers

Pin Configuration Registers were first introduced in section 3.2.3.1. Implementation values for the pin configuration registers depend on which registered bits are required to be bound to a physical pin so that they can be used as a GPIO signal. Values for the registers from an example R380/386EX design are discussed in the following sections. Implications of these value choices with respect to the R380 are noted in the right-most column of each Register Detail table.

5.2.2.1. P1CFG Register

The Register Detail table below describes the signal bindings defined by the P1CFG Register. In this configuration, all GPIO bindings are overridden. The two internal SIO (Serial I/O) Units are used in lieu of the GPIO bits in this design.

Table 5-2: 386EX P1CFG Register Detail

P1CFG Bit	Set Signal Binding	Clear Signal Binding	Bit value	Notes
7	HLDA	P1.7	1	
6	HOLD	P1.6	1	
5	LOCK#	P1.5	1	
4	RIO#	P1.4	1	
3	DSR0#	P1.3	1	
2	DTR0#	P1.2	1	
1	RTS0#	P1.1	1	
0	DCD0#	P1.0	1	

5.2.2.2. P2CFG Register

The Register Detail table below describes the signal bindings defined by the P2CFG Register. Many of the chip selects that are generated using the EX Chip Select Unit, are generated by internal address decoding by the R380. This would include peripherals that are integral to the R380, such as the keyboard controller. This results in four previously used chip selects becoming available for use as GPIO signals if the particular design warrants.

Table 5-3: 386EX P2CFG Register Detail

P2CFG Bit	Set Signal Binding	Clear Signal Binding	Bit value	R380 Notes
7	CTS0#	P2.7	1	Used by SIO Unit
6	CS6#	P2.6	1	Reserved Chip Select
5	CS5#	P2.5	1	Reserved Chip Select
4	CS4#	P2.4	1	Reserved Chip Select
3	CS3#	P2.3	0	Internal chip selects provided by the R380 allow these 386EX chip selects, CS0 - CS3, to be used as GPIO pins.
2	CS2#	P2.2	0	
1	CS1#	P2.1	0	
0	CS0#	P2.0	0	

5.2.2.3. P3CFG Register

The Register Detail table below describes the signal bindings defined by the P3CFG Register. The PWRDWN signal is overridden to provide a GPIO signal. In the sample design under consideration, this GPIO bit is used as an input.

Table 5-4: 386EX P3CFG Register Detail

P3CFG Bit	Set Signal Binding	Clear Signal Binding	Bit value	R380 Notes
7	COMCLK	P3.7	1	
6	PWRDWN	P3.6	0	
5	INT3	P3.5	1	
4	INT2	P3.4	1	
3	INT1	P3.3	1	
2	INT0	P3.2	1	
1	TMROUT1	P3.1	1	
0	TMROUT0	P3.0	1	

5.2.2.4. PINCFG Register

The Register Detail table below describes the signal bindings defined by the PINCFG Register. The PINCFG Register is different from the P*n*CFG Registers in that signal bindings are resolved between signals that are both inputs or outputs of a particular functional unit.

Table 5-5: 386EX PINCFG Register Detail

PINCFG Bit	Set Signal Binding	Clear Signal Binding	Bit value	R380 Notes
7				Reserved
6	REFRESH#	CS6#	0	
5	TMR2 Signals	NPx Signals	1	
4	CS5#	DACK0#	0	
3	CTS1#	EOP#	0	
2	TXD1	DACK1#	1	
1	DTR1#	SRXCLK	1	
0	RTS1#	SSIOTX	1	

5.2.2.5. Peripheral Configuration Registers

In addition to the Pin Configuration Registers, there are four Peripheral Configuration registers that are also initialized. These include the DMA Configuration Register (DMACFG), the Interrupt Configuration Register (INTCFG), the Timer Configuration Register (TMRCFG), and the SIO and SSIO Configuration Register (SIOCFG). These registers are specific to the particular implementation. Please refer to section 5.1 and the *Intel386EX Embedded Microprocessor User's Manual* for more information.

5.2.3. Chip Select Unit Registers

The address decode for peripherals that are internal to the R380, such as the keyboard controller is done by the R380 in the example design. The only chip select that is programmed is the UCS Chip Select, which is used to select a boot device. This could be used to supplement or replace the CE_BIOS Chip Select for the Flash Boot Device. Once again, chip select usage is highly implementation dependent.

6. Tables

Table 6-1: R380/386EX-based System Functional Unit Summary

Component	Functional Unit	Description
Intel386EX PC-Compatible Features	Interrupt Controllers (2)	8259A-Compatible Peripheral Interrupt controller.
	Timer/Counters (3)	82C54-Compatible Programmable Interval Timer with enhancements to allow remapping of peripheral addresses & interrupt assignments
	Asynchronous Serial Ports (2)	NS16450 Compatible UART. All interrupts may be connected to the interrupt controller or two may be connected to the DMA controller
Intel386EX Embedded Extensions	DMA Controller	PC-Compatible to a certain extent. Backward compatible with 8237A. Two independent DMA channels can be 8 or 16 bits wide.
	Clock & Power Management Unit	Provides a programmable clock signal for EX core and for peripherals. Power management capability provides idle (stops CPU clock; peripheral clock runs) and powerdown (both CPU and peripheral clocks stopped) modes.
	Watchdog Timer	General purpose 32-bit timer
	Synchronous Serial Port (1)	Provides bi-directional serial I/O up to 5 Mbps. Built-in protocols are not included. Synchronous serial IO interrupts may be connected to the DMA controller for high-speed transfers.
	Parallel I/O Port	
	Programmable Chip Select Units (8)	
	DRAM Refresh Control	Generates periodic refresh requests and refresh addresses
	JTAG Test-logic	Simplifies board level testing. Fully compliant with IEEE Std 1149.1-1990.
RadiSys R380 PC-Compatible Features	Real Time Clock	Provides Motorola 146818A-compatible real time clock and alarm with 114 bytes of battery-backed CMOS memory. The RTC also generates a periodic interrupt. Access to the CMOS memory is through registers 070h and 071h in an index/data fashion. The Real-time clock is enabled or disabled by bootstrap pins on the R380.
	Keyboard/Mouse Controller	Implements a 8042-Compatible keyboard controller with extensions to support a PS/2 mouse. The controller is enabled or disabled by bootstrap pins on the R380.
	PC Speaker/"Port B" Functionality	Port B register is located at 061h
RadiSys R380 Core System Support Features	DRAM Refresh Controller	Supports two banks of SIMMs as Fast Page Mode (FPM), Extended Data Out (EDO) or Flash SIMMs. Second bank start address is configurable. Supports EDO/FPM memory type detection.
	Power Management Support	Supports Power Management with Halt detection logic, SMI generation logic, and glitchless clock switching.
	ROM/Flash ROM Controller	Supports SIMM-style Flash
	Digital IO Port	16 General-purpose I/O bits
	Programmable Chip Select Units (4)	Control for ISA Bus peripheral devices
	IDE Interface	Supports EIDE transfer modes (PIO4). Located at address 01F0h.
	LED Control	Control for two pins/external indicators available

7. References

7.1. Publications

RadiSys R380 Product Development Specification, Revision 2.0, RadiSys Corporation, November 16, 1995

Intel 386™EX Embedded Microprocessor User's Manual, Intel Corporation, February 1995

The Intel 386™EX Microprocessor's Enhanced DMA and DOS Compatibility, Intel Corporation

Intel 386™EX Processor C-Step Definition, Intel Corporation

Advanced Power Management (APM) BIOS Interface Specification, Revision 1.1, Intel Corporation and Microsoft Corporation, September 1993

7.2. Internet Resources

Intel Architecture Laboratories, http://www.intel.com/IAL, Intel Corporation