■ General Description

The AT9173 is a voltage regulator which could convert the input voltage ranging from 1.8V to 5V to an output voltage that user settled. The regulator can provide sourcing or sinking current.The AT9173, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed backplane designs.

The voltage output of the regulator can be used as a termination voltage for DDR SDRAM.

Current limits in both sourcing and sinking mode, plus on-chip thermal shutdown make the circuit tolerant of the output fault conditions.

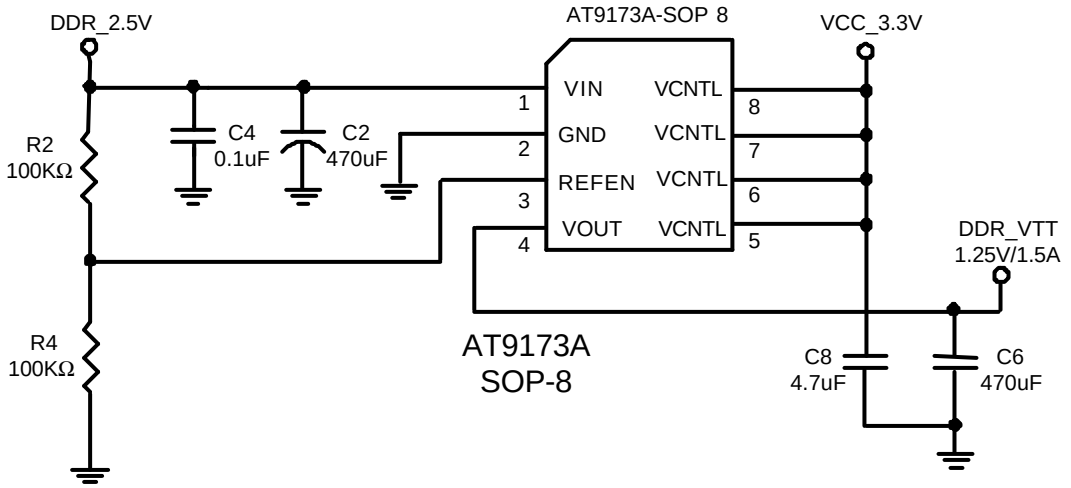
■ Features

- Support Both DDR I (1.25VTT) and DDR II (0.9VTT) Requirements
- Capable of Sourcing and Sinking Current
- Current-limiting Protection
- Thermal Protection
- Integrated Power MOSFETs
- Generates Termination Voltages for SSTL-2
- High Accuracy Output Voltage at Full-Load
- Adjustable V_{OUT} by External Resistors
- Minimum External Components
- Shutdown for Standby or Suspend Mode Operation with High-impedance Output

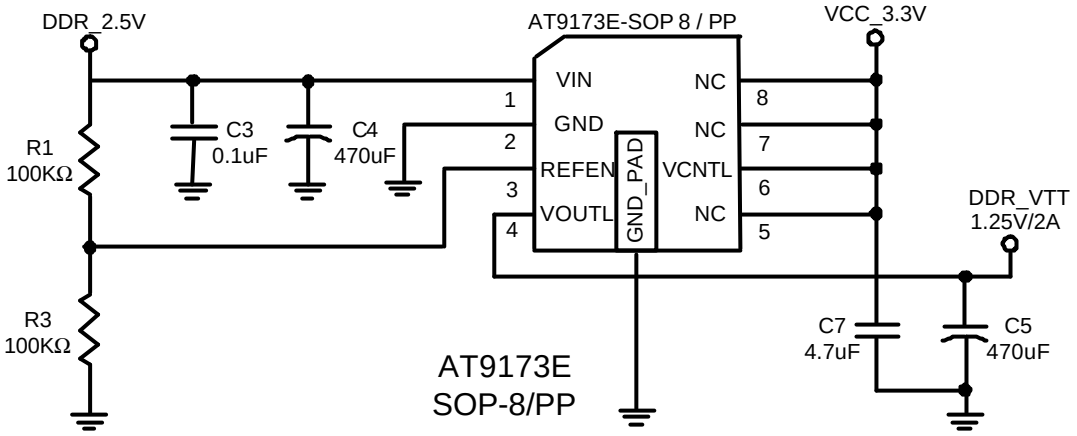
■ Applications

- DDRI/DDRII Memory Termination Supply
- Active Termination Buses
- Desktop PC,NoTebook,Server and workstation
- Graphic Card
- Set Top Box
- Embedded System

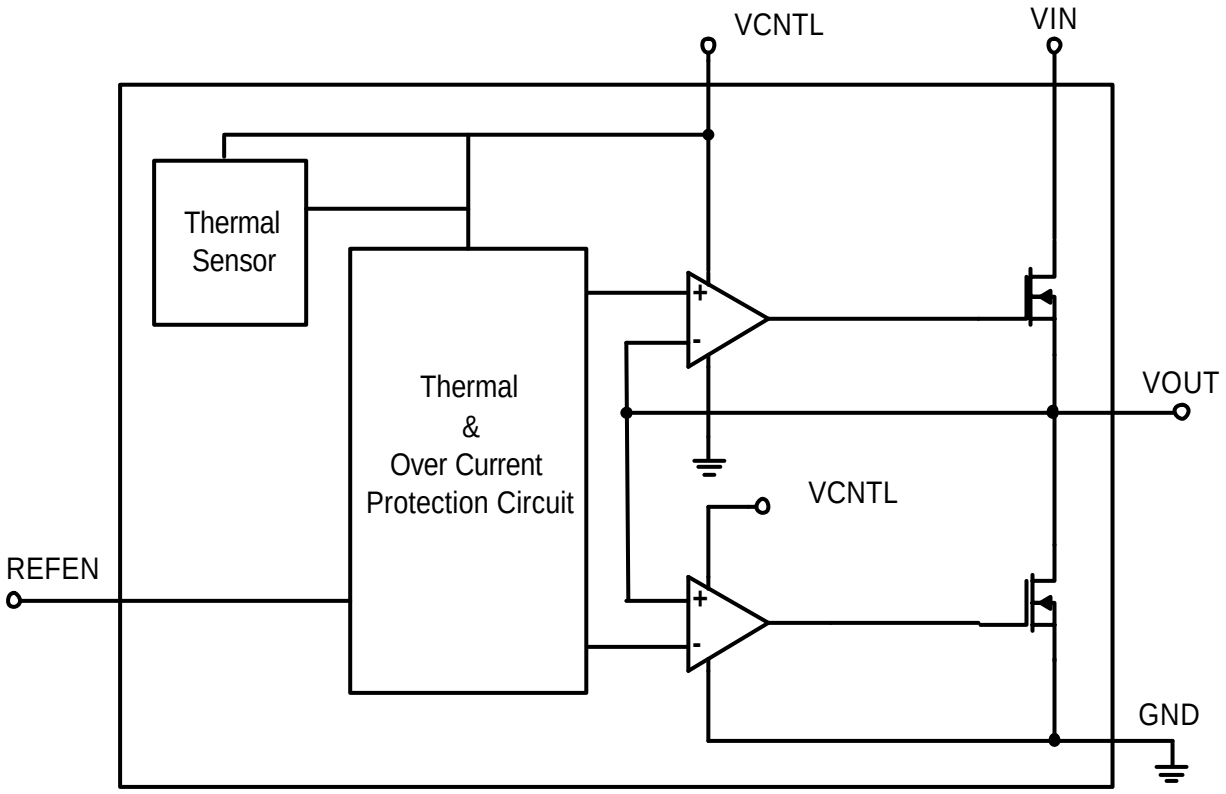
■ Typical Application



■ Typical Application(Contd.)

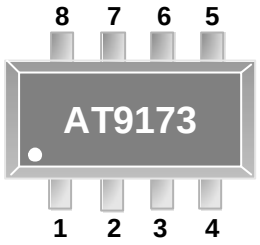


■ Function Block Diagram



■ Pin Configuration

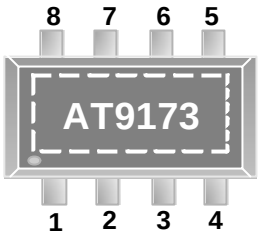
SOP- 8
Top View



AT9173A

1. IN
2. GND
3. REFEN
4. OUT
5. VCNTL
6. VCNTL
7. VCNTL
8. VCNTL

SOP- 8/PP
Top View



AT9173E

1. IN
2. GND
3. REFEN
4. OUT
5. NC
6. VCNTL
7. NC
8. NC

■ Pin Description

Pin name	Pin Description
IN	Input voltage pin which supplies current to the V_{OUT} pin. Connect this pin to a well-decoupled voltage to prevent the input rail from dropping during large load transient. A large and low ESR capacitor is recommended to use that should be placed as close as possible to the V_{IN} pin.
GND	Ground pin. Tie directly to ground plance.
VCNTL	Voltage control pin which supplies the internal control circuitry and provides the drive voltage. The driving capability of output current is proportioned to the VCNTL. Connect this pin to 5V bias supply to handle large output current with at least 1uF capacitor from this pin to GND. An important note is that V_{IN} should be kept lower or equal to VCNTL.
REFEN	Reference voltage input and active low shutdown control pin. Two resistors dividing down the V_{IN} voltage on this pin to create the regulatedoutput voltage. Pulling this pin to GND to turn off the device by an open-drain, such as 2N7002 N-Channel MOSFET.
OUT	Regulator output. V_{OUT} is regulated from REFEN voltage that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output rail. To maintain adequate large signal transient response, typical value of 1000uF electrolytic capacitor with 10uF ceramic capacitors are recommended to reduce the effects of current transients on V_{OUT}.
NC*	No Connection. Not internal connected.
GND Pad*	Connected to GND plance for better heat dissipation.

* By SOP-8/PP only

■ Ordering Information

Part Number	Marking	Output Voltage	Package	Operating Temp. Range
AT9173AG	AT9173AG yyww* AB xxxxxxx##**	ADJ	SOP-8	-25°C to +85°C
AT9173EG	AT9173EG yyww* AC xxxxxxx##**	ADJ	SOP-8/PP	

Note:

* yy and ww represents the data code.

** XXXXXXX represents the wafer lot number, ## represents the wafer number

■ Absolute Maximum Ratings

Parameter	Symbol	Maximum	Unit
Input Voltage. V_{IN} to GND	V_{IN}	6	V
VCNTL to GND	V_{CNTL}	6	V
ESD Rating (Human Body Mode)	V_{ESD}	2	KV
Storage Temperature	T_{STG}	150	^{O}C

■ Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage 1	V_{IN}	1.8 or 2.5	V
Supply Voltage 2	V_{CNTL}	3.3	V
Output Current of V_{OUT} Pin *	$*I_{OUT}$	-2 to +G92	A
Junction Temperature	T_J	-25 to +125	^{O}C

*The symbol "+" means the VOUT sources current to load; the symbol "-" means the VOUT sinks current to GND

■ Thermal Characteristics

Parameter	Package	Die Attch	Symbol	Maximum	Unit
Thermal Resistance** (Junction to Case)	SOP-8	Non-Conductive Epoxy	θ_{JC}	55	$^{O}C/W$
	SOP-8/PP	Conductive Epoxy		19	
Thermal Resistance (Junction to Ambient)	SOP-8	Non-Conductive Epoxy	θ_{JA}	120	
	SOP-8/PP	Conductive Epoxy		84	
Internal Power Dissipation	SOP-8	Non-Conductive Epoxy	P_D	1300	mW
	SOP-8/PP	Conductive Epoxy		1450	
Solder Iron (10Sec) ***				350	^{O}C

** Measure θ_{JC} on backside center of molding compund if IC has no tab.

*** MIL-STD-202G 210F

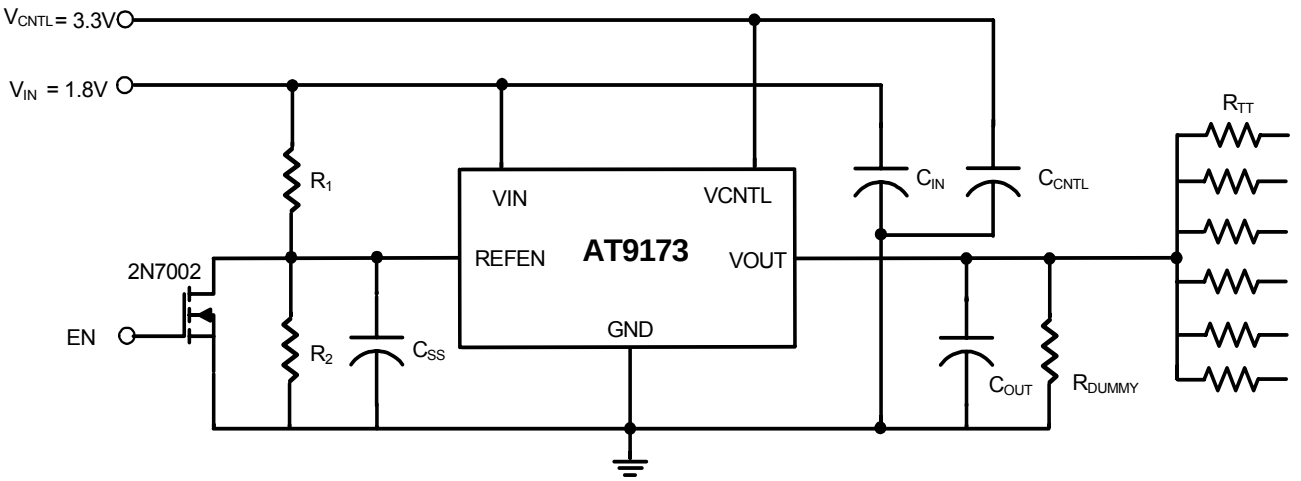
■ Electrical Specifications

Limits in standard typeface are for T_A=25°C, unless otherwise specified:
V_{IN}=2.5V, V_{CNTL}=3.3V, V_{REFEN}=0.5V_{IN}.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Offset Voltage	V_{OS}	I_{OUT}=0A (Note 1)	-20	0	20	mV
Load Regulation (DDR 1/2)	V_{LOAD}	I_L=0~1.5A (Fig 4)	-20	0	20	mV
		I_L=0~-1.5A	-20	0	20	
Input Voltage Range (DDR 1/2)	V_{IN}	KEEP $V_{CNTL} \geq V_{IN}$ on operation power on and power off	1.6	2.5/1.8	4	V
	V_{CNTL}		2.5	3.3	6	
Operating Current of V_{CNTL}	I_{CNTL}	No Load		1.4		mA
Current In Shutdown Mode	I_{SHDN}	V_{REFEN} < 0.2V, R_L=180Ω (Fig 5)		25.6		µA
Short Circuit Protection						
SOP-8 Current Limit	I_{LIMIT}	Fig 6,7	2.1			A
PSOP-8 Current Limit	I_{LIMIT}	Fig 6,7	2.4			A
Over Temperature Protection						
Thermal Shutdown Temperature	T_{SD}	3.3V ≤ V_{CNTL} ≤ 5 V	125			°C
Thermal Shutdown Hysteresis		Guaranteed by design		30		

Note1: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

■ Application Information



$R_1 = R_2 = 100K\Omega$, $R_{TT} = 50\Omega / 33\Omega / 25\Omega$
$C_{OUT(MIN)}$ = 10uF (Ceramic) + 1000uF under the worst case testing condition
R_{DUMMY} = 1KΩ as for V_{OUT} discharge when V_{IN} is not presented but V_{CNTL} is presented
C_{SS} = 1uF, C_{IN} = 470uF (Low ESR), C_{CNTL} = 47uF

■ Application Circuit

Typical application circuit is used as a regulator to provide termination voltage in double data rate (DDR) memory system. The regulator could source and sink up to 2A peak current. The output voltage will follow REFEN which generated by two external dividing resistors down from V_{IN} or to the desired output voltage set externally by forcing a voltage level to REFEN pin. To add a shutdown function , connect a small transistor to REFEN pin. To perform shutdown function , put a logic high 5V signal to EN yield a low (0V) to REFEN pin thus force output voltage to zero voltage. The capacitor Css is used to softstart the output voltage since V_{OUT} will follow REFEN.

Time constant for this circuit is Css*(R1//R2). The Css could also used as the bypass capacitor to filter out noise in REFEN pin. So carefully layout should put Css close to REFEN pin to maintain noise immunity. The C_{IN} an C_{CNTL} is used as power decoupling capacitor. C_{OUT} is composed of 10uF ceramic plus 1000uF electrolyte capacitors. The first one is to used as high frequency filter and the second one is used to reduce voltage drop during load regulating.

■ General Regulator

The AT9173 can be used as a general regulator. To get a desired output voltage, put a reference voltage to REFEN pin or dividing resistors down a input voltage source. To drive inside N-Channel MOSFET the V_{CNTL} should be larger than V_{IN} to get enough driving voltage. The minimum dropout voltage could be I_{OUT}*0.1, where I_{OUT} is the output current.

■ Layout issue

Place a bypass capacitor as close as possible to V_{IN} and V_{CNTL} pin is necessary. A low ESR capacitor is recommended for this bypass capacitor. Use wide and short PCB traces to connect in between V_{IN} power source V_{OUT} to reduce PCB resistance thus to reduce undesired power dissipation.

■ Thermal issue

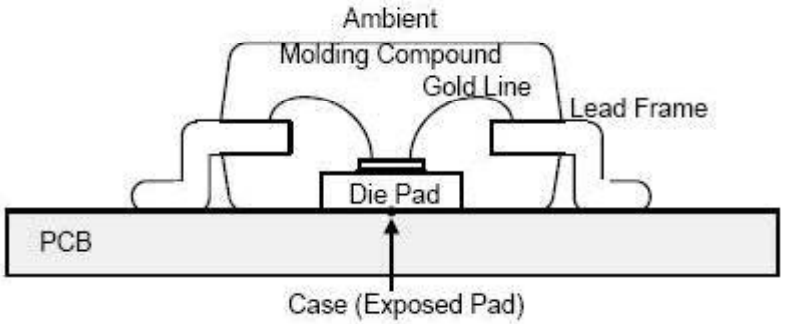
AT9173 has a internal thermal protection to protect the device at any overload conditions. For safety reason the operation junction temperature should not exceed 125 ℃. The dissipation of the device is

$$P_D = (V_{IN} - V_{OUT}) x I_{OUT}$$

And also the maximum power dissipation is

$$P_{D,MAX} = (T_{J,MAX} - T_A) / q_{JA}$$

Where Tj,max is the maximum operation junction 125 degree C, Ta is the ambient temperature and the is q_{JA} the junction to ambient thermal resistance. The junction to ambient thermal resistance is 70 ℃/W for exposed pad SOP-8 package. It can be dramatically reduced by placing a large area PCB trace under exposed pad to emit heat generated by the die attached to the exposed pad.



■ Test Circuit

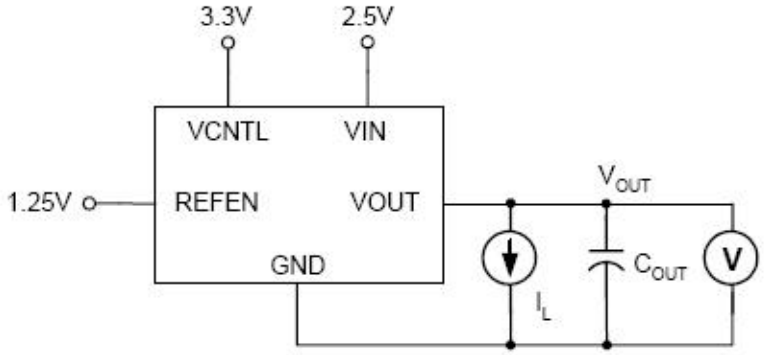


Fig 4: Output Voltage Tolerance, $\triangle V_{OUT}$

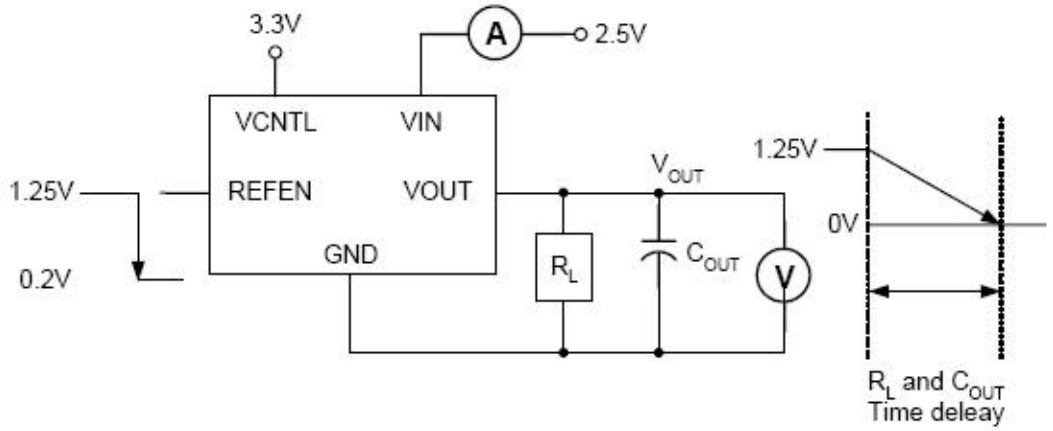


Fig 5: Current in Shutdown Mode, I_{SHDN}

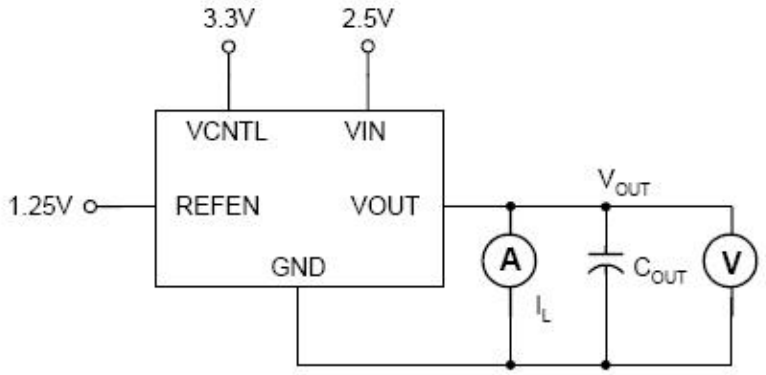


Figure 6: Current Limit for High Side, I_{CLHIGH}

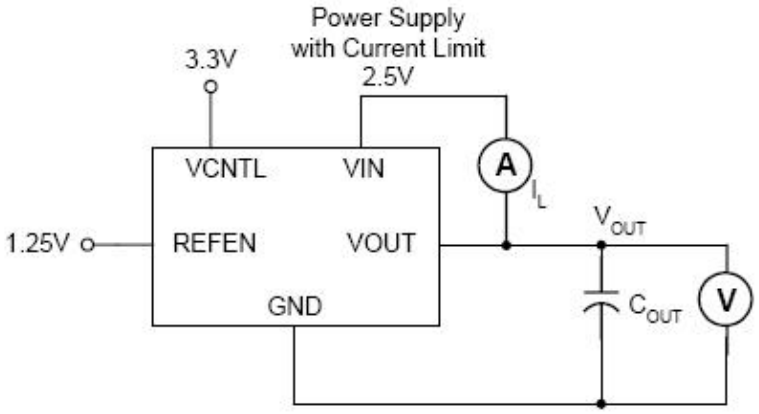
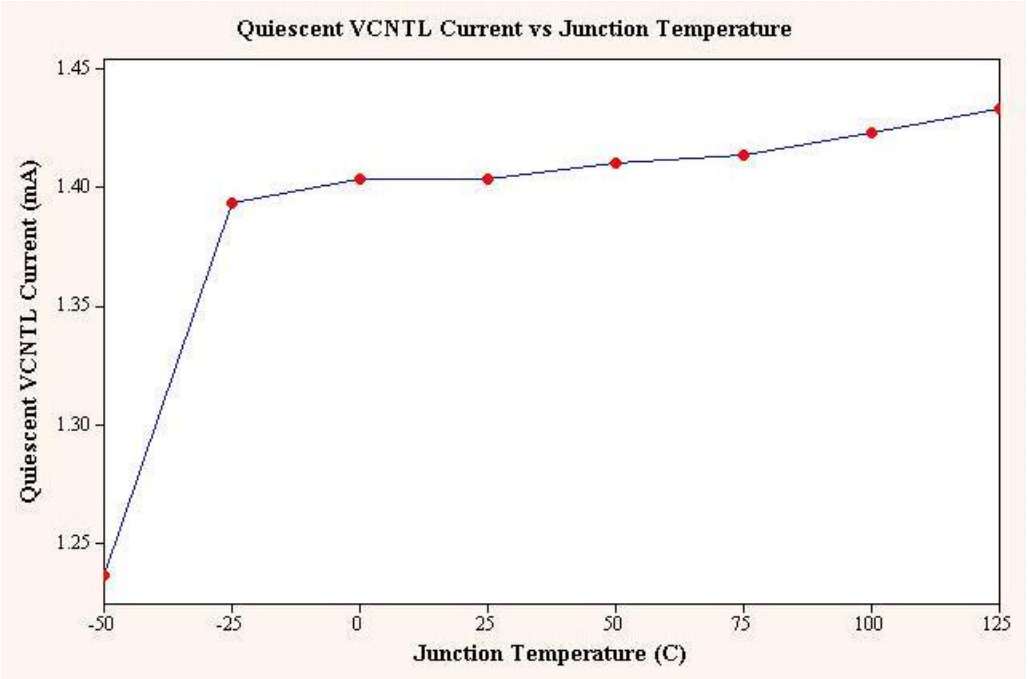
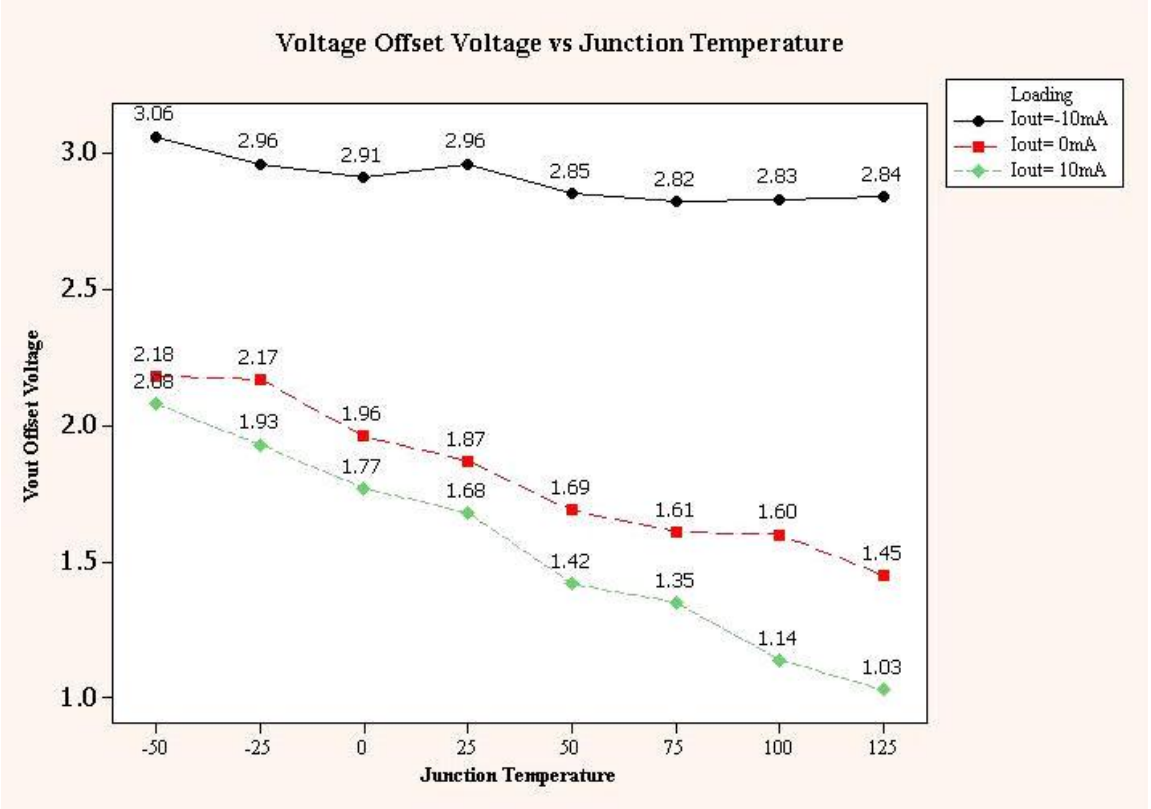


Figure 7: Current Limit for Low Side, I_{CLLOW}

■ Typical Characteristics

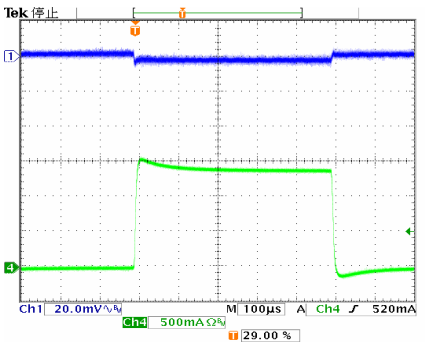
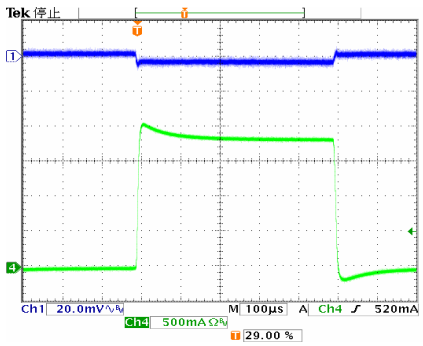
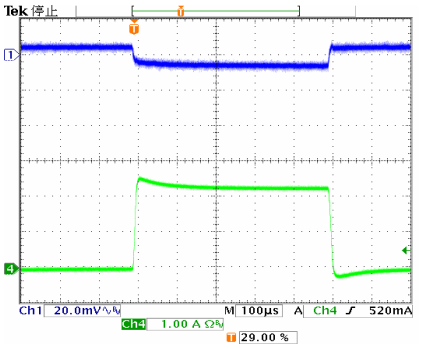




■ Operation Waveforms DDR1

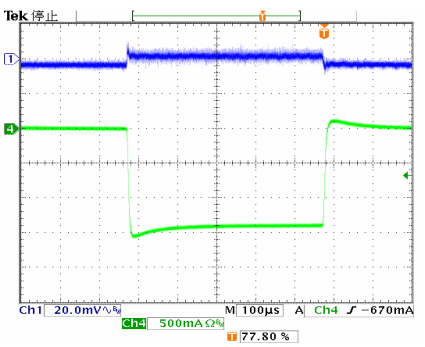
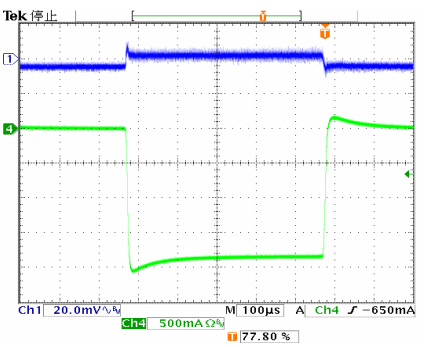
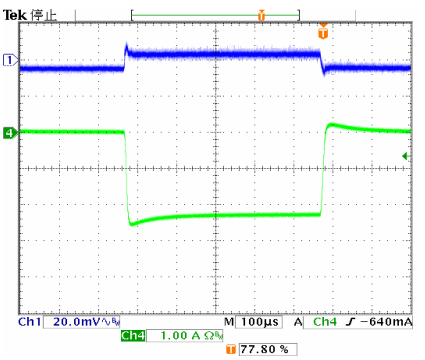
Load Transient Response

V_{IN}=2.5V, V_{CNTL}=3.3V
V_{REF} is 1.25V supplied by a regulator
C_{OUT}=1000uF/35V
I_{OUT} slew rate = +-0.25A/mS

+ 0 A→ + 1.5 A → + 0 A	+ 0 A→ + 2 A → + 0 A	+ 0 A→ + 2.5 A → + 0 A
		
Ch1= V_{OUT} , Ch4 = I_{OUT}	Ch1= V_{OUT} , Ch4 = I_{OUT}	Ch1= V_{OUT} , Ch4 = I_{OUT}

Load Transient Response

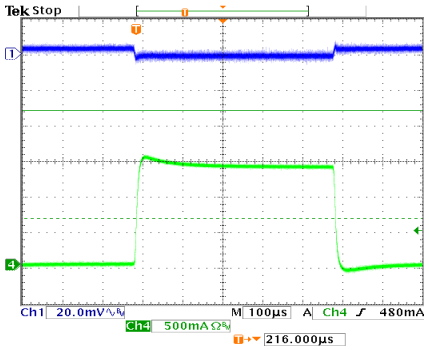
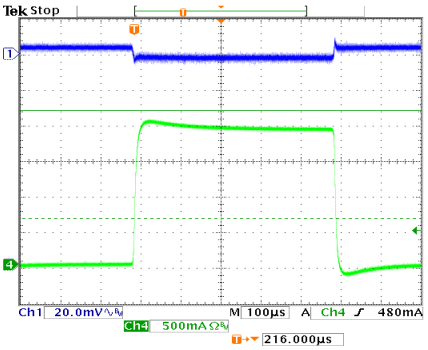
V_{IN}=2.5V, V_{CNTL}=3.3V
V_{REF} is 1.25V supplied by a regulator
C_{OUT}=1000uF/35V
I_{OUT} slew rate = +-0.25A/mS

- 0 A → - 1.5 A → - 0 A	- 0 A → - 2 A → - 0 A	- 0 A→ - 2.5 A → - 0 A
		
Ch1= V_{OUT} , Ch4 = I_{OUT}	Ch1= V_{OUT} , Ch4 = I_{OUT}	Ch1= V_{OUT} , Ch4 = I_{OUT}

■ Operation Waveforms DDR2

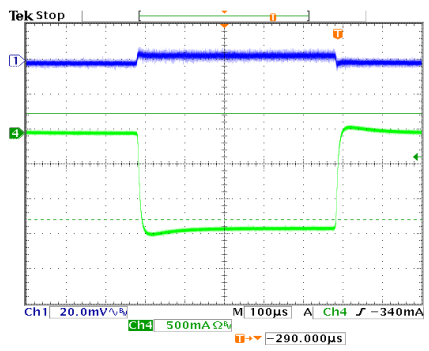
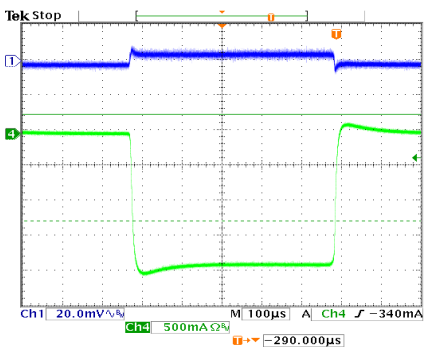
Load Transient Response

V_{IN}=1.8V, V_{CNTL}=3.3V
V_{REF} is 0.9V supplied by a regulator
C_{OUT}=1000uF/35V
I_{OUT} slew rate = +-0.25A/mS

+ 0 A→ + 1.5 A→+ 0 A	+ 0 A→ + 2 A→+ 0 A
	
Ch1= V_{OUT},Ch4= I_{OUT}	Ch1= V_{OUT} ,Ch4= I_{OUT}

Load Transient Response

V_{IN}=1.8V, V_{CNTL}=3.3V
V_{REF} is 0.9V supplied by a regulator
C_{OUT}=1000uF/35V
I_{OUT} slew rate = +-0.25A/mS

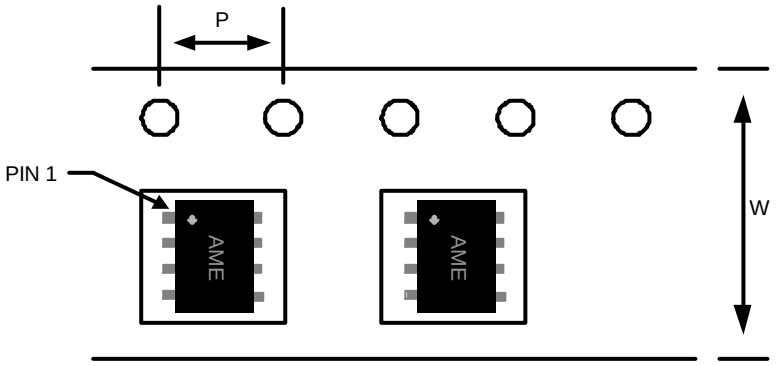
- 0 A→ - 1.5 A→ - 0 A	- 0 A→ - 2 A→ - 0 A
	
Ch1= V_{OUT}, Ch4 = I_{OUT}	Ch1= V_{OUT}, Ch4 = I_{OUT}

■ Date Code Rule

Marking			Date Code		Year
A	A	A	W	W	xxx0
A	A	A	W	W	xxx1
A	A	A	W	W	xxx2
A	A	A	W	W	xxx3
A	A	A	W	W	xxx4
A	A	A	W	W	xxx5
A	A	A	W	W	xxx6
A	A	A	W	W	xxx7
A	A	A	W	W	xxx8
A	A	A	W	W	xxx9

■ Tape and Reel Dimension

SOP- 8

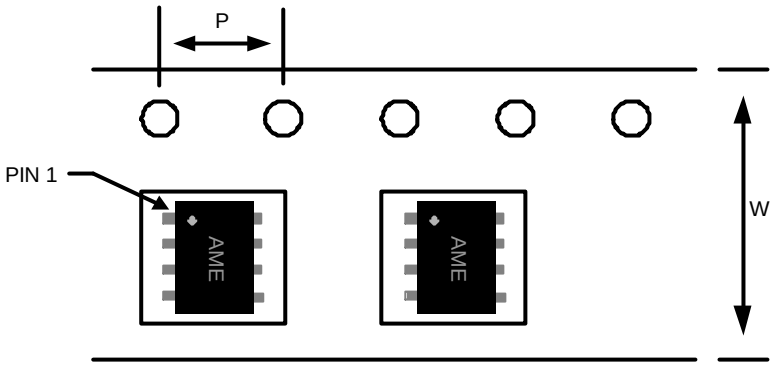


Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
SOP-8	12.0±0.1 mm	4.0±0.1 mm	2500pcs	330±1 mm

■ Tape and Reel Dimension

SOP- 8/PP

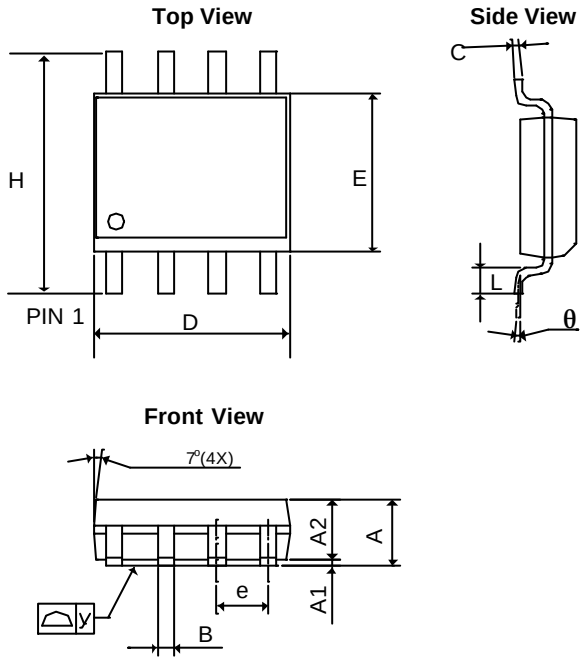


Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
SOP-8/PP	12.0±0.1 mm	4.0±0.1 mm	2500pcs	330±1 mm

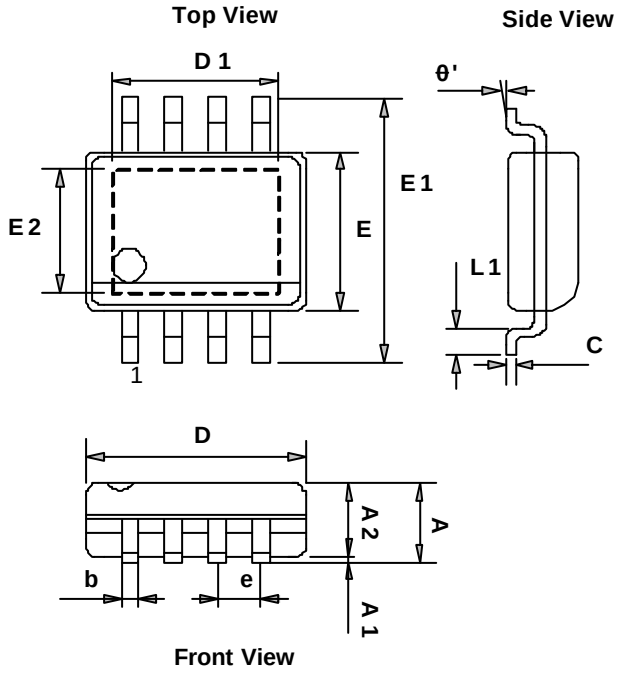
■ Package Dimension

SOP-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.05315	0.0689
A_1	0.10	0.30	0.0039	0.0118
A2	1.473 REF		0.05799 REF	
B	0.33	0.51	0.0130	0.0201
C	0.17	0.25	0.0067	0.0098
D	4.70	5.33	0.1850	0.2098
E	3.80	4.00	0.1496	0.1575
e	1.27 BSC		0.05000 BSC	
L	0.40	1.27	0.0157	0.0500
H	5.80	6.30	0.2283	0.2480
y	-	0.10	-	0.0039
q	0^o	8^o	0^o	8^o

SOP-8/PP



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0	0.150	0	0.006
A2	1.350	1.600	0.053	0.063
C	0.100	0.250	0.004	0.010
E	3.750	4.150	0.148	0.163
E1	5.700	6.300	0.224	0.248
L1	0.300	1.270	0.012	0.050
b	0.310	0.510	0.012	0.020
D	4.720	5.120	0.186	0.202
e	1.270 BSC		0.05 BSC	
q	0^o	8^o	0^o	8^o
E2	2.150	2.513	0.085	0.099
D1	2.150	3.402	0.085	0.134

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