High Definition Audio SoundMAX Codec

AD1989B

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FEATURES

- Ten 192 kHz, 101 dB DACs
  - 7.1 surround sound plus independent headphone
  - All independent sample rates, 8 kHz through 192 kHz
  - Selectable stereo mixer on outputs
  - 16-, 20-, and 24-bit resolution
- Six 192 kHz, 92 dB ADCs
  - Simultaneous record of up to 3 stereo channels
  - All independent sample rates, 8 kHz through 192 kHz
  - 16-, 20-, and 24-bit resolution
- S/PDIF output
  - 2 independent transmitters, second S/PDIF can support external HDMI interface
  - Supports 44.1 kHz through 192 kHz sample rates
  - 16-, 20-, and 24-bit data; PCM, and AC3 formats
  - Digital PCM gain control
- S/PDIF input
  - Supports 44.1 kHz through 192 kHz sample rates
  - 16-, 20-, and 24-bit data; PCM, and AC3 formats
  - Digital PCM gain control
  - Auto synchronizes to source sample rate
- Dedicated auxiliary pins
  - Stereo CD/auxiliary I/O port w/GND sense
  - MONO_OUT pin for internal speaker with EAPD support
- Microsoft Vista Premium® logo compliant
- Support up to 9 audio jacks
- Impedance and presence detection; retasking
- 5 adjustable microphone bias pins
- Digital and analog PCBeep
- 3 general-purpose digital I/O (GPIO) pins
- Multiple EAPD pins for external circuit control
- 3.3 V analog and digital supply voltages
- 1.5 V and 3.3 V HD Audio link signaling
- Advanced power management modes

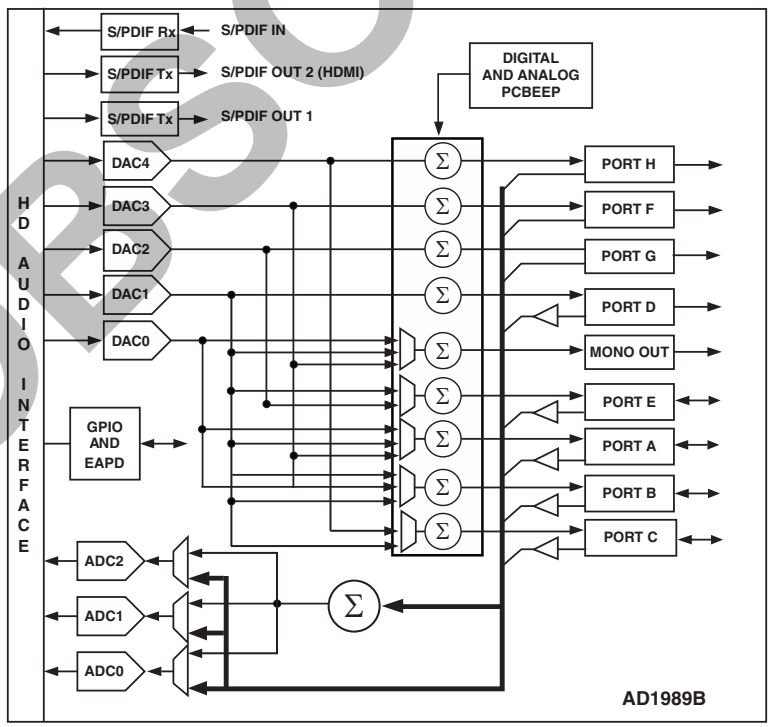

Figure 1. AD1989B Block Diagram

Rev. 0

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REVISION HISTORY

8/08—Revision 0: Initial Version

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GENERAL DESCRIPTION

The AD1989B audio codec and SoundMAX® software provides superior HD audio quality that exceeds Vista Premium performance. The AD1989B has ten 101 dB DACs and six 92 dB ADCs, three stereo headphone ports, C/LFE swapping, digital and analog PCBeep, and two independent S/PDIF outputs, making the AD1989B the right choice for PCs where performance and a rich feature set are primary considerations.

The jack retasking feature on this product supports various configurations including 7.1 on 5 jacks, 5.1 on 3 jacks, and front panel jack retasking.

The AD1989B is available in a 48-lead RoHS compliant lead frame chip scale package in both reels and trays. See Ordering Guide on Page 20.

SPECIAL SOFTWARE FEATURES

The AD1989B audio codec also supports the following additional software features:

- BlackHawk® and SoundMAX GUI contain all user audio controls
- Voice input enhancement: Andrea Electronics best-in-class noise reduction, beam forming, and echo cancellation
- Output enhancement: Sensaura/Sonic Focus, spreading/downmixing, MP3 refinement, adaptive dynamics, compressor/limiter, speaker/graphic EQ, Voice Clarity/X-Matrix™, AGC, UI tuning tools
- DTS®, SRS®, EAX® for gaming

ADDITIONAL INFORMATION

This data sheet provides a general overview of the AD1989B SoundMAX codec's architecture and functionality. Additional information on the AD1989B is available in the AD1989B Programmers Reference Manual. Please contact your local Analog Devices, Inc., sales representative for more information. For information on SoundMAX codecs and software, see Analog Devices website at http://www.analog.com/soundMAX.

JACK CONFIGURATION

The guidelines shown in Table 1 and Table 2 should be used when selecting ports for particular functions.

Table 1. Typical Desktop Applications with Discreet Jacks (Default Configuration)

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Line-In
Port D	Rear Line-Out
Port E	Rear Microphone
Port F	Rear Surround (5.1)
Port G	Rear C/LFE
Port H	Rear Surround (7.1)

Table 2. Typical Desktop Retasking to Support Input/5.1 on 3 Jacks

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Line-In/Surround Out
Port D	Rear Line-Out
Port E	Rear Microphone/C/LFE

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SPECIFICATIONS

TEST CONDITIONS

Parameter	Test Condition
Temperature	25°C
Digital Supply	3.3 V
Analog Supply	3.3 V
MIC_BIAS_IN (via Low-Pass Filter)	5.0 V
Sample Rate f_S	48 kHz
Input Signal (Frequency Sine Wave)	1008 Hz
Amplitude for THD + N	–3.0 dB Full Scale
Analog Output Pass Band	20 Hz to 20 kHz
DAC	10 kΩ Output Load: Line-Out Tests
	32 Ω Output Load: Headphone Tests
ADC	0 dB Gain

PERFORMANCE

Parameter	Min	Typ	Max	Unit
Line-Out Drive (10 kΩ loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		–86		dB
Dynamic Range (–60 dB in ref to f_S A-Weighted)		101		dB
Signal-to-Noise Ratio		101		dB
Headphone Drive (32 Ω loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		–84		dB
Dynamic Range (–60 dB in ref to f_S A-Weighted)		101		dB
Signal-to-Noise Ratio		101		dB
Input Ports (Mic Boost = 0 dB)				
Total Harmonic Distortion (THD + N)		–80		dB
Dynamic Range (–60 dB in ref to f_S A-Weighted)		92		dB
Signal-to-Noise Ratio		92		dB

GENERAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
DIGITAL DECIMATION AND INTERPOLATION FILTERS—f_S = 8 kHz to 96 kHz[1]				
Pass Band	0		0.4 f_S	Hz
Pass-Band Ripple			±0.005	dB
Stop Band	0.6 f_S			Hz
Stop-Band Rejection	–110			dB
Group Delay		20		$1/f_S$
Group Delay Variation Over Pass Band		0		µs
ANALOG-TO-DIGITAL CONVERTERS				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)[2]			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)		±0.2	±0.5	dB
ADC Offset Error[1]			±5	mV
ADC Crosstalk[1]				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–94		dB
Line Inputs to Other		–100	–80	dB
DIGITAL-TO-ANALOG CONVERTERS				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)[1]			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
DAC Crosstalk (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)[1]		–104		dB

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Parameter		Min	Typ	Max	Unit
DAC VOLUMES					
Step Size (DAC0, DAC1, DAC2, DAC3)			1.5		dB
Output Gain/Attenuation Range		–58.5		0	dB
Mute Attenuation of 0 dB Fundamental[1]			–80		dB
ADC VOLUMES					
Step Size (ADCSEL-0, ADCSEL-1)			1.5		dB
PGA Gain/Attenuation Range		–58.5		+22.5	dB
Mute Attenuation of 0 dB Fundamental[1]			–80		dB
ANALOG MIXER					
Signal-to-Noise Reduction (SNR) Input to Output			95		dB
Step Size: All Mixer Inputs			–1.5		dB
Input Gain/Attenuation Range: All Mixer Inputs		–34.5		+12.0	dB
ANALOG LINE LEVEL OUTPUTS					
Full-Scale Output Voltage: Line-Out Drive Enabled		1.0			V rms[3]
	Output Impedance[1]		190		Ω
	External Load Impedance[1]	10			kΩ
	Output Capacitance[1]		15		pF
	External Load Capacitance[1]			1000	pF
ANALOG HP DRIVE OUTPUTS					
Full-Scale Output Voltage: Line-Out Drive Enabled		1.0			V rms[3]
Ports A, B and D (when HP Drive is Enabled)		2.83			V p-p
	Output Impedance[1]			0.5	Ω
	External Load Impedance[1]	32			Ω
	Output Capacitance[1]		15		pF
	External Load Capacitance[1]			1000	pF
ANALOG INPUTS					
Input Voltages—Ports A, B, C, or E					
	Mic Boost = 0 dB		1		V rms[3]
			2.83		V p-p
Input Voltages—Microphone Boost	Mic Boost = +10 dB		0.316		V rms[3]
Amplifier, Ports B, C, or E			0.894		V p-p
	Mic Boost = +20 dB		0.1		V rms[3]
			0.283		V p-p
	Mic Boost = +30 dB		0.032		V rms[3]
			0.089		V p-p
Input Impedance					
PCBEEP			23		kΩ
Ports A, B, C, E (Mic Boost = 0 dB)			150		kΩ
Input Capacitance[1]			5	7.5	pF
MICROPHONE BIAS					
MIC_BIAS-B, MIC_BIAS-C					
MIC_BIAS_IN (Pin 33) = +5 V or +3.3 V	V_{REF} Setting = High-Z		High-Z		
	V_{REF} Setting = 0 V		0		V dc
	V_{REF} Setting = 50%		1.65		V dc
MIC_BIAS_IN (Pin 33) = +5 V	V_{REF} Setting = 80%		3.7		V dc
	V_{REF} Setting = 100%		3.9		V dc
MIC_BIAS_IN (Pin 33) = +3.3 V	V_{REF} Setting = 80%		2.86		V dc
	V_{REF} Setting = 100%		3.0		V dc
MIC_BIAS-E (When enabled as BIAS)	V_{REF} Setting = High-Z		High-Z		
	V_{REF} Setting = 0 V		0		V dc
	V_{REF} Setting = 50%		1.65		V dc
	V_{REF} Setting = 80%		2.86		V dc
	V_{REF} Setting = 100%		3.0		V dc
Output Drive Current	V_{REF} Setting = 50%, 80%, or 100%		1.6		mA

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Parameter		Min	Typ	Max	Unit
GPIO_0, GPIO_1, and GPIO_2					
Input Signal High (V_{IH})		$DV_{GPIO} \times 0.60$		DV_{GPIO}	V
Input Signal Low (V_{IL})		0		$DV_{GPIO} \times 0.24$	V
Output Signal High (V_{OH})	I_{OUT} = −500 µA	$DV_{GPIO} \times 0.72$		DV_{GPIO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{GPIO} \times 0.10$	V
Input Leakage Current (Signal High) (I_{IH})			−150		nA
Input Leakage Current (Signal Low) (I_{IL})			−50		µA
S/PDIF-Out_1, S/PDIF-Out_2					
Output Signal High (V_{OH})	I_{OUT} = −500 µA	$DV_{GPIO} \times 0.72$		DV_{GPIO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{GPIO} \times 0.10$	V
S/PDIF_IN					
Input Signal High (V_{IH})		$DV_{GPIO} \times 0.60$		DV_{GPIO}	V
Input Signal Low (V_{IL})		0		$DV_{GPIO} \times 0.24$	V
Input Leakage Current (Signal High) (I_{IH})			150		nA
Input Leakage Current (Signal Low) (I_{IL})			−50		µA
POWER SUPPLY					
Analog (AV_{DD}) 3.3 V ± 5%					
Power Supply Range		3.13	3.30	3.46	V
Power Dissipation			162		mW
Supply Current			49		mA
Digital (DV_{DD}) 3.3 V ± 10%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			241		mW
Supply Current			73		mA
Digital I/O (DV_{IO}) 3.3 V ± 10%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			0.66		mW
Supply Current			0.20		mA
Digital I/O (DV_{IO}) 1.5 V ± 5.5%					
Power Supply Range		1.42	1.50	1.58	V
Power Dissipation			0.03		mW
Supply Current			0.20		mA
Digital GPIO (DV_{GPIO}) 3.3 V ± 10%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			3.63		mW
Supply Current			1.10		mA
Power Supply Rejection (Reference to f_S 100 mV p-p Signal @ 1 kHz)[1]			80		dB

[1] Guaranteed but not tested.
[2] Measurements reflect main ADC.
[3] RMS values assume sine wave input.

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HD AUDIO LINK SPECIFICATION

HD Audio signals comply with the High Definition Audio Specifications. Please refer to these specifications at:
http://www.intel.com/standards/hdaudio/

POWER-DOWN STATES

Parameter	IDV_{DD} Typ	IAV_{DD} Typ	Unit
Function Node in D0, All Nodes Active	73	49	mA
Function Node in D3	24	1	mA
Codec in $\overline{\text{RESET}}$	3	3	mA
Individual Block Power Savings			
DAC Pair Powered Down Saves (Each)	6	5	mA
ADC Pair Powered Down Saves (Each)	6	3	mA
Mixer Power Control (and Associated Amps) Saves	0	2	mA
MIC_BIAS Powered Down Saves[1, 2]	0	0.1	mA

[1] Powering down the MIC_BIAS powers down all port MIC_BIAS pins. This disables all microphone bias circuits, setting them to the high-Z state.
[2] Test conditions: 30 pF load, 2.0 MHz frequency, 3.3 V A_{VDD}.

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ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed below may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Rating
Digital (DV_{DD})	–0.30 V to +3.65 V
Digital I/O (DV_{IO})	–0.30 V to +3.65 V
Digital GPIO (DV_{GPIO})	–0.30 V to +3.65 V
Analog (AV_{DD})	–0.30 V to +3.65 V
Input Current (Except Supply Pins)	±10.0 mA
Analog Input Voltage (Signal Pins)	–0.30 V to AV_{DD} + 0.3 V
Digital Input Voltage (Signal Pins)	–0.30 V to DV_{IO} + 0.3 V
Ambient Temperature (Operating)	0°C to +70°C
Storage Temperature	–65°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

All measurements per EIA-JESD51 with 2S2P test board per EIA-JESD51-7.

Table 3. Thermal Resistance

Package	θ_{JA}	θ_{JC}	θ_{CA}	Unit
LFCSP_VQ	47	15	32	°C/W

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

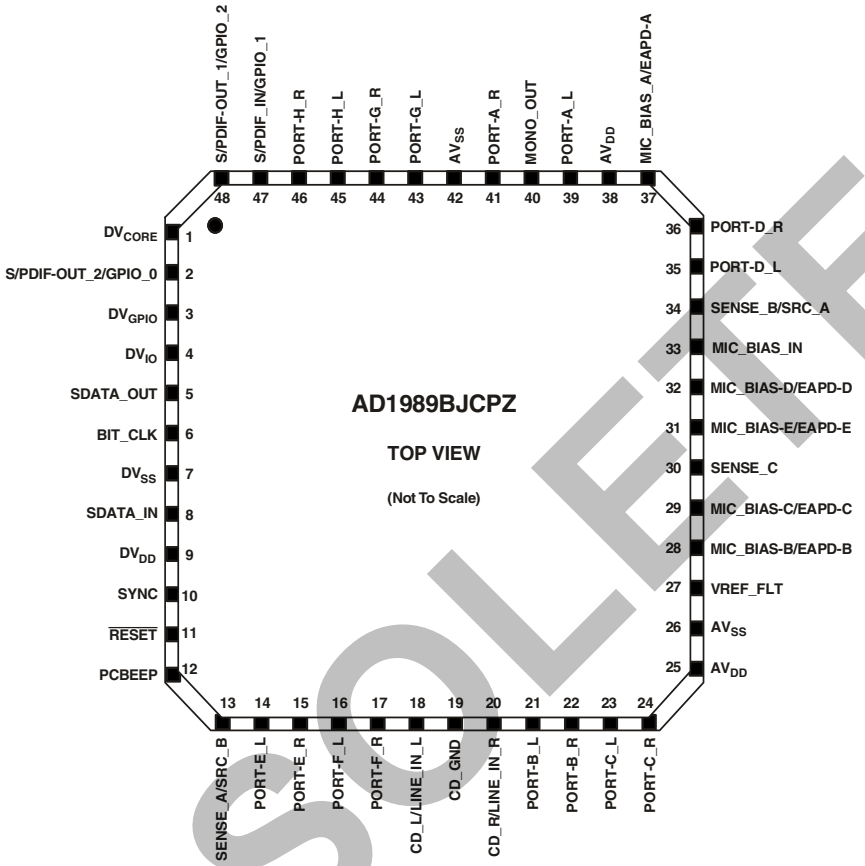

Figure 2. AD1989B 48-Lead Package and Pinout

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Table 4. Pin Function Descriptions

Mnemonic	Pin No.	Function	Description
DIGITAL INTERFACE			
SDATA_OUT	5	I	Link Serial Data Output. Clocked on both edges of BIT_CLK.
BIT_CLK	6	I	Link Bit Clock. 24.000 MHz serial data clock.
SDATA_IN	8	I/O	Link Serial Data Input. AD1989B output stream clocked only on one edge of BIT_CLK.
SYNC	10	I	Link Frame Sync.
$\overline{\text{RESET}}$	11	I	Link Reset. Master hardware reset.
DIGITAL I/O			
S/PDIF-OUT_2/GPIO_0	2	I/O	S/PDIF Out or GPIO. Supports S/PDIF output as primary function.
S/PDIF_IN/GPIO_1	47	I/O	S/PDIF Input/General-Purpose Input/Output Pin. Supports S/PDIF input as primary function.
S/PDIF-OUT_1/GPIO_2	48	I/O	S/PDIF_OUT or GPIO. Supports S/PDIF output as primary function.
JACK SENSE			
SENSE_A/SRC_B	13	I/O	JACK Sense A-D Input/Sense B drive.
SENSE_B/SRC_A	34	I/O	JACK Sense E-H Input/Sense A drive.
SENSE_C	30	I	JACK Sense CD/Line inputs.
ANALOG I/O			
PCBEEP	12	LI	Monaural Input From System for Analog PCBeep.
Port-E_L	14	LI, MIC, LO, SWAP	Auxiliary Input/Output Left Channel.
Port-E_R	15	LI, MIC, LO, SWAP	Auxiliary Input/Output Right Channel.
Port-F_L	16	LO	Auxiliary Input/Surround Rear (5.1) Left Channel.
Port-F_R	17	LO	Auxiliary Input/Surround Rear (5.1) Right Channel.
CD_L/LINE_IN_L	18	LI	CD Audio Left Channel.
CD_GND	19	LI	CD Audio Analog Ground Reference (for Differential CD Input). Must be connected to AGND via 0.1 µF capacitor if not in use as CD_GND.
CD_R/LINE_IN_R	20	LI	CD Audio Right Channel.
Port-B_L	21	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
Port-B_R	22	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
Port-C_L	23	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
Port-C_R	24	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
Port-D_L	35	LI, HP, LO	Rear Panel Headphone/Line-Out.
Port-D_R	36	LI, HP, LO	Rear Panel Headphone/Line-Out.
Port-A_L	39	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
MONO_OUT	40	LO	Monaural Output to Internal Speaker or Telephony Subsystem Speakerphone.
Port-A_R	41	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
Port-G_L	43	LO, SWAP	Rear Panel C/LFE Output.
Port-G_R	44	LO, SWAP	Rear Panel C/LFE Output.
Port-H_L	45	LO	Rear Panel Surround Center/Side (7.1).
Port-H_R	46	LO	Rear Panel Surround Center/Side (7.1).
FILTER/REFERENCE			
MIC_BIAS-B/EAPD-B	28	O	Switchable Microphone Bias. For use with Port B (Pins 21, 22).
MIC_BIAS-C/EAPD-C	29	O	Switchable Microphone Bias. For use with Port C (Pins 23, 24).
MIC_BIAS-E/EAPD-E	31	O	Switchable Microphone Bias. For use with Port E (Pins 14, 15).
MIC_BIAS-D/EAPD-D	32	O	Switchable Microphone Bias. For use with Port D (Pins 35, 36)
MIC_BIAS-A/EAPD-A	37	O	Switchable Microphone Bias. For use with Port A (Pins 39, 41) All MIC_BIAS pins are capable of: High-Z, 0 V, 1.65 V, 3.78 V, and 3.95 V (with 5.0 V on Pin 33) High-Z, 0 V, 1.65 V, 2.86 V, and 3.00 V (with 3.3 V on Pin 33).
VREF_FILT	27	O	Voltage Reference Filter.
DV_{CORE}	1	O	CAUTION: DO NOT APPLY 3.3 V TO THIS PIN! Filter connection for internal core voltage regulator. This pin must be connected to filter caps: 10 µF, 1.0 µF, and 0.1 µF connected in parallel between Pin 1 and DV_{SS} (Pin 4).

The symbols used in this table are defined as: I = input, O = output, LI = line level input, LO = line level output, HP = output capable of driving headphone load, MIC = input supports microphones with MIC bias and boost amplifier, SWAP = outputs can swap L/R channels (typically used to support C/LFE or shared C/LFE function).

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Table 4. Pin Function Descriptions (Continued)

Mnemonic	Pin No.	Function	Description
POWER AND GROUND			
DV_{GPIO} 3.3 V ± 10%	3	I	GPIO and S/PDIF Out (1 and 2) Signal Level (independent of DV_{IO}). Connect to 3.3 V ±10%.
DV_{IO} 3.3 V ± 10% or DV_{IO} 1.5 V ± 5.5%	4	I	Connect to the I/O voltage used for the HD Audio controller signals.
DV_{SS}	7	I	Digital Supply Return (Ground).
DV_{DD} 3.3 V ± 10%	9	I	Digital Supply Voltage 3.3 V. This is regulated down to Pin 1 to supply the internal digital core.
AV_{DD} 3.3 V ± 5%	25, 38	I	CAUTION: DO NOT APPLY 5.0 V TO THESE PINS! Analog Supply Voltage 3.3 V ONLY. Note: AV_{DD} supplies should be well regulated and filtered as supply noise degrades audio performance.
MIC_BIAS_IN	33	I	Source for Microphone Bias Circuitry. Connect this pin to 5.0 V via a low-pass filter. When connected this way the AD1989B is capable of providing +3.95 V as a mic bias to all of the MIC_BIAS pins. If 5 V is not available, connect this pin to +3.3 V (AV_{DD}) via a low-pass filter. The AD1989B produces a mic bias voltage relative to the AV_{DD} supply (typically 3.0 V @ AV_{DD} = 3.3 V).
AV_{SS}	26, 42	I	Analog Supply Return (Ground). AV_{SS} should be connected to DV_{SS} using a conductive trace under, or close to, the AD1989B.

The symbols used in this table are defined as: I = input, O = output, LI = line level input, LO = line level output, HP = output capable of driving headphone load, MIC = input supports microphones with MIC bias and boost amplifier, SWAP = outputs can swap L/R channels (typically used to support C/LFE or shared C/LFE function).

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HD AUDIO WIDGETS

Table 5. HD Audio Widgets[1]

Node ID	Name	Type ID	Type	Description
00	ROOT	x	Root	Device identification
01	FUNCTION	x	Function	Designates this device as an audio codec
02	S/PDIF_1 DAC	0	Audio Output	S/PDIF-1 digital stream output interface
03	DAC_0	0	Audio Output	Headphone/surround side (7.1) channel digital/audio converters
04	DAC_1	0	Audio Output	Stereo front channel digital/audio converters
05	DAC_2	0	Audio Output	Stereo C/LFE channel digital/audio converters
06	DAC_3	0	Audio Output	Stereo surround-back (5.1) channel digital/audio converters
07	S/PDIF ADC	1	Audio Input	S/PDIF digital stream input interface
08	ADC_0	1	Audio Input	Stereo record Channel 1 audio/digital converters
09	ADC_1	1	Audio Input	Stereo record Channel 2 audio/digital converters
0A	DAC_4	1	Audio Output	Stereo surround side (7.1) channel digital/audio converters
0B	S/PDIF_2 DAC	0	Audio Output	S/PDIF-2 output (typically used for HDMI)
0C	ADC Selector 0	3	Audio Selector	Selects and amplifies/attenuates the input to ADC0
0D	ADC Selector 1	3	Audio Selector	Selects and amplifies/attenuates the input to ADC1
0E	ADC Selector 2	3	Audio Selector	Selects and amplifies/attenuates the input to ADC2
0F	ADC_2	3	Audio Input	Stereo record channel 2 audio/digital converters
10	Digital Beep	7	Beep Generator	Internal digital PCBeep signal
11	Port A (Headphone)	4	Pin Complex	Front panel headphone/microphone jack
12	Port D (Front L/R)	4	Pin Complex	Rear panel output/headphone output
13	Mono Out	4	Pin Complex	Monaural output pin (internal speakers or telephony system)
14	Port B (Front Mic)	4	Pin Complex	Front panel microphone/headphone jack
15	Port C (Line In)	4	Pin Complex	Line-in jack (rear or front)
16	Port F (Surr Back)	4	Pin Complex	Rear panel surround-rear (5.1) jack
17	Port E (Rear Mic)	4	Pin Complex	Rear panel mic jack
18	CD In/Line In	4	Pin Complex	Analog CD input or line input
19	Mixer Power Down	5	Power Widget	Powers down the analog mixer and associated amps
1A	Analog PCBeep	4	Pin Complex	External analog PCBeep signal input
1B	S/PDIF Out_1	4	Pin Complex	S/PDIF_1 output pin
1C	S/PDIF In	4	Pin Complex	S/PDIF input pin
1D	S/PDIF Out_2	4	Audio Mixer	S/PDIF_2 output pin
1E	Mono Out Mixer	2	Audio Mixer	Selects which source drives the mono out signal
20	Analog Mixer	2	Audio Mixer	Mixes individually gainable analog inputs
21	Mixer Output Atten	3	Audio Selector	Attenuates the mixer output to drive the port mixers
22	Port A Mixer	2	Audio Mixer	Mixes the Port A Selected DAC and mixer output amps to drive Port A
23	V_{REF} Power Down	F	Vendor Defined	Powers down the Internal and external V_{REF} circuitry
24	Port G (C/LFE)	4	Pin Complex	Rear panel C/LFE jack
25	Port H (Surr Side)	4	Pin Complex	Rear panel surround-side (7.1) jack
26	Port E Mixer	2	Audio Mixer	Mixes DAC4 and mixer output amps to drive Port E
27	Port G Mixer	2	Audio Mixer	Mixes DAC2 and mixer output amps to drive Port G
28	Port H Mixer	2	Audio Mixer	Mixes DAC0 and mixer output amps to drive Port H
29	Port D Mixer	2	Audio Mixer	Mixes DAC1 and mixer output amps to drive Port D
2A	Port F Mixer	2	Audio Mixer	Mixes DAC3 and mixer output amps to drive Port F
2B	Port B Mixer	2	Audio Mixer	Mixes the Port B selected DAC and mixer output amps to drive Port B
2C	Port C Mixer	2	Audio Mixer	Mixes the Port C selected DAC and mixer output amps to drive Port C
2D	Stereo Mix Down	2	Audio Mixer	Mixes the stereo L/R channels to drive mono output
2F	BIAS Power Down	F	Vendor Defined	Powers down the internal MIC_BIAS_FILT and all MIC_BIAS Pins
30	Port B Out Selector	3	Audio Selector	Selects the Port B DAC (0, 1)
31	Port C Out Selector	3	Audio Selector	Selects the Port C DAC (0, 3)
32	Port E Out Selector	3	Audio Selector	Selects the Port E DAC (2, 4)
33	Port C In Selector	3	Audio Selector	Selects from the Port C, G, and H inputs to drive the mixer input
34	Port E In Selector	3	Audio Selector	Selects from the Port E, G, and H inputs to drive the mixer input
36	Mono Out Selector	3	Audio Selector	Selects the mono out DAC (0, 1, 3)

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Table 5. HD Audio Widgets[1] (Continued)

Node ID	Name	Type ID	Type	Description
37	Port A Selector	3	Audio Selector	Selects the Port A DAC (0, 1, 3)
38	Port A Boost	3	Audio Selector	Microphone boost amp for Port A
39	Port B Boost	3	Audio Selector	Microphone boost amp for Port B
3A	Port C Boost	3	Audio Selector	Microphone boost amp for Port C
3C	Port E Boost	3	Audio Selector	Microphone boost amp for Port E
3D	Port D Boost	3	Audio Selector	Microphone boost amp for Port D

[1] All node IDs (NIDs) are sequential in the codec. Any NIDs missing from this table are vendor defined.

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HD AUDIO PARAMETERS

Table 6. Root and Function Node Parameters

Node ID	Name	Vendor ID 00	01	Revision ID 02[1]	03	Sub Node Count 04	Func. Group Type 05	Audio F.G. Caps 08	GPIO Caps 11
00	ROOT	11D4989B		00100300		00010001			
01	FUNCTION					0002003C	00000001	00010C0C	40000003

[1] Subject to change with silicon stepping.

Table 7. SubSystem ID [1]

Node ID	Name	Value	31:16 SSID	15:8 SKU	7:0 ASM ID
01	FUNCTION	BFD80000	BFD8	00	00

[1] The default SSID is overwritten by platform BIOS after power on. It is preserved across HD Audio link reset and verb reset.

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WIDGET PARAMETERS

Table 8. Widget Parameters

Node ID	Widget Capabilities 09	PCM Size, Rate 0A	Stream Formats 0B	Pin Capabilities 0C	Input Amp Capabilities 0D	ConnList Length 0E	Power States 0F	Output Amp Capabilities 12
01	0x0000 0480	0x000E 07FF	0x0000 0001		0x8000 0000		0x0000 0009	0x0005 2727
02	0x0003 0211	0x000E 07E0	0x0000 0005			0x0000 0000		
03	0x0000 0405	0x000E 07FF	0x0000 0001			0x0000 0000	0x0000 0009	0x0005 2727
04	0x0000 0405	0x000E 07FF	0x0000 0001			0x0000 0000	0x0000 0009	0x0005 2727
05	0x0000 0405	0x000E 07FF	0x0000 0001			0x0000 0000	0x0000 0009	0x0005 2727
06	0x0000 0405	0x000E 07FF	0x0000 0001			0x0000 0000	0x0000 0009	0x0005 2727
07	0x0013 0391	0x000E 07E0	0x0000 0005			0x0000 0001		
08	0x0010 0501	0x000E 07FF	0x0000 0001			0x0000 0001	0x0000 0009	
09	0x0010 0501	0x000E 07FF	0x0000 0001			0x0000 0001	0x0000 0009	
0A	0x0000 0405	0x000E 07FF	0x0000 0001			0x0000 0000	0x0000 0009	0x0005 2727
0B	0x0030 0211	0x000E 07E0	0x0000 0005			0x0000 0000		
0C	0x0030 010D					0x0000 0008		0x8005 3627
0D	0x0030 010D					0x0000 0007		0x8005 3627
0E	0x0030 010D					0x0000 0007		0x8005 3627
0F	0x0010 0501	0x000E 07FF	0x0000 0001			0x0000 0001	0x0000 0009	
10	0x0070 000C					0x0000 0000		0x800B 0F0F
11	0x0040 018D			0x0000 373F		0x0000 0001		0x8000 0000
12	0x0040 018D			0x0000 373F		0x0000 0001		0x8000 0000
13	0x0040 010C			0x0000 0010		0x0000 0001		0x8005 1F1F
14	0x0040 018D			0x0000 373F		0x0000 0001		0x8000 0000
15	0x0040 018D			0x0000 3737		0x0000 0001		0x8000 0000
16	0x0040 018D			0x0000 0037		0x0000 0001		0x8000 0000
17	0x0040 098D			0x0000 3737		0x0000 0001		0x8000 0000
18	0x0040 0081			0x0000 0024		0x0000 0000		
19	0x0050 0500					0x0000 0002	0x0000 0009	
1A	0x0040 0000			0x0000 0020		0x0000 0000		
1B	0x0040 030D			0x0000 0010		0x0000 0001		0x8005 2727
1C	0x0040 020B			0x0000 0020	0x8005 1F17	0x0000 0000		
1D	0x0040 030D			0x0000 0010		0x0000 0001		0x8005 2727
1E	0x0020 0103				0x8000 0000	0x0000 0002		
20	0x0020 010B				0x8005 1F17	0x0000 0008		
21	0x0030 010D					0x0000 0001		0x8005 1F1F
22	0x0020 0103				0x8000 0000	0x0000 0002		
23	0x00F0 0100					0x0000 0008		
24	0x0040 098D			0x0000 0037		0x0000 0001		0x8000 0000
25	0x0040 018D			0x0000 0037		0x0000 0001		0x8000 0000
26	0x0020 0103				0x8000 0000	0x0000 0002		
27	0x0020 0103				0x8000 0000	0x0000 0002		
28	0x0020 0103				0x8000 0000	0x0000 0002		
29	0x0020 0103				0x8000 0000	0x0000 0002		
2A	0x0020 0103				0x8000 0000	0x0000 0002		
2B	0x0020 0103				0x8000 0000	0x0000 0002		
2C	0x0020 0103				0x8000 0000	0x0000 0002		
2D	0x0020 0100					0x0000 0001		
2F	0x00F0 0100					0x0000 0006		
30	0x0030 0101					0x0000 0003		
31	0x0030 0101					0x0000 0002		
32	0x0030 0101					0x0000 0002		
33	0x0030 0101					0x0000 0003		
34	0x0030 0101					0x0000 0003		

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Table 8. Widget Parameters (Continued)

Node ID	Widget Capabilities 09	PCM Size, Rate 0A	Stream Formats 0B	Pin Capabilities 0C	Input Amp Capabilities 0D	ConnList Length 0E	Power States 0F	Output Amp Capabilities 12
36	0x0030 0101					0x0000 0003		
37	0x0030 0101					0x0000 0003		
38	0x0030 010D					0x0000 0001		0x0027 0300
39	0x0030 010D					0x0000 0001		0x0027 0300
3A	0x0030 010D					0x0000 0001		0x0027 0300
3C	0x0030 010D					0x0000 0001		0x0027 0300
3D	0x0030 010D					0x0000 0001		0x0027 0300

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CONNECTION LIST

Table 9. Connection List

	Connections		0	1		2		3		4		5		6		7	
Node ID	**[0–3]**	**[4–7]**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**
02																	
03																	
04																	
05																	
06																	
07	0x0000 001C		0x1C														
08	0x0000 000C		0x0C														
09	0x0000 000D		0x0D														
0A																	
0B																	
0C	0x2418 BC38	0x1F20 3D25	0x38	1	0x3C	1	0x18		0x24		0x25		0x3D		0x20		0x1F
0D	0x2418 BC38	0x0020 3D25	0x38	1	0x3C	1	0x18		0x24		0x25		0x3D		0x20		
0E	0x2418 BC38	0x0020 3D25	0x38	1	0x3C	1	0x18		0x24		0x25		0x3D		0x20		
0F	0x0000 000E		0x0E														
10																	
11	0x0000 0022		0x22														
12	0x0000 0029		0x29														
13	0x0000 002D		0x2D														
14	0x0000 002B		0x2B														
15	0x0000 002C		0x2C														
16	0x0000 002A		0x2A														
17	0x0000 0026		0x26														
18																	
19	0x0000 2120		0x20		0x21												
1A																	
1B	0x0000 0002		0x02														
1C																	
1D	0x0000 000B		0x0B														
1E	0x0000 2136		0x36		0x21												
20	0x3D38 3339	0x1A18 3B34	0x39		0x33		0x38		0x3D		0x34		0x3B		0x18		0x1A
21	0x0000 0020		0x20														
22	0x0000 2137		0x37		0x21												
23	0x2524 9811	0x2120 BD38	0x11	1	0x18		0x24	1	0x25		0x38	1	0x3D		0x20		0x21
24	0x0000 0027		0x27														
25	0x0000 0028		0x28														
26	0x0000 2132		0x32		0x21												
27	0x0000 2105		0x05		0x21												
28	0x0000 210A		0x0A		0x21												
29	0x0000 2104		0x04		0x21												
2A	0x0000 2106		0x06		0x21												
2B	0x0000 2130		0x30		0x21												
2C	0x0000 2131		0x31		0x21												
2D	0x0000 001E		0x1E														
2F	0x1514 1211	0x0000 1716	0x11		0x12		0x14		0x15		0x16		0x17				
30	0x0060 0403		0x03		0x04		0x06										
31	0x0000 0A04		0x04		0x0A												
32	0x0000 0405		0x05		0x04												
33	0x0024 253A		0x3A		0x25		0x24										
34	0x0024 253C		0x3C		0x25		0x24										
36	0x0006 0403		0x03		0x04		0x06										

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Table 9. Connection List (Continued)

	Connections		0	1		2		3		4		5		6		7	
Node ID	**[0–3]**	**[4–7]**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**
37	0x0006 0403		0x03		0x04		0x06										
38	0x0000 0011		0x11														
39	0x0000 0014		0x14														
3A	0x0000 0015		0x15														
3C	0x0000 0017		0x17														
3D	0x0000 0012		0x12														

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DEFAULT CONFIGURATION BYTES

In Table 10, default configuration values are set on codec power-up only. Default configuration values are not reset by link or soft reset to preserve modifications by BIOS control.

Table 10. Default Configuration Bytes

		31:30	29:28	27:24	23:20	19:16	15:12	8	7:4	3:0
			Location							
Name	Value	Connectivity	Chassis	Position	Def. Device	Conn Type	Color	JD	Def Assn	Sequence
Port A (Headphone)	0x0221 4030	Jack	External	Front	HP Out	1/8″ Jack	Green	0	3	0
Port D (Front L/R)	0x0101 4010	Jack	External	Rear	Line Out	1/8″ Jack	Green	0	1	0
Mono Out	0x9913 01F0	Fixed	Internal	Special 3	Speaker	ATAPI	Unknown	1	F	0
Port B (Front Mic)	0x02A1 9040	Jack	External	Front	Mic In	1/8″ Jack	Pink	0	4	0
Port C (Line In)	0x0181 3021	Jack	External	Rear	Line In	1/8″ Jack	Blue	0	2	1
Port F (Surr Back)	0x0101 1012	Jack	External	Rear	Line Out	1/8″ Jack	Black	0	1	2
Port E (Rear Mic)	0x01A1 9020	Jack	External	Rear	Mic In	1/8″ Jack	Pink	0	2	0
CD IN/ Line In	0x9933 012E	Fixed	Internal	Special 3	CD	ATAPI	Unknown	1	2	E
Analog PCBeep	0x99F3 01F0	Fixed	Internal	Special 3	Other	ATAPI	Unknown	1	F	0
S/PDIF_1 Out	0x0145 11F0	Jack	External	Rear	S/PDIF Out	Optical	Black	1	F	0
S/PDIF In	0x01C5 11F0	Jack	External	Rear	S/PDIF In	Optical	Black	1	F	0
S/PDIF_2 Out	0x9856 01F0	Fixed	Internal	Special 2	Digital Out	Other Digital	Unknown	1	F	0
Port G (C/LFE)	0x0101 6011	Jack	External	Rear	Line Out	1/8″ Jack	Orange	0	1	1
Port H (7.1)	0x0101 2014	Jack	External	Rear	Line Out	1/8″ Jack	Grey	0	1	4

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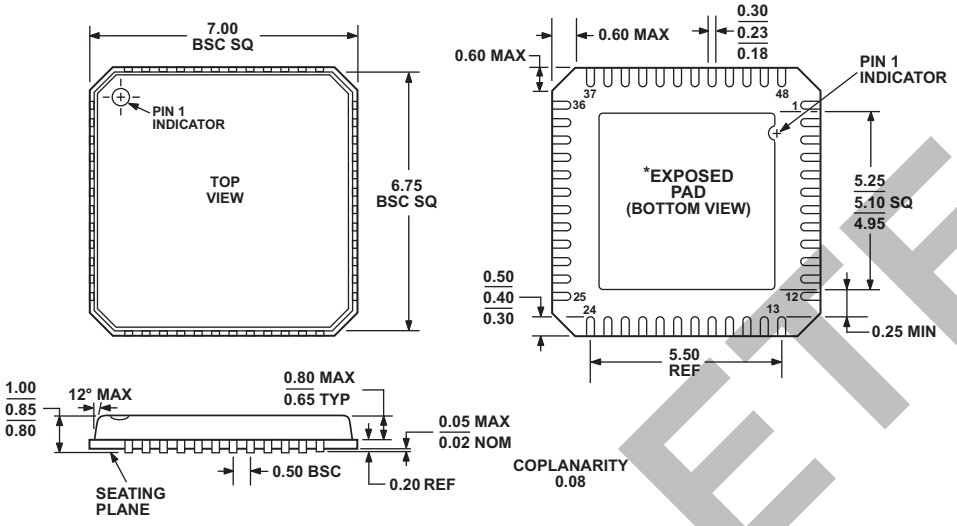
OUTLINE DIMENSIONS

Dimensions are shown in millimeters.



*NOTE:
THE EXPOSED PAD IS REQUIRED TO BE ELECTRICALLY AND THERMALLY CONNECTED TO VSS. THIS SHOULD BE IMPLEMENTED BY SOLDERING THE EXPOSED PAD TO A VSS PCB LAND THAT IS THE SAME SIZE AS THE EXPOSED PAD. THE VSS PCB LAND SHOULD BE ROBUSTLY CONNECTED TO THE VSS PLANE IN THE PCB WITH AN ARRAY OF THERMAL VIAS FOR BEST PERFORMANCE.

Figure 3. 48-Lead, Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm ×7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters

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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1989BJCPZ[1]	0°C to 70°C	48-Lead LFCSP_VQ	CP-48-1
AD1989BJCPZ-RL[1]	0°C to 70°C	48-Lead LFCSP_VQ, 13" Tape and Reel	CP-48-1

[1] Z = RoHS Compliant Part.

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