Product Bulletin

Spread Spectrum Processor with Medium Access Control

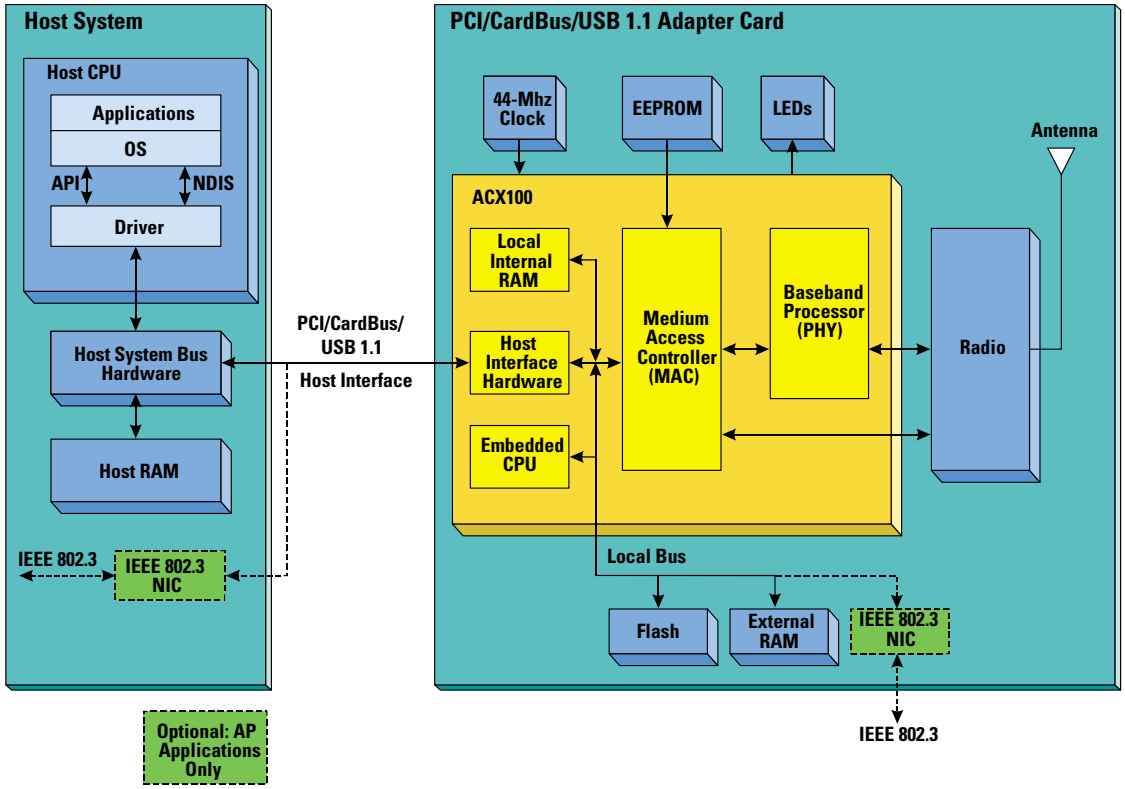
Key Benefits

- Data rates: 1, 2, 5.5, 11, and 22 Mbit/s
- Embedded ARM® 7TDMI CPU and RAM
- Supports all IEEE 802.11b modulations
- Supports CardBus, PCI, and USB 1.1 interfaces
- Supports multiple radio topologies
- Targets Wi-Fi™ systems compliance
- Processing gain up to 15 dB
- Multipath delay spread tolerance > 250 ns
- Supports JTAG boundary scan

The ACX100 single-chip wireless local area network (WLAN) medium access controller (MAC) with an IEEE 802.11b-compliant spread spectrum baseband processor from Texas Instruments combines high-performance with robust functionality. In addition to the MAC and baseband processor, the ACX100 integrates an ARM® 7TDMI RISC processor, as well as host and baseband interfaces. The ACX100 directly interfaces to a host and radio to provide a complete high-speed networking solution for OEM WLAN system providers.

The ACX100 complies with Wireless Ethernet Compatibility Alliance specifications to enhance and maintain Wi-Fi™ compliance in WLAN systems. The processor supports typical applications such as:

- CardBus/PCI/mini-PCI WLAN adapters
- High-speed WLAN access points
- High-speed WLAN bridges
- 2.4-GHz WLAN systems
- Portable notebook/PDA computer links
- Part 15-compliant radio links
- Portable bar code scanners/POS terminals.



ACX100 System Block Diagram

The IEEE 802.11-compliant MAC supports high data rates by implementing real-time functions in hardware. The embedded ARM 7TDMI RISC processor manages the host interface in addition to other high level functions. The ARM 7TDMI can also override many hardware functions.

The ACX100 host interface directly supports 32-bit CardBus and PCI interfaces. For added flexibility in host connectivity, the ACX100 also supports USB 1.1 interfaces. In access point (AP) applications, the ACX100 supports IEEE 802.3 network interface cards (NIC) for Ethernet connectivity.

The host interface supports DMA transfers between host memory and ACX100 embedded RAM in ACX100 master and slave modes. The ACX100 features embedded RAM for code execution and data buffering. It dynamically allocates transmit and receive memory for efficient memory usage. The MAC/baseband hardware parses received frames independently of the embedded CPU. An external memory interface supports additional RAM and Flash devices.

The MAC hardware can directly generate ACK, RTS, CTS, probe response and beacon packets. It also provides wired equivalent privacy (WEP). The MAC can perform encryption and decryption on frames using keys of up to 256 bits in length.

The ACX100 radio interface includes dual 8-bit, 22-MHz analog-to-digital converters (ADC) for the I and Q receive inputs, as well as dual 10-bit, 44-MHz digital-to-analog converters (DAC) for the I and Q transmit outputs. The radio interface also features transmit gain control and receive automatic gain control (AGC), which are programmable and support a variety of 2.4-GHz radios. The ACX100 receiver also implements antenna diversity and performs clear channel assessment (CCA).

While operating under dense multipath or noisy environments, the baseband receiver increases performance by means of sophisticated decoding algorithms that minimize the need for retransmission. The ACX100 has a multipath delay spread tolerance greater than 250 ns.

TI provides two package options for the ACX100: 208-pin Plastic Quad Flat Pack (PQFP) and the 257-pin BGA. The ACX100 requires supply voltages of 1.8 V and 3.3 V, and features 3.3-V tolerant I/Os. The ACX100 also provides 16 general-purpose I/Os for interfacing flexibility.

Setting the high-performance standard

Texas Instruments' enhancement of the IEEE 802.11b standard delivers the most aggressive data rates available in the 2.4 GHz WLAN market. By employing advanced forward error correction (FEC) and modulation techniques, the ACX100 achieves much higher performance levels than competing solutions. The ACX100's proprietary application of Packet Binary Convolutional Code (PBCC™) technology provides data rates up to 22 Mbit/s in 8.5 dB of signal-to-noise response (SNR) with a packet error rate (PER) of 10^{-2}.

ACX100 Performance

Data Rate (Mbit/s)	Modulation	SNR (dB)
1	Barker	0
2	Barker	3
5.5	CCK	5.5
	PBCC	1.5
11	CCK	8.5
	PBCC	4.5
22	PBCC	8.5

The ACX100 is compatible with existing 1- and 2-Mbit/s IEEE 802.11 direct sequence products. In addition to 5.5-, 11-, and 22-Mbit/s PBCC modes, the ACX100 operates at 5.5 and 11 Mbit/s in Complementary Code Keying (CCK) modes. The ACX100 supports long and short physical layer convergence protocol (PLCP) preambles according to the IEEE 802.11b high-rate specification.

The ACX100 PBCC modes require 4 dB less SNR in AWGN than the CCK modes to achieve a PER of 10^{-2}. The PBCC modes essentially double the data rates of the CCK modes at any noise or multipath distortion level.

For more information

For more information on how the ACX100 can give you a competitive advantage in your market, visit our web site at:
www.ti.com/sc/wirelessnetworking

TEXAS INSTRUMENTS