PLX Technology

Hardware Reference Manual

PEX8605-AIC Rapid Development Kit

Preface

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About This Manual
This document describes the PLX PEX8605-AIC RDK, a Rapid Development Kit, from a hardware perspective. It contains a description of all major functional circuit blocks on the board and also is a reference for the creation of software for this product. This manual also includes complete schematics and bill of materials.

Revision History

Date	Version	Comments
August 2011	1.0	Initial Release

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1 General Information

The PEX8605 RDK is a PLX Rapid Development Kit intended primarily for use by PLX customers for silicon evaluation and design reference. The form factor is based on the PCI Express Card Electromechanical specification. The board is designed to work by plugging internally into a PCI Express compliant motherboard. Figure 1 shows the board outline and component placement.

The PEX8605 RDK has 1 x4 upstream port connector and 3 x16 PCIe connectors. The upstream edge connector has 1 or 2 PCIe Gen2 lanes electrically connected to it, and the downstream PCIe connectors have 1 PCIe Gen2 lane each electrically connected to it depending on the installed configuration module.

The PEX8605 RDK supports the use of one configuration module slot to provide flexibility in the routing of PCIe lane 1 to either the x4 PCIe edge connector or to one of the PCIe slots. The Configuration Module enables the RDK to support the following port configurations:

Table 1. PEX8605 Port Configurations

PEX 8605	Port Configuration
0h	x1, x1, x1, x1
1h	x2, x1, x1

The PEX8605 RDK meets the ROHS guidelines for electronic components, and hardware.

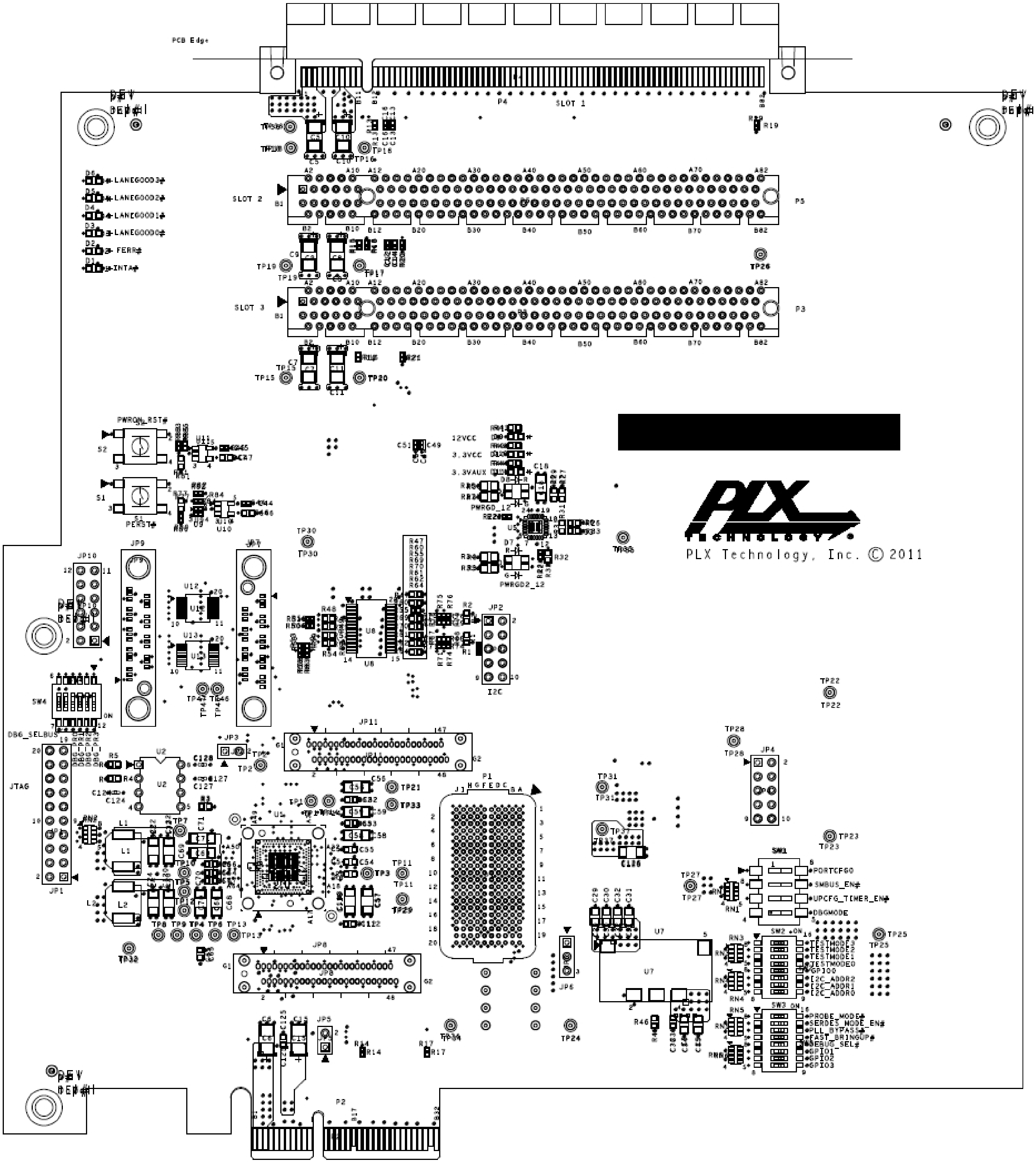

Figure 1. PEX8605 RDK Front View

1.1 PEX8605 Features

The PEX 8605 supports the following features:

- 4-Port PCI Express switch
  - 4 Lanes with integrated on-chip SerDes
  - Low-power SerDes (under 90 mW per Lane)
  - Fully Non-Blocking Switch architecture
  - Port configuration
    - 4 independent Ports
    - Choice of Link width (quantity of Lanes) per unique Link/Port (x1, x2)
    - Configurable with serial EEPROM or I2C
- High Performance
  - Full line rate on all Ports
  - Cut-Thru packet latency of less than 250 ns between symmetric (x1 to x1)
  - Maximum Payload Size – 256 bytes
- Quality of Service (QoS) support
  - All Ports support one, full-featured Virtual Channel (VC0)
  - All Ports support eight Traffic Class (TC[7:0]) mapping, independently of the other Ports
  - Weighted Round-Robin (WRR) Port arbitration
- Reliability, Availability, Serviceability (RAS) features
  - Electromechanical Interlock supported with Power Enable output
  - Baseline and Advanced Error Reporting capability
  - JTAG AC/DC boundary scan
- INTA# (PEX_INTA#) and FATAL ERROR (FATAL_ERR#) (Conventional PCI SERR# equivalent) pin support
- 4 General-Purpose Input/Output (GPIO) pins, which can be used for Link Status LEDs, GPIOs, and/or Interrupt inputs
- Other PCI Express Capabilities
  - Transaction Layer Packet (TLP) Digest support for Poison bit
  - Lane reversal (Port 0 only, when Port 0 is configured with a x2 Link width)
  - Polarity reversal
  - Conventional PCI-compatible Link Power Management states
    - L0, L0s, L1, L2, and L2/L3 Ready
    - L3 (with Vaux supported)
  - Conventional PCI-compatible Device Power Management states
    - D0, D1, D2, and D3hot
    - D3cold (with Vaux supported)
  - Active State Power Management (ASPM)
  - Dynamic speed (2.5 or 5.0 GT/s) negotiation
  - Dynamic Link-width negotiation
- Out-of-Band Initialization options

  - Serial EEPROM
  - I2C and SMBus (7-bit Slave address with 100 Kbps)
- Testability – JTAG support for DC
- 10 x 10 mm2, 136-pin Dual-Row QFN package
- Typical power – 0.8W

1.2 PEX8605 AIC RDK Features

- PEX8605-AA PCI Express 4-port Gen 2 PCIE Switch
- X4 Upstream goldfinger
- Three downstream PCI Express x16 Slot Connectors
- DIP Switches for hardware configuration of PEX8605
- Socketable Serial EEPROM
- Manual push-button PERST# capability
- I2C /SMBus header for Out-of-Band register access
- JTAG header for testability

1.3 Getting Started

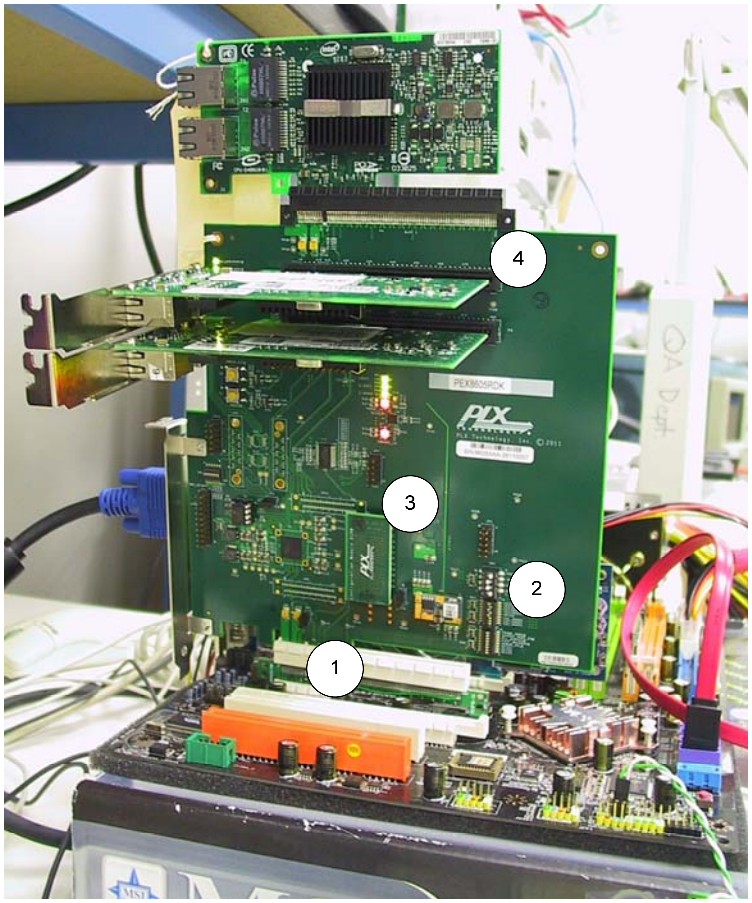

Figure 2. Getting Started

Follow the following steps to use the RDK.

1) Plug board into x16 PCI Express slot on motherboard.
2) Check and set dipswitches for desired port configuration.
3) Check that the correct configuration module is plugged into the socket.
4) Plug in PCI Express endpoints into downstream slots.

After all these steps are completed, system can be powered on.

2 PEX8605 RDK Hardware Architecture

2.1 Architecture Block Diagram

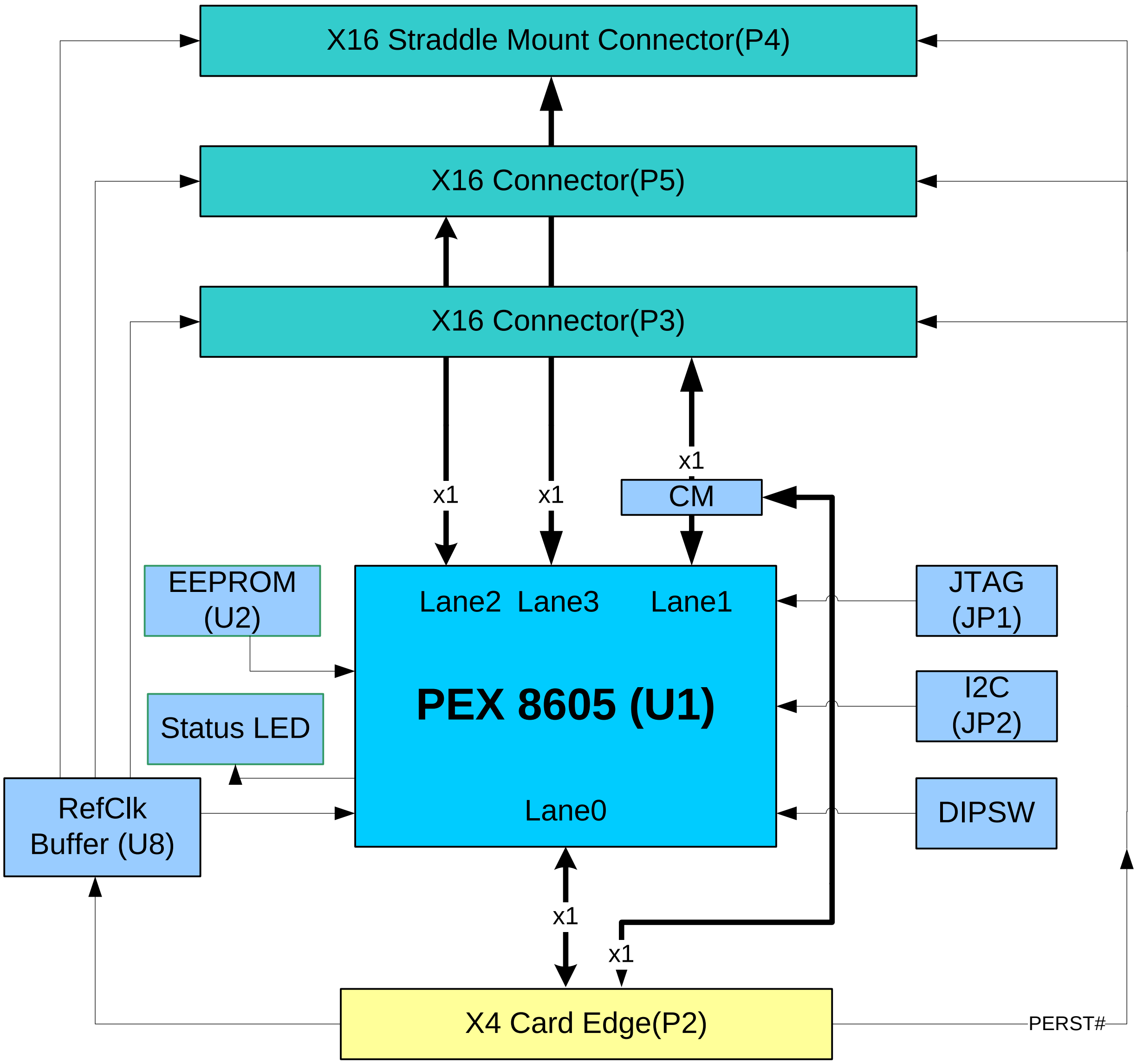

Figure 3. RDK Architecture

2.2 Board Components

(Refer to Figure 4. RDK Component Locations)

Table 2 Component Table

Component	Location	Component	Location
PCI Express Slots (P3,P4, P5)	1	JTAG connector (JP1)	8
Lane Good LEDs (D3,D4,D5,D6)	2	PEX8605 Chip (Chip not installed in diagram) (U1)	9
Power-on Reset Button (S2)	3	PCIE Goldfinger (P2)	10
PERST# Button (S1)	4	Voltage Indicator LEDs (D9,D10,D11)	11
I2C Connector (JP2)	5	Configuration Dipswitches (SW1-SW4)	12
EEPROM Enable Jumper (JP3)	6	Configuration Module Socket (P2)	13
EEPROM Chip with Socket (U2)	7		

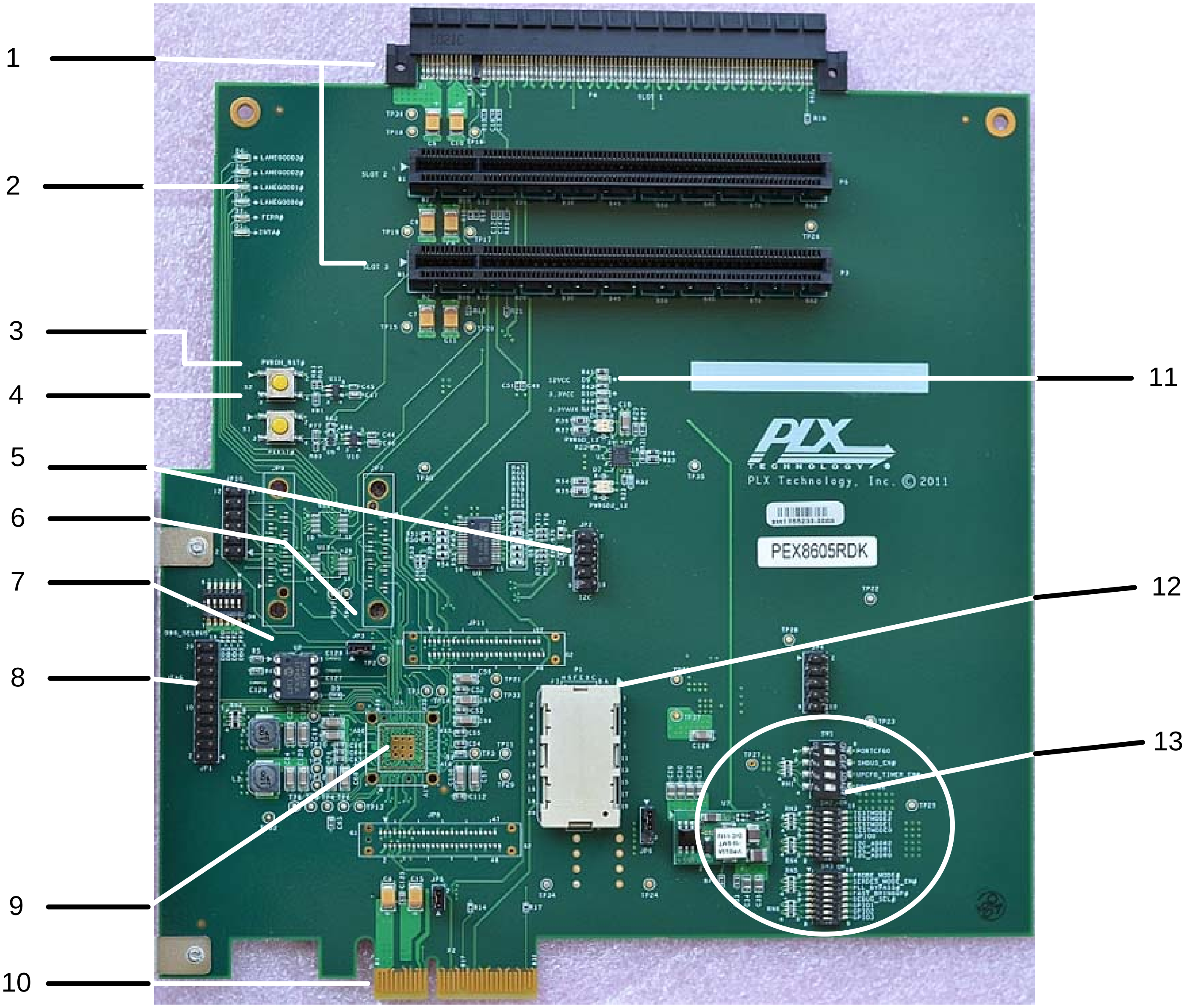

Figure 4. RDK Component Locations

2.3 PEX8605 PCI Express Switch

The PEX8605 is a 4-lane, 4-port PCIe Gen2 switch. It comes in a 10x10mm^2 136-lead QFN package.

2.4 PCI Express Upstream Port Connection

The upstream x4 connector can be configured as a x1 or x2 link connecting the PEX8605 to the add-in card male edge connector. The PEX8605 RDK can plug into x1 PCI Express slots by using a PCI Express lane converter, such as PCI Express X4-To-X1 Converter made by Adex Electronics.

2.5 PCI Express Downstream Port Connections

The PEX8605 RDK has 3 x16 type PCIe connectors. Slot 3 can be connected to lane 1 in the x1x1x1x1 port configuration.

2.6 Hardware Strap Pin Dipswitches

The PEX8605 has a number of strap pins which provide the capability to perform various types of hardware initialization without the use of EEPROM. There are two main types of switches. The extended actuator dipswitches contain the main configuration dipswitches and the recessed switches control more advanced and RESERVED functions.

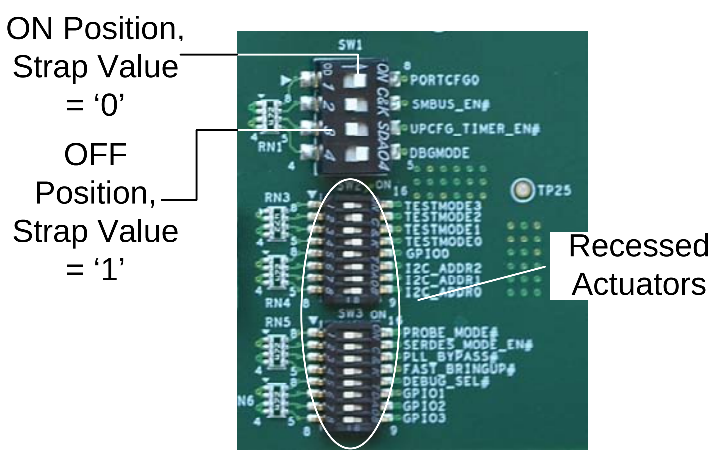

Figure 5. Configuration Dipswitches

2.7 Dipswitch Setting Tables

Dipswitches are designed such that the "ON" state selects a value of '0' for that switch.

Table 3. SW1 Functions

SW1 Functional Description	Switch Position Settings
PORTCFG0 Used to select the PEX8605's Port configuration.	L = x1 x1 x1 H = X2 x1 Default Setting = L
SMBUS_EN# System Management Bus Enable	L = Enables SMBUS Mode H = Enables I^2C Mode Default Setting = H
UPCFG_TIMER_EN# Link Upconfigure Timer Enable	L = If Link training sequence fails during the *Configuration* state, the next time the LTSSM exits the *Detect* state, TS Ordered-Sets advertise only the 2.5 GT/s (Gen 1) data rate and no Autonomous Change support. If Link training continues to fail when the LTSSM is in the *Configuration* state, the LTSSM continues to alternate between Gen 1 and Gen 2 advertisement every time it exits the *Detect* state H = The Data Rate Identifier symbol in the TS Ordered-Sets always advertises support for both the 5.0 GT/s (Gen 2) data rate and Autonomous Change. Default Setting = H
DBGMODE *Factory Test Only*	Default Setting = L

Table 4. SW2 Functions

SW2 Functional Description	Switch Position Settings
TESTMODE[3:0] *Factory Test only*	Default Setting = HLHL
GPIO0 *Factory Test Only*	Default Setting = H
I²CADDR[2:0] I²C Lower Slave Address Bits	Used to define the default value of the three least significant bits of the PEX8605 I2C/SMBus 7-bit Slave address. Default Setting = LLL

Table 5. SW3 Functions

SW3 Functional Description	Switch Position Settings
PROBE_MODE# *Factory Test Only*	Default Setting = H
SERDES_MODE_EN# *Factory Test Only*	Default Setting = H
PLL_BYPASS# *Factory Test Only*	Default Setting = H
FAST_BRINGUP# *Factory Test Only*	Default Setting = H
DEBUG_SEL# *Factory Test Only*	Default Setting = H
GPIO1-3 *Factory Test Only*	Default Setting = HHH

Table 6. SW4 Functions

SW4 Functional Description	Switch Position Settings
DBG_PRBSEL[3:0] *Factory Test Only*	Default Setting = HHHH
DBG_SELBUS *Factory Test Only*	Default Setting = H

2.8 Power Circuitry

The PEX8605 RDK is a PCI Express add-in card. All power to the on-board components, including the downstream ports, come directly from the male card edge +12VDC and +3.3VDC.

There are two DC/DC converters powering the 1.0V SerDes digital and Core Logic supply as well as the Auxiliary Core supply voltages to the PEX8605 device. There are also two DC/DC converter powering the 2.5V SerDes analog and I/O supply as well as the Auxiliary I/O supply voltages to the PEX8605 IO cells. and other onboard components for IO voltage conversion.

Voltage monitoring circuits are placed close to the PEX8605 chip. If the supplies are off 10% of their normal values, red LED(s) will be turned on to signal the potential voltage problem to the chip. Bypass capacitors, plane capacitors are used to filter out the voltage noise.

2.9 Serial EEPROM Interface

The PEX8605 RDK provides a socketed Serial EEPROM. The contents of the serial EEPROM are used to initialize the PEX8605 after power-on reset. The RDK contains a Microchip 25AA128 128K serial EEPROM device.

Note the EEPROM device orientation as shown below.

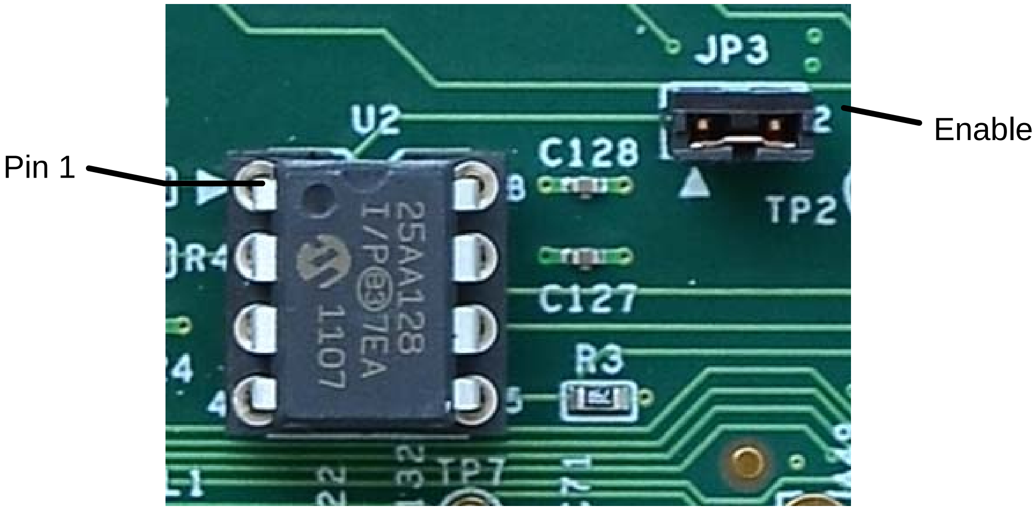

Figure 6. EEPROM in Socket

2.10 JTAG Interface

The PEX8605 RDK contains a dedicated 2x10 JTAG header (JP2). There is no “standard” JTAG header pin arrangement; therefore, JTAG header type and pin assignments are somewhat arbitrary. The header and pin assignment chosen for this board is compatible with the Scanworks USB-100 JTAG controller).

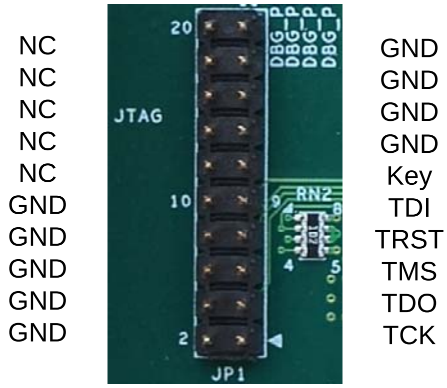

Figure 7. Pin Assignment of JTAG Port Header, JP1

2.11 I2C/SMBUS Interface

The PEX8605 provides a two-wire I2C/SMBus compatible slave mode interface with three bit addressing. Through this out-of-band channel, the users can read, write, and configure the PEX8605 internal registers, run internal output probe mode, monitor error counters, and monitor status of all ports.

The PEX8605 RDK provides a 10 pin I2C header (JP2). The pin header included is compatible with the Aardvark I2C/SPI Host Adapter Part Number: TP240141 by TotalPhase.

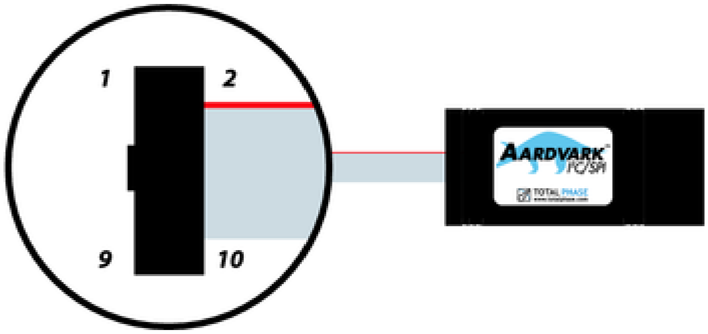

Figure 8. I2C Plug Orientation

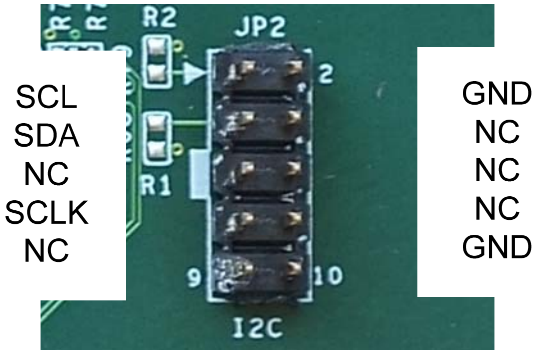

Figure 9. Pin Assignment of I2C Connector JP2

2.12 FATAL_ERR#, and INTA#

The PEX8605 RDK device has a number of chip-specific side band signals that are intended for various uses. The FATAL_ERR# output is used to indicate that the PEX8605 device detected a fatal unrecoverable error. The INTA# output is used to be compatible with PCI. The FATAL_ERR# shall also drive a red LED indicator, and the INTA# signal shall drive an amber colored LED indicator.

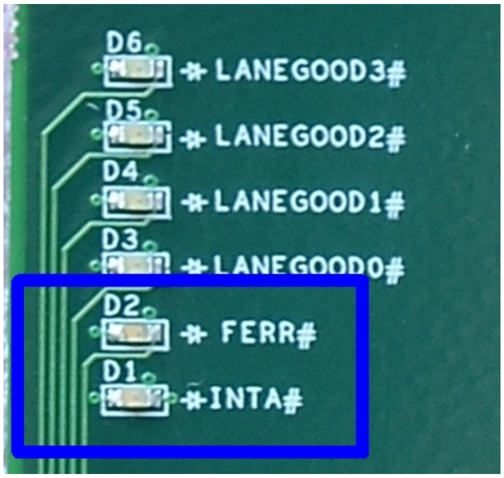

Figure 10. Fatal Error and INTA# LEDs

2.13 Reference Clock Circuitry

The PEX8605 RDK uses the RefClk provided at the male add-in card edge connector. This clock goes through a clock fan-out buffer circuit and provides the Refclk to the 3 downstream connectors and the PEX8605.

2.14 Reset Circuitry

The reset circuit of PEX8605 RDK contains a two input AND gate and a reset chip. The PERST# from the PCI Express male connector and the manual reset from the pushbutton switch input to the AND gate and the output of the AND gate is fed into the reset chip. The PERST# button (S1) and the PWRON_RST# button (S2) are shown below:

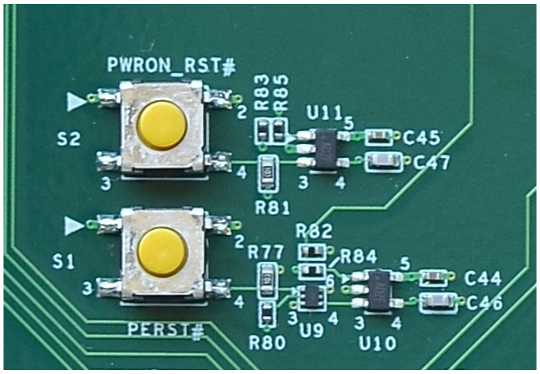

Figure 11. Manual PERST# button

2.15 Port Good Indicator LEDs

Each PCIe port has a port status indicator associated with it. They are grouped in the upper-left corner of the board for easily visibility. The port indicator LED is either on, off, or flashing to indicate the link status. These states are shown in the table below. The RDK has a total of 4 LED indicators for Port 0-3.

Figure 12 Lane Good LEDs

Table 7. Port Indicator Blink Pattern

Link State	LED Pattern
Link Down	OFF
Link Up; GEN2	ON
Link Up; GEN1	Blinking: 0.5 sec ON, 0.5 sec OFF

2.16 PCIe Protocol Debug

All PCIe Lanes pass through an Agilent soft touch midbus probe footprint in order to monitor PCIe traffic.

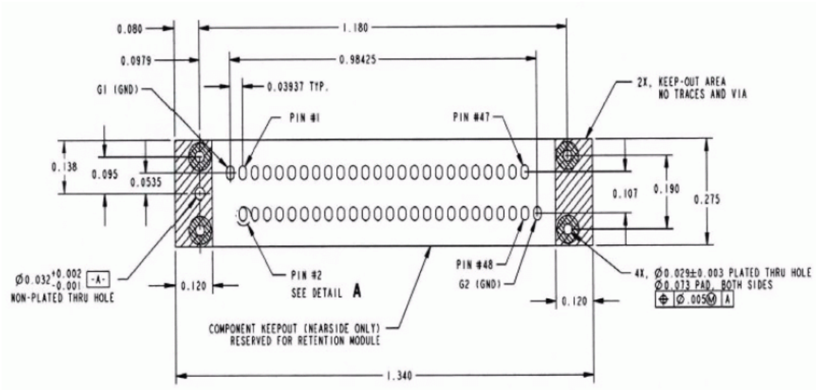

Figure 13: Midbus 2.0 Probe Footprint

2.17 WAKE# and Vaux Support

The Wake# signals will be connected together and Vaux will be routed from the upstream port to all downstream slots.

3 RDK Configurations

The PEX8605 RDK can be configured to operate in one of several modes as described in this section. The modes can be entered by changing jumpers and configuration modules. The configuration modules control the routing of the PCIE lanes and Refclk, and the strap pin dipswitches configures the modes of the PEX8605.

3.1 Default Strap Pin Settings Diagram

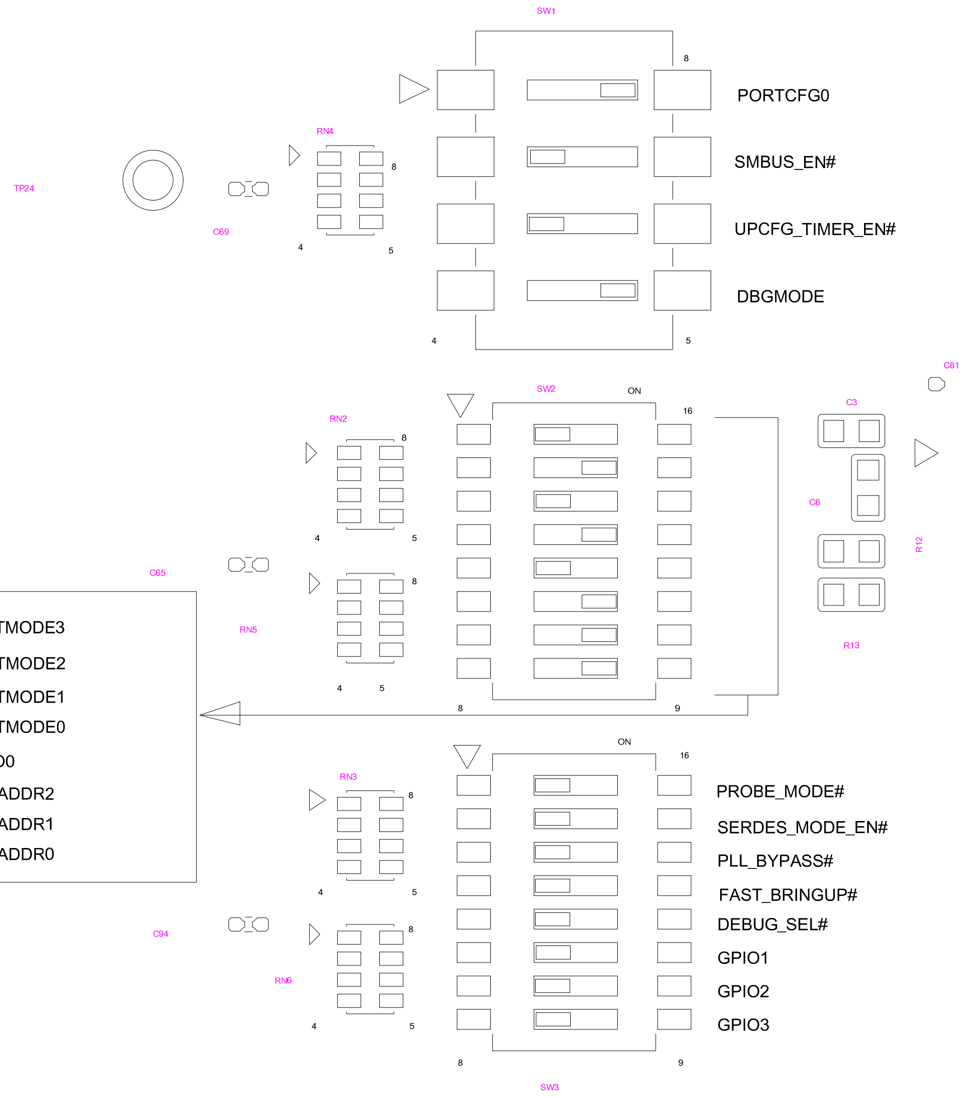

Figure 14. Default Dipswitch Settings

3.2 Hardware Strap Pins

The PEX8605 RDK has a number of strap pins which provide the capability to perform various types of hardware initialization without the use of EEPROM. Table 9 shows the port configuration strap pin values.

Table 8. PEX8605 StrapPortCfg Settings

PEX8605 StrapPortCfg Options				
StrapPortCfg	**port 0**	**port 1**	**port 2**	**port3**
0.default	**x1**	**x1**	**x1**	**x1**
1	**x2**		**x1**	**x1**

3.3 Configuration Modules

Table 9. Configuration Module Description

Configuration Module	Goldfinger	Slot1	Slot2	Slot3
CM107	x2	x1	x1	n/a
CM108	x1	x1	x1	x1

3.4 Hardware Jumpers

The PEX8605 RDK has a few jumper settings for testing purposes. These can be left at their default settings, as detailed below:

Table 10. PEX8605 RDK Jumper Settings

Jumper	Default Setting	Description
JP3	ON	Connects the EE_CS# signal of the PEX8605 to the EEPROM.Can be used to disable the EEPROM for testing.
JP6	2-3	1-2 : Connects the 3.3Vaux power rail to the 3.3VCC power coming from the PCIE slot. 2-3: Connects the 3.3Vaux power rail to the 3.3Vaux power coming from the PCIE slot. (Default setting)