VT8501

Apollo MVP4

66 / 100 MHz
Single-Chip Socket-7 / Super-7 North Bridge with PCI System Bus, Integrated AGP 2D / 3D Graphics Accelerator and Advanced ECC Memory Controller supporting PC100 SDRAM, Virtual Channel SDRAM, EDO, and FPG DRAM

Revision 1.3
February 1, 2000

VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
0.1		Initial internal release based on Apollo MVP3 specification & Porsche HRM	GH
0.2		Updated/corrected signal list; added power signal detail, corrected misc features	GH
0.3		Added FP description, AC/DC tables, pin placement diagram; Fixed misc typos	GH
0.4	7/298	Reconciled with target spec: changed pinouts & poweron config, added registers	EC
0.5	7/27/98	Changed pinout; added pin descriptions; changed p/n to VT82C501; reformatted	DH
0.6	8/21/98	Changed pinouts TVD[0-2], TVHS, TVCLK per 7/30/98 rev 1.1 ballout Changed PD[9-11,13-14,18-19], TVD[0-2,6-7], VIDCLK per 8/13, 1.3 ballout Changed name of REQ4# / GNT4# to REQX# / GNTX# to match VT82C231 Added VGA and Graphics Accelerator registers	DH
0.7	8/24/98	Added remaining Graphics Engine registers	DH
0.8	9/11/98	Changed pinouts to match internal pinout document revision 1.5: HCLK, MCLKI, MCLKO, GNDA, VCC2A, MD16-28, MD50-60	DH
0.9	10/15/98	Updated Feature Bullets Changed pins F1, G1, G3, N2, and N4 to “Reserved, Do Not Connect” Changed ADS#, M/IO#, W/R#, D/C#, BE[7-0]# to inputs, BRDY# to output Added descriptions to VLF1 and VLF2 pins Changed VSUS2 and VSUS3 to VSUS and corrected description Changed VCC2 definition to 2.5V Updated Register Definitions: - Device 0 Rx68[1-0] changed; Rx78[5] & Rx88[0] reserved; Rx79 added - Device 1 Rx41[1] reserved, Rx42[2] changed - Default values added to 3D8, GR5, E-F, 20-22, 24-28, 2A, 2C, 2F, SR8-9, B-12, 18-1B, 20-21, 24, 37-38, 96-99, 9E, BE, CE, and CR0-18, 1A-1C, 20, 21, 25, 27-2F, 34-3C, 52, 55, 56, 5E, 5F, 62, & 63 - CR11[6] reserved, CR17[4] extended function added, SRC[6] note added, SRD[3].new reserved, SRD[7-4].new redefined, SR12[7-4, 3-0] redefined, SR16-17 removed, CR1A-1C redefined, CR28/2C/2E deleted, CR2A[3-2] reserved, CR62[3-0] redefined Updated Functional Descriptions: corrected DFP config & deleted test modes	DH
0.91	10/21/98	Changed power / ground pin names to match design guide Replaced ENPVDD (F1) and ENPVEE (G1) required for DFP interface Moved CKE functions from MECC to RAS4-5#, SRASC#, SCASC# Fixed error in numerical pin list AD15-AD18 Updated block diagram	DH
0.92	11/4/98	Changed part # to VT8501, changed VT82C686 to 686A & VT82C596 to 596A Updated register definitions: Device 0 Rx51[4], 52[3,1], 53[3-0], 59-58[15-13], MA Mapping Table, 69[7], 6B[3-1], 6C[7,3], 6D[4], 70[5,0], 73[4], 74[4-0], 76[3-0], 78[2], 79[7-0], 88[2], AC[6-4,0], AD, F0-FF, Device 1 Rx41[0], 42[3-2]; Fixed Device 1 bus #	DH
1.0	12/9/98	Fixed typographical error in pin lists: VCC3 pin # was W7, should be W21	DH
1.1	6/1/99	Fixed miscellaneous typographical errors and updated feature bullets Changed defaults for Device 0 RxAC and RxAD Changed device 0 Rx6[6], 52[3], 69[1] (VGA Ena Guard Bit), 79[1-0], FB[7] Added missing device 1 registers Rx43, 44, and 47-46	DH
1.2	10/8/99	Fixed Bus 0 Device 1 Rx7-6[13-12] changed from WC to RO Fixed Bus 1 Device 0 Rx3-0 Vendor & Device ID	DH
1.3	2/1/00	Added DSTN panel tables in intro/overview; added note to Device 0 Rx78[6] Updated document logos; fixed ambient/case temp specs	DH

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66 / 100 MHz
Single-Chip Socket-7 / Super-7 North Bridge
with PCI System Bus,
Integrated AGP 2D / 3D Graphics Accelerator
and Advanced ECC Memory Controller
supporting PC100 SDRAM,
Virtual Channel SDRAM, EDO, and FPG DRAM

- **General**
  - 492 BGA Package (35mm x 35mm)
  - 2.5 Volt +/- 0.2V Core
  - Supports separately powered 3.3V tolerant interface to CPU and Memory
  - Supports separately powered 5.0V tolerant interface to PCI bus and Video interface
  - 2.5V, 0.25um, high speed / low power CMOS process
  - PC-98/99 compatible using VIA VT82C686A (352-pin BGA) south bridge chip
  - 66 / 100 MHz Operation

CPU	Internal AGP	DRAM / VGC	PCI	Comments
100 MHz	66 MHz	100 MHz	33 MHz	synchronous (DRAM uses CPU clock)
66 MHz	66 MHz	66 MHz	33 MHz	synchronous (DRAM uses CPU clock)
66 MHz	66 MHz	100 MHz	33 MHz	Up pseudo-synchronous (DRAM uses MEM clock)

- **Socket 7 Host Interface**
  - Supports all Socket-7 / Super-7 processors including 64-bit Intel Pentium™ / Pentium™ with MMX™ , AMD 6K86™ (K6™ and K6-2™), Cyrix/IBM 6x86™ / 6x86MX™ , IDT/Centaur C6, and Rise MP6 CPUs
  - 66 / 100 MHz CPU “Front Side Bus”
  - Supports 3.3V and sub-3.3V interface to CPU
  - Built-in de-skew PLL (Phase Lock Loop) circuitry for optimal skew control within and between clocking regions
  - Cyrix/IBM 6x86™ linear burst support
  - AMD K6™ and K6-2™ write allocation support
  - Supports CPU-to-DRAM write combining
  - System management interrupt, memory remap and stop clock mechanisms

- **Advanced L2 Cache**
  - Direct map write-back or write-through secondary cache
  - Pipelined burst synchronous SRAM (PBSRAM) cache support
  - Flexible cache size: 0K / 256K / 512K / 1M / 2MB
  - 32 byte line size to match the primary cache
  - Integrated 8-bit tag comparator
  - 3-1-1-1-1-1-1-1 back to back read timing for PBSRAM accesses up to 100 MHz
  - Tag timing optimized (less than 4ns setup time) to allow external tag SRAM implementation for most flexible cache organization
  - Sustained 3 cycle write access for PBSRAM access or CPU to DRAM & PCI bus post write buffers up to 100 MHz
  - Supports CPU single read cycle L2 allocation
  - System and video BIOS cacheable and write-protect
  - Programmable cacheable region
- **Internal Accelerated Graphics Port (AGP) Controller**
  - AGP v2.0 compliant for 1x and 2x transfer modes
  - Pipelined split-transaction long-burst transfers up to 533 MB/sec
  - Eight level read request queue
  - Four level posted-write request queue
  - Thirty-two level (quadwords) read data FIFO (128 bytes)
  - Sixteen level (quadwords) write data FIFO (64 bytes)
  - Intelligent request reordering for maximum AGP bus utilization
  - Supports Flush/Fence commands
  - Graphics Address Relocation Table (GART)
  - One level TLB structure
  - Sixteen entry fully associative page table
  - LRU replacement scheme
  - Independent GART lookup control for host / AGP / PCI master accesses
  - Windows 95 OSR-2 VXD and integrated Windows 98 / NT5 miniport driver support
- **Concurrent PCI Bus Controller**
  - PCI bus is synchronous / pseudo-synchronous to host CPU bus
  - 33 MHz operation on the primary PCI bus
  - Supports up to five PCI masters
  - Peer concurrency
  - Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
  - Zero wait state PCI master and slave burst transfer rate
  - PCI to system memory data streaming up to 132Mbyte/sec
  - PCI master snoop ahead and snoop filtering
  - Six levels (double-words) of CPU to PCI posted write buffers
  - Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
  - Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
  - Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
  - Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
  - Supports L1/L2 write-back forward to PCI master read to minimize PCI read latency
  - Supports L1/L2 write-back merged with PCI master post-write to minimize DRAM utilization
  - Delay transaction from PCI master reading DRAM
  - Read caching for PCI master reading DRAM
  - Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
  - Symmetric arbitration between Host/PCI bus for optimized system performance
  - Complete steerable PCI interrupts
  - PCI-2.2 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

- **High-Performance DRAM Controller**
  - 64-bit DRAM interface synchronous with host CPU (66//100 MHz) or internal Memory Clock (100 MHz)
  - Concurrent CPU and AGP access
  - Supports both standard PC100 and "Virtual Channel" PC100 SDRAMs as well as FPG and EDO DRAMs
  - Different DRAM types (FPG, EDO, and SDRAM) may be used in mixed combinations
  - Different DRAM timing for each bank
  - Dynamic Clock Enable (CKE) control for SDRAM power reduction
  - Mixed 1M / 2M / 4M / 8M / 16MxN DRAMs
  - 6 banks up to 768MB DRAMs
  - Flexible row and column addresses
  - 64-bit data width only
  - 3.3V DRAM interface
  - Programmable I/O drive capability for MA, command, and MD signals
  - Optional bank-by-bank ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
  - Two-bank interleaving for 16Mbit SDRAM support
  - Two-bank and four bank interleaving for 64Mbit SDRAM support
  - Supports maximum 8-bank interleave (i.e., 8 pages open simultaneously); banks are allocated based on LRU
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
  - Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers
  - Four quadwords of CPU/cache to DRAM read prefetch buffers
  - Concurrent DRAM writeback
  - Read around write capability for non-stalled CPU read
  - Burst read and write operation
  - 5-2-2-2-2-2-2-2 back-to-back accesses for EDO DRAM
  - 6-1-1-1-2-1-1-1 back-to-back accesses for SDRAM
  - BIOS shadow at 16KB increment
  - Decoupled and burst DRAM refresh with staggered RAS timing
  - Programmable refresh rate and refresh on populated banks only
  - CAS before RAS or self refresh
- **Sophisticated Power Management Features**
  - Independent clock stop controls for CPU / SDRAM, Internal AGP and PCI bus
  - PCI and AGP bus clock run and clock generator control
  - Suspend power plane preserves memory data
  - Suspend-to-DRAM and Self-Refresh operation
  - Dynamic clock gating for internal functional blocks for power reduction during normal operation
  - Low-leakage I/O pads

- **General Graphic Capabilities**
  - 64-bit Single Cycle 2D/3D Graphics Engine
  - Supports 2 to 8 Mbytes of Frame Buffer located in System Memory
  - Real Time DVD MPEG-2 and AC-3 Playback
  - Video Processor
  - I^2C Serial Interface
  - Integrated 24-bit 230MHz True Color DAC
  - Extended Screen Resolutions up to 1600x1200
  - Extended Text Modes 80 or 132 columns by 25/30/43/60 rows
  - DirectX 6 and OpenGL ICD API
- **High Performance rCADE3D™ Accelerator**
  - 32 entry command queue, 32 entry data queue
  - 4Kbyte texture cache with over 90% hit rates
  - Pipelined Setup/Texturing/Rendering Engines
  - DirectDraw™ acceleration
  - Multiple buffering and page flipping

Setup Engine
  - 32-bit IEEE floating point input data
  - Slope and vertex calculations
  - Back facing triangle culling
  - 1/16 sub-pixel positioning

Rendering Engine
  - High performance single pass execution
  - Diffused and specula lighting
  - Gouraud and flat shading
  - Anti-aliasing including edge, scene, and super-sampling
  - OpenGL compliant blending for fog and depth-cueing
  - 16-bit Z-buffer
  - 8/16/32 bit per pixel color formats

Texturing Engine
  - D3D compressed texture formats DXT1 and DXT2
  - Anisotropic texture filtering
  - 1/2/4/8-bits per pixel compact palletized textures
  - 16/32-bits per pixel quality non-palletized textures
  - Pallet formats in ARGB 565, 1555, or 444
  - Tri-linear, bi-linear, and point-sampled filtering
  - Mip-mapping with multiple Level-Of-Detail (LOD) calculations and perspective correction
  - Color keying for translucency

2D GUI Engine
  - 8/15/16/24/32-bits per pixel color formats
  - 256 Raster Operations (ROPs)
  - Accelerated drawing: BitBLTs, lines, polygons, fills, patterns, clipping, bit masking
  - Panning, scrolling, clipping, color expansion, sprites
  - 32x32 and 64x64 Hardware Cursor
  - DOS graphics and text modes

- **DVD**
  - Hardware-Assisted MPEG-2 Architecture for DVD with AC-3
  - Simultaneous motion compensation and front-end processing (parsing, decryption and decode)
  - Supports full DVD 1.0, VCD 2.0 and CD-Karaoke
  - Microsoft DirectShow 2.x native support, backward compatible to MCI
  - No additional frame buffer requirements
  - Dynamic frame and field de-interlace filtering for high quality playback on VGA monitors (Bob and Weave)
  - Tamper-proof software CSS implementation
  - Freeze, Fast-Forward, Slow Motion, Reverse
  - Pan-and-Scan support for 16:9 sequence
- **Video Processor**
  - On-chip Color Space Converter (CSC)
  - Anti-tearing via two frame buffer based capture surfaces
  - Minifier for video stream compression and filtering
  - Horizontal/vertical interpolation with edge recovery
  - Dual frame buffer apertures for independent memory access for graphics and video
  - YUV 4:2:2/4:1:1/4:2:0 and RGB formats
  - Capture / ZV Port to MPEG and video decoder
  - Vertical Blank Interval for Intercast™
  - Overlay differing video and graphic color depths
  - Display two simultaneous video streams from both internal AGP and Capture / ZV Port
  - Two scalers and Color Space Converters (CSC) for independent windows
- **Digital Flat Panel (DFP) Interface**
  - 85MHz DFP interface supports 1024x768 panels
  - Allows external TMDS transmitter for advanced panel interfaces
- **Testability**
  - Build-in NAND-tree pin scan test capability

SYSTEM OVERVIEW

The Apollo MVP4 is a PC Socket-7 system logic North Bridge with integrated 2D / 3D Graphics accelerator. The core logic portion of the chip is based on the popular 100MHz VIA Apollo MVP3 chipset with enhanced features and graphics accelerator based on the Cyber9398DVD from Trident Microsystems, Inc. The combination of the two leading edge technologies provides a stable, cost-effective, and high performance solution for personal computers, imbedded systems, set-top boxes and others. As shown in Figure 1 below, the Apollo MVP4 will interface to:

- Socket 7 CPU (66 – 100 MHz)
- L2 Cache RAM & Tag
- SDRAM Memory Interface
- PCI Bus (30 - 33 MHz)
- Analog RGB Monitor with DDC
- DFP / Digital Monitor Interface (TMDS)
- Video Capture / Playback CODECs

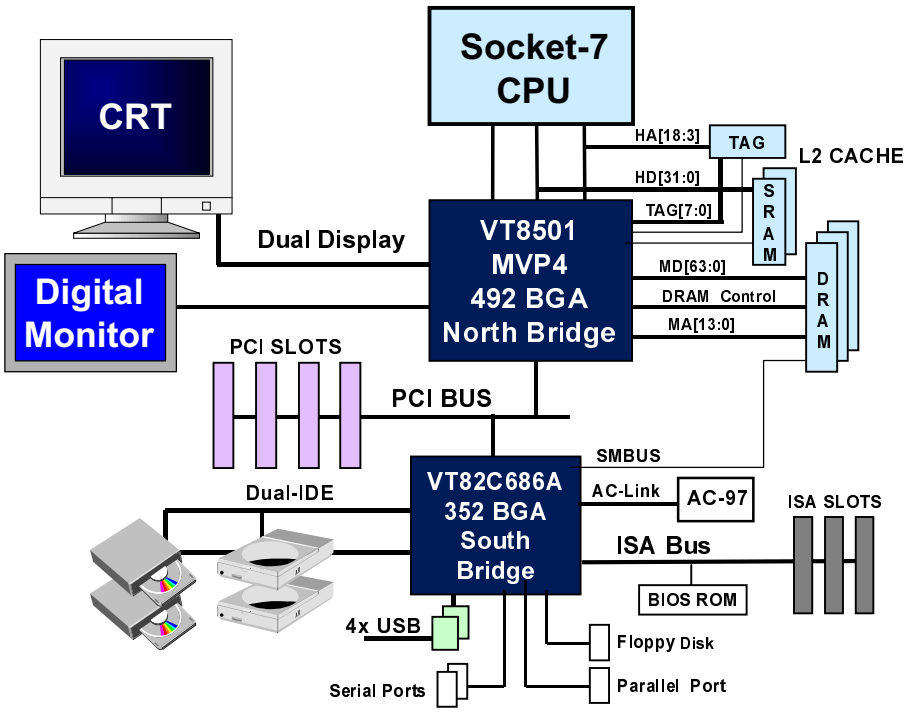

Figure 1: Apollo MVP4 High Level System Diagram

Apollo MVP4 Core Logic Overview

The Apollo MVP4 – System Media Accelerated North Bridge (SMA) is a high performance, cost-effective and energy efficient solution for the implementation of Integrated 2D/3D Graphics - PCI - ISA personal computer systems from 66 MHz to 100 MHz based on 64-bit Socket-7 (Intel Pentium and Pentium MMX; AMD K6 and K6-2; Cyrix / National 6x86 / 6x86MX, IDT / Centaur C6/WinChip), and Rise MP6 processors.

The Apollo MVP4 controller provides superior performance between the integrated 2D/3D Graphics Engine, CPU, optional synchronous cache, DRAM, and PCI bus with pipelined, burst, and concurrent operation. For L2-Cache solutions using pipelined burst synchronous SRAMs, 3-1-1-1-1-1-1-1 timing can be achieved for both read and write transactions at 100 MHz. Tag timing is specially optimized internally (less than 4 nsec setup time) to allow implementation of L2 cache using an external tag for the most flexible cache organization (0K / 256K / 512K / 1M / 2M). Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers with concurrent write-back capability are included on chip to speed up cache read and write miss cycles.

The Apollo MVP4 supports six banks of DRAMs up to 768MB. The DRAM controller supports standard Fast Page Mode (FP) DRAM, EDO-DRAM, Synchronous DRAM (SDRAM), and Virtual Channel Synchronous DRAM in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 100 MHz. The six banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16MxN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability separately selectable on a bank-by-bank basis. The DRAM Controller can run at either the host CPU bus frequency (66 / 100 MHz) or at the PC100 memory frequency (100 MHz) with built-in deskew PLL timing control. With the advanced DRAM controller, the Apollo MVP4 allows implementation of the most flexible, reliable, and high-performance DRAM interface.

The Apollo MVP4 also supports full AGP v2.0 capability with the internal 2D/3D Graphics Engine for maximum software compatibility. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU/AGP/PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / NT5 miniport drivers are supported.

The Apollo MVP4 supports one 32-bit 3.3 / 5V system bus (PCI) that is synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in AGP bus -to- PCI bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of posted write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of posted write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple, and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delayed transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The Apollo MVP4 provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the 324-pin Ball Grid Array VIA VT82C596B south bridge chip, a complete PC main board can be implemented with no external TTLs.

The Apollo MVP4 controller coupled with VIA's highly integrated south bridge, the VT82C686A, is ideal for high performance, energy efficient, and highly integrated computer systems. The VT82C686A supports a PCI-to-ISA bus controller, four USB ports, dual bus-master IDE with UltraDMA33/66, AC97 basic digital audio, system hardware monitoring, and integrated "Super-I/O" functionality.

Apollo MVP4 Graphics Controller Overview

The Apollo MVP4 Graphics Controller is a highly integrated display control device that incorporates a 64-bit 3D/2D graphic engine and video accelerator with advanced DVD video and optional TV output capability. It provides a flexible and high performance solution for graphics and video playback acceleration for various color depth and resolution modes.

The Apollo MVP4 Graphics Controller supports a video capture port to import captured live MPEG 1 or MPEG 2 video streams, or DVD decompressed video streams to be overlaid with a graphics stream of mixed color depth displays. In supporting dual live videos, the Apollo MVP4 Graphics Controller offers independent dual video windows ready for videoconferencing and with linear scaling capability.

Integrating the programmable phase lock loop with high speed LUT DACs, the Apollo MVP4 Graphics Controller is a true price/performance solution for the modern multimedia based entertainment PC.

Capability Overview

The Apollo MVP4 Graphics Controller is a fully integrated CRT and TV 64-bit 2D/3D Accelerator. The high performance graphics engine offers high speed 3D image processing in full compliance and compatibility with IBM® VGA and VESA™ extended VGA. As an integrated controller, it allows unprecedented cost and performance advantages by eliminating the need for an external frame buffer while at the same time gaining local access to a larger amount of memory. Many functions can now be eliminated that previously consumed large amounts of bandwidth.

The Apollo MVP4 Graphics Controller, equipped with a single-cycle 3D GUI Engine, pipelines 3D rendering process architecture in hardware, providing real-time interactions with solid 3D models in CAD/CAM, 3D modeling, and 3D games. It supports all key 3D rendering operations, including: Gouraud shading for smooth object surfaces, texture mapping for realistic object textures, 16-bit hardware Z-buffering for fast 3D depth calculations, and Alpha Blending for transparency effects.

The Apollo MVP4 Graphics Controller's highly innovative design, a full 64-bit memory interface with a high performance graphics engine which can support a RAMDAC™ running up to 230MHz, dramatically improves GUI functions and significantly promotes overall system operation.

The Apollo MVP4 Graphics Controller supports a full AGP implementation internally to remain compatible with existing software and programming models. However, since the engine is integrated it enjoys a higher bandwidth and lower latency than is possible with discrete solutions. AGP operations can include direct access of the system memory by the 2D/3D engine to provide increased texture memory.

To meet the requirements of a PC99 graphics adapter in a multimedia PC, the Apollo MVP4 Graphics Controller supports planar video format for MPEG-1, MPEG-2, and DVD-video playback. The dual video playback is capable of overlaying windows for videoconferencing and multimedia displays. Advanced features of the Apollo MVP4 Graphics Controller, such as color space conversion, video scaling, dual video windows, dual-view display, video capture / ZV port, Vertical Blanking Interleave (VBI), a 24-bit True Color DAC, and dual clock synthesizers allow performance at peak levels.

By using an extended 16-bit capture / ZV port the Apollo MVP4 Graphics Controller can support DTV resolution. This port can operate as either an input for video capture or as an output for video display. The Apollo MVP4 Graphics Controller is capable of supporting three simultaneous displays: CRT (analog monitor), Flat Panel (digital monitor), and Video (standard television display), each with a different "window" or desktop.

The Apollo MVP4 integrated graphics controller can drive an external TMDS transmitter. This allows an external flat panel monitor to be interfaced through the industry standard DFP interface. Many different panel types can be supported through this standard.

System Capabilities

The Apollo MVP4 Graphics Controller's main system features include:

- High Performance single cycle GUI
- Highly Integrated RAMDAC™ and Triple Clock Synthesizer
- Full Feature High Performance 3D Graphics Engine
- High speed internal AGP Bus Mastering data bus supporting DVD video playback & 3D
- Hardware implementation of motion compensation
- Dual Video Windows for Videoconferencing
- TrueVideo® Processor
- DirectDraw™ and DirectVideo™ Hardware Support
- Versatile Motion Video Capture/Overlay/Playback Support
- Flexible Frame Buffer Memory Interface
- Advanced Power Management Features
- CRT Power Management (VESA™ DPMS)
- PC99 Hardware Support

High Performance 64-bit 2D GUI

The 64-bit graphics engine of the Apollo MVP4 Graphics Controller significantly improves graphics performance through specialized hardware that accelerates the most frequently used GUI operations and matches the high-speed requirements of CPUs. Functions directly supported in hardware include: BitBLTs, image and text transfer, line draw, short stroke vector draw, rectangle fills, and clipping. The graphics engine supports 256 Raster Operations (ROPs) for up to 32-bit packed pixel graphic modes. The ROP3 Processor in the Apollo MVP4 Graphics Controller is able to perform Boolean functions which allow many additional operations, including transparency, pattern masking, color expansion alignment, and pattern enhancement. Additionally, the graphics engine features linear display memory addressing (up to 4GB memory space), accelerated color expansion modes for graphics text procession, and memory-mapped I/O registers on the graphics engine for faster access time.

Graphic functions are optimized by a 64-bit internal data bus and a four-color hardware cursor/pop-up icon, operating up to a 128x128x2 pixel image, which offloads the CPU. The hardware cursor mechanism can also be used to display patterns stored in the system memory. This pop-up icon is very useful to display user friendly information instantly through simple hot key operations. This advanced function combination allows significant performance increases over standard Super VGA designs and provides outstanding graphics acceleration on GUIs, such as Microsoft® Windows 95®.

Highly Integrated RAMDAC™ & Clock Synthesizer

The highly integrated design of the Apollo MVP4 Graphics Controller offers a "no TTL" solution for cost-effective, high-performance PC multimedia subsystem designs. The 64-bit memory data bus supporting SDRAM and SGRAM memory provides faster data transfer rates for improved system throughput. The Apollo MVP4 Graphics Controller has a built-in, high speed RAMDAC™. The RAMDAC™ is composed of one 256x24 and one 256x18 color lookup table and a triple loop frequency synthesizer, providing the read/write timing control for the Frame Buffer Memory and the refresh of the TV/CRT display.

The integrated frequency synthesizer provides a 125MHz memory clock for high speed DRAM access and a 230MHz video clock which supports various refresh rates up to 85Hz at 1280x1024.

Full Feature High Performance 3D Engine

The Apollo MVP4 Graphics Controller is equipped with an advanced Graphics Drawing, Single Cycle 3D Graphics Engine that performs premium 3D functions at a high level of more than 1M triangles per second. The 3D engine supports Microsoft® Direct3D. The 3D Engine is set up to off-load the CPU from major 3D tasks including slope calculation, sub-pixel positioning, and Tri-striping. By balancing the 3D pipeline and reducing parameter passing, the Apollo MVP4 Graphics Controller provides very high levels of performance. The 3D engine is integrated with a triangle set-up engine that sets up triangles according to vertex input data and accomplishes various functions for 3D rendering. Gouraud shading provides smooth shading for colors across surfaces, perspective correction texture mapping to correct texture data based on the perspective, bi-linear texture filtering for interpolating, alpha blending to compensate colors for the opacity of two colors blended, Z-buffering (16-bit/24-bit), video texturing to overlay 2D video play-back onto 3D images, fogging to simulate weather effects, palletized texture mapping (1-, 4-, or 8-bit) for memory and bandwidth reduction, and anti-aliasing to reduce or eliminate jaggies resulted from alias rendering. The 3D engine also works with the APM system, conserving power while 3D operations are suspended.

Video Processor

Video processor features include: on-chip hardware Color Space Conversion (CSC) for faster data conversion on the fly, Horizontal/Vertical (H/V) scaling with interpolation, edge recovery algorithm logic, gamma correction, and overlay control with different color depths from graphics. The Apollo MVP4 Graphics Controller also includes a fully integrated GUI accelerator, read cache, and command FIFO that optimize memory bandwidth and maximize graphics performance.

The Apollo MVP4 Graphics Controller, with an integrated Video Display and a Capture Engine, supports dual apertures on the PCI bus which enables independent graphic and video data to be transported simultaneously to and from different memory areas and greatly accelerates the performance of both DirectDraw™ and DirectVideo™. The Apollo MVP4 Graphics Controller can provide dual video windows that display different images from different video sources (from the PCI bus and from the capture port) on the same screen. The video image is stored in off-screen memory and is retrieved by the Video Display Processing block for video processing. With the help of DirectDraw™ acceleration for sprites, page flipping, double buffering, and color keying, video processing is performed by utilizing a proprietary edge recovery algorithm for sharper line visibility, de-interlacing, anti-tearing, multitap horizontal filtering, dithering, and scaling operations with bilinear interpolation in both horizontal and vertical directions. Linear scaling permits zoom in/out to any size without any restrictions. In addition, the on-chip hardware Color Space Conversion (CSC) accelerates conversion for 16 bit YUV pixels into linear true color 24 bit RGB pixels on the fly. The additional X and Y minifiers are capable of shrinking video images to any linear fractions, which saves bus bandwidth and memory space. The YUV planar logic of the Apollo MVP4 Graphics Controller supports a YUV 420 format that can eliminate redundant video stream decoding procedures. The load of the CPU is reduced while performing software MPEG or software video conferencing. The color and luminance control provided by the Apollo MVP4 Graphics Controller offers color compensations to prevent color distortion for display devices such as a CRT or TV with Gamma correction and hue adjustment control.

The Video Conferencing feature allows remote and local video images to be displayed simultaneously on the same screen.

Video Capture and DVD

The Apollo MVP4 Graphics Controller has a video capture / ZV port and advanced hardware interface logic allowing it to be directly connected to many MPEG and video decoders.

The Apollo MVP4 Graphics Controller, integrated with a DVD video hardware block for motion compensation, gives existing PCs the ability to play DVD video in MPEG-2 format at high bandwidths with very good video quality.

A new industry standard is being set for transmission of non-video data over a TV broadcast signal during vertical blanking dead time. This technology is referred to as Intercast. The Apollo MVP4 Graphics Controller has the ability to take the entire video stream over the video port, sending the visible video stream to the display memory for display in a window, stripping the VBI data from the stream, and then sending this data to the CPU for processing using PCI Bus Mastering.

Versatile Frame Buffer Interface

The Apollo MVP4 Graphics Controller features a versatile frame buffer interface aperture into main system memory. Optimized performance can be achieved with the single cycle memory bus interface using programmable DRAM timing. The display queue has been increased to reduce the frequency of memory bus requests, optimizing memory bus efficiency for the graphic controller.

With the support of the internal AGP aperture, the Apollo MVP4 Graphics Controller has access to system memory through the GART. In the execute mode, the Apollo MVP4 Graphics Controller is able to use both the dedicated graphics portion and the general portion of system memory for graphics operations. As a result, DVD and 3D rendering performance and quality are greatly enhanced.

Hi-Res and Hi-Ref Display Support

Apollo MVP4 Graphics Controller display enhancements dramatically improve CRT resolution. These enhancements include support of non-interlaced 1280x1024x64K, 1024x768x16M, 800x600x16M, and 640x480x16M colors for “full spectrum” color. Extended text modes of 80 or 132 columns by 25, 30, 43, or 60 rows provide an extended graphics area frequently used in many spreadsheet and database applications. Extended graphics and text modes are supported by software drivers that provide a “ready-to-go” solution, minimizing the need for additional driver development.

A virtual screen can be created with the Apollo MVP4 Graphics Controller. When this function is enabled, a selected portion of a large image can be shown on a smaller display. The image can also be moved across the whole screen, either up or down.

The Apollo MVP4 Graphics Controller is able to automatically detect DDC monitors with I^2C signaling.

CRT Power Management (VESA DPMS)

The Apollo MVP4 Graphics Controller conforms to the standard power management schemes defined by VESA™ for CRTs. The Apollo MVP4 Graphics Controller supports four states of VESA™ Display Power Management Signaling (DPMS), which decrease monitor power consumption after timeout periods. VESA™ DPMS power down states (ready, standby, suspend, and off) specify HSYNC and VSYNC signals to control the monitor power down state.

Digital Flat Panel (DFP) Interface

The Apollo MVP4 DFP interface is designed to support industry standard TFT and DSTN panels through an external TMDS transmitter. A Silicon Image SIL140 TMDS transmitter can be used to complete this interface.

MVP4 Pin	SIL140 Pin	24-Bit Color TFT	18-Bit Color TFT
PD[23]	D0	B0	
PD[22]	D1	B1	
PD[21]	D8	G0	
PD[20]	D9	G1	
PD[19]	D16	R0	
PD[18]	D17	R1	
PD[17]	D2	B2	B0
PD[16]	D3	B3	B1
PD[15]	D10	G2	G0
PD[14]	D11	G3	G1
PD[13]	D18	R2	R0
PD[12]	D19	R3	R1
PD[11]	D4	B4	B2
PD[10]	D5	B5	B3
PD[9]	D6	B6	B4
PD[8]	D7	B7	B5
PD[7]	D12	G4	G2
PD[6]	D13	G5	G3
PD[5]	D14	G6	G4
PD[4]	D15	G7	G5
PD[3]	D20	R4	R2
PD[2]	D21	R5	R3
PD[1]	D22	R6	R4
PD[0]	D23	R7	R5

Video Capture Interface / ZV Port

A video capture / ZV port is supported for video devices such as MPEG1 and MPEG2. Additionally, a zero-wait state host write buffer, read cache, and memory mapped I/O increase operating speeds and contribute to peak performance levels. All I/O interfaces are 5V tolerant, capable of interfacing with external devices operating at 5V, even though the Apollo MVP4 Graphics Controller runs at 2.5V internally. Graphics system throughput is further enhanced by a command FIFO, allowing maximum bus transfer speed for applications such as Windows™ or AutoCAD™ that directly access video memory.

Complete Hardware Compatibility

The Apollo MVP4 Graphics Controller is fully compliant with the VESA™ DDC and VAFC standards. The Apollo MVP4 Graphics Controller is 100% VGA compatible at both the BIOS and Driver level, allowing full compatibility with virtually any VGA application software. The Apollo MVP4 Graphics Controller provides hardware support to DirectDraw™, offering high-speed game graphics on Windows 95®. The Apollo MVP4 Graphics Controller meets the requirements of PC99 as well, supporting a unique ID for each customer and a unique ID for each model.