82566 Gigabit Platform LAN Connect

Networking Silicon

Datasheet

Product Features

- IEEE 802.3ab compliant
  - —Robust operation over the installed base of Category-5 (Cat-5) twisted pair cabling
- Robust end to end connections over various cable lengths
- Full duplex at 10, 100, or 1000 Mbps and half duplex at 10 or 100 Mbps.
- IEEE 802.3ab Auto-negotiation with Next Page support
  - —Automatic link configuration including speed, duplex, and flow control
- 10/100 downshift
  - —Automatic link speed adjustment with poor quality cable
- Automatic MDI crossover
  - —Helps to correct for infrastructure issues
- Advanced Cable Diagnostics
  - —Improved end-user troubleshooting
- Footprint compatible with 82562V devices for a single-board dual design (Gigabit and 10/100)
- LCI interface for a very low power 10/100 link
- Gigabit LAN Connect Interface
  - —Low pin count, high speed interface with special low power idle modes
  - —Allows PHY placement proximity to I/O back panel.
- 3 LED outputs
  - —Link and Activity indications (10, 100, and 1000 Mbps)
- Clock supplied to MAC
  - —Cost optimized design
- Full chip power down
  - —Support for lowest power state
- 81-pin, 1.0 mm pitch, 10 mm x 10 mm FCMMAP (BGA) Package
  - —Smaller footprint and lower power dissipation compared to multi-chip MAC and PHY solutions. Footprint compatible with the Intel® 82562V Platform LAN Connect device
- Integrated voltage regulator and power supply control, which can be powered from a single 3.3V DC rail
- Operating temperatures: 0° C to 70° C and 0° C to 55° C (with internal regulator) – heat sink or forced airflow not required
  - —Simple Thermal Design
- Power Consumption less than 1.16 Watts (silicon power)

317436-003
Revision 2.4

Revision History

Date	Revision	Comments
December 2007	2.4	• Removed 802.3 SerDes reference in section 1.0. • Updated Section 1.2. Added reference document “Implementing the Intel® Auto Connect Battery Saver (ACBS) With the Intel® 82566”.
August 2007	2.3	• Added ICH9 information. • Added new power consumption table for the 82566 DC/DM.
May 2007	2.2	• Change ballout row “I” to “J”. Changed all “I” pinout designations to “J”. • Updated crystal specifications. • Replaced Figure 4.
August 2006	2.1	• Removed Vcase parameter from Table 9. • Removed section 3.4 “Thermal Diode (TD)”. This information can now be found in the *82566 Gigabit Platform LAN Connect Thermal Design Considerations* Application Note. • Revised section 4.2 title. • Revised Table 10 (removed operating temperature range parameter and related notes). • Changed all “J” pinout designations to “I” to match Figure 10 “Visual Pin Assignments”.
June 2006	2.0	Initial public release. • Added note to Table 16.
March 2006	1.5	Initial Intel Confidential release.

Contents

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Tables

1.0 Introduction

The 82566 is a single port Gigabit Ethernet Physical Layer Transceiver (PHY) that connects to its MAC through a dedicated interconnect. The 82566 is based on Intel's Gigabit PHY technology, and supports operation at data rates of 10/100/1000 Mbps. The physical layer circuitry provides a standard IEEE 802.3 Ethernet interface for 10BASE-T, 100BASE-TX, and 1000BASE-T applications (802.3, 802.3u, and 802.3ab).

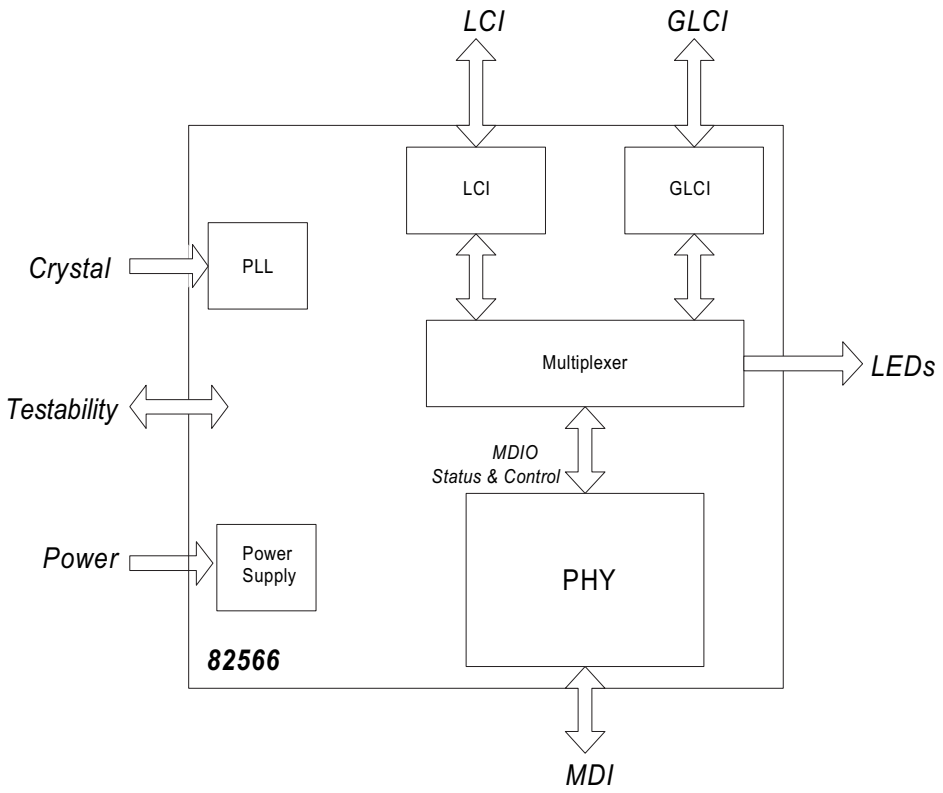
This device operates with the ICH8/ICH9 chipset that incorporates and integrates the media access controller (MAC), which is referred to as the ICH8/ICH9 LAN.

The 82566 is packaged in a small footprint flip chip molded matrix array package (FCMMAP) with 81 balls in a 9 x 9 array. The package size is 10 mm x 10 mm with a pitch of 1.0 mm, making it attractive for small form-factor platforms.

The device interfaces with its MAC through two interfaces: Gigabit LAN Connect Interface (GLCI) and LAN Connect Interface (LCI). The GLCI is a high speed proprietary serial interface. The LCI is a low speed proprietary parallel bus. The 82566 operates using both interfaces; the GLCI for 1000 Mbps traffic and LCI for all other traffic types.

Figure 1 identifies the major components of the 82566 architecture.

Figure 1. 82566 Block Diagram



1.1 Document Scope

This document contains datasheet specifications for the 82566 Gigabit Platform LAN Connect (PLC), including signal descriptions, DC and AC parameters, packaging data, and pinout information.

1.2 Reference Documents

This document assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide application information:

- *IEEE Standard 802.3*, 2002 Edition. Incorporates various IEEE Standards previously published separately. Institute of Electrical and Electronic Engineers (IEEE).
- *IEEE Standard 1149.1*, 2001 Edition (JTAG). Institute of Electrical and Electronics Engineers (IEEE).
- *I/O Control Hub 8 NVM Map and Programming Information*. Intel Corporation.
- *I/O Control Hub 9 NVM Map and Programming Information*. Intel Corporation.
- *Intel® I/O Controller Hub 8 (ICH8) Family Datasheet*, Intel Corporation.
- *Intel® I/O Controller Hub 9 (ICH9) Family Datasheet*, Intel Corporation.
- *Intel 965 Express Chipset Family Platform Design Guide*, Intel Corporation.
- *Intel® Centrino® Pro Processor Technology and Intel® Centrino® Duo Processor Technology Design Guide. For Intel® Core™2 Duo Processor, Mobile Intel® 965 Express Chipset Family and Intel® 82801HBM ICH8M & Intel® 82801HEM ICH8M-E I/O Controller Hub Based Systems*, Intel Corporation.
- *ICH8/ICH9 (MAC) GbE LAN Controller and 82566/82562V (PHY) Software Developer's Manual*. Intel Corporation.
- *Implementing the Intel® Auto Connect Battery Saver (ACBS) With the Intel® 82566*. Intel Corporation.

1.3 Product Codes

Table 1 lists the product ordering codes for the 82566 device.

Table 1. Product Ordering Codes[a]

Part Number	Product Name	Description
RU82566DM	Intel® 82566 Gigabit Platform LAN Connect Device	Business Desktop GbE LAN connection
RU82566DC	Intel® 82566 Gigabit Platform LAN Connect Device	Consumer Desktop GbE LAN connection
RU82566MM	Intel® 82566 Gigabit Platform LAN Connect Device	Business Mobile GbE LAN connection.
RU82566MC	Intel® 82566 Gigabit Platform LAN Connect Device	Consumer Mobile GbE LAN connection

a. For more information regarding the differences, please contact your Intel field representative.

2.0 Signal Descriptions

2.1 Signal Type Definitions

The signals are defined as follows in the table below:

Type	Description
In (I)	Standard input-only signal.
Out (O)	Standard output-only signal.
T/S	Bi-directional, tri-state input/output signal.
S/T/S	Sustained tri-state signal.
O/D	Open drain signal.
A-in	Analog input signal.
A-out	Analog output signal.
P	Power signal.
B	Input bias.
PU	Pull-up.
PD	Pull-down.

2.2 Gigabit LAN Connect Interface (GLCI) Pins

Table 2. GLCI Pins

Signal Name	Ball	Type	Description
GLAN_RXP GLAN_RXN	J4 H4	A-in	**GLCI Serial Data Input.** This is the differential input for GLCI (MAC to PHY).
GLAN_TXN GLAN_TXP	J2 H2	A-out	**GLCI Serial Data Output.** This is the differential output for GLCI (MAC to PHY).
KBIAS_P KBIAS_N	G7 H7	B	**Impedance Compensation.** External 1.4 KΩ 1% resistors should be used.

2.3 LAN Connect Interface (LCI) Pins

Table 3. LCI Pins

Signal Name	Ball	Type	Description
JKCLK	E2	O	**LCI/GLCI Clock.** The clock is driven by the 82566 according to the operation mode: • In 1000 Mbps mode, JKCLK frequency is 62.5 MHz. • In 100 Mbps mode, JKCLK frequency is 50 MHz. • In 10 Mbps mode, JKCLK frequency is 5 MHz. • In power down mode, JKCLK frequency is 0 MHz.
JRSTSYNC	E3	I	**Reset/SYNC.** This pin is driven by the MAC and has two functions: • Reset. When this pin is asserted beyond one LCI clock, the 82566 refers to this signal as a reset signal. However, to ensure that the 82566 resets, the reset should remain active for at least 500 µs. This functionality is also used to bring the 82566 out of a power-down state. • SYNC. When this pin is activated synchronously for one LCI clock only, it is used for synchronization between the MAC and the 82566 on LCI word boundaries.
JTXD2 JTXD1 JTXD0	F1 F3 D1	I	**LCI Transmit Data.** These pins are used for receiving real time control and management data transmitted by the ICH8/ICH9 LAN. These pins are also used to move out of band control from the MAC to the 82566. The pins should be fully synchronous to JKCLK.
JRXD2 JRXD1 JRXD0	C1 D2 D3	O	**LCI Receive Data.** These pins are used for transmitting real time control and management data received by the ICH8/ICH9 LAN. These pins are also used to move out of band control from the 82566 to the MAC.

2.4 Miscellaneous Pins

Table 4. Miscellaneous Pins

Signal Name	Ball	Type	Description
THERM_D_P THERM_D_N	A2 A3	A-out	**Thermal Diode Reference.** This pin can be used to measure the silicon temperature within the device.
RESERVED	J6 J7 A6 B5 C5	N/A	**No Connect.** These pins must not be connected to any external circuitry. Pull-up or pull-down resistors should not be connected to these pins.

2.5 PHY Pins

2.5.1 LEDs

Table 5. LED Pins[a]

Signal Name	Ball	Type	Description
LED0	A4	O	**LED0.** This signal is used for the programmable LED. It is programmed through the Intel® ICH8/ICH9 NVM word 18h.
LED1	B4	O	**LED1.** This signal is used for the programmable LED. It is programmed through the Intel® ICH8/ICH9 NVM word 17h.
LED2	A5	O	**LED2.** This signal is used for the programmable LED. It is programmed through the Intel® ICH8/ICH9 NVM word 18h.

a. The *I/O Control Hub 8 /ICH9 NVM Map and Programming Information* Application Notes can be referenced for details regarding the programming of the LEDs and the various modes.

2.5.2 Analog Pins

Table 6. Analog Pins

Signal Name	Ball	Type	Description
MDI_PLUS[0] MDI_MINUS[0]	B8 B9	A	**Media Dependent Interface [0].** In MDI configuration, MDI_PLUS[0]+/- is used for the transmit pair and in MDI-X configuration MDI_MINUS[0]+/- is used for the receive pair.
MDI_PLUS[1] MDI_MINUS[1]	D9 D8	A	**Media Dependent Interface [1].** In MDI configuration, MDI_PLUS[1]+/- is used for the receive pair and in MDI-X configuration MDI_MINUS[1]+/- is used for the transmit pair.
MDI_PLUS[2] MDI_MINUS[2] MDI_PLUS[3] MDI_MINUS[3]	F9 F8 H8 H9	A	**Media Dependent Interface [2:3].** For 1000BASE-T MDI configuration, MDI_PLUS[2:3]+/- is used for the receive pair and in MDI-X configuration MDI_MINUS[2:3]+/- is used for the transmit pair. These pins are not used for 100BASE-TX and 10BASE-T.
IEEE_TEST_P IEEE_TEST_N	A7 B7	A-out	**Analog Test Pins Output.** These are used for measurement of the transmitter 125 MHz clock jitter.
RBIAS_P RBIAS_N	E7 E6	B	**Compensation Reference Resistor.** A 1.4 KΩ, 1% tolerance resistor should be used. RBIAS_N should also be connected to ground (V_{SS}).
XTAL1 XTAL2	H6 H5	A-in A-out	**Crystal In.** These pins can be driven by an external 25 MHz crystal or by an external MOS level 25 MHz oscillator. It is also used as the clock reference for the PHY.

2.5.3 Testability Pins

Table 7. Testability Pins

Signal Name	Ball	Type	Description
JTAG_TCK	G1	I	**JTAG Clock Input**
JTAG_TDI	H1	I/PU	**JTAG TDI Input**
JTAG_TDO	G3	T/S	**JTAG TDO Output**
JTAG_TMS	G2	I/PU	**JTAG TMS Input**
TEST_EN	B6	I	**Test Mode Enable.** This signal enables test mode capabilities. It should be strapped to GND for normal operation.

2.6 Power Supply Pins

Table 8. Power Supply Pins (Sheet 1 of 2)

Signal Name	Ball	Type	Description
VCC3P3 VCC3P3	F2 B3	P	**3.3V DC Supply.** This is connected to the 82566.
VCC1P8 VCC1P8 VCC1P8 VCC1P8	C2 G5 F5 D5	P	**1.8V DC Supply.** This is connected to the 82566.
CTRL_18	B2	Out	**1.8V Control.** This is the voltage control signal for the external PNP transistor that generates the 1.8V supply.
VCC	D4 E4	P	**1.0V DC Supply.** This is connected to the 82566 core.
VCC1P0	G4	P	**1.0V DC Supply.** This is connected to the GLCI circuits.
VDD1P0 VDD1P0	F7 D7 E8	P	**1.0V DC Supply.** This is connected to the PHY.
VCCF1P0, VCCFC1P0	E5 H3	P	**1.0V DC Normal Operation.**
CTRL_10	C3	Out	**1.0V Control.** This is the voltage control signal for the external PNP transistor that generates the 1.0V supply.

Table 8. Power Supply Pins (Sheet 2 of 2)

Signal Name	Ball	Type	Description
V1P0_OUT	B1	P	**1.0V DC Output.** This output is from the on-die internal regulator. This signal should be connected to VCC1P8 when external voltage regulators are used or in IVRd mode. V1P0_OUT should be connected to VCC1P0 for IVRi mode.
VSS	A1 C4 E1 F4	P	**Ground**
VSSA	A8 A9 C6 C7 C8 C9 D6 E9 F6 G6 G8 G9 J1 J3 J5 J8 J9	P	**Analog Ground**

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3.0 Voltage, Temperature, and Timing Specifications

3.1 Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings[a]

Symbol	Parameter[b]	Min[c]	Max	Unit
$T_{storage}$	Storage Temperature Range	-65	140	°C
V_i V_o	3.3V DC Digital Compatible I/O Voltage Analog 1.0V DC I/O Voltage Analog 1.8V DC I/O Voltage	-0.5 -0.2 -0.3	4.6 1.68 2.52	V
VCCP	3.3V Periphery Voltage Range	-0.5	4.6	V
VCC1p8	1.8V Analog Voltage Range	-0.3	2.52	V
VCC1p0	1.0V DC Core/Analog DC Supply Voltage	-0.2	1.68	V

a. Ratings in this table are those beyond which permanent device damage is likely to occur. These values should not be used as the limits for normal device operation. Exposure to these absolute maximum rating conditions for extended periods may affect device reliability.
b. Recommended operating conditions require the accuracy of a power supply of +/- 5% relative to the nominal voltage.
c. Maximum ratings are referenced to ground (V_{SS}).

3.2 Recommended Operating Conditions

Table 10. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
VCCP	Periphery Voltage Range	3.0	3.6	V
VCC1p8	Core Digital Voltage Range	1.71	1.89	V
VCC1p0	Core/Analog Voltage Range	0.95	1.05	V

3.3 DC and AC Characteristics

Table 11. Preliminary DC and AC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{IL}	Voltage input LOW	-	-	0.8	V	-
V_{IH}	Voltage input HIGH	-	2.0	-	V	-
V_{OL}	Voltage output LOW	I_{OL}= -12 mA; VCC=Min I_{OL}=-100 µA; VCC=Min	- -	0.4 0.2	V	-
V_{OH}	Voltage output HIGH	I_{OH}= -16 mA; VCC=Min I_{OH}=-100 µA; VCC=Min	2.4 VCC-0.2	-	V	-
V_{hys}	Hysteresis		160	-	mV	a
I_{il}	Input Current	VCC-Max; VI=3.6V DC/GND	-	15	µA	
I_{OFF}	Current at IDDQ Mode		-	50	µA	b
PU	Internal Pull-Up		2.7	8.6	K Ω	c
C_{in}	Input capacitance		-	2.5	pF	d
C_{out}	Load capacitance	@ 160 MHz	-	16	pF	d

a. The input buffer has a hysteresis greater than 160 mV.
b. IDDQ mode maximum current consumption: CORE_VCCP: 15 µA; VCCP: 35 µA
c. The internal pull-up maximum was characterized at slow corner (110C, VCC=min, process slow); and the internal pull-up minimum, at fast corner (0C, VCC=max, process fast).
d. Pad C_{in} = 2.5 pF (maximum input capacitance), and C_{out} = 16 pF (characterized maximum output load capacitance per 160 MHz).

3.4 LED/TEST/JTAG I/F DC Specifications

Table 12. Preliminary LED/TEST/JTAG I/F DC Specifications

Symbol	Parameter	Condition	Min	Max	Unit	Notes
VCCP	Periphery Supply	-	3.0	3.6	V	-
V_{ih}	Input High Voltage	-	2.0	VCC +0.3	V	-
V_{il}	Input Low Voltage	-	-0.3	0.8	V	-
V_{leak}	Input Leakage Current	0 < V_{in}< VCCP	-	±20	µA	-
V_{oh}	Output High Voltage	I_{out} = -16 mA	2.4	-	V	-
V_{ol}	Output Low Voltage	I_{out} = -0.1 mA I_{out} = -12 mA	- -	0.2 0.4	V	-
C_{in}	Input Pin Capacitance	-	-	2.5	pF	-

3.5 Power Supply Connections

There are two options in providing power to the 82566:

- Connecting the 82566 to three external power supplies with nominal voltages of 3.3V DC, 1.8V DC, and 1.0V DC, which is covered in Section 3.5.1.
- Powering the 82566 with only an external 3.3V DC supply and using internal power regulators from the device itself combined with external PNP transistors to supply the 1.8V DC and 1.0V DC levels as described in Section 3.5.2.

3.5.1 External Voltage Regulator (EVR) Power Delivery

The following power supply requirements apply to designs where the 82566 is supplied by external voltage regulators (EVRs). These systems do not use the internal regulator logic built into the device as described in Section 3.5.2.

Table 13. 3.3V DC External Power Supply Parameters

Title	Description	Min	Max	Units
Rise Time	Time from 10% to 90% mark	0.1	100	ms
Monotonicity	Voltage dip allowed in ramp	-	0	mV
Slope	Ramp rate at any given time between 10% and 90% Min: 0.8*V(min)/Rise time (max) Max: 0.8*V(max)/Rise time (min)	24	28800	V/s
Operational Range	Voltage range for normal operating conditions	3.0	3.6	V
Ripple	Maximum voltage ripple (peak to peak)[a]	-	100	mV
Overshoot	Maximum overshoot allowed	-	100	mV

a. This is dependent on capacitance.

Table 14. 1.8V DC External Power Supply Parameters

Title	Description	Min	Max	Units
Rise Time	Time from 10% to 90% mark	0.1	100	ms
Monotonicity	Voltage dip allowed in ramp	-	0	mV
Slope	Ramp rate at any given time between 10% and 90% Min: 0.8*V(min)/Rise time (max) Max: 0.8*V(max)/Rise time (min)	14		V/s
Operational Range	Voltage range for normal operating conditions	1.71	1.89	V
Ripple	Maximum voltage ripple (peak to peak)[a]	-	40	mV

Table 14. 1.8V DC External Power Supply Parameters

Title	Description	Min	Max	Units
Overshoot	Maximum overshoot allowed	-	100	mV
Decoupling Capacitance	Capacitance range	15	25	µF
Capacitance ESR	Equivalent series resistance of output capacitance	-	50	mΩ

a. This is dependent on capacitance.

Table 15. 1.0V DC External Power Supply Parameters

Title	Description	Min	Max	Units
Rise Time	Time from 10% to 90% mark	0.1	100	ms
Monotonicity	Voltage dip allowed in ramp	-	0	mV
Slope	Ramp rate at any given time between 10% and 90% Min: 0.8*V(min)/Rise time (max) Max: 0.8*V(max)/Rise time (min)	7.6	17	V/s
Operational Range	Voltage range for normal operating conditions	0.95	1.05[a]	V
Ripple	Maximum voltage ripple (peak to peak)[b]	-	40	mV
Overshoot	Maximum overshoot allowed	-	100	mV
Decoupling Capacitance	Capacitance range	15	25	µF
Capacitance ESR	Equivalent series resistance of output capacitance	-	50	mΩ

a. To reduce BOM costs, the ICH8/ICH9 1.05V +/-5% supply can be used.
b. This is dependent on capacitance.

3.5.1.1 In-Rush Current

To meet 375 mA in-rush current requirements (not including external capacitors), the ramp time should be 5 ms to 100 ms on all power rails. For faster ramps (100 µs to 5 ms), higher in-rush current is expected due to the high charging current of the decoupling capacitors on the 3.3V DC, 1.8V DC, and 1.0V DC power rails.

3.5.1.2 82566 Power Up Sequence (External LVR)

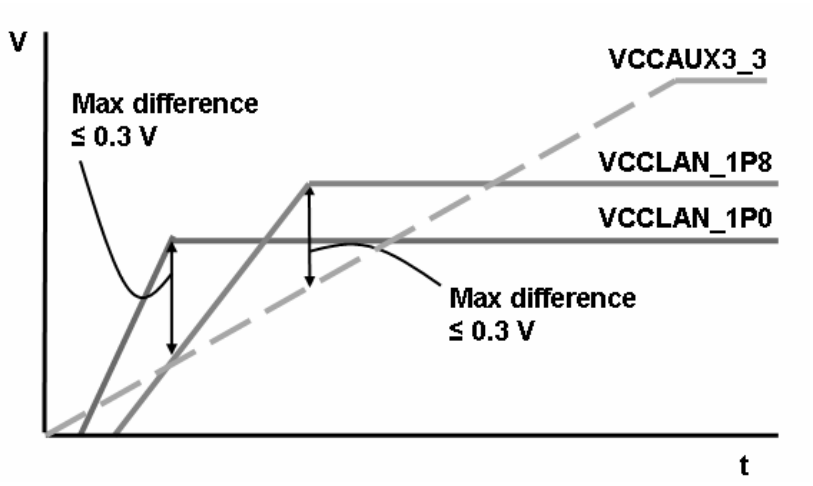
Designs must comply with power sequencing requirements to avoid latch-up and forward-biased internal diodes.

The board designer controls the power up sequence with the following stipulations:

- 1.8V must not exceed 3.3V by more than 0.3 V.
- 1.0V must not exceed 3.3V by more than 0.3 V.

For power down, there is no requirement (only charge that remains is stored in the decoupling capacitors).

Figure 2. External LVR Power-up Sequence



3.5.2 Internal Voltage Regulator (IVR) Power Delivery

The 82566 has two IVR controllers. One for the 1.8V supply and one for the 1.0V supply. There are two IVR modes of operation known as IVRd and IVRi. IVRd uses two external transistors to generate the 1.8V and 1.0V supplies. In this mode, these two voltages are stepped down from a 3.3V DC source. IVRi mode uses an external transistor to generate the 1.8V supply and an internal transistor to generate the 1.0V supply. In this mode, the 1.8V supply is stepped down from a 3.3V DC source, and the 1.0V supply is stepped down from the 1.8V DC supply.

Table 16. 3.3V DC External Power Supply Parameters

Title	Description	Min	Max	Units
Rise Time	Time from 10% to 90% mark	0.1	100	ms
Monotonicity	Voltage dip allowed in ramp	-	0	mV
Slope	Ramp rate at any given time between 10% and 90% Min: 0.8*V(min)/Rise time (max) Max: 0.8*V(max)/Rise time (min)	24	9.5	mV/ms
Operational Range	Voltage range for normal operating conditions	3.0	3.6	V
Ripple	Maximum voltage ripple (peak to peak) @ f < 20 MHz	-	100	mV
Overshoot	Maximum overshoot allowed	-	100	mV
Overshoot Settling Time	Maximum overshoot allowed duration. (At that time delta voltage should be lower than 5 mV from steady state voltage)	-	0.05	ms

3.5.2.1 In-Rush Current

To meet 375 mA in-rush current requirements, the ramp time should be 5 ms to 100 ms on the 3.3V DC power rail. For faster ramps (100 µs to 5 ms), higher in-rush current is expected due to the high charging current of the decoupling capacitors on the 3.3V DC power rail.

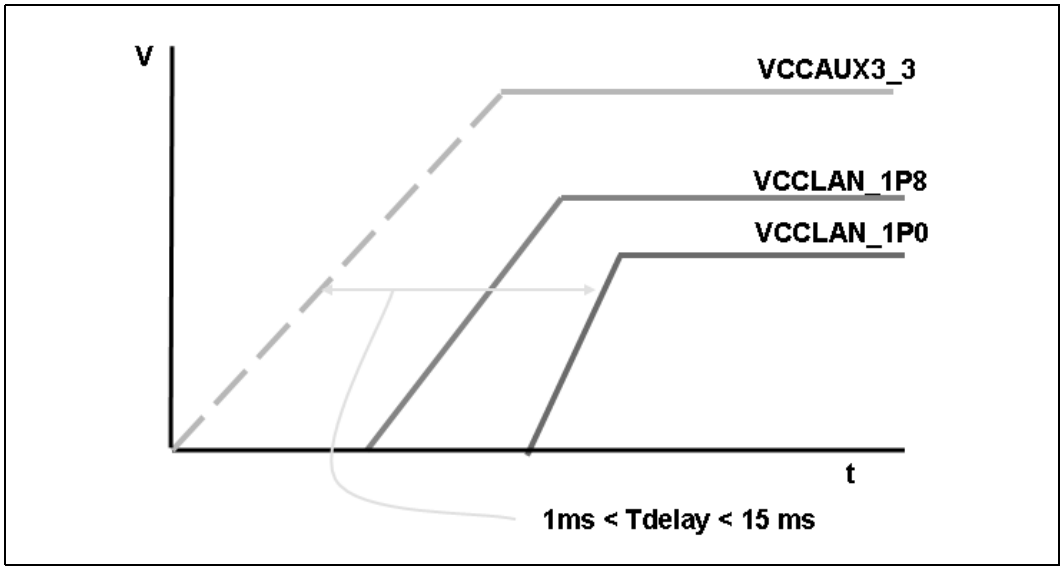
3.5.2.2 82566 Power Up Sequence (Internal LVR)

The 82566 controls the power up sequence internally and automatically with the following conditions:

- 3.3V must be the source for the internal LVR.
- 1.8V will never exceed the 3.3V.
- 1.0V will never exceed 3.3V or 1.8V.

The ramp is delayed internally, with T_{delay} depending on the rising slope of the 3.3V ramp. For power down, there is no requirement (only charge that remains is stored in the decoupling capacitors).

Figure 3. Internal LVR Power-up Sequence



3.5.2.3 1.8V DC Internal LVR Specification

Table 17. 1.8V DC Internal LVR Specification

Parameter	Value		Units	Comments
	Minimum	Maximum		
Input Voltage (V_in)	3.0	3.6	V	Typically 3.3V
Input Voltage Slew Rate (V_in_rise)	-	-	ms	Typically 5 ms
DC Output Voltage (Vdd1p8)	1.71	1.89	V	Measured on the internal sense point.
Output Current (I_vdd1p8)	5	950	mA	Typically 300 mA
Turn-On Time (T_on)	3	10	ms	Both for 1.8V DC and 1.0V DC LVRs
Peak-to-Peak Output Ripple (Vac)	-	50	mV	The peak to peak output ripple is measured at 20 MHz Bandwidth.
Power Supply Rejection Ratio (1p8_PSRR)	-	-20	dB	Typically -40 dB
1p8 LVR Voltage @ Over/Under Shoot Event (1p8_event)	-	50	mV	-

3.5.2.4 1.0V DC Internal LVR Specification

Table 18. 1.0V DC Internal LVR Specification

Parameter	Value		Units	Comments
	Minimum	Maximum		
Input Voltage (V_{in})	3.0	3.6	V	Typically 3.3V
Input Voltage Slew Rate (V_in_rise)	-	-	ms	Typically 5 ms
DC Output Voltage (V1p0_out)	0.95	1.05	V	Measured on the internal sense point.
Output Current (I_v1p0)	5	400	mA	Typically 200 mA

Table 18. 1.0V DC Internal LVR Specification

Parameter	Value		Units	Comments
	Minimum	Maximum		
Turn-On Time (T_on)	3	10	ms	Both for 1.8V DC and 1.0V DC LVRs
Peak-to-Peak Output Ripple (Vac)	-	50	mV	Both for 1.8V DC and 1.0V DC LVRs. The peak to peak output ripple is measured at 20 MHz Bandwidth.
Power Supply Rejection Ratio (1p0_PSRR)	-	-20	dB	Typically -40 dB

3.5.2.5 PNP Transistor Specification for 1.8V DC LVR

Table 19. PNP Specification for 1.8V DC LVR

PNP Connection	Description	Symbol	Min	Typ	Max	Units
PNP Transistor for 1.8V DC LVR, using internal Transistor for 1.0V DC LVR	DC Gain[a]	β	60	-	400	
	Transition Frequency	fT	-	40	-	MHz
	Thermal Resistance Junction to Ambient[b]	Rt_ja	-	-	60	°C/W
	Maximum Operation Junction Temperature	Tj_max	-	-	150	°C
	Maximum Collector Current	Ic_max	-	-	1	A
	Maximum total power dissipation[c]	Pmax	-	-	1.2	W
PNP Transistor for 1.8V DC LVR, using external Transistor for 1.0V DC LVR	DC Gain[d]	β	60	-	400	V
	Transition Frequency	fT	-	40	-	MHz
	Thermal Resistance Junction to Ambient[b]	Rt_ja	-	-	60	°C/W
	Maximum Operation Junction Temperature	Tj_max	-	-	150	°C
	Maximum Collector Current	Ic_max	-	-	1	A
	Maximum Power Dissipation[e]	Pmax	-	-	1.2	W

a. Vce = 0.4 V DC; Ic = 1 A; T = 25 °C.
b. The thermal resistance feature depends on the PNP package along with the board layout including: number of layers, layer thickness, copper area for collector pad, and component locations.
c. Ta = 70 °C; Vin = 3.6 V DC; Vout = 1.71 V DC; I = 0.95 A; 1.4 Ω 5% Series Resistor.
d. Vce = 1 V DC; Ic = 0.5 A; T = 25 °C.
e. Ta = 70 °C; Vin = 3.6 V DC; Vout = 1.7 1 V DC; I = 0.55 A.

3.5.2.6 PNP Transistor Specification for 1.0V DC LVR

Table 20. PNP Specification for 1.0V DC LVR

PNP Connection	Description	Symbol	Min	Typ	Max	Units
PNP Transistor for 1.0V DC LVR	dc Gain[a]	β	60	-	400	-
	Transition Frequency	fT	-	40	-	MHz
	Thermal Resistance Junction to Ambient[b]	Rt_ja	-	-	60	°C/W
	Maximum Operation Junction Temperature	Tj_max	-	-	150	°C
	Maximum Collector Current	Ic_max	-	-	1	A
	Maximum Power Dissipation[c]	Pmax	-	-	1.1	W

a. Vce = -1.0 V DC; Ic = 0.5 A; T = 25 °C.
b. The thermal resistance feature depends on the PNP package along with the board layout including: number of layers, layer thickness, copper area for collector pad, and component locations.
c. Ta = 70 °C; Vin = 3.6 V DC; Vout = 0.95 V DC; I = 0.4 A

3.5.3 Crystal

Table 21 lists the recommended crystal specifications for operation with the 82566.

Table 21. Crystal Specifications (Sheet 1 of 2)

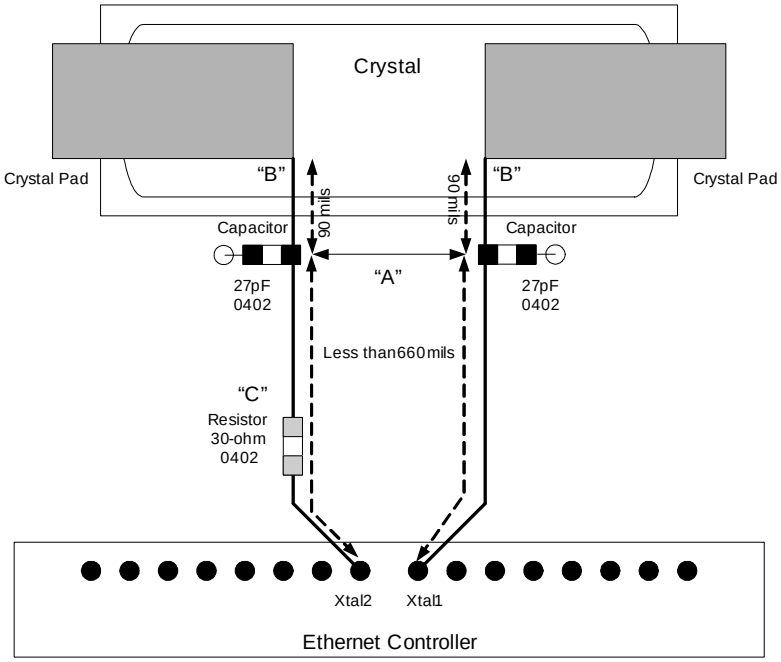
Parameter Name	Symbol	Recommended Value	Max/Min Range	Conditions
Frequency	f_o	25.000 MHz	-	@25 °C
Vibration mode	-	Fundamental	-	-
Cut	-	AT	-	-
Operating/Calibration Mode	-	Parallel	-	-
Frequency Tolerance	$\Delta f/f_o$ @25°C	±30 ppm	[a]	@25 °C
Temperature Tolerance	$\Delta f/f_o$	±30 ppm	[a]	-
Operating Temperature	T_{opr}	-20 to +70 °C	[a]	-
Non Operating Temperature	T_{opr}	-40 to +90 °C	-	-
Equivalent Series Resistance (ESR)	R_S	10 Ω	50 Ω	@25 MHz
Load Capacitance	C_{load}	20 pF (max 24 pF)	[a]	-
Shunt Capacitance	C_o	6 pF	[a]	-
Pullability from Nominal Load Capacitance	$\Delta f/C_{load}$	15 ppm/pF max	-	-
Max Drive Level	D_L	500 µW	-	-
Insulation Resistance	IR	500 MΩ min		@ 100V DC
Aging	$\Delta f/f_o$	±5 ppm per year	±5 ppm per year	-

Table 21. Crystal Specifications (Sheet 2 of 2)

Parameter Name	Symbol	Recommended Value	Max/Min Range	Conditions
Differential Board Capacitance	C_D	2 pF	b	
Board Capacitance	C_s	4 pF	c	-
External Capacitors	C_1, C_2	27 pF	a	-
Board Resistance	R_s	0.1 Ω	1 Ω	-

a. When not using values within 1% of the recommended values, the following procedures must be used:
   1. On the board with the crystal and the 82566, measure the clock at the output of the receive and transmit lines.
   2. Change C_1 and C_2 to meet with the 25 MHz requirement.
   3. Ensure the demand on the 25 MHz clock has a deviation of less then 100 ppm (for example, 25 ± 0.0025 MHz).
   4. If the measured frequency is higher then 25.0025 MHz, replace capacitors C_1 and C_2 with larger capacitors.
   5. If the measured frequency is lower then 24.9975 MHz, replace capacitors C_1 and C_2 with smaller capacitors.
b. Differential board capacitance is the capacitance between Ser_CLK_PLUS and Ser_CLK_MINUS.
c. Board capacitance is the differential capacitance between the input and output. This parasitic capacitance must be less than or equal to the specification. This value can change up to 10%. The procedures listed in footnote “a” must be followed to comply with the ppm specification.

Figure 4. Crystal Connectivity to the 82566



Note: Refer to Technical Advisory (TA-181), the 82566 Board Layout Checklist, and the 82566 Design Checklist for details relating to Figure 4.

3.6 Power Consumption

This section lists the estimated targets for the 82566 power. The numbers apply to the device current and power but do not include power losses on external components.

Table 22. Power Consumption (82566MC/MM)

System State	Link State	3.3V Current (mA)	1.8V Current (mA)	1.0V Current (mA)	82566 Device Only Power (mW) External LVR	Solution Power[a] (mW)
So (Max)	1000 Mbps Active	28	440	297	1180	2525
S0 (Typ)	1000 Mbps Active	26	441	281	1161	2468
	1000 Mbps Idle	25	442	263	1141	2409
	100 Mbps Active	33	145	56	424	772
	100 Mbps Idle	27	145	56	405	752
	10 Mbps Active	17	148	19	343	607
	10 Mbps Idle	15	46	18	150	261
	Cable Disconnect (no SPD, LVR on)	15	46	18	150	261
	Cable Disconnect (SPD, LVR on)	17	24	10	108	168
	Cable Disconnect (no Intel® ACBS[b], LVR off, no wake)	12	0	0	40	40
	Cable Disconnect (Intel® ACBS, LVR off, wake)[c]	12	0	0	40	40
	Cable Disconnect (Intel® ACBS, 3.3V power disabled, wake)[c]	0	0	0	0	0
Sx (Typ)	100 Mbps Idle (wake)	29	144	56	411	756
	10 Mbps Idle (wake)	19	46	18	159	271
	No Link (no wake) - PD, LVR off	12	0	0	40	40
	LAN Disable	12	0	0	40	40

a. Solution power is the total amount of power from the 3.3V supply required for the 82566 to operate. In its mathematical form: solution power = (82566 current) * 3.3V. The 3.3V is assumed since this is the normal voltage rail provided to the LAN solution.
b. Intel® ACBS refers to the Intel® Auto-Connect Battery Saving feature.
c. An additional 7 mW of power is consumed on the 3.3V rail by the external link detect circuitry while the device is in ACBS mode.

Table 23. Power Consumption (82566DC/DM)

System State	Link State	3.3V Current (mA)	1.8V Current (mA)	1.0V Current (mA)	82566 Device Only Power (mW) External LVR	Solution Power[a] (mW)
So (Max)	1000 Mbps Active	28	440	297	1180	2525
S0 (Typ)	1000 Mbps Active	26	441	281	1161	2468
	1000 Mbps Idle	25	442	263	1141	2409
	100 Mbps Active	33	145	56	424	772
	100 Mbps Idle	27	145	56	405	752
	10 Mbps Active	17	148	19	343	607
	10 Mbps Idle	15	46	18	150	261
	Cable Disconnect (no SPD, LVR on)	15	46	18	150	261
	Cable Disconnect (SPD, LVR on)	17	24	10	108	168
Sx (Typ)	100 Mbps Idle (wake)	29	144	56	411	756
	10 Mbps Idle (wake)	19	46	18	159	271
	No Link Idle (wake)	21	109	50	180	292
	No Link (no wake) - PD	12	0	0	40	40
	LAN Disable	12	0	0	40	40

a. Solution power is the total amount of power from the 3.3V supply required for the 82566 to operate. In its mathematical form: solution power = (82566 current) * 3.3V. The 3.3V is assumed since this is the normal voltage rail provided to the LAN solution.

The current from the 82566 does not change regardless of generating the 1.0V using the on-die transistor or an external pass transistor. The total current demand remains constant, but the power dissipated by the 82566 package changes. The 1.0V power is either on-die or at the external pass transistor.

4.0 Package and Pinout Information

The physical characteristics of the 82566 are described in this section. The pin number to signal mapping is indicated in Section 4.5.

4.1 Package Information

The package used for the 82566 is an 81-pin, 10 mm x 10 mm, small footprint FCMMAP (BGA) with a ball pitch of 1.0 mm.

Figure 5. Mechanical Drawing (1 of 4)

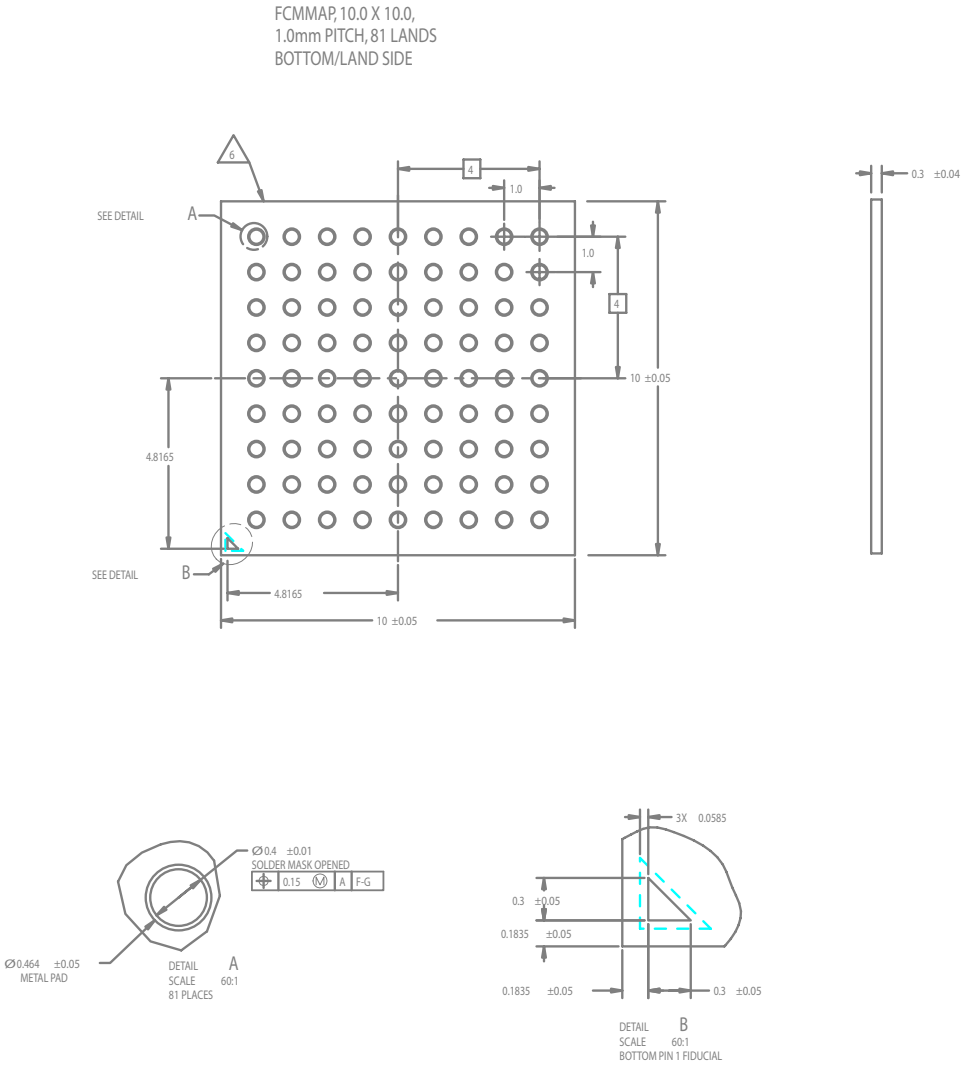


Figure 6. Mechanical Drawing (2 of 4)

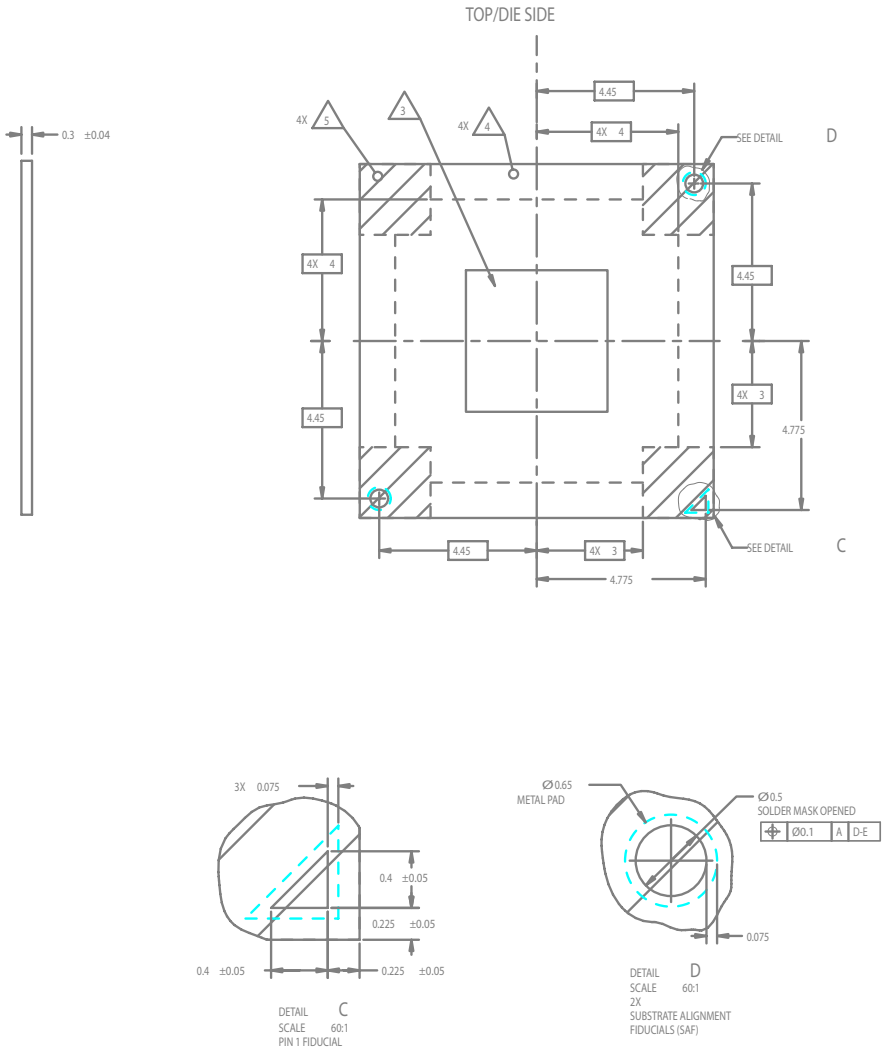


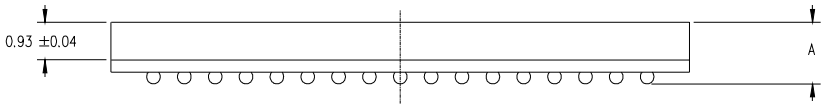
Figure 7. Mechanical Drawing (3 of 4)

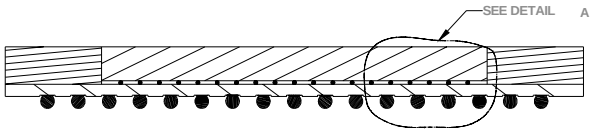
NOTES:

1). DIMENSION APPLY AFTER SOLDER BALL REFLOW.

2). INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5M-1994.

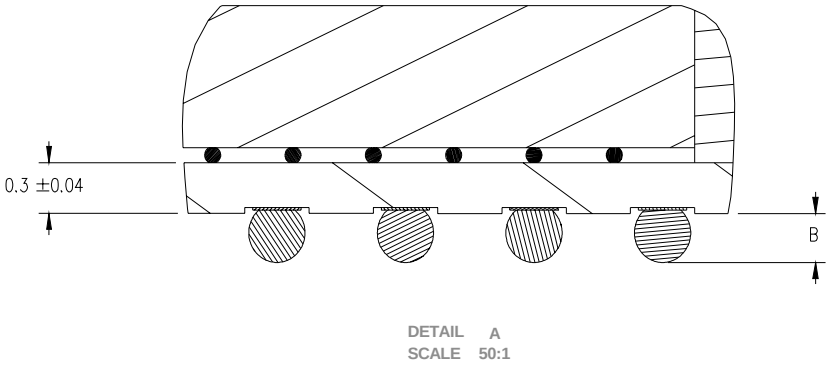
3). DIMENSION ENCLOSED IN PARENTHESES ARE FOR REFERENCE ONLY





ITEM	DIMENSION	INCOMING BALL SIZE(mm)	DETAIL
A	1.745±0.07	N/A	1.0 mm BALL PITCH
B	0.515±0.035	0.610	1.0 mm BALL PITCH

Figure 8. Mechanical Drawing (4 of 4)



4.2 Thermal

The 82566 is specified for operation when the Ambient Temperature (TA) is within the range of 0 °C to 55 °C. For information about the thermal characteristics of the 82566, including operation outside this range, refer to the *82566 Gigabit Platform LAN Connect Thermal Design Considerations* Application Note.

4.3 Internal Pull-Up Resistors

Table 24 lists the internal pull-up resistors and their functionality in different device states. Each internal pull-up resistor has a nominal value of 5 KΩ, ranging from 2.7 KΩ to 8.6 KΩ.

Table 24. Internal Pull-Up Resistors

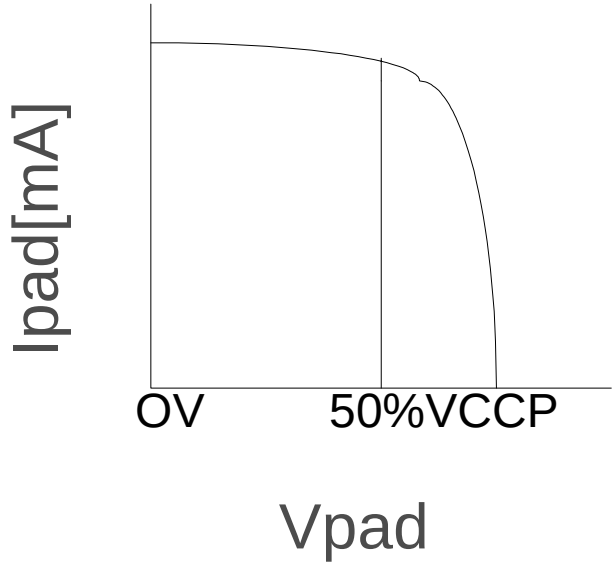
Signal Name (Ball Location)	Default State	Power-Down State[a]
LED0 (A4)	Not connected	Connected
LED1 (B4)	Not connected	Connected
LED2 (A5)	Not connected	Connected
JTAG_TCK (G1)	Not connected	Connected
JTAG_TDI (H1)	Connected	Connected
JTAG_DO (G3)	Not connected	Connected
JTAG_TMS (G2)	Connected	Connected
JTXD[2:0] (F1, F3, D1)	Not connected	Connected
JRXD[2:0] (C1, D2, D3)	Not connected	Connected

a. This column describes the state of the internal pull-up resistors in device power-down mode when the internal voltage regulators are shut down.

4.4 Pull-Up and Pull-Down Current

1. External R pull-down recommended value: ≤ 400 Ω
2. External R pull-up recommended value: ≤ 3 KΩ
3. External buffer recommended strength: ≥ 2 mA
4. As the internal pull-up acts as a current source, the external pull-down resistor can be as low as required without raising the output current.

Figure 9. V_{pad} versus I_{pad}



5. The internal pull-up maximum was characterized at the fast corner (0C, VCCP=3.6V, process fast).
6. The internal pull-up minimum was characterized at the slow corner (115C, VCCP=2.9V, process slow).

4.5 Visual Pin Assignments

Figure 10. 82566 Pinout (Top View - Balls Down)

VSSA	VSSA	RSV	RSV	VSSA	GLAN_ RXP	VSSA	GLAN_ TXN	VSSA	J
MDI_ MINUS[3]	MDI_ PLUS[3]	KBIAS_N	XTAL1	XTAL2	GLAN_ RXN	VCCFC1P0	GLAN_ TXP	JTAG_TDI	H
VSSA	VSSA	KBIAS_P	VSSA	VCC1P8	VCC1P0	JTAG_ TDO	JTAG_ TMS	JTAG_ TCK	G
MDI_ PLUS[2]	MDI_ MINUS[2]	VDD1P0	VSSA	VCC1P8	VSS	JTXD1	VCC3P3	JTXD2	F
VSSA	VDD1P0	RBIAS_P	RBIAS_N	VCCF1P0	VCC	JRSTSYNC	JKCLK	VSS	E
MDI_ PLUS[1]	MDI_ MINUS[1]	VDD1P0	VSSA	VCC1P8	VCC	JRXD0	JRXD1	JTXD0	D
VSSA	VSSA	VSSA	VSSA	RSV	VSS	CTRL_10	VCC1P8	JRXD2	C
MDI_ MINUS[0]	MDI_ PLUS[0]	IEEE_ TEST_N	TEST_EN	RSV	LED1	VCC3P3	CTRL_18	V1P0_ OUT	B
VSSA	VSSA	IEEE_ TEST_P	RSV	LED2	LED0	THERM_ D_N	THERM_ D_P	VSS	A
9	8	7	6	5	4	3	2	1	

NOTE: Some names in the pinout in Figure 10 may differ from the signal names in order for the pinout to be more easily read.