



# 82563EB/82564EB Gigabit Platform LAN Connect

Networking Silicon

Datasheet

## Product Features

- IEEE 802.3ab compliant
  - Robust operation over the installed base of Category-5 (Cat-5) twisted pair cabling
- PICMG 3.1 compliant
  - Robust operation in backplane over Ethernet applications.
- Support for cable line lengths greater than 100 m (spec); 123 m physical
  - Robust end to end connections over various cable lengths
- Full duplex at 10, 100, or 1000 Mb/s and half duplex at 10 or 100 Mb/s.
- IEEE 802.3ab Auto-negotiation with Next Page support
  - Automatic link configuration including speed, duplex, and flow control
- 10/100 downshift
  - Automatic link speed adjustment with poor quality cable
- Automatic MDI crossover
  - Helps to correct for infrastructure issues
- Advanced Cable Diagnostics
  - Improved end-user troubleshooting
- Kumeran interface
  - Low pin count, high speed interface to the Intel® 631xESB/632xESB I/O Controller Hub
    - Allows PHY placement proximity to I/O back panel.
- 7 LED outputs per port (4 configurable plus 3 dedicated)
  - Link and Activity indications (10, 100, 1000 Mb/s) on each port
- Clock supplied to the 631xESB/632xESB
  - Cost optimized design
- Full chip power down
  - Support for lowest power state
- 100 pin TQFP Package
  - Smaller footprint and lower power dissipation compared to multi-chip MAC and PHY solutions
- Operating temperature: 0°C to 60° C (maximum) – heat sink or forced airflow not required
  - Simple thermal design
- Power Consumption: < 1.0 Watts per port (silicon power)
  - Minimize impact of incorporating dual Gigabit instead of Fast Ethernet
- Leaded and lead-free<sup>a</sup> 100-pin TQFL with an Exposed-Pad\*. Devices that are lead-free are marked with a circled “e3” and have a product code: HYXXXXX

a. This device is lead-free. That is, lead has not been intentionally added, but lead may still exist as an impurity at <1000 ppm. The Material Declaration Data Sheet, which includes lead impurity levels and the concentration of other Restriction on Hazardous Substances (RoHS) -banned materials, is available at:

[ftp://download.intel.com/design/packtech/material\\_content\\_IC\\_Pack](ftp://download.intel.com/design/packtech/material_content_IC_Pack)

In addition, this device has been tested and conforms to the same parametric specifications as previous versions of the device. For more information regarding lead-free products from Intel Corporation, contact your Intel Field Sales representative.



# Revision History

| Date       | Revision | Comments   |
|------------|----------|--|
| Nov 2007   | 2.9      | Updated Tables 19, 20, 23, and 24. Updated Figures 5 and 6.  |
| Oct 2007   | 2.8      | Updated Table 16 "Recommended Operating Conditions".   |
| April 2007 | 2.7      | Updated Section 4.2, Table 16 "Core Digital Voltage Range".  |
| Feb 2007   | 2.6      | Updated Table 6.   |
| May 2006   | 2.5      | Initial public release.  |
| April 2006 | 2.1      | Removed "Preliminary" from section 4.9 "Power Consumption".<br>Updated 1.9V external power supply parameters in Tables 16 and 19.  |
| Nov 2005   | 2.0      | Initial release (Intel Confidential).  |
| Aug 2005   | 1.75     | Added lead-free information.<br>Added measured power consumption values.<br>Updated crystal specifications (drive level now 750 $\mu$ W).<br>Changed 1.8V power rail references to 1.9V. |
| Dec 2004   | 1.0      | Major revisions in all sections.   |
| Sep 2004   | 0.70     | Added power sequencing.  |
| Jul 2004   | 0.51     | Changed pin 51 (page 13) from AVDD (1.8V) to AVDDR (3.3V).   |
| May 2004   | 0.5      | Initial release (Intel Secret).  |

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## 1.0 Introduction

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The Intel® 82563EB Gigabit Platform LAN Connect is a dual, compact Physical Layer Transceiver (PHY) component designed for 10/100/1000 Mb/s operation. This device uses the Kumeran interface port of the 631xESB/632xESB I/O Controller Hub enabling the routing of long distances up to 28 inches (~711 mm). The 82564EB Gigabit Platform LAN Connect is the single port implementation. The Intel® 82563EB and 82564EB allow for Gigabit Ethernet implementations in a very small package; easing routing constraints from the 631xESB/632xESB I/O Controller Hub to the PHY.

The Intel® 82563EB/82564EB devices are based upon proven PHY technology integrated into Intel's Gigabit Ethernet Controllers. The physical layer circuitry provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The 82563EB/82564EB devices are capable of transmitting and receiving data at rates of 1000 Mb/s, 100 Mb/s, or 10 Mb/s.

### 1.1 Document Scope

This document contains datasheet specifications for the 82563EB/82564EB Gigabit Platform LAN Connect, including signal descriptions, DC and AC parameters, packaging data, and pinout information.

### 1.2 Reference Documents

This document assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide application information:

- *82563EB/82564EB LAN on Motherboard Design Guide (AP-467)*, Intel Corporation.
- *82563EB/82564EB Gigabit Platform LAN Connect Specification Update*, Intel Corporation.
- *631xESB/632xESB I/O Controller Hub EEPROM Information Guide Application Note (AP-477)*, Intel Corporation.
- *82571/82572/ESB2 LAN System Manageability Application Note (AP-497)*, Intel Corporation.
- *IEEE Standard 1149.1*, 2001 Edition (JTAG). Institute of Electrical and Electronics Engineers (IEEE).
- *IEEE Standard 802.3*, 2002 Edition. Incorporates various IEEE Standards previously published separately. Institute of Electrical and Electronic Engineers (IEEE).
- *Intel® 631xESB/632xESB I/O Controller Hub External Design Specification (EDS)*, Volumes 1-3, Intel Corporation.
- *Bensley/Bensley-VS Platform Design Guide (PDG)*, Intel Corporation.
- *PICMG3.1 Ethernet/Fiber Channel Over PICMG 3.0 Draft Specification*, September 4, 2002, Version 0.90. PCI Industrial Computer Manufacturers Group (PICMG).

Software driver developers should contact their local Intel Representatives for programming information.



### 1.3 Product Codes

The following Table 1 lists the product ordering codes for the 82563EB dual port device and the 82564EB single port device.

**Table 1. Product Ordering Codes**

| Device                  | Product Code |
|-------------------------|--------------|
| Dual Port (Leaded)      | HU82563EB    |
| Single Port (Leaded)    | HU82564EB    |
| Dual Port (Lead Free)   | HY82563EB    |
| Single Port (Lead Free) | HY82564EB    |





## 2.0 Block Diagrams

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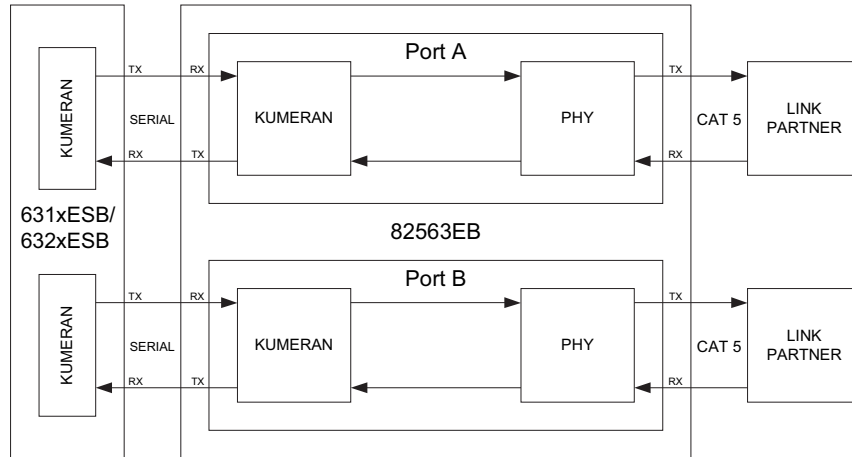


Figure 1. 82563EB Dual Port Block Diagram

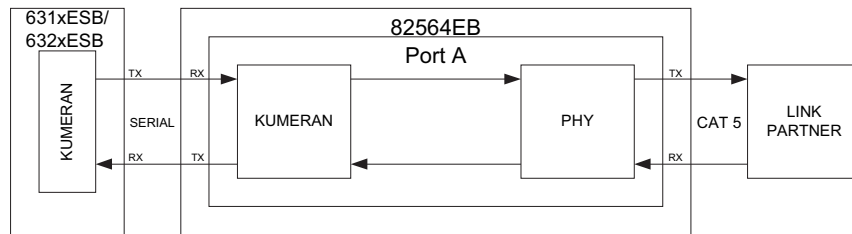


Figure 2. 82564EB Single Port Block Diagram



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## 3.0 Signal Descriptions

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### 3.1 Signal Type Definitions

The signals of 82563EB/82564EB are defined as follows:

- **I:** Standard input-only signal
- **I (T):** Functional input signal implemented as a bidirectional for test
- **O:** Standard output-only signal
- **O (T):** Functional output signal implemented as a bidirectional for test
- **I/O:** Bi-directional, tri-state input/output signal
- **A:** Analog signal
- **A-in:** Analog input signal
- **A-o:** Analog output signal
- **P:** Power signal
- **G:** Ground signal
- **NC:** No connect (these signals must not be connected to any traces or planes)
- **B:** Input bias

Signals may be further qualified to indicate whether an internal pull-up or pull-down is normally active. Unless otherwise stated, internal pull-up and pull-down impedances are between 50 K $\Omega$  and 130 K $\Omega$ .

- **PU:** Internal pull-up to VDD
- **PD:** Internal pull-down to VSS

**Note:** It may be desirable to leave some input signals as no-connects in certain system applications that rely on a device's internal pull-up or pull-down signal to be active. Care should be taken to ensure there are no long traces, such as far-away test points or errant trace routings, on any inputs which rely solely on internal pull-devices. Excess capacitance of dangling traces may generate charge and/or noise on inputs which exceeds the capability of the internal pull-device, leading to unpredictable component behavior.

In addition to a primary type, each pin can be classified according to one of the following sub-types based on its electrical characteristics, such as input and output voltages and drive strengths.

- **TTL:** TTL compatible inputs
- **TTL3:** TTL compatible pins with at least 3mA drive strength
- **TTL6:** TTL compatible pins with at least 6mA drive strength
- **TTL8:** TTL compatible pins with at least 8mA drive strength
- **TTL12:** TTL compatible pins with at least 12mA drive strength



## 3.2 Shared PHY Pins

Table 1. Shared PHY Pins

| Signal Name | Pin | Type | Sub-Type | Description   |
|-------------|-----|------|----------|---|
| PHY_REF     | 50  | B    | B        | <b>PHY Reference</b><br>External 4.99 K $\Omega$ $\pm$ 1% resistor connection to VSS. |

## 3.3 MDIO Interface

Table 2. MDIO Interface Pins

*Note:* For normal operation, the MDIO interface is strapped externally according to Table 39 due to MDIO being an in-band operation.

| Signal Name  | Pin                  | Type      | Sub-Type | Description   |
|--|----------------------|-----------|----------|---|
| MDC  | 77                   | I (T)     | TTL      | <b>Management Data Clock</b><br>This signal is received from the 631xESB/632xESB as a clock timing reference for information transfer on the MDIO signal. It is not required to be a continuous signal and can be frozen when no management data is transferred. This signal has a maximum operating frequency of 2.5 MHz.<br>A 1 - 10 K $\Omega$ $\pm$ 5% pull-down resistor should be connected to this pin.                                    |
| MDIO   | 76                   | I/O<br>PU | TTL6     | <b>Management Data Input/Output</b><br>Bi-directional data signal of the management data interface. This pin has an internal pull-up. This signal can be left disconnected (or pulled up) if not used.  |
| MDIO_ADD[0]<br>MDIO_ADD[1]<br>MDIO_ADD[2]<br>MDIO_ADD[3] | 78<br>79<br>18<br>19 | I (T)     | TTL      | <b>Bits 4:1 of MDIO address</b><br>These bits are latched at the assertion of PHY_PWR_GOOD or the de-assertion of PHY_RESET_N or PHY_SLEEP. They set the MDIO address as follows: <ul style="list-style-type: none"> <li>• bit 1 = MDIO_ADD[0]</li> <li>• bit 2 = MDIO_ADD[1]</li> <li>• bit 3 = MDIO_ADD[2]</li> <li>• bit 4 = MDIO_ADD[3]</li> </ul> A 1 - 10 k $\Omega$ $\pm$ 5% pull-down resistor should be connected to each of these pins. |



### 3.4 Port A PHY Interface

*Note:* Port A on the 82563EB/82564EB corresponds to connection to Port 0 on the 631xESB/632xESB.

**Table 3. Port A PHY Interface Pins**

| Signal Name                   | Pin      | Type | Sub-Type | Description   |
|-------------------------------|----------|------|----------|---|
| MDIA_PLUS[0]<br>MDIA_MINUS[0] | 27<br>28 | A    | A        | <p><b>Media Dependent Interface for Port A, bit 0</b></p> <p>1000BASE-T: In MDI configuration, MDI[0]+/- corresponds to BI_DA+/- and in MDIX configuration MDI[0]+/- corresponds to BI_DB+/-.</p> <p>100BASE-TX: In MDI configuration, MDI[0]+/- is used for the transmit pair and in MDIX configuration MDI[0]+/- is used for the receive pair.</p> <p>10BASE-T: In MDI configuration, MDI[0]+/- is used for the transmit pair and in MDIX configuration MDI[0]+/- is used for the receive pair.</p> |
| MDIA_PLUS[1]<br>MDIA_MINUS[1] | 31<br>32 | A    | A        | <p><b>Media Dependent Interface for Port A, bit 1</b></p> <p>1000BASE-T: In MDI configuration, MDI[1]+/- corresponds to BI_DB+/- and in MDIX configuration MDI[1]+/- corresponds to BI_DA+/-.</p> <p>100BASE-TX: In MDI configuration, MDI[1]+/- is used for the receive pair and in MDIX configuration MDI[1]+/- is used for the transmit pair.</p> <p>10BASE-T: In MDI configuration, MDI[1]+/- is used for the receive pair and in MDIX configuration MDI[1]+/- is used for the transmit pair.</p> |
| MDIA_PLUS[2]<br>MDIA_MINUS[2] | 33<br>34 | A    | A        | <p><b>Media Dependent Interface for Port A, bit 2</b></p> <p>1000BASE-T: In MDI configuration, MDI[2]+/- corresponds to BI_DC+/- and in MDIX configuration MDI[2]+/- corresponds to BI_DD+/-.</p> <p>100BASE-TX: Unused.</p> <p>10BASE-T: Unused.</p>   |
| MDIA_PLUS[3]<br>MDIA_MINUS[3] | 36<br>37 | A    | A        | <p><b>Media Dependent Interface for Port A, bit 3</b></p> <p>1000BASE-T: In MDI configuration, MDI[3]+/- corresponds to BI_DD+/- and in MDIX configuration MDI[3]+/- corresponds to BI_DC+/-.</p> <p>100BASE-TX: Unused.</p> <p>10BASE-T: Unused.</p>   |
| LINK_A                        | 65       | I/O  | TTL8     | <p><b>PHY A Link Indication</b></p> <p>This signal is registered at the rising edge of PHY_PWR_GOOD, and is used to determine the clock speed used for PHY_CLK_OUT. Once PHY_PWR_GOOD is 1, LINK_A will always be an output and indicate link up.</p>   |



## 3.5 Port A Kumeran Interface

Table 4. Port A Kumeran Interface Pins

| Signal Name            | Pin      | Type | Sub-Type | Description  |
|------------------------|----------|------|----------|--|
| TXA_PLUS,<br>TXA_MINUS | 90<br>91 | A-o  | A        | <b>Port A KumeranTX Pair</b><br>Differential Kumeran Transmit interface. |
| RXA_PLUS,<br>RXA_MINUS | 93<br>94 | A-in | A        | <b>Port A Kumeran RX Pair</b><br>Differential Kumeran Receive interface. |

## 3.6 Port A LEDs

Table 5. Port A LEDs

| Signal Name       | Pin | Type | Sub-Type | Description  |
|-------------------|-----|------|----------|--|
| LEDA_LINK_UP_N    | 73  | O    | TTL12    | <b>LED 0 – Link Up LED</b><br>This corresponds to port 0's LED#0 from the 631xESB/632xESB.   |
| LEDA_ACTIVITY_N   | 72  | O    | TTL12    | <b>LED 1 – 10 Mbps LED</b><br>This corresponds to port 0's LED#1 from the 631xESB/632xESB.   |
| LEDA_SPEED_100_N  | 71  | O    | TTL12    | <b>LED 2 – 100 Mbps LED</b><br>This corresponds to port 0's LED#2 from the 631xESB/632xESB.  |
| LEDA_SPEED_1000_N | 70  | O    | TTL12    | <b>LED 3 – 1000 Mbps LED</b><br>This corresponds to port 0's LED#3 from the 631xESB/632xESB.   |
| LEDA_DUPLEX       | 68  | O    | TTL12    | <b>LED 4 – Full Duplex LED</b><br>This LED will light when port 0's PHY is operating in Full Duplex Mode   |
| LEDA_TX_ACTIVITY  | 67  | O    | TTL12    | <b>LED 5 – Transmit Activity LED</b><br>This LED will light when the port 0's PHY transmits a packet   |
| LEDA_RX_ACTIVITY  | 66  | O    | TTL12    | <b>LED 6 – Receive Activity LED</b><br>This LED will light when the port 0's PHY receives a packet<br>This pin also functions as the clock view pin and will output clock signals required for IEEE conformance testing. This pin should have a stuffing option for a test header. |



### 3.7 Reset, Power Down, and Initialization Signals

Table 6. Reset and Power Down Signals

| Signal Name  | Pin | Type  | Sub-Type | Description   |
|--------------|-----|-------|----------|---|
| PHY_PWR_GOOD | 83  | I     | TTL      | <b>Power Good (Power-On Reset)</b><br>The PHY_PWR_GOOD signal indicates good power is available for The device. When set to 0b, the entire chip will be held in a reset state.                        |
| PHY_RESET_N  | 81  | I     | TTL      | <b>Reset</b><br>When set to 0b, resets the device, including PHY and Kumeran logic. Needs an external pull-up resistor if the signal isn't continuously being driven from an external source.         |
| PHY_SLEEP    | 80  | I (T) | TTL      | <b>Sleep / Power Down</b><br>This will power down the PHY and the Kumeran of both ports. Needs an external pull-down resistor, if the signal isn't continuously being driven from an external source. |
| TEST_JTAG    | 95  | I PU  | TTL      | <b>Enable JTAG Pin Control</b><br>This pin should be pulled high through a 1 to 10 K $\Omega$ 5% resistor in normal operation.  |

### 3.8 JTAG and IEEE Interface

Table 7. JTAG Signals

| Signal Name | Pin | Type | Sub-Type | Description  |
|-------------|-----|------|----------|--|
| JTAG_TCK    | 100 | I    | TTL      | <b>JTAG Clock</b><br>This pin should be pulled high through a 1 to 10 K $\Omega$ 5% resistor in normal operation.        |
| JTAG_TDI    | 1   | I PU | TTL      | <b>JTAG Serial Data Input</b><br>If not using JTAG, this pin may be pulled high through a 1 to 10 K $\Omega$ 5% resistor |
| JTAG_TDO    | 99  | O    | TTL3     | <b>JTAG Serial Data Output</b>   |
| JTAG_TMS    | 3   | I PU | TTL      | <b>JTAG TMS Input</b><br>If not using JTAG, this pin may be pulled high through a 1 to 10 K $\Omega$ 5% resistor         |



### 3.9 Reserved Signals

Table 8. Test Signals

| Signal Name | Pin   | Type  | Sub-Type | Description  |
|-------------|---|-------|----------|--|
| RESERVED_NC | 4<br>5<br>6<br>8<br>9<br>10<br>13<br>14<br>15<br>17<br>26<br>49<br>52<br>53<br>98 | NC    | NC       | <p><b>Reserved No Connect</b></p> <p>This pin should be left disconnected in normal operation. Connecting any of these pins may cause adverse effects and will not be supported.</p> |
| RESERVED_PD | 82  | I (T) | TTL      | <p><b>Reserved, Pull-down</b></p> <p>This signal used in the XOR chain. It should be pulled to VSS via a 1 to 10 K<math>\Omega</math> resistor.</p>                                  |

### 3.10 Voltage Control Pins

Table 9. Voltage Control Pins

| Signal Name | Pin | Type | Sub-Type | Description  |
|-------------|-----|------|----------|--|
| CTRL_18     | 25  | A    | A        | <p>1.9V LVR Power Output Reference</p> <p>Voltage control for an external 1.9V PNP transistor in order to produce a linearly-regulated supply.</p> <p>If the 1.9V internal voltage regulator control circuit is not used, connect the CTRL_18 pin to VSS through a 10 K<math>\Omega</math> resistor.</p> |
| CTRL_12     | 23  | A    | A        | <p>1.2V LVR Power Output Reference</p> <p>Voltage control for an external 1.2V PNP transistor in order to produce a linearly-regulated supply.</p> <p>If the 1.2V internal voltage regulator control circuit is not used, connect the CTRL_12 pin to VSS through a 10 K<math>\Omega</math> resistor.</p> |





### 3.11 Clock Generator Interface

Table 10. Clock Generator Related Signals

| Signal Name | Pin | Type | Sub-Type | Description  |
|-------------|-----|------|----------|--|
| XTAL1       | 21  | I    | TTL      | <b>25 MHz Clock/Crystal Input</b><br>25 MHz +/- 50 ppm input. Can be connected to an oscillator or a crystal. If using a crystal, XTAL2 must be connected as well. If a crystal is used, it must be placed within ½-inch of the XTAL1 and XTAL2 chip pins.   |
| XTAL2       | 20  | A-o  | A        | <b>25 MHz Crystal Output</b><br>Output of internal oscillator circuit used to drive crystal into oscillation. If using an oscillator, XTAL2 is left as a no connect.   |
| PHY_CLK_OUT | 96  | O    | TTL8     | <b>Clock Output</b><br>Output clock available for use by a 631xESB/632xESB or other component(s).<br>The speed depends on the how LINK_A is sampled at LAN_PWR_GOOD assertion:<br>If LINK_A is 0b, the clock speed is 62.5 MHz.<br>If LINK_A is 1b, the clock speed is 25 MHz.<br><br>The output clock can be disabled depending on how LINK_B is sampled at LAN_PWR_GOOD assertion:<br>If LINK_B is 0b: Clock output enabled (pulled-down).<br>If LINK_B is 1b: Clock output disabled (no connect). |

### 3.12 Power/Ground Pins

Table 11. Power/Ground Pins (Sheet 1 of 2)

| Signal Name | Pin                        | Type | Sub-Type | Description   |
|-------------|----------------------------|------|----------|---|
| VSS         | Central Pad                | G    | G        | <b>Ground Exposed-Pad*</b><br>The ground is provided through a large central pad on the bottom side of the package. |
| VSS         | 89                         | G    | G        | <b>Ground</b>   |
| VDDO        | 11<br>22<br>60<br>75<br>97 | P    | P        | <b>3.3V I/O Ring Power</b>  |



Table 11. Power/Ground Pins (Sheet 2 of 2)

| Signal Name | Pin  | Type | Sub-Type | Description                              |
|-------------|--|------|----------|--|
| DVDD        | 2<br>7<br>12<br>16<br>59<br>64<br>69<br>74 | P    | P        | 1.2V Digital Power                       |
| AVDD        | 29<br>30<br>35<br>40<br>45<br>46           | P    | P        | 1.9V Analog Power for PHY                |
| AVDDF       | 86<br>92                                   | P    | P        | 1.9V Analog Power for Kumeran            |
| AVDDR       | 24<br>51                                   | P    | P        | 3.3V Analog Power for Voltage Regulators |



### 3.13 Port B PHY Interface

*Note:* Port B on the 82563EB dual port device corresponds to connection to Port 1 on the 631xESB/632xESB. There is no port B on the 82564EB.

**Table 12. Port B PHY Interface Pins (Sheet 1 of 2)**

| Signal Name                   | Pin      | Type | Sub-Type | Description  | Connection on 82564EB Single Port Device |
|-------------------------------|----------|------|----------|--|--|
| MDIB_PLUS[0]<br>MDIB_MINUS[0] | 48<br>47 | A    | A        | <b>Media Dependent Interface for Port B, bit 0</b><br>1000BASE-T: In MDI configuration, MDI[0] +/- corresponds to BI_DA +/- and in MDIX configuration MDI[0] +/- corresponds to BI_DB +/-.<br>100BASE-TX: In MDI configuration, MDI[0] +/- is used for the transmit pair and in MDIX configuration MDI[0] +/- is used for the receive pair.<br>10BASE-T: In MDI configuration, MDI[0] +/- is used for the transmit pair and in MDIX configuration MDI[0] +/- is used for the receive pair. | No-connect                               |
| MDIB_PLUS[1]<br>MDIB_MINUS[1] | 44<br>43 | A    | A        | <b>Media Dependent Interface for Port B, bit 1</b><br>1000BASE-T: In MDI configuration, MDI[1] +/- corresponds to BI_DB +/- and in MDIX configuration MDI[1] +/- corresponds to BI_DA +/-.<br>100BASE-TX: In MDI configuration, MDI[1] +/- is used for the receive pair and in MDIX configuration MDI[1] +/- is used for the transmit pair.<br>10BASE-T: In MDI configuration, MDI[1] +/- is used for the receive pair and in MDIX configuration MDI[1] +/- is used for the transmit pair. | No-connect                               |



Table 12. Port B PHY Interface Pins (Sheet 2 of 2)

| Signal Name                   | Pin      | Type   | Sub-Type | Description   | Connection on 82564EB Single Port Device |
|-------------------------------|----------|--------|----------|---|--|
| MDIB_PLUS[2]<br>MDIB_MINUS[2] | 42<br>41 | A      | A        | <b>Media Dependent Interface for Port B, bit 2</b><br>1000BASE-T: In MDI configuration, MDI[2] +/- corresponds to BI_DC +/- and in MDIX configuration MDI[2] +/- corresponds to BI_DD +/-.<br>100BASE-TX: Unused.<br>10BASE-T: Unused.                                    | No-connect                               |
| MDIB_PLUS[3]<br>MDIB_MINUS[3] | 39<br>38 | A      | A        | <b>Media Dependent Interface for Port B, bit 3</b><br>1000BASE-T: In MDI configuration, MDI[3] +/- corresponds to BI_DD +/- and in MDIX configuration MDI[3] +/- corresponds to BI_DC +/-.<br>100BASE-TX: Unused.<br>10BASE-T: Unused.                                    | No-connect                               |
| LINK_B                        | 54       | I/O PD | TTL8     | <b>PHY B Link Indication</b><br>This signal is registered at the rising edge of PHY_PWR_GOOD, and is used to determine whether PHY_CLK_OUT is output. See the PHY_CLK_OUT pin for details. Once PHY_PWR_GOOD is 1b, LINK_B will always be an output and indicate link up. | See Table 10                             |

### 3.14 Port B Kumeran Interface

Table 13. Port B Kumeran Interface Pins

| Signal Name           | Pin      | Type | Sub-Type | Description   | Connection on 82564EB Single Port Device |
|-----------------------|----------|------|----------|---|--|
| TXB_PLUS<br>TXB_MINUS | 88<br>87 | A-o  | A        | <b>Port B Kumeran TX Pair</b><br>Differential Kumeran Transmit interface. | No-connect                               |
| RXB_PLUS<br>RXB_MINUS | 85<br>84 | A-in | A        | <b>Port B Kumeran RX Pair</b><br>Differential Kumeran Receive interface.  | No-connect                               |



### 3.15 Port B LEDs

Table 14. Port B LEDs

| Signal Name       | Pin | Type | Sub-Type | Description  | Connection on 82564EB Single Port Device |
|-------------------|-----|------|----------|--|--|
| LEDB_LINK_UP_N    | 63  | O    | TTL12    | <b>LED 0 – Link Up/Activity LED</b><br>This corresponds to port 1's LED#0 from the 631xESB/632xESB.  | No-connect                               |
| LEDB_ACTIVITY_N   | 62  | O    | TTL12    | <b>LED 1 – 10 Mbps LED</b><br>This corresponds to port 1's LED#1 from the 631xESB/632xESB.   | No-connect                               |
| LEDB_SPEED_100_N  | 61  | O    | TTL12    | <b>LED 2 – 100 Mbps LED</b><br>This corresponds to port 1's LED#2 from the 631xESB/632xESB.  | No-connect                               |
| LEDB_SPEED_1000_N | 58  | O    | TTL12    | <b>LED 3 – 1000 Mbps LED</b><br>This corresponds to port 1's LED#3 from the 631xESB/632xESB.   | No-connect                               |
| LEDB_DUPLEX       | 57  | O    | TTL12    | <b>LED 4 – Full Duplex LED</b><br>This LED will light when port 1's PHY is operating in Full Duplex Mode   | No-connect                               |
| LEDB_TX_ACTIVITY  | 56  | O    | TTL12    | <b>LED 5 – Transmit Activity LED</b><br>This LED will light when port 1's PHY transmits a packet   | No-connect                               |
| LEDB_RX_ACTIVITY  | 55  | O    | TTL12    | <b>LED 6 – Receive Activity LED</b><br>This LED will light when port 1's PHY receives a packet<br><br>This pin also functions as the clock view pin and will output clock signals required for IEEE conformance testing. This pin should have a stuffing option for a test header. | No-connect                               |



*Note:* This page intentionally left blank.



## 4.0 Voltage, Temperature and Timing Specifications

### 4.1 Absolute Maximum Ratings

Table 15. Absolute Maximum Ratings<sup>a</sup>

| Symbol           | Parameter            | Min  | Max                   | Unit |
|------------------|----------------------|------|-----------------------|------|
| V <sub>DD</sub>  | DC supply voltage    | -0.3 | 4.6                   | V    |
| V <sub>IN</sub>  | Input voltage        | -1.0 | V <sub>DD</sub> + 0.3 | V    |
| I <sub>IN</sub>  | DC input pin current | -10  | 10                    | mA   |
| T <sub>STG</sub> | Storage temperature  | -40  | 125                   | °C   |

a. Maximum ratings are referenced to ground (VSS). Permanent device damage is likely to occur if the ratings in this table are exceeded for an indefinite duration. These values should not be used as the limits for normal device operations.

### 4.2 Recommended Operating Conditions

Table 16. Recommended Operating Conditions

| Symbol          | Parameter                    | Condition                    | Min  | Typ  | Max  | Unit |
|-----------------|------------------------------|------------------------------|------|------|------|------|
| T <sub>OP</sub> | Operating Temperature        | Convection only <sup>a</sup> | 0    |      | 60   | °C   |
| V <sub>DD</sub> | Periphery Voltage Range      | 3.3V                         | 3.00 | 3.30 | 3.60 | V    |
| V <sub>D</sub>  | Core Digital Voltage Range   | 1.2V                         | 1.08 | 1.20 | 1.32 | V    |
| V <sub>A</sub>  | Analog V <sub>DD</sub> Range | 1.9V                         | 1.80 | 1.90 | 2.09 | V    |

a. Higher ambient temperatures may be possible with forced airflow.

### 4.3 DC and AC Characteristics

Table 17. DC and AC Characteristics (Sheet 1 of 2)

| Symbol          | Parameter           | Condition | Min  | Typ | Max                   | Unit |
|-----------------|---------------------|-----------|------|-----|-----------------------|------|
| V <sub>IL</sub> | Voltage input LOW   | -         | -0.5 | -   | 0.8                   | V    |
| V <sub>IH</sub> | Voltage input HIGH  | -         | 2.0  | -   | V <sub>DD</sub> + 0.3 | V    |
| V <sub>OL</sub> | Voltage output LOW  | -         | -    | -   | 0.4                   | V    |
| V <sub>OH</sub> | Voltage output HIGH | -         | 2.4  | -   | -                     | V    |



Table 17. DC and AC Characteristics (Sheet 2 of 2)

| Symbol    | Parameter                            | Condition                           | Min | Typ     | Max | Unit       |
|-----------|--------------------------------------|-------------------------------------|-----|---------|-----|------------|
| $I_{OL}$  | Output current LOW                   |                                     |     |         |     |            |
|           | 3mA drivers (TTL3)                   | $V_{OL}$                            | 3   | -       | -   | mA         |
|           | 6mA drivers (TTL6)                   | $V_{OL}$                            | 6   | -       | -   | mA         |
|           | 12mA drivers (TTL12)                 | $V_{OL}$                            | 12  | -       | -   | mA         |
| $I_{OH}$  | Output current HIGH                  |                                     |     |         |     |            |
|           | 3mA drivers (TTL3)                   | $V_{OH}$                            | -3  | -       | -   | mA         |
|           | 6mA drivers (TTL6)                   | $V_{OH}$                            | -6  | -       | -   | mA         |
|           | 12mA drivers (TTL12)                 | $V_{OH}$                            | -12 | -       | -   | mA         |
| $I_{IN}$  | Input Current                        |                                     |     |         |     |            |
|           | TTL inputs                           | $V_{IN} = V_{DD}$ or $V_{SS}$       | -10 | $\pm 1$ | 10  | $\mu A$    |
|           | Inputs with pull-down resistors      | $V_{IN} = V_{DD}$                   | 23  |         | 72  | $\mu A$    |
|           | TTL inputs with pull-up resistors    | $V_{IN} = V_{SS}$                   | -23 |         | -72 | $\mu A$    |
| $I_{OZ}$  | 3-state output leakage current       | $V_{OH} = V_{DD}$ or $V_{SS}$       | -10 | $\pm 1$ | 10  | $\mu A$    |
| $C_{IN}$  | Input capacitance                    | Any input and bi-directional buffer | -   | 2.5     | -   | pF         |
| $C_{OUT}$ | Output capacitance                   | Any output buffer                   | -   | 2.0     | -   | pF         |
| $R_{PUD}$ | Internal Pull-up/down Resistor value | -                                   | 50  | -       | 130 | k $\Omega$ |

## 4.4 Power Supply Connections

There are two options in providing power to the 82563EB/82564EB:

- Connecting the 82563EB/82564EB to three external power supplies with nominal voltages of 3.3V, 1.9V, and 1.2V covered in Section 4.4.1.
- Powering the 82563EB/82564EB with only an external 3.3V supply, and using internal power regulators from the 82563EB/82564EB combined with external PNP transistors to supply the 1.9V and 1.2V levels. covered in Section 4.4.3.

### 4.4.1 External LVR Power Delivery

The following power supply requirements apply to designs in which the 82563EB/82564EB is supplied by external voltage regulators. These systems do not use the internal regulator logic built into the 82563EB/82564EB as described in Section 4.4.3.





**Table 18. 3.3V External Power Supply Parameters**

| Title                   | Description   | Min | Max  | Units |
|-------------------------|---|-----|------|-------|
| Rise Time               | Time from 10% to 90% mark   | 2   | 200  | ms    |
| Monotonicity            | Voltage dip allowed in ramp   | -   | 300  | mV    |
| Slope                   | Ramp rate at any given time between 10% and 90%<br>Min: 0.8*V(min)/Rise time (max)<br>Max: 0.8*V(max)/Rise time (min)   | -   | 1500 | mV/ms |
| Operational Range       | Voltage range for normal operating conditions   | 3.0 | 3.6  | V     |
| Ripple                  | Maximum voltage ripple (peak to peak) <sup>a</sup>  | -   | 100  | mV    |
| Overshoot               | Maximum overshoot allowed   | -   | 660  | mV    |
| Overshoot Settling Time | Maximum overshoot allowed duration.<br>(At that time delta voltage should be lower than 5 mV from steady state voltage) | -   | 3    | ms    |

a. The peak to peak output rippled is measured at 20 MHz Bandwidth within the operational range.

**Table 19. 1.9V External Power Supply Parameters**

| Title                   | Description   | Min  | Max  | Units |
|-------------------------|---|------|------|-------|
| Rise Time               | Time from 10% to 90% mark   | 2    | 200  | ms    |
| Monotonicity            | Voltage dip allowed in ramp   | -    | 180  | mV    |
| Slope                   | Ramp rate at any given time between 10% and 90%<br>Min: 0.8*V(min)/Rise time (max)<br>Max: 0.8*V(max)/Rise time (min)   | -    | 1500 | mV/ms |
| Operational Range       | Voltage range for normal operating conditions   | 1.80 | 2.09 | V     |
| Ripple                  | Maximum voltage ripple (peak to peak) <sup>a</sup>  | -    | 100  | mV    |
| Overshoot               | Maximum overshoot allowed   | -    | 360  | mV    |
| Overshoot Settling Time | Maximum overshoot allowed duration.<br>(At that time delta voltage should be lower than 5 mV from steady state voltage) | -    | 1.5  | ms    |
| Decoupling Capacitance  | Capacitance range   | 5    | -    | μF    |
| Capacitance ESR         | Equivalent series resistance of output capacitance  | -    | 100  | M Ω   |

a. The peak to peak output ripple is measured at 20 MHz Bandwidth within the operational range.



Table 20. 1.2V External Power Supply Parameters

| Title                  | Description   | Min  | Max  | Units |
|------------------------|---|------|------|-------|
| Rise Time              | Time from 10% to 90% mark   | 1.5  | 200  | ms    |
| Monotonicity           | Voltage dip allowed in ramp   | -    | 120  | mV    |
| Slope                  | Ramp rate at any given time between 10% and 90%<br>Min: 0.8*V(min)/Rise time (max)<br>Max: 0.8*V(max)/Rise time (min)   | -    | 1500 | mV/ms |
| Operational Range      | Voltage range for normal operating conditions   | 1.08 | 1.32 | V     |
| Ripple                 | Maximum voltage ripple (peak to peak) <sup>a</sup>  | -    | 100  | mV    |
| Overshoot              | Maximum overshoot allowed   | -    | 240  | mV    |
| Overshoot Duration     | Maximum overshoot allowed duration.<br>(At that time delta voltage should be lower than 5 mV from steady state voltage) | -    | 1    | ms    |
| Decoupling Capacitance | Capacitance range   | 5    | -    | μF    |
| Capacitance ESR        | Equivalent series resistance of output capacitance  | -    | 100  | MΩ    |

a. The peak to peak output ripple is measured at 20 MHz Bandwidth within the operational range. The ripple must be included within the operational range.

## 4.4.2 Power Sequencing with External Regulators

The following power-on/off sequence should be applied when external power supplies are in use.

Designs must comply with the required power sequence to avoid risk of either latch-up or forward biased internal diodes.

The general rule of thumb is that the 82563EB/82564EB power sequencing should power up the three power rails in the following order: 3.3V → 1.9V → 1.2V. However, if this general guideline is not followed, there are specific requirements that must be adhered that are listed in the following two sections.

### 4.4.2.1 External LVR Power up Sequencing and Tracking

Sequencing of the external supplies during power up may be necessary to ensure that the device is not electrically overstressed and does not latch-up. These requirements are shown in Figure 3.

- The 82563EB/82564EB core voltage (1.2V) cannot exceed the 3.3V supply by more than 0.5V at any time during the power up. The 82563EB/82564EB core voltage (1.2V) can not exceed the 1.9V supply by more than 0.5V at any time during the power up. The core voltage is not required to begin ramping before the 3.3V or the 1.9V supply.
- The 82563EB/82564EB analog voltage (1.9V) cannot exceed the 3.3V supply by more than 0.5V at any time during the power up. The analog voltage is not required to begin ramping before the 3.3V supply.

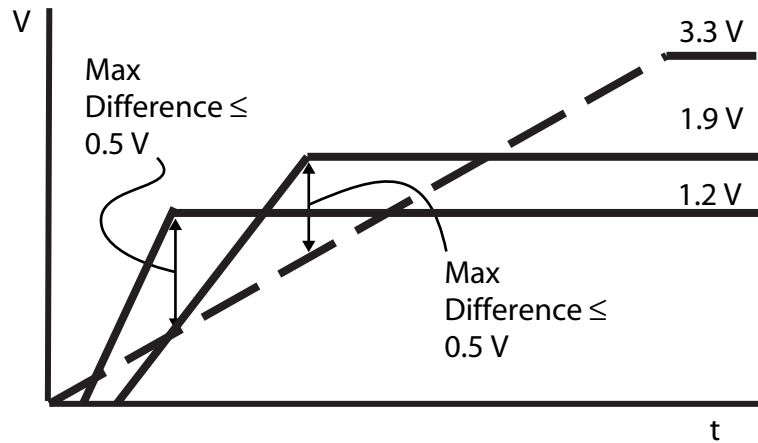


Figure 3. 82563EB/82564EB power up sequencing with external regulators

#### 4.4.2.2 External LVR Power down Sequencing

There are no specific power down sequencing and tracking requirements for the 82563EB/82564EB silicon. The risk of latch-up or electrical overstress is small because only the charge stored in the decoupling capacitors is left in the system.

#### 4.4.3 Internally-Generated Power Delivery

The 82563EB/82564EB has two internal linear voltage regulator controllers. The controllers use external transistors to generate 2 of the 3 required voltages: 1.9V (nominal) and 1.2V (nominal). These two voltages are stepped-down from a 3.3V source.

Table 21. 3.3V External Power Supply Parameters

| Title             | Description   | Min | Max  | Units |
|-------------------|---|-----|------|-------|
| Rise Time         | Time from 10% to 90% mark   | 2   | 200  | ms    |
| Monotonicity      | Voltage dip allowed in ramp   | -   | 300  | mV    |
| Slope             | Ramp rate at any given time between 10% and 90%<br>Min: $0.8 \cdot V(\text{min}) / \text{Rise time}(\text{max})$<br>Max: $0.8 \cdot V(\text{max}) / \text{Rise time}(\text{min})$ | -   | 1500 | mV/ms |
| Operational Range | Voltage range for normal operating conditions   | 3.0 | 3.6  | V     |



Table 21. 3.3V External Power Supply Parameters

| Title                   | Description   | Min | Max | Units |
|-------------------------|---|-----|-----|-------|
| Ripple                  | Maximum voltage ripple (peak to peak) <sup>a</sup>  | -   | 100 | mV    |
| Overshoot               | Maximum overshoot allowed   | -   | 660 | mV    |
| Overshoot Settling Time | Maximum overshoot allowed duration.<br>(At that time delta voltage should be lower than 5 mV from steady state voltage) | -   | 3   | ms    |

a. The peak to peak output ripple is measured at 20 MHz Bandwidth within the operational range.

#### 4.4.4 Internal LVR Power Sequencing

All supplies should rise monotonically. Sequencing of the supplies is controlled by the 82563EB/82564EB.

##### 4.4.4.1 Power up Sequencing and Tracking

During power up, the sequencing and tracking of the internally controlled supplies (1.9V and 1.2V) is controlled by the 82563EB/82564EB. No specific motherboard requirements are necessary to prevent electrical overstress or latch-up.

- The 82563EB/82564EB analog voltage (1.9V) will never exceed the 3.3V supply at any time during the power up. This is because the 1.9V supply is generated from the 3.3V supply when using the internal voltage regulator control logic (see Figure 5 and Figure 6 for a schematic of the internal LVR circuit). The 1.9V supply will track the 3.3V ramp.
- The 82563EB/82564EB core voltage (1.2V) will never exceed the 3.3V at any time during the power up. This is because the 1.2V supply is generated from the 3.3V supply when using the internal voltage regulator control logic (see Figure 5 and Figure 6 for a schematic of the internal LVR circuit). The 1.2V ramp is delayed internally to prevent it from exceeding the 1.9V and 3.3V supply at any time. The delay is proportional to the slope of the 3.3V ramp.

The delay is approximated by  $T_{\text{ramp}}(3.3\text{V}) * 0.25 < T_{\text{delay}}(1.2\text{V}) < T_{\text{ramp}}(3.3\text{V}) * 0.75$ .  $T_{\text{ramp}}$  is defined to the ramp rate of the 3.3V input to the internal voltage regulator circuit.

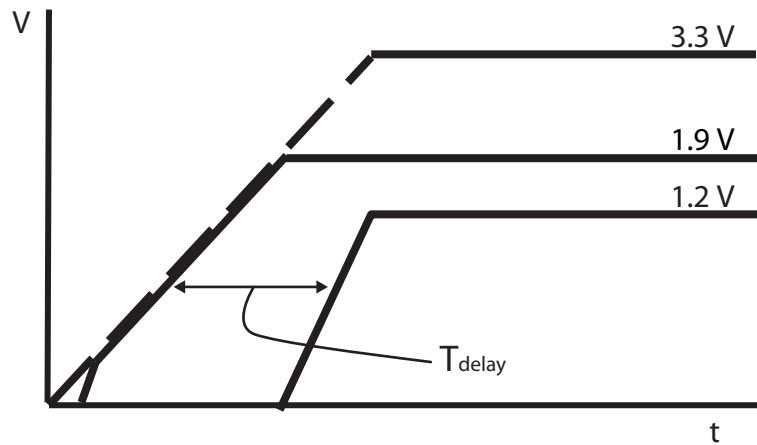


Figure 4. 82563EB/82564EB power up sequencing with internal regulators

#### 4.4.4.2 Internal LVR Power down Sequencing

There are no specific power down sequencing and tracking requirements for the 82563EB/82564EB device. The risk of latch-up or electrical overstress is small because only the only charge storing in decoupling capacitors is left in the system.

#### 4.4.4.3 82563EB/82564EB BOM for Internal Voltage Regulators

Table 22. 82563EB/82564EB BOM (Bill of Material) of Components for Internal Regulator

| Description                 | Quantity | Recommended Component |             |         |
|-----------------------------|----------|-----------------------|-------------|---------|
|                             |          | Manufacturer          | Part Number | Package |
| PNP Transistor For 1.2V LVR | 1        | Philips               | BCP-69-16   | SOT-223 |
| PNP Transistor For 1.9V LVR | 1        | Philips               | BCP-69-16   | SOT-223 |



#### 4.4.4.4 1.9V Internal LVR Specification

**Table 23. 1.9V Internal LVR Specification**

| Parameter                               | Value   |         | Units      | Comments            |
|---|---------|---------|------------|---------------------|
|   | Minimum | Maximum |            |                     |
| Input Voltage                           | 3.0     | 3.6     | V          | -                   |
| Input Capacitance                       | 4.7     | -       | $\mu$ F    | -                   |
| Input Capacitance ESR                   | -       | 100     | M $\Omega$ | -                   |
| Load Current                            | 1       | -       | A          | $V_{OUT} = 1.900$ V |
| Output Voltage Tolerance                | -5      | +10     | %          | -                   |
| Output Capacitance                      | 4.7     | -       | $\mu$ F    | -                   |
| Output Capacitance ESR <sup>a</sup>     | -       | 100     | M $\Omega$ | -                   |
| Current Consumption during power up     | -       | 0.5     | mA         | -                   |
| Current Consumption during power down   | -       | 0.5     | mA         | -                   |
| Peak to Peak output Ripple <sup>b</sup> | -       | 100     | mV         | -                   |
| PSRR                                    | -       | 20      | dB         | -                   |
| Turn-On Time                            | 0.1     | 1       | ms         | -                   |
| External PNP hFE                        | 100     | N/A     | -          | -                   |

a. The use of Tantalum capacitors is not recommended.

b. The peak to peak output rippled is measured at 20 MHz Bandwidth within the operational range.

#### 4.4.4.5 1.2V Internal LVR Specification

**Table 24. 1.2V Internal LVR Specification (Sheet 1 of 2)**

| Parameter             | Value   |         | Units      | Comments           |
|-----------------------|---------|---------|------------|--------------------|
|                       | Minimum | Maximum |            |                    |
| Input Voltage         | 3.0     | 3.6     | V          | -                  |
| Input Capacitance     | 4.7     | -       | $\mu$ F    | -                  |
| Input Capacitance ESR | -       | 100     | M $\Omega$ | -                  |
| Load Current          | 1       | -       | A          | $V_{OUT} = 1.20$ V |



Table 24. 1.2V Internal LVR Specification (Sheet 2 of 2)

| Parameter                               | Value   |         | Units      | Comments |
|---|---------|---------|------------|----------|
|   | Minimum | Maximum |            |          |
| Output Voltage Tolerance                | -10     | +10     | %          | -        |
| Output Capacitance                      | 4.7     | -       | $\mu$ F    | -        |
| Output Capacitance ESR <sup>a</sup>     | -       | 100     | M $\Omega$ | -        |
| Current Consumption during power up     | -       | 0.5     | mA         | -        |
| Current Consumption during power down   | -       | 0.5     | mA         | -        |
| Peak to Peak output Ripple <sup>b</sup> | -       | 100     | mV         | -        |
| PSRR                                    | -       | 20      | dB         | -        |
| Turn-On Time                            | 0.1     | 1       | ms         | -        |
| External PNP hFE                        | 100     | -       | -          | -        |

- a. The use of Tantalum capacitors is not recommended.
- b. The peak to peak output ripple is measured at 20 MHz Bandwidth within the operational range.

#### 4.4.4.6 PNP Transistor Specification for Internal LVR

Table 25. PNP Specification

| Title             | Description                          | Min | Max  | Units        |
|-------------------|--------------------------------------|-----|------|--------------|
| $V_{ce,sat}$      | Collector-emitter saturation voltage | -   | 0.5  | V            |
| $I_c(max)$        | Collector current, maximum sustained | -   | 1000 | mA           |
| $I_b$             | Base current, maximum sustained      | -   | 10   | mA           |
| $V_{be}$          | Base-emitter on voltage              | -   | 1    | V            |
| $T_{jmax}$        | Maximum junction temperature         | -   | 150  | $^{\circ}$ C |
| Power Dissipation | Maximum total power dissipation      | -   | 1.35 | W            |
| hFE               | DC Current gain                      | 100 | -    | -            |
| fT                | Current Gain Product Bandwidth       | 10  | -    | MHz          |

#### 4.4.4.7 Internal LVR Board Schematic

When using the internal voltage regulator controllers built into the 82563EB/82564EB, series resistors may need to be placed in series with the collector in order to prevent the PNP transistors from overheating. These series resistors dissipate a portion of the power that would otherwise be dissipated by the PNP devices. The value and power rating of the resistors must be carefully chosen to balance thermal limits against the PNP characteristics against total current draw. The regulator must never drop below the minimum  $V_{ce}$  and out of the linear region.



The effective resistance of the pass resistors should be approximately 0.5 Ω and have a combined power dissipation rating of 0.5 Watts for the 82563EB. Figure 5 shows the recommended implementation.

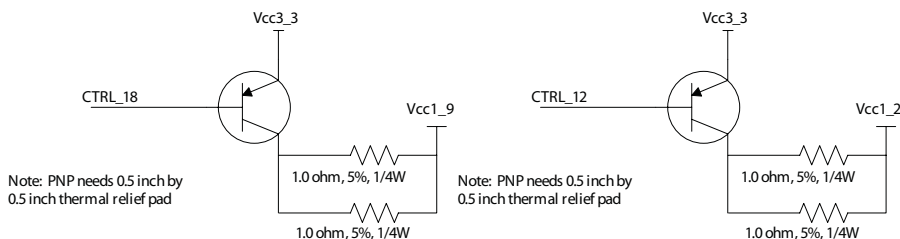


Figure 5. 82563EB 1.9V and 1.2V internal LVR schematic

**Note:** No resistors are required for the 82564EB as shown in Figure 6 due to the reduction in current demand. See Figure 4.9 for more details regarding power consumption.

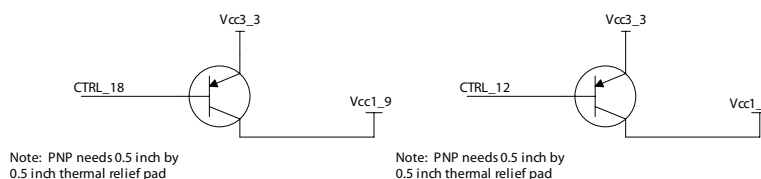


Figure 6. 82564EB 1.9V and 1.2V internal LVR schematic

## 4.5 Link (MDI) Interface

The Media Dependent Interface pins (MDIA\_PLUS[3:0], MDIA\_MINUS[3:0], MDIB\_PLUS[3:0], MDIB\_MINUS[3:0]) are analog pins conforming to the IEEE 802.3ab (802.3 Clause 40) requirements.

Table 26. Link (MDI) Interface Electrical Specification

| Symbol             | Parameter                                 | Pins      | Condition               | Min              | Typ  | Max   | Unit                            |
|--------------------|---|-----------|-------------------------|------------------|------|-------|---------------------------------|
| V <sub>ODIFF</sub> | Absolute peak differential output voltage | MDI*[1:0] | 10Base-T no cable       | 2.2              | 2.5  | 2.8   | V                               |
|                    |   | MDI*[1:0] | 10Base-T cable          | 585 <sup>b</sup> | -    | -     | mV                              |
|                    |   | MDI*[1:0] | 100Base-TX mode         | 0.950            | 1    | 1.050 | V                               |
|                    |   | MDI*[3:0] | 1000Base-T <sup>a</sup> | 0.67             | 0.75 | 0.82  | V                               |
|                    | Overshoot                                 | MDI[1:0]  | 100Base-TX mode         | 0                | -    | 5%    | (V)                             |
|                    | Amplitude Symmetry (positive / negative)  | MDI[1:0]  | 100Base-TX mode         | 0.98x            | -    | 1.02x | V <sup>+</sup> / V <sup>-</sup> |





**Table 26. Link (MDI) Interface Electrical Specification**

| Symbol      | Parameter                       | Pins     | Condition  | Min              | Typ              | Max  | Unit           |
|-------------|---------------------------------|----------|------------|------------------|------------------|------|----------------|
| $V_{IDIFF}$ | Peak differential input voltage | MDI[1:0] | 10Base-T   | 585 <sup>c</sup> | -                | -    | mV             |
|             | Signal Detect Assertion         | MDI[1:0] | 100Base-TX |                  | 460 <sup>d</sup> | 1000 | mV peak - peak |
|             | Signal Detect De-assertion      | MDI[1:0] | -          | 200              | 360 <sup>e</sup> |      | mV peak - peak |

- a. IEEE 802.3ab Figure 40-19 points A&B.
- b. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the "far end" wave form. This template allows as little as 495mV peak differential voltage at the far end receiver.
- c. See IEEE 802.3, Clause 14, Figure 14.17 for the template for the receive wave form.
- d. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect. The 82563EB/82564EB will accept signals typically with 460 mV peak-to-peak differential amplitude.
- e. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should de-assert signal detect. The 82563EB/82564EB will reject signals typically with 360 mV peak-to-peak differential amplitude

## 4.6 Kumeran (Serial) Interface

The Kumeran interface is electrically compatible with the SERDES implemented in 1000Base-BX applications, as defined in the PICMG 3.1 Specification, Version 1.0, Chapter 5, Backplane Physical Layers Interfaces. It also implements electrical idle as described in section 3.5.4. As part of the electrical idle implementation, the Kumeran interface also needs to be able to detect when the 631xESB/632xESB is in electrical idle.

### 4.6.1 Transmit

The transmit specifications are measured with the following test load.

**Table 27. Kumeran (Serial) Transmit Specifications**

| Symbol        | Parameter                                       | Min      | Typ  | Max      | Unit | Notes                       |
|---------------|---|----------|------|----------|------|-----------------------------|
|               | Data Rate (original data)                       | 999.9    | 1000 | 1000.1   | Mb/s | 1000 mb/s ± 100 ppm         |
|               | Signaling Speed (raw data rate of encoded data) | 1249.875 | 1250 | 1250.125 | V    | 1250 mb/s ± 100 ppm         |
|               | Clock Tolerance                                 | -100     | -    | +100     | ppm  |                             |
| $V_{DIFFp-p}$ | Differential Output Amplitude (peak to peak)    | 750      | -    | 1350     | mV   |                             |
| $V_{DIFFp}$   | Differential Output Amplitude (peak)            | 375      | -    | 675      | mV   | Equivalent to $V_{DIFFp-p}$ |
|               | Return Loss                                     | 10       | -    | -        | dB   |                             |
|               | Impedance at Connection                         | 70       | 100  | 130      | Ω    |                             |



The differential peak and differential peak to peak voltage is defined as follows:

- $V_{DIFFp} = \max(|V_+ - V_-|)$
- $V_{DIFFp-p} = (2 * V_{DIFFp})$

In addition, the transmitter must meet the following eye diagram.

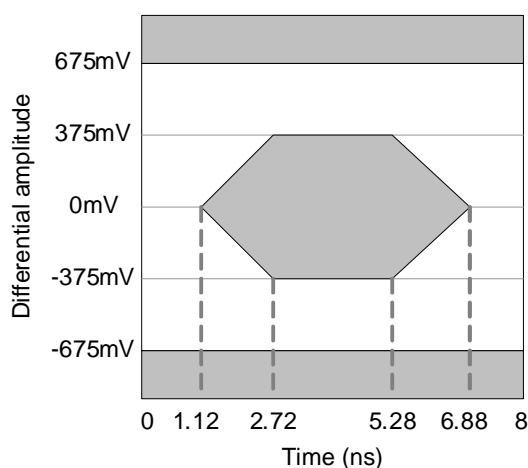


Figure 7. Kumeran (Serial) Transmit Eye Diagram

#### 4.6.2 Receive

The receiver operates with less than  $10^{-12}$  Bit Error Rate (BER) when the received signal meets valid voltage and timing specifications and is delivered from a balanced  $100 \Omega$  source.

Table 28. Kumeran (Serial) Receive Specifications

| Symbol        | Parameter                                       | Min      | Typ  | Max      | Unit     | Notes                       |
|---------------|---|----------|------|----------|----------|-----------------------------|
|               | Data Rate (original data)                       | 999.9    | 1000 | 1000.1   | Mb/s     | 1000 mb/s $\pm$ 100 ppm     |
|               | Signaling Speed (raw data rate of encoded data) | 1249.875 | 1250 | 1250.125 | V        | 1250 mb/s $\pm$ 100 ppm     |
|               | Clock Tolerance                                 | -100     | -    | +100     | ppm      |                             |
| $V_{SENSp-p}$ | Sensitivity (differential peak to peak)         | 200      | -    | 1350     | mV       |                             |
| $V_{SENSp}$   | Sensitivity (differential peak)                 | 100      | -    | 675      | mV       | Equivalent to $V_{SENSp-p}$ |
|               | Differential Skew                               | -        | -    | 175      | ps       |                             |
|               | Differential Return Loss                        | 10       | -    | -        | $\Omega$ |                             |

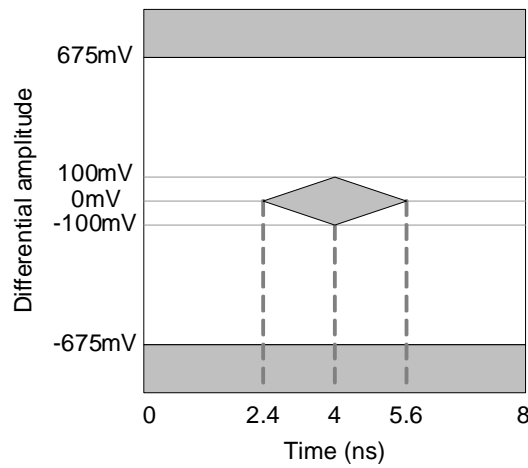


**Table 28. Kumeran (Serial) Receive Specifications**

| Symbol | Parameter               | Min | Typ | Max | Unit     | Notes |
|--------|-------------------------|-----|-----|-----|----------|-------|
|        | Common Mode Return Loss | 6   | -   | -   | dB       |       |
|        | TDR Rise                | -   | 85  | -   | $\Omega$ |       |
|        | Impedance at Connection | 70  | 100 | 130 |          |       |

**Note:** TDR measurements are recorded times. Record time = TDR transmit time \*2.

The receiver expects to receive a signal meeting the following eye diagram.



**Figure 8. Kumeran (Serial) Receive Eye Diagram**

### 4.6.3 Electrical Idle

The Kumeran interface also implements electrical idle. As a result, it needs to:

- Detect when the 631xESB/632xESB has gone into electrical idle
- Go into electrical idle



### 4.6.3.1 Electrical Idle Detection

The 82563EB/82564EB detects that the 631xESB/632xESB has gone into electrical idle when it senses that the differential voltage has gone below and is remaining below a threshold voltage.

**Table 29. Kumeran (Serial) Electrical Idle Detection**

| Symbol                       | Parameter   | Min  | Typ | Max | Unit |
|------------------------------|---|------|-----|-----|------|
| $V_{RX\_IDLE\_DET\_DIFFp-p}$ | Voltage range to detect electrical idle (differential peak to peak) | 65   | -   | 200 | mV   |
| $V_{RX\_IDLE\_DET\_DIFFp}$   | Voltage range to detect electrical idle (differential peak to peak) | 37.5 | -   | 100 | mV   |

**Note:** When the differential peak to voltage is below 65 mV (37.5 mV differential peak), the 82563EB/82564EB detects that the 631xESB/632xESB has gone into electrical idle. This voltage corresponds to the minimum output voltage in Electrical Idle plus some noise margin.

When the differential peak to peak voltage is above 200 mV (100 mV differential peak), the 82563EB/82564EB detects that the 631xESB/632xESB is not in electrical idle. This voltage corresponds to the minimum valid receive level.

### 4.6.3.2 Electrical Idle Output

The following parameters relate to electrical idle output and the transition into and out of electrical idle.

**Table 30. Kumeran (Serial) Electrical Idle Output**

| Symbol                        | Parameter   | Min | Typ | Max | Unit    |
|-------------------------------|---|-----|-----|-----|---------|
| $V_{TX\_IDLE\_DIFFp}$         | Electrical Idle peak output voltage.  | 0   | -   | 20  | mV      |
| $V_{TX\_IDLE\_MON}$           | Minimum time spent in electrical idle.  | 400 | -   | 100 | mV      |
| $V_{TX\_IDLE\_SET\_TO\_IDLE}$ | Maximum time for to transition to a valid electrical idle after electrical idle detected. |     |     | 1   | ms      |
| $T_{TX\_IDLE\_TO-DIFF-DATA}$  | Maximum time to transition to valid transmit after leaving electrical idle.               |     |     | 340 | $\mu$ s |



## 4.7 Crystal

The quartz crystal is strongly recommended as a low cost and high performance choice with the 82563EB/82564EB device. Quartz crystals are the mainstay of frequency control components and are available from numerous vendors in many package types with various specification options

Table 31. Crystal Parameters

| Parameter                    | Suggested Value   | Conditions       |
|------------------------------|---|------------------|
| Vibrational Mode             | Fundamental   |                  |
| Nominal Frequency            | 25.000 MHz  | at 25° C         |
| Frequency Tolerance          | <ul style="list-style-type: none"><li>±30 ppm recommended</li><li>±50 ppm across the entire operating temperature range (required by IEEE specifications)</li></ul> | at 25° C         |
| Temperature Tolerance        | ±30 ppm   | at 0° C to 70° C |
| Calibration Mode             | Parallel  |                  |
| Load Capacitance             | 27 pF   |                  |
| Shunt Capacitance            | 6 pF maximum  |                  |
| Equivalent Series Resistance | 50 Ω maximum  | at 25 MHz        |
| Drive Level                  | 750 μW  |                  |
| Aging                        | ±5 ppm per year maximum   |                  |

### 4.7.1 External Clock Oscillator

If using an external oscillator to provide a clock to the 82563EB/82564EB, the connection shown in Figure 9 must be used. Note that the XTAL2 output of the 82563EB/82564EB must not be connected. The XTAL1 input receives the output of the oscillator directly; AC coupling is not recommended.

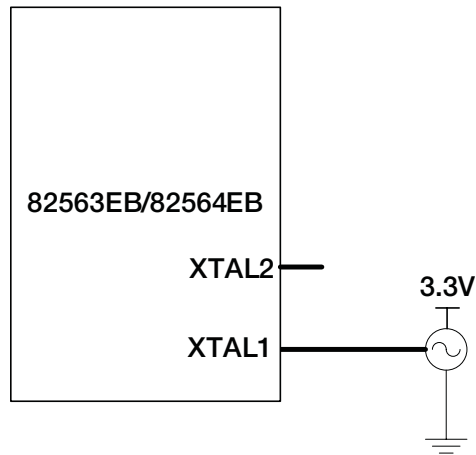


Figure 9. External Clock Oscillator Connectivity to 82563EB/82564EB



Table 32. Specification for External Clock Oscillator

| Parameter Name        | Symbol         | Value                | Conditions     |
|-----------------------|----------------|----------------------|----------------|
| Frequency             | $f_o$          | 25.0 [MHz]           | @25 [°C]       |
| Swing                 | $V_{p-p}$      | $3.3 \pm 0.3$ [V]    | -              |
| Frequency Tolerance   | $\Delta f/f_o$ | $\pm 30$ [ppm]       | -0 to +70 [°C] |
| Operating Temperature | $T_{opr}$      | -0 to +70 [°C]       | -              |
| Aging                 | $\Delta f/f_o$ | $\pm 5$ ppm per year | -              |

## 4.8 Reset and Initial Clock Timing

PHY\_PWR\_GOOD must be low throughout the time that the power supplies are ramping. This guarantees that the 82563EB/82564EB resets cleanly.

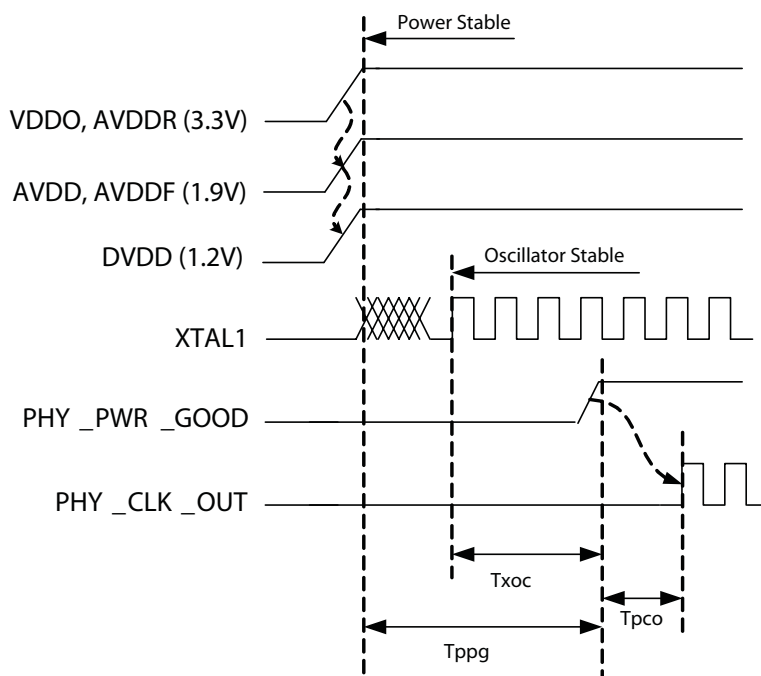


Figure 10. 82563EB/82564EB Reset Timing



**Table 33. Reset Specification**

| Title              | Description   | Min | Max | Units |
|--------------------|---|-----|-----|-------|
| PHY_PWR_GOOD pulse | Minimum pulse width for LAN_PWR_GOOD  | 100 | -   | μs    |
| T <sub>ppg</sub>   | Minimum time PHY_PWR_GOOD must be low after power supply is in operating range            | 100 | -   | μs    |
| T <sub>xoc</sub>   | Time from oscillator stable to PHY_PWR_GOOD assertion, when using an external oscillator. | 100 | -   | μs    |
| T <sub>pco</sub>   | Time from PHY_PWR_GOOD assertion until the 82563EB/82564EB outputs the PHY_CLK_OUT.       | -   | 350 | μs    |

There are no required timing relationships between PHY\_RESET\_N, PHY\_SLEEP, and either PHY\_PWR\_GOOD, the power supply being stable, or the oscillator being stable. The 82563EB/82564EB will come out of reset when both PHY\_PWR\_GOOD is asserted (1b) and PHY\_RESET\_N is deasserted (1b). It will be active when PHY\_PWR\_GOOD is asserted (1b), PHY\_RESET\_N is deasserted (1b), and PHY\_SLEEP is deasserted (0b).

## 4.9 Power Consumption

The 82563EB/82564EB’s power consumption (Tables 34 through 37) is the sum of each port’s power consumption. A port’s power consumption depends on whether the port’s logic, PHY, and Kumeran are operational, and the 82563EB/82564EB’s operating speeds. These in turn, depend on the following factors:

|                                |  |
|--------------------------------|--|
| <b>PHY_PWR_GOOD input</b>      | Powers off the entire chip (including PHY_CLK_OUT) when 0b. It has priority over PHY_RESET_N or PHY_SLEEP.   |
| <b>PHY_RESET_N input</b>       | When 0b, the entire chip is held in reset except PHY_CLK_OUT.  |
| <b>PHY_SLEEP input</b>         | When 1b the entire chip is powered down, except PHY_CLK_OUT.   |
| <b>Port Disable Register</b>   | The port’s PHY and Kumeran can be disabled by writing a 1b to the “Disable Port” bit of the “Power Management Control” register.   |
| <b>PHY Power Down</b>          | The 82563EB/82564EB can be powered down with an indication over the Kumeran bus or by writing a 1b to the “Control Register’s” “Power Down” bit.   |
| <b>Link Down</b>               | When the link is required but the link is down the 82563EB/82564EB remains in energy detect mode, attempting to detect energy from the link partner.   |
| <b>Speed</b>                   | The 82563EB/82564EB uses progressively more power as the speed increases from 10 Mb/s to 100 Mb/s to 1000 Mb/s. Speed is normally based on auto-negotiation with the link partner, but may be forced or influenced by the power state. |
| <b>Power State</b>             | The power state can be used in conjunction with the “Low Power Link Up” and “Auto-Negotiation 1000 Disable” to control the 82563EB/82564EB’s speed.  |
| <b>Kumeran Electrical Idle</b> | Nothing is transmitted on the differential pairs.  |



Table 34. Power Supply Characteristics - D0a (Both Ports)

|                    | D0a (Both Ports)  |              |                   |              |                    |              |                     |              |
|--------------------|-------------------|--------------|-------------------|--------------|--------------------|--------------|---------------------|--------------|
|                    | Unplugged/No Link |              | 10 Mb/s Operation |              | 100 Mb/s Operation |              | 1000 Mb/s Operation |              |
|                    | Typ Icc (mA)      | Max Icc (mA) | Typ Icc (mA)      | Max Icc (mA) | Typ Icc (mA)       | Max Icc (mA) | Typ Icc (mA)        | Max Icc (mA) |
| 3.3 V              | 12                | 47           | 20                | 22           | 22                 | 23           | 35                  | 36           |
| 1.9 V              | 11                | 11           | 33                | 33           | 79                 | 79           | 411                 | 411          |
| 1.2 V              | 20                | 26           | 140               | 140          | 165                | 165          | 345                 | 345          |
| Total Device Power | 145 mW            |              | 635 mW            |              | 878 mW             |              | 2610 mW             |              |

Table 35. Power Supply Characteristics - D3cold - Wake Up Enabled (Both Ports)

|                    | D3cold - Wake Up Enabled (Both Ports) |              |                   |              |                    |              | D3cold - Wake Up Disabled (Both Ports) |              |
|--------------------|---------------------------------------|--------------|-------------------|--------------|--------------------|--------------|--|--------------|
|                    | Unplugged/No Link                     |              | 10 Mb/s Operation |              | 100 Mb/s Operation |              | Typ Icc (mA)                           | Max Icc (mA) |
|                    | Typ Icc (mA)                          | Max Icc (mA) | Typ Icc (mA)      | Max Icc (mA) | Typ Icc (mA)       | Max Icc (mA) |  |              |
| 3.3 V              | 12                                    | 47           | 21                | 22           | 22                 | 23           | 12                                     | 12           |
| 1.9 V              | 11                                    | 11           | 33                | 33           | 79                 | 79           | 11                                     | 11           |
| 1.2 V              | 20                                    | 26           | 140               | 140          | 166                | 166          | 12                                     | 12           |
| Total Device Power | 145 mW                                |              | 640 mW            |              | 879 mW             |              | 115 mW                                 |              |

Table 36. Power Supply Characteristics - Uninitialized/Disabled

|                    | Uninitialized/Disabled                 |              |   |              |
|--------------------|--|--------------|---|--------------|
|                    | D(n) Uninitialized (PHY PWR GOOD = 0b) |              | Disabled <sup>a</sup> (via Flash Address) |              |
|                    | Typ Icc (mA)                           | Max Icc (mA) | Typ Icc (mA)                              | Max Icc (mA) |
| 3.3 V              | 10                                     | 13           | 11  | 13           |
| 1.9 V              | 18                                     | 20           | 19  | 19           |
| 1.2 V              | 2                                      | 2            | 7   | 12           |
| Total Device Power | 116 mW                                 |              | 120 mW                                    |              |

a. Equivalent to PHY\_SLEEP = 1b and/or PHY\_RESET\_N = 0b.





Table 37. Power Supply Characteristics - Complete Subsystem

|                               | Complete Subsystem<br>(Including Magnetics, LED, and Regulator Circuits) |         |                    |         |                     |         |
|-------------------------------|--|---------|--------------------|---------|---------------------|---------|
|                               | 10 Mb/s Operation  |         | 100 Mb/s Operation |         | 1000 Mb/s Operation |         |
|                               | Typ Icc  | Max Icc | Typ Icc            | Max Icc | Typ Icc             | Max Icc |
| 3.3 V                         | 27   | 28      | 35                 | 37      | 60                  | 63      |
| 1.9 V                         | 33   | 33      | 78                 | 79      | 413                 | 413     |
| 1.2 V                         | 280  | 280     | 220                | 220     | 704                 | 704     |
| Subsystem<br>3.3 V<br>Current | 1121 mW  |         | 1107 mW            |         | 3883 mW             | 4248 mW |



*Note:* This page intentionally left blank.



## 5.0 Package and Pinout Information

This section describes the 82563EB/82564EB device physical characteristics. The pin number-to-signal mapping is indicated beginning with Section 5.3.

### 5.1 Package Information

The package used for the 82563EB/82564EB is a 100-pin, 14 mm x 14 mm TQFL with an Exposed-Pad\*. An Exposed-Pad\* is a central pad on the bottom of the package that serves as a ground and thermal connection.

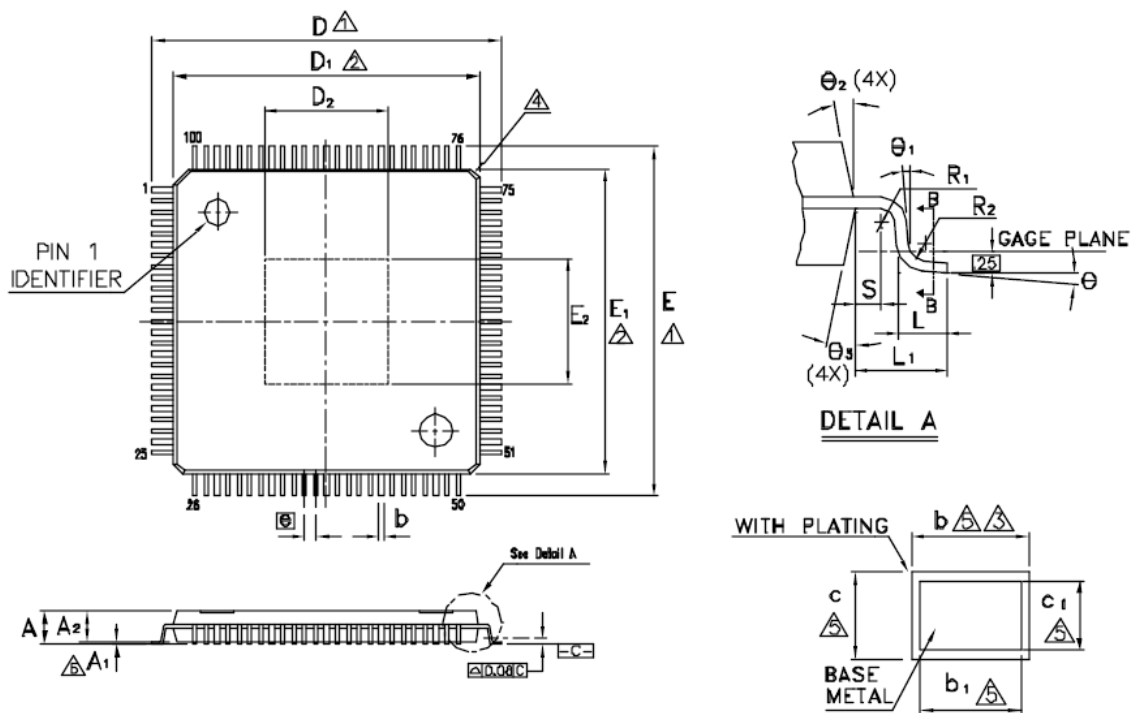


Figure 11. Mechanical Information



| Symbol         | Dimension in mm |      |      | Dimension in inch |       |       |
|----------------|-----------------|------|------|-------------------|-------|-------|
|                | Min             | Norm | Max  | Min               | Norm  | Max   |
| A              | —               | —    | 1.20 | —                 | —     | 0.047 |
| A <sub>1</sub> | 0.05            | —    | 0.15 | 0.002             | —     | 0.006 |
| A <sub>2</sub> | 0.95            | 1.00 | 1.05 | 0.037             | 0.039 | 0.041 |
| b              | 0.17            | 0.22 | 0.27 | 0.007             | 0.009 | 0.011 |
| b <sub>1</sub> | 0.17            | 0.20 | 0.23 | 0.007             | 0.008 | 0.009 |
| c              | 0.09            | —    | 0.20 | 0.004             | —     | 0.008 |
| c <sub>1</sub> | 0.09            | —    | 0.18 | 0.004             | —     | 0.630 |
| D              | 16.00 BSC       |      |      | 0.630 BSC         |       |       |
| D <sub>1</sub> | 14.00 BSC       |      |      | 0.551 BSC         |       |       |
| E              | 16.00 BSC       |      |      | 0.630 BSC         |       |       |
| E <sub>1</sub> | 14.00 BSC       |      |      | 0.551 BSC         |       |       |
| Ⓞ              | 0.50 BSC        |      |      | 0.020 BSC         |       |       |
| L              | 0.45            | 0.60 | 0.75 | 0.018             | 0.024 | 0.030 |
| L <sub>1</sub> | 1.00 REF        |      |      | 0.039 REF         |       |       |
| R <sub>1</sub> | 0.08            | —    | —    | 0.003             | —     | —     |
| R <sub>2</sub> | 0.08            | —    | 0.20 | 0.003             | —     | 0.008 |
| S              | 0.20            | —    | —    | 0.008             | —     | —     |
| θ              | 0°              | 3.5° | 7°   | 0°                | 3.5°  | 7°    |
| θ <sub>1</sub> | 0°              | —    | —    | 0°                | —     | —     |
| θ <sub>2</sub> | 11°             | 12°  | 13°  | 11°               | 12°   | 13°   |
| θ <sub>3</sub> | 11°             | 12°  | 13°  | 11°               | 12°   | 13°   |

| Die Pad Size Options |                |                 |                   |
|----------------------|----------------|-----------------|-------------------|
| Option               | Symbol         | Dimension in mm | Dimension in inch |
| Option #1            | D <sub>2</sub> | 5.72 BSC        | .225 BSC          |
|                      | E <sub>2</sub> | 5.72 BSC        | .225 BSC          |
| Option #2            | D <sub>2</sub> |                 |                   |
|                      | E <sub>2</sub> |                 |                   |

NOTE :

- ⚠ TO BE DETERMINED AT SEATING PLANE  $\square$  .
  - ⚠ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
  - ⚠ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
  - ⚠ EXACT SHAPE OF EACH CORNER IS OPTIONAL.
  - ⚠ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
  - ⚠ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.

Figure 12. Mechanical Specifications and Notes



## 5.2 Thermal Specifications

The 82563EB/82564EB device is specified for operation when the ambient temperature ( $T_A$ ) is within the range of 0° C to 60° C.

The maximum junction temperature is 120° C. The maximum ambient temperature with airflow and/or a heatsink can be calculated using the thermal coefficient data below and the power specification (see section 4.7)

$T_C$  (case temperature) is calculated using the equation:

$$T_C = T_A + P (\theta_{JA} - \theta_{JC})$$

$T_J$  (junction temperature) is calculated using the equation:

$$T_J = T_A + P \theta_{JA}$$

P (power consumption) is calculated by using the typical  $I_{CC}$ , as indicated in Table 38, and nominal  $V_{CC}$ . The preliminary thermal resistances are shown in Table 38.

**Table 38. Thermal Characteristics**

| Symbol        | Parameter                               | Value @ Given Airflow (m/s) |      |      |      | Units   |
|---------------|---|-----------------------------|------|------|------|---------|
|               |   | 0                           | 1    | 2    | 3    |         |
| $\theta_{JA}$ | Thermal Resistance, Junction to Ambient | 26.1                        | 22.9 | 21.7 | 21.1 | °C/watt |
| $\theta_{JC}$ | Thermal Resistance, Junction to Case    | 12.7                        | -    | -    | -    | °C/watt |



## 5.3 Pinout Information

Table 39. 82563EB/82564EB Pinout by Pin Number Order (Sheet 1 of 3)

| Pin | 82563EB<br>Dual Port | 82564EB<br>Single Port <sup>a</sup> | External<br>Strapping <sup>b</sup> |
|-----|----------------------|-------------------------------------|------------------------------------|
| 1   | JTAG_TDI             | -                                   | 1 - 10 K $\Omega$ , 5%, p/u        |
| 2   | DVDD                 | -                                   | -                                  |
| 3   | JTAG_TMS             | -                                   | 1 - 10 K $\Omega$ , 5%, p/u        |
| 4   | RESERVED_NC          | -                                   | -                                  |
| 5   | RESERVED_NC          | -                                   | -                                  |
| 6   | RESERVED_NC          | -                                   | -                                  |
| 7   | DVDD                 | -                                   | -                                  |
| 8   | RESERVED_NC          | -                                   | -                                  |
| 9   | RESERVED_NC          | -                                   | -                                  |
| 10  | RESERVED_NC          | -                                   | -                                  |
| 11  | VDDO                 | -                                   | -                                  |
| 12  | DVDD                 | -                                   | -                                  |
| 13  | RESERVED_NC          | -                                   | -                                  |
| 14  | RESERVED_NC          | -                                   | -                                  |
| 15  | RESERVED_NC          | -                                   | -                                  |
| 16  | DVDD                 | -                                   | -                                  |
| 17  | RESERVED_NC          | -                                   | -                                  |
| 18  | MDIO_ADD[2]          | -                                   | 1 - 10 K $\Omega$ , 5%, p/d        |
| 19  | MDIO_ADD[3]          | -                                   | 1 - 10 K $\Omega$ , 5%, p/d        |
| 20  | XTAL2                | -                                   | -                                  |
| 21  | XTAL1                | -                                   | -                                  |
| 22  | VDDO                 | -                                   | -                                  |
| 23  | CTRL_12              | -                                   | -                                  |
| 24  | AVDDR                | -                                   | -                                  |
| 25  | CTRL_18              | -                                   | -                                  |
| 26  | RESERVED_NC          | -                                   | -                                  |
| 27  | MDIA_PLUS[0]         | -                                   | -                                  |
| 28  | MDIA_MINUS[0]        | -                                   | -                                  |
| 29  | AVDD                 | -                                   | -                                  |
| 30  | AVDD                 | -                                   | -                                  |
| 31  | MDIA_PLUS[1]         | -                                   | -                                  |
| 32  | MDIA_MINUS[1]        | -                                   | -                                  |
| 33  | MDIA_PLUS[2]         | -                                   | -                                  |
| 34  | MDIA_MINUS[2]        | -                                   | -                                  |



Table 39. 82563EB/82564EB Pinout by Pin Number Order (Sheet 2 of 3)

| Pin | 82563EB Dual Port | 82564EB Single Port <sup>a</sup> | External Strapping <sup>b</sup> |
|-----|-------------------|----------------------------------|---------------------------------|
| 35  | AVDD              | -                                | -                               |
| 36  | MDIA_PLUS[3]      | -                                | -                               |
| 37  | MDIA_MINUS[3]     | -                                | -                               |
| 38  | MDIB_MINUS[3]     | RESERVED_NC                      | -                               |
| 39  | MDIB_PLUS[3]      | RESERVED_NC                      | -                               |
| 40  | AVDD              | -                                | -                               |
| 41  | MDIB_MINUS[2]     | RESERVED_NC                      | -                               |
| 42  | MDIB_PLUS[2]      | RESERVED_NC                      | -                               |
| 43  | MDIB_MINUS[1]     | RESERVED_NC                      | -                               |
| 44  | MDIB_PLUS[1]      | RESERVED_NC                      | -                               |
| 45  | AVDD              | -                                | -                               |
| 46  | AVDD              | -                                | -                               |
| 47  | MDIB_MINUS[0]     | RESERVED_NC                      | -                               |
| 48  | MDIB_PLUS[0]      | RESERVED_NC                      | -                               |
| 49  | RESERVED_NC       | -                                | -                               |
| 50  | PHY_REF           | -                                | 4.99 K $\Omega$ , 1%, p/d       |
| 51  | AVDDR             | -                                | -                               |
| 52  | RESERVED_NC       | -                                | -                               |
| 53  | RESERVED_NC       | -                                | -                               |
| 54  | LINK_B            | -                                | See Table 10                    |
| 55  | LEDB_RX_ACTIVITY  | RESERVED_NC                      | test point                      |
| 56  | LEDB_TX_ACTIVITY  | RESERVED_NC                      | -                               |
| 57  | LEDB_DUPLEX       | RESERVED_NC                      | -                               |
| 58  | LEDB_SPEED_1000_N | RESERVED_NC                      | -                               |
| 59  | DVDD              | -                                | -                               |
| 60  | VDDO              | -                                | -                               |
| 61  | LEDB_SPEED_100_N  | RESERVED_NC                      | -                               |
| 62  | LEDB_ACTIVITY_N   | RESERVED_NC                      | -                               |
| 63  | LEDB_LINK_UP_N    | RESERVED_NC                      | -                               |
| 64  | DVDD              | -                                | -                               |
| 65  | LINK_A            | -                                | See Table 10                    |
| 66  | LEDA_RX_ACTIVITY  | -                                | test point                      |
| 67  | LEDA_TX_ACTIVITY  | -                                | -                               |
| 68  | LEDA_DUPLEX       | -                                | -                               |
| 69  | DVDD              | -                                | -                               |
| 70  | LEDA_SPEED_1000_N | -                                | -                               |
| 71  | LEDA_SPEED_100_N  | -                                | -                               |



Table 39. 82563EB/82564EB Pinout by Pin Number Order (Sheet 3 of 3)

| Pin         | 82563EB<br>Dual Port | 82564EB<br>Single Port <sup>a</sup> | External<br>Strapping <sup>b</sup> |
|-------------|----------------------|-------------------------------------|------------------------------------|
| 72          | LEDA_ACTIVITY_N      | -                                   | -                                  |
| 73          | LEDA_LINK_UP_N       | -                                   | -                                  |
| 74          | DVDD                 | -                                   | -                                  |
| 75          | VDDO                 | -                                   | -                                  |
| 76          | MDIO                 | -                                   | -                                  |
| 77          | MDC                  | -                                   | 1 - 10 K $\Omega$ , 5% p/d         |
| 78          | MDIO_ADD[0]          | -                                   | 1- 10 K $\Omega$ , 5% p/d          |
| 79          | MDIO_ADD[1]          | -                                   | 1 - 10 K $\Omega$ , 5% p/d         |
| 80          | PHY_SLEEP            | -                                   | 1 - 10 K $\Omega$ , 5% p/d         |
| 81          | PHY_RESET_N          | -                                   | 1 - 10 K $\Omega$ , 5% p/u         |
| 82          | RESERVED_PD          | -                                   | 1 - 10 K $\Omega$ , 5% p/d         |
| 83          | PHY_PWR_GOOD         | -                                   | -                                  |
| 84          | RXB_MINUS            | RESERVED_NC                         | -                                  |
| 85          | RXB_PLUS             | RESERVED_NC                         | -                                  |
| 86          | AVDDF                | -                                   | -                                  |
| 87          | TXB_MINUS            | RESERVED_NC                         | -                                  |
| 88          | TXB_PLUS             | RESERVED_NC                         | -                                  |
| 89          | VSS                  | -                                   | -                                  |
| 90          | TXA_PLUS,            | -                                   | -                                  |
| 91          | TXA_MINUS            | -                                   | -                                  |
| 92          | AVDDF                | -                                   | -                                  |
| 93          | RXA_PLUS,            | -                                   | -                                  |
| 94          | RXA_MINUS            | -                                   | -                                  |
| 95          | TEST_JTAG            | -                                   | 1 - 10 K $\Omega$ , 5% p/u         |
| 96          | PHY_CLK_OUT          | -                                   | -                                  |
| 97          | VDDO                 | -                                   | -                                  |
| 98          | RESERVED_NC          | -                                   | -                                  |
| 99          | JTAG_TDO             | -                                   | -                                  |
| 100         | JTAG_TCK             | -                                   | 1 - 10 K $\Omega$ , 5%,p/d         |
| Central Pad | VSS                  | -                                   | -                                  |

- a. The 82564EB device uses the same name as the 82563EB device unless otherwise specified.  
b. For those external strappings that state 1 - 10 K $\Omega$ , 5%, the recommended value within that range is 3.3 K $\Omega$ , 5%.





## 5.4 Interface Diagrams

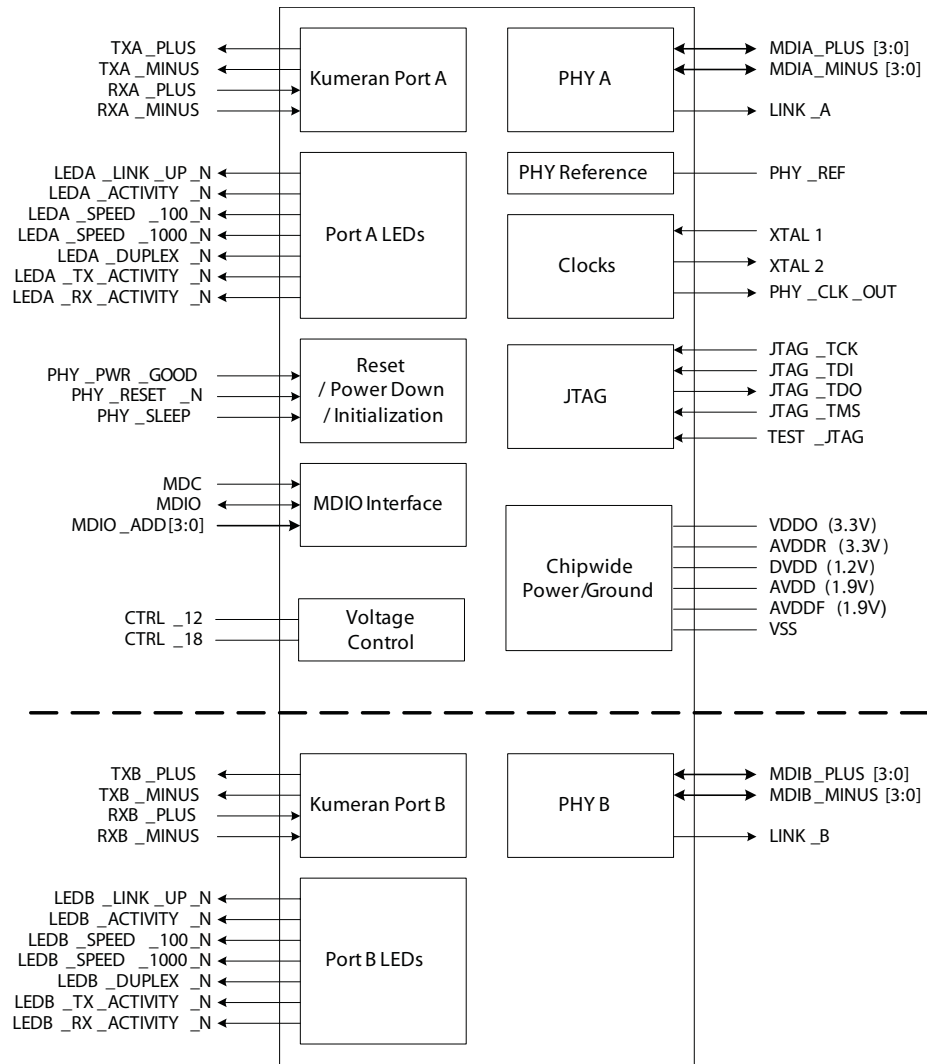


Figure 13. 82563EB/82564EB Interfaces



## 5.5 Visual Pin Assignments

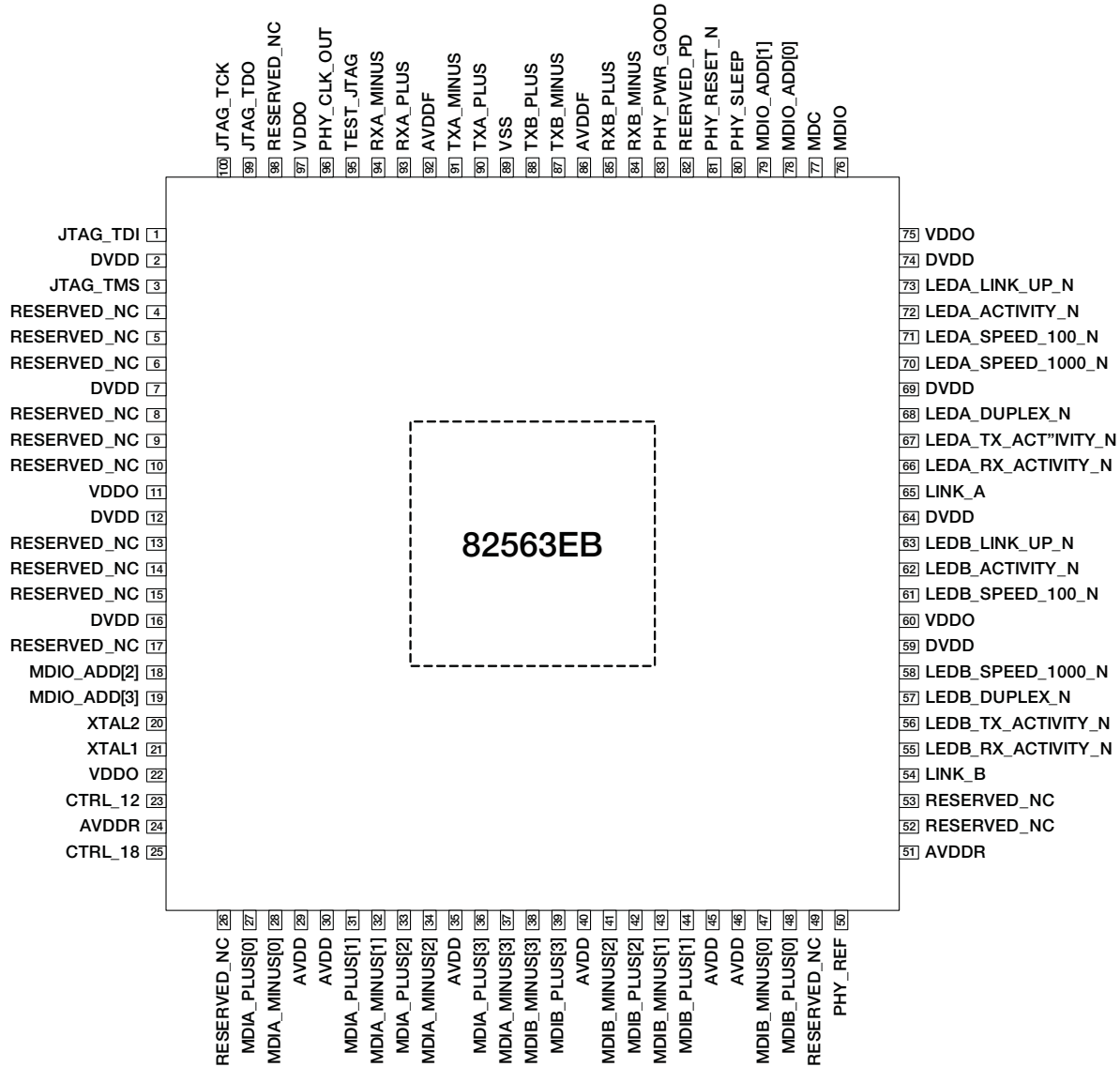


Figure 14. 82563EB Dual Port Gigabit Platform LAN connect Pinout (Top View)

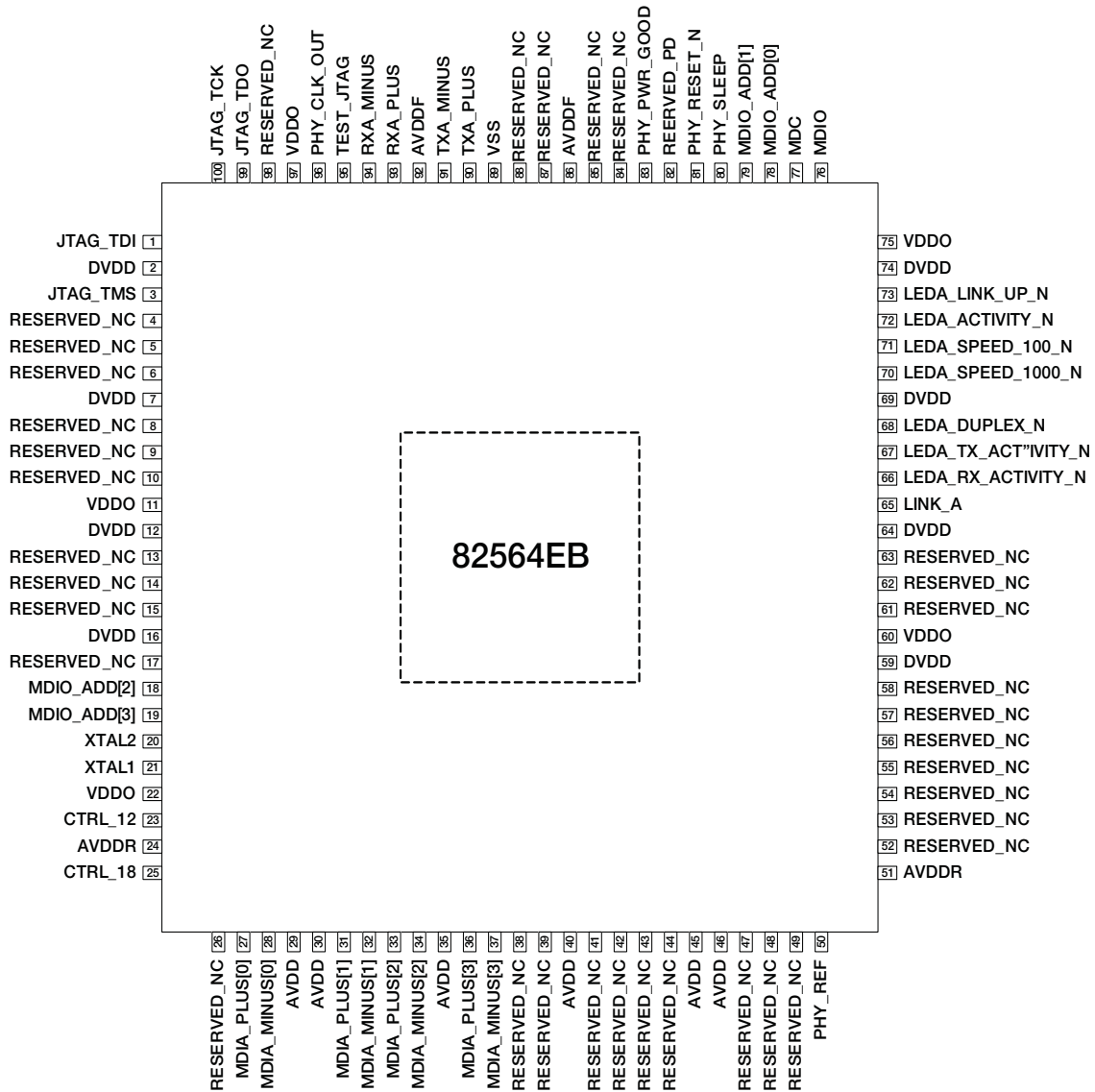


Figure 15. 82564EB Single Port Gigabit Platform LAN Connect Pinout (Top View)



*Note:* This page is intentionally left blank.