82544EI Gigabit Ethernet Controller

Networking Silicon

Datasheet

Product Features

- Full IEEE 802.3ab compliant
  - —Auto-Negotiation of speed, duplex, and flow control configuration
- 32/64-bit 33/66 MHz, PCI Rev 2.2 compliant host interface
- Host interface compliant to the PCI-X addendum, revision 1.0a, from 50 MHz to 133 MHz
- Offers both hardware and software based IEEE 802.3z Auto-Negotiation and Link Setup for Ten-Bit Interface (TBI) mode
- Internally implements IEEE 802.3 MII management interface for monitoring and control of the internal PHY
- Offers an external link interface: TBI as specified in IEEE 802.3z standard for 1000 Mb/s full duplex operation with 1.25 Gb/s SERDES
- Receive and transmit IP and TCP/UDP checksum offloading capabilities
- Automatic MDI crossover operation for 100BASE-TX and 10BASE-T modes
- IEEE 802.1q VLAN support
- Implements enhanced ACPI register set and power down functionality supporting D0 and D3 states, Wake on LAN capability with Power Management Event support
- Provides adaptive Inter Frame Spacing (IFS) capability, enabling collision reduction in half duplex networks
- Enables control of the transmission of Pause packets through software or hardware triggering
- Provides indications of receive FIFO status through programming interface
- Provides six activity and link indication outputs to directly drive LEDs
- Provides external parallel interface for up to 4 Mb of Flash or Boot EPROM for boot agent capability
- 4-wire 64 x 16 serial EEPROM interface for loading product configuration information
- Operating temperature: 0°C to 70° C (ambient)
- Targeted power dissipation is 2.5 W maximum
- Provides boundary scan through IEEE 1149.1 (JTAG) Test Access Port
- Leaded and lead-free[a] 416-pin Ball Grid Array (BGA). Devices that are lead-free are marked with a circled "e1" and have a product code: NHXXXXX

a.This device is lead-free. That is, lead has not been intentionally added, but lead may still exist as an impurity at <1000 ppm. The Material Declaration Data Sheet, which includes lead impurity levels and the concentration of other Restriction on Hazardous Substances (RoHS) -banned materials, is available at:

`ftp://download.intel.com/design/packtech/material_content_IC_Pack`

In addition, this device has been tested and conforms to the same parametric specifications as previous versions of the device. For more information regarding lead-free products from Intel Corporation, contact your Intel Field Sales representative.

Revision 1.0
April 2005

Revision History

Revision	Revision Date	Description
1.0	April 2005	Initial release (removed secret status)

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Tables

1.0 Overview

The 82544EI Gigabit Ethernet Controller is an integrated third-generation Ethernet LAN component capable of providing 1000, 100, and 10 Mbps data rates. It is a single-chip device, containing both the MAC and PHY layer functions, and optimized for LAN on Motherboard (LOM) designs, enterprise networking, and Internet appliances that use the Peripheral Component Interconnect (PCI) and PCI-X bus backplanes.

The 82544EI utilizes a 32/64 bit, 33/66 MHz direct interface to the PCI bus, compliant with the PCI Local Bus Specification, Revision 2.2. It also supports the emerging PCI-X extension to the PCI Local Bus, Revision 1.0a. The controller interfaces with the host processor through on-chip command and status registers and a shared host memory area, which is set up during initialization.

The 82544EI Gigabit Ethernet Controller provides a highly optimized architecture to deliver high performance and PCI/PCI-X bus efficiency. Its hardware, acceleration features enable offloading of various tasks, such as TCP/UDP/ IP checksum calculations and TCP segmentation, from the host processor. The 82544EI device accommodates highly-configurable Ethernet designs, which require minimal CPU overhead from interrupts and register accesses.

The physical layer circuitry provides an IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX and 10BASE-T applications. With the addition of an appropriate serializer/ deserializer (SERDES), the 82544EI controller also provides an Ethernet interface for 1000BASE-SX or 1000BASE-LX applications.

The 82544EI Gigabit Ethernet Controller is packaged in a 27 mm x 27 mm, 416-ball grid array.

1.1 Scope

This document contains datasheet specifications for the 82544EI Gigabit Ethernet Controller including signal descriptions, DC and AC parameters, packaging data, and pinout information.

1.2 Reference Documents

This document assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- 8254x Family of Gigabit Ethernet Controllers Software Developer's Manual, Intel Corporation.
- PCI Local Bus Specification, Revision 2.2, PCI Special Interest Group.
- PCI-X Specification, Revision 1.0a, PCI Special Interest Group.
- PCI Bus Power Management Interface Specification, Rev. 1.1, PCI Special Interest Group.
- IEEE Standard 802.3, 1996 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3u, 1995 Edition, Institute of Electrical and Electronics Engineers (IEEE).

- IEEE Standard 802.3x, 1997 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3z, 1998 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3ab, 1999 Edition, Institute of Electrical and Electronics Engineers (IEEE).

1.3 Product Codes

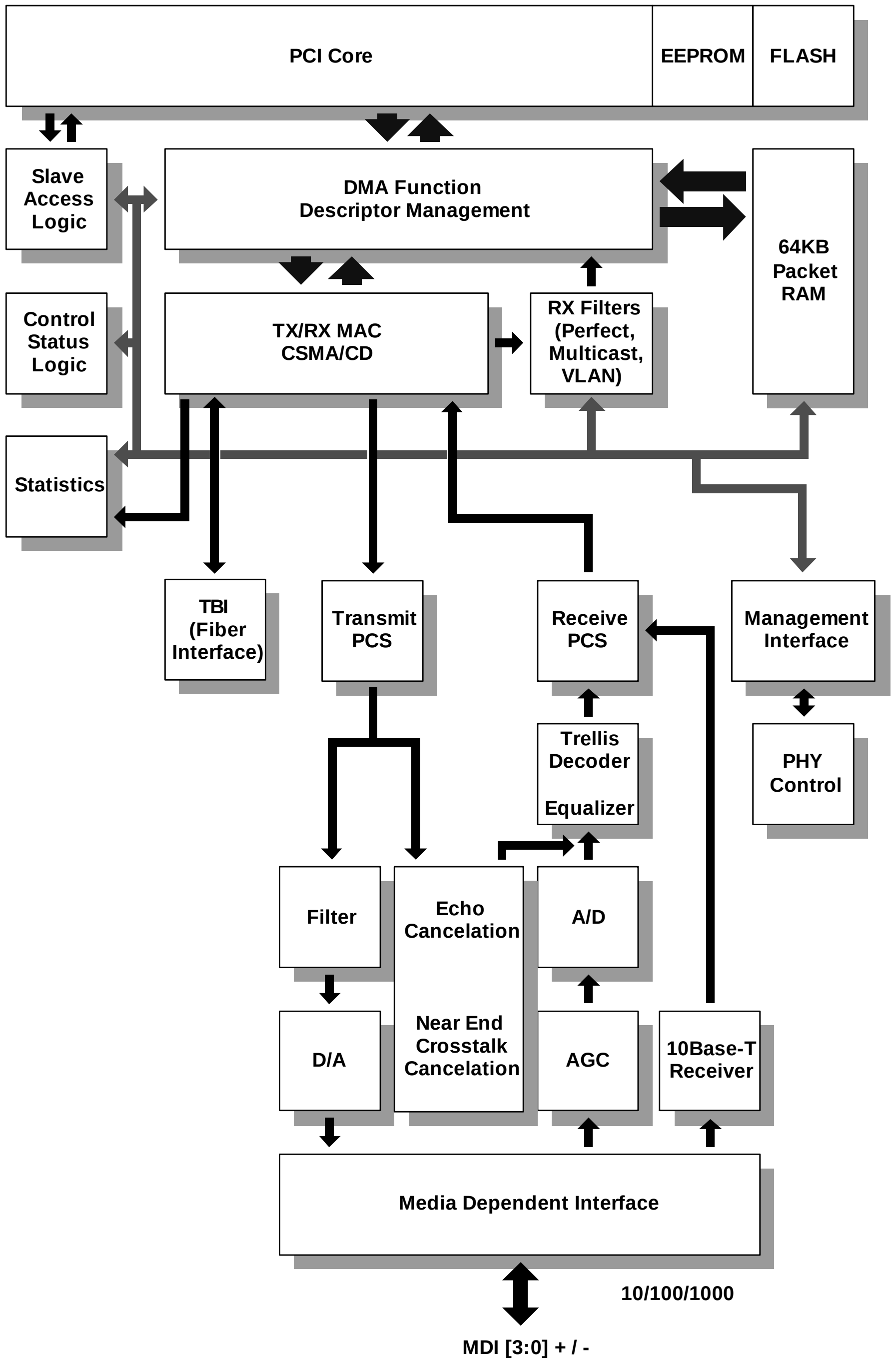
Table 1 lists the product ordering codes for the 82544EI.

Table 1. Product Ordering Codes

Device	Product Code
82544EI (Leaded)	FW82544EI
82544EI (Lead Free)	NH82544EI

1.4 Block Diagram

Figure 1. 82544EI Gigabit Ethernet Controller Block Diagram



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2.0 Additional Features of the 82544EI Gigabit Ethernet Controller

2.1 PCI/PCI-X Features

- Operates in either 5V or 3.3V PCI signaling environments
- 64-bit addressing for systems with more than 4 GB of physical memory
- Efficient PCI bus master operation, supported by optimized internal DMA controller
- Command usage optimization for advanced PCI commands such as MWI, MRM and MRL, and PCI-X commands such as MRD, MRB and MWB

2.2 PHY-Specific Features

- Complete full duplex and half duplex support
- Next page support
- Automatic polarity correction
- Digital implementation of adaptive equalizer and cancellers for echo and crosstalk

2.3 Host Offloading Features

- TCP segmentation (Large send)
- Packet filtering based on checksum errors
- Supports for various address filtering modes:
  - 16 exact matches (unicast or multicast)
  - 4096-bit hash filter for multicast frames
  - Promiscuous unicast and promiscuous multicast transfer modes
- IEEE 802.1q VLAN support
  - Ability to add and strip IEEE 802.1q VLAN tags
  - Packet filtering based on VLAN tagging, supporting 4096 tags
- SNMP and RMON statistic counters

2.4 Additional Performance Features

- Programmable host memory receive buffers (256 B to 16 KB)
- Programmable cache line size from 16 B to 128 B for efficient usage of PCI bandwidth

- Implements a total of 64 KB of configurable receive and transmit data FIFOs:
  - default allocation is 48 KB for Receive data FIFO and 16 KB for transmit data FIFO
- Descriptor ring management hardware for transmit and receive:
  - optimized descriptor fetching and write-back mechanisms for efficient system memory and PCI bandwidth usage
- Provides a mechanism for reducing the number of interrupts generated by receive and transmit operations
- Supports reception and transmission of packets with length up to 16 KB

2.5 Additional Device Features

- Provides seven general-purpose user mode pins
- Supports little-endian byte ordering for both 32- and 64-bit systems
- Supports big-endian byte ordering for 64-bit systems
- Provides loopback capabilities
- Provides boundary scan through IEEE 1149.1 (JTAG) Test Access Port

2.6 Technology Features

- Implemented in 0.18µ process
- Packaged in 416 PBGA package (27 mm x 27 mm)
- Implemented as low power CMOS device

3.0 Signal Descriptions

Special Note: The targeted signal names are subject to change without notice. Verify with your local Intel sales office that you have the latest data sheet before finalizing a design.

3.1 Signal Type Definitions

The signals of the 82544EI controller are electrically defined in the following fashion:

Name	Definition
I	A standard input-only digital signal.
O	A standard output-only digital signal.
TS	A bi-directional, three-state digital input/output signal.
STS	A sustained, digital, three-state signal that is driven by one owner at a time. An agent that drives an STS pin low must actively drive it high for at least one clock before letting it float. The next owner of the signal cannot start driving it any sooner than one clock after it is released by the previous owner.
OD	An open-drain digital signal. It is wired-OR'ed with other agents. The signaling agent asserts the signal, but the signal is returned to the inactive state by a weak pull-up resistor. The pull-up resistor may take two or three clock periods to fully restore the signal to the deasserted state.
A	PHY analog data signal.
P	A power connection, voltage reference, or other reference connection.

3.2 PCI/PCI-X Bus Interface

When RST# is asserted, the 82544EI Gigabit Ethernet Controller will not drive any PCI output or bi-directional pins except PME#.

3.2.1 PCI Address, Data and Control Signals

Signal Name	Type	Name and Function
AD[63:0]	TS	**Address and Data.** Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[63:0] contain a physical address (64 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. The 82544EI device uses little endian byte ordering. During data phases AD[7:0] contain the least significant byte (LSB) and AD[63:56] contain the most significant byte (MSB). The 82544EI controller may be optionally connected to a 32-bit PCI Local Bus. On a 32-bit bus, AD[63:32] and other signals corresponding to the high order byte lanes do not participate in the bus cycle.
CBE[7:0]#	TS	**Bus Command and Byte Enables.** Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, CBE#[7:0] define the bus command. During the data phase CBE#[7:0] are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. CBE#[0] applies to byte 0 (LSB) and CBE#[7] applies to byte 7 (MSB).
PAR	TS	**Parity.** Parity issued to implement Even Parity across AD[31:0] and CBE#[3:0]. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted after a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. When the 82544EI controller is a bus master, it drives PAR for address and write data phases. As a slave, it drives PAR for read data phases.
PAR64	TS	**Parity 64.** Parity issued to implement Even Parity across AD[63:32] and CBE#[7:4]. PAR64 is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted after a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. When the 82544EI controller is a bus master, it drives PAR64 for address and write data phases. As a slave, it drives PAR64 for read data phases.
FRAME#	STS	**FRAME.** FRAME# is driven by the 82544EI device to indicate the beginning and duration of an access. FRAME# is asserted to indicate the beginning of a bus transaction. While FRAME# is asserted, data transfers continue. When FRAME# is asserted, the transaction is in the final data phase.
IRDY#	STS	**Initiator Ready.** IRDY# indicates the ability of the 82544EI controller (as a bus master device) to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock in which both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[63:0]. During a read, it indicates the master is ready to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82544EI controller drives IRDY# when acting as a master and samples it when acting as a slave.

Signal Name	Type	Name and Function
TRDY#	STS	**Target Ready.** TRDY# indicates the ability of the 82544EI controller (as a selected device) to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock in which both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[63:0]. During a write, it indicates the target is ready to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82544EI device drives IRDY# when acting as a slave and samples it when acting as a master.
STOP#	STS	**Stop.** STOP# indicates the current target is requesting the master to stop the current transaction. As a slave, the 82544EI controller drives STOP# to request the bus master to stop the transaction. As a master, the 82544EI controller receives STOP# from the slave and stops the current transaction.
IDSEL	I	**Initialization Device Select.** IDSEL is used by the 82544EI device as a chip select during configuration read and write transactions.
DEVSEL#	STS	**Device Select.** When being actively driven by the 82544EI controller, DEVSEL# indicates to the bus master that it has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
VIO	P	**VIO.** VIO is a voltage reference for PCI interface (3.3 V or 5 V). It is used as the clamping voltage. **NOTE:** An external resistor is required between the voltage reference and the VIO balls.The targeted resistor value is 100 KΩ.

3.2.2 Arbitration Signals

Signal Name	Type	Name and Function
REQ64#	TS	**Request Transfer.** REQ64# is generated by the current initiator to indicate its desire to perform a 64-bit transfer. REQ64# has the same timing as the FRAME# signal.
ACK64#	TS	**Acknowledge Transfer.** ACK64# is generated by the currently-addressed target in response to a REQ64# assertion by the initiator. ACK64# has the same timing as the DEVSEL# signal.
REQ#	TS	**Request Bus.** REQ# indicates to the arbiter that the 82544EI controller desires use of the bus. This is a point to point signal.
GNT#	I	**Grant Bus.** GNT# indicates to the 82544EI device that access to the bus has been granted. This is a point to point signal
LOCK#	I	**Lock Bus.** LOCK# is asserted by an initiator to require sole access to a target memory device during two or more separate transfers. The 82544EI device does not implement bus locking.

3.2.3 Interrupt Signal

Signal Name	Type	Name and Function
INTA#	TS	**Interrupt A.** The signal is used to request an interrupt by the 82544EI controller. This is an active low, level-triggered interrupt signal.

3.2.4 System Signals

Signal Name	Type	Name and Function
CLK	I	**PCI_Clock.** CLK provides timing for all transactions on the PCI bus and is an input to the 82544EI device. All other PCI signals, except RST# and INTA# lines are sampled on the rising edge of CLK. All other timing parameters are defined with respect to this edge.
M66EN	I	**66 MHz Enable.** M66EN indicates whether the system bus is enabled for 66MHz if the slot is capable of that operating frequency. This signal is ignored by the 82544EI controller, but should be connected properly for future compatibility.
RST#	I	**PCI Reset.** Most of the internal state of the 82544EI controller is reset on the de-assertion (rising edge) of RST#. Whenever RST# is asserted, all PCI output signals except PME# are floated and inputs are ignored. The PME# context is preserved, depending on power management settings.

3.2.5 Error Reporting Signals

Signal Name	Type	Name and Function
SERR#	OD	**System Error.** SERR# is used by the 82544EI controller to report address parity errors. SERR# is open drain and is actively driven for a single PCI clock when reporting the error.
PERR#	STS	**Parity Error.** PERR# is used by the 82544EI controller to report data parity errors during all PCI transactions except by a Special Cycle. PERR# is sustained tri-state and must be driven active by the 82544EI controller receive data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected.

3.2.6 Power Management Signals

Signal Name	Type	Name and Function
LAN_PWR_GOOD	I	**Power Good (Power-On Reset).** The LAN_PWR_GOOD signal indicates that good power is available for 82544EI device. When the signal is zero, the 82544EI controller will hold the entire chip in reset state and float all PCI signals.
PME#	OD	**Power Management Event.** The 82544EI device will drive this signal to zero when it receives a wakeup event and either the PME_En bit in the Power Management Control / Status Register is 1 or the Advanced Power Management Enable (APME) bit of the Wake Up Control Register (WUC) is 1.
APM_WAKEUP	O	**Advance Power Management Wakeup.** When APM Wakeup is enabled in the 82544EI controller and the 82544EI controller receives a Magic Packet* it will set this signal to a logic 1 for 50 ms.
AUX_PWR	I	**Auxiliary Power Available.** If AUX_PWR equals 1, it indicates that Auxiliary Power is available and the 82544EI device should support $D3_{cold}$ power state.
PWR_STATE[1:0]	O	**Power State.** The bits are set in the following power states: 00b = D0u, D1, or D3 state with wakeup disabled • No PHY operation is required 01b = D0u, D1, or D3 state with wakeup enabled • PHY operation is required in this state, although it may be at low speed. 11b = D0 active state • Full speed PHY operation is required. The resulting meaning of the bits is as follows: • Bit 1: asserted when normal (full power/speed) operation is required. • Bit 0: asserted when link is required. The polarity of bit 0 and 1 may be individually inverted by setting the IPS0 and IPS1 bits in the Extended Device Control Register (CTRL_EXT), respectively.

3.2.7 Impedance Compensation Signals

Signal Name	Type	Name and Function
ZN_COMP	I/O	**N Device Impedance Compensation.** Connect to an external precision resistor (to VDD) that is indicative of the PCI/PCI-X trace load. This cell is used to dynamically determine the drive strength required on the N-channel transistors in the PCI/PCI-X IO cells.
ZP_COMP	I/O	**P Device Impedance Compensation.** Connect to an external precision resistor (to VSS) that is indicative of the PCI/PCI-X trace load. This cell is used to dynamically determine the drive strength required on the P-channel transistors in the PCI/PCI-X IO cells.

3.3 Ten-Bit Interface (TBI) Signals

The TBI is a MAC interface that can connect to an external Serializer/Deserializer (SERDES) device for fiber-based designs. When the 82544EI controller is not in TBI mode, the TBI signals are in a high-impedance state.

The 82544EI device has a special GMII test mode for the IEEE Unfiltered Jitter Test. This test mode reuses the TBI signals as GMII outputs. After PHY conformance testing is completed, it is permissible to gang the TBI interface pins together to reduce the number of pulldown resistors needed.

Signal Name	Type	Name and Function
TBI_MODE	I	**TBI Mode Enable.** This signal forces the device into TBI mode when TBI_MODE is asserted (high).
TX_DATA[9:0]	O	**Transmit Data.** Parallel TBI data bus to be transmitted through a serializer/deserializer (SERDES). If TBI mode is not used, connect these pins to ground through pulldown resistors. During GMII test mode these pins become GMII outputs.
GTX_CLK	O	**Transmit Clock.** Operates at 125 MHz. If TBI mode is not used, connect this ball to ground through a pulldown resistor. During GMII test mode this pin becomes the transmit clock test output.
EWRAP	O	**Enable Wrap.** EWRAP is low in normal operation. When it is high, the SERDES device is forced to transceiver loopback the serialized transmit data to the receiver. If TBI mode is not used, connect this ball to ground through a pulldown resistor.
RX_DATA[9:0]	I	**Receive Data.** Parallel TBI data bus received from a serializer/ deserializer (SERDES). If TBI mode is not used, connect these balls to ground through a pulldown resistor. During GMII test mode these pins become GMII outputs.
RBC0	I	**Receive Clock.** RBC0 is the 62.5 MHz receive clock. If TBI mode is not used, connect this ball to ground through a pulldown resistor. During GMII test mode this pin becomes an output.
RBC1	I	**Receive Clock:** RBC1 is the 62.5 MHz receive clock shifted 180 degrees from RBC0. If TBI mode is not used, connect this ball to ground through a pulldown resistor. During GMII test mode this pin becomes the receive clock test output.

3.4 EEPROM/FLASH Interface Signals

Signal Name	Type	Name and Function
EE_DI	O	**EEPROM DI.** This pin is an output to the memory device.
EE_DO	I	**EEPROM DO.** This pin is an input from the memory device. Internal pullup resistor provided.
EE_CS	O	**EEPROM CSO.** Used to enable the device.
EE_SK	O	**EEPROM Serial Clock.** The clock rate of the EEPROM interface is approximately 1 MHz.
FL_ADDR[18:0]	O	**FLASH Address Outputs.** Used to FLASH or Boot ROM
FL_CS#	O	**FLASH Chip Select.** Used to enable FLASH or Boot ROM
FL_OE#	O	**FLASH Output Enable.** Used to enable buffers in FLASH.
FL_WE#	O	**FLASH Write Enable Output.** Used for write cycles.
FL_DATA[7:0]	TS	**FLASH Data I/O.** Bi-directional data bus for FLASH data. These signals have internal pullup devices.

3.5 Miscellaneous Signals

3.5.1 LED Signals

Signal Name	Type	Name and Function
LINK_UP#	O	**Link Up.** LINK_UP# indicates link connectivity
RX_ACTIVITY#	OD	**Receive Activity.** Flashes an LED to indicate link receive activity. This output uses an open drain cell to allow a wired-OR of activity signals.
TX_ACTIVITY#	OD	**Transmit Activity.** Flashes an LED to indicate link transmit activity. This output uses an open drain cell to allow a wired-OR of activity signals.
LINK10#	OD	**Link 10.** Drives an LED to indicate link at 10 Mbps. This output uses an open drain cell.
LINK100#	OD	**Link 100.** Drives an LED to indicate link at 100 Mbps. This output uses an open drain cell.
LINK1000#	OD	**Link 1000.** Drives an LED to indicate link at 1000 Mbps. This output uses an open drain cell.

3.5.2 Other Signals

Signal Name	Type	Name and Function
LOS	I	**Loss of Signal.** Loss of signal from the optical transceiver when TBI_MODE=1
XOFF	I	**External XOFF.** This is an external indication of the Above High Threshold for flow control.
XON	I	**External XON.** This provides an external indication of Below Low Threshold for flow control.

Signal Name	Type	Name and Function
ABV_HI	O	**Above High Threshold.** Output indicating the RX FIFO fullness is above the programmed high threshold.
BLW_LO	O	**Below Low Threshold.** Output indicating the RX FIFO fullness is below the programmed low threshold.
SDP[7:6] SDP[4:0]	TS	**S/W Defined Pins.** These pins are reserved pins which are software programmable with respect to input/output capability. These default to inputs upon power up but may have their direction and output values defined in the EEPROM. The upper four bits may be mapped to the General Purpose Interrupt bits when configured as inputs. **SPECIAL NOTE:** SDP5 is intentionally missing from the group of software-defined pins.
TEST0	I	**Factory Test Pin.** Connect this ball to ground through a pulldown resistor.
TEST1		**Factory Test Pin.** Attach an external pullup resistor to the pin to ensure the test mode is disabled. Use a common value resistor such as 1 KΩ (the value is not critical). Alternatively, the pin may be connected directory to the 3.3V supply.
GMII_TEST[1:0]	I	**GMII Test Mode Pins.** For normal operation, the test pins are connected to ground through a common pulldown resistor. For PHY Unfiltered Jitter Test, drive both pins high.
COL_TEST	O	**Collision Test Pin.** For normal operation, these pins are connected to ground through a pulldown resistor. During GMII test mode it is driving as an output.
CRS_TEST	O	**Carrier Sense Test Pin.** For normal operation, this pin is connected to ground through a pulldown resistor. It is driven as an output during GMII test mode.

3.6 PHY Signals

3.6.1 Crystal Signals

Signal Name	Type	Name and Function
XTAL1	I	**XTAL1.** 25MHz +/- 30 ppm input; can be connected to an oscillator or a crystal. If a crystal is used, XTAL2 must be connected as well.
XTAL2	O	**XTAL2.** Output of internal oscillator circuit used to drive crystal into oscillation. If an external oscillator is used, XTAL2 must be disconnected.

3.6.2 Analog Signals

Signal Name	Type	Name and Function
REF	P	**Reference.** External 2.49 KΩ resistor connection to VSS.
MDI[0]+/-	A	**Media Dependent Interface[0].** 1000BASE-T: In MDI configuration, MDI[0]+/- corresponds to BI_DA+/- and in MDIX configuration MDI[0]+/- corresponds to BI_DB+/-. 100BASE-TX: In MDI configuration, MDI[0]+/- is used for the transmit pair and in MDIX configuration MDI[0]+/- is used for the receive pair. 10BASE-T: In MDI configuration, MDI[0]+/- is used for the transmit pair and in MDIX configuration MDI[0]+/- is used for the receive pair.
MDI[1]+/-	A	**Media Dependent Interface[1].** 1000BASE-T: In MDI configuration, MDI[1]+/- corresponds to BI_DB+/-, and in MDIX configuration, to the BI_DA+/-. 100BASE-TX: In MDI configuration, MDI[1]+/- is used for the receive pair, and in MDIX configuration, the transmit pair. 10BASE-T: In MDI configuration, MDI[1]+/- is used for the receive pair, and in MDIX configuration, the transmit pair.
MDI[2]+/-	A	**Media Dependent Interface[2].** 1000BASE-T: In MDI configuration, MDI[2]+/- corresponds to BI_DC+/-, and in MDIX configuration, to the BI_DD+/-. 100BASE-TX: Unused. 10BASE-T: Unused.
MDI[3]+/-	A	**Media Dependent Interface[3].** 1000BASE-T: In MDI configuration, MDI[3]+/- corresponds to BI_DD+/-, and in MDIX configuration, to the BI_DC+/-. 100BASE-TX: Unused. 10BASE-T: Unused.

3.7 Test Interface Signals

Signal Name	Type	Name and Function
JTAG_TCK	I	**JTAG Clock.** Input to device
JTAG_TDI	I	**JTAG TDI.** Input to device
JTAG_TDO	O	**JTAG TDO.** Output from device
JTAG_TMS	I	**JTAG TMS.** Input to device
JTAG_TRST#	I	**JTAG Reset.** Active low reset for JTAG. Terminate this signal through a resistor to ground. Do not leave unconnected.

3.8 Power Supply Connections

3.8.1 Digital Supplies

Signal Name	Type	Name and Function
VDDO	P	**VDDO.** 3.3 V I/O power supply.
DVDDH	P	**DVDDH.** 1.8 V Digital core power supply.
DVDDL	P	**DVDDL.** 1.5 V Digital core power supply.

3.8.2 Analog Supplies

Signal Name	Type	Name and Function
AVDDH	P	**AVDDH.** 3.3 V Analog power supply.
AVDDL	P	**AVDDL.** 2.5 V Analog power supply.

3.8.3 Ground and No Connects

Signal Name	Type	Name and Function
GND	P	**Grounds.**
NO_CONNECT	P	**No Connects.** Do not connect to these pins to any circuit. Do not use pullup or pulldown resistors.

4.0 Targeted Electrical and Timing Specifications

4.1 Targeted Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings (Referenced to VSS [Ground])[a]

Symbol	Parameter	Min	Max	Units
$V_{DD(3.3)}$	DC supply voltage on VDDD or AVDDH with respect to VSS	VSS - 0.5	4.6	V
$V_{DD(2.5)}$	DC supply voltage on AVDDL with respect to VSS	VSS - 0.5	4.6 or $V_{DD(2.5)}$ + 0.5 (whichever is less)[b]	V
$V_{DD(1.8)}$	DC supply voltage on DVDDH with respect to VSS	VSS - 0.5	4.6 or $V_{DD(2.5)}$ + 0.5 (whichever is less)[b]	V
$V_{DD(1.5)}$	DC supply voltage on DVDDL with respect to VSS	VSS - 0.5	4.6 or $V_{DD(2.5)}$ + 0.5 (whichever is less)[b]	V
V_{DD}	DC supply voltage	VSS - 0.5	4.6	V
VI / VO	LVTTL input voltage	VSS - 0.5	4.6	V
VI / VO	5 V compatible input voltage	VSS - 0.5	6.6	V
I_O	DC output current (by cell type): $I_{OL = 1mA}$ $I_{OL = 2 mA}$ $I_{OL = 3 mA}$ $I_{OL = 6 mA}$ $I_{OL = 9 mA}$ $I_{OL = 12 mA}$ $I_{OL = 18 mA}$ $I_{OL = 24 mA}$		 3 7 10 20 30 40 60 75	mA
T_{STG}	Storage temperature range	-40	125	°C
	ESD per MIL_STD-883 Test Method 3015, Specification 2001V Latchup Over/Undershoot: ±150 mA, 125 C		V_{DD} overstress: $V_{DD(3.3)}$(7.2 V)	V

a. Permanent device damage is likely to occur if the ratings in this table are exceeded. These values should not be used as the limits for normal device operations.
b. This specification applies to biasing the device to a steady state for an indefinite duration. During normal device powerup, explicit power sequencing is not required.

4.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions[a]

Symbol	Parameter	Min	Max	Units
$V_{DD(3.3)}$	DC supply voltage on VDDD or AVDDH[b]	3.0	3.6	V
$V_{DD(2.5)}$	DC supply voltage on AVDDL[c]	2.38	2.62	V
$V_{DD(1.8)}$	DC supply voltage on DVDDH[c]	1.71	1.89	V
$V_{DD(1.5)}$	DC supply voltage on DVDDL[c]	1.43	1.57	V
VIO	PCI bus voltage reference	3.0	5.25	V
t_R/t_F	Input rise/fall time (normal input)	0	200	ns
t_r/t_f	Input rise/fall time (Schmitt input)	0	10	ms
T_A	Operating temperature range (ambient)	0	70	C
T_J	Junction temperature		≤125	C

a. For normal device operations, adhere to the limits in this table. Sustained operation of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, might result in permanent guaranteed if conditions exceed recommended operating conditions.
b. It is recommended that VDD0 = AVDDH during powerup and normal operation.
c. It is recommended that both VDDO and AVVDH are greater than AVDDL > DVDDH > DVDDL during powerup. However, voltage sequencing is not a strict requirement as long as the power supply ramp is faster than approximately 200 ms.

4.3 Targeted DC Specifications

Table 3. DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD(3.3)}$	DC supply voltage on VDDO or AVDDH		3.00	3.3	3.60	V
$V_{DD(2.5)}$	DC supply voltage on AVDDL		2.38	2.5	2.62	V
$V_{DD(1.8)}$	DC supply voltage on DVDDH		1.71	1.8	1.89	V
$V_{DD(1.5)}$	DC supply voltage on DVDDL		1.43	1.5	1.57	V

Table 4. Power Supply Characteristics – 1 (Sheet 1 of 2)

Symbol	Parameter	Condition	Min	Typ[a]	Max[b]	Units
$I_{CC(3.3)}$	3.3 V supply current	TBI mode		200	230	mA
		1000BASE-T		130	160	
		100BASE-T		90	110	
		10BASE-T		85	105	
		Powerdown[c]		85	105	
		Quiescent[d]		50	60	

Table 4. Power Supply Characteristics – 1 (Sheet 2 of 2) (Continued)

Symbol	Parameter	Condition	Min	Typ[a]	Max[b]	Units
$I_{CC(2.5)}$	2.5 V supply current	TBI mode		2.2	2.6	mA
		1000BASE-T		340	410	
		100BASE-T		85	105	
		10BASE-T		125	150	
		Powerdown[c]		85	105	
		Quiescent[d]		2.0	2.5	
$I_{CC(1.8)}$	1.8 V supply current	TBI mode		170	200	mA
		1000BASE-T		300	360	
		100BASE-T		160	200	
		10BASE-T		110	135	
		Powerdown[c]		90	110	
		Quiescent[d]		15	20	
$I_{CC(1.5)}$	1.5 V supply current	TBI mode		0.4	0.5	mA
		1000BASE-T		200	240	
		100BASE-T		0.3	0.4	
		10BASE-T		0.2	0.3	
		Powerdown[c]		0.1	0.15	
		Quiescent[d]		0.1	0.15	

a. Typical conditions are T_A = 25 C, voltages are nominal. Where applicable, network traffic is moderate at full duplex and the system interface is PCI 66 MHz.
b. Maximum conditions are T_A = minimum, voltages are maximum. Where applicable, network traffic is continuous at full duplex and the system interface is PCI-X 100 to 133 MHz.
c. In the powerdown mode, the controller is in the $D3_{hot}$ state, with PME# wake-up enabled. Link is present at 100 Mbps.
d. In the quiescent mode, the controller is in the $D3_{cold}$ state, with wake-up disabled. Link is not present.

Table 5. Power Supply Characteristics – 2 (Sheet 1 of 2)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	LVTTL	2.0		$V_{DD(3.3)}$	V
		5 V tolerant	2.0		5.5	
		3.3 V PCI	$0.5_{VDD(3.3)}$		$V_{DD(3.3)}$	
V_{IL}	Input low voltage	LVTTL	VSS		0.8	V
		5 V tolerant	VSS		0.8	
		3.3 V PCI	VSS		$0.3V_{DD(3.3)}$	
V_{T+}	Switching threshold: Positive edge	LVTTL & 5 V tolerant	1.2		2.4	V
V_{T+}	Switching threshold: Negative edge	LVTTL & 5 V tolerant	0.6		1.8	V
V_H	Schmitt trigger-hysteresis		0.3		1.5	V

Table 5. Power Supply Characteristics – 2 (Sheet 2 of 2) (Continued)

Symbol	Parameter		Condition	Min	Typ	Max	Units
I_{IN}	Input current		$V_{IN} = V_{DD(3.3)}$ or VSS	-10		10	µA
	Inputs with pull-down resistor (50 KΩ)		$V_{IN} = V_{DD(3.3)}$	28		191	
	Inputs with pull-up resistor (5 KΩ)		V_{IN} = VSS	-28		-191	
I_{OL}	Output low current:						mA
	Type LVTTL	3 mA	V_{OL} = 0.4 V	3			
		6 mA		6			
		12 mA		12			
	Type: 5 V tol	3 mA		3			
		6 mA		6			
I_{OH}	Output high current						mA
	Type: LVTTL	3 mA	V_{OL} = 0.4 V	-3			
		6 mA		-6			
	Type: 5 V tol	3 mA		-2			
		6 mA		-2			
V_{OH}	Output high voltage						V
	LVTTL		I_{OH} = 0 mA	$V_{DD(3.3)}$ -0.1			
	5 V tolerant		I_{OH} = 0 mA	$V_{DD(3.3)}$ -0.2			
	3.3 V PCI		I_{OH} = -500 µA	$0.9V_{DD(3.3)}$			
V_{OL}	Output low voltage						V
	LVTTL		I_{OL} = 0 mA	0.1			
	5 V tolerant		I_{OL} = 0 mA	0.1			
	3.3 V PCI		I_{OL} = 1500 µA	$0.1V_{DD(3.3)}$			
I_{OZ}	Off-state output leakage current		$V_O = V_{DD}$ or VSS	-10		10	µA
I_{OS}	Output short circuit current					-250	µA
C_{IN}	Input capacitance[a]		Input and bi-directional buffers		4		pF
			5 V tolerant		8		
C_{OUT}	Output capacitance[a]		Output buffers		6		pF
			5 V tolerant		10		

a. $V_{DD(3.3)}$ = 0 V; T_A = 25 C; f = 1 MHz

4.4 Targeted AC Characteristics

Table 6. AC Characteristics: 3.3 V Interfacing

Symbol	Parameter	Min	Typ	Max	Units
f_{PCICLK}	CLK frequency in PCI mode			66	MHz
	CLK frequency in PCI-X mode	66		133	

Table 7. Switching Current

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{OH(min)}$	Switching current high	$V_{OUT} = 0.3V_{CC(3.3)}$	TBD			mA
$I_{OH(max)}$	Switching current high	$V_{OUT} = 0.7V_{CC(3.3)}$			TBD	mA
$I_{OL(min)}$	Switching current low	$V_{OUT} = 0.6V_{CC(3.3)}$	TBD			mA
$I_{OL(max)}$	Switching current low	$V_{OUT} = 0.18V_{CC(3.3)}$			TBD	mA

Table 8. 25Mhz Clock Input Requirements

Symbol	Parameter[a]	Min	Typ	Max	Units
$f_{i\_TX\_CLK}$	TX_CLK_IN Frequency	25 – 50 ppm	25	25 + 50 ppm	MHz

a. This parameter applies to an oscillator connected to the XTAL1 input. Alternatively, a crystal may be connected to XTAL1 and XTAL 2 as the frequency source for the internal oscillator.

Table 9. Link Interface Clock Requirements

Symbol	Parameter	Min	Typ	Max	Units
f_{GTX}[a]	GTX_CLK Frequency GMII Mode (1000 Mb/s)		125		MHz

a. GTX_CLK is used externally only for test purposes.

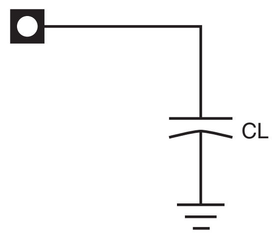
Table 10. EEPROM Interface Clock Requirements

Symbol	Parameter	Min	Typ	Max	Units
f_{SK}	O_EE_SK Frequency			1	MHz

Table 11. AC Test Loads for General Output Pins

Symbol	Signal Name	Value	Units
C_L	TDO	10	pF
C_L	EWRAP, GTX_CLK, ABV_HI, BLW_LO, PWR_STATE[1:0], APM_WAKEUP, PME#, TX_DATA,[9:0], SDP[7:0]	16	pF
C_L	FL_ADDR[18:0], FL_OE#, FL_CS#, FL_WE#, FL_DATA[7:0], EE_SK, EE_DI	18	pF
C_L	RX_ACTIVITY, TX_ACTIVITY, LINK_UP	20	pF

Figure 2. AC Test Loads for General Output Pins



4.5 Targeted Timing Specifications

Note: Timing specifications are **preliminary** and subject to change.

4.5.1 PCI/PCI-X Bus Interface

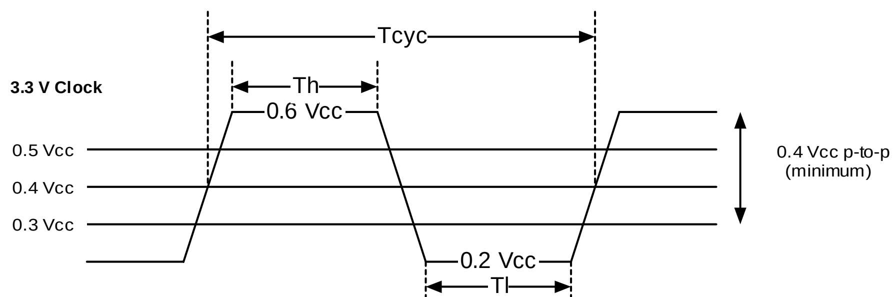
4.5.1.1 PCI/PCI-X Bus Interface Clock

Table 12. PCI/PCI-X Bus Interface Clock Parameters

Symbol	Parameter[a]	PCI-X 133 MHz		PCI-X 66 MHz		PCI 66 MHz		PCI 33 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
T_{CYC}	CLK Cycle Time	7.5	20	15	20	15	30	30	∞	ns	
T_H	CLK High Time	3		6		6		11		ns	
T_L	CLK Low Time	3		6		6		11		ns	
	CLK Slew Rate	1.5	4	1.5	4	1.5	4	1	4	V/ns	a
	RST# Slew Rate[b]	50		50		50		50		mV/ns	b

a. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown.
b. The minimum RST# slew rate applies only to the rising (de-assertion) edge of the reset signal, and ensures that system noise cannot render an otherwise monotonic signal to appear to bounce in the switching range.

Figure 3. PCI/PCI-X Clock Timing



4.5.1.2 PCI/PCI-X BUS Interface Timing

Table 13. PCI/PCI-X BUS Interface Timing Parameters[a, b, c]

Symbol	Parameter	PCI-X 133 MHz		PCI-X 66 MHz		PCI 66 MHz		PCI 33 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
T_{VAL}	CLK to Signal Valid Delay - bused signals	0.7	3.8	0.7	3.8	2	6	2	11	ns	a,b,c
T_{VAL}(ptp)	CLK to Signal Valid Delay - point-to-point signals	0.7	3.8	0.7	3.8	2	6	2	12	ns	a,b,c
T_{ON}	Float to Active Delay	0		0		2		2		ns	a
T_{OFF}	Active to Float Delay		7		7		14		28	ns	a
T_{SU}	Input Setup Time to - bused signals	1.2		1.7		3		7		ns	c
T_{SU}(ptp)	Input Setup Time to CLK - point-to-point signals	1.2		1.7		5		10,12		ns	c
T_H	Input Hold Time from CLK	0.5		0.5		0		0		ns	
T_{RRSU}	REQ64# to RST# setup time	10* T_{CYC}		10* T_{CYC}		10* T_{CYC}		10* T_{CYC}		ns	
T_{RRH}	RST# to REQ64# hold time	0		0		0		0		ns	

a. Output timing measurement as shown.
b. REQ# and GNT# are point-to-point signals, and have different output valid delay and input set up times than do bused signals. GNT# has a set up of 10; REQ# has a set up of 12. All other signals are bused
c. Input timing measurement as shown.

Figure 4. PCI Bus Interface Output Timing Measurement Conditions

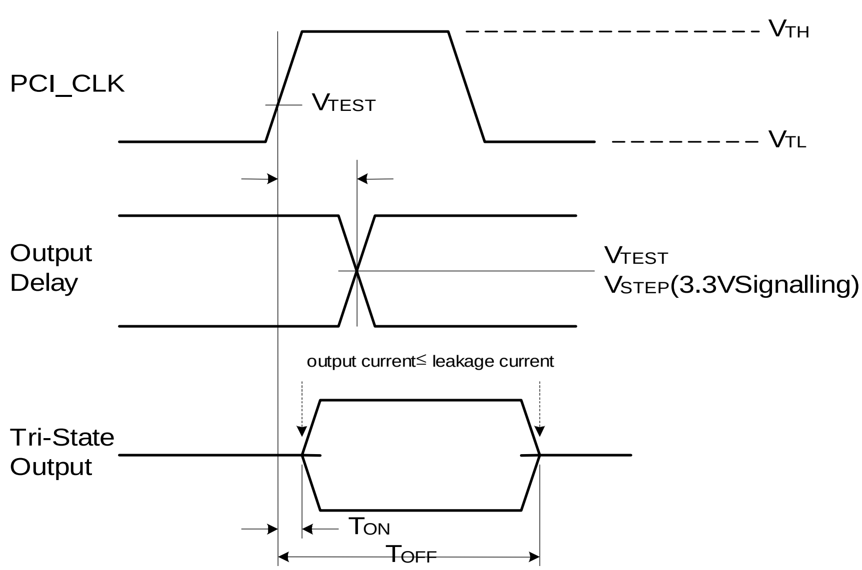


Figure 5. PCI Bus Interface Input Timing Measurement Conditions

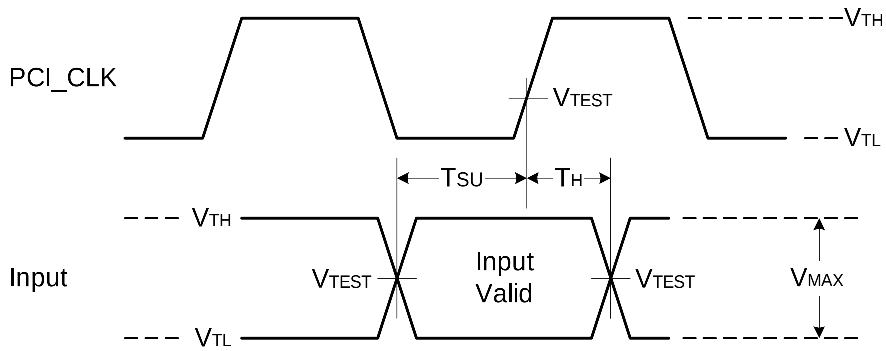


Table 14. PCI/PCI-X Bus Interface Timing Measurement Conditions

Symbol	Parameter	PCI-X	PCI 66 MHz 3.3V	Units	Notes
V_{TH}	Input Measurement Test Voltage (high)	0.6*V_{CC}	0.6*V_{CC}	V	
V_{TL}	Input Measurement Test Voltage (low)	0.25*V_{CC}	0.2*V_{CC}	V	
V_{TEST}	Output Measurement Test Voltage	0.4*V_{CC}	0.4*V_{CC}	V	
	Input Signal Slew Rate	1.5	1.5	V / ns	

Figure 6. T_{VAL} (max) Rising Edge Test Load

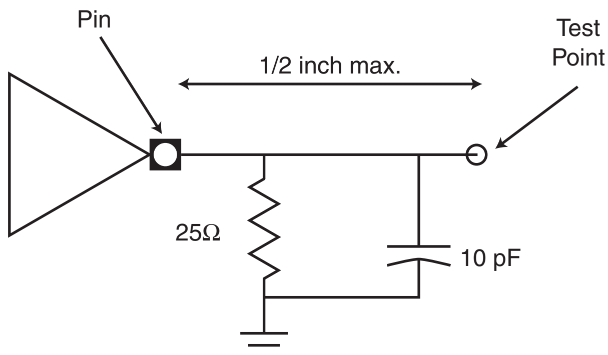


Figure 7. T_{VAL} (max) Falling Edge Test Load

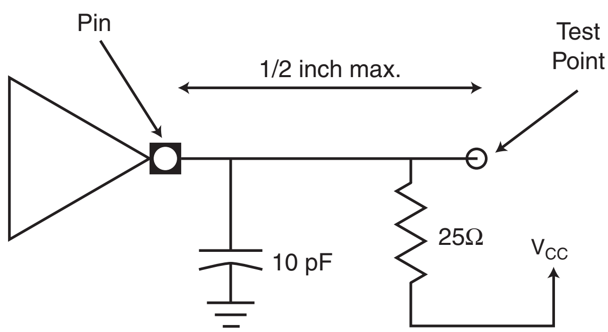


Figure 8. T_{VAL} (min) Test Load

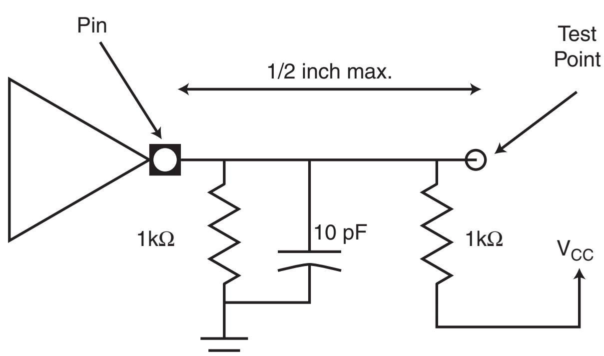
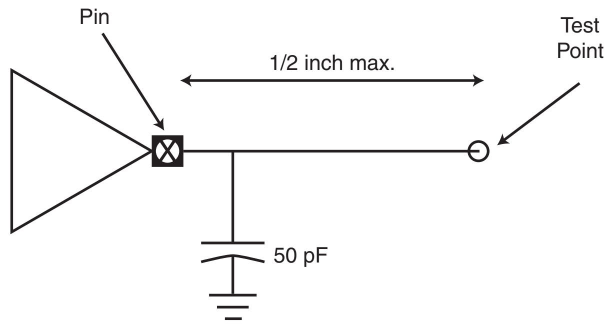
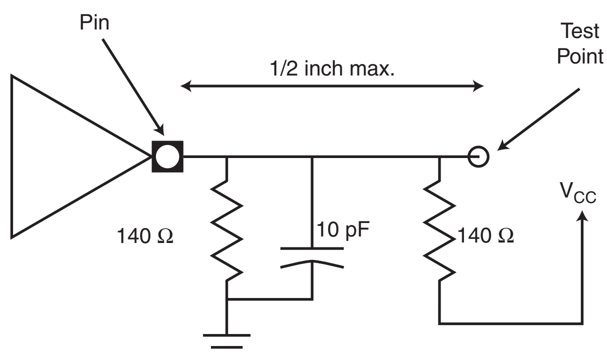


Figure 9. T_{VAL} Test Load (PCI 5V Signalling Environment)



Note: 50 pF load used for maximum times. Minimum times are specified with 0 pF load.

Figure 10. Output Slew Rate Test Load (PCI-X only)



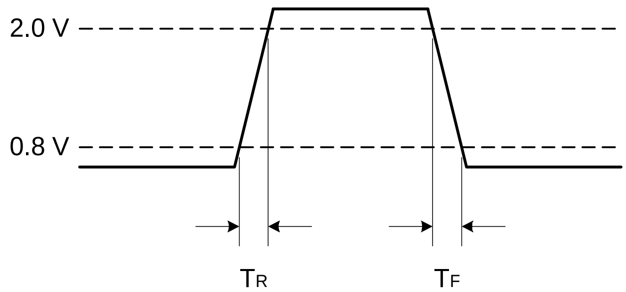
4.5.2 Targeted Link Interface Timing

4.5.2.1 Link Interface Rise and Fall Time

Table 15. Rise and Fall Time Definition

Symbol	Parameter	Condition	Min	Max	Units
T_R	Clock Rise Time	0.8V to 2.0V	0.7		ns
T_F	Clock Fall Time	2.0V to 0.8V	0.7		ns
T_R	Data Rise Time	0.8V to 2.0V	0.7		ns
T_F	Data Fall Time	2.0V to 0.8V	0.7		ns

Figure 11. Link Interface Rise/Fall Timing



4.5.2.2 Link Interface Transmit Timing

Figure 12. Transmit Interface Timing

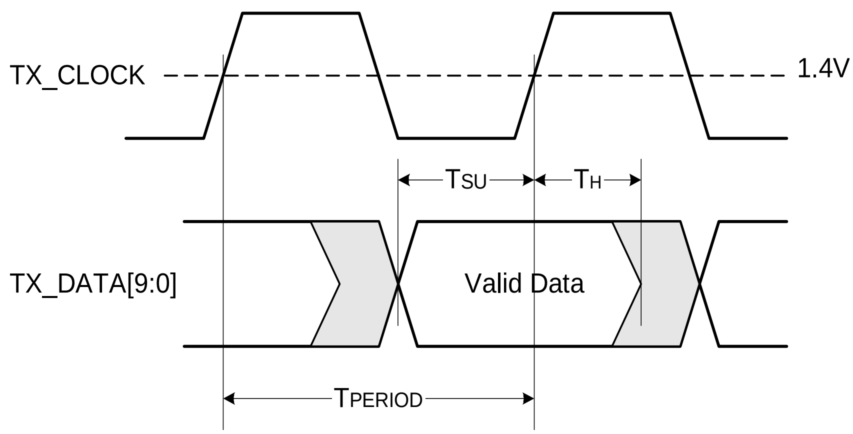


Table 16. Transmit Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{PERIOD}	GTX_CLK Period[a] TBI Mode (1000 Mb/s)		8		ns
T_{SETUP}	Data Setup to Rising GTX_CLK		2.5		ns
T_{HOLD}	Data Hold from Rising GTX_CLK		1.0		ns
T_{DUTY}	GTX_CLK Duty Cycle	40		60	%

a. ±100 ppm tolerance on GTX_CLK

4.5.2.3 Link Interface Receive Interface Timing

Figure 13. Receive Interface Timing

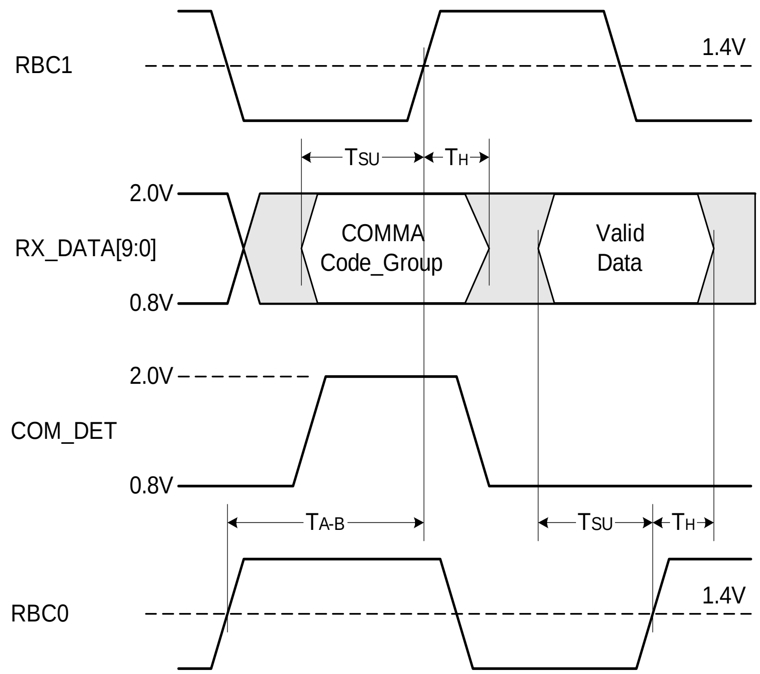


Table 17. Receive Interface Receive Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{FREQ}	RBC0/RBC1 Frequency TBI Mode (1000Mb/s)		62.5		MHz
T_{SETUP}	Data Setup before Rising RBC0 / RBC1		2.5		ns
T_{HOLD}	Data Hold after Rising RBC0 / RBC1		1		ns
T_{DUTY}	RBC0 / RBC1 Duty Cycle	40		60	%
T_{A-B}	RBC0 / RBC1 Skew	7.5		8.5	ns

4.5.3 FLASH Interface

Figure 14. Flash Read Timing

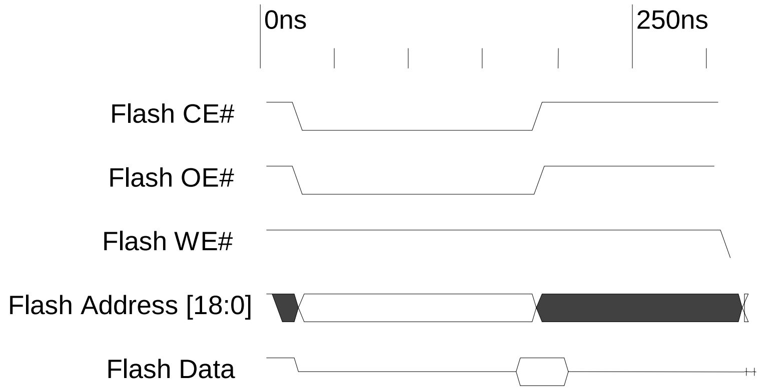


Table 18. Targeted Flash Read Operation Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{CE}	Flash CE# or OE# to Read Data Delay			160	ns
T_{ACC}	Flash Address Setup time			160	ns
T_{HOLD}	Data hold time	0			ns

Figure 15. Flash Write Timing

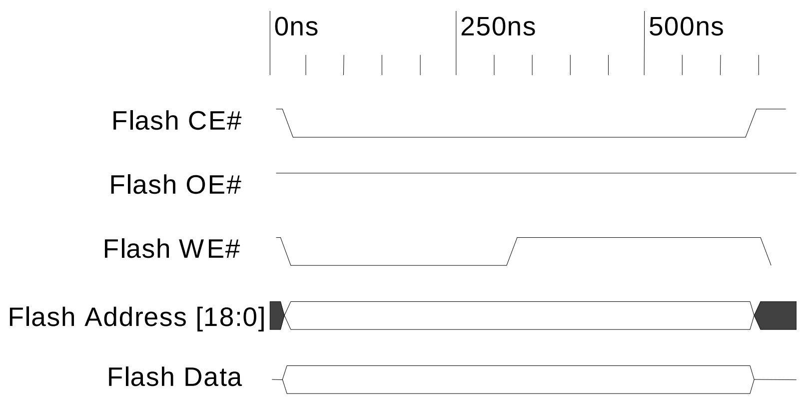


Table 19. Targeted Flash Write Operation Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{WE}	Flash Write Pulse Width (WE#)		160		ns
T_{AH}	Flash Address Hold Time	0			ns
T_{DS}	Flash Data Setup Time	160			ns

4.5.4 EEPROM Interface

Table 20. EEPROM Interface Clock Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{PW}	EE_SK Pulse width[a]		T_{PERIOD}*128		ns

a. The EE_SK EEPROM clock output is derived from GTX_CLK.

Table 21. EEPROM Interface Clock Data Timing

Symbol	Parameter[a]	Min	Typ	Max	Units
T_{DOS}	EE_DO Setup Time	T_{CYC}*2			ns
T_{DOH}	EE_DO Hold Time	0			ns

a. The EE_DO setup and hold time is a function of the CLK cycle time as indicated, but is referenced to O_EE_SK.

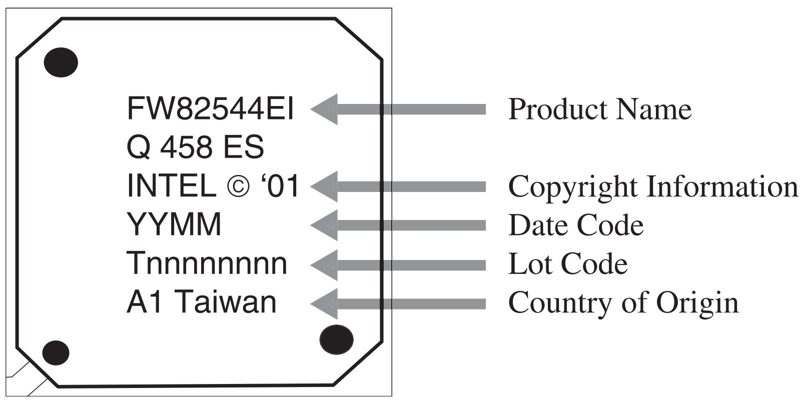
Note: This page intentionally left blank.

5.0 Package and Pinout Information

The 82544EI controller is packaged in a space-saving, 416-lead, ball grid array (BGA) package that measures 27 mm x 27 mm, with a nominal ball pitch of 1 mm.

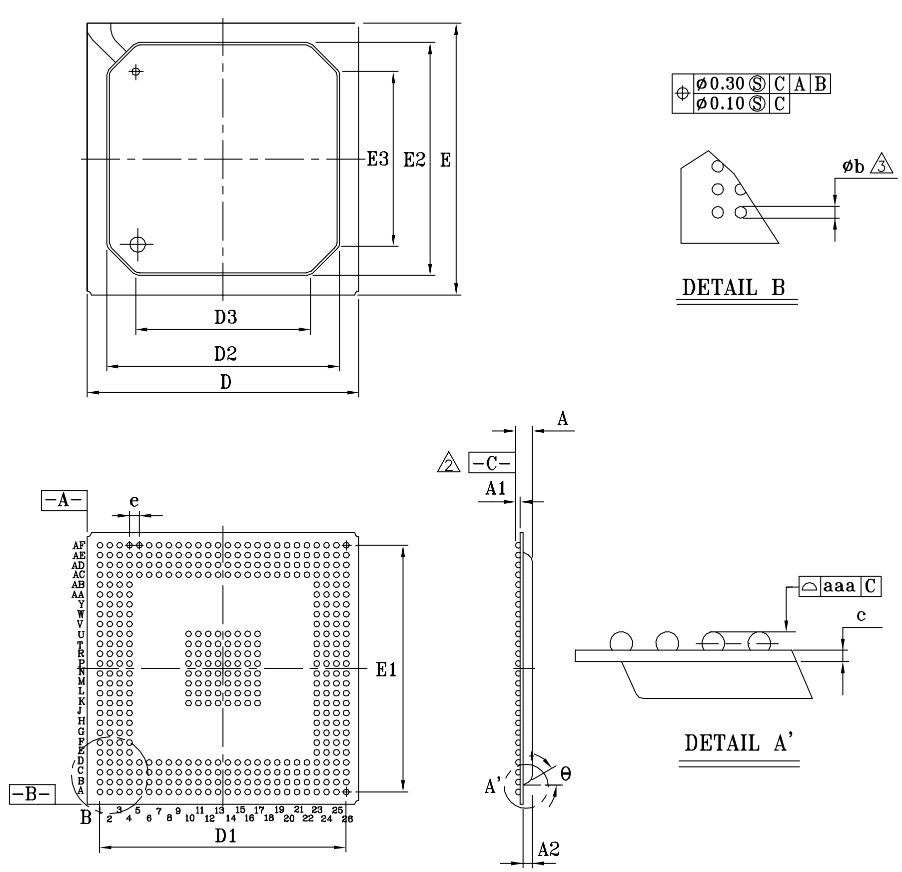
5.1 Device Identification

Figure 16. Device Identification:



5.2 Mechanical Specifications

The drawing on the following page indicates the complete package dimensions:



Symbol	dimension in mm			dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.03	2.23	2.43	0.080	0.088	0.096
A1	0.40	0.50	0.60	0.016	0.020	0.024
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	0.50	0.60	0.70	0.020	0.024	0.028
c	0.51	0.56	0.61	0.020	0.022	0.024
D	26.80	27.00	27.20	1.055	1.063	1.071
D1	—	25.00	—	—	0.984	—
D2	23.80	24.00	24.20	0.937	0.945	0.953
D3	17.95	18.00	18.05	0.707	0.709	0.711
E	26.80	27.00	27.20	1.055	1.063	1.071
E1	—	25.00	—	—	0.984	—
E2	23.80	24.00	24.20	0.937	0.945	0.957
E3	17.95	18.00	18.05	0.707	0.709	0.711
e	—	1.00	—	—	0.039	—
aaa	—	0.15	—	—	0.006	—

NOTE:

1. CONTROLLING DIMENSION: MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25 mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.

TITLE:

SUBSTRATE MATERIAL:

APPR.		DWG NO.	
ENG.		REV NO.	
Q.M		PRODUCT CODE	
CHK.		DATE	
DWG.		SHT No.	

REV NO	DESCRIPTION	DATE

COPY CONTROLLED

5.3 Targeted Thermal Specifications

The 82544EI device is specified for operation when T_A (ambient temperature) is within the range of $0° - 55°C$.

T_C (case temperature) is calculated using the equation:

$T_C = T_A + P (\theta_{JA} - \theta_{JC})$

T_J (junction temperature) is calculated using the equation:

$T_J = T_A + P \theta_{JA}$

P (power consumption) is calculated by using the typical Icc as indicated in Table 4 and nominal Vcc. The thermal resistances are shown in Table 22.

Table 22. 82544GC Gigabit Ethernet Controller Thermal Characteristics

Symbol	Parameter	Value @ Given Airflow (m/s)			Units
		0	1	2	
θ_{JA}	Thermal Resistance, Junction-to-Ambient	16.6	14.6	13.7	°C/Watt
θ_{JC}	Thermal Resistance, Junction-to-Case	0.4	0.4	0.4	°C/Watt

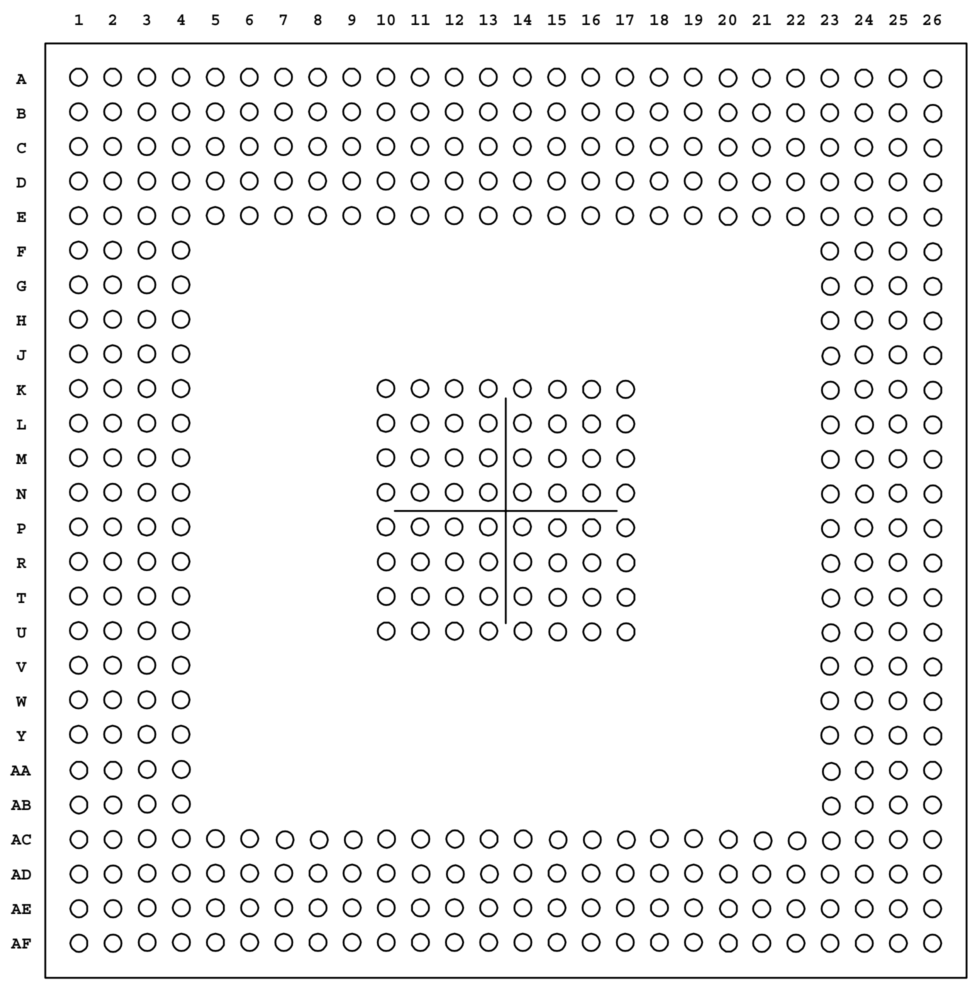
Thermal resistances are determined empirically with test devices mounted on standard thermal test boards. Real system designs may have somewhat different characteristics due to board thickness, arrangement of ground planes, and proximity of other components. Use case temperature measurements to assure that the 82544EI device is operating under recommended conditions.

5.4 Targeted Ball Mapping Diagram

The figure below represents the overall targeted signal ballout map from a top view. Following the figure is a table (in two-column format) mapping the signal names to targeted ball numbers and pad cell types:

Note: The 82544EI device employs five categories of VDD connections:

- VDDO (3.3V)
- DVDDH (1.8V)
- AVDDH (Analog 3.3V)
- AVDDL (Analog 2.5V)
- DVDDL (1.5V)



Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
PCI Address, Data and Control Signals		
AD0	PCI BI-DIR	AF18
AD1	PCI BI-DIR	AD17
AD2	PCI BI-DIR	AF17
AD3	PCI BI-DIR	AC16
AD4	PCI BI-DIR	AE16
AD5	PCI BI-DIR	AF16
AD6	PCI BI-DIR	AC15
AD7	PCI BI-DIR	AD15
AD8	PCI BI-DIR	AC14
AD9	PCI BI-DIR	AE14
AD10	PCI BI-DIR	AF14
AD11	PCI BI-DIR	AD13
AD12	PCI BI-DIR	AC13
AD13	PCI BI-DIR	AF13
AD14	PCI BI-DIR	AE12
AD15	PCI BI-DIR	AC12
AD16	PCI BI-DIR	AF8
AD17	PCI BI-DIR	AC7
AD18	PCI BI-DIR	AD7
AD19	PCI BI-DIR	AF7
AD20	PCI BI-DIR	AE6
AD21	PCI BI-DIR	AC6
AD22	PCI BI-DIR	AF6
AD23	PCI BI-DIR	AD5
AD24	PCI BI-DIR	AF4
AD25	PCI BI-DIR	AC1
AD26	PCI BI-DIR	AE4
AD27	PCI BI-DIR	AC2
AD28	PCI BI-DIR	AB3
AD29	PCI BI-DIR	AC3
AD30	PCI BI-DIR	AB1
AD31	PCI BI-DIR	AB4
AD32	PCI BI-DIR	P24
AD33	PCI BI-DIR	P23
AD34	PCI BI-DIR	R26
AD35	PCI BI-DIR	R25
AD36	PCI BI-DIR	R23

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
AD37	PCI BI-DIR	T26
AD38	PCI BI-DIR	T24
AD39	PCI BI-DIR	T23
AD40	PCI BI-DIR	U26
AD41	PCI BI-DIR	U25
AD42	PCI BI-DIR	U23
AD43	PCI BI-DIR	V26
AD44	PCI BI-DIR	V24
AD45	PCI BI-DIR	W26
AD46	PCI BI-DIR	W25
AD47	PCI BI-DIR	W23
AD48	PCI BI-DIR	Y26
AD49	PCI BI-DIR	Y24
AD50	PCI BI-DIR	Y23
AD51	PCI BI-DIR	AA26
AD52	PCI BI-DIR	AA25
AD53	PCI BI-DIR	AA23
AD54	PCI BI-DIR	AB26
AD55	PCI BI-DIR	AB24
AD56	PCI BI-DIR	AB23
AD57	PCI BI-DIR	AC25
AD58	PCI BI-DIR	AC24
AD59	PCI BI-DIR	AD23
AD60	PCI BI-DIR	AC22
AD61	PCI BI-DIR	AC21
AD62	PCI BI-DIR	AD21
AD63	PCI BI-DIR	AF21
CBE0#	PCI BI-DIR	AF15
CBE1#	PCI BI-DIR	AF12
CBE2#	PCI BI-DIR	AE8
CBE3#	PCI BI-DIR	AF5
CBE4#	PCI BI-DIR	AC20
CBE5#	PCI BI-DIR	AE20
CBE6#	PCI BI-DIR	AF20
CBE7#	PCI BI-DIR	AC19
PAR	PCI BI-DIR	AC11
PAR64	PCI BI-DIR	AD19
FRAME#	PCI BI-DIR	AC8

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
IRDY#	PCI BI-DIR	AF9
TRDY#	PCI BI-DIR	AD9
STOP#	PCI BI-DIR	AE10
IDSEL	PCI BI-DIR	AC5
DEVSEL#	PCI BI-DIR	AF10
VIO	Power	AF3
VIO	Power	AF24
Arbitration Signals		
REQ64#	PCI BI-DIR	AF19
ACK64#	PCI BI-DIR	AC18
REQ#	PCI BI-DIR	AA1
GNT#	PCI BI-DIR	AA4
LOCK#	PCI BI-DIR	AC10
Interrupt Signal		
INTA#	PCI BI-DIR	W2
System Signals		
CLK	PCI IN	Y3
M66EN	PCI IN	AE18
RST#	PCI IN	Y1
Error Reporting Signals		
SERR#	PCI BI-DIR	AD11
PERR#	PCI BI-DIR	AF11
Power Management Signals		
LAN_PWR_GOOD	IN	B21
PME#	OPEN DRAIN	AA2
APM_WAKEUP	BI-DIR	P25
AUX_PWR	PCI IN	Y4
PWR_STATE1	BI-DIR	V1
PWR_STATE0	BI-DIR	V4
Impedance Compensation Signals		
ZN_COMP	IN	W1
ZP_COMP	IN	W4
TBI Interface Signals		
TBI_MODE	IN	A21
TX_DATA0	BI-DIR	A4
TX_DATA1	BI-DIR	D5
TX_DATA2	BI-DIR	C5
TX_DATA3	BI-DIR	A5

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
TX_DATA4	BI-DIR	D6
TX_DATA5	BI-DIR	B6
TX_DATA6	BI-DIR	A6
TX_DATA7	BI-DIR	D7
TX_DATA8	BI-DIR	D8
TX_DATA9	BI-DIR	A7
GTX_CLK	BI-DIR	C7
EWRAP	BI-DIR	D13
RX_DATA0	BI-DIR	A8
RX_DATA1	BI-DIR	D9
RX_DATA2	BI-DIR	B9
RX_DATA3	BI-DIR	A9
RX_DATA4	BI-DIR	D10
RX_DATA5	BI-DIR	A10
RX_DATA6	BI-DIR	C11
RX_DATA7	BI-DIR	B11
RX_DATA8	BI-DIR	C12
RX_DATA9	BI-DIR	D12
RBC0	BI-DIR	B13
RBC1	BI-DIR	A12
EEPROM/FLASH Interface Signals		
EE_DI	BI-DIR	D25
EE_DO	IN	D24
EE_CS	BI-DIR	D23
EE_SK	BI-DIR	E24
FL_ADDR0	BI-DIR	M25
FL_ADDR1	BI-DIR	K26
FL_ADDR2	BI-DIR	K24
FL_ADDR3	BI-DIR	K25
FL_ADDR4	BI-DIR	J24
FL_ADDR5	BI-DIR	H25
FL_ADDR6	BI-DIR	J23
FL_ADDR7	BI-DIR	H24
FL_ADDR8	BI-DIR	J26
FL_ADDR9	BI-DIR	G26
FL_ADDR10	BI-DIR	L26
FL_ADDR11	BI-DIR	G23
FL_ADDR12	BI-DIR	F24

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
FL_ADDR13	BI-DIR	G25
FL_ADDR14	BI-DIR	F25
FL_ADDR15	BI-DIR	E26
FL_ADDR16	BI-DIR	H26
FL_ADDR17	BI-DIR	D26
FL_ADDR18	BI-DIR	F26
FL_CS#	BI-DIR	L23
FL_OE#	BI-DIR	H23
FL_WE#	BI-DIR	F23
FL_DATA0	BI-DIR	M23
FL_DATA1	BI-DIR	N26
FL_DATA2	BI-DIR	N23
FL_DATA3	BI-DIR	P26
FL_DATA4	BI-DIR	M24
FL_DATA5	BI-DIR	N24
FL_DATA6	BI-DIR	M26
FL_DATA7	BI-DIR	L25
LED Signals		
LINK_UP#	BI-DIR	P3
RX_ACTIVITY#	BI-DIR	P1
TX_ACTIVITY#	BI-DIR	R4
LINK10#	BI-DIR	R3
LINK100#	BI-DIR	R2
LINK1000#	BI-DIR	R1
Other Signals		
LOS	IN	A14
XOFF	IN	C23
XON	IN	A23
ABV_HI	BI-DIR	C22
BLW_LO	BI-DIR	D21
SDP0	BI-DIR	G2
SDP1	BI-DIR	J1
SDP2	BI-DIR	J3
SDP3	BI-DIR	K4
SDP4	BI-DIR	K3
SDP6	BI-DIR	K2
SDP7	BI-DIR	K1
TEST0	BI-DIR	A13

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
TEST1	IN	N1
GMII_TEST0	IN	
GMII_TEST1	IN	
COL_TEST	BI-DIR	
CRS_TEST	BI-DIR	
PHY Signals		
XTAL1	IN	B4
XTAL2	OUT	C4
REF	IN	E3
MDI[0]-	BI-DIR	C1
MDI[0]+	BI-DIR	C2
MDI[1]-	BI-DIR	D1
MDI[1]+	BI-DIR	D2
MDI[2]-	BI-DIR	E1
MDI[2]+	BI-DIR	E2
MDI[3]-	BI-DIR	F1
MDI[3]+	BI-DIR	F2
Test Interface Signals		
JTAG_TCK	IN	T3
JTAG_TDI	IN	U4
JTAG_TDO	OUT	U2
JTAG_TMS	IN	U1
JTAG_TRST#	IN	T1
Digital Power Supplies		
VDDO	3.3V Power	B5
VDDO	3.3V Power	B7
VDDO	3.3V Power	B10
VDDO	3.3V Power	B17
VDDO	3.3V Power	B19
VDDO	3.3V Power	B22
VDDO	3.3V Power	E25
VDDO	3.3V Power	J25
VDDO	3.3V Power	N25
VDDO	3.3V Power	P2
VDDO	3.3V Power	T2
VDDO	3.3V Power	T25
VDDO	3.3V Power	V2
VDDO	3.3V Power	V25

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
VDDO	3.3V Power	Y2
VDDO	3.3V Power	Y25
VDDO	3.3V Power	AB2
VDDO	3.3V Power	AB25
VDDO	3.3V Power	AE5
VDDO	3.3V Power	AE7
VDDO	3.3V Power	AE9
VDDO	3.3V Power	AE11
VDDO	3.3V Power	AE13
VDDO	3.3V Power	AE15
VDDO	3.3V Power	AE17
VDDO	3.3V Power	AE19
VDDO	3.3V Power	AE21
DVDDH	1.8V Power	D4
DVDDH	1.8V Power	D14
DVDDH	1.8V Power	D19
DVDDH	1.8V Power	E23
DVDDH	1.8V Power	J4
DVDDH	1.8V Power	K10
DVDDH	1.8V Power	K11
DVDDH	1.8V Power	K16
DVDDH	1.8V Power	K17
DVDDH	1.8V Power	K23
DVDDH	1.8V Power	L10
DVDDH	1.8V Power	L17
DVDDH	1.8V Power	T4
DVDDH	1.8V Power	T10
DVDDH	1.8V Power	T17
DVDDH	1.8V Power	U10
DVDDH	1.8V Power	U11
DVDDH	1.8V Power	U16
DVDDH	1.8V Power	U17
DVDDH	1.8V Power	V23
DVDDH	1.8V Power	AC4
DVDDH	1.8V Power	AC9
DVDDH	1.8V Power	AC17
DVDDH	1.8V Power	AC23
DVDDL	1.5V Power	C10

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
DVDDL	1.5V Power	C13
DVDDL	1.5V Power	C14
DVDDL	1.5V Power	G3
Analog Power Supplies		
AVDDH	3.3V Power	A22
AVDDH	3.3V Power	D11
AVDDH	3.3V Power	G4
AVDDH	3.3V Power	AD3
AVDDL	2.5V Power	D22
AVDDL	2.5V Power	H2
AVDDL	2.5V Power	H3
AVDDL	2.5V Power	H4
Grounds and No Connects		
GND	Power	A1
GND	Power	A2
GND	Power	A3
GND	Power	A11
GND	Power	A24
GND	Power	A25
GND	Power	A26
GND	Power	B1
GND	Power	B2
GND	Power	B3
GND	Power	B8
GND	Power	B12
GND	Power	B24
GND	Power	B25
GND	Power	B26
GND	Power	C3
GND	Power	C6
GND	Power	C8
GND	Power	C9
GND	Power	C16
GND	Power	C18
GND	Power	C21
GND	Power	C24
GND	Power	C25
GND	Power	C26

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
GND	Power	D3
GND	Power	E4
GND	Power	G24
GND	Power	H1
GND	Power	K12
GND	Power	K13
GND	Power	K14
GND	Power	K15
GND	Power	L1
GND	Power	L2
GND	Power	L3
GND	Power	L11
GND	Power	L12
GND	Power	L13
GND	Power	L14
GND	Power	L15
GND	Power	L16
GND	Power	L24
GND	Power	M1
GND	Power	M3
GND	Power	M4
GND	Power	M10
GND	Power	M11
GND	Power	M12
GND	Power	M13
GND	Power	M14
GND	Power	M15
GND	Power	M16
GND	Power	M17
GND	Power	N3
GND	Power	N4
GND	Power	N10
GND	Power	N11
GND	Power	N12
GND	Power	N13
GND	Power	N14
GND	Power	N15
GND	Power	N16

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
GND	Power	N17
GND	Power	P4
GND	Power	P10
GND	Power	P11
GND	Power	P12
GND	Power	P13
GND	Power	P14
GND	Power	P15
GND	Power	P16
GND	Power	P17
GND	Power	R10
GND	Power	R11
GND	Power	R12
GND	Power	R13
GND	Power	R14
GND	Power	R15
GND	Power	R16
GND	Power	R17
GND	Power	R24
GND	Power	T11
GND	Power	T12
GND	Power	T13
GND	Power	T14
GND	Power	T15
GND	Power	T16
GND	Power	U3
GND	Power	U12
GND	Power	U13
GND	Power	U14
GND	Power	U15
GND	Power	U24
GND	Power	W3
GND	Power	W24
GND	Power	AA3
GND	Power	AA24
GND	Power	AD1
GND	Power	AD2
GND	Power	AD4

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
GND	Power	AD6
GND	Power	AD8
GND	Power	AD10
GND	Power	AD12
GND	Power	AD14
GND	Power	AD16
GND	Power	AD18
GND	Power	AD20
GND	Power	AD22
GND	Power	AD24
GND	Power	AD25
GND	Power	AD26
GND	Power	AE1
GND	Power	AE2
GND	Power	AE3
GND	Power	AE23
GND	Power	AE24
GND	Power	AE25
GND	Power	AE26
GND	Power	AF1
GND	Power	AF2
GND	Power	AF25
GND	Power	AF26
NO_CONNECT		A15
NO_CONNECT		A16
NO_CONNECT		A17
NO_CONNECT		A18
NO_CONNECT		A19
NO_CONNECT		A20
NO_CONNECT		B14
NO_CONNECT		B15
NO_CONNECT		B16
NO_CONNECT		B18
NO_CONNECT		B20
NO_CONNECT		B23
NO_CONNECT		C15
NO_CONNECT		C17
NO_CONNECT		C19

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
NO_CONNECT		C20
NO_CONNECT		D15
NO_CONNECT		D16
NO_CONNECT		D17
NO_CONNECT		D18
NO_CONNECT		D20
NO_CONNECT		F3
NO_CONNECT		F4
NO_CONNECT		G1
NO_CONNECT		J2
NO_CONNECT		L4
NO-CONNECT		M2
NO_CONNECT		N1
NO_CONNECT		N2
NO_CONNECT		V3
NO_CONNECT		AC26
NO_CONNECT		AE22
NO_CONNECT		AF22
NO_CONNECT		AF23