intel®

PRELIMINARY

82437MX SYSTEM CONTROLLER (MTSC) AND 82438MX DATA PATH UNIT (MTDP)

SmartDie™ Product Specification

- **Supports the Pentium® Processor at iCOMP® Index 1110/133, 1000/120, 815/100, 735/90, and 610/75 MHz**
- **Integrated Second Level Cache Controller**
  - **Direct Mapped Organization**
  - **Write-Back Cache Policy**
  - **Cacheless, 256 Kbytes, and 512 Kbytes**
  - **Standard, Burst and Pipelined Burst SRAMs**
  - **Cache Hit Read/Write Cycle Timings at 3-1-1-1 with Burst or Pipelined Burst SRAMs**
  - **Back-to-Back Read Cycles at 3-1-1-1-1-1-1-1 with Burst or Pipelined Burst SRAMs**
  - **Integrated Tag/Valid Status Bits for Cost Savings and Performance**
  - **Supports 3.3 V SRAMs and Tag Address**
- **Integrated DRAM Controller**
  - **64-Bit Data Path to Memory**
  - **4-Mbyte to 128-Mbytes Main Memory**
  - **EDO/Hyper Page Mode DRAM (x-2-2-2 Reads) Provides Superior Cacheless Designs**
  - **Standard Page Mode DRAMs**
  - **4 RAS Lines**
  - **4 Qword Deep Buffer for 3-1-1-1 Posted Write Cycles**
  - **Symmetrical and Asymmetrical DRAMs**
  - **3 V or 5 V DRAMs**
- **Power Management**
  - **DRAM Refresh During Suspend**
  - **Self Refresh and Extended Refresh**
- **Fully Synchronous 25/30/33 MHz PCI Bus Interface**
  - **100 Mbytes/s Instant Access Enables Native Signal Processing on Pentium Processors**
  - **Synchronized CPU-to-PCI Interface for High Performance Graphics**
  - **PCI Bus Arbiter: MPIIX and Three PCI Bus Masters Supported**
  - **CPU-to-PCI Memory Write Posting with 4 Dword Deep Buffers**
  - **Converts Back-to-Back Sequential CPU to PCI Memory Writes to PCI Burst Writes**
  - **PCI-to-DRAM Posting of 12 Dwords**
  - **PCI-to-DRAM up to 120 Mbytes/s Bandwidth Utilizing Snoop Ahead Feature**
- **NAND Tree for Board-Level ATE Testing**
- **Intel SmartDie™ Product**
  - **Full AC/DC Testing at Die Level**
  - **0° C to 105° C (Junction) Temperature Range**

NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in "DEVICE NOMENCLATURE" on page 17. This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest product specification before finalizing a design.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet on a specific product. Please refer to the standard package datasheet (order number 290524) for product information and specifications not found in this document.

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82437MX SYSTEM CONTROLLER (MTSC) AND 82438MX DATA PATH UNIT (MTDP)

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1.0 DIE SPECIFICATIONS

The die photos (below and next page) and the plots on pages 3 and 4 indicate the orientation of the die in the GEL-PAK* (shipping container). Die are aligned as shown relative to a 45° notch which is in one corner of the GEL-PAK. An Intel internal manufacturing name "82437MX" appears on the MTSC die. An Intel internal manufacturing name "82438MX" appears on the MTDP die. Tables 1 and 2 describe the bond pad number and pad center data for each signal.

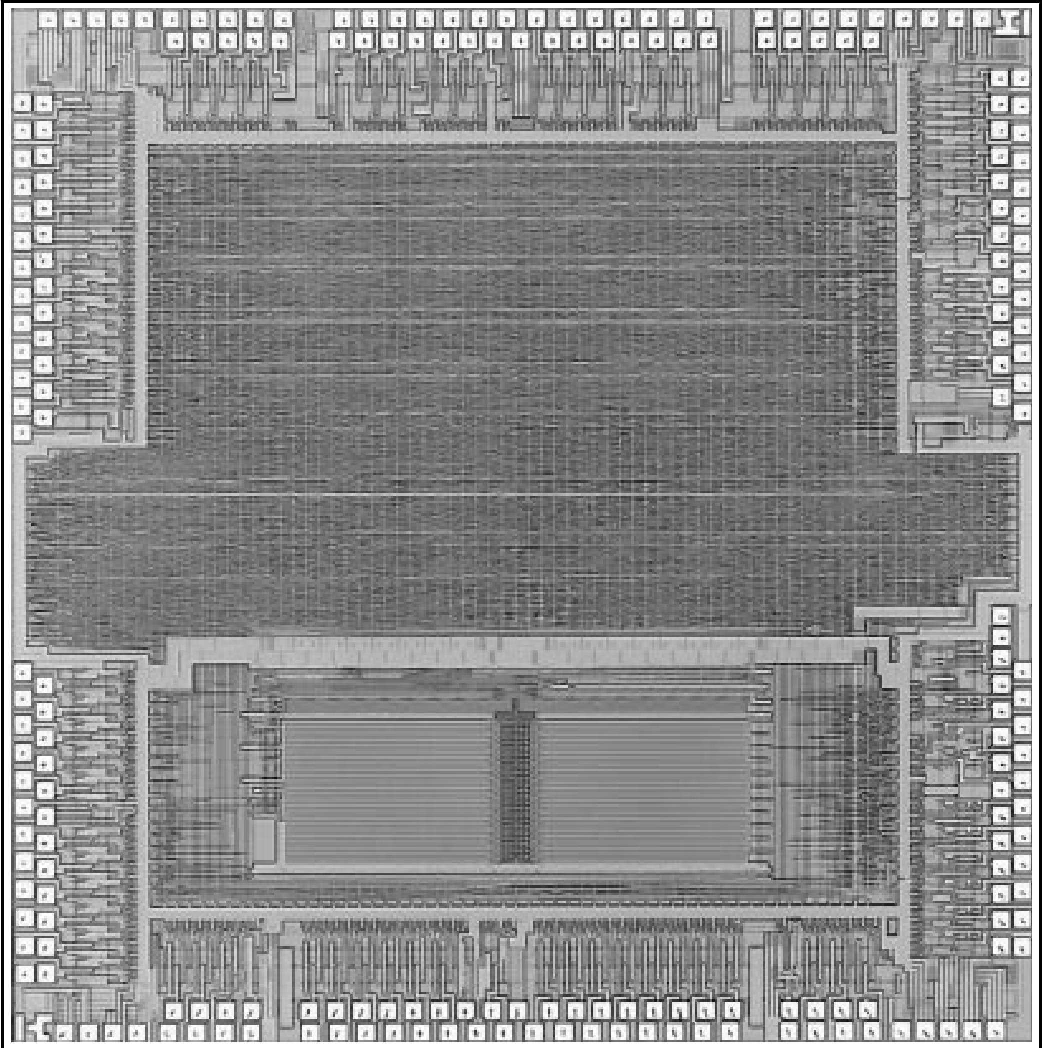

Figure 1. 82437MX System Controller Die Photo

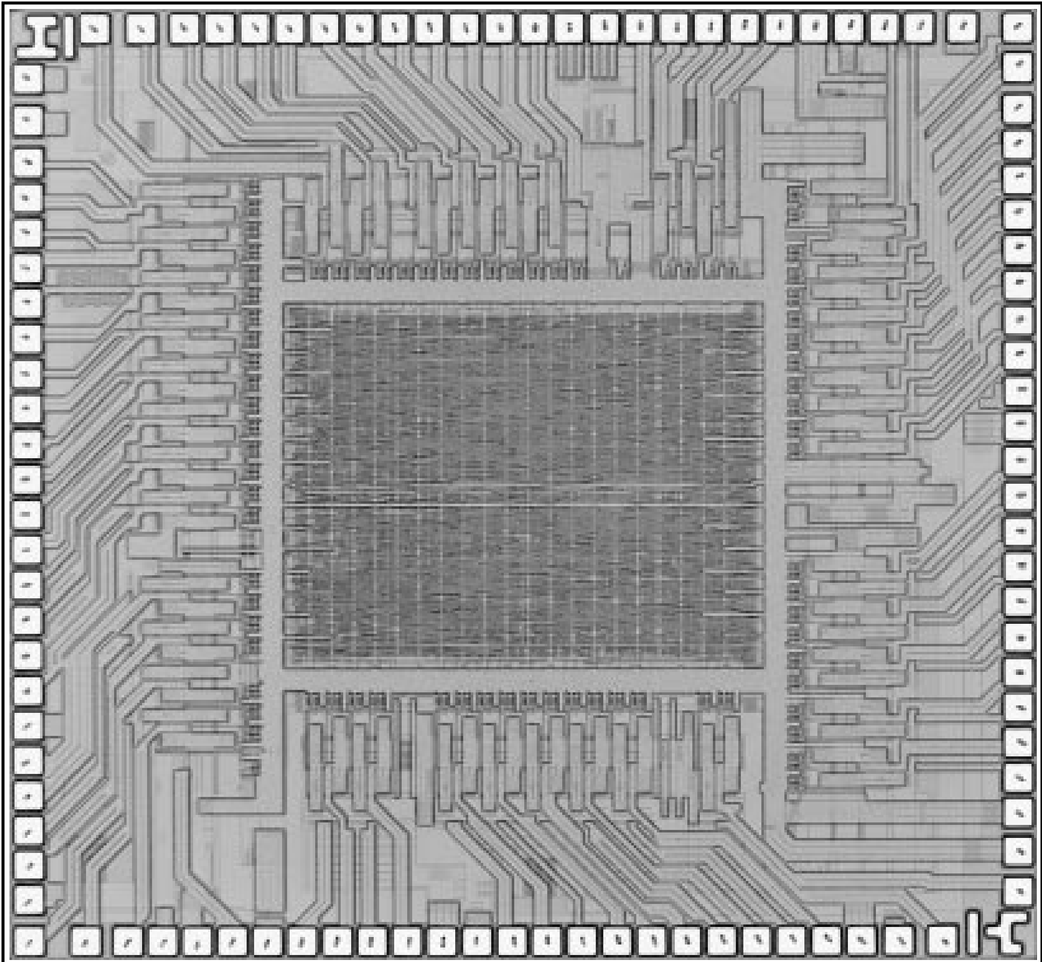

Figure 2. 82438MX Data Path Die Photo

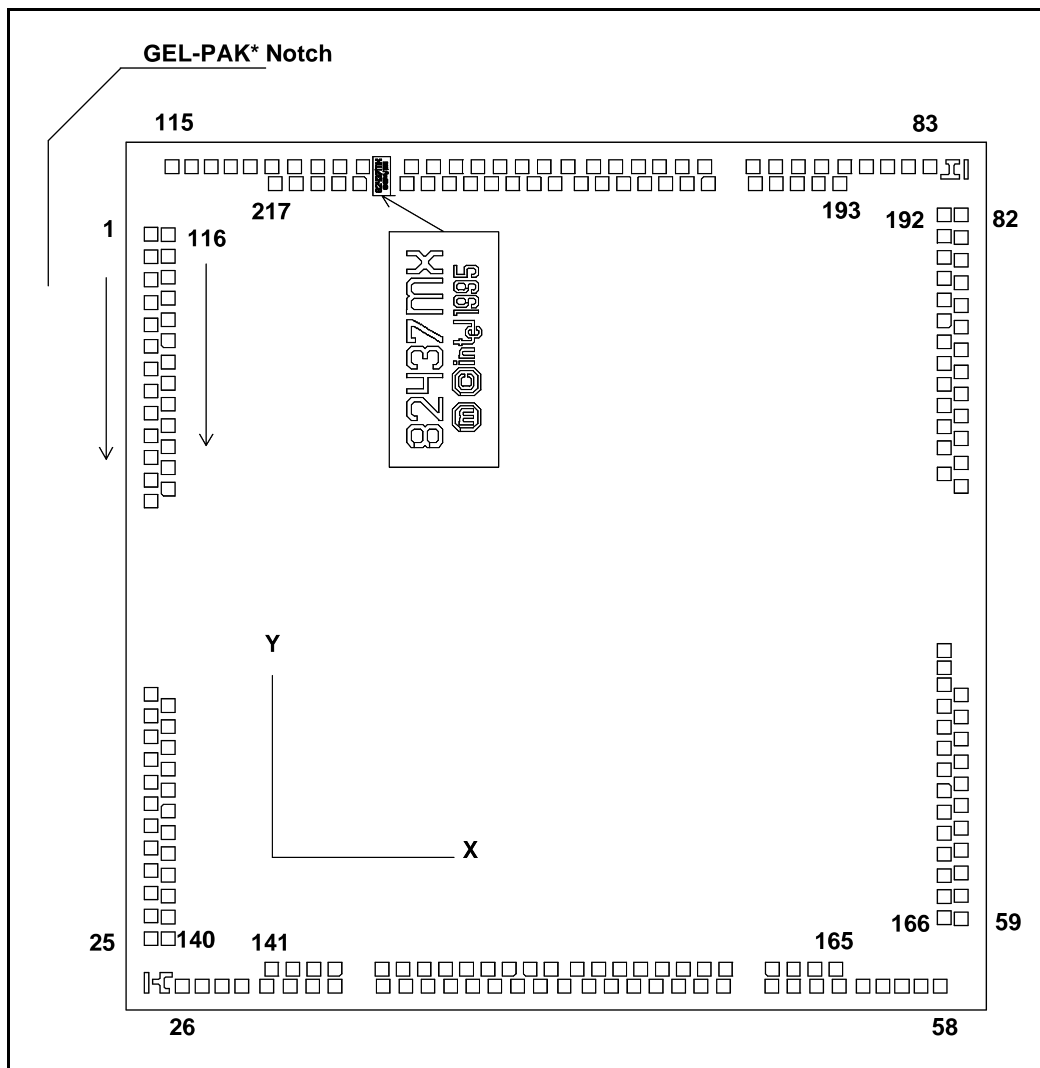

Figure 3. 82437MX System Controller Die/Bond Pad Layout

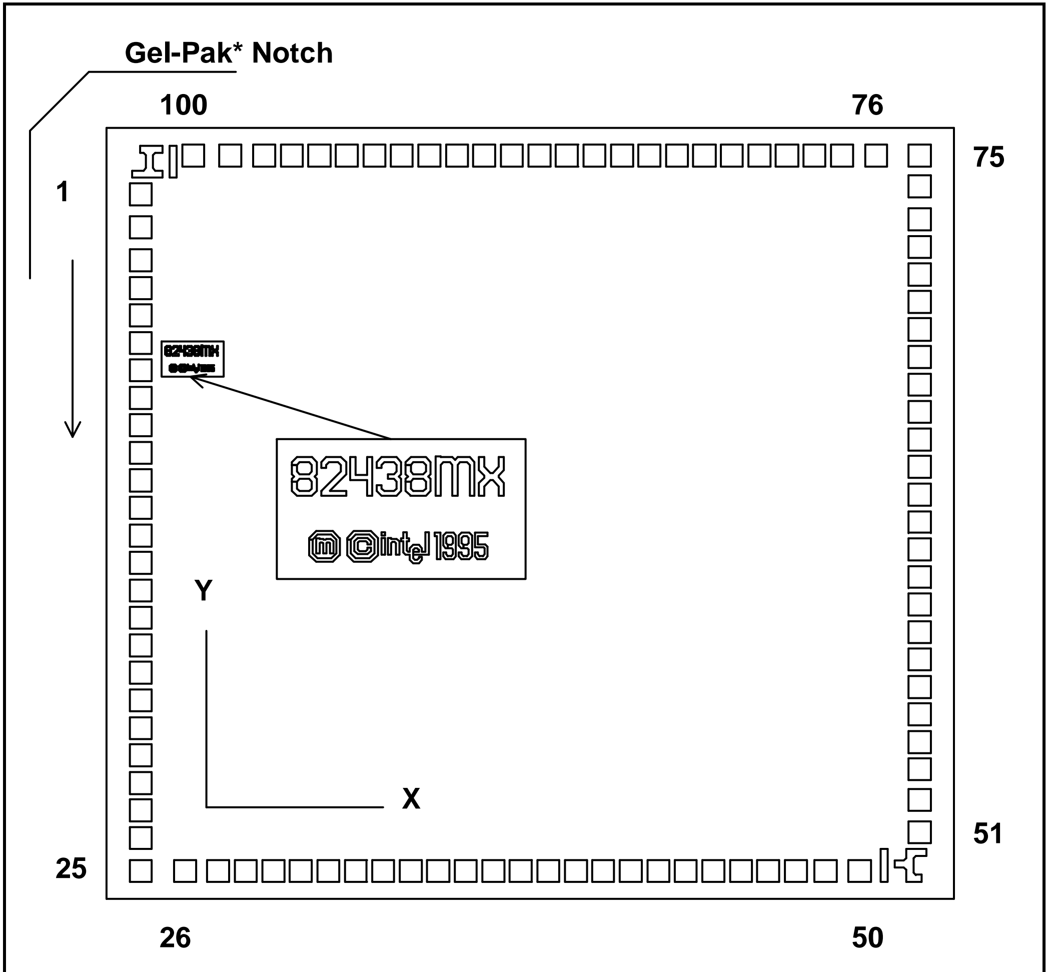

Figure 4. 82438MX Data Path Die/Bond Pad Layout

Table 1. 82437MX System Controller Bond Pad Center Data (Sheet 1 of 7)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
001	TIO0	-111.7	94.3	-2837	2395
002	TIO2	-111.7	88.0	-2837	2236
003	TIO6	-111.7	81.7	-2837	2075
004	TIO4	-111.7	75.4	-2837	1916
005	TWE#	-111.7	69.3	-2837	1760
006	VSS	-111.7	63.3	-2837	1608
007	COE#	-111.7	57.2	-2837	1452
008	CWE5#	-111.7	51.0	-2837	1294
009	CWE7#	-111.7	44.9	-2837	1141
010	CWE1#	-111.7	38.7	-2837	984
011	CWE3#	-111.7	32.7	-2837	831
012	A23	-111.7	26.5	-2837	673
013	VCC3	-111.7	20.7	-2837	525
014	A21	-111.7	-32.6	-2837	-827
015	A27	-111.7	-38.4	-2837	-975
016	A26	-111.7	-44.2	-2837	-1123
017	A28	-111.7	-50.4	-2837	-1281
018	A3	-111.7	-56.6	-2837	-1439
019	VSS	-111.7	-62.7	-2837	-1592
020	A4	-111.7	-68.7	-2837	-1745
021	A6	-111.7	-74.8	-2837	-1899
022	A8	-111.7	-81.0	-2837	-2057
023	A10	-111.7	-87.2	-2837	-2216
024	A17	-111.7	-93.5	-2837	-2375
025	A19	-111.7	-99.7	-2837	-2533
026	VCC3	-103.0	-112.9	-2617	-2867
027	VSS	-97.6	-112.9	-2478	-2867
028	VSS	-92.1	-112.9	-2339	-2867
029	VCC5	-86.6	-112.9	-2200	-2867
030	A12	-79.7	-112.9	-2025	-2867
031	A13	-73.4	-112.9	-1863	-2867
032	HLOCK#	-67.1	-112.9	-1703	-2867

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 1. 82437MX System Controller Bond Pad Center Data (Sheet 2 of 7)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
033	VSS	-61.0	-112.9	-1550	-2867
034	KEN#	-47.7	-112.9	-1213	-2867
035	BRDY#	-41.5	-112.9	-1054	-2867
036	BOFF#	-35.3	-112.9	-896	-2867
037	ADS#	-29.1	-112.9	-740	-2867
038	HITM#	-23.0	-112.9	-584	-2867
039	SMIACT#	-16.8	-112.9	-427	-2867
040	VCC5	-10.6	-112.9	-268	-2867
041	PCIRST#	-4.4	-112.9	-111	-2867
042	BE1#	2.3	-112.9	57	-2867
043	BE3#	9.0	-112.9	229	-2867
044	BE5#	15.2	-112.9	386	-2867
045	BE7#	21.4	-112.9	543	-2867
046	PLINK1	27.6	-112.9	701	-2867
047	PLINK3	33.8	-112.9	857	-2867
048	PLINK5	39.9	-112.9	1014	-2867
049	PLINK7	46.2	-112.9	1173	-2867
050	VSS	59.4	-112.9	1509	-2867
051	PLINK10	65.5	-112.9	1663	-2867
052	PLINK12	71.8	-112.9	1823	-2867
053	PLINK14	78.1	-112.9	1983	-2867
054	PCMD0	84.6	-112.9	2148	-2867
055	VCC5	90.0	-112.9	2286	-2867
056	VSS	95.3	-112.9	2420	-2867
057	VSS	100.6	-112.9	2554	-2867
058	VCC3	105.8	-112.9	2688	-2867
059	MSTB#	111.7	-94.3	2837	-2395
060	HOE#	111.7	-88.0	2837	-2236
061	MOE#	111.7	-81.7	2837	-2076
062	MA0	111.7	-75.5	2837	-1916
063	MA2	111.7	-69.3	2837	-1761
064	MA4	111.7	-63.0	2837	-1601

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol "#" is used to denote active low signals.

Table 1. 82437MX System Controller Bond Pad Center Data (Sheet 3 of 7)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
065	VSS	111.7	-57.1	2837	-1451
066	MA7	111.7	-51.0	2837	-1296
067	VCCM	111.7	-44.9	2837	-1139
068	MA10	111.7	-38.8	2837	-985
069	VCCR	111.7	-32.7	2837	-830
070	RTCCLK	111.7	24.8	2837	630
071	RAS2#	111.7	31.3	2837	795
072	RAS0#	111.7	38.0	2837	965
073	CAS7#	111.7	44.1	2837	1120
074	CAS5#	111.7	50.2	2837	1275
075	VCCM	111.7	56.3	2837	1429
076	CAS0#	111.7	62.4	2837	1585
077	VSS	111.7	68.6	2837	1742
078	CLKRUN#	111.7	74.6	2837	1896
079	REQ2#	111.7	80.8	2837	2051
080	REQ1#	111.7	87.0	2837	2210
081	REQ0#	111.7	93.3	2837	2370
082	PHLD#	111.7	99.6	2837	2529
083	VCC5	103.0	112.9	2617	2867
084	VSS	97.2	112.9	2468	2867
085	VSS	91.3	112.9	2320	2867
086	VCC5	85.5	112.9	2172	2867
087	AD30	79.5	112.9	2020	2867
088	AD28	73.2	112.9	1859	2867
089	AD26	66.8	112.9	1698	2867
090	AD24	60.6	112.9	1538	2867
091	AD23	54.3	112.9	1379	2867
092	VCC5	41.0	112.9	1041	2867
093	AD21	34.7	112.9	882	2867
094	AD19	28.5	112.9	724	2867
095	VSS	22.6	112.9	574	2867
096	AD16	16.5	112.9	418	2867

NOTES:
1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 1. 82437MX System Controller Bond Pad Center Data (Sheet 4 of 7)

PAD#	SIGNAL(2,3)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
097	FRAME#	10.4	112.9	263	2867
098	TRDY#	3.3	112.9	84	2867
099	VCC5	-3.3	112.9	-84	2867
100	STOP#	-9.3	112.9	-237	2867
101	PAR	-15.5	112.9	-395	2867
102	VSS	-21.6	112.9	-548	2867
103	AD14	-27.6	112.9	-701	2867
104	AD12	-33.8	112.9	-858	2867
105	AD10	-39.9	112.9	-1013	2867
106	VCC5	-53.2	112.9	-1353	2867
107	AD8	-59.5	112.9	-1512	2867
108	AD7	-65.7	112.9	-1670	2867
109	AD5	-72.1	112.9	-1830	2867
110	AD3	-78.4	112.9	-1991	2867
111	AD1	-84.3	112.9	-2142	2867
112	VCC5	-89.7	112.9	-2278	2867
113	VSS	-95.1	112.9	-2415	2867
114	VSS	-100.4	112.9	-2551	2867
115	VCC5	-105.8	112.9	-2688	2867
116	AD0	-107.0	94.0	-2718	2389
117	TIO1	-107.0	88.2	-2718	2240
118	TIO7	-107.0	82.4	-2718	2092
119	TIO5	-107.0	76.5	-2718	1944
120	TIO3	-107.0	70.7	-2718	1796
121	CADV#/CA4	-107.0	64.9	-2718	1648
122	CADS#/CA3	-107.0	59.0	-2718	1499
123	CWE4#	-107.0	53.2	-2718	1351
124	CWE6#	-107.0	47.4	-2718	1203
125	CWE0#	-107.0	41.5	-2718	1055
126	CWE2#	-107.0	35.7	-2718	907
127	CCS#	-107.0	29.9	-2718	758
128	VSS	-107.0	24.0	-2718	610

NOTES:
1. X-Y coordinates represent pad centers and are relative to center of die.
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3. The symbol "#" is used to denote active low signals.

Table 1. 82437MX System Controller Bond Pad Center Data (Sheet 5 of 7)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
129	A24	-107.0	-35.5	-2718	-903
130	A22	-107.0	-41.4	-2718	-1051
131	A25	-107.0	-47.2	-2718	-1199
132	A31	-107.0	-53.0	-2718	-1347
133	A30	-107.0	-58.9	-2718	-1496
134	A29	-107.0	-64.7	-2718	-1644
135	A7	-107.0	-70.6	-2718	-1792
136	A5	-107.0	-76.4	-2718	-1940
137	A11	-107.0	-82.2	-2718	-2088
138	A16	-107.0	-88.1	-2718	-2237
139	A18	-107.0	-93.9	-2718	-2385
140	A20	-107.0	-99.7	-2718	-2533
141	A9	-78.4	-108.2	-1992	-2749
142	A14	-72.6	-108.2	-1843	-2749
143	A15	-66.7	-108.2	-1695	-2749
144	M/IO#	-60.9	-108.2	-1547	-2749
145	CACHE#	-48.0	-108.2	-1219	-2749
146	AHOLD	-42.2	-108.2	-1071	-2749
147	NA#	-36.3	-108.2	-923	-2749
148	EADS#	-30.5	-108.2	-775	-2749
149	D/C#	-24.7	-108.2	-626	-2749
150	W/R#	-18.8	-108.2	-478	-2749
151	BE0#	-13.0	-108.2	-330	-2749
152	HCLKIN	-7.2	-108.2	-182	-2749
153	VSS	-1.4	-108.2	-35	-2749
154	BE2#	5.9	-108.2	149	-2749
155	BE4#	11.7	-108.2	297	-2749
156	BE6#	17.5	-108.2	445	-2749
157	PLINK0	23.4	-108.2	593	-2749
158	PLINK2	29.2	-108.2	741	-2749
159	PLINK4	35.0	-108.2	890	-2749
160	PLINK6	40.9	-108.2	1038	-2749

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol "#" is used to denote active low signals.

Table 1. 82437MX System Controller Bond Pad Center Data (Sheet 6 of 7)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
161	PLINK8	46.7	-108.2	1186	-2749
162	PLINK9	59.6	-108.2	1514	-2749
163	PLINK11	65.4	-108.2	1662	-2749
164	PLINK13	71.3	-108.2	1810	-2749
165	PLINK15	77.1	-108.2	1958	-2749
166	PCMD1	107.0	-94.1	2718	-2390
167	MADV#	107.0	-88.2	2718	-2241
168	POE#	107.0	-82.4	2718	-2093
169	DWE#	107.0	-76.6	2718	-1945
170	MA1	107.0	-70.7	2718	-1797
171	MA3	107.0	-64.9	2718	-1649
172	MA5	107.0	-59.1	2718	-1500
173	MA6	107.0	-53.2	2718	-1352
174	MA8	107.0	-47.4	2718	-1204
175	MA9	107.0	-41.6	2718	-1056
176	MA11	107.0	-35.7	2718	-908
177	PWROK	107.0	-29.9	2718	-759
178	PWRSD	107.0	-25.2	2718	-640
179	VSS	107.0	-20.5	2718	-521
180	VSS	107.0	28.2	2718	716
181	RAS3#	107.0	35.4	2718	898
182	RAS1#	107.0	41.2	2718	1046
183	CAS3#	107.0	47.0	2718	1195
184	CAS1#	107.0	52.9	2718	1343
185	CAS4#	107.0	58.7	2718	1491
186	CAS6#	107.0	64.5	2718	1639
187	CAS2#	107.0	70.4	2718	1787
188	GNT2#	107.0	76.2	2718	1936
189	GNT1#	107.0	82.0	2718	2084
190	GNT0#	107.0	87.9	2718	2232
191	PHLDA#	107.0	93.7	2718	2380
192	PCLKIN	107.0	99.5	2718	2528

NOTES:
1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 1. 82437MX System Controller Bond Pad Center Data (Sheet 7 of 7)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
193	AD31	78.2	108.2	1986	2749
194	AD29	72.3	108.2	1838	2749
195	AD27	66.5	108.2	1689	2749
196	AD25	60.7	108.2	1541	2749
197	C/BE3#	54.8	108.2	1393	2749
198	VSS	41.9	108.2	1064	2749
199	AD22	36.1	108.2	916	2749
200	AD20	30.2	108.2	768	2749
201	AD18	24.4	108.2	620	2749
202	AD17	18.6	108.2	471	2749
203	C/BE2#	12.7	108.2	323	2749
204	IRDY#	6.9	108.2	175	2749
205	VSS	-0.3	108.2	-7	2749
206	DEVSEL#	-6.1	108.2	-156	2749
207	LOCK#	-12.0	108.2	-304	2749
208	C/BE1#	-17.8	108.2	-452	2749
209	AD15	-23.6	108.2	-600	2749
210	AD13	-29.5	108.2	-748	2749
211	AD11	-35.3	108.2	-897	2749
212	VSS	-41.1	108.2	-1045	2749
213	AD9	-54.1	108.2	-1373	2749
214	C/BE0#	-59.9	108.2	-1522	2749
215	AD6	-65.7	108.2	-1670	2749
216	AD4	-71.6	108.2	-1818	2749
217	AD2	-77.4	108.2	-1966	2749

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 2. 82438MX Data Path Bond Pad Center Data (Sheet 1 of 3)

PAD#	SIGNAL(2,3)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
001	VSS	-66.2	54.2	-1682	1377
002	VCC3	-66.2	48.6	-1682	1235
003	HD5	-66.2	43.0	-1682	1092
004	HD6	-66.2	38.3	-1682	973
005	HD7	-66.2	33.6	-1682	855
006	HD8	-66.2	29.0	-1682	736
007	HD9	-66.2	24.3	-1682	617
008	HD10	-66.2	19.6	-1682	498
009	HD11	-66.2	14.9	-1682	380
010	HD12	-66.2	10.3	-1682	261
011	HD13	-66.2	5.6	-1682	142
012	HD14	-66.2	0.9	-1682	23
013	HD15	-66.2	-3.8	-1682	-95
014	HD16	-66.2	-8.4	-1682	-214
015	HD17	-66.2	-13.1	-1682	-333
016	HD18	-66.2	-17.8	-1682	-452
017	HD19	-66.2	-22.5	-1682	-570
018	HD20	-66.2	-27.1	-1682	-689
019	VSS	-66.2	-31.8	-1682	-808
020	HD21	-66.2	-36.5	-1682	-927
021	HD22	-66.2	-41.2	-1682	-1045
022	HD23	-66.2	-45.8	-1682	-1164
023	HD24	-66.2	-50.5	-1682	-1283
024	VCC3	-66.2	-55.2	-1682	-1402
025	HD25	-66.2	-60.8	-1682	-1544
026	HD26	-58.6	-60.8	-1489	-1544
027	HD27	-53.0	-60.8	-1347	-1544
028	VSS	-48.3	-60.8	-1228	-1544
029	VCC5	-43.7	-60.8	-1109	-1544
030	HCLK	-39.0	-60.8	-990	-1544
031	VSS	-34.3	-60.8	-872	-1544
032	HD28	-29.6	-60.8	-753	-1544
033	HD29	-25.0	-60.8	-634	-1544

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 2. 82438MX Data Path Bond Pad Center Data (Sheet 2 of 3)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
034	HD30	-20.3	-60.8	-516	-1544
035	HD31	-15.6	-60.8	-397	-1544
036	VCC3	-10.9	-60.8	-278	-1544
037	VSS	-6.3	-60.8	-159	-1544
038	MD24	-1.6	-60.8	-41	-1544
039	MD8	3.1	-60.8	78	-1544
040	MD16	7.8	-60.8	197	-1544
041	MD0	12.4	-60.8	316	-1544
042	MD25	17.1	-60.8	435	-1544
043	MD9	21.8	-60.8	553	-1544
044	MD17	26.5	-60.8	672	-1544
045	MD1	31.1	-60.8	791	-1544
046	MD26	35.8	-60.8	910	-1544
047	MD10	40.5	-60.8	1028	-1544
048	VCCM	45.2	-60.8	1147	-1544
049	VSS	50.2	-60.8	1275	-1544
050	MD18	56.0	-60.8	1423	-1544
051	MD2	66.2	-54.2	1682	-1378
052	VCC5	66.2	-48.8	1682	-1239
053	VSS	66.2	-43.6	1682	-1106
054	MD27	66.2	-38.9	1682	-988
055	MD11	66.2	-34.2	1682	-869
056	MD19	66.2	-29.5	1682	-750
057	MD3	66.2	-24.9	1682	-631
058	MD28	66.2	-20.2	1682	-513
059	MD12	66.2	-15.5	1682	-394
060	MD20	66.2	-10.8	1682	-275
061	MD4	66.2	-6.2	1682	-156
062	MD21	66.2	-1.5	1682	-38
063	MD5	66.2	3.2	1682	81
064	VCCM	66.2	7.9	1682	200
065	VSS	66.2	12.5	1682	319
066	MD29	66.2	17.2	1682	437
067	MD13	66.2	21.9	1682	556

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 2. 82438MX Data Path Bond Pad Center Data (Sheet 3 of 3)

PAD#	SIGNAL(2,3)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
068	MD22	66.2	26.6	1682	675
069	MD6	66.2	31.2	1682	794
070	MD30	66.2	35.9	1682	912
071	MD14	66.2	40.6	1682	1031
072	MD23	66.2	45.3	1682	1150
073	MD7	66.2	49.9	1682	1269
074	MD31	66.2	55.6	1682	1411
075	MD15	66.2	60.8	1682	1544
076	VCCM	58.8	60.8	1493	1544
077	MOE#	53.0	60.8	1346	1544
078	POE#	48.3	60.8	1227	1544
079	VCC3	43.6	60.8	1109	1544
080	VSS	39.0	60.8	990	1544
081	HOE#	34.3	60.8	871	1544
082	MADV#	29.6	60.8	752	1544
083	MSTB#	24.9	60.8	634	1544
084	PCMD1	20.3	60.8	515	1544
085	PCMD0	15.6	60.8	396	1544
086	VCC5	10.9	60.8	277	1544
087	VSS	6.2	60.8	159	1544
088	PLINK7	1.6	60.8	40	1544
089	PLINK6	-3.1	60.8	-79	1544
090	PLINK5	-7.8	60.8	-198	1544
091	PLINK4	-12.5	60.8	-316	1544
092	PLINK3	-17.1	60.8	-435	1544
093	PLINK2	-21.8	60.8	-554	1544
094	PLINK1	-26.5	60.8	-673	1544
095	PLINK0	-31.2	60.8	-791	1544
096	HD0	-35.8	60.8	-910	1544
097	HD1	-40.5	60.8	-1029	1544
098	HD2	-45.2	60.8	-1148	1544
099	HD3	-51.0	60.8	-1295	1544
100	HD4	-57.3	60.8	-1456	1544

NOTES:
1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

2.0 INTEL DIE PRODUCTS PROCESSING

2.1 Test Procedure

Intel has instituted full-speed functional testing at the die level for all SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

2.2 Wafer Probe

Wafer probing is performed on every wafer produced in Intel Fabs. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

2.3 Wafer Saw

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts totally through the wafer.

2.4 Die Inspection

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

2.5 Packing Procedure

Intel will ship all Intel die products in GEL-PAKs. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel SmartDie
- Intel Part Number
- Assembly Process Order / Spec
- ROM Code (if applicable)
- Customer Part Number (if applicable)
- Assembly Lot Traveler Number
- Finished Product Order Number
- Quantity
- Seal Date
- Country of Origin

NOTE:

GEL-PAKs require a Vacuum Release Station. Contact Vichem* Corporation for more information.

2.6 Inspection Steps

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

2.7 Storage Requirements

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

2.8 Electro-Static Discharge (ESD)

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Physical Specifications

Table 3 defines 82437MX System Controller physical specifications. Table 4 defines 82438MX Data Path physical specifications.

Table 3. 82437MX System Controller Physical Specifications

Die Revision:	B-0
Post-Saw Die Dimensions:	Mils: X = 236 ± 0.5, Y = 238 ± 0.5 See associated Die/Bond Pad Layout for X, Y orientation.
Die Thickness:	17 ± 1 mils
Minimum Pad Pitch:	118.8 microns (4.7 mils)
Pad Passivation Opening Size:	Mils: 3.7 x 3.7 (single pads) Microns: 95 x 95 (single pads)
Bond Pad Metallization: (outermost layer first)	1 micron Aluminum (0.5% Copper), 0.1 microns Titanium
Pads per Die:	217
Die Backside Material: (outermost layer first)	1500 (+/-) 500 angstroms Gold, 200 (+/-) 100 angstroms Chrome
Passivation: (outermost layer first)	5 microns Polyimide, 0.6 microns Nitride
Intel Fabrication Process:	CHMOSV (min. feature size 0.8 microns)

Table 4. 82438MX Data Path Physical Specifications

Die Revision:	A-1
Post-Saw Die Dimensions:	Mils: X = 145 ± 0.5, Y = 134 ± 0.5 See associated Die/Bond Pad Layout for X, Y orientation.
Die Thickness:	17 ± 1 mils
Minimum Pad Pitch:	118.8 microns (4.7 mils)
Pad Passivation Opening Size:	Mils: 3.7 x 3.7 (single pads) Microns: 95 x 95 (single pads)
Bond Pad Metallization: (outermost layer first)	1 micron Aluminum (0.5% Copper), 0.1 microns Titanium
Pads per Die:	100
Die Backside Material: (outermost layer first)	Polished bare silicon
Passivation: (outermost layer first)	5 microns Polyimide, 0.6 microns Nitride
Intel Fabrication Process:	CHMOSV (min. feature size 0.8 microns)

3.2 DC Specifications

ABSOLUTE MAXIMUM RATINGS†

GEL-PAK Storage Temperature .... 0°C to +70°C
Junction Temperature Under Bias .... -65°C to +110°C

OPERATING CONDITIONS†

T_J (Junction Temperature Under Bias) .... 0°C to +105°C
Substrate Bias ....Float (Self Biasing to V_{SS}),
.... Alternative is to Drive V_{SS}
Core Operating Frequency .... 60, 66 MHz

NOTICE: This datasheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

† ***WARNING:*** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.0 DEVICE NOMENCLATURE

X	8	2	4	3	7	M	X	6	6

Package Type
X = Die
Base Product Number
Bus Speed
(MHz)

VALID COMBINATIONS:
X82437MX60
X82437MX66

X	8	2	4	3	8	M	X	6	6

Package Type
X = Die
Base Product Number
Bus Speed
(MHz)

VALID COMBINATIONS:
X82438MX60
X82438MX66

NOTE: The 430MX PCIset consists of the 82437MX System Controller (MTSC), two 82438MX Data Paths (MTDP), and the 82371MX PCI I/O IDE Xcelerator (MPIIX).

5.0 REFERENCE INFORMATION

Document Title	Order #
Intel430MX PCIset (82437MX, 82438MX) Datasheet	290524
Intel430MX PCIset (82371MX) Datasheet	290525

6.0 REVISION HISTORY

Revision	Date	Description
001	6/96	Initial Release