6202 Data Book

PCI True-Color Graphics Accelerator

Preliminary

Ver. 1.0

December 1994

SiS 6202

PCI True-Color

Graphics Accelerator

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1. SiS 6202 OVERVIEW

1.1 Introduction

SiS has created a completely new design for the SiS 6202, which based on a new generation of advanced architecture and local bus standard, added with the characteristics of high performance, high integration, and low cost solution to form a PCI True-Color Graphics Accelerator.

1.2 Features

PCI Bus Interface

- Support 32-bit PCI Local Bus Standard Revision 2.0
- Support PCI Bus-Master Architecture
- Support PCI Burst Write
- Support PCI Multi-Function Device
- Follow the One-Load-Per-Slot PCI Specification

Performance

- Support PCI Bus-Master Architecture to Achieve Extra-High Performance
- Built-in an Enhanced 32-bit BITBLT Graphic Engine with following functions:
  - 256 Raster Operation Functions
  - Rectangle Fill
  - Color/Font Expansion
  - Enhanced Color/Font expansion
  - Line-Drawing with Styled Pattern
  - Built-in 8x8 Pattern Registers
  - Built-in 8x8 Mask Registers
  - 24 Doublewords Command Queue
- Built-in 64x64x2 Bit-Mapped Hardware Cursor
- Built-in 4 Stages CPU Write-Buffer and 128 Bits Read-ahead Cache to Minimize CPU Wait-state
- Built-in 32x24 CRT FIFOs to Support Super High Resolution Graphic Modes and Reduce CPU Wait-State
- Memory-Mapped I/O to Reduce I/O Trapping Overhead Under Protected Mode
- Support Linear Addressing Mode up to 4MByte to Speed Up Graphic Performance

Integration

- Built-in Programmable 24-bit True-Color RAMDAC with Reference-Voltage Generator
- Built-in Monitor-Sense Circuit
- Built-in Feature Connector Logic
- Built-in Dual-Clock Generator
- External Dual-Clock Generator Option Available

Display Memory Interface

- 32-bit Interleaved Video Memory Data Bus Architecture up to 4 banks with 240 MByte/sec Peak Memory Bandwidth
- Support 256Kx4, 256Kx8, and 256Kx16 DRAM Types
- Support 1MB, 2MB and 4MB DRAM Configuration
- Support Auto Memory Size Detecting and Auto Bank Switching
- Support 2-CAS/1-WE and 2-WE/1-CAS 256Kx16 DRAM Types

Resolution, Color & Frame Rate

- Support Super High Resolution Graphic Modes
  - 640x480 256/32K/64K/16M colors NI
  - 800x600 16/256/32K/64K/16M colors NI
  - 1024x768 16/256/32K/64K colors NI, 16M colors interlace only
  - 1280x1024 16/256 colors NI, 32K/64K colors interlace only
- Support Virtual Screen Up to 2048x2048
- Support 80/132 Columns Text Mode in 25, 30, 44 or 60 Rows and other modes
- Support 75Hz Vertical Refresh Rate

Power Management

- Support VESA DPMS Compliant VGA Monitor for Power Management
- Built-in 30 min. Standby and Suspend Timers with Keyboard, Hardware Cursor and/or Video Memory Read/Write as Activation Source
- Support Direct I/O Command to Force Graphics Controller into Standby/Suspend/Off State
- Power Down internal SRAM in Direct Color Mode

Multimedia Application

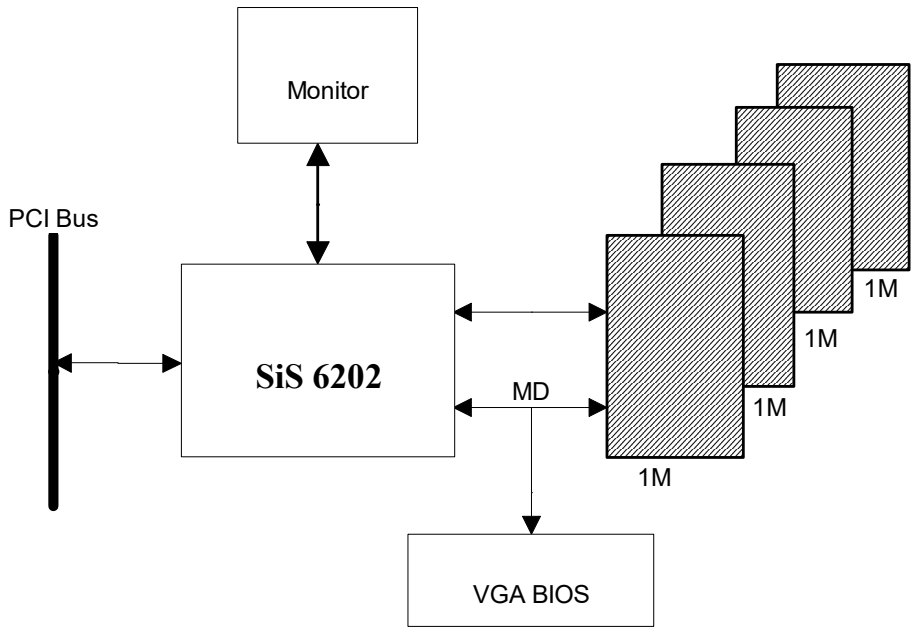
- Support DDC1 and DDC2B Specifications
- Follow the Plug & Play Specification for Display Controller
- Support RAMDAC Snoop for Multimedia Applications

Misc.

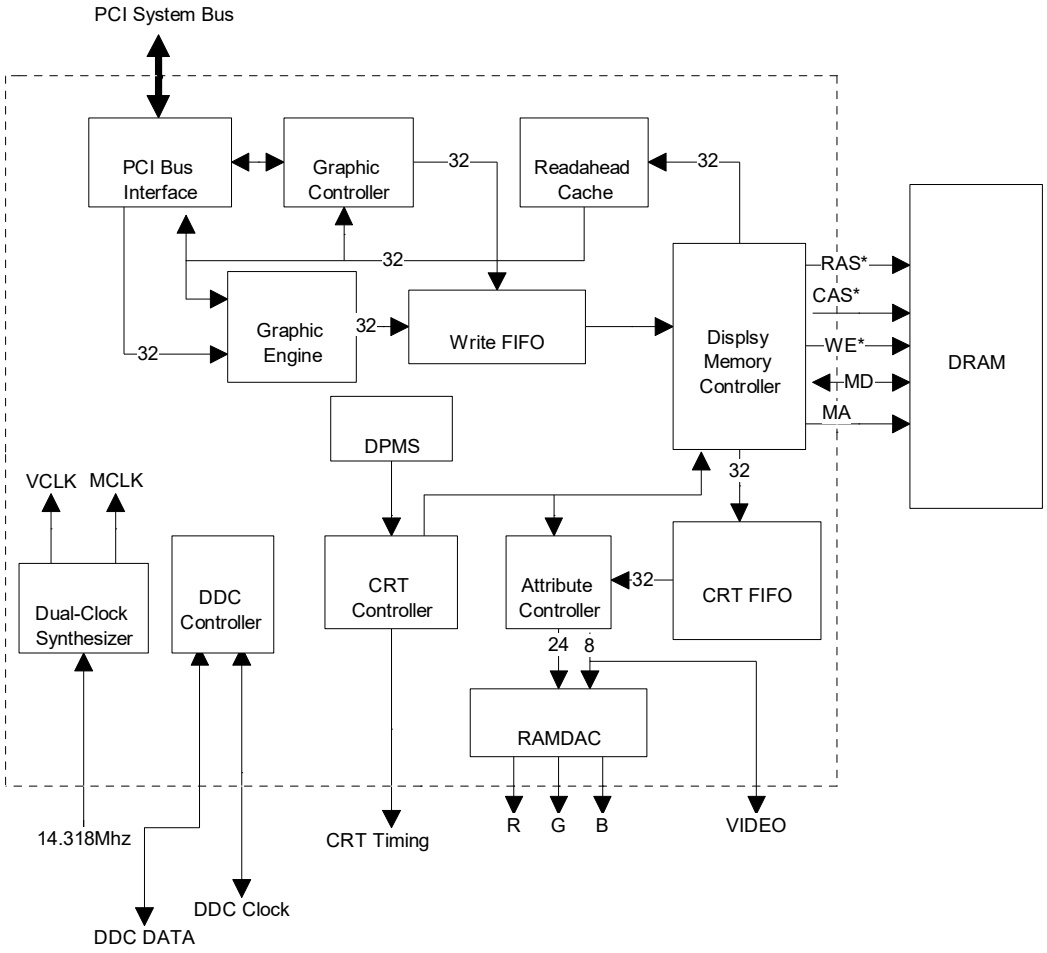
- Only 4 ICs (including DRAMs) Required to Implement a PCI True-Color Graphics Adapter Without Any TTLs
- Support 64K ROM Decoding
- Implemented by Sub-Micron CMOS Technology in 160 Pins PQFP Package

1.3 BLOCK DIAGRAM

1.3.1 System Block Diagram



1.3.2 SiS 6202 Block Diagram



2. FUNCTIONAL DESCRIPTION

2.1 Functional Blocks

2.1.1 Attribute Controller

The Attribute Controller formats the display for the screen. Display color selection, text blinking, alternate font selection, and underlining are performed by the Attribute Controller.

2.1.2 CRT Controller

The CRT Controller generates the HSYNC and VSYNC signals required for the monitor, as well as BLANK* signals required by the Attribute Controller.

2.1.3 CRT FIFO

The 32x24 CRT FIFO allows the Display Memory Controller to access the display memory for screen refresh at maximum memory speed rather than at the screen refresh rate. It provides 3 programmable thresholds - CRT/CPU Threshold Low, CRT/CPU Threshold High, and CRT/Engine Threshold High. With adequate programming these three thresholds, the CPU wait-time would be reduced to improve the graphic performance.

2.1.4 DDC Controller

The DDC Controller provides two different channels to communicate with the monitor which supports DDC level 1 or DDC level 2B. One is DDC CLK channel which is bidirectional and provides the clock for DDC. The other is DDC DATA channel which is bidirectional and could query some information from monitor.

With the advantage of DDC, VGA BIOS could realize the capability of the connected monitor and take adequate action (such as to program the parameters for higher frame rate, ..., etc.) to make end users feel more comfortable.

2.1.5 Display Memory Controller

The Display Memory Controller generates timing for display memory. This includes RAS*, CAS* and multiplexed-address timing, as well as WE*.

2.1.6 DPMS

It provides some registers to control the CRT Timing to be compatible with the VESA DPMS specification. (For detail description, refer to "2.7 Power Management".)

2.1.7 Dual-Clock Synthesizer

The Dual-Clock Synthesizer generates MCLK and VCLK with single external reference clock. With this character, we could set the MCLK at the maximum speed which the display memory could work normally, thus it takes the advantage of the real peak memory bandwidth and improves the graphic performance. (For detail description, refer to "2.6 Internal Dual-Clock Synthesizer".)

2.1.8 Graphic Controller

It performs text manipulation, data rotation, color mapping, and miscellaneous operations.

2.1.9 Graphic Engine

It is an enhanced 32-bit BitBlt Graphic Engine.

For enhanced 256-color graphic mode, the engine supports the following functions:

- 256 Raster Operation Functions
- Rectangle Fill
- Color/Font Expansion
- Enhanced Color/Font Expansion
- Line Drawing
- Built-in 8x8 Pattern Registers
- Built-in 8x8 Mask Registers

For 32K or 64K-color graphic mode, the engine supports the following functions:

- 256 Raster Operation Functions
- Rectangle Fill
- Color/Font Expansion
- Enhanced Color/Font Expansion
- Line Drawing
- Built-in 8x8 Mask Registers

For 16M-color graphic mode, due to different graphic process method, the engine supports the following functions:

- Source/Destination BitBlt
- Pattern/Destination BitBlt
- Color/Font Expansion

There are two different kinds of Command Queue available. One is Hardware Command Queue and the other is Software Command Queue.

For the Hardware Command Queue, the queue is 24 doublewords FIFO built in graphic engine. Since the average length of each engine command is 8 doublewords, the graphic engine could be regarded as 4 stages, for one is active and three are in the queue.
For the Software Command Queue, SiS 6202 takes some area of system memory to be command FIFO, the size of FIFO could be 256K bytes maximum. Thus the stages of graphic engine could be regarded as infinite. With the infinite stages, it could get extra high graphic performance.

Note that the new art for Software Command Queue is developed by SiS corp. and is in patent pending.

2.1.10 PCI Bus Interface

SiS 6202 connects directly to the PCI bus with no glue logic, and it decodes the 32-bit address and responds to the applicable control lines. It could execute both I/O and memory access as an 8-, 16-, 32-bit device.

2.1.11 RAMDAC

The RAMDAC contains the color palette and 24-bit true color DAC.

The color palette, with 256 18-bit entries, converts a color code that specifies the color of a pixel into three 6-bit values, one each for red, green, and blue.

The 24-bit true color DAC is designed for direct color graphic mode. It converts each digital color value to three analog voltages for red, green, and blue.

2.1.12 Read-ahead Cache

It is a 128-bit cache. With this cache, the times of the operation of display memory read would be reduced, thus increase the performance.

2.1.13 Write FIFO

The Write FIFO contains a queue of CPU write accesses to display memory that have not been executed because of memory arbitration. With this queue, the SiS 6202 will release CPU as soon as it record the address and executed data, and write into display memory when the display memory is available. Thus CPU performance is increased.

2.2 BIOS ROM

SiS 6202 follows the One-Load-Per-Slot specification of PCI standard Revision 2.0. The address bus of BIOS ROM are multiplexed with MD[15:0] and the data bus are multiplexed with MD[23:16]. Note that this solution is without glue logic.

2.3 Bus Interface

The SiS 6202 dedicatedly supports 32-bit PCI Local Bus Standard Revision 2.0. Furthermore SiS 6202 supports PCI burst write to take advantage of PCI bus advanced feature to further improve performance. But PCI burst read is not supported since it has very little impact on performance in graphic application.
The SiS 6202 also supports PCI Bus Master with the pins for REQ* and GNT* to achieve extra high graphic performance. The following sub-section would give this feature a detail description.

2.3.1 Bus Master

With the signal protocol of PCI bus master, SiS 6202 would request the right to control PCI bus by asserting REQ* to handshake with PCI bus arbiter. When the PCI bus arbiter asserts the signal GNT*, SiS 6202 gets the right to control the PCI bus and acts as current bus master.

At present only the PCI memory read transaction command is implemented for the SiS 6202 bus master operation, since this is the most important factor in graphics performance. Furthermore SiS 6202 would perform the burst PCI memory read from the system memory if the burst operation is supported and enabled by the system memory controller.

This bus master mechanism is implemented to fetch the graphics engine commands from the Software Command Queue which is located in the system memory. When the graphics engine of SiS 6202 is free and there are some commands in the Software Command Queue, SiS 6202 will assert PCI bus signal REQ* to request the right to read data (graphics engine commands) from system memory.

The whole process is controlled by SiS developed software drivers and executed by SiS 6202 hardware regardless which kind of system you are using (Of course, your system must support PCI bus master operation and it would be preferred for the support of burst PCI memory read.). Therefore the end users would get extra high graphics performance from such kind of design.

2.4 DRAM Support

SiS 6202 supports 1 MByte, 2 Mbyte and 4 MByte DRAM configuration. With the interleaved architecture, only the 70ns DRAMs are required to achieve 1024x768x16M color and 1280x1024x64K color resolutions.

SiS 6202's signal interface can support IBM PS II 72-pin SIMM (single side & dual side). This will help vender to reduce the cost of the mass production for either all-in-one mainboard or graphics adapter card.

The DRAM types that SiS 6202 supports are: 256Kx4, 256Kx8, 1-CAS/2-WE 256Kx16, and 2-CAS/1-WE 256Kx16.

SiS 6202 also supports auto memory size detecting and auto bank switching to provide more flexibility in mass production.

2.5 Interleaved Video Memory Data Bus Architecture

The SiS 6202 uses the technology of Interleave to raise the peak video memory bandwidth to 240 MByte/sec under 2MByte or 4MByte DRAM configuration. This increases approximately 100% of peak video memory bandwidth compared with the traditional 32-bit noninterleaved peak video memory bandwidth of 120MByte/sec.

In the interleaved mode, it would not only greatly increase the screen resolution, but also boost the performance of CPU and Graphic Engine.

In 2MByte DRAM configuration, SiS 6202 can support 1024x768x32K color, 1024x768x64K color, and 800x600x16M color resolutions with no degradation in the graphic performance.

In 4MByte DRAM configuration, SiS 6202 can support 1024x768x16M color, 1280x1024x32K color, and 1280x1024x64K color resolutions. These resolutions are not easily implemented by the regular Graphics Controller architecture.

2.5.1 Memory Configuration Pins

RASA* and RASB* are independent from CASA[0:3]* (WEA[0:3]*[1]), CASB[0:3]* (WEB[0:3]*[1]), OEA* (CASA*[1]), OEB*(CASB*[1]), MAA[0:8], and MAB[0:8]. i.e. You may use different combinations of these signals without any limits. RASA* and RASB* would be internally swapped to support different combinations.

CASA[0:3]* (WEA[0:3]*[1]) and CASB[0:3]*(WEB[0:3]*[1]) are independent from RASA*, RASB*, OEA* (CASA*[1]), OEB* (CASB*[1]), MAA[0:8], and MAB[0:8]. i.e. You may use different combinations of these signals without any limits. CASA[0:3]* (WEA[0:3]*[1]) and CASB[0:3]*(WEB[0:3]*[1]) would be internally swapped to support different combinations. But there is a limitation lies on 2-bank configuration. The valid 2-bank configuration is as follows:

Bank 0	Bank 1	Bank 2	Bank 3
RASA* CASA[0:3]* (WEA[0:3]*[1]) OEA* (CASA*[1])	RASA* CASB[0:3]* (WEB[0:3]*[1]) OEB* (CASB*[1])	RASB* CASA[0:3]* (WEA[0:3]*[1]) OEA* (CASA*[1])	RASB* CASB[0:3]* (WEB[0:3]*[1]) OEB* (CASB*[1])
√	√		
		√	√

In 1-bank configuration,

- Only RASA* would be active inside the chip , but
  it may be swapped to Pin 52 "RASB*".
- Only CASA[0:3]* (WEA[0:3]*[1]) would be active inside the chip , but
  it may be swapped to Pin 49, 48, 47, 46 "CASB[0:3]*" (WEB[0:3]*[1]).
- Only OEA* (CASA*[1]) would be active inside the chip, but
  it may be swapped to Pin 50 "OEB*" (CASB*[1]).
- MAA[0:8] and MAB[0:8] are asserted and deasserted in the same time.

In 2-bank configuration,

- Only RASA* would be active inside the chip , but
  it may be swapped to Pin 52 "RASB*".
- CASA[0:3]* (WEA[0:3]*[1]) and CASB[0:3]*(WEB[0:3]*[1]) would be interleaved.
- OEA* (CASA*[1]) and OEB* (CASB*[1]) would be interleaved.
- MAA[0:8] and MAB[0:8] are asserted and deasserted in the same time.

In 4-bank configuration,

- RASA* and RASB* are asserted exclusively, i.e. they won't be asserted in the same time except in refresh cycle.
- CASA[0:3]* (WEA[0:3]*[1]) and CASB[0:3]* (WEB[0:3]*[1]) would be interleaved.
- OEA* (CASA*[1]) and OEB* (CASB*[1]) would be interleaved.
- MAA[0:8] and MAB[0:8] are asserted and deasserted in the same time.

OEA* and OEB* are pre-reserved for future version to support EDO (Extended Data Output) DRAM .

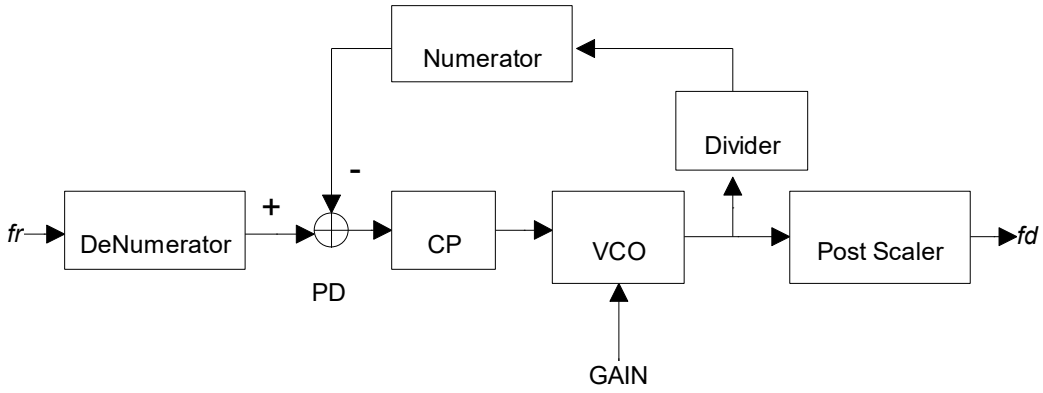
For recommended memory configuration layout, please refer to Appendix A.

Note1: For 2-WE/1-CAS 256Kx16 DRAM.

2.6 Internal Dual-Clock Synthesizer

SiS 6202 has built-in a dual-clock synthesizer to generate the MCLK and VCLK. This clock synthesizer could generate several variable frequencies, thus it could provide the flexibility for selecting the working frequency.

The following block diagram is for clock synthesizer.



where PD is **phase detection**,
CP is **charge pump**,
VCO is **voltage controlled oscillator,**
fr is **reference frequency,** and
fd is **desired frequency**.

The operation of clock synthesizer is described as follow:

When the synthesizer outputs the steady frequency, it means that

fr/DeNumerator = *fd**Post Scaler /(Divider*Numerator).

i.e.

fd=*fr**(Numerator/DeNumerator)*(Divider/Post Scaler).

With this formula, we could select adequate values for Numerator, DeNumerator, Divider, and Post Scaler to obtain the desired frequency.

The planned Video Clocks (VCLK) are as follow: (units: MHz)

25.175	28.322	40.000	50.000	77.000
36.000	44.889	130.000	120.000	80.000
31.500	110.000	65.000	75.000	94.500

These frequencies are compatible with ICS2494-275 or -280.

Other video clocks would be added to the scheme after verified OK.

The planned Memory Clocks (MCLK) are from 50 MHz to 60 MHz with resolution 2 MHz.
Higher memory clocks would be added after verified OK.

2.7 Power Management

To satisfy the power saving for Green PC, SiS 6202 supports the control protocol of DPMS (Display Power Management Signaling) proposed by VESA Monitor Committee. This protocol can reduce the VGA Monitors' power consumption.

SiS 6202 has built-in two timers for stand-by and suspend modes that can be programmed from 2 minutes to 30 minutes (2 min./increase) with the extended registers.

SiS 6202 also supports forcing the video subsystem into stand-by, suspend or off modes with the extended registers.

Power saving is done by blocking HSYNC and/or VSYNC signals to the VGA monitor. The sources of activation are from the monitoring of keyboard, hardware cursor and/or video memory read/write. The overview of the signal blocking requirements are as follows:

POWER MANAGEMENT STATE	HORIZONTAL SYNC	VERTICAL SYNC	VIDEO DISPLAY
ON	Pulses	Pulses	Yes
Stand-By	No Pulses	Pulses	No
Suspend	Pulses	No Pulses	No
OFF	No Pulses	No Pulses	No

2.8 Resolutions Supported

Resolution	1 MByte DRAM	2 MByte DRAM	4 MByte DRAM
640x480x8	√	√	√
640x480x16	√	√	√
640x480x24	√	√	√
800x600x4	√	√	√
800x600x8	√	√	√
800x600x16	√	√	√
800x600x24	X	√	√
1024x768x4	√	√	√
1024x768x8	√	√	√
1024x768x16	X	√	√
1024x768x24	X	X	√

1280x1024x4	√	√	√
1280x1024x8	X	√	√
1280x1024x16	X	X	√

Except these real resolution modes, SiS 6202 is also built-in virtual screen mode which could support up to 2048x2048 resolution.

2.9 Compatibility

The SiS 6202 is fully compatible with all standard IBM VGA modes and EGA, CGA, MDA, and Hercules modes.

2.10 Software Support

To fully utilize and support the SiS 6202 hardware features, SiS has developed a high-performance VESA extension compliant BIOS.

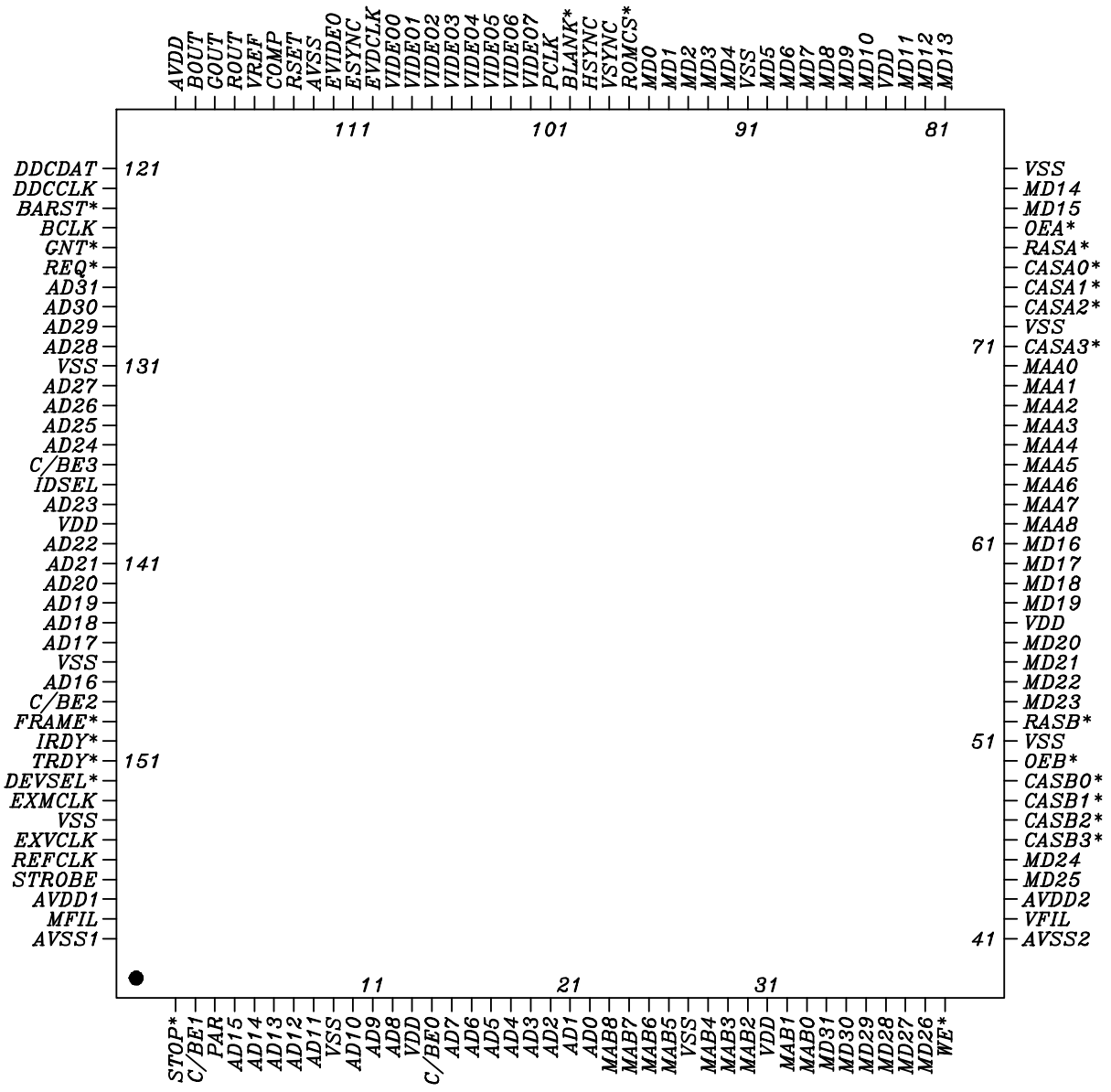
Extended graphic and text modes are supported by software application drivers developed by SiS. The following applications are currently supported:

- 3D Studio Ver. 3.0 & 4.0
- AutoCAD/386 Release 11, 12, 13
- Auto Shade/386 Ver. 2.0
- GEM 3.0/Ventura 2.0
- Lotus 1-2-3/Symphony Ver. 3.x
- MicroSoft Windows 3.1
- MicroSoft Windows 95
- MicroSoft Windows NT Ver. 3.1 & 3.5
- OrCad (SDT/VST/PCB) Rel 4
- OS/2 Presentation Manager 2.1 & 3.0
- P-CAD Ver. 6.06
- VersaCAD/386 Ver. 2.1
- Word Perfect 5.x & 6.0

3. PIN DESCRIPTION

3.1 Pin Assignment

3.1.1 Pin Outline



3.1.2 Pin List

Pin No.	Pin Name	Type	Driving Type
1	STOP*	I/O	8R
2	C/BE1	I/O	8R
3	PAR	I/O	8R
4	AD15	I/O	4
5	AD14	I/O	4
6	AD13	I/O	4
7	AD12	I/O	4
8	AD11	I/O	4
9	VSS		
10	AD10	I/O	4
11	AD9	I/O	4
12	AD8	I/O	4
13	VDD		
14	C/BE0	I/O	8R
15	AD7	I/O	4
16	AD6	I/O	4
17	AD5	I/O	4
18	AD4	I/O	4
19	AD3	I/O	4
20	AD2	I/O	4
21	AD1	I/O	4
22	AD0	I/O	4
23	MAB8	O	8R
24	MAB7	O	8R
25	MAB6	O	8R
26	MAB5	O	8R
27	VSS		
28	MAB4	O	8R
29	MAB3	O	8R
30	MAB2	O	8R
31	VDD		
32	MAB1	O	8R
33	MAB0	O	8R
34	MD31	I/O	4R
35	MD30	I/O	4R
36	MD29	I/O	4R
37	MD28	I/O	4R
38	MD27	I/O	4R
39	MD26	I/O	4R
40	WE*	O	8

Pin No.	Pin Name	Type	Driving Type
41	AVSS2		
42	VFIL	I	
43	AVDD2		
44	MD25	I/O	4R
45	MD24	I/O	4R
46	CASB3*	O	8
47	CASB2*	O	8
48	CASB1*	O	8
49	CASB0*	O	8
50	OEB*	O	8
51	VSS		
52	RASB*	O	8
53	MD23	I/O	4R
54	MD22	I/O	4R
55	MD21	I/O	4R
56	MD20	I/O	4R
57	VDD		
58	MD19	I/O	4R
59	MD18	I/O	4R
60	MD17	I/O	4R
61	MD16	I/O	4R
62	MAA8	O	8R
63	MAA7	O	8R
64	MAA6	O	8R
65	MAA5	O	8R
66	MAA4	O	8R
67	MAA3	O	8R
68	MAA2	O	8R
69	MAA1	O	8R
70	MAA0	O	8R
71	CASA3*	O	8
72	VSS		
73	CASA2*	O	8
74	CASA1*	O	8
75	CASA0*	O	8
76	RASA*	O	8
77	OEA*	O	8
78	MD15	I/O	4R
79	MD14	I/O	4R
80	VSS		

Note: Driving Type
8R: 8mA, 1 driven factor
8 : 8mA, 2 driven factor
4R: 4mA, 0.5 driven factor
4 : 4mA, 1 driven factor

Pin No.	Pin Name	Type	Driving Type
81	MD13	I/O	4R
82	MD12	I/O	4R
83	MD11	I/O	4R
84	VDD		
85	MD10	I/O	4R
86	MD9	I/O	4R
87	MD8	I/O	4R
88	MD7	I/O	4R
89	MD6	I/O	4R
90	MD5	I/O	4R
91	VSS		
92	MD4	I/O	4R
93	MD3	I/O	4R
94	MD2	I/O	4R
95	MD1	I/O	4R
96	MD0	I/O	4R
97	ROMCS*	O	4R
98	VSYNC	O	8R
99	HSYNC	O	8R
100	BLANK*	I/O	4R
101	PCLK	I/O	4
102	VIDEO7	I/O	4R
103	VIDEO6	I/O	4R
104	VIDEO5	I/O	4R
105	VIDEO4	I/O	4R
106	VIDEO3	I/O	4R
107	VIDEO2	I/O	4R
108	VIDEO1	I/O	4R
109	VIDEO0	I/O	4R
110	EVDCLK	I	
111	ESYNC	I	
112	EVIDEO	I	
113	AVSS		
114	RSET	A. I	
115	COMP	A. I	
116	VREF	A. I	
117	ROUT	A. O	
118	GOUT	A. O	
119	BOUT	A. O	
120	AVDD		

Pin No.	Pin Name	Type	Driving Type
121	DDCDAT	I/O	4R
122	DDCCLK	O	4R
123	BARST*	I	
124	BCLK	I	
125	GNT*	I	
126	REQ*	O	4R
127	AD31	I/O	4
128	AD30	I/O	4
129	AD29	I/O	4
130	AD28	I/O	4
131	VSS		
132	AD27	I/O	4
133	AD26	I/O	4
134	AD25	I/O	4
135	AD24	I/O	4
136	C/BE3	I/O	8R
137	IDSEL	I	
138	AD23	I/O	4
139	VDD		
140	AD22	I/O	4
141	AD21	I/O	4
142	AD20	I/O	4
143	AD19	I/O	4
144	AD18	I/O	4
145	AD17	I/O	4
146	VSS		
147	AD16	I/O	4
148	C/BE2	I/O	8R
149	FRAME*	I/O	8R
150	IRDY*	I/O	8R
151	TRDY*	I/O	8R
152	DEVSEL*	O	8R
153	EXMCLK	I	
154	VSS		
155	EXVCLK	I	
156	REFCLK	I	
157	STROBE	O	8R
158	AVDD1		
159	MFIL	I	
160	AVSS1		

Note: Driving Type
8R: 8mA, 1 driven factor
8 : 8mA, 2 driven factor
4R: 4mA, 0.5 driven factor
4 : 4mA, 1 driven factor

Note: A. I: Analog Input
A. O: Analog Output

3.2 Pin Definition

3.2.1 PCI Bus Interface

Pin No.	Symbol	Type	Name and Function
123	BARST*	I	*PCI Reset* is used to bring PCI-specific registers, sequencer, and signals to a consistent state.
124	BCLK	I	*PCI Bus Clock* provides timing for all transactions on PCI bus.
15~22, 10~12, 4~8, 147, 140~145, 138, 132~135, 127~130	AD7~AD0, AD10~AD8, AD15~AD11, AD16, AD22~AD17, AD23 AD27~AD24 AD31~AD28	I/O	*PCI Address/Data Bus* are multiplexed on the same pins. The Address phase is the clock cycle in which FRAME is asserted and the data phase is immediately after the address phase.
14, 2, 148, 136	C/BE0, C/BE1, C/BE2, C/BE3	I/O	*PCI Command/Byte Enable Bus* are multiplexed on the same pins. During the address phase of a transaction, C/BE define the bus command, and during the data phase C/BE are used as Byte Enables.
3	PAR	I/O	*PCI Parity Bit* is even parity across AD[31:0] and C/BE[3:0]
149	FRAME*	I/O	*PCI Frame Cycle* is driven by the current master to indicate the beginning and duration of an access.
151	TRDY*	I/O	*PCI Target Ready* indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
150	IRDY*	I/O	*PCI Initiator Ready* indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction
1	STOP*	I/O	*PCI Stop* indicates the current target is requesting the master to stop the current transaction.

137	IDSEL	I	*PCI Initialization Device Select* is used as a chip select during configuration read and write transactions.
152	DEVSEL*	O	*PCI Device Select* indicates whether any device on the bus has been selected.
126	REQ*	O	*Request* indicates to the arbiter that this agent desires use of the bus.
125	GNT*	I	*Grant* indicates to the agent that access to the bus has been granted.

3.2.2 Display Memory Interface

Pin No.	Symbol	Type	Name and Function
76	RASA*	O	*Bank 0, 1 Row Address Strobe*
52	RASB*	O	*Bank 2, 3 Row Address Strobe*
62~70	MAA[8:0]	O	*Bank 0, 2 Memory Address bus*
23~26, 28~30, 32~33	MAB[8:5], MAB[4:2], MAB[1:0]	O	*Bank 1, 3 Memory Address bus /* *External Clock Gen. Frequency Select* Note that FS[3:0] multiplex with MAB[3:0]
34~39, 44~45, 53~56, 58~61, 78~79, 81~83, 85~90, 92~96	MD[31:26], MD[25:24], MD[23:20], MD[19:16], MD[15:14], MD[13:11], MD[10:5], MD[4:0]	I/O	*Memory Data Bus*

For all DRAM types except 1-CAS/2-WE DRAM,

Pin No.	Symbol	Type	Name and Function
71, 73~75	CASA3*, CASA[2:0]*	O	*Bank 0, 2 Column Address Strobe bus*
46~49	CASB[3:0]*	O	*Bank 1, 3 Column Address Strobe bus*
40	WE*	O	*Write Enable*
77	OEA*	O	*Bank 0, 2 Output Enable*
50	OEB*	O	*Bank 1, 3 Output Enable*

for 1-CAS/2-WE DRAM,

Pin No.	Symbol	Type	Name and Function
71, 73~75	WEA3*, WEA[2:0]*	O	*Bank 0, 2 Write Enable*
46~49	WEB[3:0]*	O	*Bank 1, 3 Write Enable*
40	NC		*No Connection (Left Open)*
77	CASA*	O	*Bank 0, 2 Column Address Strobe*
50	CASB*	O	*Bank 1, 3 Column Address Strobe*

3.2.3 Clock Control

Pin No.	Symbol	Type	Name and Function
156	REFCLK	I	*Reference Clock 14.318 MHz*
159	MFIL	I	*Memory Clock Filter*
160	AVSS1		*Analog Ground for Clock Gen. 1*
158	AVDD1		*Analog Power for Clock Gen. 1*
42	VFIL	I	*Video Clock Filter*
41	AVSS2		*Analog Ground for Clock Gen. 2*
43	AVDD2		*Analog Power for Clock Gen. 2*

3.2.4 Video/Video DAC Interface

Pin No.	Symbol	Type	Name and Function
99	HSYNC	O	*Horizontal Sync*
98	VSYNC	O	*Vertical Sync*
101	PCLK	I/O	*Pixel Clock*
102~109	VIDEO[7:0]	I/O	*Video Data Bus*
100	BLANK*	I/O	*Blank Video signal*
117	ROUT	A. O	*Red Video Signal Output*
118	GOUT	A. O	*Green Video Signal Output*
119	BOUT	A. O	*Blue Video Signal Output*
115	COMP	A. I	*Compensation Pin* Bypass this pin with an external 0.1 uF capacitor to AVDD.

114	RSET	A. I	*Reference Resistor* An external resistor is connected between the RSET pin and AGND to control the magnitude of the full-scale current.
116	VREF	A. I	*Voltage Reference* If an external voltage is used, it must supply this input with a 1.235V reference.
111	ESYNC	I	*Enable Sync Output*
110	EVDCLK	I	*Enable Video Clock Output*
112	EVIDEO	I	*Enable Video Data Output*

Note: A. I: Analog Input, A. O: Analog Output

3.2.5 BIOS Interface

Pin No.	Symbol	Type	Name and Function
97	ROMCS*	O	*ROM Chip Select*
	ROMADR[15:0]	I/O	*ROM Address* Mux with MD[15:0]
	ROMDAT[7:0]	I/O	*ROM Data Bus* Mux with MD[23:16]

3.2.6 DDC Interface

Pin No.	Symbol	Type	Name and Function
121	DDCDAT	I/O	*Display Data Channel Data Line*
122	DDCCLK	I/O	*Display Data Channel Clock Line*

3.2.7 External Clock Interface (option)

Pin No.	Symbol	Type	Name and Function
157	STROBE	O	*Frequency Select Data Strobe* Mux with INTA*
153	EXMCLK	I	*External Memory Clock*
155	EXVCLK	I	*External Video Clock*

3.2.8 Power and Ground

Pin No.	Symbol	Type	Name and Function
120	AVDD		*Analog Power*
113	AVSS		*Analog Ground*
13, 31, 57, 84, 139	VDD		*Digital Power*

9, 27, 51, 72, 80, 91, 131, 146, 154	VSS		*Digital Ground*

4. MODE TABLES

4.1 Standard VGA Modes

MODE	TYPE	DISPLAY SIZE	COLORS SHADES	ALPHA FORMAT	BUFFER START	BOX SIZE	MAX. PAGES
0	A/N	320x200	16	40x25	B800	8x8	8
0*	A/N	320x350	16	40x25	B800	8x14	8
0+	A/N	360x400	16	40x25	B800	9x16	8
1	A/N	320x200	16	40x25	B800	8x8	8
1*	A/N	320x350	16	40x25	B800	8x14	8
1+	A/N	360x400	16	40x25	B800	9x16	8
2	A/N	640x200	16	80x25	B800	8x8	8
2*	A/N	640x350	16	80x25	B800	8x14	8
2+	A/N	720x400	16	80x25	B800	9x16	8
3	A/N	640x200	16	80x25	B800	8x8	8
3*	A/N	640x350	16	80x25	B800	8x14	8
3+	A/N	720x400	16	80x25	B800	9x16	8
4	APA	320x200	4	40x25	B800	8x8	1
5	APA	320x200	4	40x25	B800	8x8	1
6	APA	640x200	2	80x25	B800	8x8	1
7	A/N	720x350	4	80x25	***B000***	9x14	8
7+	A/N	720x400	4	80x25	***B000***	9x16	8
0D	APA	320x200	16	40x25	A000	8x8	8
0E	APA	640x200	16	80x25	A000	8x8	4
0F	APA	640x350	2	80x25	***B000***	8x14	2
10	APA	640x350	16	80x25	A000	8x14	2
11	APA	640x480	2	80x30	A000	8x16	1
12	APA	640x480	16	80x30	A000	8x16	1
13	APA	320x200	256	40x25	A000	8x8	1

Note: 1. A/N: Alpha/Numeric

2. APA: All Point Addressable (Graphic)

MODE	DISPLAY SIZE	COLORS SHADES	FRAME RATE.	H-SYNC.	VIDEO FREQ.
0	320x200	16	70	31.5 K	25.1 M
0*	320x350	16	70	31.5 K	25.1 M
0+	360x400	16	70	31.5 K	28.3 M
1	320x200	16	70	31.5 K	25.1 M
1*	320x350	16	70	31.5 K	25.1 M
1+	360x400	16	70	31.5 K	28.3 M
2	640x200	16	70	31.5 K	25.1 M
2*	640x350	16	70	31.5 K	25.1 M
2+	720x400	16	70	31.5 K	28.3 M
3	640x200	16	70	31.5 K	25.1 M
3*	640x350	16	70	31.5 K	25.1 M
3+	720x400	16	70	31.5 K	28.3 M
4	320x200	4	70	31.5 K	25.1 M
5	320x200	4	70	31.5 K	25.1 M
6	640x200	2	70	31.5 K	25.1 M
7*	720x350	4	70	31.5 K	28.3 M
7+	720x400	4	70	31.5 K	28.3 M
0D	320x200	16	70	31.5 K	25.1 M
0E	640x200	16	70	31.5 K	25.1 M
0F	640x350	2	70	31.5 K	25.1 M
10	640x350	16	70	31.5 K	25.1 M
11	640x480	2	60	31.5 K	25.1 M
12	640x480	16	60	31.5 K	25.1 M
13	320x200	256	70	31.5 K	25.1 M

Note : i - interlaced mode

n - noninterlaced mode

4.2 Enhanced Video Modes

MODE	TYPE	DISPLAY SIZE	COLORS SHADES	ALPHA FORMAT	BUFFER START	BOX SIZE	MAX. PAGES
22	A/N	1056x352	16	132x44	B800	8x8	2
23	A/N	1056x350	16	132x25	B800	8x14	4
24	A/N	1056x364	16	132x28	B800	8x13	4
25	APA	640x480	16	80x60	A000	8x8	1
26	A/N	720x480	16	80x60	B800	9x8	3
29	APA	800x600	16	100x37	A000	8x16	1
2A	A/N	800x600	16	100x40	B800	8x15	4
2D	APA	640x350	256	80x25	A000	8x14	1
2E	APA	640x480	256	80x30	A000	8x16	1
2F	APA	640x400	256	80x25	A000	8x16	1
30	APA	800x600	256	100x37	A000	8x16	1
37	APA	1024x768	16	128x48	A000	8x16	1
38	APA	1024x768	256	128x48	A000	8x16	1
39	APA	1280x1024	16	160x64	A000	8x16	1
3A	APA	1280x1024	256	160x64	A000	8x16	1
40	APA	320x200	32K	40x25	A000	8x8	1
41	APA	320x200	64K	40x25	A000	8x8	1
42	APA	320x200	16.8M	40x25	A000	8x8	1
43	APA	640x480	32K	80x30	A000	8x16	1
44	APA	640x480	64K	80x30	A000	8x16	1
45	APA	640x480	16.8M	80x30	A000	8x16	1
46	APA	800x600	32K	100x37	A000	8x16	1
47	APA	800x600	64K	100x37	A000	8x16	1
48	APA	800x600	16.8M	100x37	A000	8x16	1
49	APA	1024x768	32K	128x48	A000	8x16	1
4A	APA	1024x768	64K	128x48	A000	8x16	1
4B	APA	1024x768	16.8M	128x48	A000	8x16	1
4C	APA	1280x1024	32K	160x64	A000	8x16	1
4D	APA	1280x1024	64K	160x64	A000	8x16	1

Note: 1. A/N: Alpha/Numeric

2. APA: All Point Addressable (Graphic)

MODE	DISPLAY SIZE	COLORS SHADES	FRAME RATE.	H-SYNC.	VIDEO FREQ.
22	1056x352	16	70	30.5 K	40.0 M
23	1056x350	16	70	30.5 K	40.0 M
24	1056x364	16	70	30.5 K	40.0 M
25	640x480	16	60	31.5 K	25.1 M
26	720x480	16	60	31.5 K	25.1 M
29	800x600	16	56	35.1 K	30.0 M
29*	800x600	16	60	37.9 K	40.0 M
29+	800x600	16	72	48.0 K	50.0 M
29#	800x600	16	75	46.8 K	50.0 M
2A	800x600	16	56	35.1 K	36.0 M
2D	640x350	256	70	31.5 K	25.1 M
2E	640x480	256	60	31.5 K	25.1 M
2E*	640x480	256	72	37.9 K	31.5 M
2E+	640x480	256	75	37.5 K	31.5 M
2F	640x400	256	70	31.5 K	25.1 M
30	800x600	256	56	35.1 K	36.0 M
30*	800x600	256	60	37.9 K	40.0 M
30+	800x600	256	72	48.0 K	50.0 M
30#	800x600	256	75	46.8 K	50.0 M
37i	1024x768	16	87	35.5 K	44.9 M
37n	1024x768	16	60	48.4 K	65.0 M
37n+	1024x768	16	70	56.5 K	75.0 M
37n#	1024x768	16	75	60.2 K	80.0 M
38i	1024x768	256	87	35.5 K	44.9 M
38n	1024x768	256	60	48.4 K	65.0 M
38n+	1024x768	256	70	56.5 K	75.0 M
38n#	1024x768	256	75	60.2 K	80.0 M
39i	1280x1024	16	89	48.8 K	80.0 M
39n	1280x1024	16	60	65.0 K	110.0 M
3Ai	1280x1024	256	89	48.8 K	80.0 M
3An	1280x1024	256	60	65.0 K	110.0 M

40	320x200	32K	70	31.5 K	25.1 M
41	320x200	64K	70	31.5 K	25.1 M
42	320x200	16.8M	70	31.5 K	25.1 M
43	640x480	32K	60	31.5 K	25.1 M
43*	640x480	32K	72	37.9 K	31.5 M
43+	640x480	32K	75	37.5 K	31.5 M
44	640x480	64K	60	31.5 K	25.1 M
44*	640x480	64K	72	37.9 K	31.5 M
44+	640x480	64K	75	37.5 K	31.5 M
45	640x480	16.8M	60	31.5 K	25.1 M
45*	640x480	16.8M	72	37.9 K	31.5 M
45+	640x480	16.8M	75	37.5 K	31.5 M
46	800x600	32K	56	35.1 K	36.0 M
46*	800x600	32K	60	37.9 K	40.0 M
46+	800x600	32K	72	48.0 K	50.0 M
46#	800x600	32K	75	46.8 K	50.0 M
47	800x600	64K	56	35.1 K	36.0 M
47*	800x600	64K	60	37.9 K	40.0 M
47+	800x600	64K	72	48.0 K	50.0 M
47#	800x600	64K	75	46.8 K	50.0 M
48	800x600	16.8M	56	35.1 K	36.0 M
48*	800x600	16.8M	60	37.9 K	40.0 M
48+	800x600	16.8M	72	48.0 K	50.0 M
48#	800x600	16.8M	75	46.8 K	50.0 M
49i	1024x768	32K	87	35.5 K	44.9 M
49n	1024x768	32K	60	48.4 K	65.0 M
49n+	1024x768	32K	70	56.5 K	75.0 M
49n#	1024x768	32K	75	60.2 K	80.0 M
4Ai	1024x768	64K	87	35.5 K	44.9 M
4An	1024x768	64K	60	48.4 K	65.0 M
4An+	1024x768	64K	70	56.5 K	75.0 M
4An#	1024x768	64K	75	60.2 K	80.0 M
4Bi	1024x768	16.8M	87	35.5 K	44.9 M
4Ci	1280x1024	32K	89	48.8 K	80.0 M
4Di	1280x1024	64K	89	48.8 K	80.0 M

Note: i - interlaced mode

n - noninterlaced mode

5. REGISTERS DESCRIPTION

- 5.1 to 5.6 are IBM VGA standard registers.
- 5.7 to 5.8 are SiS 6202 Extended Registers.

5.1 General Registers

5.1.1 Miscellaneous Output Register

Register Type: Read/Write
Read Port: 3CC
Write Port: 3C2
Default: 00h

D7 Vertical Sync Polarity
- 0: Select 'positive vertical sync'
- 1: Select 'negative vertical sync'

D6 Horizontal Sync Polarity
- 0: Select 'positive horizontal sync'
- 1: Select 'negative horizontal sync'

Sync Polarity vs. Vertical Screen Resolution

D7	D6	EGA	VGA
0	0	200 Lines	Invalid
0	1	350 Lines	400 Lines
1	0	Invalid	350 Lines
1	1	Invalid	480 Lines

D5 Odd/Even Page
- 0: Select low page of memory
- 1: Select high page of memory

D4 Reserved

D[3:2] Clock Select

Table for Video Clock Selection

D3	D2	FS[3:0]
0	0	0000 (25.175 MHz)
0	1	0001 (28.322 MHz)
1	0	Don't Care
1	1	For external clock, refer to Extended Registers 5.7.3, Index_07h D[3:0]. For internal clock generator, it's don't care.

D1 Display RAM Enable
- 0: Disable processor access to video RAM
- 1: Enable processor access to video RAM

D0 I/O Address Select
- 0: Sets addresses for monochrome emulation
- 1: Sets addresses for color graphics emulation

5.1.2 Feature Control Register

Register Type: Read/Write
Read Port: 3CA
Write Port: 3BA/3DA
Default: 00h

D[7:4] Reserved (0)

D3 Vertical Sync Select
- 0: Normal Vertical Sync output to monitor
- 1: [Vertical Sync OR Vertical Display Enable] output to monitor

D[2:0] Reserved (0)

5.1.3 Input Status Register 0

Register Type: Read only
Read Port: 3C2
Default: 00h

D7 Vertical Retrace Interrupt Pending
- 0: Cleared
- 1: Pending

D[6:5] Reserved
D4 Switch Sense
D[3:0] Reserved

5.1.4 Input Status Register 1

Register Type: Read only
Read Port: 3BA/3DA
Default: 00h

D[7:6] Reserved
D[5:4] Diagnostic

Table for Video Read-back Through Diagnostic Bit (I)

Color Plane Enable Register		Input Status Register 1	
D5	**D4**	**D5**	**D4**
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table for Video Read-back Through Diagnostic Bit (II)

Color Plane Enable Register		Input Status Register 1	
D5	**D4**	**D5**	**D4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D3 Vertical Retrace
0: Inactive
1: Active
D[2:1] Reserved
D0 Display Enable Not
0: Display period
1: Retrace period

5.1.5 VGA Enable Register

Register Type: Read/Write
Read/Write Port: 3C3 or 46E8
Default: 00h

D0 VGA Enable (for 3C3 only)
0: Disable
1: Enable

D3 VGA Enable (for 46E8 only)
0: Disable
1: Enable

5.2 CRT Controller Registers

5.2.0 CRT Controller Index Register

Register Type: Read/Write
Read/Write Port: 3B4/3D4
Default: 00h

D[7:5] Reserved
D[4:0] CRT Controller Index (00~18h)

Index (3B4/3D4)	CRT Controller Registers (3B5/3D5)
0h	Horizontal Total
1h	Horizontal Display End
2h	Horizontal Blank Start
3h	Horizontal Blank End
4h	Horizontal Retrace Start
5h	Horizontal Retrace End
6h	Vertical Total
7h	Overflow Register
8h	Preset Row Scan
9h	Max Scan Line/Text Character Height
Ah	Text Cursor Start
Bh	Text Cursor End
Ch	Screen Start Address High
Dh	Screen Start Address Low
Eh	Text Cursor Location High
Fh	Text Cursor Location Low
10h	Vertical Retrace Start
11h	Vertical Retrace End
12h	Vertical Display End
13h	Screen Offset
14h	Underline Location
15h	Vertical Blank Start
16h	Vertical Blank End
17h	Mode Control
18h	Line Compare

5.2.1 CR0: Horizontal Total

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 00h
Default: 00h

D[7:0] Horizontal Total Bit[7:0]

5.2.2 CR1: Horizontal Display Enable End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 01h
Default: 00h

D[7:0] Horizontal Display Enable End Bit[7:0]

5.2.3 CR2: Horizontal Blank Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 02h
Default: 00h

D[7:0] Horizontal Blank Start Bit[7:0]

5.2.4 CR3: Horizontal Blank End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 03h
Default: 00h

D7 Reserved
D[6:5] Display Skew Control Bit[1:0]
00: No skew
01: Skew 1 character
10: Skew 2 characters
11: Skew 3 characters
D[4:0] Horizontal Blank End Bit[4:0]

5.2.5 CR4: Horizontal Retrace Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 04h
Default: 00h

D[7:0] Horizontal Retrace Start Bit[7:0]

5.2.6 CR5: Horizontal Retrace End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 05h
Default: 00h

D7 Horizontal Blank End Bit[5]
D[6:5] Horizontal Retrace Delay Bit[1:0]
00: Skew 0 character clock
01: Skew 1 character clock
10: Skew 2 character clocks
11: Skew 3 character clocks
D[4:0] Horizontal Retrace End Bit[4:0]

5.2.7 CR6: Vertical Total

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 06h
Default: 00h

D[7:0] Vertical Total Bit[7:0]

5.2.8 CR7: Overflow Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 07h
Default: 00h

D7 Vertical Retrace Start Bit[9]
D6 Vertical Display Enable End Bit[9]
D5 Vertical Total Bit[9]
D4 Line Compare Bit[8]
D3 Vertical Blank Start Bit[8]
D2 Vertical Retrace Start Bit[8]
D1 Vertical Display Enable End Bit[8]
D0 Vertical Total Bit[8]

5.2.9 CR8: Preset Row Scan

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 08h
Default: 00h

D7	Reserved
D[6:5]	Byte Panning Control Bit[1:0]
D[4:0]	Preset Row Scan Bit[4:0]

5.2.10 CR9: Maximum Scan Line/Text Character Height

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 09h
Default: 00h

D7	Double Scan 0: Disable 1: Enable 400 lines display
D6	Line Compare Bit[9]
D5	Vertical Blank Start Bit[9]
D[4:0]	Character Cell Height Bit[4:0]

5.2.11 CRA: Text Cursor Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Ah
Default: 00h

D[7:6]	Reserved
D5	Text Cursor Off 0: Text Cursor On 1: Text Cursor Off
D[4:0]	Text Cursor Start Bit[4:0]

5.2.12 CRB: Text Cursor End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Bh
Default: 00h

D7	Reserved

D[6:5] Text Cursor Skew
- 00: No skew
- 01: Skew one character clock
- 10: Skew two character clocks
- 11: Skew three character clocks

D[4:0] Text Cursor End Bit[4:0]

5.2.13 CRC: Screen Start Address High

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Ch
Default: 00h

D[7:0] Screen Start Address Bit[15:8]

5.2.14 CRD: Screen Start Address Low

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Dh
Default: 00h

D[7:0] Screen Start Address Bit[7:0]

5.2.15 CRE: Text Cursor Location High

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Eh
Default: 00h

D[7:0] Text Cursor Location Bit[15:8]

5.2.16 CRF: Text Cursor Location Low

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Fh
Default: 00h

D[7:0] Text Cursor Location Bit[7:0]

5.2.17 CR10: Vertical Retrace Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 10h
Default: 00h

D[7:0] Vertical Retrace Start Bit[7:0]

5.2.18 CR11: Vertical Retrace End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 11h
Default: 00h

D7 Write Protect for CR0 to CR7
- 0: Disable Write Protect
- 1: Enable Write Protect

D6 Alternate Refresh Rate
- 0: Selects three refresh cycles per scanline
- 1: Selects five refresh cycles per scanline

D5 Vertical Interrupt Enable
- 0: Enable
- 1: Disable

D4 Vertical Interrupt Clear
- 0: Clear
- 1: Not Clear

D[3:0] Vertical Retrace End Bit[3:0]

5.2.19 CR12: Vertical Display Enable End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 12h
Default: 00h

D[7:0] Vertical Display Enable End Bit[7:0]

5.2.20 CR13: Screen Offset

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 13h
Default: 00h

D[7:0] Screen Offset Bit[7:0]

5.2.21 CR14: Underline Location Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 14h

Default: 00h

D7	Reserved
D6	Doubleword Mode Enable
	0: Disable
	1: Enable
D5	Count by 4
	0: Disable
	1: Enable
D[4:0]	Underline Location Bit[4:0]

5.2.22 CR15: Vertical Blank Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 15h
Default: 00h

D[7:0]	Vertical Blank Start Bit[7:0]

5.2.23 CR16: Vertical Blank End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 16h
Default: 00h

D[7:0]	Vertical Blank End Bit[7:0]

5.2.24 CR17: Mode Control Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 17h
Default: 00h

D7	Hardware Reset
	0: Disable horizontal and vertical retrace outputs
	1: Enable horizontal and vertical retrace outputs
D6	Word/Byte Address Mode
	0: Set the memory address mode to word
	1: Set the memory address mode to byte
D5	Address Wrap
	0: Disable the full 256K of memory
	1: Enable the full 256K of memory

D4	Reserved
D3	Count by Two
	0: Byte refresh
	1: Word refresh
D2	Horizontal Retrace Select
	0: Normal
	1: Double Scan
D1	RA1 replace MA14
	0: Enable
	1: Disable
D0	RA0 replace MA13
	0: Enable
	1: Disable

5.2.25 CR18:Line Compare Register

Register Type:	Read/Write
Read/Write Port:	3B5/3D5, Index 18h
Default:	00h

D[7:0]	Line Compare Bit[7:0]

5.3 Sequencer Registers

5.3.0 Sequencer Index Register

Register Type: Read/Write
Read/Write Port: 3C4
Default: 00h

D[7:6] Reserved
D[5:0] Sequencer Index Bit[5:0]

Table of Sequencer Registers

Index (3C4)	Sequencer Register (3C5)
00	Reset Register
01	Clock Mode
02	Color Plane Write Enable
03	Character Generator Select
04	Memory Mode

5.3.1 SR0: Reset Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 00h
Default: 00h

D[7:2] Reserved
D1 Synchronous reset
0: Reset
1: Normal
D0 Asynchronous reset
0: Reset
1: Normal

5.3.2 SR1: Clock Mode Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 01h
Default: 00h

D[7:6] Reserved
D5 Screen Off

0: Display On
1: Display Off

D4 Shifter Load 32 enable
0: Disable
1: Data shifter loaded every 4th Character Clock

D3 Dot Clock Divide by 2 enable
0: Disable
1: Video Clock is divided by 2 to generate Dot Clock

D2 Shifter Load 16 (while D4=0)
0: Disable
1: Data shifter loaded every 2nd Character Clock

D1 Reserved

D0 8/9 Dot Clock
0: Dot Clock is divided by 9 to generate Character Clock
1: Dot Clock is divided by 8 to generate Character Clock

5.3.3 SR2: Color plane Write Enable Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 02h
Default: 00h

D[7:4] Reserved

D3 Plane 3 write enable
0: Disable
1: Enable

D2 Plane 2 write enable
0: Disable
1: Enable

D1 Plane 1 write enable
0: Disable
1: Enable

D0 Plane 0 write enable
0: Disable
1: Enable

5.3.4 SR3: Character Generator Select Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 03h
Default: 00h

D[7:6] Reserved
D5 Character generator table B select Bit[2]
D4 Character generator table A select Bit[2]
D[3:2] Character generator table B select Bit[1:0]
D[1:0] Character generator table A select Bit[1:0]

Table of Selecting Active Character Generator

D5	D3	D2	Used when text attribute bit 3 is 1
D4	D1	D0	Used when text attribute bit 3 is 0
0	0	0	Character Table 1
0	0	1	Character Table 2
0	1	0	Character Table 3
0	1	1	Character Table 4
1	0	0	Character Table 5 (VGA only)
1	0	1	Character Table 6 (VGA only)
1	1	0	Character Table 7 (VGA only)
1	1	1	Character Table 8 (VGA only)

5.3.5 SR4: Memory Mode Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 04h
Default: 00h

D[7:4] Reserved
D3 Chain-4 Mode enable
0: Disable
1: Enable
D2 Odd/Even Mode enable
0: Disable
1: Enable

D1	Extended Memory	
	0:	Select 64K
	1:	Select 256K
D0	Reserved	

5.4 Graphics Controller Registers

5.4.0 Graphics Controller Index Register

Register Type: Read/Write
Read/Write Port: 3CE
Default: 00h

D[7:4] Reserved
D[3:0] Graphics Controller Index Bit[3:0]

Index (3CE)	Graphics Controller Register (3CF)
00	Set/Reset Register
01	Set/Reset Enable Register
02	Color Compare Register
03	Data Rotate & Function Select
04	Read Plane Select Register
05	Mode Register
06	Miscellaneous Register
07	Color Don't Care Register
08	Bit Mask Register

5.4.1 GR0: Set/Reset Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 00h
Default: 00h

D[7:4] Reserved
D3 Set/Reset Map for plane 3
D2 Set/Reset Map for plane 2
D1 Set/Reset Map for plane 1
D0 Set/Reset Map for plane 0

5.4.2 GR1: Set/Reset Enable Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 01h
Default: 00h

D[7:4] Reserved
D3 Enable Set/Reset for plane 3

0: Disable
1: Enable

D2 Enable Set/Reset for plane 2
0: Disable
1: Enable

D1 Enable Set/Reset for plane 1
0: Disable
1: Enable

D0 Enable Set/Reset for plane 0
0: Disable
1: Enable

5.4.3 GR2: Color Compare Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 02h
Default: 00h

D[7:4] Reserved
D3 Color Compare Map for plane 3
D2 Color Compare Map for plane 2
D1 Color Compare Map for plane 1
D0 Color Compare Map for plane 0

5.4.4 GR3: Data Rotate/Function Select Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 03h
Default: 00h

D[7:5] Reserved

D[4:3] Function Select

Table of Function Select

D4	D3	Function
0	0	write data unmodified
0	1	write data AND processor latches
1	0	write data OR processor latches
1	1	write data XOR processor latches

D[2:0] Rotate Count

Table of Rotate Count

D2	D1	D0	Right Rotation
0	0	0	none
0	0	1	1 bits
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

5.4.5 GR4: Read Plane Select Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 04h
Default: 00h

D[7:2] Reserved
D[1:0] Read Plane Select bit 1, 0
00: Plane 0
01: Plane 1
10: Plane 2
11: Plane 3

5.4.6 GR5: Mode Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 05h
Default: 00h

D7 Reserved
D6 256-color Mode
0: Disable
1: Enable
D5 Shift Register Mode
0: Configure shift register to be EGA compatible
1: Configure shift register to be CGA compatible
D4 Odd/Even Addressing Mode enable
0: Disable
1: Enable
D3 Read Mode
0: Map Select Read
1: Color Compare Read
D2 Reserved
D[1:0] Write mode

Table for Write Mode

D1	D0	Mode Selected
0	0	*Write Mode 0:* Direct processor write (Data Rotate, Set/Reset may apply).
0	1	*Write Mode 1:* Use content of latches as write data.
1	0	*Write Mode 2:* Color Plane n(0-3) is filled with the value of bit m in the processor write data.
1	1	*Write Mode 3:* Color Plane n(0-3) is filled with 8 bits of the color value contained in the Set/Reset Register for that plane. The Enable Set/Reset Register is not effective. Processor data will be AND with Bit Mask Register content to form new bit mask pattern. (data rotate may apply)

5.4.7 GR6: Miscellaneous Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 06h
Default: 00h

D[7:4] Reserved

D[3:2] Memory Address Select

Table of Memory Address Select

D3	D2	Address range
0	0	A0000 to BFFFF
0	1	A0000 to AFFFF
1	0	B0000 to B7FFF
1	1	B8000 to BFFFF

D1 Chain Odd And Even Maps
- 0: Disable
- 1: Enable

D0 Graphics Mode Enable
- 0: Select alphanumeric mode
- 1: Select graphics mode

5.4.8 GR7: Color Don't Care Register

Register Type: Read/Write
Read/Write Port: 3CF, Index 07h
Default: 00h

D[7:4] Reserved

D3 Plane 3 Don't Care
- 0: Disable color comparison
- 1: Enable color comparison

D2 Plane 2 Don't Care
- 0: Disable color comparison
- 1: Enable color comparison

D1 Plane 1 Don't Care
- 0: Disable color comparison
- 1: Enable color comparison

D0 Plane 0 Don't Care
- 0: Disable color comparison
- 1: Enable color comparison

5.4.9 GR8: Bit Mask Register

Register Type: Read/Write

Read/Write Port: 3CF, Index 08h
Default: 00h

D[7:0] Bit Mask Enable Bit[7:0]

5.5 Attribute Controller and Video DAC Registers

5.5.0 Attribute Controller Index Register

Register Type: Read/Write
Read Port: 3C0
Write Port: 3C0
Default: 00h

D[7:6] Reserved
D5 Palette Address Source
0: From CPU
1: From CRT
D[4:0] Attribute Controller Index Bit[4:0] (00h-14h)

Index (3C0)	Attribute Controller Register (3C0)
00h	Color Palette Register 0
01h	Color Palette Register 1
02h	Color Palette Register 2
03h	Color Palette Register 3
04h	Color Palette Register 4
05h	Color Palette Register 5
06h	Color Palette Register 6
07h	Color Palette Register 7
08h	Color Palette Register 8
09h	Color Palette Register 9
0Ah	Color Palette Register 10
0Bh	Color Palette Register 11
0Ch	Color Palette Register 12
0Dh	Color Palette Register 13
0Eh	Color Palette Register 14
0Fh	Color Palette Register 15
10h	Mode Control Register
11h	Screen Border Color
12h	Color Plane Enable Register
13h	Horizontal Panning Register
14h	Color Select Register (VGA)

5.5.1 AR0~ARF: Palette Registers

Register Type: Read/Write
Read Port: 3C1, Index 00h ~ 0Fh
Write Port: 3C0, Index 00h ~ 0Fh
Default: 00h

D[7:6] Reserved
D[5:0] Palette Entries

5.5.2 AR10: Mode Control Register

Register Type: Read/Write
Read Port: 3C1, Index 10h
Write Port: 3C0, Index 10h
Default: 00h

D7 P4, P5 Source Select
- 0: AR0-F Bit[5:4] are used as the source for the Lookup Table Address Bit[5:4]
- 1: AR14 Bit[1:0] are used as the source for the Lookup Table Address Bit[5:4]

D6 Pixel Double Clock Select
- 0: The pixels are clocked at every clock cycle
- 1: The pixels are clocked at every other clock cycle

D5 PEL Panning Compatibility with Line Compare
- 0: Disable
- 1: Enable

D4 Reserved

D3 Background Intensity or Blink enable (while the Character Attribute D7=1)
- 0: Background Intensity attribute enable
- 1: Background Blink attribute enable

D2 Line Graphics enable
- 0: The ninth bit of nine-bit-wide character cell will be the same as the background.
- 1: The ninth bit of nine-bit-wide character cell will be made be the same as the eighth bit for character codes in the range C0h through DFh.

D1 Display Type
- 0: The contents of the Attribute byte are treated as color attribute.
- 1: The contents of the Attribute byte are treated as MDA-compatible attribute.

D0 Graphics/Text Mode
- 0: The Attribute Controller will function in text mode.
- 1: The Attribute Controller will function in graphic mode.

5.5.3 AR11: Screen Border Color

Register Type: Read/Write
Read Port: 3C1, Index 11h
Write Port: 3C0, Index 11h
Default: 00h

D[7:6] Reserved
D[5:0] Palette Entry

5.5.4 AR12: Color Plane Enable Register

Register Type: Read/Write
Read Port: 3C1, Index 12h
Write Port: 3C0, Index 12h
Default: 00h

D[7:6] Reserved
D[5:4] Display Status MUX Bit[1:0]
These bits select two of the eight bits color outputs to be available in the status register. The output color combinations available on the status bits are as follows:

Table for Video Read-back Through Diagnostic Bit (I)

Color Plane Enable Register		Input Status Register 1 (Refer to 5.1.4)	
D5	**D4**	**D5**	**D4**
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table for Video Read-back Through Diagnostic Bit (II)

Color Plane Enable Register		Input Status Register 1 (Refer to 5.1.4)	
D5	**D4**	**D5**	**D4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D[3:0] Enable Color Plane Bit[3:0]

5.5.5 AR13: Pixel Panning Register

Register Type: Read/Write
Read Port: 3C1, Index 13h
Write Port: 3C0, Index 13h
Default: 00h

D[7:4] Reserved
D[3:0] Pixel Pan Bit[3:0]
This field specifies the number of pixels the display data will be shifted to the left. This field is interpreted as indicated in the following table:

D3	D2	D1	D0	Monochrome Text	VGA Mode 13	All others
0	0	0	0	8	0	0
0	0	0	1	0	Invalid	1
0	0	1	0	1	1	2
0	0	1	1	2	Invalid	3
0	1	0	0	3	2	4
0	1	0	1	4	Invalid	5
0	1	1	0	5	3	6
0	1	1	1	6	Invalid	7
1	0	0	0	7	Invalid	Invalid
1	0	0	1	Invalid	Invalid	Invalid
1	0	1	0	Invalid	Invalid	Invalid
1	0	1	1	Invalid	Invalid	Invalid
1	1	0	0	Invalid	Invalid	Invalid
1	1	0	1	Invalid	Invalid	Invalid
1	1	1	0	Invalid	Invalid	Invalid
1	1	1	1	Invalid	Invalid	Invalid

5.5.6 AR14: Color Select Register

Register Type: Read/Write
Read Port: 3C1, Index 14h
Write Port: 3C0, Index 14h
Default: 00h

D[7:4] Reserved

D[3:2] Color Bit[7:6]
These two bits are concatenated with the six bits from the Palette Register to form the address into the LUT and to drive P[7:6]

D[1:0] Color Bit[5:4]
If AR10 D7 is programmed to a '1', these two bits replace the corresponding two bits from the Palette Register to form the address into the LUT and to drive P[5:4]. If AR10 D7 is programmed to a '0', these two bits are ignored.

5.6 Color Registers

5.6.1 DAC Status Register

Register Type: Read Only
Read Port: 3C7
Default: 00h

D[7:2] Reserved
D[1:0] DAC State Bit[1:0]
00: Write Operation in progress
11: Read Operation in progress

5.6.2 DAC Index Register (Read Mode)

Register Type: Write Only
Write Port: 3C7
Default: 00h

D[7:0] DAC Index Bit[7:0]

5.6.3 DAC Index Register (Write Mode)

Register Type: Read/Write
Read/Write Port: 3C8
Default: 00h

D[7:0] DAC Index Bit[7:0]

5.6.4 DAC Data Register

Register Type: Read/Write
Read/Write Port: 3C9
Default: 00h

D[7:6] Reserved
D[5:0] DAC Data [5:0]
Before writing to this register, 3C8h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue values for the DAC entry are written. After the third value is written, the values are transferred to the LUT and the DAC index is incremented in case new values for the next DAC index are to be written.

Before reading from this register, 3C7h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue value for the DAC entry may be read from this DAC index. After the third value is read, the DAC index is incremented in case the value for the next DAC index to be read.

5.6.5 PEL Mask Register

Register Type: Read/Write
Read/Write Port: 3C6
Default: 00h

D[7:0] Pixel Mask Bit[7:0]

This field is the Pixel Mask for the palette DAC. If a bit in this field is programmed to a '0', the corresponding bit in the pixel data will be ignored in looking up an entry in the LUT.

5.7 SiS 6202 Extended Registers

5.7.0 Extended Index Register

Register Type: Read/Write
Read/Write Port: 3C4
Default: 00h

D[7:6] Reserved
D[5:0] Extended Register Index Bit[5:0] (05h ~ 2Fh)

Index (3C4)	Extended Enhanced Register (3C5)
05h	Extended Password/Identification Register
06h	Extended Graphics Mode Control Register
07h	Extended External Video Frequency Select Register
08h	Extended CRT/CPU Threshold Control Register 0
09h	Extended CRT/CPU Threshold Control Register 1
0Ah	Extended CRT Overflow Register
0Bh	Extended Misc. Control Register 0
0Ch	Extended Misc. Control Register 1
0Dh	Extended Configuration Register 0
0Eh	Extended Configuration Register 1
0Fh	Extended Scratch Register 0
10h	Extended Scratch Register 1
11h	Extended DDC and Power Control Register
14h	Extended Hardware Cursor Color 0 Red Register
15h	Extended Hardware Cursor Color 0 Green Register
16h	Extended Hardware Cursor Color 0 Blue Register
17h	Extended Hardware Cursor Color 1 Red Register
18h	Extended Hardware Cursor Color 1 Green Register
19h	Extended Hardware Cursor Color 1 Blue Register
1Ah	Extended Hardware Cursor Horizontal Start Register 0
1Bh	Extended Hardware Cursor Horizontal Start Register 1
1Ch	Extended Hardware Cursor Horizontal Preset Register
1Dh	Extended Hardware Cursor Vertical Start Register 0
1Eh	Extended Hardware Cursor Vertical Start Register 1
1Fh	Extended Hardware Cursor Vertical Preset Register
20h	Extended Linear Addressing Base Address Register 0
21h	Extended Linear Addressing Base Address Register 1
22h	Extended Standby/Suspend Timer Register
23h	Extended Misc. Control Register 2
24h	Extended Scratch Register 2
25h	Extended Scratch Register 3

26h	Extended Graphic Engine Register 0
27h	Extended Graphic Engine Register 1
28h	Extended Internal Memory Clock Register 0
29h	Extended Internal Memory Clock Register 1
2Ah	Extended Internal Video Clock Register 0
2Bh	Extended Internal Video Clock Register 1
2Ch	Extended Software Command Queue Base Address 0
2Dh	Extended Software Command Queue Base Address 1
2Eh	Extended Software Command Queue Base Address 2
2Fh	Extended DRAM Row-Repair Table Register

5.7.1 SR5: Extended Password/Identification Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 05h
Default: 00h

D[7:0] Password/Identification Bit[7:0]
If 86h is written into this register, then A1h will be read from this register , and unlock all the extension registers.
If the value other than 86h is written into this register, then 21h will be read from this register, and lock all the extension registers.

5.7.2 SR6: Extended Graphics Mode Control Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 06h
Default: 00h

D7 Graphic mode linear addressing enable
0: Disable
1: Enable

D6 Graphic mode hardware cursor display enable
0: Disable
1: Enable

D5 Graphic mode interlaced enable
0: Disable
1: Enable

D4	True-Color graphic mode enable
	0: Disable
	1: Enable
D3	64K-Color graphic mode enable
	0: Disable
	1: Enable
D2	32K-Color graphic mode enable
	0: Disable
	1: Enable
D1	Enhanced graphic mode enable
	0: Disable
	1: Enable
D0	Enhanced text mode enable
	0: Disable
	1: Enable

5.7.3 SR7: Extended External Video Frequency Select Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 07h
Default: 00h

D[7:6]	Reserved
D5	Internal RAMDAC operation
	0: Low Speed mode (low power consumption)
	1: High Speed mode
D4	External video clock frequency divide by 2
	0: Disable
	1: Enable
D[3:0]	External video clock frequency selection Bits[3:0]

5.7.4 SR8: Extended CRT/CPU Threshold Control Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 08h
Default: 00h

D[7:4]	CRT/CPU Arbitration Threshold Low Bit[3:0]
D[3:0]	CRT/Engine Threshold High Bit[3:0]

5.7.5 SR9: Extended CRT/CPU Threshold Control Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 09h
Default: 00h

D[7:4]	ASCII/Attribute Threshold Bit[3:0]
D[3:0]	CRT/CPU Threshold High Bit[3:0]

5.7.6 SRA: Extended CRT Overflow Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Ah
Default: 00h

D[7:4]	Extended Screen Offset Bit[11:8]
D3	Extended Vertical Retrace Start Bit[10]
D2	Extended Vertical Blank Start Bit[10]
D1	Extended Vertical Display Enable End Bit[10]
D0	Extended Vertical Total Bit[10]

5.7.7 SRB: Extended Misc. Control Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Bh
Default: 00h

D7 True-Color Graphic mode RGB Sequence Selection
- 0: Red, Green, and Blue in byte order
- 1: Blue, Green, and Red in byte order

D[6:5] Memory-mapped I/O Space Selection Bit[1:0]
- 00: Disable
- 01: Select Axxxxh as Memory-mapped I/O Space
- 10: Select Bxxxxh as Memory-mapped I/O Space
- 11: Select Bxxxxh as Memory-mapped I/O Space

D4 True-Color frame rate modulation enable
- 0: Disable
- 1: Enable

D3 Dual segment register mode enable
- 0: Disable
- 1: Enable

D2 I/O getting enable while write-buffer is not empty
- 0: Disable
- 1: Enable

D1 16-color packed pixel enable
- 0: Disable
- 1: Enable

D0 CPU-driven BITBLT operation enable
- 0: Disable
- 1: Enable

5.7.8 SRC: Extended Misc. Control Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Ch
Default: 00h

D7 Graphic mode 32-bit memory access enable
- 0: Disable
- 1: Enable

D6 Text mode 16-bit memory access enable
- 0: Disable
- 1: Enable

D5 Read-ahead cache operation enable
- 0: Disable
- 1: Enable

D4 Swap CASA- and CASB- signal pin location
- 0: Do not Swap
- 1: Swap

D3 Test mode enable
- 0: Disable
- 1: Enable

D[2:1] Memory Configuration Bit[1:0]
- 00: 1MByte/1 bank
- 01: 2MByte/2 bank
- 10: 4MByte/4 bank
- 11: Invalid

D0 Synchronous reset timing generator enable
- 0: Disable
- 1: Enable

5.7.9 SRD: Extended Configuration Register 0

Register Type: Read Only
Read Port: 3C5, Index 0Dh
Default: 00h

D7 Enable 64K ROM decoding
- 0: Disable
- 1: Enable when MD23 is pulled up with resister.

D6 Clock Generator Selection
- 0: Select External Clock Generator
- 1: Select Internal Clock Generator when MD22 is pulled up with resister.

D5 Disable internal RAMDAC
- 0: Enable
- 1: Disable when MD21 is pulled up with resister.

D4 PCI Function Device Behavior
- 0: Single Function Device
- 1: Multi-Function Device when MD20 is pulled up with resister.

D3 256Kx16 DRAM Type Selection
- 0: 1-WE/2-CAS 256Kx16 DRAM type
- 1: 2-WE/1-CAS 256Kx16 DRAM type when MD19 is pulled up with resister.

D2 Disable BIOS ROM decoding logic
- 0: Enable
- 1: Disable when MD18 is pulled up with resister.

D1 Video subsystem enable/disable at power-on is
- 0: Controlled by System BIOS
- 1: Forced to disable when MD17 is pulled up with resister.

D0 Select I/O address 3C3h or 46E8h as video subsystem port
0: Select 3C3h
1: Select 46E8h when MD16 is pulled up with resister.

5.7.10 SRE: Extended Configuration Register 1

Register Type: Read Only
Read Port: 3C5, Index 0Eh
Default: 00h

D[7:3] Reserved
D[2:0] PCI Function Device Number Bit[2:0] which are configured by whether MD[10:8] are pulled up with resistors (bit = 1) or not (bit = 0)
[000:111] = PCI Function Device Number [0:7] (default = 0)

5.7.11 SRF: Extended Scratch Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Fh
Default: 00h

D[7:0] Reserved for video BIOS

5.7.12 SR10: Extended Scratch Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 10h
Default: 00h

D[7:0] Reserved for video BIOS

5.7.13 SR11: Extended DDC and Power Control Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 11h
Default: 00h

D7 Force VGA into suspend mode
0: Disable
1: Enable
D6 Force VGA into standby mode
0: Disable
1: Enable

D5	Enable video memory access as activation source
	0: Disable
	1: Enable
D4	Enable keyboard and hardware cursor as system activation source
	0: Disable
	1: Enable
D3	Reserved
D2	Row-Repair Table enable
	0: Disable
	1: Enable
D1	DDC DATA Programming
	While writing this bit,
	0: Output '0' logic into DDC Data Signal.
	1: Output '1' logic into DDC Data Signal.
	While reading this bit,
	0: Get '0' logic from DDC Data Signal .
	1: Get '1' logic from DDC Data Signal .
D0	DDC CLK Programming
	While writing this bit,
	0: Output '0' logic into DDC Clock Signal.
	1: Output '1' logic into DDC Clock Signal.
	While reading this bit,
	0: Get '0' logic from DDC Clock Signal .
	1: Get '1' logic from DDC Clock Signal .

5.7.14 SR14: Extended Hardware Cursor Color 0 Red Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 14h
Default: 00h

D[7:6]	Reserved
D[5:0]	Hardware Cursor Color 0 Red Bit[5:0]

5.7.15 SR15: Extended Hardware Cursor Color 0 Green Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 15h

Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Color 0 Green Bit[5:0]

5.7.16 SR16: Extended Hardware Cursor Color 0 Blue Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 16h
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Color 0 Blue Bit[5:0]

5.7.17 SR17: Extended Hardware Cursor Color 1 Red Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 17h
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Color 1 Red Bit[5:0]

5.7.18 SR18: Extended Hardware Cursor Color 1 Green Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 18h
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Color 1 Green Bit[5:0]

5.7.19 SR19: Extended Hardware Cursor Color 1 Blue Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 19h
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Color 1 Blue Bit[5:0]

5.7.20 SR1A: Extended Hardware Cursor Horizontal Start Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Ah

Default: 00h

D[7:0] Hardware Cursor Horizontal Start Bit[7:0]

5.7.21 SR1B: Extended Hardware Cursor Horizontal Start Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Bh
Default: 00h

D[7:3] Reserved
D[2:0] Hardware Cursor Horizontal Start Bit[10:8]

5.7.22 SR1C: Extended Hardware Cursor Horizontal Preset Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Ch
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Horizontal Preset Bit[5:0]

5.7.23 SR1D: Extended Hardware Cursor Vertical Start Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Dh
Default: 00h

D[7:0] Hardware Cursor Vertical Start Bit[7:0]

5.7.24 SR1E: Extended Hardware Cursor Vertical Start Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Eh
Default: 00h

D[7:4] Hardware Cursor Pattern Select Bit[3:0]
D3 Reserved
D[2:0] Hardware Cursor Vertical Start Bit[10:8]

5.7.25 SR1F: Extended Hardware Cursor Vertical Preset Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Fh
Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Vertical Preset Bit[5:0]

5.7.26 SR20: Extended Linear Addressing Base Address Register 0

Register Type: Read/Write

Read/Write Port: 3C5, Index 20h

Default: 00h

D[7:0] Linear Addressing Base Address Bit[26:19]

5.7.27 SR21: Extended Linear Addressing Base Address Register 1

Register Type: Read/Write

Read/Write Port: 3C5, Index 21h

Default: 00h

D7 Reserved

D[6:5] Linear Addressing Space Aperture Bit[1:0]

00: 512KByte

01: 1MByte

10: 2MByte

11: 4MByte

D[4:0] Linear Addressing Base Address Bit[31:27]

5.7.28 SR22: Extended Standby/Suspend Timer Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 22h

Default: 00h

D[7:4] Suspend Timer Bit[3:0]

The resolution for Suspend Timer is 2 minutes.

D[3:0] Standby Timer Bit[3:0]

The resolution for Standby Timer is 2 minutes.

5.7.29 SR23: Extended Misc. Control Register 2

Register Type: Read/Write

Read/Write Port: 3C5, Index 23h

Default: 00h

D[7:4] Reserved

D3	Video compatible Hardware Cursor visibility enable
	0: Disable
	1: Enable
D2	86C201C Engine Emulation enable
	0: Enable
	1: Disable
D[1:0]	DRAM Control Signal Delay Compensation Bit[1:0]
	00: Delay 4 ns
	01: Delay 5 ns
	10: Delay 6 ns
	11: Delay 7 ns

5.7.30 SR24: Extended Scratch Register 2

Register Type: Read/Write
Read/Write Port: 3C5, Index 24h
Default: 00h

D[7:0]	Reserved for VGA BIOS

5.7.31 SR25: Extended Scratch Register 3

Register Type: Read/Write
Read/Write Port: 3C5, Index 25h
Default: 00h

D[7:0]	Reserved for VGA BIOS

5.7.32 SR26: Extended Graphic Engine Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 26h
Default: 00h

D7	Reserved
D6	Power-down Internal RAMDAC
	0: Disable
	1: Enable
D5	PCI Burst-Write Mode enable
	0: Disable
	1: Enable

D4	Suspend Software Command Queue
	0: Do not suspend
	1: Suspend
D[3:2]	Software Command Queue Length Bit[1:0]
	00: 32K
	01: 64K
	10: 128K
	11: 256K
D1	Fast DRAM Timing enable
	0: Disable (7 MCLK/DRAM cycle)
	1: Enable (6 MCLK/DRAM cycle)
D0	Swap RASA* and RASB* signal pins
	0: Do not Swap
	1: Swap

5.7.33 SR27: Extended Graphic Engine Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 27h
Default: 00h

D7	Software Command Queue Engine enable
	0: Disable
	1: Enable
D6	Graphic Engine Register Programming enable
	0: Disable
	1: Enable
D[5:4]	Logical Screen Width and Byte-Per-Pixel Select Bit[1:0]
	00 1024, 256 colors or 512, 32k/64k colors
	01 2048, 256 colors or 1024, 32k/64k colors
	10 4096, 256 colors or 2048, 32k/64k colors
	11 invalid
D[3:0]	Extended Screen Start Address Bit[19:16]

5.7.34 SR28: Extended Internal Memory Clock Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 28h
Default: 00h

D[7] MCLK Divider
0: Do not divide
1: Divide by 2
D[6:0] MCLK Numerator Bit[6:0]
[0000000:1111111] = [1:128]

Note: For the operation of internal memory clock generation, please refer to "2.6 Internal Dual-Clock Synthesizer".

5.7.35 SR29: Extended Internal Memory Clock Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 29h
Default: 00h

D7 MCLK VCO Gain
0: Gain for low frequency operation
1: Gain for high frequency operation
D[6:5] MCLK Post-Scale Bit[1:0]
00: Do not scale
01: Scale by 2
10: Scale by 3
11: Scale by 4
D[4:0] MCLK DeNumerator Bit[4:0]
[00000:11111] = [1:32]

Note: For the operation of internal memory clock generation, please refer to "2.6 Internal Dual-Clock Synthesizer".

5.7.36 SR2A: Extended Internal Video Clock Register 0

Register Type: Read/Write
Read/Write Port: 3C5h,Index 2Ah
Default: 00h

D[7] VCLK Divider
0: Do not divide
1: Divide by 2
D[6:0] VCLK Numerator Bit[6:0]
[0000000:1111111] = [1:128]

Note: For the operation of internal video clock generation, please refer to "2.6 Internal Dual-Clock Synthesizer".

5.7.37 SR2B: Extended Internal Video Clock Register 1

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Bh
Default: 00h

D7 VCLK VCO Gain
- 0: Gain for low frequency operation
- 1: Gain for high frequency operation

D[6:5] VCLK Post-Scale Bit[1:0]
- 00: Do not scale
- 01: Scale by 2
- 10: Scale by 3
- 11: Scale by 4

D[4:0] VCLK DeNumerator Bit[4:0]
[00000:11111] = [1:32]

Note: For the operation of internal video clock generation, please refer to "2.6 Internal Dual-Clock Synthesizer".

5.7.38 SR2C: Extended Software Command Queue Base Address 0

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Ch
Default: 00h

D[7:0] Software Command Queue Base Address Bit[11:4]

5.7.39 SR2D: Extended Software Command Queue Base Address 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 2Dh
Default: 00h

D[7:0] Software Command Queue Base Address Bit[19:12]

5.7.40 SR2E: Extended Software Command Queue Base Address 2

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Eh

Default: 00h

D[7:0] Software Command Queue Base Address Bit[27:20]

5.7.41 SR2F: Extended DRAM Row-Repair Table Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 2Fh
Default: 00h

D[7:0] Row Repair Table Entry Bit[7:0]

5.8. Graphic Engine Related Registers

SiS 6202 supports powerful graphic engines to increase the performance. The graphic engines include BitBlt, BitBlt with mask, Color/Font Expansion, Enhance Color/Font Expansion, and Line Drawing.

Since the engine format for line drawing is different from other operations, we would use a separate section to describe that (refer to "5.8.2 Graphic Engine Part II").

The general engine format would be described in the following "5.8.1 Graphic Engine Part I" section.

5.8.1 Graphic Engine Part I

The engine format for Graphic Engine except that Line Drawing is shown in the following table.

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O Address
Reserved	SRC Start Linear Address [21:0]			**8280h**
Reserved	DST Start Linear Address [21:0]			**8284h**
DST Pitch		SRC Pitch		**8288h**
Rectangular Height		Rectangular Width		**828Ch**
FG Rop	FG (Foreground) Color			**8290h**
BG Rop	BG (Background) Color			**8294h**
Mask3	Mask2	Mask1	Mask0	**8298h**
Mask7	Mask6	Mask5	Mask4	**829Ch**
Top Clipping		Left Clipping		**82A0h**
Bottom Clipping		Right Clipping		**82A4h**
Command 1	Command 0	Command Queue Status		**82A8h**
Pattern 3	Pattern 2	Pattern 1	Pattern 0	**82ACh**
Pattern 7	Pattern 6	Pattern 5	Pattern 4	**82B0h**
Pattern 11	Pattern 10	Pattern 9	Pattern 8	**82B4h**
Pattern 15	Pattern 14	Pattern 13	Pattern 12	**82B8h**
Pattern 19	Pattern 18	Pattern 17	Pattern 16	**82BCh**
Pattern 23	Pattern 22	Pattern 21	Pattern 20	**82C0h**
Pattern 27	Pattern 26	Pattern 25	Pattern 24	**82C4h**
Pattern 31	Pattern 30	Pattern 29	Pattern 28	**82C8h**

5.8.1.1 Source Start Linear Address

Register Type: Read/Write
Read/Write Port: 8280h~8283h
Default: 00h

D[31:22]	Reserved
D[21:0]	Source Start Linear Address Bit[21:0]

5.8.1.2 Destination Start Linear Address

Register Type: Read/Write
Read/Write Port: 8284h~8287h
Default: 00h

D[31:22]	Reserved
D[21:0]	Destination Start Linear Address Bit[21:0]

5.8.1.3 Source Pitch

Register Type: Read/Write
Read/Write Port: 8288h~8289h
Default: 00h

D[15:12]	Reserved
D[11:0]	Source Pitch Bit[11:0]

5.8.1.4 Destination Pitch

Register Type: Read/Write
Read/Write Port: 828Ah~828Bh
Default: 00h

D[15:12]	Reserved
D[11:0]	Destination Pitch Bit[11:0]

5.8.1.5 Rectangular Width

Register Type: Read/Write
Read/Write Port: 828Ch~828Dh
Default: 00h

D[15:12]	Reserved
D[11:0]	Destination Rectangular Width Bit[11:0]

5.8.1.6 Rectangular Height

Register Type: Read/Write
Read/Write Port: 828Eh~828Fh
Default: 00h

D[15:12]	Reserved
D[11:0]	Destination Rectangular Height Bit[11:0]

5.8.1.7 Foreground Color

Register Type: Read/Write
Read/Write Port: 8290h~8292h
Default: 00h

D[23:0]	Foreground Color Bit[23:0]

5.8.1.8 FG Rop

Register Type: Read/Write
Read/Write Port: 8293h
Default: 00h

D[7:0]	Foreground Raster Operation Bit[7:0]

5.8.1.9 Background Color

Register Type: Read/Write
Read/Write Port: 8294h~8296h
Default: 00h

D[23:0]	Background Color Bit[23:0]

5.8.1.10 BG Rop

Register Type: Read/Write
Read/Write Port: 8297h
Default: 00h

D[7:0]	Background Raster Operation Bit[7:0]

5.8.1.11 Mono Mask Register

Register Type: Read/Write
Read/Write Port: 8298h~829Fh

Default: 00h

D[63:0] Mono Mask Bit[63:0]

5.8.1.12. Left Clipping

Register Type: Read/Write
Read/Write Port: 82A0h~82A1h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Left Bit[11:0]

5.8.1.13 Top Clipping

Register Type: Read/Write
Read/Write Port: 82A2h~82A3h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Top Bit[11:0]

5.8.1.14 Right Clipping

Register Type: Read/Write
Read/Write Port: 82A4h~82A5h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Right Bit[11:0]

5.8.1.15 Bottom Clipping

Register Type: Read/Write
Read/Write Port: 82A6h~82A7h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Bottom Bit[11:0]

5.8.1.16 Command Queue Status

Register Type: Read/Write
Read/Write Port: 82A8h~82A9h
Default: 00h

If 201C Emulation Mode is enable, then

D[15:5] reserved

D[4:0] Available Command Queue Length Bit[4:0]

If Software Command Queue is enable, then

D[15:0] Head/Tail Index Bit[15:0]

The Head Index is written into this register, and the Tail Index is read from this registers.

5.8.1.17 Command Register 0

Register Type: Read/Write

Read/Write Port: 82AAh

Default: 00h

D7 Rectangular clipping mode
- 0: Clipping internal region
- 1: Clipping external region

D6 Rectangular Clipping Control
- 0: Disable rectangular clipping logic
- 1: Enable rectangular clipping logic

D5 Y direction control
- 0: Y counter decrease
- 1: Y counter increase

D4 X direction control
- 0: X counter decrease
- 1: X counter increase

D[3:2] Pattern select bit 1-0
- 00: From background color registers
- 01: From foreground color registers
- 10: From pattern registers

D[1:0] Source select bit 1-0
- 00: From background color registers
- 01: From foreground color registers
- 10: From video memory

5.8.1.18 Command Register 1

Register Type: Read/Write

Read/Write Port: 82ABh

Default: 00h

D7	Hardware Command Queue status
	0: Hardware Command queue is not empty
	1: Hardware Command queue is empty
D6	Graphic engine status
	0: Graphic engine is idle and Hardware command queue is empty
	1: Graphic engine is busy or Hardware command queue is not empty
D5	Enhanced Color/Font Expansion
	0: Disable enhanced color expansion
	1: Enable enhanced color expansion
D4	Software Command Queue Status
	0: Software Command queue empty
	1: Software Command queue not empty
D3	Line drawing last pixel control
	0: Last pixel will be drawn
	1: Last pixel will not be drawn
D2	Line drawing major axial selection
	0: Y-axial is major
	1: X-axial is major
D[1:0]	Command type select Bit[1:0]
	00: BitBlt
	01: BitBlt with mask
	10: Color/Font expansion
	11: Line drawing

Note: Word_Writing to Command 1 and Command 0, it will automatically initiate graphic engine to execute the specified command.

5.8.1.19 Pattern Register n

Register Type: Read/Write
Read/Write Port: 82ACh-82C8Bh
Default: 00h

D[7:0]	For 256 color mode with BitBlt engine, these registers store the 8x8 color bitmap. For Color-Expansion, these registers store the monochrome bitmap, thus it could expand 256 pixels at a time.

5.8.2 Graphic Engine Part II

The engine format for Line-Drawing is shown in following table.

D[31:24]	D[23:16]	D[15:08]	D[07:00]	IO Address
Reserved		X Start		**8280h**
Reserved		Y Start		**8284h**
Reserved		Reserved		**8288h**
Reserved		Major Axial Pixel Count		**828Ch**
FG Rop	FG (Foreground) Color			**8290h**
BG Rop	BG (Background) Color			**8294h**
K2 Term		K1 Term		**8298h**
Line Style		Error Term		**829Ch**
Top Clipping		Left Clipping		**82A0h**
Bottom Clipping		Right Clipping		**82A4h**
Command/Status		Reserved	Status 0	**82A8h**

5.8.2.1 X Start

Register Type: Read/Write
Read/Write Port: 8280h~8281h
Default: 00h

D[15:12] Reserved
D[11:0] X Start Bit[11:0]

5.8.2.2 Y Start

Register Type: Read/Write
Read/Write Port: 8284h~8285h
Default: 00h

D[15:12] Reserved
D[11:0] Y Start Bit[11:0]

5.8.2.3 Major Axial Pixel Count

Register Type: Read/Write
Read/Write Port: 828Ch~828Dh
Default: 00h

D[15:12] Reserved

D[11:0] Major Axial Pixel Count Bit[11:0]

5.8.2.4 Foreground Color

Register Type: Read/Write
Read/Write Port: 8290h~8292h
Default: 00h

D[23:0] Foreground Color Bit[23:0]

5.8.2.5 FG Rop

Register Type: Read/Write
Read/Write Port: 8293h
Default: 00h

D[7:0] Foreground Raster Operation Bit[7:0]

5.8.2.6 Background Color

Register Type: Read/Write
Read/Write Port: 8294h~8296h
Default: 00h

D[23:0] Background Color Bit[23:0]

5.8.2.7 BG Rop

Register Type: Read/Write
Read/Write Port: 8297h
Default: 00h

D[7:0] Background Raster Operation Bit[7:0]

5.8.2.8 K1 Term

Register Type: Read/Write
Read/Write Port: 8298h~8299h
Default: 00h

D[15:14] Reserved
D[13:0] K1 Term Bit[13:0]

5.8.2.9 K2 Term

Register Type: Read/Write

Read/Write Port: 829Ah~829Bh
Default: 00h

D[15:14] Reserved
D[13:0] K2 Term Bit[13:0]

5.8.2.10 Error Term

Register Type: Read/Write
Read/Write Port: 829Ch~829Dh
Default: 00h

D[15:14] Reserved
D[13:0] Error Term Bit[13:0]

5.8.2.11 Line Style

Register Type: Read/Write
Read/Write Port: 829Eh~829Fh
Default: 00h

D[15:0] Style Pattern Bit[15:0]

5.8.2.12 Left Clipping

Register Type: Read/Write
Read/Write Port: 82A0h~82A1h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Left Bit[11:0]

5.8.2.13 Top Clipping

Register Type: Read/Write
Read/Write Port: 82A2h~82A3h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Top Bit[11:0]

5.8.2.14 Right Clipping

Register Type: Read/Write
Read/Write Port: 82A4h~82A5h

Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Right Bit[11:0]

5.8.2.15 Bottom Clipping

Register Type: Read/Write
Read/Write Port: 82A6h~82A7h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Bottom Bit[11:0]

5.8.2.16 Command Queue Status

Register Type: Read/Write
Read/Write Port: 82A8h~82A9h
Default: 00h

If 201C Emulation Mode is enable, then
D[15:5] reserved
D[4:0] Available Command Queue Length Bit[4:0]

If Software Command Queue is enable, then
D[15:0] Head/Tail Index Bit[15:0]
The Head Index is written into this register, and the Tail Index is read from this registers.

5.8.2.17 Command Register 0

Register Type: Read/Write
Read/Write Port: 82AAh
Default: 00h

D7 Rectangular Clipping Mode
0: Clipping internal region
1: Clipping external region
D6 Rectangular Clipping Control
0: Disable rectangular clipping logic
1: Enable rectangular clipping logic

D5	Y direction control
	0: Y counter decrease
	1: Y counter increase
D4	X direction control
	0: X counter decrease
	1: X counter increase
D[3:2]	Pattern select bit 1-0
	00: From background color registers
	01: From foreground color registers
	10: From pattern registers
D[1:0]	Source select bit 1-0
	00: From background color registers
	01: From foreground color registers
	10: From video memory

5.8.2.18 Command Register 1

Register Type: Read/Write
Read/Write Port: 82ABh
Default: 00h

D7	Hardware Command Queue status
	0: Hardware Command queue is not empty
	1: Hardware Command queue is empty
D6	Graphic engine status
	0: Graphic engine is idle and Hardware command queue is empty
	1: Graphic engine is busy or Hardware command queue is not empty
D5	Enhanced Color/Font Expansion
	0: Disable enhanced color expansion
	1: Enable enhanced color expansion
D4	Software Command Queue Status
	0: Software Command queue empty
	1: Software Command queue not empty
D3	Line drawing last pixel control
	0: Last pixel will be drawn
	1: Last pixel will not be drawn

D2 Line drawing major axial selection
- 0: Y-axial is major
- 1: X-axial is major

D[1:0] Command type select bit 1-0
- 00: Bitblt
- 01: BitBlt with mask
- 10: Color/Font expansion
- 11: Line drawing

Note: Word_writing to Command 1 and Command 0, it will automatically initiate graphic engine to execute the specified command.

5.9 PCI Configuration Registers

5.9.1 Configuration Register 00h

Register Type: Read
Read Port: 0000h
Default: 00021039h

D[31:16] Device ID
SiS 6202 Device ID is 0002h
D[15:0] Vendor ID
SiS Vendor ID is 1039h

5.9.2 Configuration Register 04h

Register Type: Read/Write
Read Port: 0004h
Default: 02000000h

D[26:25] DEVSEL* timing (= 01, Read Only)
00: fast
01: medium (fixed at this value)
10: slow
D5 VGA Palette Snoop
0: Disable
1: Enable
D2 Bus Master
0: Disable
1: Enable
D1 Memory Space
0: Disable
1: Enable
D0 I/O Space
0: Disable
1: Enable

5.9.3 Configuration Register 08h

Register Type: Read
Read Port: 0008h

Default: 03000000h

D[31:8] Class Code (= 030000h)
D[7:0] Revision ID (= 00h)

5.9.4 Configuration Register 30h

Register Type: Read/Write
Read Port: 0030h
Default: 000C0000h

D[31:11] Expansion ROM Base Address
D0 ROM Enable Bit
0: Disable
1: Enable

5.9.5 Configuration Register 3Ch

Register Type: Read/Write
Read Port: 003Ch
Default: 00000109h

D[15:8] Interrupt Pin (= 01h, Read Only)
D[7:0] Interrupt Line (= 09h)

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Ambient operation temperature	0	70	^{0}C
Storage temperature	-40	125	^{0}C
Input voltage	-0.3	5.5	V
Output voltage	-0.5	5.5	V

Note:

Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

6.2 DC Characteristics

T_A = 0 - 70 ^{0}C, V_{DD} = 5 V ± 5 %, GND = 0 V

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{IL}	Input low voltage	-0.5	0.8	V	
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL} = 4.0 mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH} = -1.0 mA
I_{IL}	Input leakage current	-	± 10	uA	
I_{OZ}	Tristate leakage current	-	± 20	uA	0.45 < V_{OUT} < V_{DD}

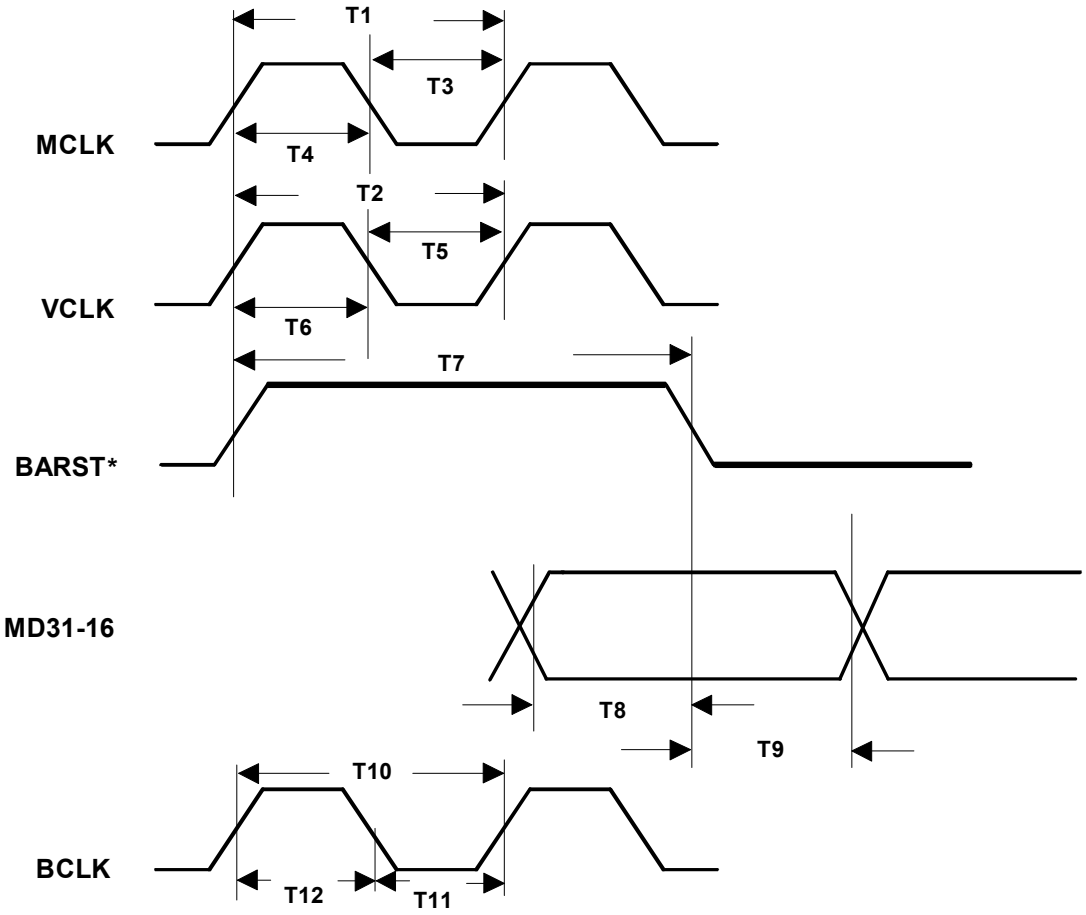
6.3 DC Characteristics for DAC (Analog Output Characteristics)

Description	Min.	Typ.	Max.	Unit
Black Level	-	0	-	V
White Level	-	660	-	mV
ILE	-1.0	-	+1.0	LSB
DLE	-0.5	-	+0.5	LSB
1 LSB	-	2.625	-	mV
Iref	-	8.40	-	mA

6.4 AC Characteristics for DAC (Analog Output Characteristics)

Description	Parameter	Condition	Typ.	Max.	Unit
Settling Time	Tsett	R=37.5 ohm C1=30 pF	-	12.5	ns

6.5 AC Characteristics

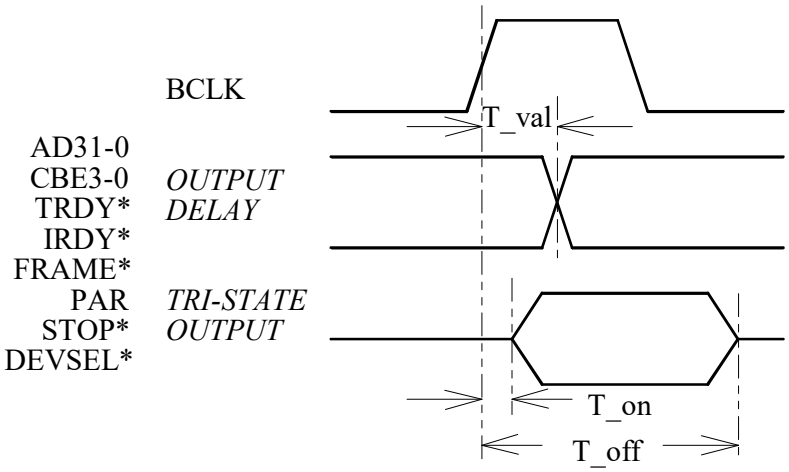


Clock And Reset Cycles

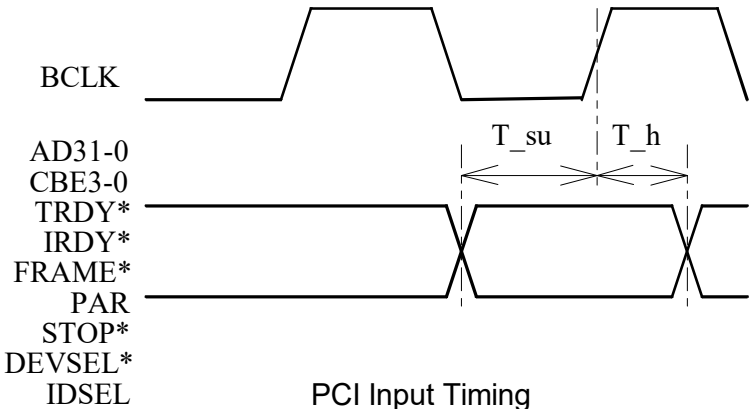
Clock and Reset Timing Table

Symbol	Parameter	Min.	Max.
T_1	MCLK Period	14.3	
T_2	VCLK Period	9	
T_3	MCLK Low Time	6.5	
T_4	MCLK High Time	6.5	
T_5	VCLK Low Time	4	
T_6	VCLK High Time	4	
T_7	Reset High Time	400	
T_8	System Configuration Data Setup Time	20	
T_9	System Configuration Data Hold Time	20	
T_{10}	BCLK Period	30	
T_{11}	BCLK High Time	10	
T_{12}	BCLK Low Time	10	

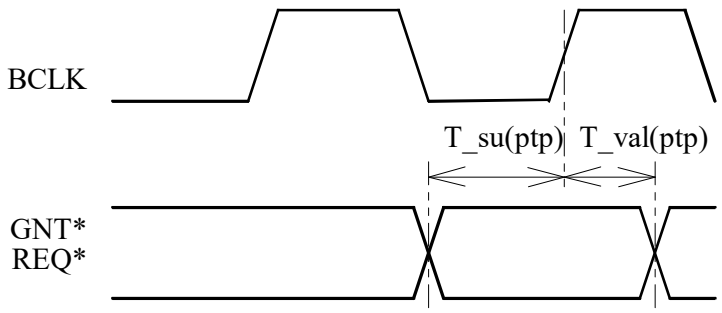
(Units: ns)



PCI Output and Tri-state Timing



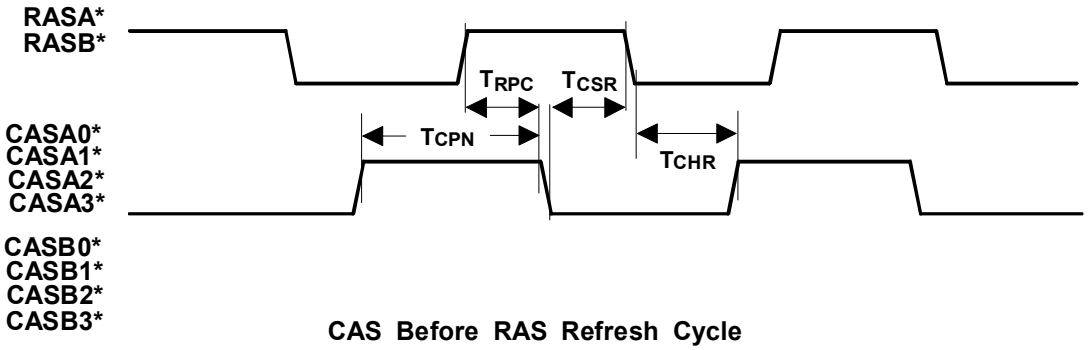
PCI Input Timing



PCI Point to Point Signal Timing

PCI Timing Table

Symbol	Parameter	Min.	Max.	Units
T_{val}	BCLK to Signal Valid Delay	2	11	ns
T_{on}	Float to Active Delay	2	-	ns
T_{off}	Active to Float Delay	-	28	ns
T_{su}	Input Setup Time to BCLK	7	-	ns
T_{h}	Input Hold Time from BCLK	0	-	ns
T_{val} (ptp)	BCLK to Signal Valid Delay - point to point	2	12	ns
T_{su} (ptp)	Input Setup Time to BCLK - point to point	10 (GNT*) 12 (REQ*)	-	ns

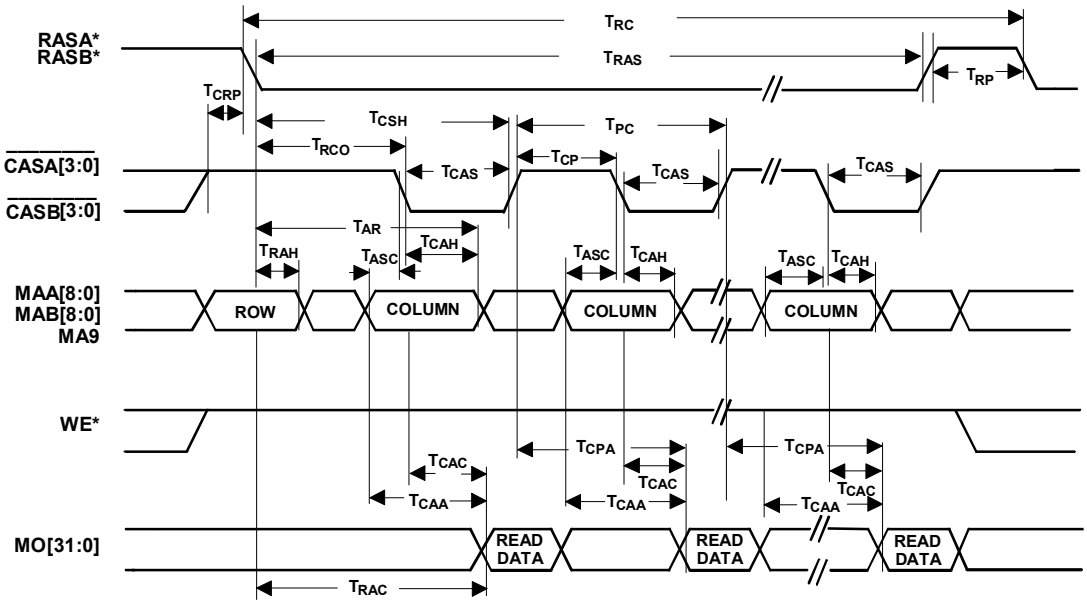


CAS Before RAS Refresh Cycle

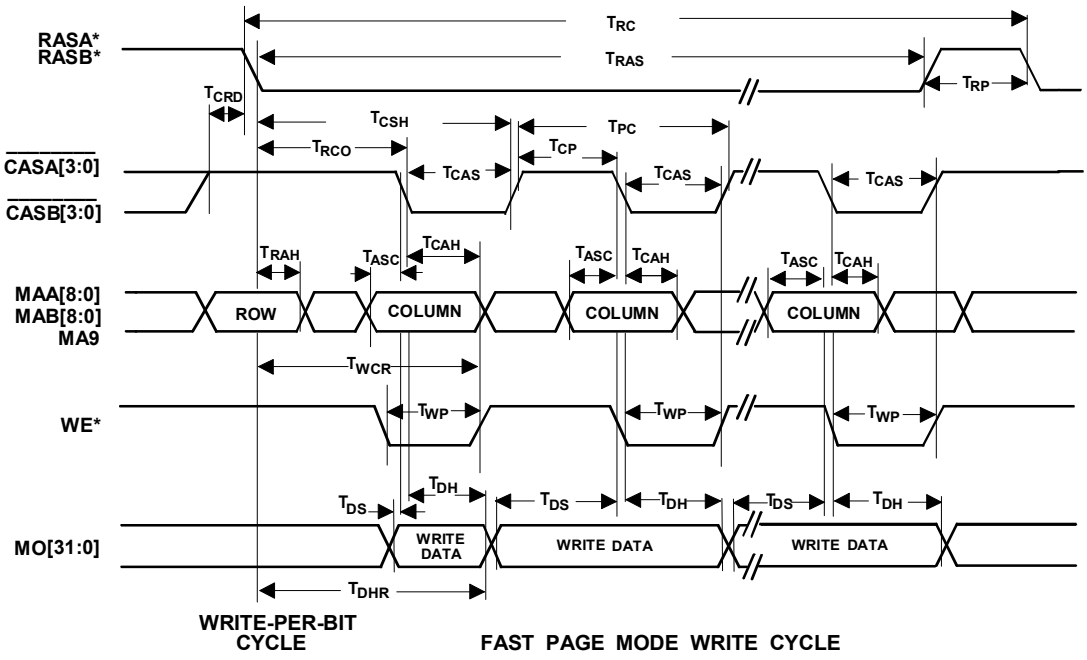
CAS Before RAS Refresh Cycle Timing Table

Sym.	Parameter	T-Value		MCLK 50 MHz		MCLK 60 MHz	
		Min.	Max.	Min.	Max.	Min.	Max.
T_{CPN}	CAS* Precharge Time	1	-	20	-	16.7	-
T_{RPC}	RAS* High to CAS* Low Precharge Time	2	-	40	-	33.4	-
T_{CSR}	CAS* Before RAS* Setup Time	1	-	20	-	16.7	-
T_{CHR}	CAS* Before RAS* Hold Time	3	-	60	-	50.1	-

(Units: ns)



Video Memory Fast Page Mode Read Cycle



Video Memory Fast Page Mode Write Cycle

Video Memory Fast Page Mode Read/Write Cycle Timing Table

Guaranteed Timings

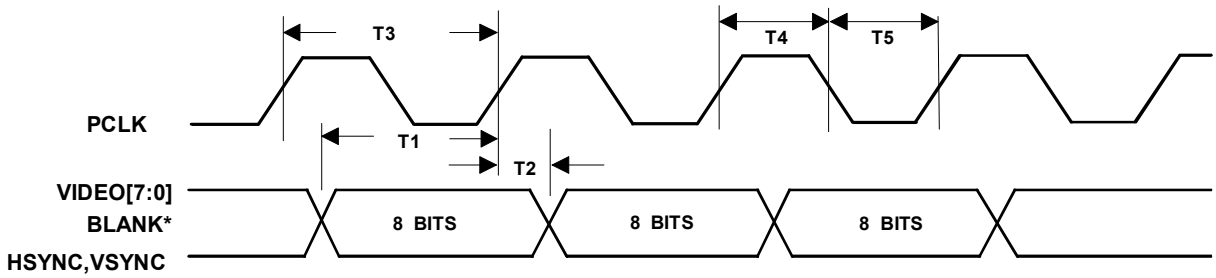
Sym.	Parameter	T-Value		MCLK 50 MHz		MCLK 60 MHz	
		Min.	Max.	Min.	Max.	Min.	Max.
T_{CAS}	CAS* Pulse Width	1	-	20	-	16.7	-
T_{CRP}	CAS* to RAS* Precharge Time	2	-	40	-	33.4	-
T_{CSH}	CAS* Hold Time	4	-	80	-	66.8	-
T_{PC}	CAS* Cycle Time	2	-	40	-	33.4	-
T_{CP}	CAS* Precharge Time	1	-	20	-	16.7	-
T_{RP}	RAS* Precharge Time	3	-	60	-	50.1	-
T_{RC}	RAS* Cycle Time	7	-	140	-	116.9	-
T_{RAS}	RAS* Pulse Width	4	-	80	-	66.8	-
T_{RCD}	RAS* to CAS* Delay Time	3	-	60	-	50.1	-
T_{RAH}	Row Address Hold Time	2	-	40	-	33.4	-
T_{AR}	Column Address Hold From RAS*	4	-	80	-	66.8	-
T_{ASC}	Column Address Setup Time	1	-	20	-	16.7	-
T_{CAH}	Column Address Hold Time	1	-	20	-	16.7	-
T_{WCH}	Write Command Hold Time	1	-	20	-	16.7	-
T_{WCR}	Write Command Hold Referenced to RAS*	3.5	-	70	-	58.5	-
T_{WP}	Write Command Pulse Width	1.5	-	30	-	25.1	-
T_{DS}	Data-in Setup Time	0.5	-	10	-	8.4	-
T_{DH}	Data-in Hold Time	1	-	20	-	16.7	-
T_{DHR}	Data Hold Referenced to RAS*	4	-	80	-	66.8	-

(Units: ns)

Required Timing Table

Sym.	Parameter	T-Value		MCLK 50MHz		MCLK 60MHz	
		Min.	Max.	Min.	Max.	Min.	Max.
T_{CPA}	Data Access Time from CAS* Precharge	-	2	-	40	-	33.3
T_{RAC}	Data Access Time from RAS*	-	4	-	80	-	66.6
T_{CAC}	Data Access Time from CAS*	-	1	-	20	-	33.3
T_{CAA}	Data Access Time form Column Address	-	2	-	40	-	66.6

(Units: ns)



Video Timing 4, 8, 24 Bits/Pixel Modes

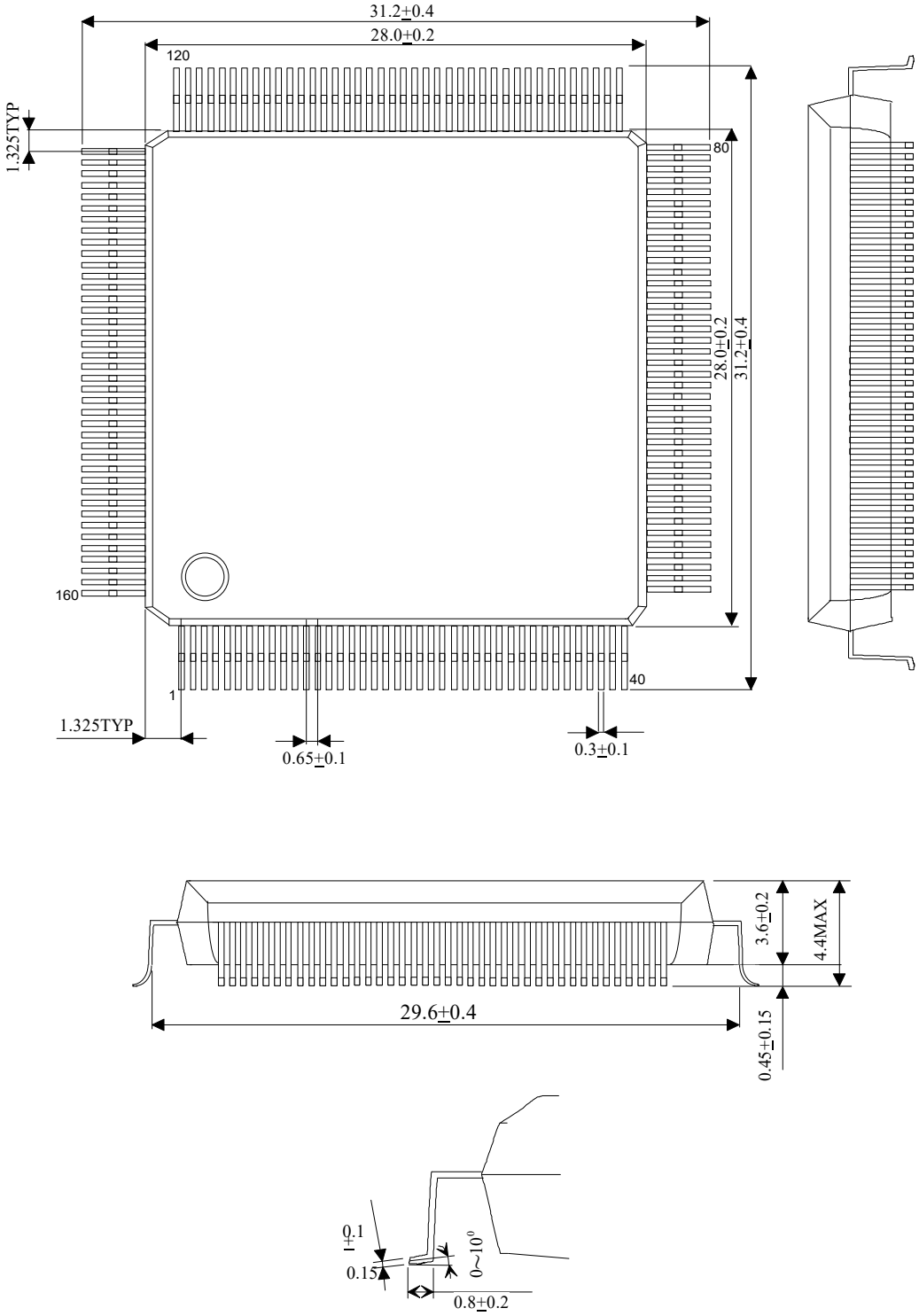
4,8,16 and 24 BPP Video AC Timing Table

Symbol	Parameter	Min.	Max.	Notes
T_1	VIDEO[7:0], BLANK*, SYNC Setup Time	2	-	
T_2	VIDEO[7:0], BLANK*, SYNC Hold Time	2	-	
T_3	PCLK Period	9	-	
T_4	PCLK High Time	4	-	
T_5	PCLK Low Time	4	-	

(Units: ns)

7. Mechanical Dimension

QFP160-P (160-Pin Plastic Flat Package) Unit: mm



Appendix A. Recommended Memory Configuration

A.1.1.1 1M Byte Display Memory Using 256Kx4 DRAM

	U1	U2	U3	U4
RAS*	RASA*	RASA*	RASA*	RASA*
CAS*	CASA0*	CASA0*	CASA1*	CASA1*
WE*	WE*	WE*	WE*	WE*
OE*	OEA*	OEA*	OEA*	OEA*
ADDR	MAA[0:8]	MAA[0:8]	MAA[0:8]	MAA[0:8]
DATA	MD[0:3]	MD[4:7]	MD[8:11]	MD[12:15]
PLANE	0	0	1	1
Bank	0	0	0	0

	U5	U6	U7	U8
RAS*	RASA*	RASA*	RASA*	RASA*
CAS*	CASA2*	CASA2*	CASA3*	CASA3*
WE*	WE*	WE*	WE*	WE*
OE*	OEA*	OEA*	OEA*	OEA*
ADDR	MAA[0:8]	MAA[0:8]	MAA[0:8]	MAA[0:8]
DATA	MD[16:19]	MD[20:23]	MD[24:27]	MD[28:31]
PLANE	2	2	3	3
Bank	0	0	0	0

A.1.1.2 1M Byte Display Memory Using 256Kx4 DRAM

	U1	U2	U3	U4
RAS*	RASA*	RASA*	RASA*	RASA*
CAS*	CASB0*	CASB0*	CASB1*	CASB1*
WE*	WE*	WE*	WE*	WE*
OE*	OEB*	OEB*	OEB*	OEB*
ADDR	MAB[0:8]	MAB[0:8]	MAB[0:8]	MAB[0:8]
DATA	MD[0:3]	MD[4:7]	MD[8:11]	MD[12:15]
PLANE	0	0	1	1
Bank	1	1	1	1

	U5	U6	U7	U8
RAS*	RASA*	RASA*	RASA*	RASA*
CAS*	CASB2*	CASB2*	CASB3*	CASB3*
WE*	WE*	WE*	WE*	WE*
OE*	OEB*	OEB*	OEB*	OEB*
ADDR	MAB[0:8]	MAB[0:8]	MAB[0:8]	MAB[0:8]
DATA	MD[16:19]	MD[20:23]	MD[24:27]	MD[28:31]
PLANE	2	2	3	3
Bank	1	1	1	1

A.1.2.1 1M Byte Display Memory Using 2-CAS 256Kx16 DRAM

	U1	U2
RAS*	RASA*	RASA*
CASU*	CASA1*	CASA3*
CASL*	CASA0*	CASA2*
WE*	WE*	WE*
OE*	OEA*	OEA*
ADDR	MAA[0:8]	MAA[0:8]
DATA	MD[0:15]	MD[16:31]
PLANE	0,1	2,3
Bank	0	0

A.1.2.2 1M Byte Display Memory Using 2-CAS 256Kx16 DRAM

	U1	U2
RAS*	RASA*	RASA*
CASU*	CASB1*	CASB3*
CASL*	CASB0*	CASB2*
WE*	WE*	WE*
OE*	OEB*	OEB*
ADDR	MAB[0:8]	MAB[0:8]
DATA	MD[0:15]	MD[16:31]
PLANE	0,1	2,3
Bank	1	1

A.1.3.1 1M Byte Display Memory Using 2-WE 256Kx16 DRAM

	U1	U2
RAS*	RASA*	RASA*
WEU*	CASA1* (# a)	CASA3* (# a)
WEL*	CASA0* (# a)	CASA2* (# a)
CAS*	OEA* (# b)	OEA* (# b)
OE*	Ground	Ground
ADDR	MAA[0:8]	MAA[0:8]
DATA	MD[0:15]	MD[16:31]
PLANE	0,1	2,3
Bank	0	0

a : CASA*[0:3] pin becomes WEA*[0:3] for dual-WE 256K x 16 Dynamic RAM.
b : OEA* pin becomes CASA* pin for dual-WE 256K x 16 Dynamic RAM.

A.1.3.2 1M Byte Display Memory Using 2-WE 256Kx16 DRAM

	U1	U2
RAS*	RASA*	RASA*
WEU*	CASB1* (# a)	CASB3* (# a)
WEL*	CASB0* (# a)	CASB2* (# a)
CAS*	OEB* (# b)	OEB* (# b)
OE*	Ground	Ground
ADDR	MAB[0:8]	MAB[0:8]
DATA	MD[0:15]	MD[16:31]
PLANE	0,1	2,3
Bank	1	1

a : CASB*[0:3] pin becomes WEB*[0:3] for dual-WE 256K x 16 Dynamic RAM.
b : OEB* pin becomes CASB* pin for dual-WE 256K x 16 Dynamic RAM.

A.2.1 2M Byte Display Memory Using 2-CAS 256Kx16 DRAM

	U1	U2	U3	U4
RAS*	RASA*	RASA*	RASA*	RASA*
CASU*	CASA1*	CASA3*	CASB1*	CASB3*
CASL*	CASA0*	CASA2*	CASB0*	CASB2*
WE*	WE*	WE*	WE*	WE*
OE*	OEA*	OEA*	OEB*	OEB*
ADDR	MAA[0:8]	MAA[0:8]	MAB[0:8]	MAB[0:8]
DATA	MD[0:15]	MD[16:31]	MD[0:15]	MD[16:31]
PLANE	0,1	2,3	0,1	2,3
Bank	0	0	1	1

A.2.2 2M Byte Display Memory Using 2-WE 256Kx16 DRAM

	U1	U2	U3	U4
RAS*	RASA*	RASA*	RASA*	RASA*
WEU*	CASA1* (# a)	CASA3* (# a)	CASB1* (# b)	CASB3* (# b)
WEL*	CASA0* (# a)	CASA2* (# a)	CASB0* (# b)	CASB2* (# b)
CAS*	OEA* (# c)	OEA* (# c)	OEB* (# d)	OEB* (# d)
OE*	Ground	Ground	Ground	Ground
ADDR	MAA[0:8]	MAA[0:8]	MAB[0:8]	MAB[0:8]
DATA	MD[0:15]	MD[16:31]	MD[0:15]	MD[16:31]
PLANE	0,1	2,3	0,1	2,3
Bank	0	0	1	1

a : CASA*[0:3] pin becomes WEA*[0:3] for dual-WE 256K x 16 Dynamic RAM.
b : CASB*[0:3] pin becomes WEB*[0:3] for dual-WE 256K x 16 Dynamic RAM.
c : OEA* pin becomes CASA* pin for dual-WE 256K x 16 Dynamic RAM.
d : OEB* pin becomes CASB* pin for deal-WE 256K x 16 Dynamic RAM.

A.3.1 4M Byte Display Memory Using 2-CAS 256Kx16 DRAM

	U1	U2	U3	U4
RAS*	RASA*	RASA*	RASA*	RASA*
CASU*	CASA1*	CASA3*	CASB1*	CASB3*
CASL*	CASA0*	CASA2*	CASB0*	CASB2*
WE*	WE*	WE*	WE*	WE*
OE*	OEA*	OEA*	OEB*	OEB*
ADDR	MAA[0:8]	MAA[0:8]	MAB[0:8]	MAB[0:8]
DATA	MD[0:15]	MD[16:31]	MD[0:15]	MD[16:31]
PLANE	0,1	2,3	0,1	2,3
Bank	0	0	1	1

	U5	U6	U7	U8
RAS*	RASB*	RASB*	RASB*	RASB*
CASU*	CASA1*	CASA3*	CASB1*	CASB3*
CASL*	CASA0*	CASA2*	CASB0*	CASB2*
WE*	WE*	WE*	WE*	WE*
OE*	OEA*	OEA*	OEB*	OEB*
ADDR	MAA[0:8]	MAA[0:8]	MAB[0:8]	MAB[0:8]
DATA	MD[0:15]	MD[16:31]	MD[0:15]	MD[16:31]
PLANE	0,1	2,3	0,1	2,3
Bank	2	2	3	3

A.3.2 4M Byte Display Memory Using 2-WE 256Kx16 DRAM

	U1	U2	U3	U4
RAS*	RASA*	RASA*	RASA*	RASA*
WEU*	CASA1* (# a)	CASA3* (# a)	CASB1* (# b)	CASB3* (# b)
WEL*	CASA0* (# a)	CASA2* (# a)	CASB0* (# b)	CASB2* (# b)
CAS*	OEA* (# c)	OEA* (# c)	OEB* (# d)	OEB* (# d)
OE*	Ground	Ground	Ground	Ground
ADDR	MAA[0:8]	MAA[0:8]	MAB[0:8]	MAB[0:8]
DATA	MD[0:15]	MD[16:31]	MD[0:15]	MD[16:31]
PLANE	0,1	2,3	0,1	2,3
Bank	0	0	1	1

	U5	U6	U7	U8
RAS*	RASB*	RASB*	RASB*	RASB*
WEU*	CASA1* (# a)	CASA3* (# a)	CASB1* (# b)	CASB3* (# b)
WEL*	CASA0* (# a)	CASA2* (# a)	CASB0* (# b)	CASB2* (# b)
CAS*	OEA* (# c)	OEA* (# c)	OEB* (# d)	OEB* (# d)
OE*	Ground	Ground	Ground	Ground
ADDR	MAA[0:8]	MAA[0:8]	MAB[0:8]	MAB[0:8]
DATA	MD[0:15]	MD[16:31]	MD[0:15]	MD[16:31]
PLANE	0,1	2,3	0,1	2,3
Bank	2	2	3	3

a : CASA*[0:3] pin becomes WEA*[0:3] for dual-WE 256K x 16 Dynamic RAM.
b : CASB*[0:3] pin becomes WEB*[0:3] for dual-WE 256K x 16 Dynamic RAM.
c : OEA* pin becomes CASA* pin for dual-WE 256K x 16 Dynamic RAM.
d : OEB* pin becomes CASB* pin for dual-WE 256K x 16 Dynamic RAM.

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